

Integrating Nano-logic into an Undergraduate Logic Design Course

Saket Srivastava and Sanjukta Bhanja

Electrical Engineering, University of South Florida, Tampa

(ssrivast, bhanja)@eng.usf.edu

Abstract

The goal of this work is to motivate our students and enhance their ability to address newer logic blocks namely majority gates in the existing framework. We use a K-map based methodology to introduce a few novel nano-logic design concepts for the undergraduate Logic Design class. We want them to possess knowledge about a few fundamental abstracted logical behaviors of future nano-devices and their functionality which in turn would motivate them to further investigate these non-CMOS emerging devices, logics and architectures. This would augment critical thinking of the students where they apply the learnt knowledge to a novel/unfamiliar situation. We intend to augment the existing standard EE and CS courses by inserting K-map based knowledge modules on nano-logic structure for stimulating their interest without significant diversion from the course framework. Experiments with our students show that all the students were able to grasp the basic concept of majority logic synthesis and almost 63% of them had a deeper understanding of the synthesis algorithm demonstrated to them.

1. Introduction

With the recent advancement in novel nanotech devices, many efforts are focusing on developing new courses on nanofabrication [2] and even nano-computing. Just like the AND/OR logic in CMOS, other technologies use diverse logic styles. For example, in Quantum-Dot Cellular Automata (QCA), the most optimum designs are those that make use of majority logic. Similarly, while using Single Electron Transistors (SET) and Tunneling Phase Logic (TPL), minority gate logic design is used to implement circuits [1]. Several researches are currently underway on logic level and circuit level designs of these nanotech devices. It is highly likely that in near future our students would have to design circuits using some of nanodevices. Our goal is to augment the existing

courses with flavors of the nanotechnology in a friendly, abstracted manner.

In this work we propose a knowledge module that we have successfully introduced in Digital logic design class. We introduced graphical K-map based majority network realization[1] that were first derived from the SOP expressions and later on we emphasized on creating optimum majority network by using a set of pre-determined graphical libraries. Towards the end we showed the abstracted view of QCA logic and functionality to motivate students into nano-device and nano-computing research. It is clear that at every step, apart from exposing the students towards nanotechnology, our goal has been to enhance their critical thinking by reinforcement of the known idea and synthesis of novel logic structures applying the logic design concepts that they are familiar with.

2. K-map based knowledge module

We introduce this knowledge module right after the students have acquired significant knowledge on logic expression and logic minimization using K-maps.

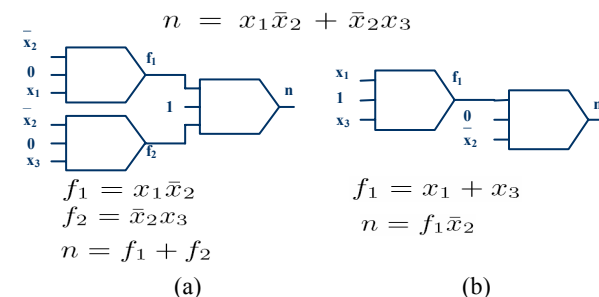


Figure 1. AND/OR mapping of a Boolean Logic function

First, students are explained how a 3-input majority gate can be represented as an AND or OR gate by fixing one of its inputs as a 0 or 1 respectively as shown in Fig 1. In this way students are able to visualize and synthesize small Boolean circuits using majority gate logic just by representing each AND and

OR gate by its equivalent majority gate. Fig. 2 shows QCA implementation [4] for the Boolean expression mapped by AND/OR logic in Fig 1. Also we emphasize that any Boolean function can be implemented by using majority gates and inverters.

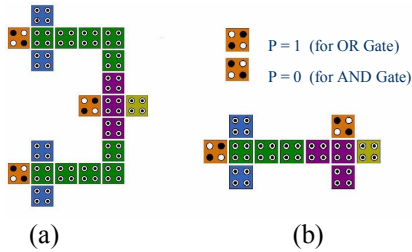


Figure 2. QCA implementation of an AND/OR mapped function shown in Fig. 1

Next, we introduced a low complexity K-map based synthesis method to represent a logic expression in majority gate based logic. For the sake of simplicity, we only reduced logical expression that had at most three inputs. Using [3] it has been proven that any three input logic function f can be represented using a maximum of four majority gates.

$$f(a, b, c) = M(M1, M2, M3)$$

The algorithm was explained using small examples where on a few K-map patterns (out of a library of 38 such choices) were needed for the optimum design. We also explained the generalized algorithm that involved an iterative method to achieve an optimized design. Fig. 3 shows the majority logic schematic and QCA implementation of a Boolean expression that has been derived using the K-map based synthesis algorithm discussed above.

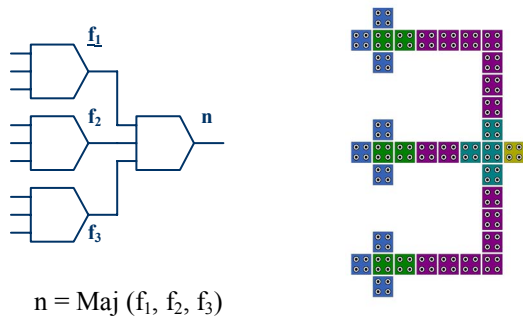


Figure 3. Schematic diagram and QCA implementation of a Boolean expression represented in majority logic.

Finally, we wanted the students to learn about a nano-device implementation that uses majority logic. For this class we used QCA and showed how information can be processed by the mutual interaction

of the neighboring cells without actual transfer of electronic charge.

3. Evaluation

In order to evaluate the level of understanding that students gained from this course module, they were given worksheets for each step. Worksheet-1 evaluated their understanding of QCA majority logic. Worksheet -2 evaluated their level of understanding to perform an AND/OR mapping of simple Boolean expressions. Finally, in worksheet-3, students were asked to perform a K-map based synthesis method to reduce a complex three input logic function. Students were also asked to perform an AND/OR mapping for the same function to understand the advantage of K-map based method over AND/OR mapping method.

In both **worksheet-1** and **worksheet-2**, all the students received grade A or B. In **worksheet-3**, 37.5% students were able to complete each problem, 25% students were able to complete K-map based synthesis but were not able to do the AND/OR mapping for the same.

4. Conclusion

We believe that this module will serve as a good resource for faculties teaching logic design class. The deliverables of this work are the lecture notes, sample student worksheets and feedbacks. In future semesters we also intend to introduce students to other promising nano-logic devices such as SET and TPL and logic associated with them.

[1] Rui Zhang; Gupta, P.; Jha, N.K., "Synthesis of majority and minority networks and its applications to QCA, TPL and SET based nanotechnologies," *18th International Conference on VLSI Design*, vol., no.pp. 229- 234, 3-7 Jan. 2005

[2] Minsu Choi; Park, N., "Teaching nanotechnology by introducing crossbar-based architecture and quantum-dot cellular automata," *Microelectronic Systems Education, 2005. (MSE '05). Proceedings. 2005 IEEE International Conference on*, vol., no.pp. 29- 30, 12-14 June 2005

[3] S. B. Akers, "Synthesis of combinational logic using three-input majority gates," in *Proc. Third Annual Symp. Switching Circuit Theory & Logical Design*, Oct. 1962, pp. 149–157.

[4] "QCADesigner", www.qcadesigner.ca