MASCOT ON-BOARD COMPUTER BASED ON SPACEWIRE LINKS

SpaceWire Onboard Equipment and Software
Long Paper

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ABSTRACT

Aeroflex Gaisler (SE) has together with Pender Electronic Design (CH) and Hirel Design (NL) has under DLR (D) contract and VEGA (D) management developed the Onboard Computer (OBC) engineering model (EM) for the MASCOT asteroid lander.

INTRODUCTION

The general concept of the "Mobile Asteroid Surface Scout" (MASCOT) is to provide a small landing system intended to be deployed from a supporting main spacecraft. It is specifically designed to be compatible with JAXA's Hayabusa 2 (HY2, scheduled for launch in 2014) mission design and the environment given by the target asteroid 1999JU3. The design foresees an OBC for gathering, processing, compressing and storing of the scientific payload and the housekeeping data and to run system and subsystem tasks.

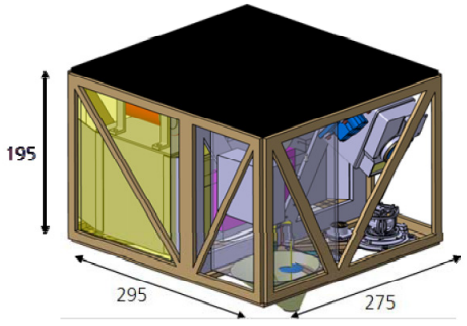

Figure: MASCOT, with dimensions

CONCEPT

The MASCOT OBC comprises two fully redundant CPU and IO boards, where the CPU boards are operated in cold redundancy and the IO boards in hot redundancy.

The MASCOT CPU board is based on the GR712RC device, which is System-on-Chip (SoC) is a dual core LEON3FT system suitable for advanced high reliability space avionics. It is the first of its kind, offering the space community powerful multi-core processor capability in combination with multiple RMAP enabled SpaceWire links fully compliant with ECSS standards. The device is configurable and can operate in many different applications, ranging from platform to payload processing.

The board comprises MRAM, SRAM and optionally SDRAM memory. External LVDS drivers are provided for four SpaceWire links, of which two are used for communication with the nominal and redundant MASCOT IO boards. It includes local voltage regulation is for the processor core voltage, as well as local power down of the analogue acquisition functionality for optimized cold sparing.

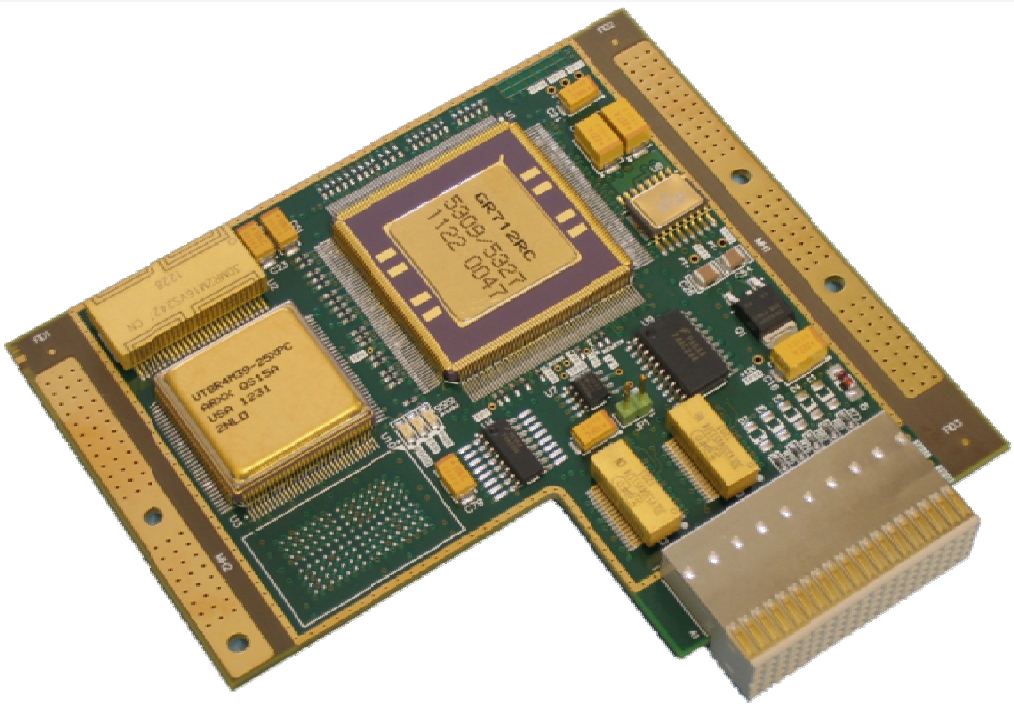

Figure: MASCOT CPU board (based on commercial quality components)

The MASCOT IO board is based on Microsemi RT ProASIC3 FPGA technology. The FPGA implements two SpaceWire links with RMAP target support in hardware. It provides an SPI interface towards a multichannel ADC, control of additional analogue multiplexers, including automatic sequencing for the analogue acquisition, several UARTs with support for large (up to 2KiB) buffers, control of low power commands (LPC) and digital sensor logic (CSM), a parallel interface to a NAND Flash memory which is protected by a Reed-Solomon code, and finally switch over (SO) control logic. The SO logic is in charge of the overall OBC supervision, reconfiguring to the redundant CPU board in case of hardware or software anomaly, independently from the OBC software. All the resource can be accessed from the nominal and the redundant MASCOT CPU board.

Analogue acquisition provides 15 fixed differential analogue acquisition channels (AVM), 12 biased PT1000 acquisitions (TSM) and 4 channels being configurable between AVM and TSM mode. The analogue acquisition system is implemented with additional HW to support an in-orbit SW calibration procedure of offset drifts and SW FDIR detection.

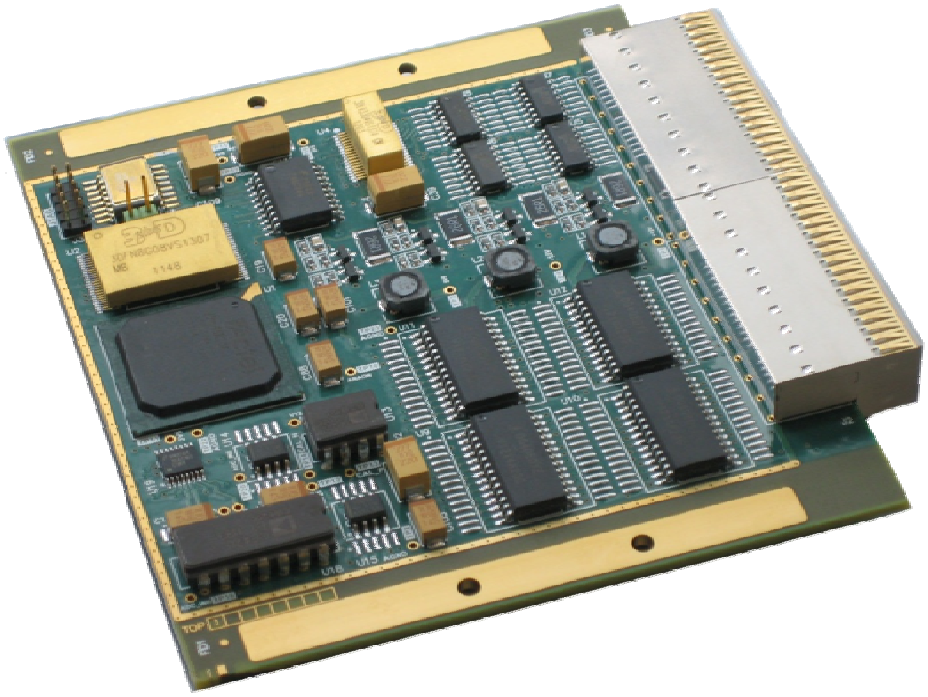

Figure: MASCOT IO board (based on commercial quality components)

The FPGA architecture is based on the on-chip AMBA bus, which is supported both by ESA's and by Aeroflex Gaisler's IP cores. It is therefore a very open architecture into which cores from different sources can be integrated. Aeroflex Gaisler has extended the AMBA on-chip bus with a plug-and-play capability at the IP core level, which can be utilized by software developments tools and device drivers for real-time operating systems, as explained further down. The plug-and-play information on IP core level allows for distributed address decoding, interrupt steering, etc. This enables automatic generation of a table including vendor and device identifier for each core, including version and interrupt information. Software and hardware debuggers can scan the table to install corresponding drivers etc.

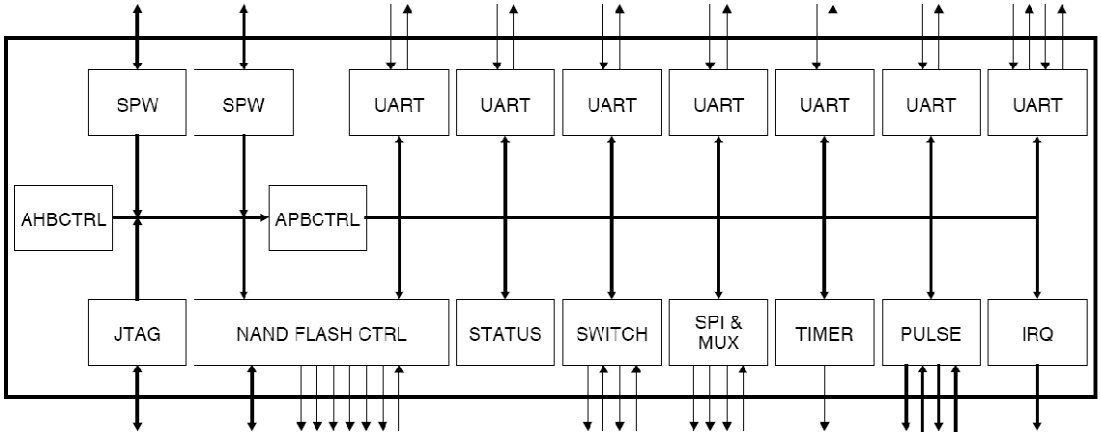

Figure: MASCOT IO FPGA

USE OF SPACEWIRE AND RMAP

Each MASCOT CPU board has four SpaceWire links, of which two are used for communicating with the payload, and two are used for internal communication with the FPGAs on the IO boards. There is thus no direct SpaceWire connection between the two CPU boards.

The communication between processor on the MASCOT CPU board and the FPGA on the MASCOT IO board is done by means of RMAP over the two internal SpaceWire links. Via RMAP read and write commands the device status can be observed and it can be controlled in a safe (verified-write command) and standardized way (ECSS standard).

The processor does not need to implement RMAP in hardware. An RMAP initiator can be any device that can generate standard SpaceWire packets. The RMAP command is just a SpaceWire packet sent from the processor using its SpaceWire core. The RMAP response is just a SpaceWire packet sent from the TC FPGA to the processor. A complete RMAP initiator software stack has been implemented for the RTEMS real-time operating system which has been used to demonstrate the functionality of the system.

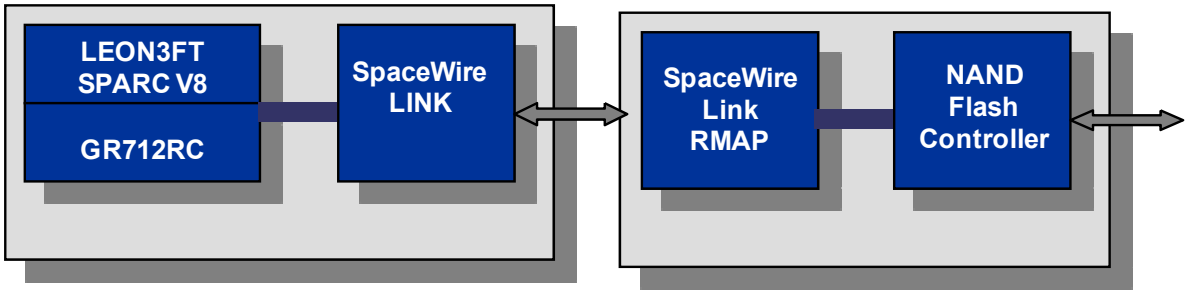

Figure: Illustration of RMAP over SpaceWire

The processors on the CPU boards are connected both the FPGA on the nominal and the redundant IO board. This way the active processor can access all redundant external interfaces and on-board resources such as the NAND Flash memory.

The SpaceWire node in the FPGA has been based on the GRSPW IP core. The core is configured in an RMAP target only configuration, which means that it is not capable of initiating any SpaceWire transmission on its own, with a master interface to the internal AMBA bus in the FPGA.

A possible enhancement of the concept is to replace the two GRSPW IP cores located in the FPGA with a three port SpaceWire router. The router would then have two SpaceWire ports and an internal AMBA master port with a built in RMAP target, thus similar interfaces as used above.

The main difference would be that the routing functionality would allow one processor to access the memory space and the Debug Support Unit of the other processor, via either of the two FPGAs. This will require that both processors are powered. The benefit would be that the active processor could modify the contents of non-volatile memory on the non-active processor, or upload software directly to volatile memory, etc. This remote debug scenario via SpaceWire has previously been demonstrated in an ESA activity.

MASCOT EGSE

The EM verification and software development is performed using the MASCOT EGSE, which is a 19” crate with two internal backplanes, one for power conditioning and distribution, and one hosting two CPU boards and two IO board and also providing all external connectors for interfaces such as SpaceWire, UART, PT1000 elements, JTAG debug etc.

Figure: MASCOT EGSE

USE OF THE OBC EM BOARDS AND EGSE

One of the objectives of the EM boards and EGSE is to support the MASCOT OBC Flight Software (FSW) development, done by VEGA. In this context the EM boards will be integrated in a Software Development and Verification Facility (SDVF), which will provide the I/O acquisition/stimuli, enabling FSW closed loop testing with the OBC Hardware In the Loop (HIL). The SDVF is based on existing ESA SimSat kernel and provides a complete real time simulation environment of the MASCOT subsystems, including the payload SpaceWire links to the OBC. The FSW uses RODOS as RTOS and is developed in C++, applying a tailored version of JSF++ standard.

The OBC EM is also used by DLR for functional system and spacecraft level integration and testing.

CONCLUSION

The current MASCOT OBC engineering model is based on the latest GR712RC dual-core LEON3FT technology with SpaceWire links being used for both internal and external communication, utilizing the RMAP protocol to its full.

The full paper will present the status of the development and report on user feedback received during flight software development, system and spacecraft level integration.