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## Synthesis of Cerium Dioxide High-k Thin Films as a Gate Dielectric in MOS Capacitor

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In the present study, the Al/CeO<sub>2</sub>/p-Si MOS capacitor was fabricated by depositing the Aluminium (Al) metal layer by thermal evaporation technique on sol-gel derived CeO<sub>2</sub> high-k thin films on p-Si substrate. The deposited CeO<sub>2</sub> films were characterized by Ellipsometer to study the refractive index that is determined to be 3.62. The FTIR analysis was carried out to obtain chemical bonding characteristics. Capacitance-voltage measurements of Al/CeO<sub>2</sub>/p-Si MOS capacitor were carried out to determine the dielectric constant, equivalent oxide thickness (EOT) and flat band shift ( $V_{FB}$ ) for the deposited CeO<sub>2</sub> film of 16.22, 1.62 nm and 0.7 V respectively. The conductance voltage curve was used to determine the interface trap density (Dit) at the CeO<sub>2</sub>/p-Si interface that is calculated to be  $1.29 \times 10^{13}$  cm<sup>-2</sup> eV<sup>-1</sup> for measurement frequency of 500 kHz.

Keywords: High-k, CeO<sub>2</sub>, Gate dielectric, Sol-gel, XRD, FTIR.

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# 1. INTRODUCTION

The scaling of devices in current ultra large scale integrated (ULSI) circuits reached to a limit where SiO<sub>2</sub> gate dielectrics has been replaced by alternate high dielectric constant (high-k) oxides in order to overcome the gate delay and other related issues [1-3]. It is clear from the development of high-k materials that only replacing the gate insulator may not be sufficient for device scaling. Hence, the research is focused on developing the novel high-k/metal gate (HK/MG) stacks in order to enhance the performance of the devices. The poly depletion effects and the  $V_t$  pinning at the high-k/polysilicon interface can be eliminated while providing higher channel mobilities by selecting a compatible metal gate electrode with the high-k gate dielectric material [4] by finding dual-band edge metals that are compatible with the high-k dielectric. The high-k materials used in gate stack must have high permeability, thermal stability, good quality of film and interface property, processing and material compatibility with fabrication of CMOS devices and long term reliability [5]. Sol-gel technology allows the deposition of thin films of controlled thickness with the additional advantage that, it is also possible to dope them with a large variety of organic and inorganic compounds, substantially increasing the range of possible applications in many fields of science and technology [6-7]. Stable chemical properties, compatibility with silicon, ease of processing, high oxygen diffusivity and high dielectric constant with low leakage current density make CeO<sub>2</sub> remarkable as gate dielectrics for MOS devices [8, 9, 10], an electrolyte material for integrated solid oxide fuel cells (SOFC) and buffer layers between silicon and other functional ceramics, such as PbTiO3 and Pb (Zr,Ti)O<sub>3</sub> [11]. However, it has been consistently observed that high-k based MOSFETs have problems such as reduced mobility of electronic carriers in the transistor channel, difficulty in setting the threshold voltage for both PMOS and NMOS devices,  $(V_{th})$  instability, and other device reliability problems [12-13]. Further improvement requires a fundamental under-

### 2. METHODS AND MATERIALS

Cerium oxide thin films have been deposited on precleaned p-Si (100) substrates by the Sol-gel spin coating technique wherein, the Cerium (III) chloride heptahydrate is used as a source of Ce with ethanol as a solvent. The citric acid is used to accelerate the rate of reaction. Solution was prepared by using 2.5 g of cerium chloride heptahydrate (make-Himedia) in 30 ml ethanol as solvent, citric acid (Fisher scientific) has been added in dissimilar mole ratios so that transparent deposition soluheptahydrate tions containing cerium chloride (CeCl<sub>3</sub>.7H<sub>2</sub>O) and citric acid in 1:0 and 1:5 mole ratios are prepared by stirring the mixture for half an hour. Prepared solution was used for deposition by spin coating on commercially available pre-cleaned Si (100) wafers, rotated at 5000 rpm for the duration of 30 s and subsequently these spin coated films were annealed for 5 min in an open air electric furnace at 250 °C in air for densification. Deposited films were characterized by ellipsometer (Philips SD-1000), XRD (Rigeku Miniflex) and Fourier transforms infrared spectroscopy (Nicolet 380). The Al/CeO<sub>2</sub>/p-Si MOS capacitor was formed by depositing Aluminium (Al) metal with electrode area of  $3.14 \times 10^{-4}$  cm<sup>2</sup> on the deposited CeO<sub>2</sub> film by the thermal evaporation technique. The back contact was formed by etching the backside native oxide with the help of buffered hydrofluoric acid. Capacitance-Voltage (Agilent 4284A LCR meter) measurement was carried out to investigate the dielectric constant, EOT, flat-band shift etc.

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standing of these phenomena. The MOS capacitor applications using  $CeO_2$  thin films as a high-k oxide, deposited by metal organic decomposition (MOD) on Si, 4H-SiC, GaN have been recently reported by other researchers [14, 15, 16]. In this investigation, the Al / CeO<sub>2</sub> / p-Si MOS capacitors were fabricated by depositing Al on sol gel deposited CeO<sub>2</sub> thin films. The expe-rimental work carried out for CeO<sub>2</sub> thin films deposition is described in second part of the paper. The results are discussed in third part and the fourth part concludes the paper.

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## 3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 Fourier-transform infrared spectroscopy (FTIR)



**Fig. 1** – FTIR spectra of deposited CeO<sub>2</sub> film

The FTIR analysis was carried out to obtain information about chemical bonding characteristics using the FTIR spectrometer. The Fig. 1 shows the IR spectra of the deposited CeO<sub>2</sub> thin film. The spectrum is shown in range 500-800 cm<sup>-1</sup>. The spectrum shows the existence of Ce oxide phases. The peaks from 500-800 cm<sup>-1</sup> are due to presence of Ce-O bond [17]. In the present spectra of the CeO<sub>2</sub> film, the Si-O band appears at 1050 cm<sup>-1</sup> (not shown in the spectra) the broad O-H bond has been detected at 3402 cm<sup>-1</sup> (not shown in the spectra) may be due to the presence of moisture, however, it can be reduced by annealing the deposited CeO<sub>2</sub> films at higher annealing temperatures.

#### 3.2 Ellipsometer

The deposited films were characterized by Ellipsometer to study the thickness and refractive index profile of the films. The equivalent oxide thickness (EOT) of the deposited film is calculated using the relation EOT =  $(3.9 \times t_{high-k}) / k_{high-k}$ . The effect of variation in mole ratio of citric acid on thickness of deposited CeO<sub>2</sub> film has been observed to be noteworthy and the EOT determined for the deposited  $CeO_2$  thin films is 1.19 and 1.79 nm, for the physical thickness of 4.94 nm and 7.44 nm for 1:1.0 and 1:1.5 molar ratio respectively. The refractive index of the deposited  $CeO_2$  film has been measured using the Ellipsometer at the visible wavelength of 632.8 nm is 3.615. It was studied that solutions containing larger citric acid amount produce thicker films due to citric acid's ability to promote sol's gelation [18]. Citric acid facilitates the dissolution process of cerium chloride in ethanol due to a unidentate complex formation between the cerium cation (Ce<sub>3+</sub>) and the COO- group of citric acid, thereby leading to highly homogeneous and uniform films as reported by A. Verma et al. [19].

### 3.3 XRD

The crystal structure of the film is verified with the X-ray diffraction (XRD); Fig. 2 shows the XRD spectra of  $CeO_2$  film.  $CeO_2$  peaks with JCPDS card no. 81-0792 were detected. Two diffraction peaks, which were as-



cribed to cubic phases of  $CeO_2$ , were detected at (111) and (222). These peaks are in well agreement with the

CeO<sub>2</sub> films deposited by MOD [10].

Fig. 2 – XRD spectra of deposited CeO<sub>2</sub> film

#### 3.4 Capacitance-Voltage (C-V) characteristics

Al/CeO<sub>2</sub>/p-Si MOS capacitor was characterized by the Agilent 4284A LCR meter for the measurements of electrical properties of the fabricated MOS structure. A typical C-V characteristics curve of MOS structure is shown in the Fig. 3. The dielectric constant determined from accumulation capacitance of CV curve, physical thickness of CeO<sub>2</sub> layer and electrode area of  $3.14 \times 10^{-4}$  cm<sup>2</sup> obtained at 500 kHz is 16.22. This k value is lower than the ideal (k = 26) may be due to the growth of low-k interface layer between substrate (p-Si) and high-k (CeO<sub>2</sub>) during annealing in the open air furnace. There is a slight negative shift (0.7-0.8 V) in the flat-band voltage  $(V_{FB})$ , which indicates the presence of positive fixed charges near the CeO<sub>2</sub> / Si interface. The value of interface trap density  $(D_{il})$  is determined from the parallel capacitance conductance model using C-V and conductance- voltage (G-V) curves of Fig. 3 and 4 as previously reported by Khairnar et al. [20].



Fig. 3 - C-V characteristics of the Al/CeO<sub>2</sub>/Si MOS capacitor

The value of Dit for 500 kHz frequency is found to be  $1.29 \times 10^{13}$  cm<sup>-2</sup> eV<sup>-1</sup>. The  $D_{it}$  value obtained in this work is slightly higher as compared with that reported by W.F. Lim et al. [15] for CeO<sub>2</sub> in the range of  $10^{12}$  to



Fig.  $4 - C \cdot V$  characteristics of the Al/CeO<sub>2</sub>/Si MOS capacitor



Fig. 5 - Variation of dielectric constant with measurement frequency

 $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ . The obtained value of  $D_{it}$  can be minimized further by annealing these CeO<sub>2</sub> films at higher

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annealing temperatures. The dependence of the dielectric constant of the deposited films on the measurement frequency is shown in figure 5. It is observed that the dielectric constant decreases with increase in the measurement frequency [11]. This decrease in k value due to the fact that, the dielectric constant is the function of capacitance and capacitance is the function of measurement frequency.

#### 4. CONCLUSIONS

The FTIR spectra clearly show the presence of the CeO<sub>2</sub> film, deposited by sol-gel spin coating technique in the range of 500-800 cm<sup>-1</sup>. The XRD shows the crystalline structure of deposited CeO<sub>2</sub> films. The Dit value results in slight leakage in current but that can be controlled with annealing films at higher temperature. We have determined dielectric constant of 16.22 and EOT of 1.62 nm for the deposited  $CeO_2$  film with 1:1.5 mole ratios. Therefore, based on the aforementioned properties, like higher dielectric constant, the desired structural and compositional properties, the deposited CeO<sub>2</sub> thin film with 1:1.5 mole ratio of cerium chloride heptahydrate citric acid can be a promising alternative highk gate dielectric layer to replace conventional SiO<sub>2</sub> for advanced gate stack in advanced HK/MG stack technology.

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