SINGLE-AMPLIFIER INTEGRATOR-BASED LOW POWER CMOS FILTER FOR VIDEO FREQUENCY APPLICATIONS

Chris Hill, Yichuang Sun, and Hsiao Wei Su***

Department of Electronic, Communication and Electrical Engineering
Faculty of Engineering and Information Sciences
University of Hertfordshire, Hatfield, Herts, AL10 9AB, UK
* Tel: ++44 1707 284196, Fax: ++44 1707 284199, Email: y.sun@herts.ac.uk
** Tel: ++44 1707 285082, Fax: ++44 1707 284199, Email: h.w.1.su@herts.ac.uk

ABSTRACT

This paper describes a new low power fully differential second-order continuous-time low pass filter for use at video frequencies. The filter uses a single active device in combination with MOSFET resistors and grounded capacitors to achieve very low power consumption, small chip area and large dynamic range. The ideal integrator is realised using an internally compensated op-amp consisting of only current mirrors and voltage buffers, whilst the lossy integrator is implemented by a single passive RC circuit. The filter has been simulated using a CMOS process. Results show that with a single 5V power supply, cut-off frequency can be tuned from 3.5MHz to 8MHz, dynamic range is better than 67dB, and power consumption is less than 1.7mW.

1. INTRODUCTION

In recent years continuous-time filters have played an increasingly important role in low power high frequency signal processing applications. Analogue filters often have much lower power consumption and require less chip area than a digital filter with the same characteristics. One approach to analogue filter design which is particularly well established is the MOSFET-C filters [1, 2]. MOSFET-C filters generally use op-amps embedded in RC circuits. This limits the high frequency performance of the circuit to at best 1/10 of the bandwidth of the op-amp. Recent attempts to overcome this problem include the use of a BiCMOS process to produce an op-amp with a very large bandwidth [3], and use of alternative active elements such as a current conveyor [4]. So far in most continuous-time filter designs, multiple active devices have been used. This has limited the performance of power consumption and chip size and may not be suitable for application in stringent portable equipment. This paper presents a design which takes advantage of the frequency response of an internally compensated op-amp to produce an integrator in a manner similar to that used in active-R filters [5]. To achieve low power consumption, small chip area and large dynamic range, only one amplifier is used for the second-order filter and the lossy integrator is realized using a simple MOSFET-C circuit. Compared with traditional two integrator loop filter designs that use at least two op-amps, the new realisation requires only one op-amp. The filter is different from traditional single op-amp filters in that it is integrator based. It also differs from active-R filters since it uses the capacitor for the lossy integrator. The op-amp consists of only voltage buffers and current mirrors, thus simplifying the design and aiding integration. The primary aims in the design of the filter are summarised below:

i) Power consumption as low as possible.
ii) Design readily adaptable to integration: The design should have few or preferably no resistors; small capacitors, ideally grounded in order to minimise the effects of parasitics; and chip area should be kept to a minimum.
iii) Total harmonic distortion below 1%.
iv) Dynamic range greater than 60dB.
v) Implementation in a CMOS process.
vi) Tuneable cut-off frequency.

The paper is laid out as follows; section 2 discusses filter structures; section 3 examines practical aspects of the design and presents the transistor level design; and simulation results are given in section 4 followed by conclusions in section 5.

2. FILTER STRUCTURE

Figure 1 shows the structure of a commonly used second-order low pass filter [6]. The circuit is comprised of three elements; an integrator, a lossy integrator and a summing junction. If the circuit has unity feedback, the transfer characteristic of the filter can be derived as

$$\frac{V_{O2}(s)}{V_i(s)} = \frac{1}{s^2\tau_1\tau_2 + s\tau_1 + 1} = \frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \quad (1)$$

giving the quality factor

$$Q = (\tau_2/\tau_1)^{1/2} \quad (2)$$

and the cut-off angular frequency

$$\omega_0 = 1/(\tau_1\tau_2)^{1/2} \quad (3)$$

The DC gain of the filter is equal to one. From (3) it can be seen that variation of the cut-off frequency can be achieved by altering the value of the product $\tau_1\tau_2$. However, in order to maintain the Q of the filter at a constant level τ_2/τ_1 must remain a constant, i.e.

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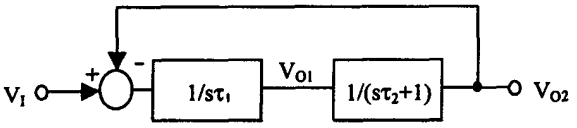

Figure 1. Second-order filter structure.

$$\tau_2/\tau_1 = k \quad (4)$$

This implies that the proportional adjustment must be the same for both time constants. It is also possible to have tuneable Q with fixed ω_0. This can be achieved by changing τ_2 and τ_1 with the same amount but opposite direction.

3. IMPLIMENTATION

Inspection of Figure 1 shows that if a simple MOSFET-C stage is used as the lossy integrator only one active element is required to realise the ideal integrator and summer. The realisation of Figure 1 uses an internally compensated op-amp as the ideal integrator and the lossy integrator is synthesised with a simple RC circuit, as shown in Figure 2. Compared with traditional two integrator loop filter designs that use at least two op-amps, the new realisation requires only one op-amp. It should thus have reduced power consumption, reduced chip size and increased dynamic range. The filter in Figure 2 is different from traditional single op amp filters which use an op-amp embedded in a RC network and are not integrator based. It also differs from active-R filters since it uses the capacitor for the lossy integrator. The op-amp integrator has a differential input and its output impedance is low and not too dependent on frequency. In order to support a fully differential structure and also to minimise the distortion due to the MOSFET resistors [1] the op-amp must have two pairs of differential inputs and a pair of balanced output.

3.1 A 4-input 2-output Op-amp

Any op-amp is essentially a three stage amplifier: a differential input stage which is usually a transconductor; a transimpedance voltage amplification stage, with dominant pole compensation; and a buffer to lower the output impedance. The requirements of this particular design differ from a standard op-amp in two important ways: the input stage must be able to support the entire input voltage without clipping and the gain of the op-amp must be well controlled and tuneable with respect to frequency. The design chosen is shown in Figure 3. The structure is based on a number of interconnected current conveyors, each driving a resistance to control the transconductance of the input stage. In order to aid integration the design uses only two different circuit elements: voltage buffers and current mirrors as shown in Figure 4. Because of the square law nature of the transistors the buffers possess good linearity and a maximum output current four times the bias current, giving good efficiency. In order to improve the output impedance of the current mirrors the output is via cascode transistors M3 which are biased from analogue ground. If the output impedance of the current mirrors and the input impedance of the buffers are both sufficiently high, then the circuit will behave like an ideal integrator and have a transfer characteristic of

$$T_1(s) = g_m/sC_1 \quad (5)$$

where g_m is the transconductance of the input stage given by

$$g_m = 2/(R_1 + 2R_O) \quad (6)$$

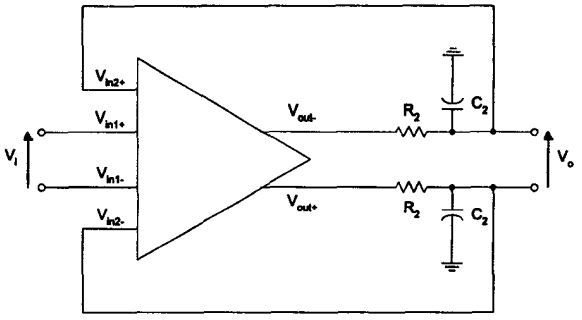

Figure 2. Second order op-amp MOSFET-C filter.

where R_O is the output impedance of the buffers at the input. The output impedance of the buffers is desired to be as low as possible, as the presence of R_O limits the tuning range, especially at low values of R_1. For this reason transistors M3 and M4 are chosen to be quite large. Simulation of this circuit shows R_O to be close to 3.5kΩ. Equation (4) requires that the same degree of tuning is applied to both time constants, i.e., $R_1 = R_2$ and the output impedance of the op-amp should equal $2R_O$. This is achieved by reducing the bias current at the outputs by a factor of four, making the transfer characteristic of the lossy RC integrator

$$T_2(s) = 1/[sC_2(R_2 + 2R_O) + 1] \quad (7)$$

The DC voltage at the output of the op-amp is controlled by a common mode feedback network in order to provide the balanced output necessary to drive the MOSFET resistors. Dimensions for transistors used are given in Table 1.

3.2 Passive Components

The tuning range of the MOSFET resistors is very poor with a 5V power supply, and also conflicts with linear range requirements. This can be increased by adding further transistors in parallel [3]. This technique is illustrated in Figure 5. Each MOSFET has its gate connected to either the tuning voltage, V_{tune}, or to ground effectively removing it from the circuit. This design uses two parallel MOSFETs to give two overlapping tuning ranges, however additional transistors may be added to further increase the tuning range if desired. In order to simplify the design and satisfy the conditions imposed in section 2 the resistors used have

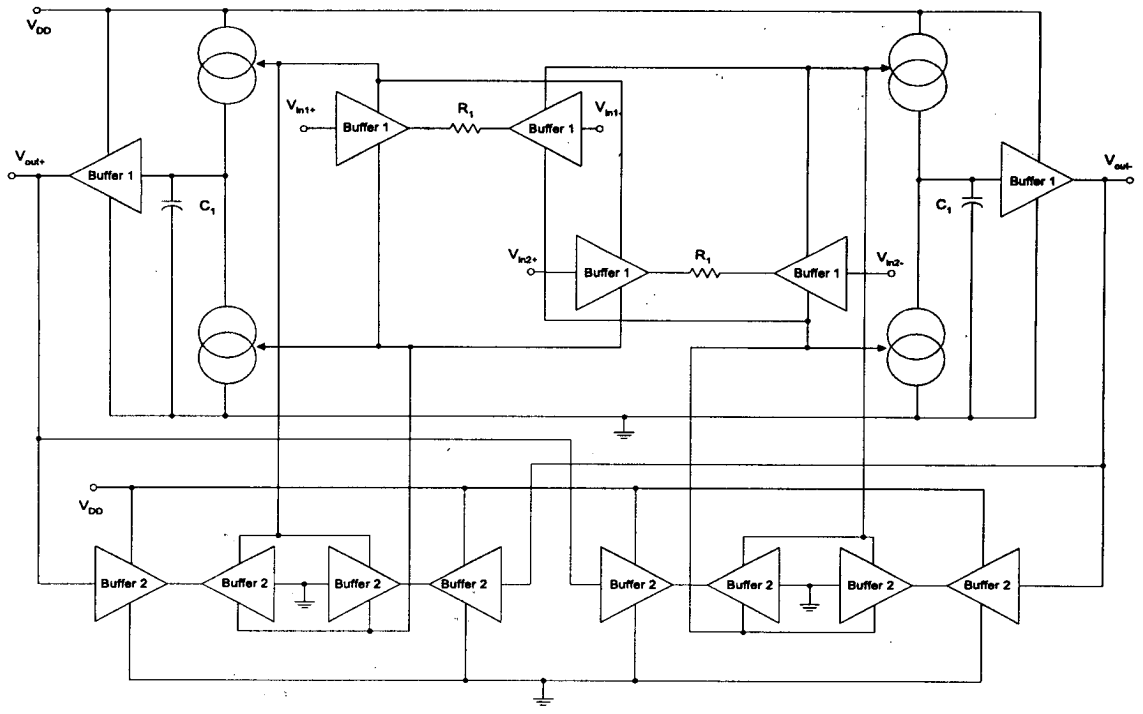

Figure 3. Op-amp structure.

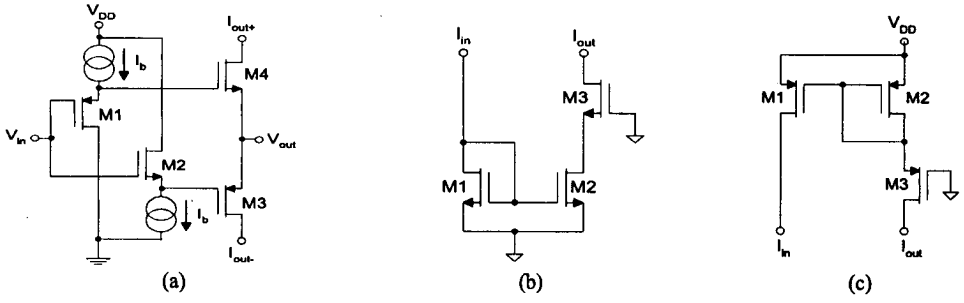

Figure 4. Components of op-amp circuit. (a) Buffer, (b) N-channel mirror, and (c) P-channel mirror.

Table 1. Transistor dimensions and bias currents.

	M1 (μm)	M2 (μm)	M3 (μm)	M4 (μm)	I_b (μA)
Buffer 1	50/2	20/2	100/2	40/2	10 (input stage) 2.5 (output stage)
Buffer 2	12/2	5/2	24/2	10/2	2.5
N-Mirror	50/2	50/2	50/2	-	-
P-Mirror	120/2	120/2	120/2	-	-

identical values for R_1 and R_2. This leads to a convenient 4:1 ratio for C_1 and C_2 to achieve a Butterworth response ($Q = 1/\sqrt{2}$). Values chosen for this filter are 4pF and 1pF respectively. Details of the resistors used are shown in Table 2, together with predicted cut-off frequencies.

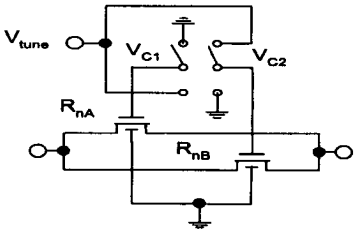

Figure 5. Scheme for extending tuning range of MOSFET resistors.

Table 2. Details of MOSFET resistors and predicted cut-off frequencies.

	Transistor dimensions	Maximum resistance (kΩ)	Minimum resistance (kΩ)	f_0 (MHz)
R_{nA}	2/2	39.2@V_{tune} = 4V	19.2@V_{tune} = 5V	2.4 to 5.9
R_{nB}	3/2	22.5@V_{tune} = 4V	8.2@V_{tune} = 5V	4.1 to 8

4. SIMULATION RESULTS

The filter was simulated using a 2μm CMOS process with k_{on} = 53.6μA/V^2, k_{op} = 21.05μA/V^2, V_{Tn} = 0.855V, and V_{Tp} = -0.8112V. The frequency response of the filter is shown in Figure 6 and details of cut-off frequencies are shown in Table 3. It can be observed that the upper cut-off frequencies match closely that predicted in section 3.3, although the lower cut-off frequencies are slightly higher that expected. It can also be seen that at lower bias voltages the DC gain drops by up to 2.4dB. Both these effects are due to the finite output impedance of the current mirrors limiting the open loop gain of the op-amp. It can be noted that the Q of the circuit is slightly higher than expected, due to excess phase in the integrator. Dynamic range was simulated using the definition of

$$DR = 20\log[V_{max}/(V^2_{ni})^{1/2}] \quad (8)$$

where V_{max} is the input level where THD = 1% and $(V^2_{ni})^{1/2}$ is the mean-square-root input noise integrated over the bandwidth of the circuit. Simulation results show the DR to be in excess of 67dB over the entire tuning range. As expected the DR falls as V_{tune} increases, due to increased linear range and reduced resistance in series with the input. Simulation also shows that power consumption of the filter is less than 1.7mW, which is very low for two pole filters. Distortion performance is shown in Figure 7 as a function of V_{tune} for a 1MHz 500mV_{pk-pk} differential input signal. Results are shown for both tuning ranges. A summary of simulated dynamic range, power consumption and distortion is given in Table 3.

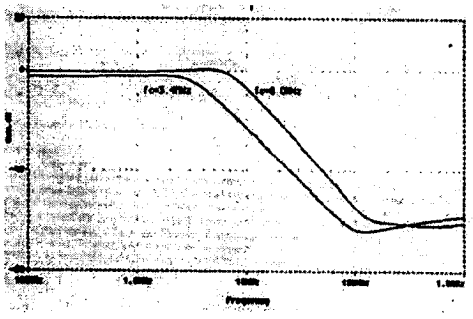

Figure 6. Frequency response of filter (dB), showing the maximum extent of the tuning range.

Table 3. Summary of filter performance.

Tuning voltage	f_0 (MHz)	Dynamic range	Power consumption	THD (%)
$V_{C1} = V_{tune}$, $V_{C2} = 0$	3.4 to 6.2	>67dB	1.68mW	<0.8%
$V_{C1} = 0$, $V_{C2} = V_{tune}$	5.0 to 8.0	>70dB	1.68mW	<0.3%

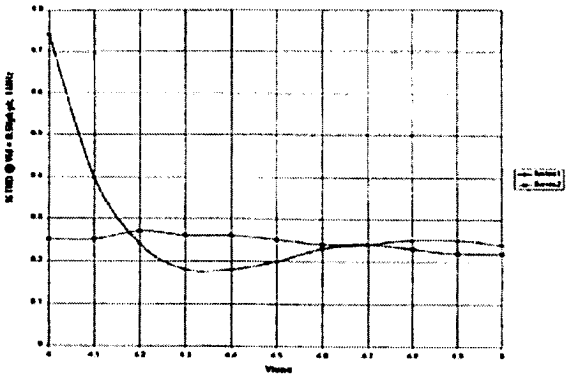

Figure 7. THD (%) as a function of V_{tune} for a 1MHz 500mV_{pk-pk} differential input signal. Series 1 : $V_{C1} = V_{tune}$; V_{C2} = 0V. Series 2 : V_{C1} = 0V; $V_{C2} = V_{tune}$.

5. CONCLUSIONS

Presented in this paper is a differential second order filter suitable for full integration in a standard CMOS process. The filter uses a structure based on MOSFET resistors and a single op-amp in order to reduce the complexity and power consumption of the circuit. The filter contains only grounded capacitors so as to minimise parasitic effects. Even order non-linearities are cancelled by the use of a fully differential structure. Power consumption for the circuit is less than 1.7mW. The filter cut-off frequency can be adjusted over one octave, and the high impedance tuning port eliminates the need for a low impedance tuning voltage. A technique is described which overcomes the inherently poor tuning range of the MOSFET resistors.

6. REFERENCES

[1] M. Banu and Y. P. Tsividis, "Fully integrated active RC filters in MOS technology", IEEE J. Solid State Circuits, Vol. 18, pp. 644-651, Dec. 1983.

[2] Y. P. Tsividis and J. O. Voorman, Eds., *Integrated Continuous-time Filters-Principle, Designs, and Applications*, New York, IEEE Press, 1993.

[3] G. Groenewold, "Low power MOSFET-C 120MHz Bessel allpass filter with extended tuning range", IEE Proc. Circuits, Devices and Systems, Vol. 147, No. 1, pp. 28-34, Feb. 2000.

[4] H. P. Schmid and G. S. Moschytz, "Active MOSFET-C single-amplifier biquadratic filters for video frequencies", IEE Proc. Circuits, Devices and Systems, Vol. 147, No. 1, pp. 35-41, Feb. 2000.

[5] R. Schaumann, M. A. Soderstrand and K. R. Laker, Eds., *Modern Active Filter Design*. New York, IEEE Press, 1981.

[6] T. Deliyannis, Y. Sun, and J. K. Fidler, *Continuos-time Active Filter Design*. CRC Press, Florida, USA, 1999.