A CMOS 80mW 400MHz Seventh-Order MLF FLF Linear Phase Filter with Gain Boost

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Abstract—**A 400MHz CMOS seventh-order linear phase g_m-C filter based on current-mode (CM) follow-the-leader-feedback (FLF) structure is realized. The filter is implemented using a fully-differential linear operational transconductance amplifier (OTA) based on source degeneration topology. PSpice simulations in a standard TSMC 0.18μm CMOS process and with 2.5V power supply have shown that the cut-off frequency of the filter ranges from 290MHz to 430MHz and dynamic range is about 54dB. The group delay ripple is approximately 6% over the whole tuning range and total power consumption is only 78.7mW at 400MHz cut-off frequency.**

I. INTRODUCTION

Integrated continuous-time filters with a few hundred megahertz operating range and low power consumption are widely used in modern hard disk drive (HDD) products [1-3]. Most filters employ ladder or cascade topologies. However, for the HDD design, a certain amount of amplification (boost) at moderate frequencies is also required to achieve sufficient "pulse slimming" to equalize a typical input pulse to the target. The ladder simulation method is not suitable for HDD design, because it can only directly realize transmission zeros on the imaginary axis, and converting the ladder filters into g_m-C filters cost extra amount of power. The cascade topology can realize filters with arbitrary zeros, but the sensitivity is higher, with performance degradation particularly noticeable as filter order increases [4]. One of the solutions proposed for obtaining low passband magnitude sensitivity, non imaginary axis zeros and low power as required is to use multiple loop feedback (MLF) networks.

The MLF g_m-C filters have received world-wide attention since 1990s [5]; all of inverse follow the leader feedback (IFLF), follow the leader feedback (FLF) and leap frog (LF) have been found in literature [5-7]. Among others, the LF structure has attracted most attentions due to better phase responses [8]; therefore, the cut-off frequency has been pushed up to 650MHz. However, it has paid the expense of large amount of power consumption [6]. For the solution of next generation HDD read channels, the power consumption needs to be further reduced. The easiest way to reduce the overall power consumption is using a low order filter to replace the high order filter [2, 3]. However, the overall filter performance is degraded as the filter order decreases. Moreover, using reduced supply voltage can certainly reduce total power consumption of circuits. However, most specifications of a continuous-time filter rely on supply voltage strongly. Especially, the speed of a filter is limited by reduced supply voltage severely. On the other hand, it is such a challenge to design a MLF FLF active filter, although the MLF FLF structure has been used to optimize the filter performance and power consumption for HDD read channels [7]; because they have a main intrinsic drawback in that their global feedback loops introduce hard-to-minimize phase errors, which severely affect the filter group delay responses. Thus we proposed a 0.18μm CMOS 400MHz fully-balanced seventh-order linear phase lowpass filter to balance the power consumption, filter speed, and group delay ripple in this paper, which may become one of the filtering solutions for next generation HDD systems.

The paper is organized in five sections. The design of a fully-balanced four outputs OTA is discussed in Section II. Filter architecture and synthesis are described in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. FULLY–BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The cut-off frequency of continuous-time g_m-C filters can be programmed by controlling the C/g_m time constant. This control can be achieved by varying the g_m value while keeping the capacitance values fixed, or vice versa. In the former, the dynamic range is not dependent on the cut-off frequency value. For this reason, several CMOS transconductors with a programmable g_m value have been developed.

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However, most OTAs reported provide only one or two outputs. The design of multiple output (MO) OTAs has not been well investigated. One MIMO-OTA may perform the functions of multiple SISO-OTAs, but has much fewer components than when the SISO-OTAs are used directly, as some circuits in the SISO-OTAs such as the input stage, output stage, or bias circuit may be shared in the combined MIMO-OTA. The circuit of implementation of the proposed fully symmetric fully balanced multiple output OTA is presented in Figure 1.

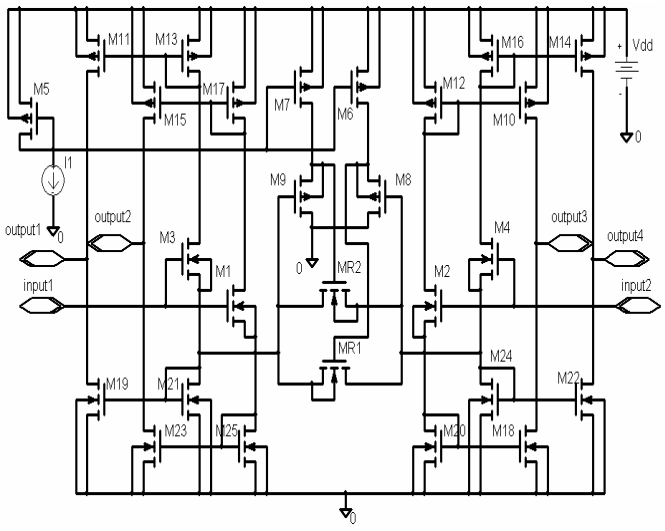

Figure 1 Fully-balanced OTA

The presented structure uses two parallel differential pairs in the input stage. The output stages consist of eight current mirrors. The input stage currents are differentially mirrored through P–type current mirrors $M_{10,12}$ $M_{11,13}$ $M_{14,16}$ $M_{15,17}$ and N–type current mirrors $M_{18,20}$ $M_{19,21}$ $M_{22,24}$ $M_{23,25}$ to the outputs. Assuming matching between transistors, the output differential current $I_{out} = I_{output1} - I_{output4} = I_{output2} - I_{output3}$. The gate voltages of M_{R1} and M_{R2} are connected to the separate source followers M_9 and M_8 biased with a control current I_1, so that both DC level shifts are identical and tuning is obtained via I_1 without disturbing the bias current of the input stage. It is worth mentioning that the geometry of the input devices also affects the DC transconductance value, and these are usually designed to be large in order to improve matching of threshold voltage V_T and K between the transconductance stages. In order to shift the poles to higher frequencies and get the large transconductance the channel length used for these devices is the minimum length allowed by the process. The M_{R1} and M_{R2} are connected in parallel to increase the total transconductance value and therefore the widths of four input stage transistors can be designed quite small, and it can optimize the power consumption, parasitic effects and high frequency response. Neglecting the second order effects, the total drain current of MOS transistors M_{R1} and M_{R2} in triode region is given by, when V_{ds} is much smaller than V_{GS}-V_T:

$$I_{R1,2} = 2K(V_{GS} - V_T)V_{ds} \tag{1}$$

Where $K=0.5\mu_n C_{ox}(W/L)$ is the N–type transconductance parameter. Then:

$$I_{out} = I_{R1,2} - (-I_{R1,2}) = 2I_{R1,2} \tag{2}$$

By substituting (1) into (2) we get:

$$I_{out} = 4K(V_{GS} - V_T)V_{ds} \tag{3}$$

Note that $V_{ds} \approx V_{id}$ when source degeneration is deep. Therefore, we get:

$$I_{out} \approx 4K(V_{GS} - V_T)V_{id} = \frac{V_{id}}{R} = g_m \cdot V_{id} \tag{4}$$

Where $V_{id} = V_{input1} - V_{input2}$, V_{id} is the differential input voltage and g_m is the DC transconductance of the MO–OTA given by:

$$g_m = \frac{1}{R} = 4K \cdot V_B, V_B = V_{GS} - V_T \tag{5}$$

From (4) and (5), we can see that the MO–OTA exhibits a linear V–I characteristic with the assumptions made. However, in practice, second order effects such as body effects, mobility reduction, and channel length modulation will degrade the V–I function of the MO–OTA. Equation (5) shows that the transconductance value can be controlled by varying the bias voltage V_B. The bias voltage V_B can be adjusted by the bias current source I_1. Thus, the allowed values of V_B determine the achievable transconductance tuning range. However, for high frequency applications the second order effects are severe, therefore often in implementation, the bulks/substrates of most transistors in Figure 1 are tied to ground or V_{DD}, apart from the four input stage transistors. For this case, the threshold voltage of $M_{1,3}$, $M_{2,4}$ will be modulated and these results in so called body or threshold modulation effects. The threshold voltage of an NMOS transistor is defined by

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) \tag{6}$$

Where V_{T0} is the threshold voltage with zero bias. γ is the body/bulk polarization factor or bulk threshold parameter and ϕ is the strong inversion surface potential.

With the mentioned threshold modulation effect for Figure 1, using (6) the modified I_{out} can be shown as

$$I'_{out} = g'_m V_{id} \tag{7}$$

Where $g'_m = 4K(V_{GS} - V_{T0} - \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}))$ is the modified DC transconductance of the OTA. Hence, there is an error given by $\Delta V_T = \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$ in g_m'. Thus the bulk effects cause non-linear behaviors in g_m with respect to V_{in}. In practice, thinner gate oxides are recommended to minimize the body effects as γ is decreased

with a smaller oxide thickness at the expense of increased mobility reduction.

The first-order model of mobility reduction or degradation in MOS transistors is given by

$$\mu = \frac{\mu_0}{1+\theta(V_{GS}-V_T)} \tag{8}$$

where μ_o is the zero-field mobility of carriers, $\theta = 1/t_{ox}E_{CR}$ is the coefficient of the effect of the electric field on the mobility, t_{ox} is the gate oxide thickness and E_{CR} is the critical field. In relation to the proposed OTA, the mobility reduction μ causes the transconductance parameter K_n that is μ dependent to change. This in turns causes variation in g_m or I_{out}.

In fact the drain current in a MOS transistor increases slightly as a result of the extension of the depletion layer at the drain into the channel towards the source over a short distance. Thus the channel length is reduced and it is called short channel effect. To characterize this effect, a channel length modulation parameter λ is introduced. The parameter determines the slope of the output characteristic (I_d versus V_{ds}) of a MOS device where V_{ds} is the drain-to-source voltage. The resultant drain current in saturation is thus given by,

$$I_D = K(V_{GS}-V_T)^2(1+\lambda V_{DS}) \tag{9}$$

Thus, the resultant drain current as a result of the short channel effect will cause I_{out} to vary from its ideal expression as given in (4). Note that for short-channel lengths the λ parameter is larger than for long-channel lengths. Thus, λ is critical in deep-submicron. Although using large geometry process can reduce the short channel effects, other performances such as the parasitic effects, power consumption, and speed are degraded. Therefore, there is a tradeoff between transistor sizes.

III. FILTER ARCHITECTURE AND SYNTHESIS

A critical design aspect of filters performing the equalization function is the gain boost capability. Boosting is done to shape the spectrum of the received signal according to the desired equalization of a PRML read channel. This feature is typically realized through two real zeros without changing the group delay response. Several topologies have been proposed to realize these symmetric zeros. Many of them make use of additional circuits (amplifiers, derivators, etc.) that require a large amount of power to keep the parasitic poles out of the band of interest. In the circuit shown in Figure 2, the zeros are realized directly by just adding two extra OTAs.

The normalized characteristic of a current mode seventh–order 0.05° equiripple linear phase lowpass filter with real zeros at the cut–off frequency is given by:

$$H_d(s) = \frac{(s^2-1)}{D(s)} \tag{10}$$

With

$$D(s) = 0.055617s^7 + 0.291094s^6 + 1.095656s^5 + 2.554179s^4 + 4.255922s^3 + 4.676709s^2 + 3.176156s + 1$$

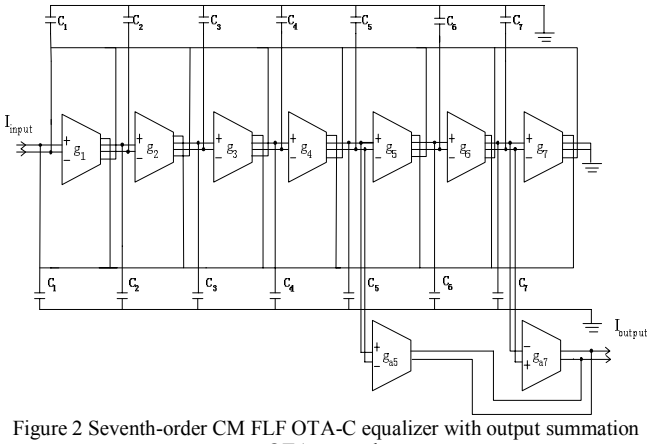

Figure 2 Seventh-order CM FLF OTA-C equalizer with output summation OTA network

The fully–balanced realization of the function in (10) using the CM FLF structure with output summation OTAs is shown in Figure 2. With $\tau_j = c_j/g_j$, $\alpha_j = g_{aj}/g_j$ the overall transfer function of the circuit can be derived as:

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{N(s)}{D(s)} \tag{11}$$

Where

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^7 + \tau_2\tau_3\tau_4\tau_5\tau_6\tau_7 s^6 + \tau_3\tau_4\tau_5 \tau_6\tau_7 s^5 + \tau_4\tau_5\tau_6\tau_7 s^4 + \tau_5\tau_6\tau_7 s^3 + \tau_6\tau_7 s^2 + \tau_7 s + 1$$

$$N(s) = \alpha_5\tau_6\tau_7 - \alpha_7$$

The design formulae for the equalizer can be attained by coefficient matching between (10) and (11) [9, 10].

The resulting pole and zero parameters are:

$$\tau_1 = 0.19106, \tau_2 = 0.26568, \tau_3 = 0.42897, \tau_4 = 0.60015,$$
$$\tau_5 = 0.91002, \tau_6 = 1.47244, \tau_7 = 3.17616, \alpha_5 = 0.213826,$$
$$\alpha_7 = 1$$

The equalizer is designed with identical unit OTAs using the CMOS OTA cell in Figure 1, with selected transconductance g_j of 1.4mS, to improve OTA matching and facilitate design automation. The cut-off frequency of the equalizer is chosen as 400 MHz. Using the computed parameter values, the capacitor values can be calculated, but the parasitic capacitance must also be taken into account. For the circuit of Figure 1, the parasitic capacitance is about 0.15pF. The capacitance values are recalculated below:

$$C_1 = 0.1054\ pF, C_2 = 0.2052\ pF, C_3 = 0.4235\ pF,$$
$$C_4 = 0.6294\ pF, C_5 = 1.0666\ pF, C_6 = 1.8185\ pF,$$
$$C_7 = 4.0963\ pF, g_{a5} = 300\,\mu S, g_{a7} = 1.4mS$$

IV. Simulation Results

The circuit was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18µm CMOS process available from MOSIS [11]. Figure 3 shows the magnitude response of the filter with and without the gain boost. As can be seen from Figure 3, the gain boost of the filter is about 8dB. By varying the bias current I_1 of the unit OTA cell, the tuning range of cut–off frequency without gain boost is 290–430MHz. The total power consumption of the filter is about 78.7mW at 400MHz cut–off frequency for a single 2.5V power supply.

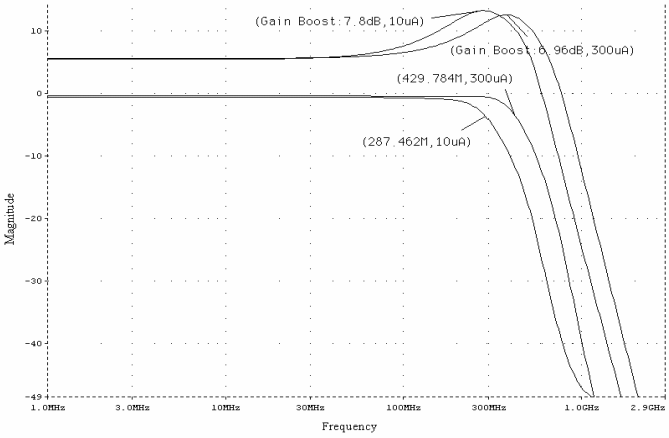

Figure 3 Simulated magnitude response of the filter without and with gain boost

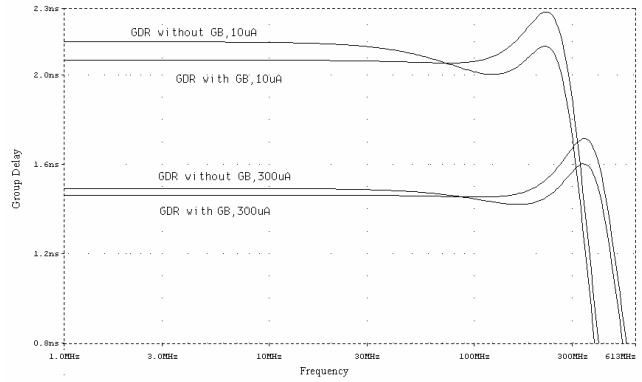

Figure 4 Simulated group delay response at I_1=10µA and I_1=300µA, respectively

The filter phase response is fairly linear, as can be seen from Figure 4. The filter group delay ripple up to cut-off frequency is approximately 6% ±100ps, which is slightly higher than the minimum read channel filter specification (≤5%).This is mainly due to parasitic effects. As we mentioned before, the group delay ripple can be further improved by decreasing the widths of OTA input stage and increasing the widths of OTA output stage, but decreasing the widths of the input stage will reduce the transconductance value and increasing the widths of the output stage will increase power consumption. Therefore, there is a tradeoff between the group delay ripple and power consumption. Simulations of the filter have shown a total harmonic distortion (THD) of less than 1% with a single tone of 400µA at 10MHz. The dynamic range is about 54dB at f_c =400MHz. The total output noise is about 0.6µV/√Hz.

V. Conclusions

A CMOS 400MHz current-mode seventh-order linear phase FLF equalizer has been described. A linear multiple output OTA based on source degeneration topology with a typically large transconductance has been used. Simulation results in 0.18µm CMOS have shown the frequency range of 290-430MHz, gain boost programmable up to 9dB, dynamic range of 54dB, and group delay ripple of 6%, with only 78.7mW power consumption. The power consumption is very low. The group delay ripple is slightly higher than the 5% specification of HDD systems. However, the equalization can be further done by the digital adaptive function. Therefore, the current-mode analogue MLF FLF equalizer may become useful for next generation HDD systems.

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