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Design and validation of key components for the readout electronics of future PET scanners

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SOMMARIO

Il presente lavoro di tesi tratta il progetto e la validazione di due componenti circuitali utilizzati nell'elettronica di lettura di scanner per tomografia a emissione di positroni (PET) per applicazioni biomedicali: un discriminatore a frazione costante (CFD) ed un convertitore tempo-digitale (TDC) CMOS integrato.
Il primo è utilizzato per la lettura di uno scanner PET a due teste precedentemente realizzato dal gruppo di fisica medica presso l'Istituto Nazionale di Fisica Nucleare (INFN) di Pisa per il monitoraggio non invasivo della dose somministrata in adroterapia. L'obiettivo del lavoro è stato l'ottimizzazione del front-end realizzato su PCB in termini di prestazioni temporali al fine di ridurre il tempo morto e la risoluzione del sistema. È stata così realizzata una nuova scheda CFD e le misure sperimentali hanno dimostrato un significativo miglioramento delle caratteristiche temporali che hanno permesso l'acquisizione di dati PET durante l'irraggiamento del fascio, fondamentale per il trattamento in adroterapia.
Il secondo argomento della tesi riguarda il progetto di un TDC CMOS integrato da impiegare nella misura del tempo di volo in un rivelatore PET compatibile con i campi magnetici. Al fine di definire la migliore topologia circuitale, sono stati analizzati diversi fattori derivanti dalle specifiche di progetto, tra i quali la risoluzione temporale, la linearità e il tipo di comunicazione con gli altri elementi del sistema di lettura. Simulazioni eseguite con Cadence e Verilog hanno dimostrato che è possibile ottenere un passo di misura di 100 ps mediante combinazione di una tecnologia sub micrometrica (UMC 65 nm LLLVT) con un approccio sistolico basato su un contatore a 10 bit accoppiato ad una linea ad aggancio di ritardo (DLL) a 4 stadi. Ciò si traduce in una risoluzione nominale di 29 ps. Inoltre, l'uso di una DLL costituita da pochi elementi di ritardo garantisce un comportamento lineare, particolarmente determinante nelle misure di tipo PET. Sebbene in letteratura siano documentate risoluzioni più spinte ottenibili con topologie di TDC differenti, risulta spesso difficile la realizzazione di buone prestazioni sia in termini di risoluzione temporale che di linearità. Il convertitore è anche dotato di un algoritmo di validazione in tempo reale che permette la reiezione degli ingressi di rumore generati dal fotorivelatore senza influire sulla capacità di acquisizione del sistema. È stata, inoltre, progettata una sezione a celle standard che si occupa dell'immagazzinamento dei dati e dell'invio degli stessi alle schede di lettura esterne in forma seriale. Tale stadio fornisce in uscita una parola di 47 bit ad una velocità selezionabile tra 31.25 MHz e 62.5 MHz con una risoluzione di doppio evento pari a 170 ns. A marzo 2013 è stato sottomesso un prototipo ad 8 canali di 1.875 x 1.875 mm^2 al fine di validare i dati simulati con risultati sperimentali.

ABSTRACT

This thesis work discusses the design and validation of two circuit components used in the electronic readout of positron emission tomography (PET) scanners for biomedical applications: a constant fraction discriminator (CFD) and an integrated CMOS time to digital converter (TDC).

The former is used in the read out of a double-head PET scanner already developed by the group of medical physics at INFN Pisa for non-invasive dose delivery monitoring in hadrontherapy. The goal of the work has been the optimization of the front-end PCB in terms of timing performances so as to reduce the dead time and resolution at system level. A new CFD board has been implemented and experimental results have shown a significant enhancement of the timing characteristics which have enabled performing in-beam PET data acquisition which is fundamental in hadrontherapy treatment.

The design of an integrated CMOS TDC to be used for the time of flight measurement in a magnetic field-compatible PET block detector is the second topic of the thesis. The required time resolutions, linear behaviour as well as the communication with other readout elements have been taken into account in the definition of the circuit topology. Cadence and Verilog simulations have shown that a bin size of 100 ps can be obtained with the combination of a submicron technology (UMC 65 nm LLLVT) and a pipeline approach where a 10 bit systolic counter coupled to a 4 stage delay locked loop (DLL) are exploited. This translates into a nominal resolution of 29 ps. In addition, the use of a short DLL leads to a high linearity which is an issue in PET measurements. Despite lower resolutions are obtained in literature with different TDC topologies, achieving good performances in terms of both time resolution and linearity is not straightforward. The converter also features a real-time validation algorithm which is capable to reject noise inputs generated by the photodetector without impairing the acquisition capability of the system. A standard-cell unit has been also designed which is in charge of data buffering and serial communication with external readout boards. A 47 bit output word is provided by the semi-custom stage at a measurement rate which is selectable between 31.25 MHz and 62.5 MHz with a double hit resolution of 170 ns. An 8 channel prototype of 1.875 x 1.875 mm^2 has been submitted in March 2013 in order to validate simulated data with experimental results.

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LIST OF SYMBOLS

ADC	Analogue to Digital Converter
ADDLL	All Digital DLL
ADLL	Array of DLL
APD	Avalanche Photo Diode
ARC CFD	Amplitude and Rise Time Compensation CFD
ARM	Arming Discriminator
ASIC	Application Specific Integrated Circuit
BaF_2	Barium Fluoride
BGO	Bismuth Germanate
BPC	Binary Pulse Counter
CSA	Charge Sensing Amplifier
CSC	Common Systolic Counter
CFA	Current Feedback Amplifier
CFD	Constant Fraction Discriminator
CL-ME	Control Logic for Missed Event
CL-PC	Control Logic for Pulse Count
CL-TOF	Control Logic for TOF
CL-TOT	Control Logic for TOT
CM ASIC	Current Mode ASIC
CsF	Caesium Fluoride
CT	Computed Tomography
CTR-U	Control Unit
D-FF	D-Flip Flop
DAQ	Data Acquisition Board
DHR	Double Hit Resolution
DL	Delay Line
DLL	Delay Locked Loop
DNL	Differential Non Linearity
DOI	Depth Of Interaction
DR	Dynamic Range
FCU	Full Custom Unit
FDG	Fludeoxyglucose
FIFO	First In First Out register
FOV	Field Of View
FPGA	Field Programmable Gate Array
FWHM	Full Width at Half Maximum
GRO	Gated Ring Oscillator
GSO	Gadolinium Silicate
INL	Integral Non Linearity
LaBr3	Lanthanum Bromide
LD	Last Dynode
LED	Leading Edge Discriminator
LOR	Line Of Response
LSB	Least Significant Bit
LSO	Lutetium Oxyorthoslicate

LVDS	Low Voltage Differential Signalling
LYSO	Lutetium Yttrium Oxyorthosilicate
ME	Missed Event
MRI	Magnetic Resonance Imaging
MSB	Most Significant Bit
NaI(Tl)	Thallium-activated Sodium Iodide
NECR	Noise Equivalent Count Rate
NOCG	Non Overlapping Clock Generator
PA-D	Position Amplification and Discriminator
PCB	Printed Circuit Board
PD	Phased Detector
PECL	Positive Emitter Coupled Logic
PET	Positron Emission Tomography
PISO	Parallel Input Serial Output register
PLL	Phased Locked Loop
PLS-C	Pulse-Counter
PMMA	Poly Methyl Methacrylate
PMT	Photo Multiplier Tube
PSP	Pulse Shaping Preamplifier
PVT	Process Voltage Temperature variation
RF	Radio Frequency
RO	Ring Oscillator
RT	Radiation Therapy
SCD	Symmetric Charge Division
SCU	Semi Custom Unit
SF	Scatter Fraction
SFD	Systolic Frequency Divider
SiPM	Silicon Photo Multiplier
SNR	Signal to Noise Ratio
SPAD	Single Photon Avalanche Detector
SPECT	Single Particle Emission Computed Tomography
SPI	Serial Peripheral Interface
SyC	Systolic Counter
TA	Time Amplification
TAC	Time to Amplitude Conversion
TOF	Time Of Flight
TOF-HR	Time Of Flight-Hit Register
TOT	Time Over Threshold
TOT-HR	Time Over Threshold-Hit Register
TWA	Time Window A
TWB	Time Window B
TWS	Time Window Stage
UD-C	Up Down-Counter
UT	Ultra Transmitting
VCBC	Very Coarse Binary Counter
VC-UD	Very Coarse-Updater
VDL	Vernier Delay Line
VFA	Voltage Feedback Amplifier
ZCD	Zero Crossing Discriminator

1. INTRODUCTION

1.1. The role of electronics in medical physics

Medical physics is the combination of applied physics, electronics and computing for the diagnosis and treatment of human disease. The subject is further divided into many branches, including diagnostic radiology, nuclear medicine, which uses radioactive materials for diagnosis of disease, ultrasound, magnetic resonance imaging (MRI) and radiotherapy, which employs radiation to destroy cancerous tissue. All of these applications need or provide an imaging tool for health care. The demand for better image quality entails continuous research to improve instrumentation and techniques. Furthermore, shorter examination times, shift to outpatient testing and non-invasive imaging are required while saving costs. Studies in the fields of detector technologies, circuit design techniques, materials and system approach have led to significant progress in ultrasound, MRI, X-ray, computed tomography (CT) and nuclear medicine. Despite significant differences in the principle of operation, all of these imaging tools require readout electronics, usually referred to as front-end, to perform signal processing such as signal amplification, filtering, multiplexing and analogue to digital conversion [1].
X-ray imaging is based on the analysis of attenuation data of the patient who undergoes the ray exposure. Indeed, since internal organs have different matter composition, they experience different levels of X-ray absorption. This makes it possible to reconstruct a 2D image of the area under investigation. Main drawbacks of this technique are reduced image contrast due to collapsing 3D structures into bi-dimensional images and poor resolution capability in soft tissues given the small differences in attenuation coefficients. A 3D extension of X-ray technology is computer tomography (CT) where a large number of X-ray images is taken at multiple angles so as to elaborate a 3D view of the structures. In general, X-ray detection is based on the use of materials which absorb the incoming radiation and transform the corresponding photon energy into an electrical signal. The latter must be further processed by dedicated electronics in order to be amplified, filtered and then converted into digital form for reconstruction purposes. Most of the improvements in CT have attempted to provide faster acquisition times, better spatial resolution and shorter computer reconstruction times. At the beginning, the use of a single semiconductor CT detector required a single readout channel system. Nowadays, modern X-ray detectors make use of large-scale arrays of active picture elements (pixels) each one to be readout by an independent electronic channel. This solution improves image quality as it concentrates more pixels in a given detector volume. The implementation of such novel layouts has been possible thanks to the technology progress. The use of VLSI electronics along with advanced techniques of IC design makes it possible to integrate a large number of channels within a single chip. Thus, each pixel on the detector array can be readout individually. This leads to good spatial resolution in the final image and large dynamic range. The measurement resolution of the X-ray system strongly depends on the properties of the readout unit, which influences both time and noise profiles of the overall system itself. A primary example of VLSI electronics used for X-ray detection is Medipix which is a CMOS pixel detector readout chip designed to be connected to a segmented semiconductor sensor

[2,3]. One of the main drawbacks of the increasing level of integration between analogue and digital parts in mixed-signal systems is on-chip noise coupling. Noise currents caused by switching digital circuits are spread to the sensitive analogue components via the power distribution network and through the substrate by current injection. This is especially true in radiation pixel detectors where an extreme level of integration is required to read out the array. A dedicated circuit design can improve the noise performance [4]. A further issue in X-ray detection is related to the high count rate of the system. Thus, special attention must be paid in the front-end design in order to maximize the throughput while keeping a high resolution. This problem can be addressed with the use of dedicated strategies in the ASIC design [5]. Area occupancy of readout channels must also be considered in order to accommodate the large number of channels required by novel block layouts. Thus, innovative architectures must be introduced [6]. Finally, image contrast can also be improved by setting an energy window in the low energy range which can be selectable by hardware [7].

As opposed to X-ray imaging which provides morphological information of the body, nuclear medicine techniques inform about the functional activities inside the tissues. Two major imaging modalities can be considered: positron emission tomography (PET) and single particle emission computed tomography (SPECT). In both the two techniques no external radiation is used to scan the object as in X-ray imaging. Instead, radiotracers are injected inside the body and accumulate in the region of interest. Then, radiation is detected to recover the distribution of the isotopes and 2D or 3D images are elaborated through computer analysis. Mapping of emitted radiation is performed either by collimator (SPECT) or by electronic coincidence using two opposite detectors (PET). Currently, almost all commercially available scanners employ scintillation crystals with photodetectors coupled to readout electronics. The latter must measure the photon energy so as to discriminate true events from background and scattered photons. Then, the number of detected photons and the coordinates of each interaction in the detectors are recorded in order to inform about the amount of radiation and the directions of photons' arrivals. Additionally, PET systems record the timing information of photons to detect coincidence pairs. The accuracy and resolution of nuclear imaging tools are severely restricted by both physical effects, such as photon attenuation and scatter, and deficiencies of the equipment which limit the system capability in reconstructing the tracer distribution. As in X-ray technology, reading out the signals from both SPECT and PET sensors requires highly specialized electronics with stringent requirements in terms of signal to noise ratio (SNR), dynamic range, linearity and stability. The use of novel pixelated photodetectors with high rate of events per pixel causes the demand for high density, high rate, multichannel ASICs. Each channel processes the charge signals coming from the associated pixel by performing amplification, filtering, discrimination, measurement and storage. Pixel amplification can be performed by providing either charge to voltage [8], charge to charge or current to current amplification [9]. Shaping is another important step in pixel readout as it limits the bandwidth to maximize SNR and shorten the pulse width to minimize dead time and avoid pile up. Different approaches to implement optimal shapers are reported in literature [10,11]. The last step in the readout chain is the extrapolation of energy and timing information from data. Accurately extracting such information requires employing specialized circuits such as peak detectors and digitizers [12,13].

Magnetic resonance imaging (MRI) is a relatively new medical imaging technique which is able to generate images with excellent soft tissue contrast. It does not use ionizing radiation and therefore is considered safer than CT, PET and SPECT. MRI systems are based on superconducting magnets that produce a highly uniform static field inside a cylindrical bore. Hydrogen nuclei present in biological structures tend to align with the field. This results in a small bulk magnetization which is subsequently tilted from its equilibrium position of alignment; this gives rise to the magnetic resonance phenomenon which consists of the precession of the individual nuclear moments around the field vector. As a consequence of the return to an equilibrium stage, radio-frequency (RF) magnetic fields are generated that can be detected with pickup loop coils. The rates at which the longitudinal and transverse components of the magnetization return to their respective equilibrium values create contrast between different biological tissues. The tilting of the magnetization is provided by the energy of a short, intense pulse of RF magnetic field produced by a large transmission coil. Spatial encoding is performed after the excitation pulse generation by driving time-variant currents in the gradient field coils, during which the RF signal induced by the magnetization in receiver coil is acquired. This measurement procedure can be repeated several times so as to acquire enough data to produce an image [1,14]. The acquisition of signals detected by the receiver coil is performed by the spectrometer, whose function is also to generate the precisely timed gradient and RF pulses that are required to excite and encode spatial information into the nuclear magnetization. Initially, a single receiver coil was used with a size covering the area of interest. The drawback of this approach is that for the large regions positioned far away from the surface, field of the coil is weak and results in a poor SNR. This problem has been overcome by using an array of surface coils whose individual noise is not correlated, thus improving the overall SNR [15]. In these array structures, each resonating loop must be connected to a low-noise preamplifier through a matching network for SNR optimization [16]; moreover, preamplifier decoupling must be implemented in order to avoid coupling among the coil loops [17]. These techniques make it possible the design of coil arrays with a large number of independent channels. In order to exploit the use of such multichannel receivers, new approaches are currently being investigated in order to address issues related to the construction and acquisition of data (i.e., RF interferences among cables and data volume). Advances in semiconductor technology such as photonics, wireless high-speed communications, large-scale integration and MEMS are fundamental for planning new solutions, such as the use of fibre-optic based cabling [18,19], wireless communication [20] and pre-processing hardware [21].

According to what stated so far, it is evident that electronics play a fundamental role in the implementation of imaging tools for medical applications. Indeed, each technique makes use of a transducer apparatus (scintillator plus photodetector in X-ray, CT, PET, SPECT and receiver coil in MRI) which translates physical phenomena into an electrical signal. Therefore, the information required for image reconstruction must be extrapolated by means of signal processing. Improvements in detector layouts and procedures demand for further innovation of readout techniques. Currently, the trend in most of medical imaging fields is shifting from a single large transducer to arrays of small structures which allow for image quality enhancement. It follows that a very small area is available for readout electronics, thus requiring the development of VLSI multichannel front-ends. In this scenario,

main challenges in ASIC design include power limitation, low noise levels, crosstalk prevention and good matching performance among channels. Physicists, engineers and doctors are working together in order to increase medical imaging performances, thus allowing a better quality of life.

1.2. Positron emission tomography

Positron emission tomography is a molecular imaging technique that provides images of physiological processes inside the body. After β^+ decay of a radiotracer injected into the tissues, a positron is released which annihilates with an atomic electron, thus producing two 511 keV photons (*event*). These pairs of gamma rays are emitted in almost exactly opposite directions within the PET scanner. Coincidence detection of the two photons is exploited to provide projection data used for image reconstruction. Production of the radionuclides requires the use of a cyclotron, which must be near the testing centre due to the short half-lives of the radioisotopes.
A PET scanner is made up of an array of detectors surrounding the object to be imaged. Each time a detector is hit by a gamma ray, opposite detectors are checked for detection of a second photon. If this happens within a given coincidence time window (typically ranging from 5 ns up to 10 ns), an event is counted and the straight line connecting the centres of the two detectors, called the line of response (LOR), is created (see figure 1.1).

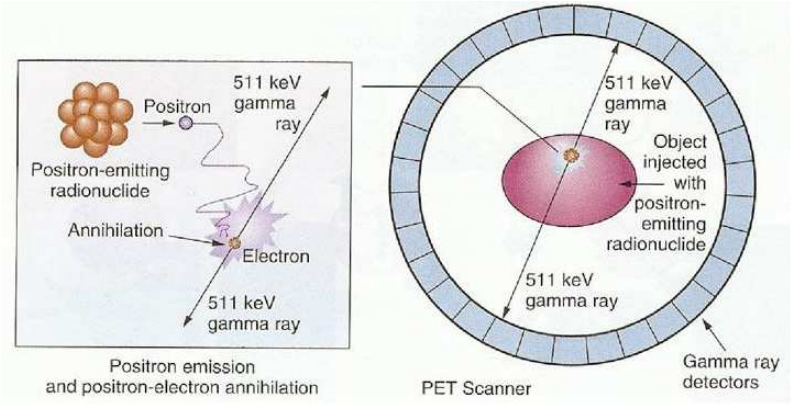


Figure 1.1 – Physical phenomena of annihilation (left) and PET scanner scheme [22].

Each detector element is connected by a coincidence circuit with the time window to a set of n opposite detector elements. The n fan-beam projections available for each detector form an angle of acceptance in the transaxial plane; the angles of acceptance for all detectors in the ring form the transaxial field of view (FOV).
Combining all counts from the detectors produces a single projection; several projections are needed to reconstruct an image of the area of interest. Nowadays, PET cameras consist of a large number of detectors and a real time check of detector pairs is impractical. Instead, each hit is associated to a timestamp and buffered into a digital coincidence processor that compares all data in order to identify true coincidence events. Next, the pulse height of the detected photons is

checked if it is within the pulse energy window set for 511 keV (~20-30% FWHM centred on the 511 keV photopeak) and the position of the LOR is determined by a weighted centroid algorithm to store the event in the computer memory for reconstruction purposes. Data storage should be organized so that the spatial information carried by each LOR is preserved. Two storage methods are available. A first approach is based on binning the acquired data into projection representation of the data also known as sinograms. Events are accumulated into a 3D sinogram array, where each element is identified by a radial position, a transaxial angle and an axial position (with polar angle) with respect to the centre of the scan field [23]. A second approach is listmode reconstruction in which data are stored as a list of detected events each one associated to its position, energy and detection time [24].

1.2.1. Performance parameters of PET

PET technology makes use of solid scintillation detectors to sense gamma pairs. Several materials have been investigated in order to find the most performing one according to some characteristics such as stopping power of the detector for 511 keV photons, scintillation decay time, light output per keV of photon energy, energy resolution and detection efficiency. The stopping power of the detector is related to the mean distance the photon travels until it stops after complete deposition of its energy and depends on the density and effective atomic number (Z) of the detector material. The scintillation decay time derives from interactions between gamma rays and atoms of the detector material. This results in the atoms being excited to a higher energy level and then decaying to the ground state with emission of visible light. This time of decay is called the scintillation decay time and depends on the detector material. A shorter decay time leads to a higher efficiency of the detector at high count rates. Light output is responsible of a well-defined pulse, thus resulting in better energy resolution. The intrinsic energy resolution is affected by inhomogeneities in the crystal structure of the detector and random variations in the production of light in it. Usually detectors in PET scanners have relatively poor energy resolution (from 10% up to 25%). Finally, the detection efficiency depends on the linear attenuation coefficient (μ) which determines the fraction of incident gamma rays which experience either photoelectric absorption or Compton scattering when passing through the detector material.

Unfortunately, detector properties may vary from block to block. This is an issue in large PET scanners where thousands of detectors are assembled. Along with such a problem, variations in the gain of the photodetectors and detector block misalignments determine nonuniformity in the PET ring. This affects the integrity of the acquired projection data, thus requiring calibration procedures. Other problems are related to photon attenuation, random coincidences, scatter coincidences, dead time and parallax error.

Photon attenuation by tissues arises from variation of the thicknesses and distance of tissues from the detector pair in coincidence. Indeed, if photons travel through organs and tissues with uniform density (thus having the same μ), the probability P of coincidence detection is independent of the position of the annihilation site along the line of response, but is only related to the attenuation coefficient and to body size. In addition, when non-uniform organs and tissues are passed through, the attenuation coefficient and thickness of each of them influences the detection probability P. This leads to nonuniformity in the images since more coincidence

events are lost from the largest sections of the body, as depicted in figure 1.2; furthermore, the two photons may travel through different organs along the LOR. As such, correction is required to take into account this phenomenon.

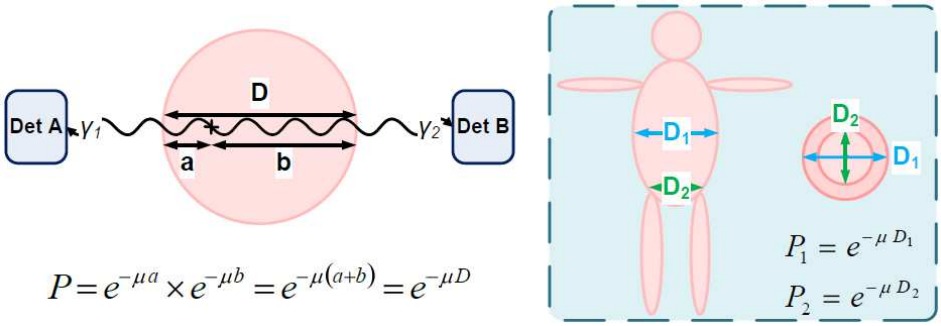


Figure 1.2 – Coincidence detection probability does not depend on the annihilation point but on the object size only (left). Nonuniformity in different sections of the body arises form different values of probability (right).

Random coincidences occur when two unrelated 511 keV photons from two separate positron annihilation locations are detected by a detector pair within the time window. This causes artefacts and loss of image contrast. A common method of correcting random events is to employ two coincidence circuits, one with the standard time window and another with a delayed time window both windowed in the same energy range. The counts in the standard time window include both random and true events, whereas the delayed time window contains the random ones only. Given that random events in both time windows are the same within statistical variations, correction is made by subtracting the delayed window counts from the standard window counts.

Scatter coincidences are related to radiations incurring in Compton scattering with energy within the acceptance window. These scattered radiations increase the background of the image, thus degrading the image contrast. Moreover, two Compton scattered photons are likely to sum up simultaneously in a detector. If the resultant peak falls within the energy window, an event will be counted but mispositioned because of the unrelated events involved, thus causing image distortion at high count rates. The scatter contribution increases with the density and depth of the body tissue, the density of the detector material, the activity in the patient and the energy window width.

Dead time is the time interval during which the system processes a gamma ray pair. It begins with the photon interaction with the detector and lasts until the end of event recording. During this interval the detection system is unable to process a second event, which is lost. This undesired effect can be reduced by using detectors with shorter scintillation decay time and high speed electronics components in the PET scanners.

Parallax error is due to coincidence events occurring at off-centre points with respect to the FOV. In this condition, the photons can strike tangentially at the backside of the detector pair with unknown depth of interaction. The resulting coincidence event blurs the image. This effect can be corrected by measuring the

light in the front and back of the detector and using the difference to estimate the depth of photon interaction in the detector.
In commercial PET scanners, where more adjacent rings are arranged, coincidences between detectors in different rings can be processed in either two possible modalities: 2D and 3D acquisition mode. The former is performed in scanners where annular shielding rings called septa are placed between the crystal rings so as to absorb photons travelling along large oblique angles. This allows coincidences to take place between neighbouring rings only, thus significantly reducing contributions from scattered photons and photons from radioactivity outside the FOV of the scanner from 30% to 40%. In 3D mode acquisition, no septa are used so that coincidences between all detectors in any ring are allowed. This results in increased sensitivity but in poorer spatial resolution due to random coincidences as well as in a larger amount of data to be stored.
Projection data acquired in 2D or 3D mode are further processed for reconstruction. The quality of the image and the accuracy of the resulting data strongly depend on the method used. Two reconstruction techniques are available: filtered backprojection and iterative methods. The former is the most commonly used in clinical environment as it is fast and simple although the generated images lack quantitative accuracy and often contain significant artefacts. It is based on the assumption that the number of photons recorded in any given detector bin represents the sum of contributions from the activity located along a line perpendicular to the detector surface. In iterative methods, an initial estimate of an image is made and the projections are computed from the image and compared with the measured projections. If there is a difference between the estimated and measured projections, corrections are made to improve the estimated image and a new iteration is performed to assess the convergence between the estimated and measured projections. Iterations are continued until a reasonable agreement between the two sets of projections is achieved. The main drawback of this technique is the reconstruction time which could be an issue especially for very large 3D data sets.
Image quality is also associated to several scanner parameters including spatial resolution, sensitivity, noise, scattered radiations and contrast [25,26].
Spatial resolution of a PET scanner is a measure of the ability of the device to faithfully reproduce the image of an object. It is empirically defined as the minimum distance between two points (sources) in an image that can be clearly distinguished by a scanner. It is influenced by the following factors.

- Detector size: Intrinsic resolution of the scintillation detectors significantly affects the spatial resolution. For multi-detector PET scanners, the intrinsic resolution is related to the detector size. For continuous single detectors, however, the intrinsic resolution strongly depends on the number of photons detected.
- Positron range: The positron is emitted with a kinetic energy conceiving to an energy spectrum between 0 and E_{max} (usually around 1 MeV for most of the positron emitters used in PET). The positron travels a distance in tissue, losing most of its energy and then annihilates after capturing an electron, i.e., forming a “positronium” atom. Since coincidence detection is related to the location of annihilation, an error occurs in the localization of true position of the positron emission, thus resulting in the degradation of spatial resolution.

- Non-colinearity: Non-colinearity arises from the deviation of the two annihilation photons from the exact 180° position; in a first ap proximation, this arises from some small residual momentum of the positron at the end of the positron range. Therefore, the observed LOR between the two photons is somewhat displaced from the annihilation site due to the *Lorentz boost*.
- Other factors which influence image quality are the reconstruction method used and the correct localization of the detector.

Sensitivity of a PET scanner is defined as the number of counts per unit time detected by the device for each unit of activity present in a source. It depends on the geometric efficiency, detection efficiency, energy window settings and the dead time of the system. The higher the sensitivity, the better the SNR achieved in the reconstructed image.
Image noise is mainly due to the random variation in pixel counts across the image and can be reduced by increasing the total counts in the image. Another source of noise arises from non-random or systematic addition of counts due to imaging devices or procedural artefacts. The image noise is characterized by a parameter called the *noise equivalent count rate (NECR)* which is related to true, random and scatter coincidence count rates.
Scatter fraction (SF) is often used to compare the performances of different PET scanners. It is defined as that fraction of the total coincidences recorded in the photopeak window which have been scattered.
Image contrast is a measure of the detectability of an abnormality relative to normal tissue. It arises from the relative variations in count densities between adjacent areas in the image of an object and can be influenced by count density, scattered radiation, size of the lesion and patient motion.

1.2.2. Photodetectors

In a PET scanner, the role of the photodetector is to translate the light emitted by the scintillator into an electrical signal. Generally, the photodetectors used in PET can be divided into two categories, the photomultiplier tubes (PMT) and the semiconductor-based photodiodes, which include avalanche photodiodes (APD) and silicon photomultipliers (SiPM).
Photomultiplier tubes are the most common photosensors used in PET. They consist of a vacuum enclosure with a thin photocathode layer at the entrance window. An incoming scintillation photon deposits its energy at the photocathode and triggers the release of a photoelectron. Depending upon its energy, the photoelectron can escape the surface potential of the photocathode and in the presence of an applied electric field accelerate to a nearby dynode which is at a positive potential with respect to the photocathode. Upon impact with the dynode, the electron, with its increased energy, will result in the emission of multiple secondary electrons. The process of acceleration and emission is then repeated through several dynode structures with increasing potentials, leading to a gain of more than a million at the final dynode (anode). This high gain leads to a very good SNR for low light levels and is the primary reason for the success and applicability of PMTs in PET detectors. The main drawback of a PMT is the low efficiency in the emission and escape of a photoelectron from the cathode after the deposition of energy by a single scintillation photon. This property is called the *quantum*

efficiency (QE) of the PMT and it is typically 25% [26]. Furthermore, PMTs are bulky, require very high bias voltages and are not magnetic field compatible.
Photodiodes are based on semiconductor technology and have high sensitivity in the detection of the low energy of scintillation photons. These detectors typically are in the form of inversely-biased PIN diodes where the incoming photons produce electron–hole pairs, thus resulting in a charge flow after the application of an electric field. In particular, APDs have a built-in avalanche region which generates a gain depending on the applied voltage. If operating below the breakdown, the total output current is proportional to the amount of incoming radiation (linear mode behaviour). Unfortunately, in these conditions the mean gain per photon is low so that the low output signal cannot be easily distinguished from noise. On the other hand, if the applied voltage is slightly above the breakdown (10% - 20%), a gain in the order of 10^2 is obtained. The APD is said to work in Geiger mode and exhibits a "digital" behaviour. Arrays of such APDs, called single photon avalanche detectors (SPAD), have been thought suitable for PET scanners in the early 2000s, given their compactness and IC technology and magnetic field compatibility. Some problems in SPADs are related to the increase of dark pulses (avalanches independent of the incident light) and recovery time with increased area [27].
Silicon photomultipliers overcome these limits by exploiting a dense array of SPADs connected in parallel on the same substrate. SiPMs combine the advantages of both PMTs, such as high gain and total QE, and APDs, like the small dimensions which permit extremely compact, light and robust mechanical design and magnetic field compatibility. The use of SiPM-based detectors is very promising for the implementation of high performance PET scanners [28,29].
Table 1.1 summarizes the main characteristics of PMTs, APDs and SiPMs.

Table 1.1 – Performance characteristics of the main photodetectors used in PET scanners.

	PMT	APD	SiPM
Gain	108	102	106
Bias voltage (V)	1000-2000	100-200	30-70
Output response (ns)	5-10	>1	<1
MRI compatibility	No	Yes	Yes
Compactness	No	Yes	Yes

1.2.3. History and state of the art of PET

Although modern PET technology has taken approximately thirty years to develop, the history of molecular imaging is strictly connected to several inventions and discoveries which took place since the early 1920s such as Rutherford experiments, the design of the first cyclotron and the positron discovery [30].

Furthermore, the application of modern biology and medicine to molecular medicine has been fundamental in making PET an essential tool in health care.
In 1951 William H. Sweet exploited for the first time the positron concept for medical purposes by implementing a simple brain probe where coincidence was used to localize brain tumours. Based on this idea, he collaborated with Gordon L. Brownell and a physics group at Massachusetts General Hospital to develop the first brain probe using two opposing sodium iodide (NaI(Tl)) detectors which detected photons when radiation passed through them. Photomultiplier tubes were placed to measure the amount of released light, which was proportional to the amount of radiation produced. The patient's head had to be placed between the two detectors and the circuitry was designed to detect the coincidence photons from the annihilation products. The idea of coincidence detection with mechanical motion in two dimensions used in these studies was the underlying principle of modern PET. Brownwell and Sweet performed the initial studies with positron emitters by changing Polaroid films in rapid succession. Electronic formatters increased the rate of obtaining images and image quality. In the same year, Wrenn, Good and Handler published studies on positron annihilation for localizing brain tumours. In their work, they presented the technique of simultaneous detection of the annihilation product photons to localize positron emission. They also discussed the principles behind the earliest cameras in positron studies. These two independent papers represent the first attempts to record positron data for use in a medical application.
In the early 1960s, Kuhl and Edwards were developing image reconstruction techniques for single photon tomography. Although this algorithm was not a true computed tomography approach, it did employ the principle of superimposition of back projections. About a decade later, Chesler introduced the filtered back projection technique whereas Hounsfield and Cormack reported their results on iterative techniques.
In the mid 1960s, Allan Cormack published papers where he demonstrated a bench top X-ray computerized tomograph scanner. Image reconstruction was based on a decomposition algorithm of a function in a set of projections, known as Radon transform (J. Radon, 1917). A few years later, Godfrey Hounsfield directed a project to combine X-ray and digital computer technology. This effort gave birth to computerized tomography.
In 1973, James Robertson of Brookhaven National Laboratory built the first ring tomograph, which consisted of 32 detectors. However, he was unable to obtain true reconstructed cross sectional images due to limited sampling, lack of attenuation correction and lack of a proper image reconstruction algorithm. In the same year, Michael E. Phelps built the first PET tomograph, known as PETT I (Positron Emission Transaxial Tomography). Later he reduced the name to PET because transaxial was not the only plane in which images could be reconstructed. Limited sampling, attenuation problems and bad collimators interfered with a successful transverse back projection.
From this moment on, ten fundamental steps paved the way to the development of modern PET [31].

- Event 1: In 1973, Mike Phelps and Ed Hoffman of Washington University joined EG&G ORTEC, a spin-off company of the Oak Ridge National Laboratory, and developed PETT II and PETT II ½ These tomographs were

used to establish the mathematics and physics of PET, as well as to perform imaging of blood flow and metabolism in animals. The principles of PET, as they are known today, were published from studies performed on these tomographs developed by Phelps and his team. At the end of 1974, Phelps and Hoffman constructed PET III for human studies. This system was a hexagonal array with excellent sampling by a combination of linear movement of detectors and a 60-degree rotation of the gantry. The system had its own computer for controlling the motion of the detectors, gantry and bed, as well as performing image reconstruction. Nizar Mullani developed the coincidence logic while EG&G ORTEC designed the electronics. The first images of blood flow, oxygen and glucose metabolism and F-18 bone scans from this tomograph represented the first published human PET images using the filtered back projection algorithm. Soon after, the first commercial PET scanner named ECAT II (Emission Computed Axial Tomograph) was designed at EG&G ORTEC. This tomograph used a total of 96 3.75cm NaI(Tl) crystals, had a PDP-11 computer with 32Kbytes of memory for a console and was sold for approximately $600,000 in 1978.

- Event 2: During 1970s, the only detector used in PET was NaI(Tl), which was difficult to manufacture because of its hygroscopic nature. Also, the NaI(Tl) scintillator had medium/low density and effective atomic number that limited the efficiency for the high energy photons (i.e., 511 keV). On the other hand, it had a high light yield and reasonably fast decay time to provide good coincidence time resolution. The use of another crystal, the bismuth-germanate (BGO), was considered after studies made by Cho and Derenzo so that in 1978 EG&G ORTEC produced the NeuroECAT, the first commercial tomograph to use BGO.
- Event 3: In the years 1978-80, fludeoxyglucose (FDG), a positron-emitting radiopharmaceutical, was used for PET imaging for the first time.
- Event 4: Between 1984 and 1986, CTI, Inc. built the first PET medical cyclotron; in the same years, Satyamurthy, Barrio and Padgett at UCLA developed the first automated chemistry module for synthesizing FDG, as well as other molecular probes. Nowadays, several companies (General Electric, Siemens, IBA) provide cyclotrons with various forms of automated chemistry for producing molecular imaging probes. Additionally, other companies sell automated chemistry modules for PET without the cyclotron.
- Event 5: During 1984-85, the idea of a block detector was introduced by Casey and Nutt, where thirty-two crystals for four photomultipliers were arranged, thus making possible the implementation of high-resolution PET tomographs. In 1983-84, the Computer Technology and Imaging, Inc. (CTI) a spin-off company of EG&G ORTEC dedicated to the ECAT design, paved the way to the commercial commitment of PET.
- Event 6: From 1985 to 1990, Schelbert, Schwaiger and Phelps developed and validated the match/mismatch principle for determining cardiac viability, which proved to be very important in the process of making clinical PET a reality.

- Event 7: Between 1987 and 1990, the entrance of the two major imaging companies (Siemens and General Electric) in PET design gave birth to a commercial focus on developing and supplying PET products for clinical service.
- Event 8: In 1991, Phelps presented the first whole-body oncology images obtained by using a technique developed by himself, Hoffman and Dahlbom. This started the evolution to detect primary and metastatic disease, differentiate benign from malignant lesions and assess therapeutic responses by being able to image all organs of the body in a single examination. These applications formed the basis of the Food and Drug Administration's (FDA) approval of FDG and the Medicare reimbursement of several oncology indications.
- Event 9: In the years 1997-98, the FDA Reform Bill was signed into law and government reimbursement for PET was finally announced.
- Event 10: The introduction, in the years 1990-2000, of cerium-doped lutetium oxyorthosilicate (LSO) revolutionized PET imaging. LSO has a slightly greater density, slightly lower effective atomic number and has five times more light output than BGO. Also, LSO has 7.5 times faster scintillation decay time. This LSO performance results in a combination of speed and light output improvement of 37.5 over BGO (see table 1.2). The first LSO PET tomograph, microPET, was designed and fabricated by Simon Cherry for small animals, whereas the first human LSO tomograph was delivered to the Max Planck Institute, Köln, Germany, in February 1999.

Table 1.2. – Some physical properties of common PET scintillators [26].

Parameter	NaI(Tl)	BGO	LSO	GSO	BaF_2
Effective atomic number (Z)	50.6	74.2	65.5	58.6	52.2
Density (g/cm3)	3.67	7.13	7.4	6.71	4.89
Attenuation length	2.88	1.05	1.16	1.43	2.2
Scintillation decay time (ns)	230	300	40	60	0.6
Light output (photons/keV)	38	6	29	10	2
Wavelength λ (nm)	410	480	420	440	220
Relative light output	100	15	75	25	5
Linear attenuation coefficient (cm-1)	0.35	0.96	0.87	0.70	0.44
Energy resolution (% at 511 keV)	6.6	10.2	10	8.5	11.4

1.2.3.1. Time of flight PET

In clinical applications, PET image quality benefits from the time of flight (TOF) feature either using analytical or iterative reconstruction algorithms. By measuring the photons arrival time on the detectors, the annihilation point can be estimated, thus leading to better noise level, contrast and clarity of detail in the reconstructed images [32]. In conventional PET, each time positron annihilation is registered, its position along the LOR is unknown. However, in TOF PET, faster detectors are used to measure the difference in the arrival time of the two gamma rays, thus narrowing the position of the annihilation along the LOR. This added information enables the reconstruction algorithm to provide the final image with fewer iterations and less image noise.

Figure 1.3 illustrates the principle of TOF PET [33]. Named d the radius of the detector ring and d_1 the distance between the annihilation site and the centre of the FOV, the distance of the two detectors in coincidence and the annihilation point is $(d + d_1)$ and $(d - d_1)$, respectively. Then, the arrival time difference between the two photons travelling at the speed of light c at the detectors is $2 \cdot (d_1/c)$. Clearly, photons originating from the centre of the FOV arrive at the detectors at the same time, since in this case it is $(d_1 = 0)$.

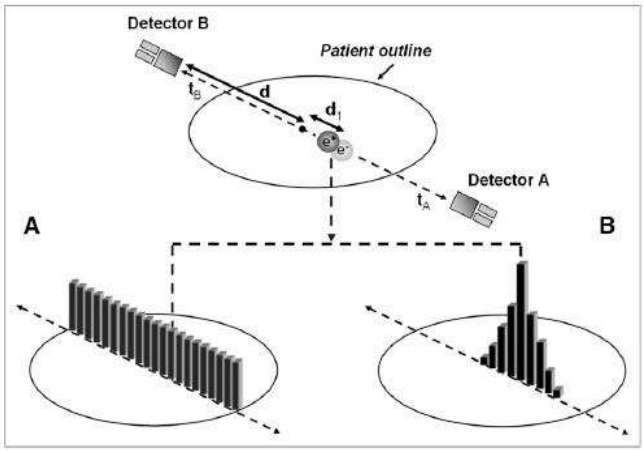


Figure 1.3 – Illustration of the TOF principle. Without TOF information (A) annihilation is equiprobable along the LOR. With TOF (B), the annihilation point can be estimated with restriction to a smaller region [33].

In a conventional PET (figure 1.3A) all voxels along the LOR are assigned equal probability in the generation of the annihilation site. Instead, in TOF PET the most probable location of the annihilation is at the centre of the uncertainty distribution (figure 1.3B).

Therefore, the TOF information is incorporated directly into the reconstruction algorithm, leading to an improvement in SNR given by [34]:

$$\frac{\sigma_{nonTOF}}{\sigma_{TOF}} = \sqrt{\frac{2D}{c\,\Delta t}} \qquad (1)$$

where σ_{nonTOF} and σ_{TOF} are the standard deviation of the image SNR without and with TOF measurement, *D* is the size of the object to be imaged and Δt is the TOF time resolution. Then, it is clear that the time resolution plays a key role in improving the image quality.
Figure 1.4 illustrates conventional PET and TOF PET in filtered backprojection [35].

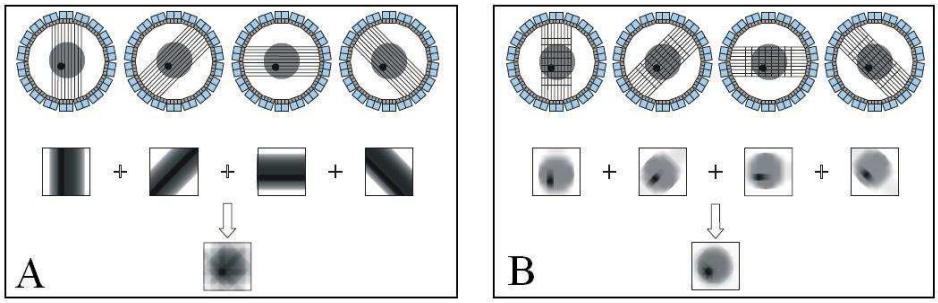


Figure 1.4 – Data collection and reconstruction in conventional PET (a) and TOF PET (b) (Adapted from [35]).

In conventional PET, the system just records the fact that an event took place somewhere along the lines connecting the detectors. In figure 1.4a, only four measurement angles are considered with a low resolution along the lines and a high resolution perpendicular to the lines. From these measurements four estimates are obtained (figure 1.4a, middle) and added to form the final estimate (figure 1.4a, bottom). The TOF information in figure 1.4b allows the placement of the events along the LORs thus defining 7 regions (figure 1.4b, top). In this case, the four estimates resulting from the measurement angles are closer to the original image (figure 1.4b, middle). Consequently, the quality of the final estimate given by the sum is much better than the conventional case (figure 1.4b, bottom). This can be observed in a real situation from figure 1.5, where both non-TOF PET and TOF PET acquisitions of a lung lesion are reported: the lesion is more easily discernible in the TOF PET study [36].

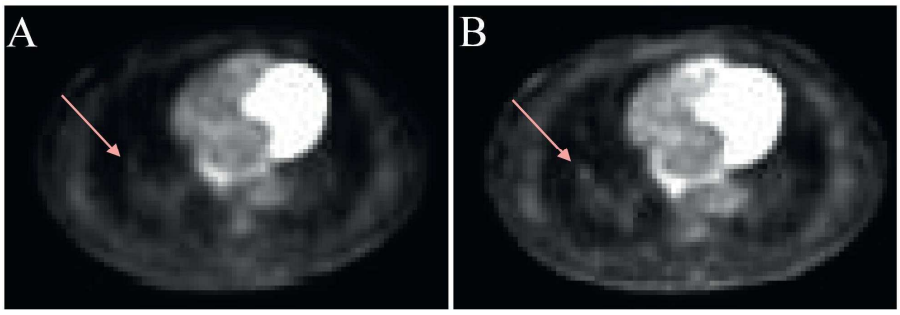


Figure 1.5 – Transverse slices showing lung lesion (arrows) with non-TOF PET (a) and TOF PET (b) acquisitions [36].

The potential benefits of TOF were understood in the early 1980s, thus leading to the development of the first TOF PET scanners at Washington University, CEA

LETI in Grenoble and University of Texas. These systems were based on caesium fluoride (CsF) or barium fluoride (BaF_2) scintillators which were very fast but did not have good stopping power for 511 keV photons (cf. table 1.2). The obtained timing resolution at system level was between 470 and 750 ps although stabilization of electronics and calibration was an issue. Furthermore, low density, low photoelectric fraction and low light output resulted in poor spatial resolution and sensitivity. Also, the ultraviolet emission of BaF_2 made light collection difficult and required the use of more expensive photomultipliers with quartz windows. By the early 1990s, interest in TOF PET scanners diminished until the recent emergence of new scintillators that are both fast and sensitive [37]. Cerium-doped lutetium orthosilicate , with a relatively high light yield, high effective Z and high density, has become the standard PET detector for the major PET scanner manufacturers. Moreover, LSO features a short decay time (40 ns), which was exploited to reduce the coincidence window from the 12 ns typical of BGO scanners to 6 ns and it was later reduced to 4.5 ns with the development of faster electronics. The short time coincidence window reduced the random coincidences in the acquired data. These characteristics proved that LSO could be a good candidate for a new generation of TOF PET scanners. In mid 2000s, the discovery of cerium-doped lanthanum bromide ($LaBr_3$) opened further possibilities for TOF instrumentation given its shorter decay time (16 ns), excellent energy resolution and twice as much light output than LSO, although it exhibits a lower stopping power [38].
A number of TOF PET scanners are currently commercially available [39]. The first commercial scanner, the Gemini TOF PET/CT, was introduced by Philips in 2006 and showed a time resolution of 585 ps [40]. It was based on LYSO scintillator crystal which has a structure very similar to LSO but with a fraction of the lutetium atoms in the crystal replaced with yttrium. LYSO properties are also very similar to those of LSO, the main difference being the slightly lower density due to yttrium's lower weight [41]. Also Siemens and General Electric have developed their own TOF PET scanners, Biograph mCT TOF PET/CT and Discovery 690, respectively. The former exploits arrays of LSO crystal pixels with a time resolution of around 500 ps [42], while the latter is based on LYSO scintillator and can reach a time resolution of 600 ps [43].

1.2.3.2. Combined PET/CT

The main drawback of PET in tumour imaging is the virtually complete absence of anatomic landmarks, which obstructs precise localization of lesions. Multimodality image fusion has been recognized as a possible solution where different tools can yield complementary information [44]. An improved performance in diagnostics can be obtained by combining high resolution CT images and low resolution PET scans of a patient. To this end, efforts have been made to co-register two sets of digital images where a one-to-one correspondence is established, thus adding precision of anatomic localization to functional imaging. This process, called the *alignment of images*, is based on the use of several techniques, such as the *manual method*, where alignment is obtained from the contour of the two sets of images; the *landmark technique*, where a common point either external or internal to the pictures is used; the *fully automated method*, based on algorithms which use surfaces or boundaries between organs to define the images; finally, other techniques implement alignment by exploiting the difference in the voxel intensities of the two pictures. These algorithms are usually implemented in vendor-neutral software such as Siemens Medical Solutions' Syngo, Philips Medical's Syntegra,

MIMvista's MIM, Mirada Solutions' Fusion 7D and Hermes Medical Solutions' BRASS. The co-registered images are displayed side by side with a linked cursor indicating spatial correspondence, or may be overlaid or fused using the gray scale or colour display [25]. However, the spatial correspondence obtained from separate imaging sessions suffers from both voluntary and involuntary movements of the patient (internal organs motion and repositioning errors) and software artefacts. Also, time differences in imaging create problems. For example, the contours of the abdomen are dependent on the pallet design; also, gastrointestinal organs move over time [45].
These problems have been addressed with the integration of the PET and CT systems within the same facility (PET/CT scanner) where both units are mounted on a common support with the CT unit in the front and the PET unit at the back next to the CT, both sharing the same couch (see figure 1.6). In this scenario, the CT scan data can also be used for attenuation correction of the PET images, thus providing higher quality images over shorter examination times [46]. Combined PET/CT imaging has proved to significantly influence the patient management affecting both the diagnostic and therapeutic approach [47]. The first PET/CT prototype was introduced by David Townsend and colleagues at University of Pittsburgh in 1998 [48]. At present, several vendors are producing PET/CT systems (Philips Gemini GXL, Siemens Biograph series, GE Discovery ST series, Toshiba Aquiduo, Shimadzu Eminence) where the latest high performance PET scanner and high performance multi-detector CT are used [49].

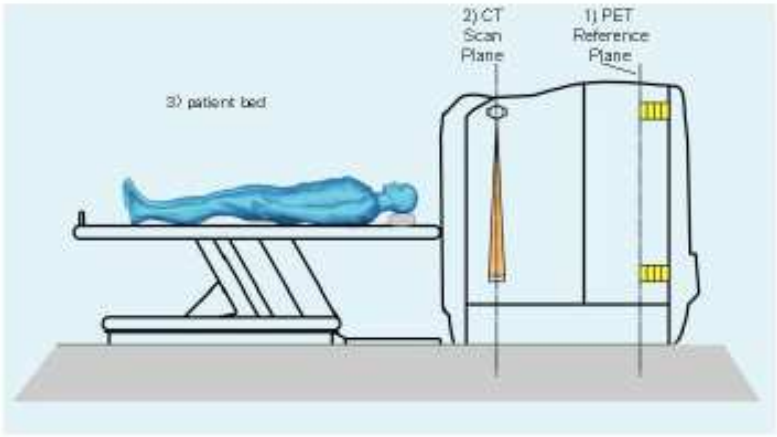


Figure 1.6 – Design of a combined PET/CT scanner [45].

It is worth noting that although PET and CT detectors are placed within the same gantry in PET/CT scanners, image fusion is not actually performed at hardware level. As a matter of fact, the two exams are still taken separately and a software fusion is performed between the images taken by each camera. However, the acquisitions are implemented with the same mechanical support and with the separate scanners positioned in-line at a fixed distance, which makes image fusion much more accurate than previous software fusion with images taken by separate camera systems at different times. Although PET/CT solves the problem caused by body contour deformability and time difference, some issues still exist like

breathing artefacts or inadvertent positioning changes between the two scans. This is especially true in the organs most affected by respiratory motion since CT scans are usually acquired during a breath hold while PET scans are acquired during free tidal breathing because of the long duration of scan, thus causing misregistration [45].

1.2.4. Some new trends in PET

PET is widely used in both clinical and preclinical research to study the molecular bases and treatments of disease. In clinical applications, PET has become a powerful tool in cancer diagnosing and staging, assessing neurological diseases such as Alzheimer's disease and dementias, myocardium blood flow and viability evaluation in cardiology.
Although PET/CT scanners are worldwide spreading, CT still has some serious limitations related to soft tissue contrast since it provides restricted resolution of these anatomical structures, thus requiring additional injections of contrast agents inside the tissues. Furthermore, the use of CT imaging in repeated scanning for therapy monitoring and other non-oncology pathologies leads to high levels of radiation exposure. An alternative approach for hybrid imaging is to combine PET with magnetic resonance imaging [50]. Compared to PET/CT, hybrid PET/MRI shows better contrast in soft tissues (i.e., human brain) because of the higher morphological resolution achievable with MR, thus leading to a better quality in the final image. Furthermore, PET/MRI would provide a useful tool for imaging children due to its reduced radiation dose. In table 1.3 the merits of the different medical imaging techniques are reported [51].

Table 1.3 – Merits of different medical imaging technique [51].

Parameter	Ultrasound	Optical imaging	CT scanner	MRI scanner	PET camera
Anatomical detail	OK	Good	Good	Excellent	Poor
Spatial resolution	OK	Good	Good	Excellent	OK
Clinical penetration	OK	Poor	Excellent	Excellent	Poor
Sensitivity	Poor	Poor	Poor	Poor	Excellent
Molecular imaging	Poor	Poor	Poor	OK	Excellent

From table 1.3 it is evident that combining PET with MRI leads to significant advantages in terms of image quality. As an example, CT (A), PET/CT (B), MRI (C), PET/MRI (D) scans of a squamous cell carcinoma of tongue are presented in figure 1.7. In the PET/CT scan, the lesion (indicated by the arrow) is identifiable but no anatomic correlation is present. This problem is overcome in PET/MRI given the contrast-enhancing mass of the base of tongue [52].

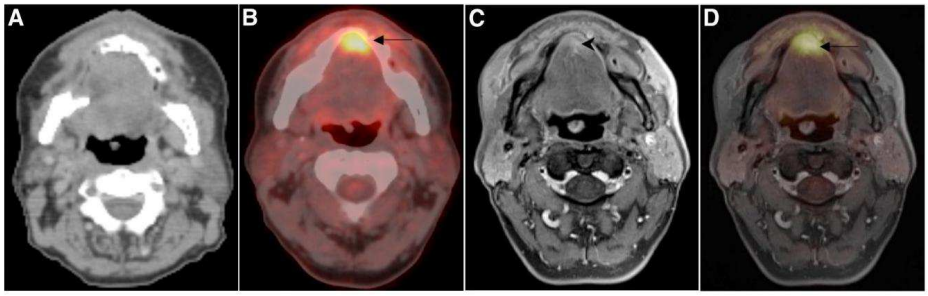


Figure 1.7 – Squamous cell carcinoma of tongue (arrow) scanned with CT (A), PET/CT (B), MRI (C), PET/MRI (D) [52].

Nowadays PET and MRI are generally performed at different times, in different places and with different facilities as in a "tandem" configuration, i.e., sharing the same bed as depicted in figure 1.8a. A software fusion technique is then used for merging the two images. This is because PET scanners make generally use of photomultiplier tubes as light detectors given their high gain. PMTs, however, are inherently unable to operate inside a magnetic field, thus implying distinct PET and MRI facilities. As previously stated, several problems are related to the tandem procedure, such as different patient positioning on the couch and involuntary movement of internal organs even when the temporal difference between scans is small [33]. Hybrid PET/MRI addresses many of these problems by combining the two techniques within a single device that simultaneously acquires the different images without moving the patient from the couch (figure 1.8b). This design minimizes misalignments due to involuntary internal organ motion and avoids artefacts related to the software fusion.

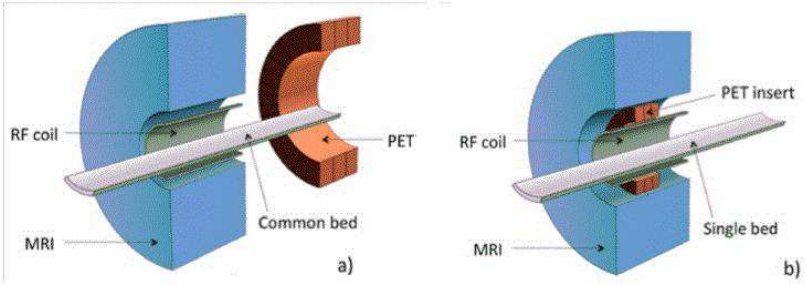


Figure 1.8 – PET/MRI tandem configuration (a) and hybrid PET/MRI (b) (Adapted from [50]).

However, simultaneous PET and MRI imaging is challenging, as the magnetic field of MRI technology interferes with PET, specifically with the PMTs needed for data acquisition, and PET signal processing might disturb high frequency signals of MRI. Current approaches combining PET and MRI are based on avalanche photodiode technology given its MR compatibility. Notwithstanding, a more effective solution can be provided by the use of silicon photomultipliers. The implementation of SiPM-based PET/MRI systems coupled to fast electronics is fundamental to achieve good performance in terms of time and spatial resolution,

thus requiring innovative detector designs. During the last fifteen years several PET/MRI prototypes for small animal imaging have been developed by research groups. In simultaneous PET/MRI for humans, the full use of multi-parametric imaging may be limited by the legally restricted application of PET radiopharmaceuticals outside diagnostically justified and allowed investigations. Such a limitation does not exist for small animal studies [53]. Recently, the first PET/MRI for human imaging (Biograph mMR) has been put on the market by Siemens Healthcare. The system features APD-based detectors and a 3T MR scanner. The PET ring consists of 56 copper shielded cassettes. Each cassette contains 8 detector modules with a matrix of 8 x 8 individual LSO crystals ($4 \times 4 \times 20\ mm^3$); a 3 by 3 array of APDs serves as readout electronics. The temperature is controlled by water-cooling. Each detector module contains a high voltage board supplying 500 V to the APDs, a board with a charge sensitive preamplifier ASIC and an ASIC output driver board. The energy resolution is 14.5% with a coincidence window of about 6 ns. The PET image resolution is 4.8 mm (FWHM) at a radial distance of 1 cm from the FOV's centre. Additional tests of the MR component regarding magnetic field and radiofrequency field homogeneities as well as possible interferences of the PET electronics with the MR signals revealed no significant distortions and no visible interferences [54]. In 2008, the HYPERImage research project has been funded by European Union to develop innovative PET components for PET/MRI integration in order to improve the performance currently available with APDs. To this end, SiPM has been selected for the PET detectors given the higher gain and faster timing resolution. However, although the design and first experiments of preclinical SiPM-based PET inserts for human 3T MR scanners and a solid state detector stack for TOF-PET/MRI have been performed, a commercial product of a SiPM-based PET/MRI has not yet been announced.

In addition to disease detection applications, PET is proving its benefit in radiotherapy treatment planning and chemotherapy monitoring. Besides the use of FDG for tumour tissue detection, other PET tracers have been developed in recent years, which can visualize biological pathways with particular significance for tumour response to the treatment.
Radiation therapy (RT) is a local treatment used to kill all clonogenic tumour cells by damaging the DNA of cancerous cells and to reach a complete local tumour remission. In external beam RT, DNA damage can be caused by two types of energy: photons or charged particles (proton, boron, carbon, neon ions). The former is based on the formation of free radicals from indirect ionization of the atoms of the DNA chain. One of the main limitations of photon radiation therapy is related to the low oxygen state (called hypoxia) in some solid tumours. As oxygen is a potent radiosensitizer, hypoxic environment makes cancerous cells 2 to 3 times more resistant to radiation damage. Instead, charged particles have an antitumor effect which is independent of the oxygen level since they cause DNA damage based on direct energy transfer. Furthermore, ions have little side scatter in the tissue and exploit the Bragg peak effect which leads to a better precision in targeting the tumour, thus reducing damage to healthy tissue. Indeed, particles at high energy deposit relatively little energy as they enter an absorbing material but tend to deposit extremely large amounts of energy in a very narrow peak (Bragg peak) as they reach the end of their range. The depth and magnitude of this peak

depends on mass, charge and initial energy of the particle. It follows that tissue damage range after the tumour has been reached is short, in contrast to uncharged particles whose energy damages healthy cells along the path after the cancerous area has been passed through as they exhibit an exponential decline of the dose distribution with depth. This is a serious issue in photon radiation as it can increase both treatment side effects and the probability of secondary cancer induction. This difference between the two types of radiation is crucial in the event of the proximity of critical organs [55,56].

Traditionally, treatment planning, monitoring and evaluation of response after RT are mainly based on computed tomography and magnetic resonance imaging. These radiological methods, called *anatomical imaging*, have the advantage of showing the anatomy with a high resolution. By exploiting these methods, in the past three decades highly sophisticated RT techniques have been developed in order to focus and intensify the irradiation dose on the tumour area with a high precision and to spare the healthy tissue to lower risk of sides effects. Nevertheless, anatomical imaging has some limitations in the delineation of the target volume as it is based on variation of tissue properties which may be similar both in tumour and non-tumour tissues affected by other pathological conditions. Moreover, anatomical imaging gives no information about important biological characteristics of the tumour. In this scenario, the new imaging methods of *biological imaging* such as PET represent a useful alternative in staging, treatment planning, response evaluation and follow up [57]. PET has also proven to be a valuable technique to monitor in situ and non-invasively the delivered dose in ion beam therapy, exploiting the β^+ activity produced in nuclear interactions along the beam path within the target volume. Monitoring of radiation therapy by means of PET can be performed according to three possible modalities: *in-beam*, where the measurement is performed during the irradiation by an integrated PET scanner; *in-room*, where a nearby scanner implements the measurement immediately after the irradiation; *off-line* in which the measurement is taken 10-30 min after the irradiation by a standard PET/CT scanner located outside the treatment bunker. In-beam PET has shown the best performance since image data are acquired simultaneously with the irradiation. The interpretation of the images is easier as for other modalities because the most relevant distribution of positron emitters is only slightly influenced by the radioactive decay and biological transport processes. However, a complete integration of in-beam PET into the therapy unit is a very challenging and costly engineering task as it requires the implementation of a measuring technique in order to suppress strong γ-ray background from the interactions of the beam in the beam line elements and the patient as well as the design of a dedicated double-head PET scanner and radiation hardness components. The in-room and off-line modalities are easier to implement and require cheaper facilities since a standard PET or PET/CT scanner can be used. However, β^+ activity distributions change during the time between irradiation and measurement due to decay of positron emitters and metabolic processes in tissue, thus making the evaluation of the β^+ activity images more difficult as compared to in-beam PET. Generally, in-room radiation monitoring is usually employed as it offers a compromise between the quality of measured data and the integration efforts [58]. However, in-beam PET techniques are being studied by several research groups in order to make it more feasible for treatment planning [59,60,61].

PET applications are uncountable and researchers are putting their efforts in order to improve instruments and techniques from several points of view (physical performance, image rendering and software reconstruction, biological effects, medical diagnosis and treatment). There is plenty of literature on new trends in each field involved with PET and it is beyond the scope of this work to introduce them all. Among the others, hybrid PET/MRI and in-beam ion radiation treatment have been discussed since possible hardware solutions to these applications will be provided in the next chapters.

1.3. Goals and organization of the thesis

The goal of this thesis work is to present the design and validation of two circuit components used in the electronic readout of PET scanners. After introducing some information about the architecture of the PET systems involved, design challenges and proposed solutions will be provided. The obtained results will be discussed and compared to the state of the art.

The first topic is about the optimization of a constant fraction discriminator used in the PCB read out of a double-head PET scanner for particle therapy, in order to improve the system performances by decreasing both the time window and the dead time of the electronics (chapter 2). These features become critical if in-beam acquisitions have to be taken because of the significant noise background, as previously discussed. The scanner had been originally developed some years ago at Istituto Nazionale di Fisica Nucleare (INFN) and improvements were required for this specific application. The work has been supported by the TPS (Treatment Planning System) project and coordinated by the group of medical physics at the department of physics/INFN of Pisa.

Chapter 3 is focused on the design of an integrated CMOS time to digital converter to be used for the time of flight measurement in a PET/MRI system. The required time resolution, linear behaviour as well as the communication with other readout elements will be discussed in order to motivate the choice of the circuit topology. The block detector (scintillator, photodetector and readout electronics) is being developed thanks to the collaboration among several Italian universities and INFN sections which are supported by the 4DMPET (4 Dimensions Magnetic compatible module for Positron Emission Tomography) project.

Finally, chapter 4 will point out the results obtained in both the two topics and give recommendations for further improvements.

2. OPTIMIZATION OF A CONSTANT FRACTION DISCRIMINATOR FOR PET

This chapter deals with the optimization of a constant fraction discriminator implemented on the PCB readout board of a double-head PET scanner. The work has been focused on the improvement of the system performances in terms of dead time and timing performances in order to provide a PET scanner capable to acquire coincidences during the beam delivery for hadrontherapy treatment. The activity has been supported by the TPS project collaboration at INFN Pisa.

2.1. The TPS project

Hadrontherapy is a form of external beam radiotherapy using beams of particles that are made of quarks (i.e., protons, neutrons or positive ions) for cancer treatment. In the last years, local control and survival statistics resulting from the employment of hadrontherapy in clinical treatment have shown several improvements over conventional radiotherapy. Furthermore, accelerator technology and systems for the computation of the delivered dose have experienced a significant progress, thus increasing the interest in the development of hadrontherapy techniques. This has led to the building of new advanced clinical centres for particle therapy with hadrons such as the CNAO that opened in Pavia (Italy) in 2011.
The TPS (Treatment Planning System) project has been established by INFN in 2008 and focused on the implementation of innovative treatment planning systems for hadrontherapy [62]. The TPS is a set of tools used to translate the prescribed dose into a set of beam energies, positions and intensities which have to be adopted during the treatment. Several INFN research groups have been involved in the project in order to give support to the different scientific areas covered, such as experimental and theoretical/phenomenological nuclear physics, Monte Carlo calculations and techniques for numerical analysis, radiobiology and hardware/software development for dose monitoring purposes. In particular, the development of a complete in-beam PET detection system for ^{12}C ion therapy monitoring has been the main goal of the project in order to perform the measurement of the β^+ activity produced during the irradiation. To this end, the hardware and software available from previous INFN collaborations have represented the starting point for further improvements. It consists of a double-head PET scanner with dedicated readout boards implemented on PCB and *ad hoc* reconstruction algorithms. Given the initial performances of the system, the design of new boards as well as novel software was needed in order to fulfil the TPS application requirements.

2.2. PET system at INFN

In figure 2.1 the PET scanner developed at INFN is depicted. It consists of two planar heads of 10 x 10 cm^2 housing up to four block detectors each and mounted on a variable aperture gantry.

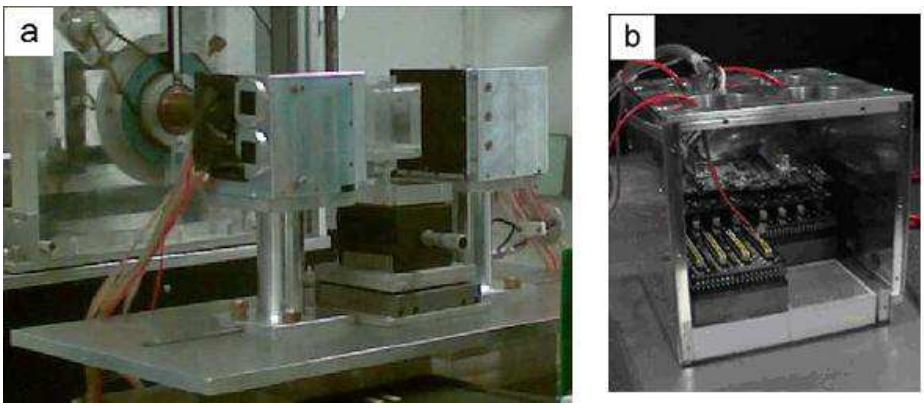


Figure 2.1 – Dual-head PET system developed at INFN (a). Each head can house up to 4 block detectors (b).

The light is sensed through matrices of 23 x 23 pixels of cerium-doped LYSO (LYSO:Ce) crystal having a size of 5 x 5 cm^2 and optically coupled to photomultiplier tubes (see figure 2.2).

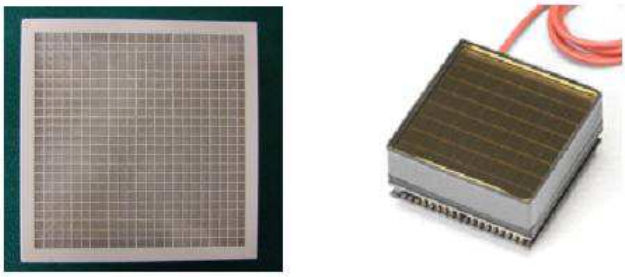


Figure 2.2 – LYSO:Ce scintillator crystal (a) and PMT H8500 (b) employed in the PET system.

The PMT used in the scanner heads (H8500 by Hamamatsu shown in figure 2.2b) features 64 anodes organized in an 8 x 8 matrix with a total active area of 4.9 x 4.9 cm^2. The required bias voltage ranges from -700V to -1100V with a gain ranging from 0.5 x 10^6 up to 1.5 x 10^6 and a rise time of 0.8 ns [63]. Table 2.1 summarizes the main characteristics of the PMT H8500.
The detector front-end, which was split up into three *on-board* PCBs communicating with each other in the initial configuration, provides the position signals of the light on the crystal as well as the trigger pulse informing that an event occurred. These data are sent to an external readout system including data acquisition boards (DAQ) driven by a synchronous coincidence unit running at 288 MHz and implemented on FPGA. Each DAQ digitizes and stores the position signals of its corresponding block detector by means of peak detectors and ADCs.

Table 2.1 – Main characteristics of Hamamatsu H8500 [63].

Spectral response (nm)	300-650
Peak wavelength (nm)	400
Maximum supply voltage (V)	-1100
Rise time (ns)	0.8
Gain	0.5×10^6 - 1.5×10^6
QE (% at 420 nm)	24

On the other hand, the FPGA checks for coincidences between the triggers sent by the front-ends. If this happens within a programmable time window (set at 10 ns), the DAQs are triggered to send the stored data to a computer via USB. Here, dedicated software implements a reconstruction of the event position on the detectors based on a common centroid algorithm.

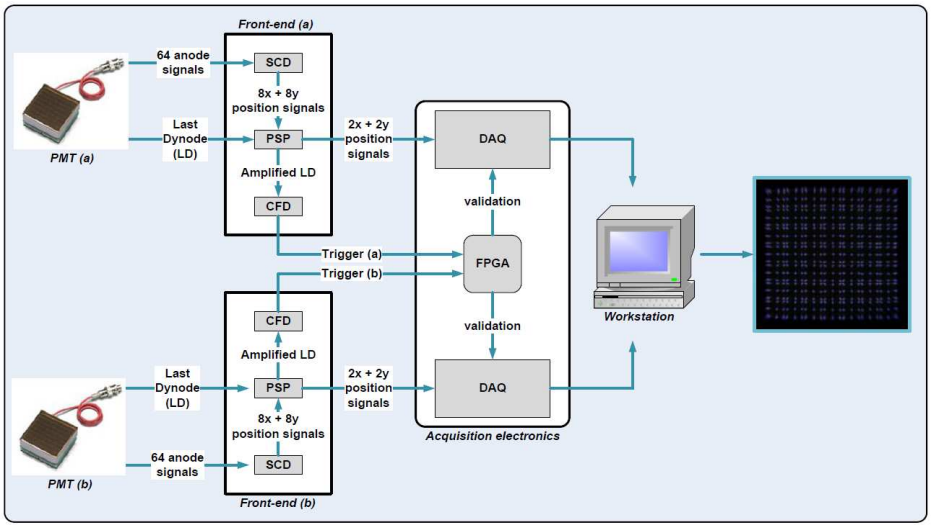


Figure 2.3 – Schematic representation of the readout process in a PET acquisition with the facility developed at INFN. Reconstructed image of the crystal pixel matrix is also shown (right).

The original multi-board front-end is divided as follows:

- A symmetric charge division (SCD) board, where a resistive chain is used to reduce the 64 position signals down to 16 (8 along the x axis plus 8 along the y axis).
- A pulse shape preamplifier (PSP) board, which amplifies and filters the 16 SCD outputs and further reduces them down to 4 position signals to be sent to the

DAQ. Furthermore, the PSP features a preamplification stage to elaborate the signal coming from the last dynode (LD) of the PMT.

- A constant fraction discriminator (CFD) board that receives the amplified LD signal from the PSP and generates the trigger which is forwarded to the external FPGA.

In figure 2.3, a block diagram of the readout process is shown.

2.2.1. Electronic readout performances

In this section a brief description of the multi-board front-end is given. Attention will be paid to the issues related to the configurations used, with special regard to the constant fraction discriminator. The voltage supply is ±5 V both for analogue and digital components.

2.2.1.1. Symmetric charge division

Symmetric charge division is a technique of dividing the charge signals produced by the PMT anodes into an X and Y decoder network [64]. This allows reducing the number of channels to be processed without impairing the resolution in the reconstructed image. Given N the total number of anodes of the squared PMT matrix, the signals resulting at the output of the decoder network are lowered down to $2 \cdot \sqrt{N}$. The SCD configuration, depicted in figure 2.4, is very simple and makes use of commercial analogue components such as resistors, operational amplifiers and capacitors.

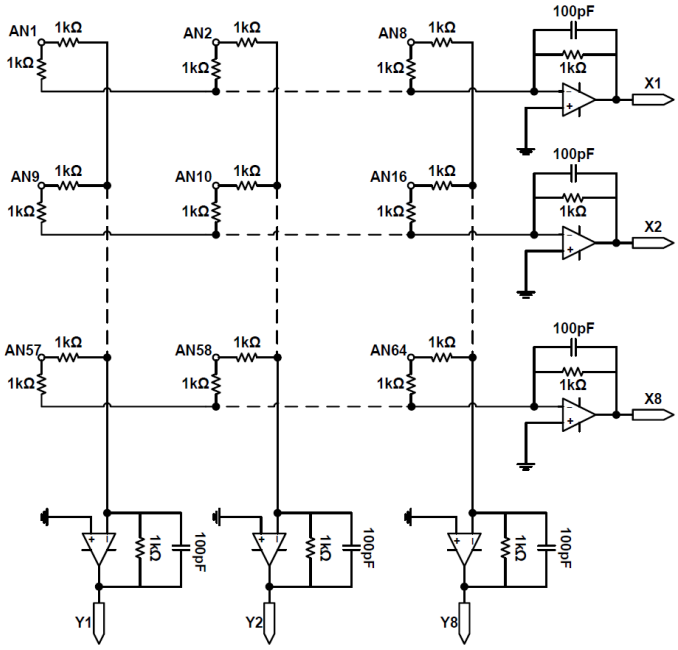


Figure 2.4 – Symmetric charge division network [65].

The incoming charge from each anode (*AN#* in figure 2.4) is split in half, with one part being collected in a X collection opamp and the other half in a Y collection

opamp. The resistor matrix is connected to low impedance charge sensing amplifiers (CSA) which perform a current to voltage conversion of the collected signals on each row/column. Indeed, CSAs take the input current pulse and deliver an output voltage proportional to the total charge contained in the input pulse. The feedback capacitor stores charge from the input so that a voltage appears on the output proportional to the total charge in the input signal. Thereafter, the resistor discharges the capacitor between pulses. Thus, high frequency noise is filtered whereas pulse stretching ensures that all output pulses have the same shape and decay time constant given by R_fC_f (equal to 100 ns in this case). This makes subsequent processing for amplitude discrimination much easier. Each resistor of the matrix is of the same value (1 kΩ) and the ratio of the resistor value to the input amplifiers impedance value is used to determine the coordinate information of the light on the PMT by exploiting a centre of gravity algorithm. The value of the splitting resistors is chosen to be large compared to the effective input impedance of the opamps so as to minimize the amount of charge lost along the loss paths that exist from each anode to the virtual ground of the charge sensing preamplifier [66].

2.2.1.2. Pulse shaping preamplifier

The PSP board receives the 8 + 8 outputs from the SCD network and reduces the number of channels from 16 down to 4. To this end, a standard and very robust technique is used to encode the light position on the photodetector [67]. Weighted resistive division networks perform a voltage to position conversion along the x and y axis, as depicted in figure 2.5.

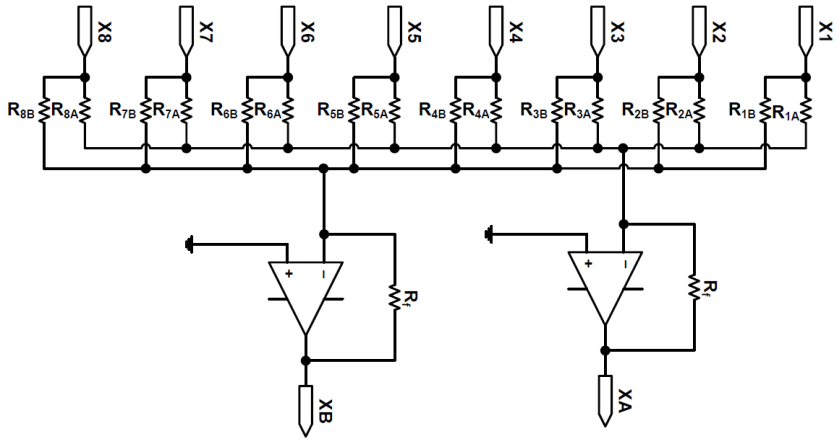


Figure 2.5 – Weighted resistive network for signal reduction along the x axis. The same scheme is implemented for the y direction. The value of the feedback resistor is 1.74 kΩ and the opamps used are AD8058.

Resistors R_{nA} and R_{nB} provide the signal distribution to the A and B summing amplifiers with values based on equations (2) and (3):

$$R_{nA} = \frac{R_{\max}}{(n-1)\cdot\frac{G-1}{N-1}+1} \qquad (2)$$

$$R_{nB} = \frac{R_{\max}}{(N-n)\cdot\frac{G-1}{N-1}+1} \tag{3}$$

where R_{max} is the highest resistor value used (5.11 kΩ in this case), N is the total number of channels (8 for each axis), n is the resistor index and G is the maximum conversion gain from node (R_{1A}, R_{1B}) to node (R_{NA}, R_{NB}) and it is equal to 8, given the lowest R_n value of 634 Ω. From equations (2)-(3) it can be seen that the conversion gain changes linearly as a function of input index, so that the output voltages at nodes X_A and X_B are given by:

$$V_{XA} = -R_f \cdot \sum_n \frac{V_{Xn}}{R_{nA}} \tag{4}$$

$$V_{XB} = -R_f \cdot \sum_n \frac{V_{Xn}}{R_{nB}} \tag{5}$$

where V_{Xn} are the voltages at the input nodes of the resistive network. Equations (4)-(5) stand for V_{YA} and V_{YB} as well at the output nodes Y_A and Y_B relative to the y axis. Therefore, the final position of an event on the detector can be evaluated with the common centroid formulas:

$$X = \frac{V_{XA} - V_{XB}}{V_{XA} + V_{XB}} \tag{6}$$

$$Y = \frac{V_{YA} - V_{YB}}{V_{YA} + V_{YB}} \tag{7}$$

However, before sending the 4 position signals (V_{XA}, V_{XB}, V_{YA}, V_{YB}) to the DAQ boards, shaping is performed on each channel by means of a 4th order Sallen-Key low-pass filter. This ensures that, in the event of coincidence, DAQ boards receive the trigger pulse in correspondence of the peak of position signals. The characteristic topology of the constant fraction discriminator determines a delay in the trigger generation with respect to the signal coming from the last dynode of the PMT, as it will be described in the next paragraph. Thus, by choosing the number of integrators to be cascaded with a given time constant, the peaking time can be set so that the peak detector on the DAQ board will measure the position value with precision. Furthermore, a single-ended to differential conversion is performed at the last stage of the PSP chain since position signals have to be forwarded to the acquisition system through cables, thus common mode noise rejection is required. Figure 2.6 illustrates the last section of the PSP including filtering and differential conversion. Each stage of the integrator can be described by the transfer function:

$$H(s) = K\frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \tag{8}$$

where K is the gain factor, ω_c is related to the cut-off frequency f_c of the filter and Q is the quality factor.

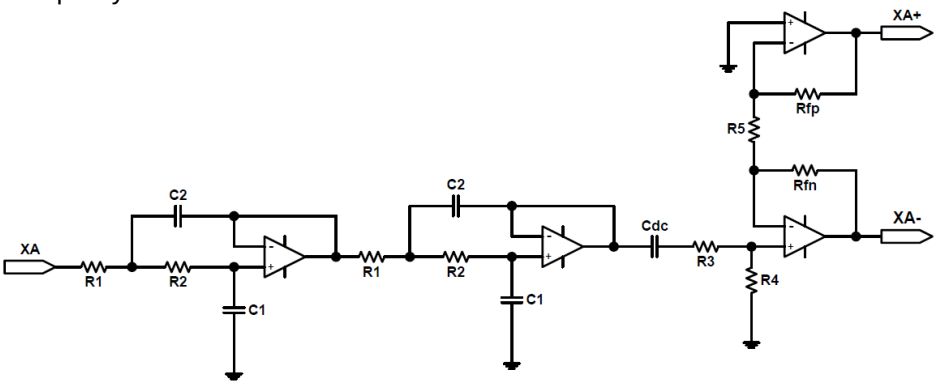


Figure 2.6 – 2 stage Sallen-Key low-pass filter coupled to a single-ended to differential converter for position signal processing before sending data to the DAQ boards. All opamps are AD8058.

With the opamp in the buffer configuration, it results K=1; furthermore, choosing R_1=R_2=R=1.74 kΩ and C_1=C_2=C=10 pF leads to:

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} = \frac{1}{2\pi RC} = 9.15MHz \quad (9)$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_1(R_1 + R_2) + R_1 C_2 (1-K)} = \frac{RC}{2RC} = 0.5 \quad (10)$$

The time constant is:

$$\tau = RC = 17.4ns \quad (11)$$

Thus, the peaking time can be calculated as:

$$t_{pk} = n\tau = 34.8ns \quad (12)$$

where n is the number of the cascaded integrators, which is 2 in this case. As it will be described in the next paragraph, t_{pk} has been set approximately equal to the delay affecting the trigger at the output of the CFD.
Finally, the single-ended to differential conversion stage provides the differential components with a gain factor given by:

$$K^+ = 1 + \frac{R_{fp}}{R_5} = 1 + \frac{680}{220} = 4.09 \quad (13)$$

$$K^- = -\frac{R_{fn}}{R_5} = -\frac{909}{220} = 4.13 \quad (14)$$

Resistor R_3, equal to 3.3 kΩ (originally 0 Ω), has been placed so that a voltage divider can be implemented together with resistor R_4 (1 kΩ) if signals exceed the dynamic range of the last stage opamps after the amplification according to (13)-

(14). Indeed, since the gain of detectors may vary with the characteristics of the material (cf. paragraph 1.2.1), the amplitude of signals must be controlled in order to avoid distortion. The C_{dc} decoupling capacitor has a value of 100 nF.
In the original configuration, the PSP board features a further stage dedicated to the preamplification of the signal coming from the last dynode of the PMT, as depicted in figure 2.7.

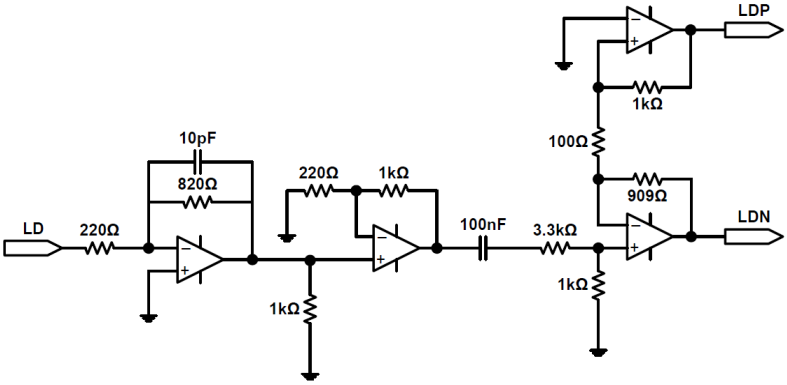


Figure 2.7 – LD preamplification stage on PSP board. After shaping and amplification, single-ended to differential conversion is performed.

Figure 2.7 shows that, after passing through a charge sensitive amplifier and a stage of amplification, the LD signal is transformed into a differential form. The PSP design was originally dedicated to an older PET system where the constant fraction discriminator was external to the block detector, thus requiring the use of cables. It follows that the signal must be converted back to single-ended on the CFD before filtering and processing. Of course, these stages are redundant in the latest PET version where the PSP and the CFD are close together and need to be replaced by a unique amplifier. Furthermore, after several amplification and conversion stages, the steepness of the LD rise edge worsens, thus decreasing the CFD timing performance. These considerations have been taken into account in designing the new front-end board.

2.2.1.3. Constant fraction discriminator

As previously discussed, detection of photon pairs in PET is based on the use of a coincidence unit which is triggered by the timestamps of the hits on the detectors. When a PMT is used as photodetector, the signal coming from the last dynode is processed to provide the arrival time of the events. By definition, the timestamp is the instant when a signal V(t) passes through a given threshold r(t) so that:

$$V(t) - r(t) = 0 \qquad (15)$$

In this scenario, a leading edge discriminator (LED), which combines a differential amplifier (DA) with a zero-crossing discriminator (ZCD), can be used to produce the trigger pulses. However, the timing performance of the system is related to several sources of errors that both affect signal and threshold, mainly the jitter and the *walk*. The former is related to the noise (thermal, shot, flicker) produced by the system components and causes fluctuations of the intersection point between V(t) and r(t). The walk is due to the statistical fluctuations of the radiation which

determine variations of the signal amplitude. In addition, variations of the rise time can arise from fluctuations of the drift velocity of the charge along its path through the PMT. As such, a more sophisticated system is required to process the LD signal in order provide the event timestamp with higher accuracy. Firstly, signal to noise ratio can be maximized by placing a filter before the LED. A semi-Gaussian filter is a common choice although some techniques have been studied for optimum filtering [68-69]. The system including a filter coupled to a LED is quite robust against walk. Assuming all input signals with the same rise time but variable amplitude, the zero-crossing time of the derivative will be constant. Nevertheless, if the threshold is kept fixed, rise time fluctuations are an issue. A solution is provided by constant fraction discriminators (CFD) where a threshold proportional to the amplitude of the input signal V(t) is applied. This technique can be implemented by splitting the input pulse in half, with one part being delayed by a time t_d and the other one being attenuated down to f·V(t), with f<1. Then, the two halves are sent to a differential amplifier which provides the bipolar signal (1-f)·V(t) to the ZCD with a zero-crossing phase point corresponding to the desired fractional triggering level on the leading edge configuration [70]. Moreover, since triggers may be generated by both noise and true signals, another discriminator (arming discriminator, ARM) is used in leading edge configuration in order to discard fake triggers at the output of the CFD by a logic *and* operation. The overall scheme of the CFD is depicted in figure 2.8.

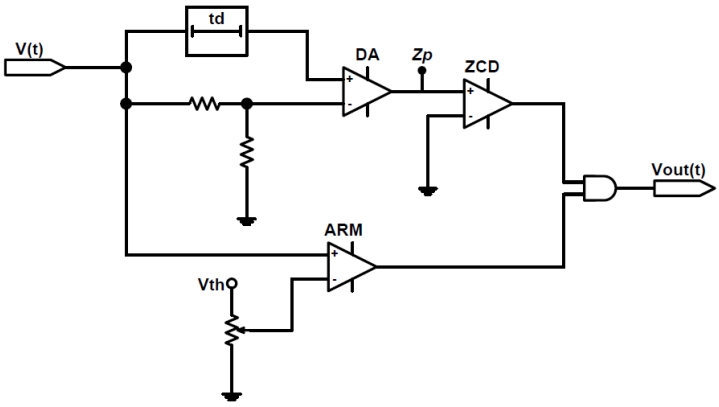


Figure 2.8 – CFD scheme: the input signal V(t) is split into 3 branches in order to minimize both amplitude and rise time fluctuations as well as to discard noise.

It is worth noting that, since the signal at node Z_p is affected by noise, it is usually compared by the ZCD with a threshold (*walk threshold*) slightly above 0 V so as to prevent the ZCD output from firing in correspondence of noise other than V_{Zp}.
The choice of t_d is critical to get optimal behaviour with respect to rise time fluctuations. The rise edge of V(t) can be approximated as a straight line described by the equation:

$$y = V\frac{t}{t_r} \qquad (16)$$

where t_r is the rise time of the input signal. If the delay is chosen so that $t_d > t_r$, the situation depicted in figure 2.9b appears at node Z_p.

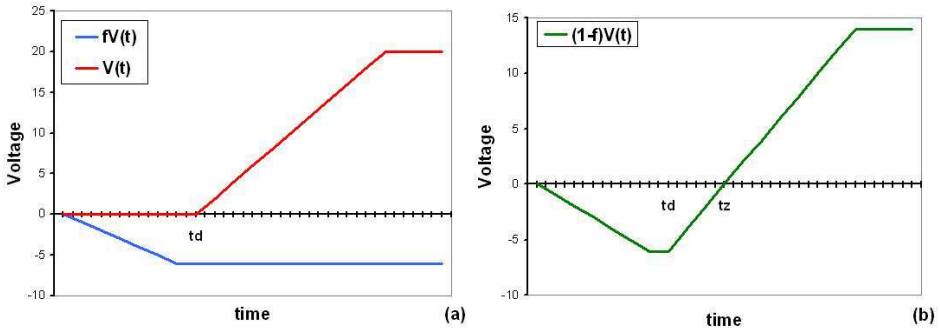


Figure 2.9 – Delayed and attenuated signals at the input of the differential amplifier (a) and waveform resulting at node Z_p (b) when $t_d > t_r$.

In figure 2.9, t_z is the zero crossing time and it results:

$$V\frac{(t_z - t_d)}{t_r} = fV \quad \Rightarrow \quad t_z = t_d + ft_r \tag{17}$$

Equation (17) highlights that in this situation t_z is independent of the signal amplitude but is still influenced by t_r.
By choosing $t_d < t_r$, the waveforms shown in figure 2.10 appear at the input and output of the DA.

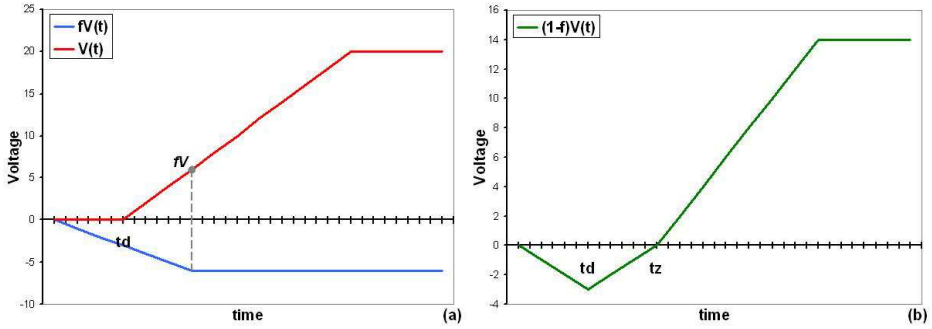


Figure 2.10 – Delayed and attenuated signals at the input of the differential amplifier (a) and waveform resulting at node Z_p (b) when $t_d < t_r$.

The zero-crossing time can now be expressed as:

$$V\frac{(t_z - t_d)}{t_r} = fV\frac{t_z}{t_r} \quad \Rightarrow \quad t_z = \frac{t_d}{1-f} \tag{18}$$

This expression states that rise time variations do not interfere with t_z anymore. Then, given the desired triggering level f which defines the attenuation factor, the delay time is chosen smaller than t_r such that the f % phase point on the delayed signal is in line with the maximum amplitude of the attenuated and inverted pulse as shown in figure 2.10a. Thus, calculating the delayed signal in $t = t_r$ and equating to the attenuated value leads to:

$$V\frac{(t_r - t_d)}{t_r} = fV \quad \Rightarrow \quad t_d = (1-f)t_r \tag{19}$$

The described configuration is called Amplitude and Rise Time Compensation CFD (ARC CFD) and is the one implemented in the multi-board front-end of the PET at INFN. The detailed circuit is depicted in figure 2.11.

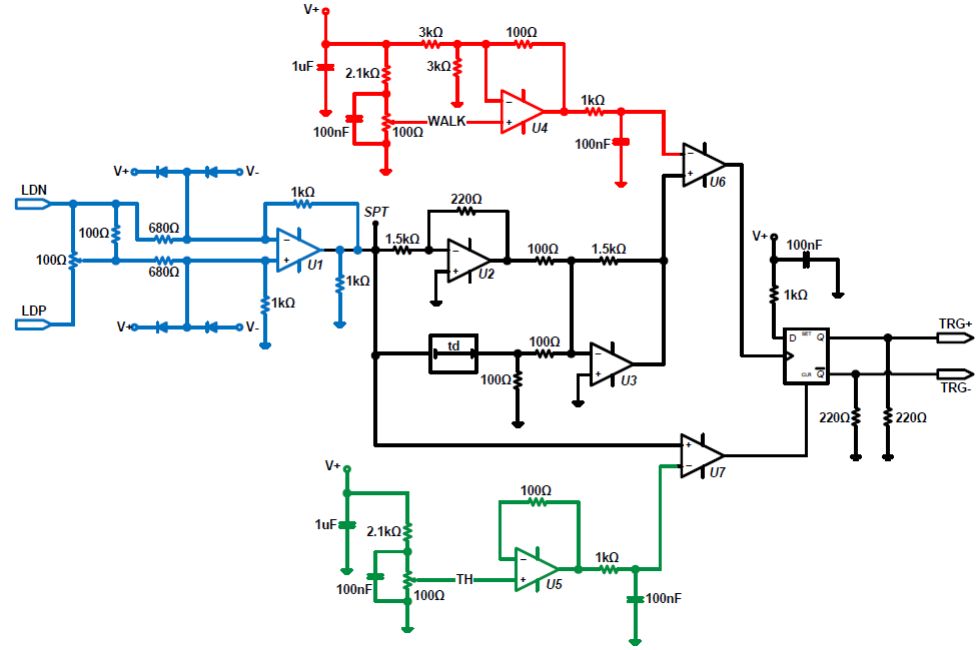


Figure 2.11 – CFD implementation in the multi-board front-end of the PET scanner.

The first stage of the circuit is a differential to single-ended converter (blue) that receives the differential LD signal previously filtered by the PSP board, as already discussed. Then, the signal at node SPT is split into the three branches of the CFD. The green section implements the threshold (TH) to be used by the ARM (U7) for discriminating noise, whereas the walk threshold (WALK) is provided by the red circuitry. Both the two thresholds are set by cascading a trimmer with an opamp which decouples the input level from the load. Given the desired attenuation f of 15% provided by U2 and the rise time of the signal at node SPT, applying equation (19) gives $t_d \approx 30$ ns. Then, the inverted and attenuated pulse is summed up to the delayed one by U3, which amplifies the two signals by 15 and provides the bipolar waveform to the ZCD (U6). The output of U6 fires according to the (18) at t_z = 35 ns in ideal conditions (i.e., when no noise is present and WALK = 0 V), which is almost equal to the peaking time of the position signals defined by the two Sallen-Key filters on the PSP board. Outputs from U6 and U7 (MAX9601) are in PECL mode and feed an SR flip-flop (MC100EL31) which discards noise-related pulses, since the clear signal (output of U7) is switched from high logic level down to 0 only when V_{SPT} is above TH. Then, as soon as a clock pulse is generated at the output of U6, the flip-flop forwards a trigger to the

coincidence FPGA. During this time range, the CFD is said to be paralysed as no other input pulses can be processed until both the clear and the clock signal return back to logic 1 and 0, respectively. This dead time is mainly responsible of the in-beam acquisition capabilities of the PET system and strongly depends on the timing properties of the LD signal feeding the CFD branches.

2.3. Proposed CFD topology

The use of the double-head PET system for in-beam RT applications requires readout electronics with fast timing properties as well as reduced dead time in order to sustain the single photon count rates. These properties mainly arise from the CFD performances. Thus, some topology improvements have been carried out on the front-end board in order to provide a tool capable to fulfil the application requirements. Bearing in mind the original readout configuration, some considerations have been made. Firstly, the differential conversion of the LD signal is redundant given that communication with the CFD does not require the use of cables. Second, the LD signal is amplified and attenuated several times in succession, whereas a single effective amplification would be sufficient. Lastly, the circuit components are not fast enough to exploit the steep rise edge of the LD signal which has a rise time of around 3 ns, as reported in figure 2.12.

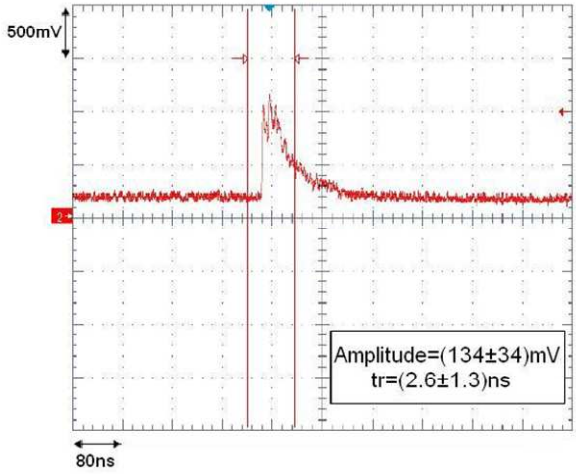


Figure 2.12 – LD signal measured at the output of the PMT.

The signal shown in figure 2.12 arises from the lutetium radioactivity and the measured amplitude and rise time values have been used to build a triangular shaped waveform for simulation purposes.
Based on the previous observations, some changes have been made to the LD processing blocks which have led to the circuit configuration shown in figure 2.13 (hereafter referred to as new board, NB). The sections in black are almost unchanged with respect to the circuit in figure 2.11 (old board, OB). The ARM threshold (TH) implementation is simplified as no buffering is included; the 1 kΩ trimmer is directly connected to a 220 Ω load which feeds the inverting input of comparator U3.

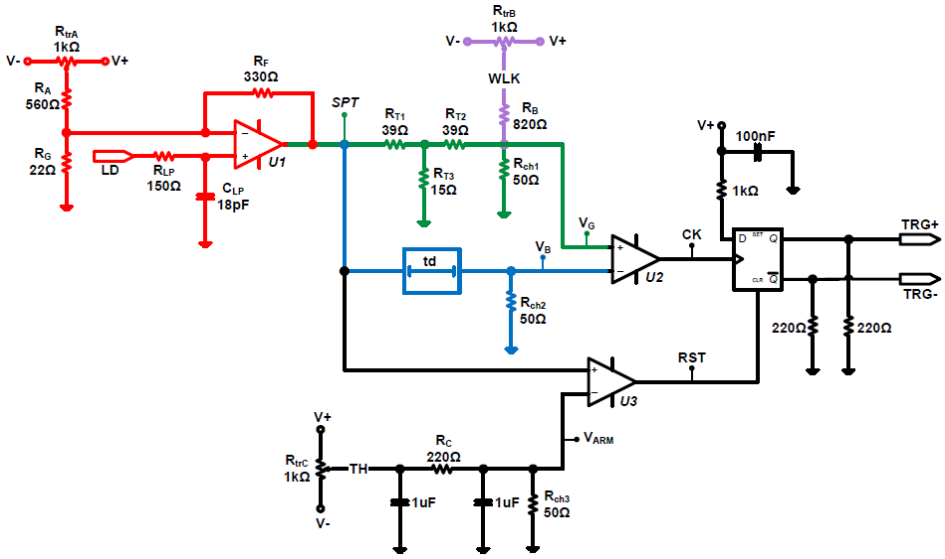


Figure 2.13 – New CFD circuitry. All resistors are 0603-size with 5% tolerance.

The PMT forwards the LD pulse straight to the red section of the circuit which performs both amplification and filtering and provides the V_{SPT} signal to the CFD branches. Thus, the PSP blocks of figure 2.7 as well as the blue section of figure 2.11 are now replaced by this single red stage. Firstly, the LD signal is processed by a low pass filter with a time constant given by:

$$\tau = R_{LP}C_{LP} = 2.7ns \qquad (20)$$

which is approximately equal to the rise time of the input (cf. figure 2.12). Afterwards, the non-inverting opamp U1 amplifies the filtered signal. A high speed current feedback amplifier (CFA) has been selected for U1. CFAs do not have the traditional differential amplifier input structure like voltage feedback amplifiers (VFA). The circuit configuration lacks of precision but exhibits an increased bandwidth and slew rate, faster rise/fall times and less intermodulation distortion compared to VFAs. Moreover, CFAs can be dc-coupled unlike previous generation high-frequency amplifiers, therefore they are well suited for high speed applications such as pulse amplification.

Figure 2.14 shows the CFA model. The non-inverting pin corresponds to the input of an input buffer which provides a very high impedance; on the other hand, the CFA inverting pin features the low input impedance offered by the input buffer's output which is usually less than 50 Ω (modelled by Z_b in figure 2.14). This mismatch at the two input pins of the CFA precludes it from operation in the differential amplifier configuration. Low output impedance is provided by the output buffer's output. The current-controlled current source, Z, is a transimpedance which serves the same function as gain in VFAs. Its value is usually in the MΩ range, so the CFA accuracy improves by closing a feedback loop as in VFAs [71]. Both the input and output buffers have open loop gains (G_B and G_{OUT}, respectively) close to unity.

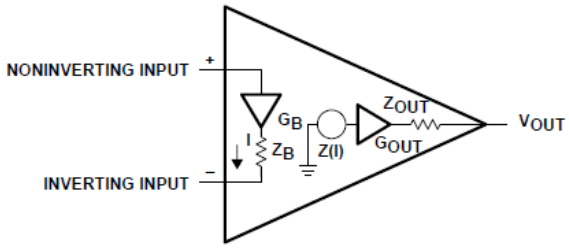


Figure 2.14 – Model of a current feedback amplifier [71].

When configured as non-inverting amplifier (see figure 2.15), the closed loop gain equation of the CFA is identical to that of VFA. This is true if the transimpedance Z is very high and the input buffer's output impedance Z_B is close to zero. These two assumptions are harder to meet than assuming only high open loop gain in VFA and this is what makes CFAs less precise than VFAs.

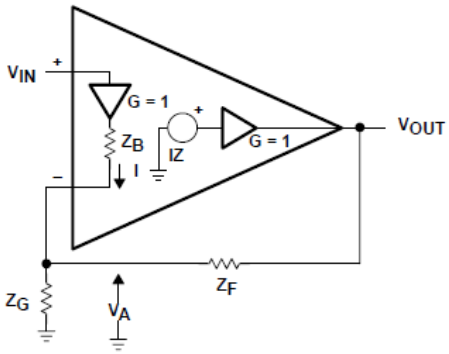


Figure 2.15 – CFA in non-inverting configuration.

Stability in CFA is affected by both internal parameters (Z and Z_B) as well as external components such as Z_F and Z_G. The transimpedance and the feedback resistor Z_F have a major impact on stability, whereas the parallel combination of Z_B and Z_G has little effect on phase margin because of the low value of Z_B. The optimum value of Z_F is usually determined by the manufacturer during characterization of the IC and is provided on data sheet for a set of gains.
The stability equation can be written as:

$$\frac{V_{out}}{V_{in}} = \frac{Z}{Z_F + Z_B\left(1 + \frac{R_F}{R_G}\right)} \qquad (21)$$

In ideal conditions, when Z_B approaches to zero, the opamp becomes independent of the ideal closed-loop gain; thus, R_F only determines stability whereas the bandwidth is independent of the external resistors. However, Z_B strongly depends on the working frequency and the transistor parameters so it adds variability to the CFA performances.

The CFA employed in the new CFD is AD8009 and its main characteristics are summarized in table 2.2.

Table 2.2 – Main characteristics of AD8009 [72].

Slew rate (V/μs)	5500
Rise time (ps)	545
Bandwidth (MHz)	440
Settling time (ns)	10
Voltage supply (V)	±5

The feedback resistor recommended by the manufacturer is 326 Ω (R_F = 330 Ω is the commercial value used). In order to get an amplification of 15, the value of R_G is 22 Ω. The trimmer at the inverting pin has been added for offset adjustment.
Once V_{SPT} exits U1, it is split into three branches: the green path provides an attenuated version of the signal summed up with an adjustable offset (purple in figure 2.13) which serves the same function as the walk threshold in the OB. Attenuation is provided by a T-shaped attenuator which is terminated on the impedance R_{ch1} of 50 Ω and is sized so as to provide the required attenuation f of around 15% according to the following relations:

$$R_{T1} = R_{T2} = \left(\frac{K-1}{K+1}\right) R_{ch1} \tag{22}$$

$$R_{T3} = \left(\frac{K}{K^2-1}\right) 2R_{ch1} \tag{23}$$

where K is related to the attenuation factor expressed in dB:

$$K = 10^{-f_{dB}} \tag{24}$$

Applying equations (22) and (23) leads to $R_{T1} = R_{T2} \approx 36$ Ω and $R_{T3} \approx 15$ Ω. Commercial resistors with closest values have been used as reported in figure 2.13. The attenuated signal V_G enters the positive input pin of comparator U2 (ADCMP562) where it is compared with the delayed signal V_B provided at the inverting input of U2. A clock pulse is generated when V_B increases above V_G. The intersection point between V_B and V_G satisfies equation (18) as t_z. Thanks to the high speed behaviour of the CFA, the resulting waveform at the output of U1 (V_{SPT}) exhibits a short rise time of 5.9 ns whereas in the OB a larger value of 44.4 ns was calculated, as shown in the simulations of figure 2.16. Thus, the time delay applied along the blue path has been evaluated based on expression (19) and set equal to 3 ns. Figure 2.16 also shows that the fall time of V_{SPT} is almost halved in the new CFD. This has important consequences on the dead time performance as the output pulses of U2 and U3 have shorter duration which depends on the V_{SPT}

width. This can be observed in figure 2.17 where simulations of the CK and RST signals in both the OB and the NB are reported.

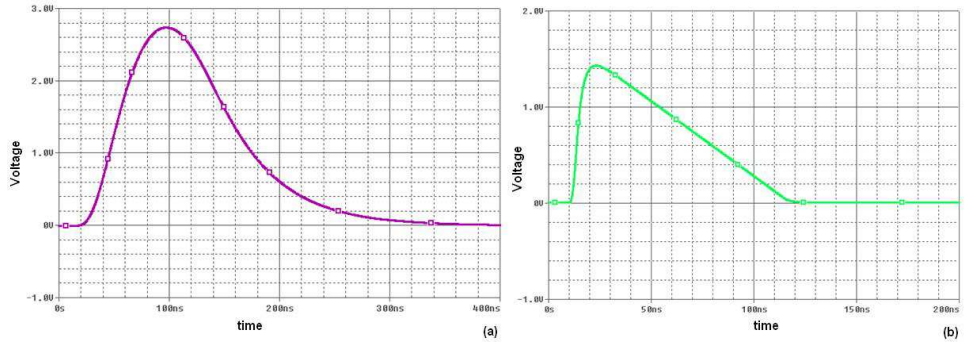


Figure 2.16 – Simulated V_{SPT} in the old (a) and new (b) CFD.

Since the circuit is only able to process a new signal when both U2 and U3 have returned to their *wait* condition (i.e., RST = "1" and CK = "0"), the dead time can be calculated between the fall edges of RST and CK. The comparators which have been used in the OB are MAX9601 and feature a propagation delay of 500 ps [73] whereas, in the NB, the ADCMP562 features a propagation delay of 700 ps [74] since the former was not commercially available anymore. Simulations of figure 2.17 show a reduction of the dead time in the new CFD down to one third with respect to the old board.

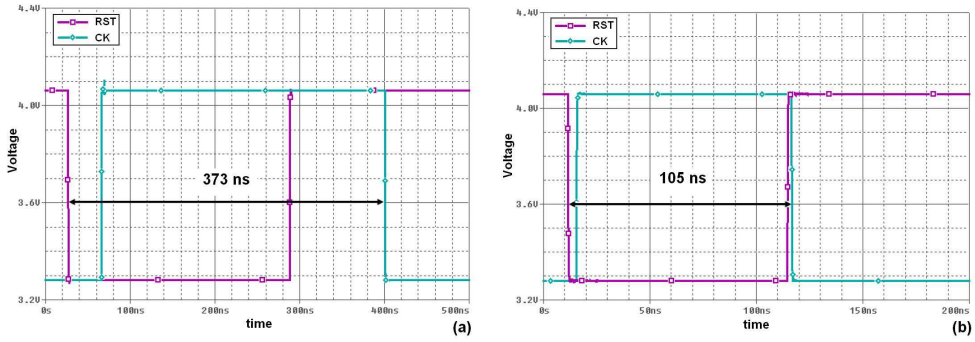


Figure 2.17 – Simulated dead time in the old (a) and new (b) CFD. The latter exhibits a significant reduction down to one third with respect to the old circuit.

Finally, some considerations about robustness against rise time and amplitude variations (walk effect) can be made. Although equation (18) states that the zero crossing point is independent of the input signal characteristics, in the real world some fluctuations affect the CFD performance. This is mainly due to noise which influences both TH and WALK thresholds as well as approximation in the determination of f and t_d parameters. In figure 2.18 the CK pulse behaviour in the original and modified discriminator configurations is depicted. The simulated results are obtained by varying the LD amplitude between 100 mV and 160 mV and its rise time between 1.5 ns and 3.5 ns, according to the measured data reported in figure 2.12. The improvement in the timing performance of the NB comes from the

use of the high speed preamplifier (U1), since the steeper rise edge of the V_{SPT} output makes it less susceptible to rise time and amplitude fluctuations.

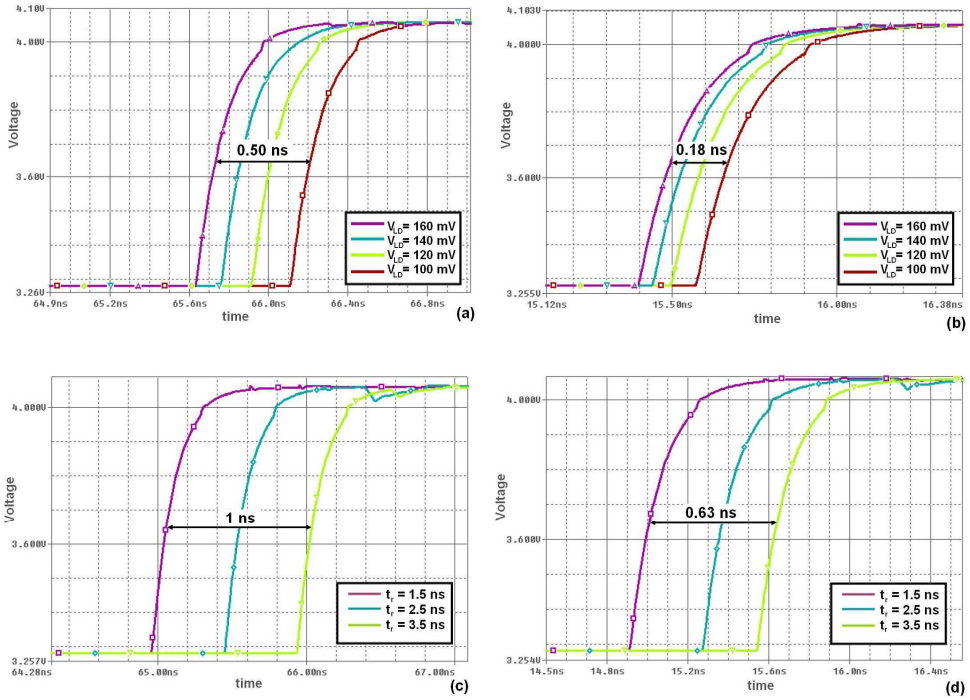


Figure 2.18 – Effect of amplitude and rise time variation on CK generation in the old (a-c) and new (b-d) CFD.

A final observation has to be made about the creation of position signals on the PSP board. As previously stated, the peaking time of the (x, y) coordinates at the output of the low-pass Sallen-Key filter is set so that DAQ boards are triggered in correspondence of the maximum values of V_x and V_y. Thus, the reduction of the time delay in the new CFD configuration leads to a faster trigger generation and requires shorter peaking time in the PSP circuitry. This is accomplished by removing one of the two filter stages and reducing the feedback resistor down to 220 Ω which leads to a peaking time of 2.2 ns.

2.3.1. Experimental results

Given the simulated results of the modified CFD configuration, a new PCB has been realised which gathers both the PSP and the discriminator circuitry on the same board, thus reducing the noise due to inter-board communication. Furthermore, this solution offers an improved mechanical robustness to the readout which has to be inserted within the block detector. The new front-end, called PA-D (Position Amplification and Discriminator), is shown in figure 2.19. The TH and WALK thresholds have been set after measurement of the noise affecting the signals at the input of the comparators (U2 and U3 in figure 2.13) and applying the "three sigma rule" in order to reject 99.73% of noise (which is assumed to have normal distribution) out of the trigger generation process. According to the acquired

data reported in figure 2.20, the following configuration has been defined: TH = 50 mV and WALK = 40 mV. Thereafter, the performance of the new circuitry has been tested and compared to the results derived from measurements performed on the old board.

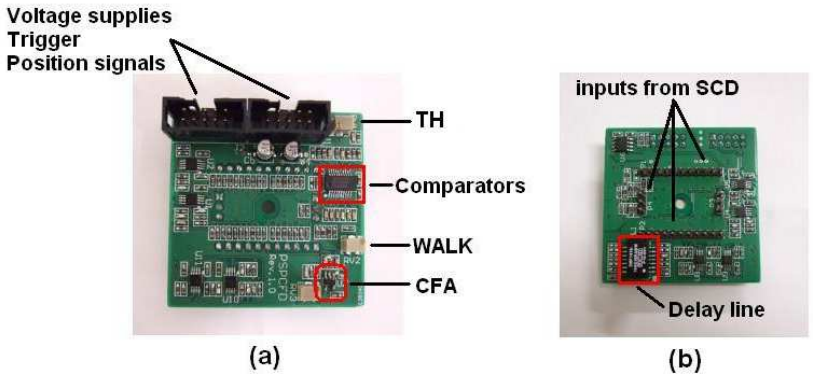


Figure 2.19 – Front (a) and back (b) sides of the new PA-D board.

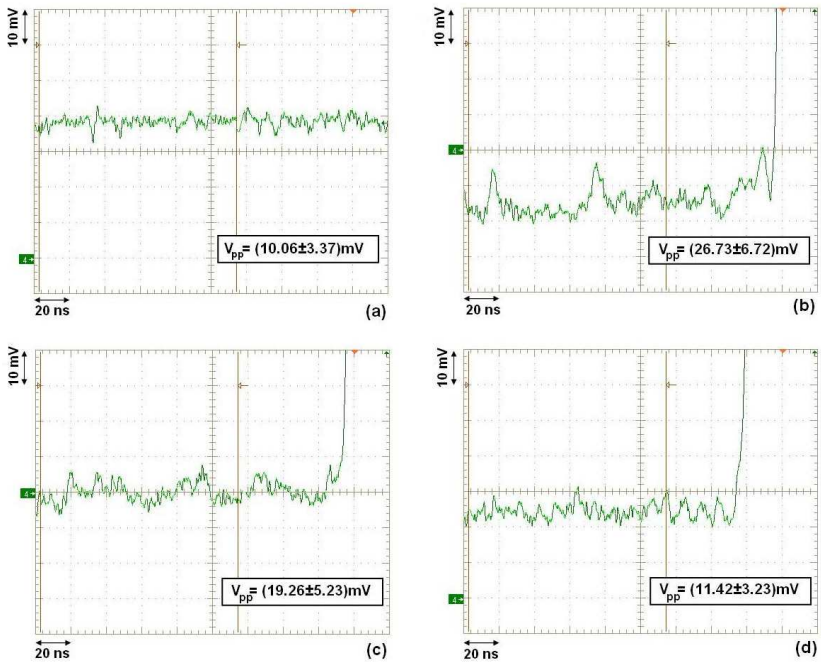


Figure 2.20 – Peak to peak noise at nodes V_{ARM} (a),V_{SPT} (b), V_B (c) and V_G (d) for setting TH and WALK thresholds (cf. figure 2.13).

As already discussed, the dead time of the CFD is defined by evaluating the time difference between the fall edges of RST and CK pulses. The histograms of the dead time in the OB and NB along with the corresponding Gaussian fits are depicted in figure 2.21. The measurements have been performed without any source but exploiting the natural scintillator radioactivity. Measured data are in

agreement with simulations of figure 2.17 and show a significant improvement of the NB with respect to the old configuration. Signal dispersion is also reduced.

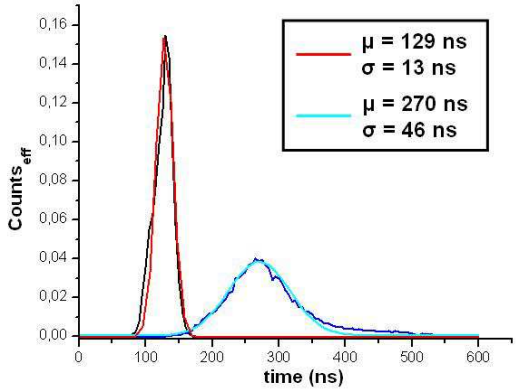


Figure 2.21 – Dead time distribution in the OB (blue) and NB (black). Gaussian fits are superimposed (light blue for the OB and red for the NB). Counts are normalized to the total number of events.

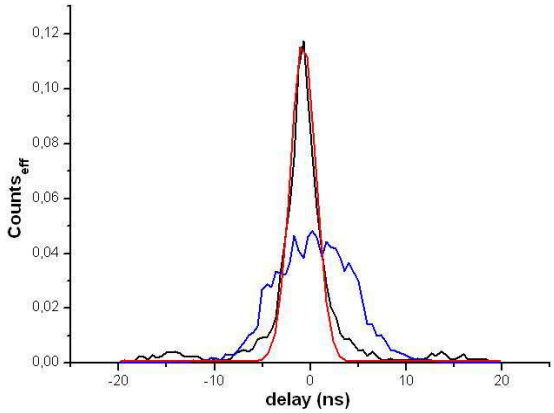


Figure 2.22 – Time delay distribution in the OB (blue) and NB (black). Gaussian fit of the NB is superimposed (red). Counts are normalized to the total number of events.

Another important figure of merit to consider is the timing resolution of the PET system which is defined as the minimum time window of the scanner to detect coincidences. This can be quantified by measuring the delay between pairs of triggers associated to events in coincidence, thus requiring the use of a source (^{22}Na in the measurement) to be placed within the two heads. The resulting histograms are shown in figure 2.22. Since the distribution in the old front-end has a no “standard” behaviour, the FWHM is evaluated which gives a standard deviation σ of 4 ns and a mean value μ of -1.2 ns. On the other hand, a Gaussian fit (red in figure 2.22) can be performed for the NB data, thus providing μ = -0.75 ns and σ = 1.32 ns. In both the two cases, the negative mean value is due to the signal taken as a reference during the measurements which arrives later with

respect to the other trigger, as confirmed by inverting the oscilloscope probes. This may be caused by slight different threshold levels in the two heads. The measured data show that the timing resolution of the NB is improved compared to the original configuration given that the variance is less that a half with respect to the OB.
Furthermore, the ^{22}Na spectrum has been reconstructed in order to compare the energy resolution of the two readout boards. To this end, the events corresponding to different energy levels which are collected by each pixel have been summed up and normalized to the total number of events. Therefore, the energy resolution (ER) can be determined as the ratio of the FWHM of the energy variation to the energy peak:

$$ER = \frac{\Delta E_{FWHM}}{E_{peak}} \tag{25}$$

From equation (25), ER of (24.6±1.0)% and (18.6±0.6)% at 511 keV have been obtained for the original board and PA-D, respectively. Thus, the new electronics exhibit improved timing performances as well as a better energy resolution with respect to the old front-end. A qualitative comparison can be derived from the images of the crystal pixels acquired with the two readout boards and reported in figure 2.23.

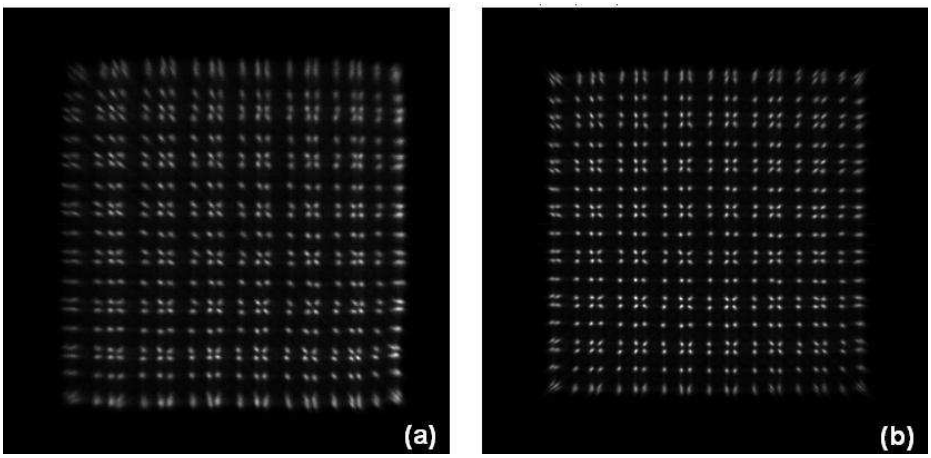


Figure 2.23 – Reconstructed images of the crystal scintillator pixel matrix acquired with the old electronics (a) and PA-D (b).

In both the two pictures, lateral pixels are not well resolved because the common centroid algorithm is not valid at the borders of the matrix. However, central pixels are better resolved in the acquisition obtained with the new front-end. It is worth noting that the reconstructed pixel matrix has a defined pattern (paired pixels followed by singleton) which differs from the expected regular matrix. This is due to the different size of the scintillator pixels compared to the PMT anodes so that the common centroid technique alters the effective positions in the reconstructed image. However, a simple look-up table is sufficient to restore the effective pixel position.

2.4. Conclusions and future work

According to the experimental results, the performance of the new front-end fulfils the goal of the project. A significant reduction of both the dead time and the timing resolution, as well as an improved energy resolution have been extensively proven. Table 2.3 offers a comparison between the old and new front-end characteristics.

Table 2.3 – Performance comparison between the old and the new front-end.

Figure of merit	Old front-end	New front-end
Dead time (ns)	(270 ± 46)	(129 ± 13)
Time resolution (ns)	(-1.2 ± 4)	(-0.75 ± 1.32)
Energy resolution (%) at 511 keV	(24.6±1.0)	(18.6±0.6)

Given the availability of such faster readout electronics, some measurements have been carried out at the cyclotron facility CATANA of INFN-LNS in Catania (Italy). The PET scanner has been equipped with a 4 versus 4 detector module configuration with the two heads placed at a distance of 14 cm. Passively collimated proton beams of 36 mm diameter and 62 MeV initial energy have been delivered impinging onto a PMMA (poly-methyl methacrylate) target. The experiment has demonstrated that the PET system is able to sustain the single photon count rates and acquire coincidences during the beam delivery (full in-beam measurement), in conditions of sub-clinical beam currents [75-76]. Further experiments have been performed at the Italian National Centre for Oncological Hadron Therapy (CNAO) in Pavia (Italy) using beams in the energy range of 93 – 112 MeV impinging on a plastic phantom. The performance of the PET prototype has been studied in terms of the ability to determine the proton fall-off position. The results have shown that the achieved spatial resolution is sufficient to extend the studies to both composed and anthropomorphic phantoms [77]. Studies on pixel identification enhancement of the scanner have been performed as well. To this end, different ultra-transmitting (UT) glasses have been inserted between the crystal and PMT in order to promote light spread and avoid overlap of responses. The experimental results have shown that this technique enables to identify pixels located within the inactive areas between two photodetectors [78].
Supported by the promising results of the PET prototype, a commercial scanner is under development at INFN.

3. DESIGN OF A MULTICHANNEL TIME TO DIGITAL CONVERTER FOR TOF PET

In this chapter, the design of an integrated CMOS time to digital converter is discussed which has to be exploited for the time of flight measurement in a PET/MRI system. The main characteristics to be accomplished include the time resolution, a multichannel topology feasibility, SiPM dark noise management and linear behaviour. The chip will communicate with a front-end in order to read out the photodetector output pulses. Digitized time and energy data will be forwarded to external electronics for post processing. The work has been supported by the 4DMPET collaboration.

3.1. The 4DMPET project

As extensively discussed in chapter 1, the combination of both the morphological and functional information in medical imaging provides a better diagnosis and prognosis. The implementation of hybrid systems combining PET with MRI within the same facility leads to better contrast in soft tissues with respect to PET/CT and addresses most of the problems related to tandem-configured scanners. Furthermore, PET image quality benefits from the time of flight feature in terms of signal to noise ratio. However, the TOF information requires an increased time resolution compared to conventional PET, thus demanding for fast electronics, scintillator and light detectors such as SiPMs.
The 4DMPET (4 Dimensions Magnetic compatible module for Positron Emission Tomography) project aims to design a PET detection module capable of working inside a MRI system. The module is based on the combination of a single LYSO scintillator crystal coupled to SiPMs which allow a high precision in the determination of the x and y coordinates of the event. Moreover, SiPMs are magnetic field compatible detectors and therefore are suitable for combined PET/MRI. Compared to APDs, SiPMs exhibit a higher gain (10^6 c.f. 10^2) which is less sensitive to temperature variations and makes it possible to exploit the time of flight technique. The detection module will also feature the depth of interaction information related to the z coordinate of the gamma rays inside the crystal. This reduces the parallax error in the determination of the LOR by minimizing errors due to non-colinearity of the annihilation photons. The arrival time and the energy of the events will be measured by integrated readout electronics in order to implement a compact detection module which can be used as a basic element for a PET ring.

3.1.1. TOF PET/MRI block detector

In figure 3.1 the block layout is depicted. The LYSO scintillator slab (A in figure 3.1b) has a size of 48 x 48 x 10 mm^3 with a decay time of 41 ns; spatial resolution optimization is achieved by painting the side faces of the crystal black. Both on the top and at the bottom of the scintillator a SiPM layer is laid out (B in figure 3.1b) featuring 16 x 16 square pixels with 3 mm pitch and a microcell size of 50 μm. The two SiPM layers are read out by independent and identical electronics (C in figure 3.1b); every board is made up of multiple channels each one reading one SiPM pixel output. Figure 3.1c shows a top view of the detection module where

the electronic blocks are highlighted: (i) four front-end (FE) application-specific integrated circuits (ASIC), each featuring 64 channels, for time and energy measurement; (ii) a cluster processor (CP) ASIC for data reduction; (iii) a laser driver/photodiode receiver/clock reconstruction (LD) ASIC for communication with an external data acquisition system through optical fibres (OF).
All ASICs communicate through low voltage differential signalling (LVDS) pads for magnetic field compatibility and have to be mounted and wire-bonded without package; encapsulation for protection and top-side contact cooling will be performed after test [79].

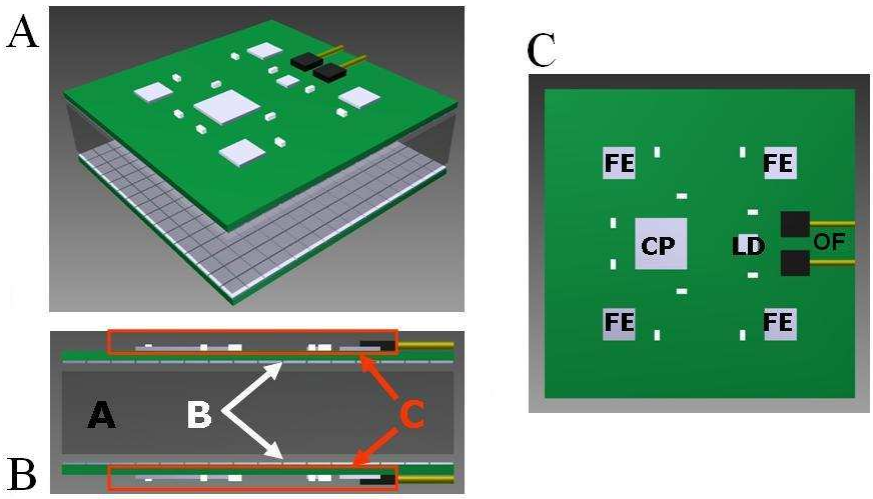


Figure 3.1 – Block detector layout: 3D view (a), side view (b) and top view (c).

In order to implement the TOF technique, a time resolution of σ = 100 ps is required if the SiPM jitter of 60 ps is considered [80] along with other system block contributions. Such resolution can be achieved if events are triggered on a low threshold (TH_{low}), which corresponds to the first emitted photoelectron so as to measure the interaction time within the crystal with high accuracy. However, the high SiPM dark noise of ~2 MHz/mm^2 at room temperature (dark count for SiPMs manufactured by FBK-irst [81]) requires the additional use of a validation threshold TH_{high} (corresponding to a programmable number of emitted photoelectrons) to discriminate events from noise as in a double threshold technique. Simulations have shown that a resolution of σ = 102 ps can be achieved [82]. Once a valid event has been detected, the system translates the relevant timestamp into a digital word by a converter and evaluates the associated energy by exploiting a time over threshold (TOT) technique. The best IC implementation of the discussed double threshold technique can be implemented with the aid of two different CMOS technologies. Therefore, the FE ASIC has been split up into two separated chips which communicate with each other: a current-mode (CM) ASIC which converts all SiPM analogue outputs into digital pulses and a time to digital converter (TDC) which provides both TOF and TOT information of valid pulses only.

3.1.2. Time to digital converter requirements

The readout circuitry of the TOF PET module is based on a current-mode ASIC with low input impedance, fast current buffer as very first detector front-end [83]. Such architecture is implemented in AMS 0.35 μm SiGe-BiCMOS technology featuring both MOSFET and fast HBT bipolar transistors. This allows achieving a time resolution of ~100 ps FWHM given the very low input impedance (17 Ω) of the current buffer which leads to a short time constant even when combined with the large SiPM capacitive load. Furthermore, a wide bandwidth of about 1 GHz ensures a very short rise time of the response, which limits the jitter due to noise. Power consumption is also controlled at reasonable values, thanks to the large transconductance/current ratio offered by the HBTs. The CM ASIC reads out the SiPM output current and translates it into a digital pulse whose rise edge timestamp represents the arrival time of the signal (TOF data) while the fall edge timestamp provides its energy information (TOT data). In the occurrence of a SiPM outputs dark current (noise), a fixed width short pulse is generated. The block diagram of the circuit is depicted in figure 3.2.

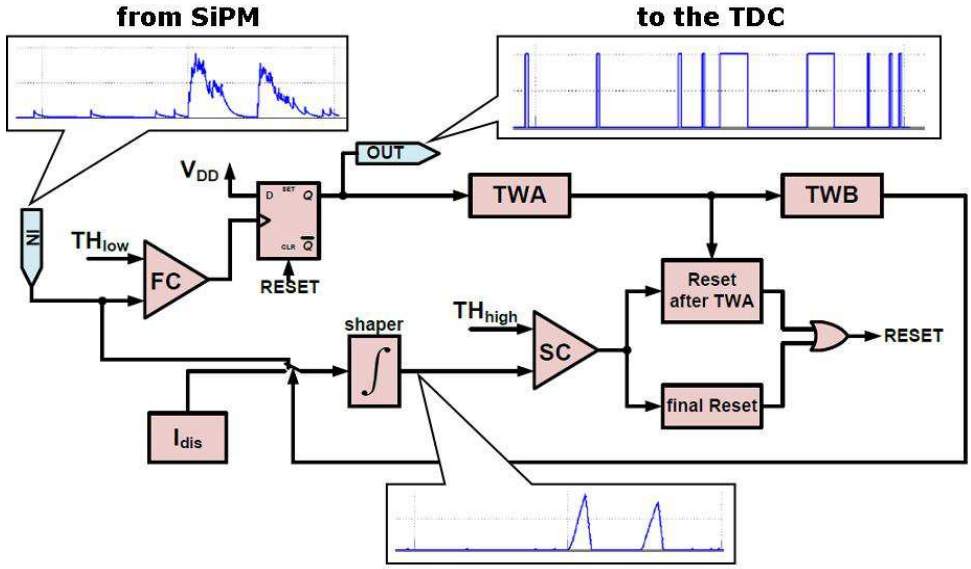


Figure 3.2 – Block diagram of the CM ASIC. Simulated signals are also reported.

The working mechanism is the following. A SiPM output signal is compared with the low threshold TH_{low} by a fast comparator (FC) at the input of the circuit. As soon as the input goes over TH_{low}, the FC sets a flip-flop which in turn triggers a counter labelled as Time Window A (TWA). At the same time, a shaper starts integrating the input so that its output, which feeds a slow comparator (SC), increases from zero. When TWA expires the system evolves towards two different statuses according to the value of the SC output. If it is 0, the SiPM signal is recognized as noise because the shaper output is below the validation threshold (TH_{high}); the circuit resets itself and a digital pulse with duration of TWA is produced at the circuit output. If it is 1, a second counter labelled as Time Window B (TWB) is triggered and the shaper keeps on integrating the SiPM output; when TWB

expires the shaper is discharged through a constant current (I_{dis} in figure 3.2), thus decreasing its output. As soon as the shaper output goes below TH_{high} the circuit resets itself. The circuit outputs a digital pulse having duration of TWA plus TWB plus the time required by the shaper to be discharged: this time is proportional to the energy associated to the event and thus it represents the TOT information. For calibration issues, the counters TWA and TWB will be programmable within the time intervals (6 – 30) ns and (50 – 120) ns, respectively. It follows that noise pulses are shorter than valid pulses and can be easily distinguished and discarded. On the other hand, the rising edge of a valid pulse provides the timestamp of its associated event while the trailing edge contains the energy information.
The CM ASIC digital outputs have to be forwarded to a time to digital converter (TDC) ASIC to measure and digitize both the TOF and TOT data of the events while neglecting noise pulses. The timing information must be evaluated with a resolution below 100 ps so as not to compromise the block resolution of 102 ps as previously discussed. On the other hand, the non-linear, constant current discharge mechanism of the charge integrated during TWA and TWB in the CM ASIC eliminates any constraint on the stability and uniformity of the SiPM pulse and relaxes precision requirements in the TDC for the TOT assessment, while preserving a good linearity. Thus, sub-nanosecond precision is sufficient for the TOT evaluation. A strictly linear behaviour is required in performing the measurements since PET examinations are not repeatable and no statistic correction can be applied to the acquired data. Moreover, noise pulses must be recognized and discarded in real time by the TDC ASIC without impairing the system acquisition capabilities. Given the required compactness of the TOF PET/MRI module, a simple and regular topology must be implemented for the converter in order to allow for multichannel feasibility. The TOF dynamic range must be in the order of milliseconds, as demanded in PET applications. Finally, serial communication is required at the output of the chip in order to forward TOF and TOT data to the cluster processor for image signal processing purposes. Table 3.1 summarizes the main characteristics required to the TDC ASIC.

Table 3.1 – Design requirements for the TDC ASIC.

TOF resolution	< 100 ps
TOT resolution	< 1 ns
Linearity (DNL, INL)	< 0.1 LSB
Dynamic range	> 1 ms
Topology	Multichannel
Output communication	Serial at f < 100MHz
Other features	Real time noise rejection

Finally, some considerations about the input characteristics have to be made which are related to the considered SiPMs. Since in preclinical studies a Poisson distributed data rate of 100 kHz/cm^2 is expected, which lowers down to 10 kHz/cm^2 for clinical applications [84], the choice of 3 x 3 mm^2 SiPM pixels leads to an input data rate of 9 kHz and 900 Hz in preclinical and clinical applications, respectively. However, noise is superimposed to events. As previously mentioned, dark noise rate approximates to 2 MHz/mm^2 for single events, which corresponds to 18 MHz for each SiPM channel [85]. These data have been considered during the design.

3.2. State of the art of TDC

Time to digital converters are electronic components which quantize small time differences between two signals (referred to as start and stop) and provide a digital representation of this time interval, as depicted in figure 3.3. Technology progress, increased integration level capability and working speed have led to significant improvements in the time measurement performance. Some examples involve the time resolution [86], linearity [87], dynamic range [88], power consumption [89] and low process-voltage-temperature (PVT) variations [90] of the converter.

The operation of a TDC is very similar to that of analogue to digital converters (ADC) although the former deals with the time difference rather than voltage or current differences. The measured time is evaluated as the phase difference between the positive edges of the start and stop signals. Thus, the input is defined in the continuous time domain whereas the output is expressed in digital form. The transfer characteristic is similar to that of ADCs, with the real behaviour deflected from the ideal curve because of quantization errors, as shown in figure 3.3c.

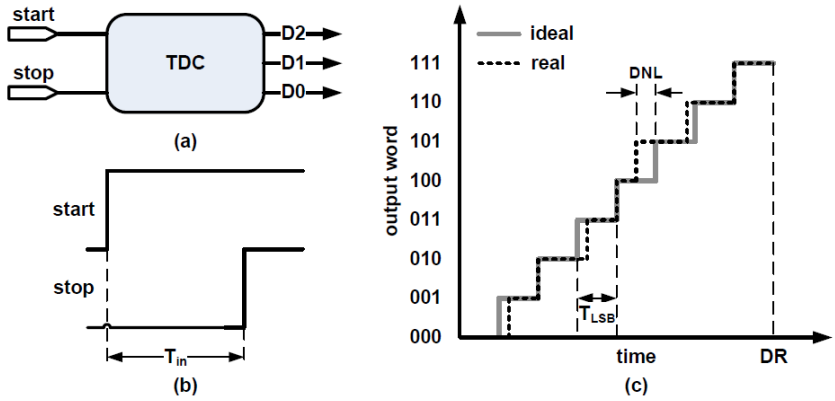


Figure 3.3 – Working mechanism (a-b) and characteristic transfer curve (c) of a 3 bit TDC. Component mismatches and noise cause the real transfer curve to deflect from the ideal condition, generating quantization errors (adapted from [91]).

The measured time T_{in} is related to the output digital code according to the following expression:

$$T_{in} = T_{LSB} \cdot \sum_{k=0}^{k=n-1} D_k \cdot 2^k \qquad (26)$$

where T_{LSB} is the minimum unit of time measurement, n is the number of bits and D_k are the output digits.
Most of the figures of merits of TDCs are directly derived from those of ADCs, with some additional features, as follows [91-92]:

- *Least significant bit T_{LSB}* is the ideal code bin width referred to the input time interval.
- *Minimum interval* refers to the shortest measurable time interval.
- *Dynamic Range (DR)* is defined as the difference between maximum and minimum measurable time intervals. For an ideal n-bit TDC, DR is given by:

$$DR = 2^n \cdot T_{LSB} \tag{27}$$

- *Single-shot precision* σ is the standard deviation of the measurement distribution when a single time interval is evaluated repeatedly, under repeatability conditions.
- *Noise* refers to any deviation between the output (expressed in input units) and the input signal. It includes both random and systematic noise sources.
- *Differential nonlinearity (DNL)* is the deviation of the output bin size from its ideal value of 1 LSB. DNL in the i-th bit is given by:

$$DNL_i = \frac{T_{LSB}^{id} - T_{LSB}}{T_{LSB}} \tag{28}$$

  where T_{LSB}^{id} and T_{LSB} are the i-th ideal and actual code bin widths, respectively.
- *Integral nonlinearity (INL)* is defined as the deviation of the step position from its ideal value normalized to one T_{LSB}. Assuming that both gain and offset correction have been performed, INL in the i-th bin is given by:

$$INL_i = \sum_{k=0}^{i-1} DNL_k \tag{29}$$

- *Dead time* is calculated as the shortest time interval between the end of a measurement and the start of the next one.
- *Double hit resolution* refers to the minimum time interval between two consecutive input samples that can be resolved by the converter.
- *Measurement rate* is the frequency at which the TDC provides digital output words.
- *Offset variation* is related to the delay that the sampling signals experience when passing though the converter. It is usually calibrated at start-up time by direct measurement of the propagation delay.
- *Calibration* relates to the adjustment of the transfer function to the ideal curve. It can be performed either offline or online. In the first case, if the calibration reference does not depend on environment variations, calibration can be

executed only once during the converter lifetime; otherwise, a periodic correction is required. In both the two situations, some conversion dead time occurs. On the other hand, a continuous online calibration which is performed in a non-intrusive way (auto-calibration) prevents from dead time penalty, thus continuously minimizing the conversion error [93].

- *Power dissipation (P_d)* is the power consumed by the device during its operation. It includes both static and dynamic power. The former is given by the product of static consuming current and the power supply voltage V_{DD}:

$$P_{static} = V_{DD} \cdot I_{static} \tag{30}$$

The dynamic power is related to the switched capacitors and the working frequency as well as to the voltage supply:

$$P_{dynamic} = \alpha C \cdot V_{DD}^2 \cdot f \tag{31}$$

where α is the active factor (0 < α < 1).

- *Stability* depends on the TDC behaviour against PVT variations. It can be expressed in resolution deviation ΔLSB and measured in units of LSB.
- Other features include system clock, technology used, dimension, packaging, pinouts, amount of analogue vs. digital processing, number of digital functions, circuit complexity and ease of design.

The traditional approach to time-to-digital conversion is first to convert the time interval into a voltage (*analogue TDC*). Thereafter, this voltage is digitized by a conventional ADC [94].The time to analogue conversion (TAC) is usually based on current integration where a charge pump is used to charge/discharge a capacitor. Then, a sample-and-hold circuit provides a stable voltage signal to the ADC, as depicted in figure 3.4. The performance of such TDCs is strictly related to the integrated precision of both the current and capacitance values as well as to the ADC resolution; since analogue circuits are used, this topology is not suitable for technology scaling.

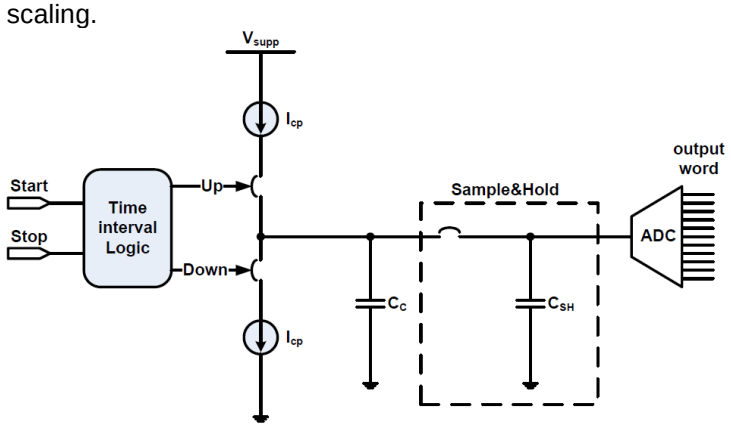


Figure 3.4 – Schematic of the analogue approach for TDC (adapted from [91]).

A second generation of TDCs makes use of the digital approach (*fully digital TDC*). The topology can be based on the use of counters which provide a measurement of the time interval in terms of the counted number multiplied by the clock period, like the example shown in figure 3.5. The main advantages of this approach are the wide dynamic range and the possibility to implement the design in several technologies like CMOS/BiCMOS process, FPGA and GaAs superconductive process. However, the resolution is limited by the clock frequency and the conversion time depends on the counted periods. As such, this topology alone is not suitable in high-precision time interval measurements.

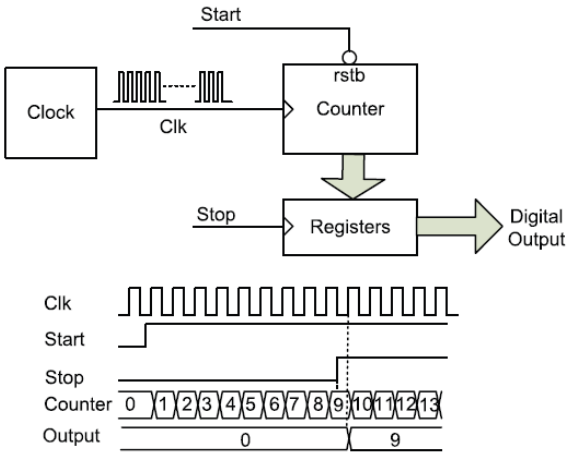


Figure 3.5 – Counter-based TDC. The counter runs at the clock frequency and is reset by the start signal. The output bits are sampled by the stop pulse [91].

Another approach is based on *multiphase sampling* by means of a digital delay line (DL) where a start signal is synchronized to the positive edge of the reference clock and delayed replicas are generated with a fixed gate delay. Then, the states of the delayed clocks are sampled in parallel by a common stop signal. This results in a thermometer code since only delay stages already passed by the start signal give a high value at the outputs of the sampling elements. The position of the high-to-low transition in the thermometer code eventually informs about the distance between the start and stop signals, thus providing a measure which can be easily converted to the binary form [95]. This topology is mainly limited by the minimum gate delay time which depends on the technology and by PVT variations. However, if a delay locked loop (DLL) is used, the overall delay of the DL chain is kept constant over pressure, voltage and temperature fluctuations. A DLL is a chain of n delay elements with a control loop which keeps the input (clock) and the last delayed output in phase. If T_{CK} is the clock period, the DLL produces n outputs phase shifted of T_{CK}/n, as depicted in figure 3.6. This leads to:

$$T_{LSB} = \frac{T_{ck}}{n} \tag{32}$$

From equation (32) it follows that increasing the number of delay stages reduces the LSB. However, long DLL chains suffer from non-linearity as mismatches occur

when a large number of elements are used. Thus, great care must be taken at layout stage if linear performance is an issue.

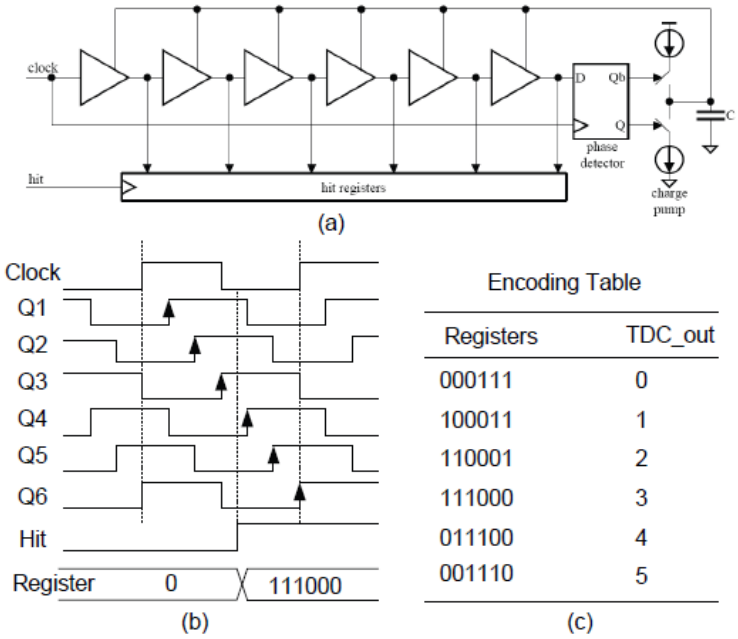


Figure 3.6 – DLL-based TDC. Schematic analogue implementation (a), sampling diagram (b) and encoding table (c) [91].

A solution to gate delay limit is given by the use of techniques which lead to smaller time taps such as DLL arrays and Vernier delay lines (VDL). These topologies are grouped together within the *sub-gate delay TDC* class. DLL arrays (ADLL) make use of two types of DLLs having length of n and m and with different cell delay T_n and T_m, respectively. The bin size of the TDC can be expressed as:

$$T_{LSB} = T_m - T_n = T_{ck}\left(\frac{1}{m} - \frac{1}{n}\right) = \frac{T_{ck}}{n \cdot F} \tag{33}$$

where F is the number of DLLs with n delay cells. Thus, increasing n and F leads to a smaller bin size down to a few picoseconds [96]. However, DLL arrays are affected by jitter and offset within the chains which lead to non-linearity issues as in conventional DLLs. In addition, large arrays dissipate high static power, thus requiring low-power design. Finally, outputs with pseudo binary codes are generated since it is not possible to produce multiphase clocks with a number of a power of 2. In figure 3.7 the scheme of a DLL array-based TDC is depicted.
In VDL-based converters, the principle of Vernier callipers is applied. Two scales are used: a reference scale, with a time bin T, and the Vernier scale, with shorter time bin but spanning the same number N of reference bins. Thus, the converter bin size is evaluated as the difference between the two scales [97-98-99]. The main drawback of this technique arises from the accumulation of non-linearity along the Vernier delay line. Other techniques based on the Vernier difference exist. They are based on the use of two DLLs along which the start and stop signal

travel. The output phases are connected to the D and CK inputs of flip-flops, respectively, so that the first flip-flop which is not set provides the time interval between the two pulses. However, this topology is affected by dead time between measurements, requires frequent calibration and exhibits limited dynamic range. As an alternative, ring oscillator-like DLLs can be used which expand the DR available. Nevertheless, non-linearity accumulation occurs and a calibration circuit is still required [93].

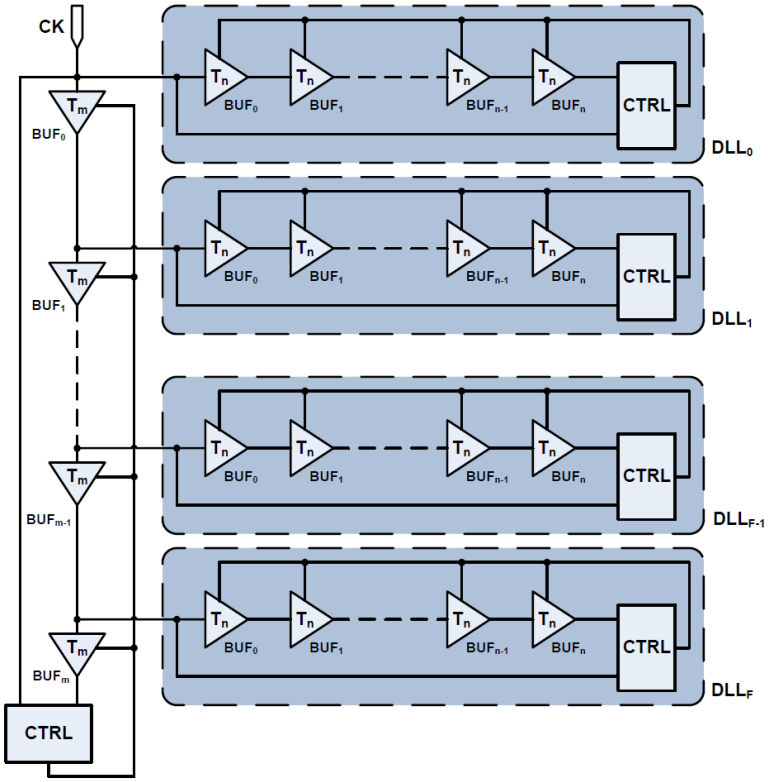


Figure 3.7 – ADLL-based TDC.

The last TDC class includes special architectures that exploit technology progress to provide sub-picosecond resolution. Cyclic TDC using pulse shrinking delay line (see figure 3.8a) is based on a DL with delay cells having different gain [100-101]. The time interval to be measured cyclically passes through the DL and is progressively shrinked because of the difference of the input capacitance and equivalent on-resistance of the DL elements. After a fixed time interval, the output signal is generated without positive edge and feeds a high resolution counter which provides a digital output proportional to the time interval. This architecture has the advantage to be purely digital so that it can be implemented both in CMOS technology and on FPGA. In addition, it is low power consuming and can reach a bin size down to a few picoseconds.
Gated-ring oscillator (GRO) TDC (see figure 3.8b) provides multiphase sampling with high resolution [102]. It is based on a ring oscillator whose operation is only

enabled during the time interval to be measured. The ring phases are used as clock inputs for counters whose counts are summed up to provide the measurement. The bin size can be lowered down to 100 fs; mismatch among the ring elements is not an issue, thus leading to good linearity. Furthermore, the low static power dissipation along with a fully digital topology make this approach a good choice for sub-picosecond applications. However, electronic noise, metastability and non-oscillation are the main issues of this topology.
Another architecture that provides a sub-picosecond bin size is based on time amplification (TA). TA can be developed in order to facilitate the measurement of time intervals in circuits whose magnitudes are decreasing with technology progress. Its principle is based on stretching the input time interval with constant gain [103]. Then, the resulting amplified signal is forwarded to the TDC core, as reported in figure 3.8c.

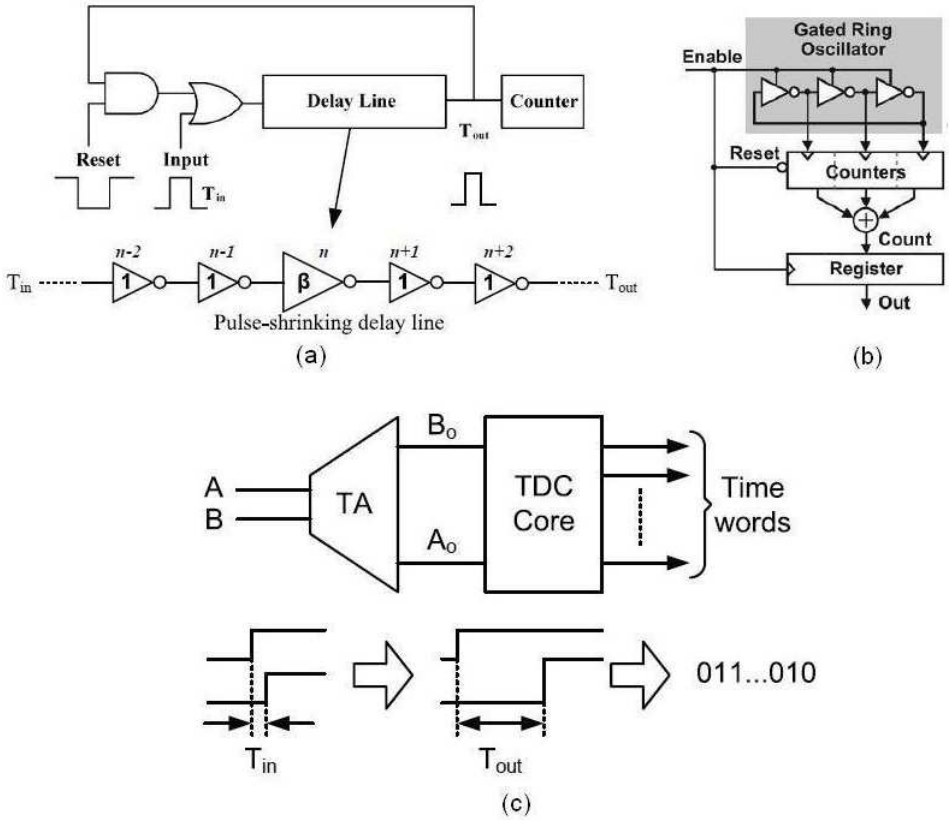


Figure 3.8 – Sub-picosecond TDCs. Cyclic TDC using pulse shrinking DL (a), GRO-TDC (b), TA-based TDC (c) (adapted from [91]).

According to the specific application the TDC is intended for, different performances can be required. Thus, custom architectures are usually employed which combine two or more topologies. Usually, a counter-based TDC offers wide DR whereas high precision can be obtained using time-interpolation and multiple sampling techniques. The most common hybrid topologies include a combination of

a counter with a single DLL or a DLL array, whit the counter providing a coarse time information whereas the DLL (either single or in an array form) producing a fine measurement; multiphase flash sampling together with a Vernier DL is a frequent choice as well. In addition, TA can be used to enhance the resolution performance in both the two cases [91].
The employment of TDCs is increasingly spreading in the electronics for several fields of applications such as object and person monitoring, land and sea surveying, laser/radio ranging, medical applications, high energy physics, time domain reflectometry, phase meters, frequency synthesis, automatic test equipment and on-chip jitter measurements. Among these, some TDCs specifically designed for TOF PET can be found in literature. Analogue DLLs are largely used individually [104-105], in combination with counters [106] or in array configuration [107-108], although they generally exhibit either poor resolution or linearity. In particular, optimal resolution along with multichannel feasibility is achieved in [109], where dual counters together with a DLL coupled to RC lines are used. However, high values of INL are observed. Time to analogue conversion coupled to a digital counter is exploited in [110] with acceptable values of both resolution and linearity but such topology is not suitable for multichannel implementation. Other approaches include ring oscillators (RO) for fine time measurement coupled to counters for DR extension [111-112] featuring small area occupation and FPGA-based TDC [113].

3.3. Proposed TDC architecture

Given the requirements summarized in table 3.1, the best TDC topology has been defined for the specific TOF PET application.
The need for multichannel feasibility implies the implementation of a simple architecture which can be easily replicated. As such, the use of a digital counter can be the optimal choice which offers wide dynamic ranges as well. Furthermore, since the resolution requirements for the TOF and TOT measurements are not significantly challenging, a sub-picosecond approach is not necessary. On the other hand, sub-gate delay topologies can be extremely power consuming for multichannel implementation (ADLL) or require strong calibration efforts (VDL). As such, a single DLL coupled to the counter can be a good option if a sufficiently small gate delay is available. Thus, a deep sub-micron technology must be used which is capable to offer a gate delay in the range of a few picoseconds. However, linearity is an issue in PET examinations so that a short chain should be employed so as to minimize mismatches. As a consequence, a high speed clock must be used. Indeed, according to equation (32), T_{CK} has to be reduced in order to get a small LSB if the number n of delay cells is kept small. Nevertheless, high speed is an issue in counters with a large number of bits which are required to provide large DR. The carry propagation along the counter blocks limits the maximum working frequency when increasing the number of bits. This problem can be addressed by using a pipeline architecture where local communication between adjacent cells arranged in a systolic array fashion is exploited to implement the counting function with almost no frequency dependency. In a systolic array, computations are performed simultaneously in all processing elements (referred to as *systolic cells*), while data travel from cell to cell. When moving between cells, partial results are computed in a pipeline fashion so that parallelism is exploited by partitioning the

computation effort over the array cells. Communication within the array and with the external world is performed at the same time, thus providing high performance. Other features of systolic arrays include modular expandability, simple and regular data and control flows, simple and uniform cells and efficient fault tolerant schemes [114]. Then, a systolic array-based counter coupled to a short DLL implemented in a high performing CMOS technology is the most suitable TDC architecture for the target application. In addition, an all-digital implementation for the DLL (ADDLL) provides better performance over analogue designs in terms of PVT sensitivity, locking time, circuit complexity, low voltage supply, occupation area and easy migration to advanced technology [115-116-117].
In this scenario, three sub-micron technologies have been considered: UMC 130 nm, UMC 90 nm and UMC 65 nm, all of them supported by the Europractice IC Service. Simulations of a 5 stage ring oscillator (RO) and of a 4 bit systolic counter (SyC) have been performed in order to survey the clock speed that can be achieved with each technology. The results are listed in table 3.2 along with some technology features.

Table 3.2 – Features and performances of the three UMC technologies considered.

	Nominal gate delay [ps]	Core V_{DD} [V]	Block size [µm]	f_{max} RO [GHz]	f_{max} SyC [GHz]
UMC 130 nm	14	1.2	1525x1525	4.5	3.5
UMC 90 nm	9.8	1.2	1875x1875	8.2	5
UMC 65 nm	8.1	1.2	1875x1875	9.9	5

According to the information collected, UMC 65 nm has been selected for the TDC design, given the short gate delay applicable to the DLL and the high working frequency that can be sustained by the systolic counter. Although a higher number of bits has to be implemented for the SyC in the converter, its maximum speed should stay the same unless some clock skew occurs which can be managed with an accurate clock tree network distribution. Post-layout simulations of the SyC in worst case conditions (slow process, 90% V_{DD} and 40°C) have shown that a maximum working frequency of 2.5 GHz can be achieved which has been fixed as the system clock for the TDC (see figure 3.9). Since UMC 65 nm has no phased locked loop (PLL) available in library, a tuneable RO is used as a clock generator. However, RO suffers from PVT fluctuations, thus providing poor clock stability. Then, the TDC has been designed so that the whole circuit follows the clock speed dictated by the RO according to the process, voltage and temperature sensed by the circuitry. This results in poorer time resolution when frequency is lowered down but ensures a correct functionality of the converter in all conditions. Furthermore, since different speed may result in distinct chips, one of the TDC channels is fed with an external reference signal for off-chip calibration purposes.
Given the size available from the foundry service, 8 channels can be housed within one chip. A 4 stage ADDLL is global for all of them whereas two 10 bit systolic counters are placed symmetrically so as to feed four channels each. In normal

conditions when the chip runs at a working frequency of 2.5 GHz, the LSB of the systolic counter equals 400 ps. This offers a good resolution for the measurement of the TOT information so that sampling the counter on the trailing edge of the input pulse is sufficient for deriving correct energy information. On the other hand, feeding a 4 stage ADDLL with the 2.5 GHz clock leads to a timestamp of 100 ps since each delay cell provides a replica of the input clock with a delay of $T_{CK}/4$. Thus, sampling both the systolic counter (coarse time) and ADDLL outputs (fine time) on the leading edge of the event provides TOF information with a nominal resolution (single-shot precision) of:

$$\sigma_{TOF} = \frac{T_{LSB}}{\sqrt{12}} = \frac{T_{CK}}{n\sqrt{12}} = 28.9\,ps \qquad (34)$$

In a first approximation, this value satisfies the system requirements although other noise sources come to play when chip measurements are performed.

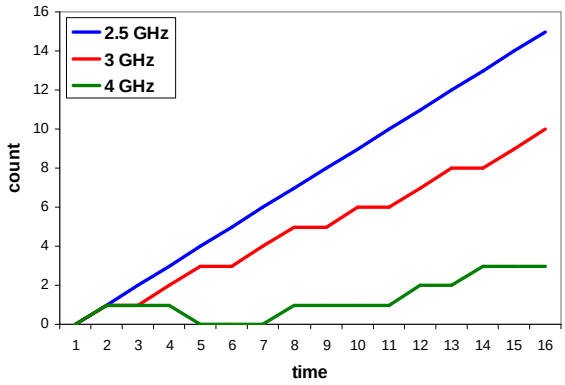


Figure 3.9 – Post-layout simulations of the 4 bit systolic counter in UMC 65 nm at 90% V_{DD}, 40℃ and slow process.

According to what stated so far, the following mechanism is implemented within the TDC architecture. When an event occurs, the clock phases generated by the delay line as well as the output bits of the systolic counters are sampled by hit registers which freeze the arrival time of both the leading and trailing edges of the input pulse. A validation section informs the system when data must be discarded (noise pulse). These operations are performed by a full-custom unit (FCU) at 2.5 GHz in normal conditions. If data are validated, sampled bits are serially forwarded to a semi-custom unit (SCU) where encoding and buffering are performed at 250 MHz. Thereafter, SPI-like communication provides the output word at a frequency that can be selected between 62.5 MHz and 31.25 MHz. The SCU has been designed in Verilog code and implemented with the standard cell library available from the technology. The FCU has been simulated in Verilog as well so as to test the performance of the complete system (FCU+SCU) when pulses are applied with a Poisson statistic distribution and featuring the typical widths of the CM ASIC data.

3.3.1. Full-custom unit

As briefly discussed, the full-custom unit represents the core of the TDC since TOF and TOT data are registered at this stage. Figure 3.10 illustrates the block diagram

of the components implemented in the FCU. Only one channel out of 8 is depicted along with the blocks which are common to all channels (red coloured) and include:

- A 5 stage tuneable ring oscillator with external enable.
- A 4 stage ADDLL (control loop blocks are not shown).
- A non-overlapping clock generator (NOCG) that provides the master/slave clock to the dynamic flip-flops implementing the pipeline communication at 2.5 GHz within the channels.
- A reset synchronizer which starts the two systolic counters of the chip at the beginning of a measurement.
- A multiplexer for clock selection among the 4 ADDLL output phases to feed the NOCG with the correct set-up and hold time required for data sampling.
- A systolic frequency divider (SFD) which reduces the frequency of the FCU of 10 times in order to generate the clock for the SCU.

Moreover, in figure 3.10 only one of the two systolic counters (common systolic counter, CSC) is shown which feeds 4 channels in a pipeline fashion with the 10 bits travelling horizontally respect to the blocks:
Each channel features five groups of elements:

- The sampler, which freezes the ADDLL output phases when it is triggered by the pulse generated by the front-end. In addition, the sampler generates the store commands to be sent to the hit registers.
- The TOF hit register (TOF-HR, light blue in figure 3.10) which includes 13 memory cells to store both the counter and ADDLL outputs on the leading edge of the input pulse, a store enable (ST-EN) block that prevents data corruption and an interface for serial communication with the SCU.
- The TOT hit register (TOT-HR, pink in figure 3.10) that is made up of 10 memory cells (plus 3 fake cells for pattern regularity) to store the counter bits on the trailing edge of the input, a data acquisition stop (DAQ stop) block to prevent data corruption and an interface block for serial communication with the SCU.
- The time window stage (TWS, green in figure 3.10) for input validation, including a 7 bit configurable systolic counter which is controlled by the count enable (CNT-EN) block and communicates with the SCU through the TW interface.
- A 12 bit systolic counter (pulse counter, PLS-C, yellow in figure 3.10) which counts the number of inputs (both valid and noise) sent from the CM ASIC.

After passing through the blocks belonging to the first channel, the 10 bits of the CSC are forwarded to the next channel and so on. Thus, the counter bits arrive to the second channel with a delay of 4 T_{CK}, to the third one after 8 T_{CK} and finally to the fourth channel after 12 T_{CK}. These delays will be accounted for during the reconstruction phase.

All configuration bits are provided by means of a scan chain (not shown in figure 3.10) which runs through the elements of the FCU and distributes data at a low frequency (i.e., 1 kHz provided by the user).

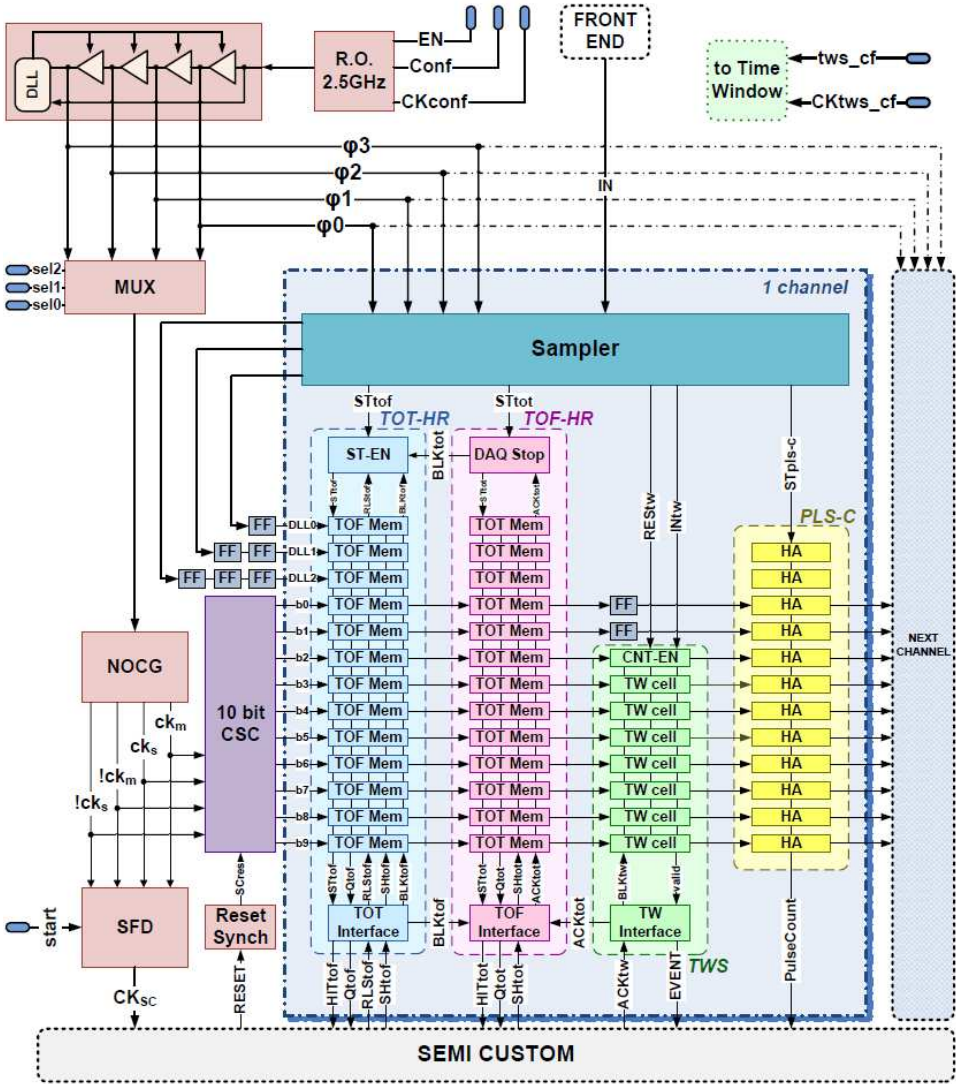


Figure 3.10 – Block diagram of the FCU. Red blocks are common to the 8 channels of the TDC whereas the systolic counter feeds 4 channels only in pipeline fashion.

3.3.1.1. Ring oscillator and all-digital delay locked loop

Ring oscillators are used in several electronic systems where a time reference is required for operation synchronization. Although ROs are expected to provide a perfect periodic waveform, in the real world noise phenomena corrupt the generated signals which are not perfectly periodic anymore. However, the demand for monolithic oscillators with low cost and low power dissipation is growing so that research efforts have improved the performance of ROs in terms of both speed of

operation and noise performance. RO implemented as a chain of delay elements has several attractive features such as low voltage operation, high oscillation frequency with low power consumption, electrical tuning within wide ranges and multiphase outputs [118]. The oscillation frequency is determined by the propagation delay per stage t_d and the number of stages. The self-sustained oscillation is obtained with a 2π phase shift and unity voltage gain along a ring of n stages: each delay element provides a phase shift of π/n whereas a remaining phase shift of π is given by dc inversion. It follows that a π phase shift is obtained each time the oscillating signal passes through the ring in $t = n \cdot t_d$. If the ring cells are implemented as inverter gates, an odd number k of elements must be used. Thus, couples of inverters form a time delay t_d, whereas the last inverter provides the inversion with a delay t_{inv}. After two rotations of the signal through the ring, a complete 2π phase shift is achieved (see figure 3.11) which leads to an oscillation frequency of:

$$f_{RO} = \frac{1}{\frac{(k-1)}{2}\left(t_d^{11} + t_d^{00}\right) + t_{inv}^{10} + t_{inv}^{01}} \qquad (35)$$

where t_d^{11} and t_d^{00} are the time delay between leading and trailing edges of the delayed signals, t_{inv}^{10} and t_{inv}^{01} are the high-to-low and low-to-high inverter delay, respectively.

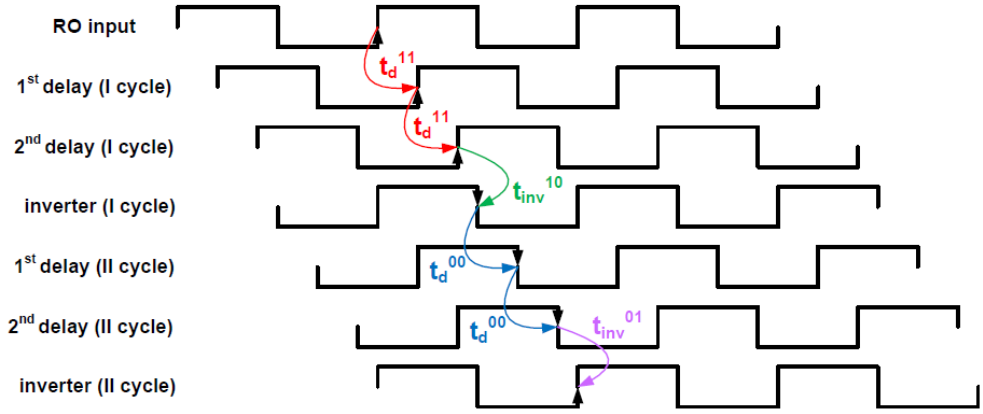


Figure 3.11 – Delayed waveforms at the outputs of a 5 inverter stage RO. Inverters 1-2 are grouped together as 1st delay, inveters 3-4 form the 2nd delay.

The RO implemented for the TDC is based on tuneable inverters where 8 varactors are used as externally configurable load at the output of each stage, as depicted in figure 3.12. Each cell has two outputs: one is used to connect elements in series within the chain whereas the other one provides an inverted version of the delayed signal through gate G to the output of the ring. This prevents the RO cells from being loaded when the clock signal is picked up at the output of an inverter G since its load contribution is already taken into account in the evaluation of t_d. It is worth noting that the fifth inverter is made up by the gate G of the fourth tuneable element in cascade with a NAND gate that receives the enable signal.

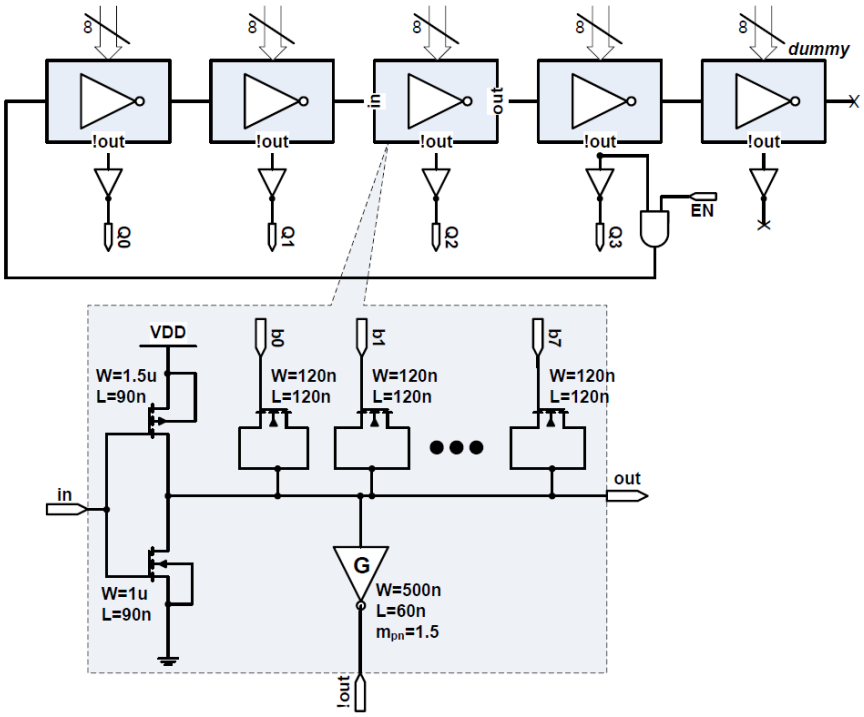


Figure 3.12 – 5-stage RO implementation (up) and detail of the delay cell (down).

The time delay of the cells in ideal conditions (typical process, 100% V_{DD} and T=27℃) and half-load configuration (only b_3,b_2,b_1,b_0 on) are listed in table 3.3.

Table 3.3 – RO cell delays in ideal conditions (post-layout values).

t_d^{11}	t_d^{00}	t_{inv}^{10}	t_{inv}^{01}	f_{osc}
69.7 ps	69.7 ps	70.1 ps	64.1 ps	2.51 GHz

As already discussed, the oscillation frequency of ROs is very sensitive to PVT fluctuations; however, clock variations due to temperature instability (see figure 3.13a) are in the order of a few percent and can be corrected by external tuning of the delay elements. Varactor-based tuning offers the capability to slightly modify the oscillation frequency for calibration purposes. The n-MOS capacitors are sized so that one bit adjusts the clock of about 1% within a range of around 200 MHz in typical conditions, as shown in figure 2.14. On the other hand, voltage fluctuations (see figure 3.13b) as well as slow (sp) and fast (fp) process corners significantly modify the clock frequency; in sp with all loads switched off, a maximum frequency of 2.08 GHz can be achieved whereas in fp corner the clock can be lowered down to a minimum value of 2.93 GHz with full load configuration and typical temperature and supply. Forcing the TDC to work at 2.5 GHz in the sp corner with a different RO cell configuration would lead to abnormal functioning, thus making the TOF and

TOT measurements impractical. As a consequence, the RO is left running at the frequency imposed by the process corner. Although slow process reduces the TDC resolution because of the lower clock feeding the ADDLL, this design ensures a correct behaviour no matter the working conditions.

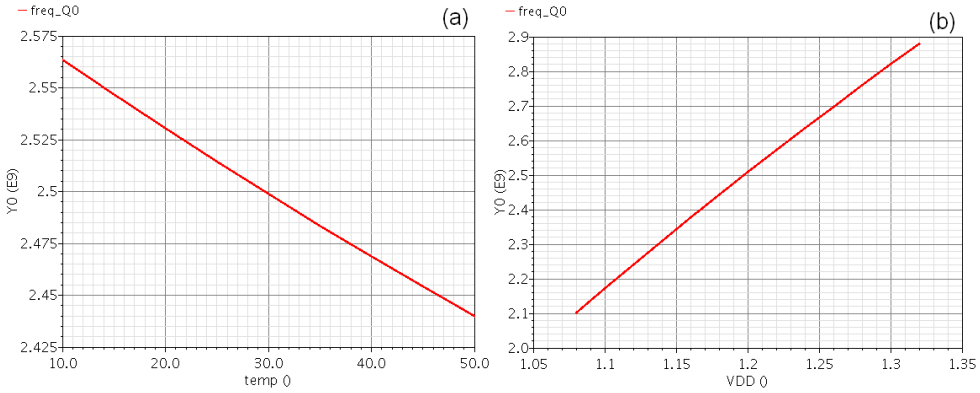


Figure 3.13 – Variation of the RO frequency over temperature (a) and voltage in a range 10% -110% V_{DD} (b) in half-loaded configuration and typical process condition (post-layout simulations).

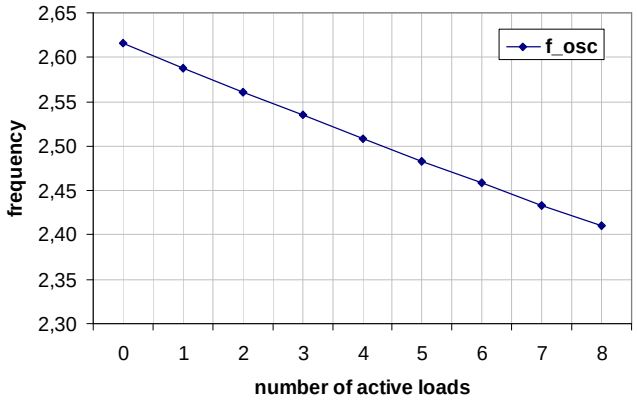


Figure 3.14 – Frequency tuning of the RO delay cells (post-layout simulations).

The RO and the delay line of the ADDLL have been designed with similar delay cell configurations so that externally incrementing/decrementing the RO load of 1 bit translates into a DL load variation alike. In particular, an m-stage ADDLL realizes a 2π phase shift at the end of the chain thanks to the closed control loop behaviour, so that the frequency within the block is given by:

$$f_{ADDLL} = \frac{1}{m\,t_{dll}} \qquad (36)$$

where t_{dll} is the delay cell.
With a 5-stage RO and a 4-stage ADDLL having equal cell delay t_d, equations (35)-(36) lead to:

$$f_{RO} = \frac{1}{\frac{(5-1)}{2}\left(t_d^{11} + t_d^{00}\right) + t_{inv}^{10} + t_{inv}^{01}} \approx \frac{1}{4t_d + \left(t_{inv}^{10} + t_{inv}^{01}\right)} \neq f_{ADDLL} = \frac{1}{4t_d} \quad (37)$$

The extra delay in the RO arising form the last inverter makes the two frequencies not equal if the cells in both the RO and the ADDLL are the same. Thus, the elements of the delay line are provided with an additional load so as to match the RO output clock, as illustrated in figure 3.15. This load is split into 5 varactors per cell with one of them always being on (green in figure 3.15); the others (red) are used as safety margin for the upper and lower bounds of the locking condition in the slow and fast process and are driven along with the other 8 capacitors by the control loop of the ADDLL.

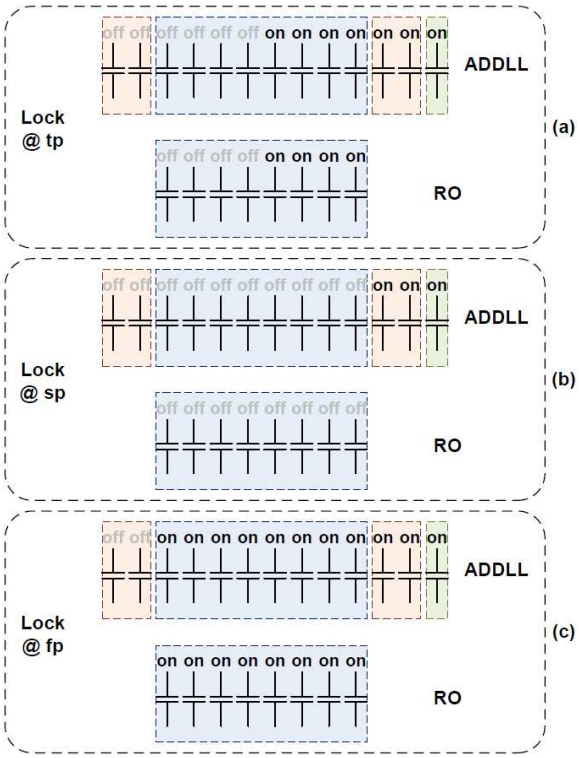


Figure 3.15 – ADDLL and RO locking for typical (a), slow (b) and fast process(c).

The closed control loop of the ADDLL is made up of a phase detector (PD) and an up/down counter (UD-C) which is controlled by a control unit (CTR-U); the latter enables the DL tuning every 32 T_{CK} so as to reduce the frequency of the tuning action, as reported in figure 3.16. The picture also shows that the ADDLL input and output signals are picked up for phase detection one inverter after CK and φ_3 respectively but always preserving the overall $4T_{CK}$ delay along the chain. This prevents φ_3 from being loaded with the D input of the PD.
The phase detector is based on a classical D-flip-flop (D-FF) that samples the ADDLL output at the rise edge of its input (i.e., the 2.5 GHz clock), thus providing

the absolute value of the delay difference, also known as phase error. When this difference approaches zero, the PD output starts shifting between two states. This condition is called the “bangbang” behaviour of the closed control loop which results in a zero average phase error although the instantaneous value oscillates around the ideal value. Reducing the time range of the PD sampling uncertainty around the sampling instant improves the ADDLL performance. Another issue in PDs is metastability which is responsible of a delay in the decision taken at the output of the D-FF. Metastability limits the corrections that can be performed in T_{CK} and can lead to lack of loop control when the decision delay is too long. This may result in a dead band around the zero phase error when the probability of metastability is large.

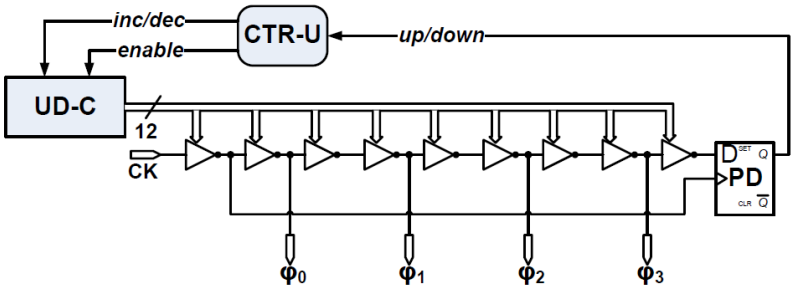


Figure 3.16 – Block diagram of the ADDLL.

Both “bangbang” behaviour and metastability issues can be addressed by optimizing the input latch of the D-FF which must be made fast in achieving its finale state after input signals have changed. A balanced fan-in/fan-out design for the D-FF has been proposed in [93] which leads to an improved PD performance when layout matching is also accounted for. The phase error of the PD implemented for the TDC is shown in figure 3.17.

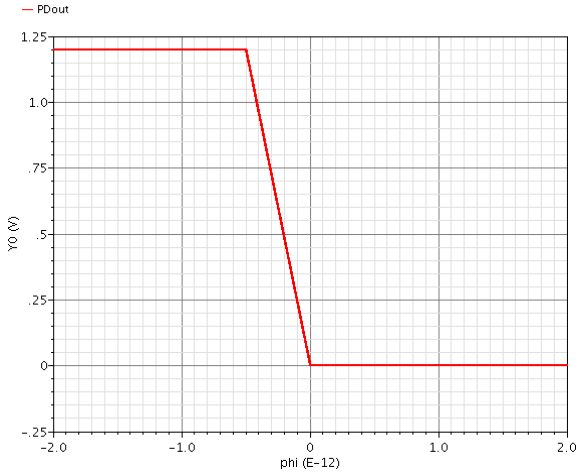


Figure 3.17 – PD phase error vs. input delay (post-layout simulation in typical conditions).

The up/down signal produced by the D-FF is sent to the CTR-U which is in charge of enabling the UD-C to increase/decrease its count of 1 bit every $32T_{CK}$ so as to keep the input and output of the DL in phase over PVT fluctuations. The CTR-U is implemented as a 5 bit systolic counter with auto-reset capability each time a high-to-low/low-to-high transition is detected at the PD output pin. If after reset the up/down signal stays constant over 2^5 clock periods, the output carry of the last CTR-U cell enables the UD-C to update its configuration according to the logic value of the up/down signal. The UD-C is implemented with a systolic approach as well by pipelining the incrementing/decrementing algorithms along systolic arrays (see figure 3.18).

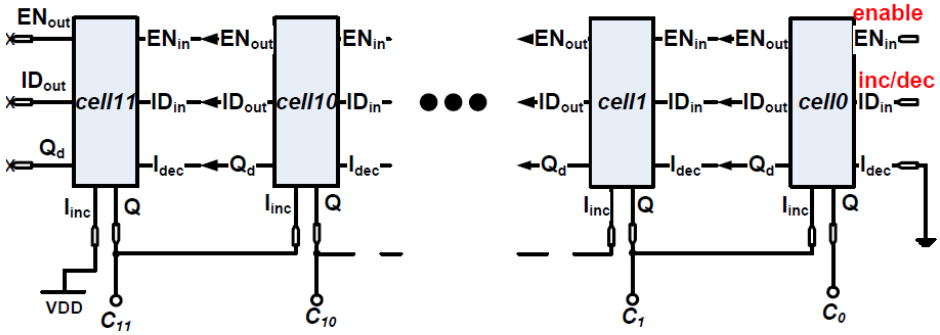


Figure 3.18 – Block diagram of the up/down counter.

When the enable is at a high logic level, each i-th cell updates its output Q according to the following conditions:

- $if\ \ inc/dec=1 \quad \Rightarrow \quad Q^i = I^i_{inc} = Q^{i+1}$
- $if\ \ inc/dec=0 \quad \Rightarrow \quad Q^i = I^i_{dec} = Q^{i-1}_d$

where Q^i, Q^{i+1} and Q^{i-1} are the output bits of the i-th, (i+1)-th and (i-1)-th cells, respectively, and Q_d is bit Q delayed of one clock period. Communication between cells is performed in a pipeline fashion at the clock speed. On the other hand, if the UD-C is disabled, the cell retains its output, thus preserving the DL configuration until the next configuration change command. Up-counting from all 0 condition starts at cell11, which has the I_{inc} pin connected to V_{DD}; similarly, down-counting is obtained by connecting the I_{dec} pin of cell0 to ground.
Figure 3.19 shows the ADDLL behaviour from the starting to the locking condition. In figure 3.19a the input-output DL delay is shown: the odd up/down behaviour at the beginning of the simulation arises from undefined initial condition of the UD-C cells since no reset is performed at the start time and the simulator arbitrarily assigns an initial value. The locking is achieved after 95 ns and then a peak-to-peak jitter of 4.37 ps can be observed with a non-zero mean value of 1.59 ps. This is probably due to a non perfect matching at the locking condition between the RO and the DL. The enable and inc/dec waveforms generated by the CTR-U are shown in figure 3.19b. Before locking is achieved, an enable pulse is produced every 12.8 ns, as expected; after locking, a larger period of time is required for the UD-C to be updated since reset occurs within the CTR-U which takes 4.8 ns (i.e.,

$12T_{CK}$) to be transmitted from cell0 down to cell11 at the clock frequency. Thus, after the equilibrium has been reached, the ADDLL oscillates between two states with a frequency of about 57 MHz. The UD-C is also able to warning the user when the locking is not achieved; two external signals denoted as *all0* and *all1* inform when the ADDLL is either too slow or too fast compared to the input clock, respectively. Thus, the user can increase/decrease the RO frequency until locking takes place.

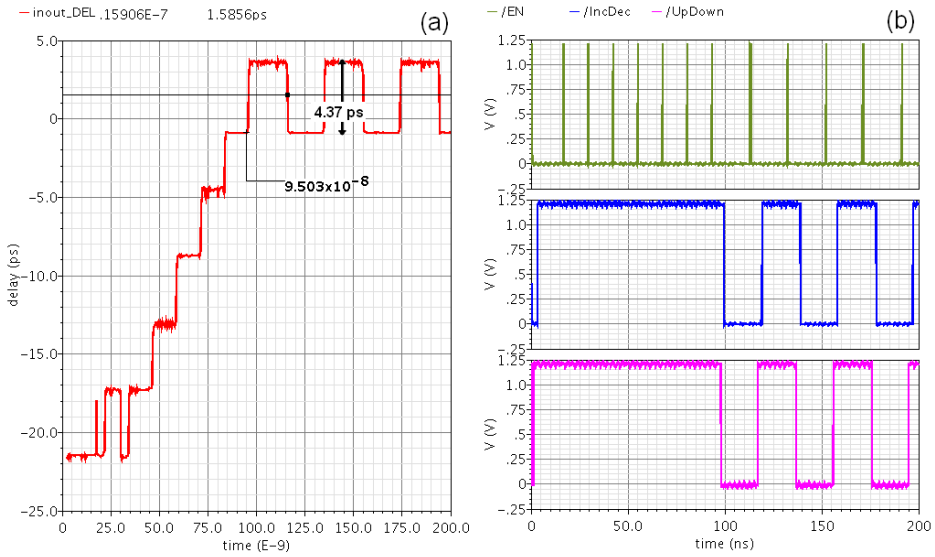


Figure 3.19 – ADDLL behaviour from the starting to the locking condition. Input-output delay (a) and control loop waveforms (b).

3.3.1.2. Systolic counter

Similarly to the design procedure implemented for the UD-C, the common 10 bit systolic counter (CSC) is based on the repetition of cells which perform the function of an half-adder in a pipeline arrangement, as depicted in figure 3.20.

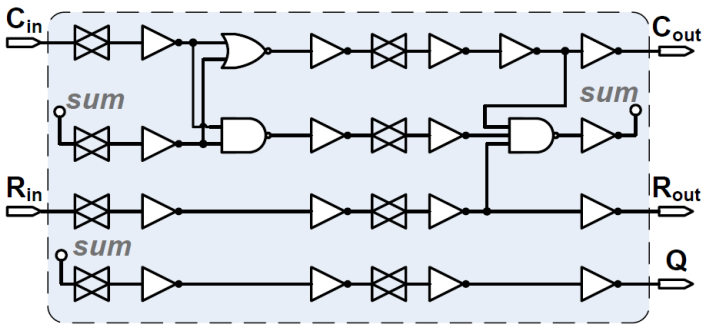


Figure 3.20 – Systolic implementation of the half-adder function.

The output carry is given by the logic *and* of the inputs which are the output carry and sum of the previous stage whereas the sum is evaluated as the *xor* of the

inputs. Dynamic flip-flops are used inside the cell given the high working frequency which makes it possible to exploit the capacitance of pass-gates for storage purposes. This design solution is used everywhere within the systolic blocks of the TDC with the following rules to be accomplished:

- Inputs directly feed the master pass-gate
- Maximum fan-in per gate is 3
- Maximum fan-out per gate is 3 (with the exception of pass-gates)
- Pass-gates always loaded by one inverter only

These rules have been derived from simulations of the gates in order to find optimal transistor size and post-layout cell behaviour at 2.5 GHz and ensure a correct implementation of the systolic functions within the pipeline blocks.

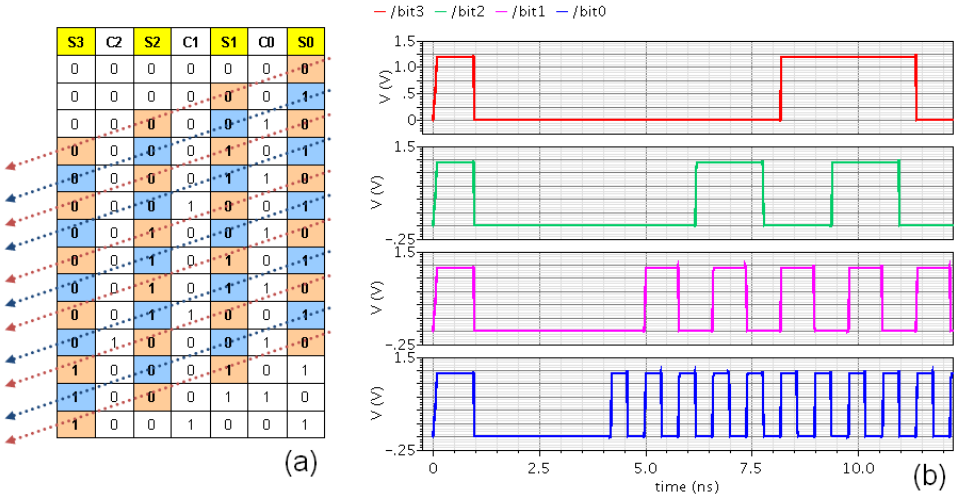


Figure 3.21 – Skewed output (orange and blue) of a 4 bit systolic counter. S_i and C_i are sum and carry at the output of the i-th half-adder (a). Simulated output bits (b).

The CSC is configured at an all 0 initial state through the reset which is externally provided to the chip and then synchronized before reaching the two systolic counters after passing through the semi-custom unit.
It is worth noting that the output bits are skewed by T_{CK} one after another because of the systolic architecture of the counter (see figure 3.21). However, this is not an issue since pipelined hit registers are used for data sampling so that each bit is stored with one clock delay, thus compensating for the counter skew.

3.3.1.3. Data sampling

When an event occurs, a store command is generated and sent to the hit registers so as to record both the systolic counter bits and the ADDLL status. In order to perform the TOF measurement with a timestamp of 100 ps, the TDC must check where the event rise edge is located among the four ADDLL output phases $(\frac{T_{CK}}{4}, \frac{T_{CK}}{2}, \frac{3}{4}T_{CK}, T_{CK})$. This is accomplished by sampling the input pulse with the

ADDLL signals (φ_0, φ_1, φ_2, φ_3) in order to freeze the event edge position with respect to each phase, as shown in figure 3.22a; to this end, the same D-FF block designed for the phase detector has been used. Thereafter, low-to-high and high-to-low transitions are identified at the system frequency by dynamic flip-flops which compare the Q3 and !Q3 outputs between consecutive clock periods to generate a store pulse of width T_{CK} in correspondence of the rise and fall edges of the event, respectively (see figure 3.22b).

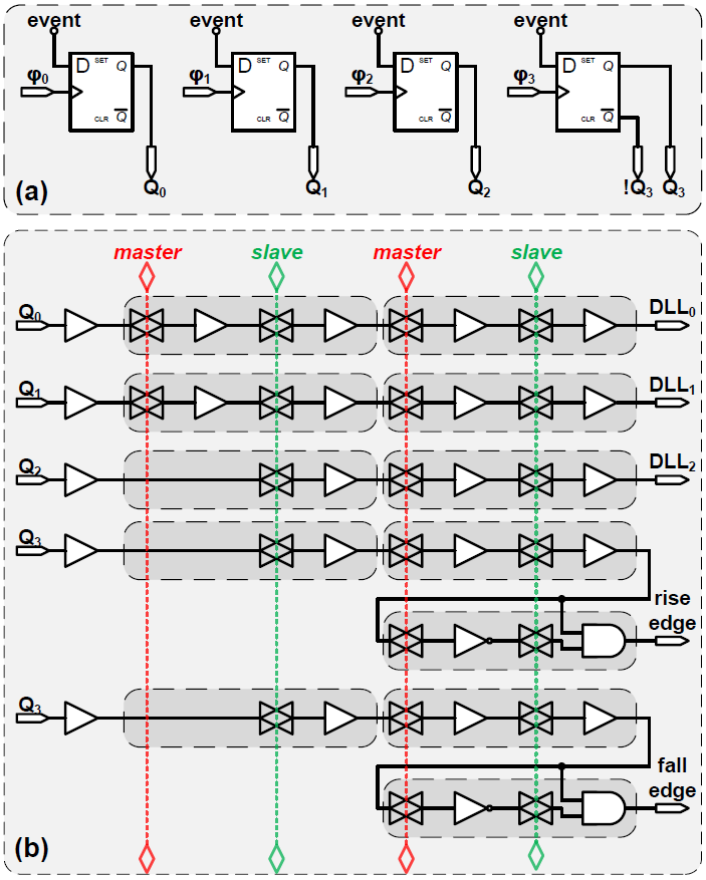


Figure 3.22 – Event sampling with the four ADDLL phases (a) and rise/fall edge detection at systolic level (b).

Signals Q_0, Q_1 and Q_2 are sampled as well and the resulting outputs (DLL_0, DLL_1 and DLL_2 in figure 3.22b) are forwarded to the hit registers which memorize data in correspondence of the store pulse. All sampler outputs feed another flip-flop stage (not shown in figure 3.22) before being sent to the other blocks of the TDC. An example of the output waveforms generated by the sampler for a given input pulse is reported in figure 3.23. The green signal of figure 3.23a is the input from the CM ASIC and its rise edge is located between $T_{CK}/4$ and $T_{CK}/2$ with respect to the clock (pink). This translates into Q_0 being delayed compared to the other D-FF outputs since the event occurs after φ_0 has already passed by. As a consequence,

when hit registers memorize the ADDLL status on the store command, the DLL_0 signal is zero whereas DLL_1 and DLL_2 are already at a high logic level, thus providing a thermometer code of 110. This can be observed in figure 3.23b, where the store for the rise edge ($store_{TOF}$ in orange) occurs before DLL_0 switches to V_{DD}. The blue pulse ($store_{TOT}$) is the store at the input fall edge; the ADDLL status is not of interest in this case, since only the systolic counter has to provide the TOT measurement.

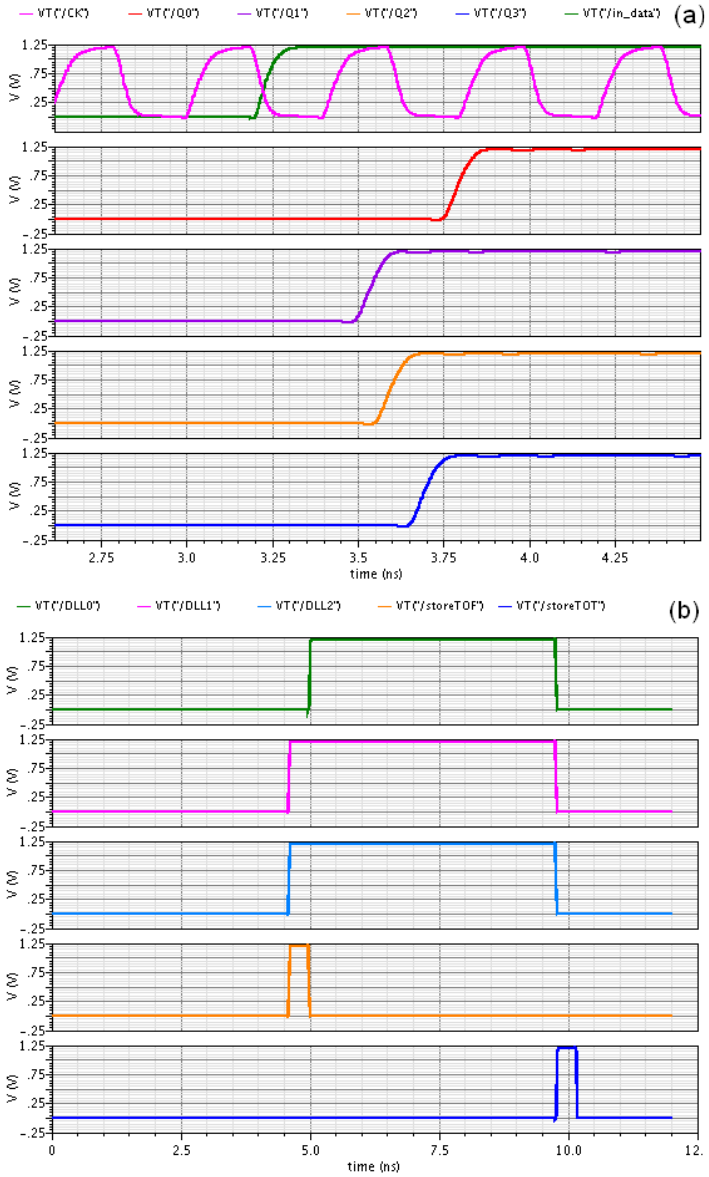
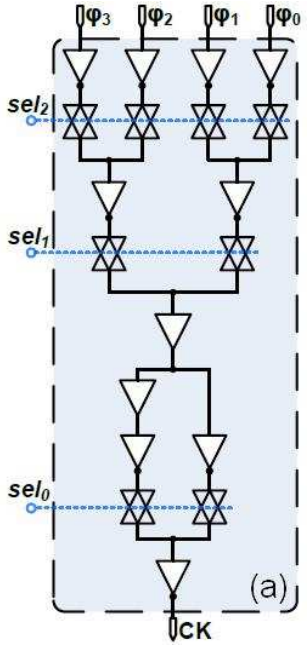


Figure 3.23 – Input signal sampled with the 4 phases of the ADDLL (a); store signals and DL status at the input arrival time (b) (post-layout simulations).

It is worth noting that, since the D-FF has a maximum set-up (t_{su}) and clock-to-output time (t_{co}) of about 220 ps and 240 ps respectively, the master/slave clocks (ck_m, ck_s) that trigger the dynamic flip-flops of figure 3.22b must be chosen with high accuracy so as to prevent Q_i signals from being sampled at the transition time. Thus, ck_m and ck_s are generated by a non-overlapping clock generator (NOCG) which is driven by a multiplexer in order to choose the optimal clock among the delay line outputs. In addition, each ADDLL phase can be further shifted of about 50 ps so as to enable a fine tuning of the clock. The selection is performed by the user with 3 configuration bits in order to ensure a correct sampling over PVT fluctuations (see figure 3.24).



sel2	sel1	sel0	clock
0	0	0	φ0
0	0	1	φ0 + 50 ps
0	1	0	φ1
0	1	1	φ1 + 50 ps
1	0	0	φ2
1	0	1	φ2 + 50 ps
1	1	0	φ3
1	1	1	φ3 + 50 ps

(b)

Figure 3.24 – Multiplexer for clock selection (a) and configuration table (b).

The NOCG is implemented with a standard configuration as shown in figure 3.25a. The resulting master and slave clocks have non-overlapping widths (m_{on} and s_{on} in figure 3.25b) to ensure a correct sampling by the pass-gates within the dynamic flip-flops. The time intervals T_1, T_2, T_3 arise from the gate delays and determine the master/slave pulse width according to the following equations:

$$m_{on} = T_{on} - (T_2 + T_3) + T_1 \tag{38}$$

$$s_{on} = T_{off} - (T_1 + T_2) + T_3 \tag{39}$$

where T_{on} and T_{off} are the on- and off-widths of the input clock. It follows that the master/slave on-width can be set by conveniently sizing the gates. A post-layout simulation of master/slave clocks is shown in figure 3.25c; the pulse widths for ck_m and ck_s correspond to 132.9 ps and 113.5 ps, respectively. The non-overlapping time between the master 1-0 transition and the slave 0-1 equals 78.1 ps while between the slave 1-0 and the master 0-1 a range of 74.2 ps occurs.

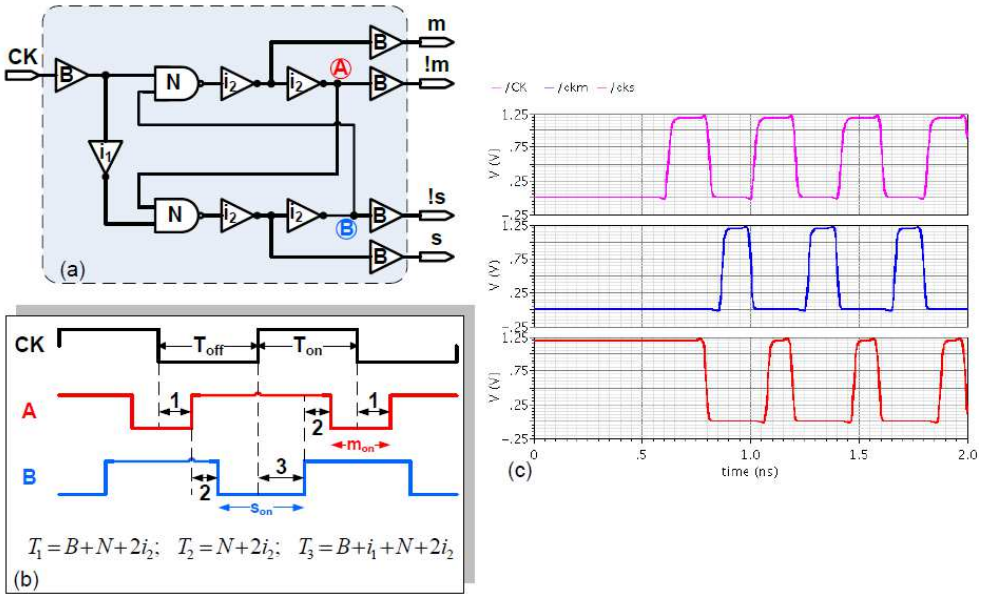


Figure 3.25 – Schematic block of the NOCG (a) and timing diagram of the clock master/slave generation (b).

3.3.1.3.1. Input validation

The SiPM noise background arriving at the input of the CM ASIC is converted into pulses with fixed width that can be selected within the TWA range (6 – 30) ns for calibration purposes. This makes it possible for the TDC to differentiate noise from valid inputs based on the evaluation of the pulse length since events have larger duration of TWA plus TWB (which can be extended up to 120 ns) plus the TOT (in the order of a few nanoseconds). Such a computation can be easily performed by a systolic counter that is configured according to the calibration settings of the CM ASIC. A time threshold higher than the selected TWA can be used to discard noise. When an input occurs, the counting is enabled along the cells until two possible conditions are satisfied according to the type of signal received. If it is noise, the count achieved at the end of the pulse does not match the desired time threshold; the counter is reset and no validation is provided to the hit registers of the TDC. On the other hand, a valid event enables the counting for a sufficiently large period of time until the threshold is reached. A flag is sent to the circuit blocks in order to trigger the store process while the validation counter is frozen by a block (BLK) command until a reset is generated on the trailing edge of the input. The TDC unit that executes these actions is called time window stage (TWS) which includes a 7 bit configurable systolic counter, a count enable (CNT-EN) stage for reset/blockage and an interface for communication with the other circuit units. The counter implementation is similar to that of figure 3.20; in addition, each cell performs a comparison between the programmed output bit and the calculated sum and forwards logic 1 to the next cell if the two bits are equal and the previous cell has provided a 1 as well (see figure 3.26). If this is true at each stage of the counter, pin n of the last cell produces the validation signal. Furthermore, the BLK command is pipelined along the cells from down to top and an additional flip-flop

forwards the bits of the CSC (T_{in} in figure 3.26) to the next stage of the TDC channel.

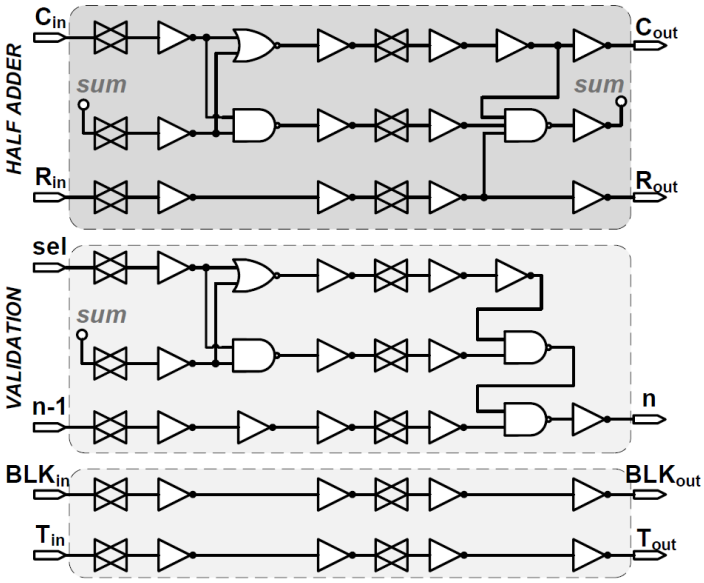


Figure 3.26 – Configuration of the TWS cell. The validation section performs an xnor between the configured bit (sel) and the calculated sum; if the two bits are equal and the comparison has been true at the previous cell as well (signal n-1), a logic 1 is generated at pin n.

The CNT-EN communicates with the sampler block of the channel in order to receive a sampled copy of the input signal for the count enable function and the $store_{TOT}$ signal (cf. figure 3.23) which is used as a reset by the TWS. If a BLK pulse arrives at the CNT-EN, the count is stopped although the input pulse is still high and the TWS counter is frozen until reset occurs. Only a new event can trigger the time window stage to start a new count. The BLK signal is provided by the interface stage each time the validation flag goes to logic 1, since it means that count threshold has been reached. This prevents the TWS from experiencing overflow due to long input pulses. In addition, another BLK command is generated each time the semi-custom unit acknowledges the TWS that data buffering is about to start as well. Although this might be redundant, it is necessary at the starting time when initialization is required by the blocks. The TWS acknowledgement cannot be used alone for the BLK generation since the SCU runs at a lower speed than the FCU so that a large time interval (higher than 9 ns) exists between the valid flag generation and the acknowledgement. This can be a problem when a short time window (i.e., less than 9 ns) is selected, thus producing multiple validation at the output of the TWS. The BLK signal travels from the interface across the 7 bit counter up to the CNT-EN which stops the counting function of the TWS until a new input pulse occurs. The interface stage also translates the valid flag pulse into a signal that stays at a high logic value until it is read (i.e., acknowledged) by the SCU since the two units work at different frequencies. A simulation of the signals

generated by the time window is reported in figure 3.27. The red waveform is the TWS input and is made up of a noise pulse of 6 ns followed by a valid pulse of 30 ns (for simulation purposes, it is shorter than real pulses generated by the CM ASIC). The threshold is set to 12.8 ns and the green reset is sent on the trailing edge of the pulses. The validation signal (blue) is used by the interface to produce the EVENT flag (orange) which is sensed by the SCU. This signal returns to a low logic value after an acknowledgment (ACK, purple) is sent from the semi-custom unit which has a width equal to its clock period. The pink pulses are the BLK commands arising from the validation and ACK signals. Finally, at t = 0 the initialization of the TWS is triggered by an ACK pulse.

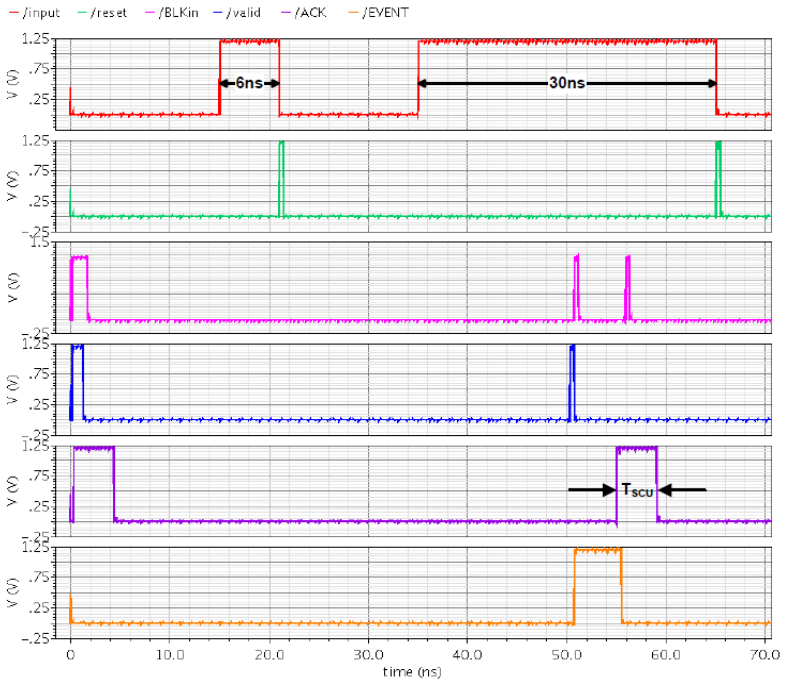


Figure 3.27 – Input and output signals of the time window stage. Both noise and valid input (red) is simulated.

3.3.1.3.2. Hit registers

Any event (both valid and noise) occurring at the input of a channel triggers the sampler block, which in turn produces the $store_{TOF}$ and $store_{TOT}$ pulses. The former is sent to the TOF-HR and to the PLS-C whereas the latter supplies the TOT-HR and resets the TWS. Thus, the TOF-HR captures the CSC and ADDLL configurations in correspondence of the input rise edge to measure the TOF information with a timestamp of 100 ps; on the other hand, the TOT-HR records the counter bits only on the trailing edge of the event pulse so as to provide the energy (TOT) data with a bin size of 400 ps.

The memory cells of the TOF-HR and TOT-HR are based on the same algorithm. When a store command arrives from the sampler unit, each cell records its corresponding bit from the CSC (and ADDLL for the TOF-HR) and holds it down

until two possible events take place. If the input is recognised as valid, the SCU sends a sequence of shift pulses to the hit registers so that all stored bits are serially sent out from cell to cell for buffering and encoding purposes. On the contrary, noise pulses are ignored by the TDC so that no shifting is performed along the TOF-HR and TOT-HR. Then, each cell retains the stored value until a new input occurs which causes the previous bit to be overwritten with the new one. This process repeats until a valid event arrives at the channel. In figure 3.28b the pink waveform is the CSC output bit (T_{in2}) and the red signal is the output of the previous cell ($D_2 = Q_1$). When a store pulse occurs (blue), the cell output Q_2 (yellow) is updated according to the value of T_{in2}; in correspondence of the shift command (purple), Q_2 is switched to the value of D_2. Repeating the shift n-times along a chain of n memory cells allows for a complete serial output of the stored bits from the hit registers.

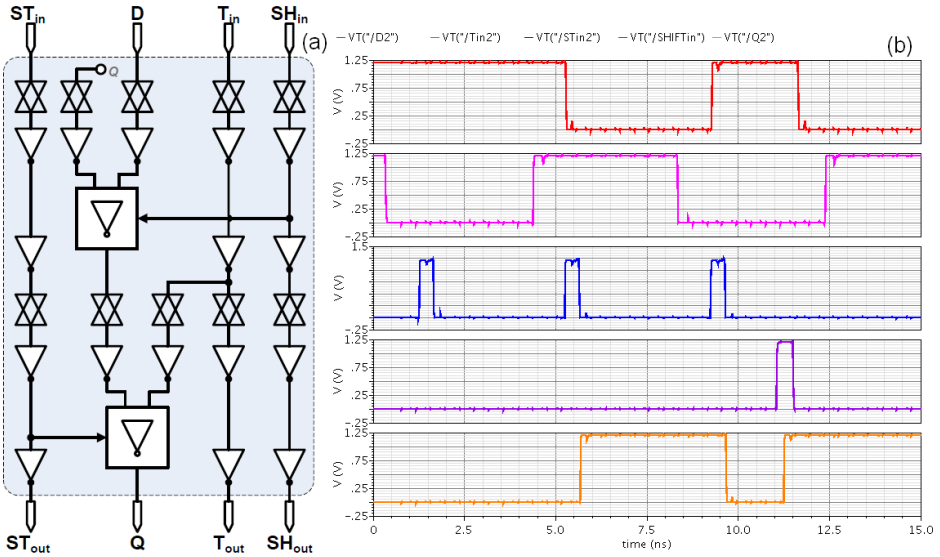


Figure 3.28 – Schematic implementation of the store/shift process within memory cells (a). Waveforms at the input/output of a single cell in typical conditions (b).

The high SiPM noise rate of about 18 MHz per channel requires an accurate control of the store process within the registers in order to avoid data corruption. When a valid input is closely followed by noise (i.e., a few nanoseconds), the TOF-HR may overwrite the recorded bits before the shifting procedure has been completed. Indeed, the SCU takes $13T_{SC}$ to serially acquire the 10 bits of the CSC and the 3 DLL_i outputs, where T_{SC} is the clock period of the semi-custom unit equal to 4 ns in typical conditions. This stands for the TOT-HR as well where the fall edge of a valid pulse is even closer to the trailing edge of a close placed noise input. For this reason, both the TOF-HR and TOT-HR are provided with control blocks which prevent data corruption without impairing the system acquisition capability. The store process of the TOT-HR is controlled by the DAQ stop unit which receives the $store_{TOT}$ command from the sampler. On the rise edge of an input, the data acquisition is disabled by a blockage pulse (BLK_{TOT}) sent from the TOF-HR so that the DAQ stop masks the store commands and no data are recorded. On the other

hand, when a valid input is detected the TWS sends an acknowledge signal (ACK_{TOT}) to the TOT interface which forwards it through the hit registers up to the DAQ stop (see figure 3.29a). Thereafter, only one $store_{TOT}$ is passed to the memory cells so that the trailing edge of the event can be stored and no further recording is allowed unless a new validation is provided. This technique is very robust since events have a width larger than 56 ns (i.e., the sum of minimum TWA and TWB) and the time threshold of TWS should be set at 30 ns at most (i.e., the maximum TWA). The validation takes $15T_{CK}$ to travel from the TWS interface up to the DAQ stop[1] which translates into a time interval of 6 ns. Then, the TOT-HR hangs on until the arrival of $store_{TOT}$ with no loss of information.
In figure 3.29b, the store command (purple) is provided to the hit registers only when the DAQ control signal (blue) is at a low logic value. This happens when validation (green) is awarded from the TWS. When a new input occurs, BLK_{TOT} (red) arrives from the TOF-HR which sets the DAQ back to 1 so that $store_{TOT}$ (pink) is not forwarded unless validation is provided once again.

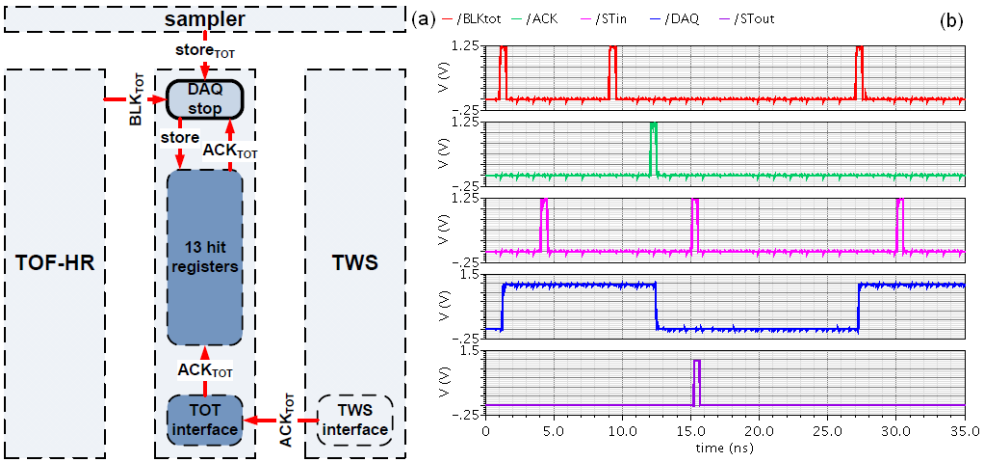


Figure 3.29 – Signals feeding the DAQ stop stage (a) and waveforms resulting from simulations in typical conditions (b).

The control logic within the TOF-HR slightly differs from the DAQ stop algorithm. The $store_{TOF}$ must always pass to the hit registers since it is not possible to establish the type of input in correspondence of its rise edge. However, after validation the control unit (referred to as store enable, ST-EN) is blocked and it masks the store command until all bits are shifted out of the FCU in order to prevent overwriting in the event of a close new input pulse. After the SCU has downloaded all TOF data, it sends a release signal (RLS_{TOF}) to the TOF interface which makes the ST-EN transparent again with respect to $store_{TOF}$, as can be observed in figure 3.30. The block command (BLK_{TOF}, pink in figure 3.30b) is the validation signal sent from the TWS and forwarded by the TOT interface. The store

[1] Although only 10 cells are required to store the output bits of the CSC, 3 dummy cells have been added in order to match the TOF-HR for regular structure and layout, as shown in figure 3.10.

inputs (blue) arriving from the sampler are not propagated by the ST-EN until it is released (RLS, green) by the SCU.

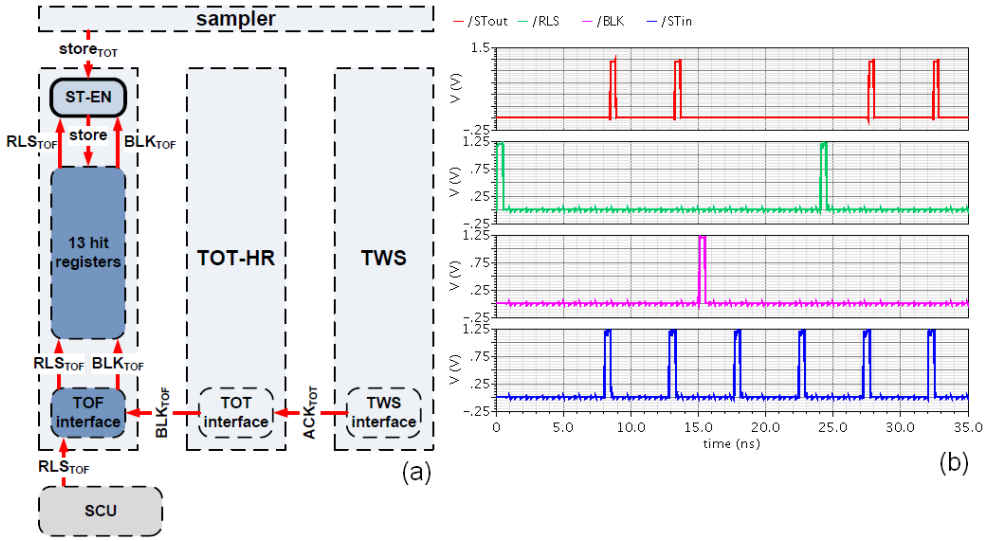


Figure 3.30 – Signals feeding the store enable unit (a) and waveforms resulting from simulations in typical conditions (b).

The TOF-HR and TOT-HR communicate with the SCU through the interface stages which synchronize the shift pulses and translate them into signals with 400 ps width. Moreover, they inform the SCU that TOF/TOT storage has been accomplished by switching a dedicated bit (HIT_{TOF}, HIT_{TOT}) to V_{DD} until acknowledgement by the SCU occurs. Then, the bit stream travels through the TOF/TOT interface down to the semicustom unit during the shifting phase.

3.3.1.4. Other features

The $store_{TOF}$ signal generated by the sampler unit is sent to the TOF-HR and to another systolic counter featuring 12 bits. The latter has the same structure of the CSC and its task is to provide the SCU with the total number of events (both valid data and noise) occurred from the beginning of the measurement for statistical purposes. Each time an input is sensed by the TDC, the pulse counter (PLS-C) increments its count of 1 bit. After 2^{12} events, the carry of the last half adder switches to logic 1 and is sent to the SCU where a 4 bit binary counter extends the dynamic range of the pulse computation. Thereafter, the PLS-C experiences overflow and a new count is taken. Furthermore, the PLS-C cells forward the output bits of the CSC to the next channel of the TDC (cf. figure 3.10).

As already mentioned, the SCU is fed with a clock (T_{SC}) whose frequency is 10 times lower than the one generated by the ring oscillator. Since the division operation required for the clock generation is not a power of 2, a classical approach cannot be exploited. The desired frequency is obtained by implementing a division algorithm with the aid of systolic structures. The block diagram of the systolic frequency divider (SFD) is depicted in figure 3.31a. It is based on a counting mechanism performed by 4 systolic cells starting from the 0011 configuration; each time the 1000 status is achieved, cells A, B are preset and cells C, D are reset by

the carry of cell D. The latter propagates back through the SDF and restores the initial condition after $5T_{CK}$; thus, output Q_D shows a periodic up/down behaviour with period of $10T_{CK}$ and 50% duty cycle so that it provides the 250 MHz clock to the SCU. The SDF can be initialised either with or without an external start signal in which case it takes some time to reach the 0011 state. This topology is easily designed and can be exploited to generate any clock division by simply modifying the initial configuration and the number of cells used. The post-layout simulation of figure 3.31b shows that a period of 3.99 ns is achieved in typical conditions, where an input clock of 2.5046 GHz is applied to the SDF.

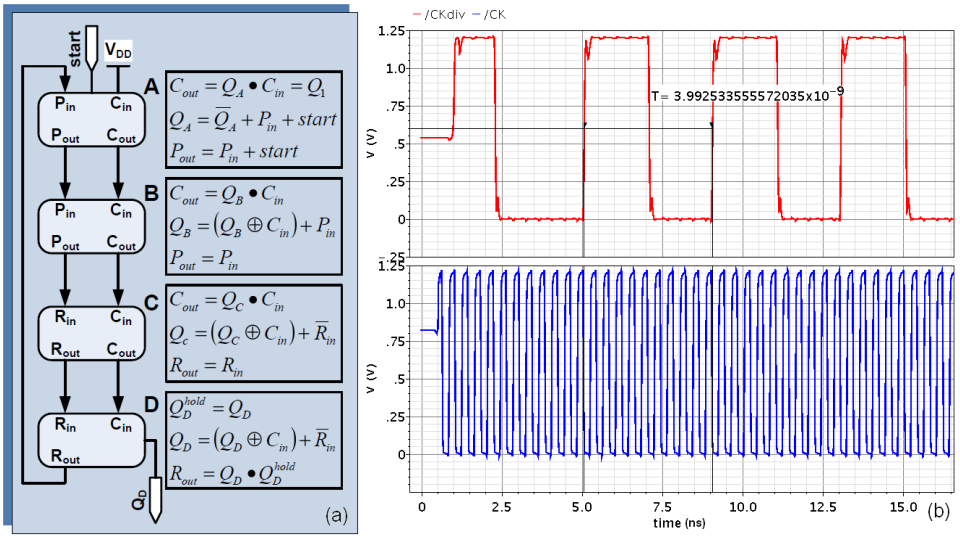


Figure 3.31 – Systolic implementation of the frequency divider by 10 (a) and post-layout simulation of the output clock (b).

All the configuration bits dedicated to the FCU blocks described so far are serially provided to the chip through a scan chain where bits travel in opposite direction with respect to the clock of the chain in order to ensure a correct allocation of data even in the presence of undesired delays due to parasitic effects. According to the scan chain arrangement across the 8 channels of the chip, the correct sequence to configure the TDC is:
TW_{111} – TW_{110} – TW_{101} – TW_{100} – $start_{SFD}$ – MUX_{CK} – RO – Z_{DLL} - TW_{011} – TW_{010} – TW_{001} – TW_{000}
The acronyms have the following meaning:

- TW_i = (c_6 c_5 c_4 c_3 c_2 c_1 c_0) are the seven configuration bits of the TWS to be set according to the desired time threshold with the MSB to be sent first.
- $start_{SFD}$ is the initialisation bit of the SFD to be set to one and then back to zero; since the SFD can start working from an unknown initial condition as well, this bit is optional and can be left to zero.
- MUX_{CK} = (sel_0 sel_1 sel_2) are the three bits to be used for clock selection among the 4 ADDLL output phases for correct data sampling within the sampler block;

in typical working conditions (typical process, V_{DD} = 1.2 V, T = 27℃) it should be set to: (sel_0 sel_1 sel_2) = (1 1 0). LSB must be sent first.

- RO = (b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0) are the eight configurable capacitors of the ring oscillator for clock tuning; in typical conditions, a clock of 2.5 GHz is obtained with: (b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0) = (00001111). MSB must be sent first.
- Z_{DLL} is the extra capacitor of the ADDLL for frequency matching with the RO; it is usually set to 1 but can be switched down to 0 for locking condition checks.

The ring oscillator also features an enable pin which can be directly controlled through a dedicated input PAD.
Since the chip is provided with both input and output pads for the clock and data signals of the scan chain, the configuration settings can be checked out by double sending the bit stream which can be externally read out by the user.

3.3.2. Semi-custom unit

The task of the semi-custom unit is to serially download TOF and TOT data from the FCU by sending trains of shift pulses to the TOF-HR and TOT-HR each time the validation flag of TWS switches to 1. Furthermore, it features an 18 bit very coarse binary counter which is sampled on the rise edge of events in order to expand the TOF dynamic range to 1.048 ms, as required in PET exams. Another 4 bit binary counter is incremented of 1 count by the PLS-C of the FCU for extended DR of the pulse counting.

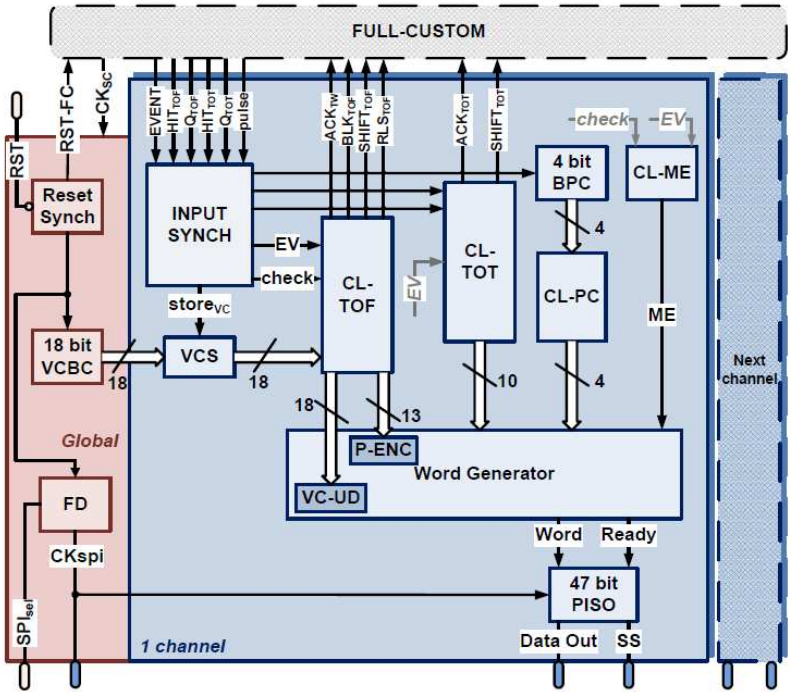


Figure 3.32 – Block diagram of the semi-custom unit. The red section is shared by the 7 channels of the SCU.

It is worth noting that shifting the 13 bits from the TOF-HR at 250 MHz requires 104 ns while the TOT bit stream is downloaded in 80 ns. It follows that these time ranges combined with the event pulse width entails a TDC dead time during which no further inputs can be processed. As a consequence, a new event occurring when the SCU is busy is lost. However, the system is provided with a control logic which flags the missed event with a dedicated bit.
The block diagram of the SCU is depicted in figure 3.32. It includes a common stage (red) which is global to the SCU blocks and 7 readout stages, since one FCU channel has to be directly controlled through dedicated PADs for debug purposes.
The common section of the SCU includes the following elements:

- A reset synchronizer (Reset Synch) which is triggered by external reset and sends an initialization pulse to the systolic counters of the FCU; this pulse also resets the SCU itself.
- The 18 bit very coarse binary counter (VCBC) for TOF data range extension.
- A frequency divider (FD) that provides the clock for serial output of data in SPI-like fashion; an external bit (SPI_{sel}) must be set either to 0 if a clock division by 4 is required (CK_{SPI} = 62.5 MHz) or to 1 for a frequency of 31.25 MHz.

Each FCU channel communicates with a corresponding SCU section which buffers TOF and TOT bits, performs data encoding and sends an output word with time, energy, pulse and missed event information through a serial link. The main blocks of an SCU channel can be summarized as follows:

- An input synchronizer which is fed by the signals produced by the FCU. It also generates the pulse command for VCBC sampling ($store_{VC}$) when the HIT_{TOF} signal switches to the high logic level.
- A very coarse sampler (VCS) that stores the VCBC output bits.
- Control logic for TOF (CL-TOF) that is in charge of sending 13 shift bits to the TOF-HR and buffering the ADDLL and CSC data along a 4 word FIFO. It also generates the acknowledge signal to the TWS when validation occurs at the EVENT input pin.
- Control logic for TOT (CL-TOT) which sends 10 shift bits to the TOT-HR and allocates the CSC output configuration within a 4 word FIFO.
- A 4 bit binary pulse counter (BPC) that is incremented of 1 bit by the output carry of the FCU pulse counter. Then, the output configuration of the BPB is sampled by the control logic pulse count (CL-PC) and buffered within a 4 word FIFO.
- A control logic missed event (CL-ME) that checks if a valid input is flagged by the TWS while the SCU is still processing a previous event. If this is the case, it sets a dedicated bit (ME) to logic 1; this bit is included in a further output word with all the other bits fixed at logic 0. This informs the user when data have been missed. Buffering is also performed along a 4 word FIFO.
- A word generator block where data encoding is performed. At this stage, a priority encoder (P-ENC) translates the thermometric ADDLL output into binary

form (2 bits); in addition, a very coarse updater (VC-UD) compares the LSB of the sampled VCBC output with the MSB of the CSC, removes the redundant LSB_{VCBC} and updates the VCBC output bits according to the algorithm reported in table 3.4. As soon as the update process is accomplished and all bits have been shifted out from the FCU, the word generator assembles all data within a 47 bit word containing the event information labelled with the channel ID to be sent out of the chip, as reported in figure 3.33.

- A 47 bit parallel input serial output (PISO) register with a 2 word FIFO which serially outputs the event word in an SPI-like fashion. A chip select (SS in figure 3.32) is generated each time a bit stream is about to leave the channel which acts as a master with respect to an external readout FPGA. The latter is also provided with the CK_{SPI} by the global stage of the SCU.

Because of the FIFOs used for data buffering, the output data are provided with a latency of 6 words with respect to the first event.

Table 3.4 – Algorithm implemented by the VC-UD.

LSB_{VCBC}	MSB_{CSC}	action	meaning
0	0	+1 bit	No change
0	1	+0 bit	Decrement
1	0	+2 bit	Increment
1	1	+1 bit	No change

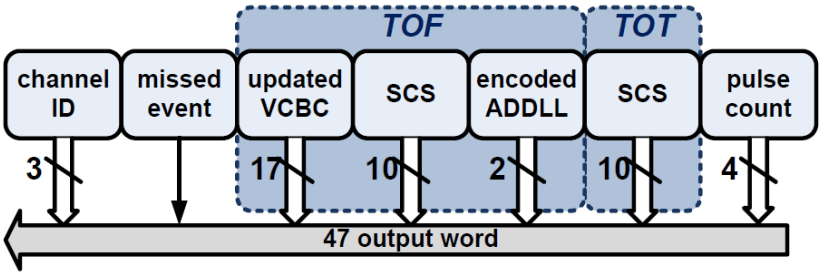


Figure 3.33 – Output word generation.

The semi-custom stage has been described in Verilog code and synthesised with the standard-cell library of UMC 65 nm. Figure 3.34 shows a simplified flow chart that illustrates the SCU algorithm when an event is processed. The steps are the ones described so far which are triggered by the validation flag (EVENT) generated by the TWS and finish with the generation of the event output word containing the time and energy information.
A Verilog simulation of the whole TDC (full-custom and semi-custom units) is reported in figure 3.35. The channel input (light blue) is made up of a valid event

followed by noise pulses. When the time threshold is achieved, the validation (yellow) is provided by the FCU. Then, 13 TOF and 10 TOT shifts (green and purple, respectively) are generated by the SCU control logics: after each shift pulse, the TOT (red) and TOF (light green) bits progress through the FIFOs. Finally, the data word (grey) is updated before being serially sent out of the chip.

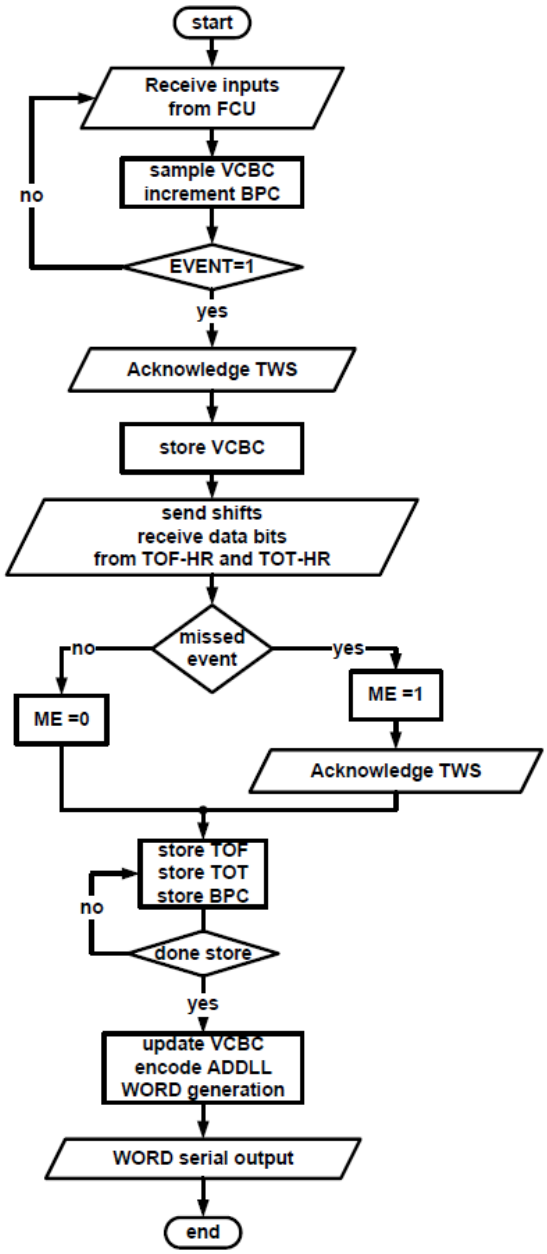


Figure 3.34 – Flow chart of the SCU algorithm.

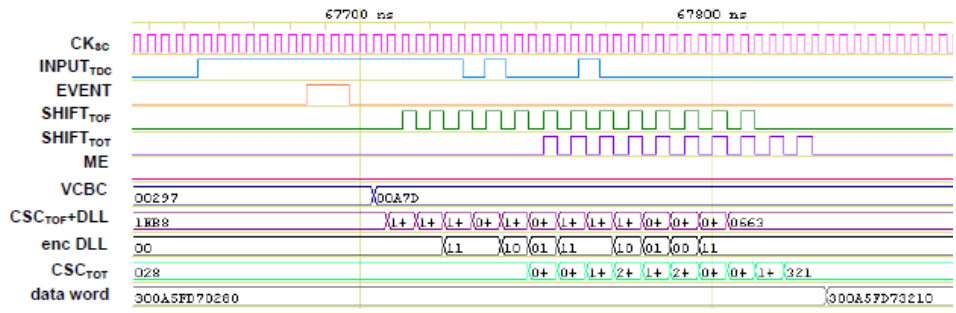


Figure 3.35 – Verilog simulation of one channel of the TDC.

The double hit resolution (DHR) of a TDC has been defined as the minimum time interval between two consecutive inputs that can be resolved by the circuit. Given the topology adopted, this feature depends on the time employed by the SCU to serially download data from the hit registers. Since the TOF-HR is enabled to store a new value only after a release pulse (RLS) is sent from the SCU, the DHR can be evaluated as the time range between the rise edge of an input and the arrival of the RLS signal at the ST-EN block. Despite the TOT data are shifted after the TOF bits, the semi-custom stage takes 132 ns to release the TOF-HR from the validation time. Thereafter, the RLS pulse travels through the registers and arrives to the ST-EN after 5.6 ns, thus allowing the FCU for a new data storage. Assuming input pulses of similar widths (TOT time has small influence on pulse duration compared to the sum of TWA and TWB), this time is sufficiently large to avoid TOT data corruption due to overwriting, since data shifting always ends before the fall edge of a new event in validation conditions.

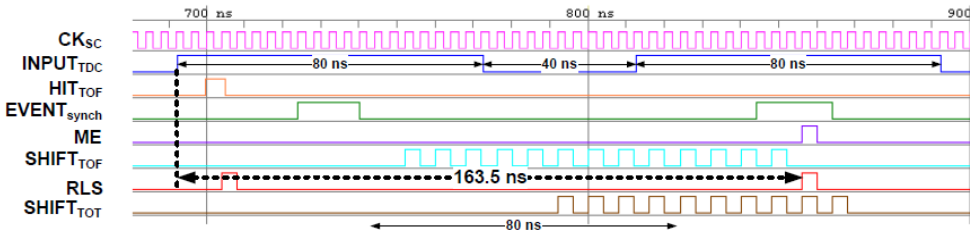


Figure 3.36 – DHR evaluation with a time threshold of 6 ns.

In figure 3.36, a Verilog simulation shows that the RLS pulse is sent from the SCU after 163.5 ns from the leading edge of the input pulse with a time threshold set to 6 ns. With larger TWS settings, the extra delay must be taken into account. Thus, the DHR can be evaluated by adding this value to the time required by the ST-EN to be released which equals 6 ns (one T_{CK} after RLS arrives at its input pin). This leads to a double hit resolution of around 170 ns.

3.3.3. Chip assembly

The layout of the full-custom stage is reported in figure 3.37. The FCU has a regular structure with the two groups of 4 channels symmetrically placed with respect to the ring oscillator and the ADDLL. The systolic counters are located

besides channel CH100 and CH011 (only one CSC is highlighted in figure 3.37) and their bits are propagated in opposite directions towards the left and right side of the layout, respectively. The frequency divider is close to the bottom of the FCU since it must feed the SCU which is placed immediately below the full-custom stage. Finally, the clock tree can be seen which spreads from the centre of the layout (where it originates) to the 8 channels. The FCU occupies an area of about 0.297 mm^2.

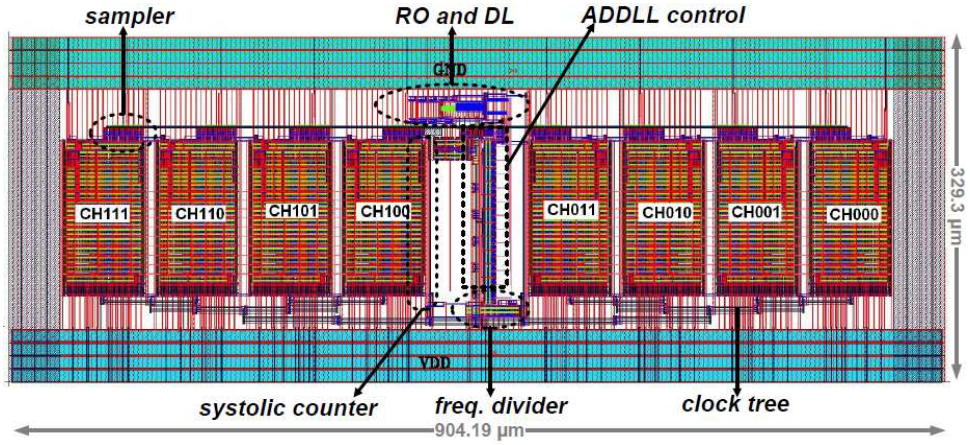


Figure 3.37 – Layout of the full-custom unit.

After synthesizing the semi-custom unit with Synopsys Design Compiler in order to get its structural Verilog file, the FCU and the SCU have been assembled together with Cadence SOC Encounter. A PAD ring has been arranged so as to satisfy the required minimum PAD pitch of 90 um. The total number of PADs used for the ring is 76 including the 4 corners; the IO supply voltage is 2.5 V. Unfortunately, only single ended PADs are available from the technology library. This is an issue for the final TOF PET module since LVDS communication is required for a correct working function in the presence of magnetic fields. However, this prototype can be used for debugging and test and represents the starting point for future improvements.
The chip size allowed by the foundry is 1.875 x 1.875 mm^2 for mini-asic tapeouts. Figure 3.38 shows the complete chip layout; the pinout configuration is also visible where two VDD – VSS couples are arranged on each chip side. On the left, the input/output signals of CH111 from the full-custom unit are directly driven from the external world for debug purposes. The core is surrounded by the power ring with an overall size of around 1173 x 912 μm^2; the semi-custom unit is placed within an area of approximately 450 x 244 μm^2. The empty spaces of the core are filled with dummies (not visible in figure 3.38).

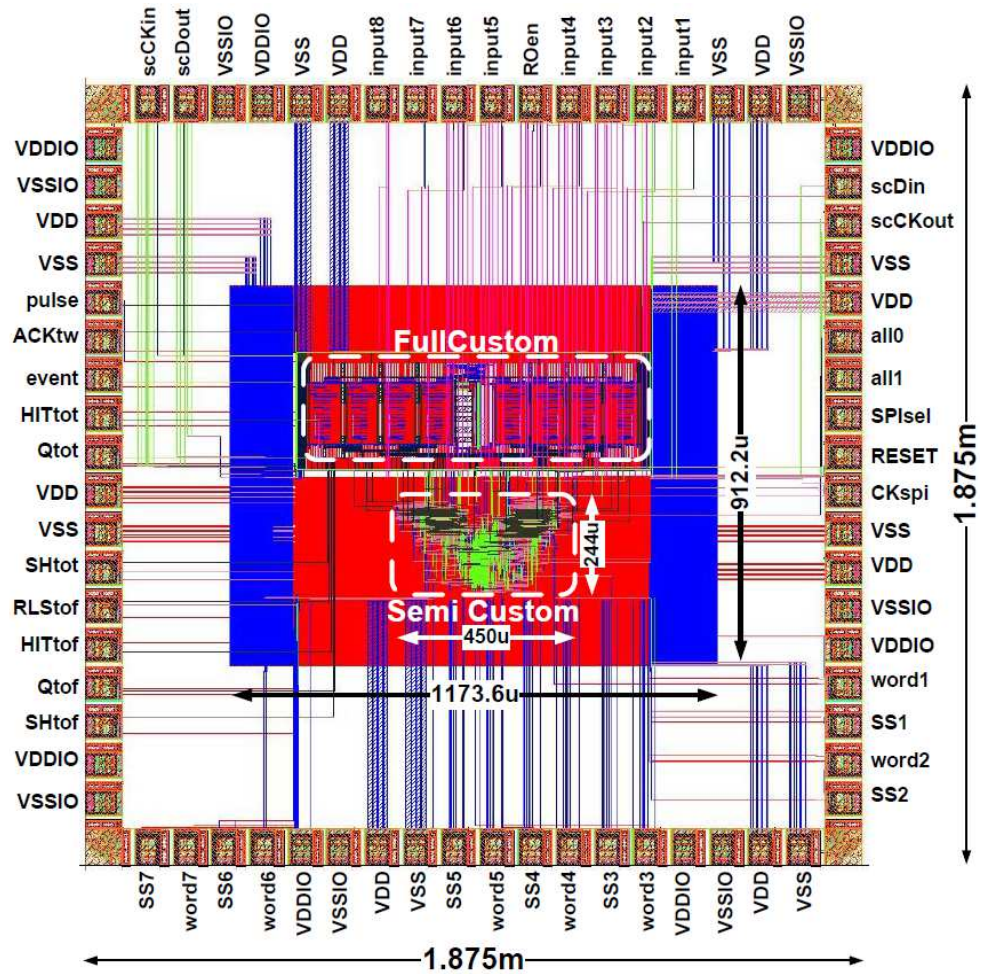


Figure 3.38 – Chip layout.

3.4. Conclusions and future work

The complete 8 channel TDC has been simulated in Verilog with input data generated according to a Poisson distribution and to the timing characteristics of the CM ASIC which have been derived from a Matlab model provided by the designer of the front-end. The FCU has been designed with the aid of Cadence platforms and post-simulations have validated the performance of the blocks in all critical corners. The mixed-signal pipelined configuration allows for working at a high frequency of 2.5 GHz which leads to a time stamp of 100 ps for the TOF measurement in typical conditions. The FCU components are based on the use of dynamic flip-flops where a maximum fan-in/fan-out of 3 gates is used in order to ensure a correct functionality at the system clock. The regular structure of the blocks makes it easy the implementation of a multichannel topology with a small occupation area; the current consumption per channel is 3.7 mA while the ADDLL and the RO consume around 6 mA in total. A real-time validation algorithm

combined with a buffering/encoding stage based on standard-cells ensures a correct data storage without impairing the system acquisition capability. With a time threshold set to 6 ns, a DHR of 170 ns is obtained which is acceptable given the low data rate of 9 kHz in preclinical applications. However, missed events are notified to the user for statistical correction. A linear performance is also expected because of the very short number of stages employed within the delay line. The "bangbang" behaviour of the ADDLL generates a peak-to-peak jitter of around 4 ps which has to be added to other noise sources such as the jitter present in the reference clock; these contributions alter the TDC resolution (i.e., single shot precision) whose theoretical value for a TOF LSB of 100 ps is 28.9 ps according to equation (34). The same calculation can be performed with regard to the TOT measurement which leads to an energy resolution of 115.5 ps. However, this value is not as critical as for TOF because of the system requirements discussed in paragraph 3.1.2. Finally, the TOT dynamic range equals 409.6 ns which is sufficiently large with respect to the constant time discharge process that takes place within the CM ASIC and is in the order of a few nanoseconds according to the average energy per event. The DR is further extended to 1.04 ms for the TOF evaluation where larger time intervals must be computed. The main features of the TDC are summarized in table 3.5.

Table 3.5 – TDC performances from post-simulation results.

System clock	2.5 GHz
Channels	8
TOF T_{LSB}	100 ps
TOT T_{LSB}	400 ps
TOF DR	1.048 ms
TOT DR	409.6 ns
DHR	170 ns
Output data	47 bits
Measurement rate	62.5 MHz 31.25 MHz

However, the lack of a robust clock reference can worsen the TDC performance in terms of both linearity and resolution. The design of a phased locked loop might significantly improve the timing performance of the chip by minimizing the noise contributions. In addition, it would lead to a uniform behaviour in different chips, thus removing the need for a calibration channel which must receive an external reference signal for off-line data correction as depicted in figure 3.39.

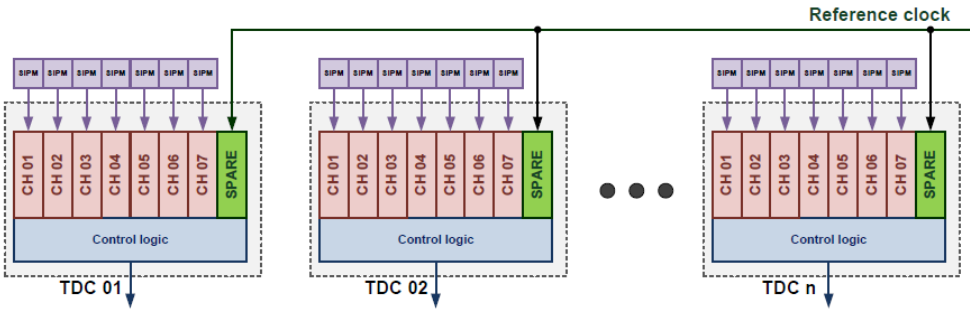


Figure 3.39 – Spare channel used in the TDC chip for off-line calibration.

Another issue regarding the final TOF PET module arises from the use of single-ended PADs which keeps the chip from working within a magnetic field. Then, the design of ad hoc LVDS PADs is essential to allow the chip for being coupled to the target detector module.
The 8 channel prototype has been submitted to the foundry in March 2013 so that the next step is the design of a readout board for test and debug purposes.
The simulation results and the working mechanism of the TDC in communication with the other blocks of the PET module have been reported in several contributions [119-123].

4. CONCLUSIONS

This thesis work has been focused on the design and validation of two circuit components which are usually employed in the electronic readout of positron emission tomography scanners: a constant fraction discriminator and a time to digital converter.

- The optimization of the CFD has been required to improve the timing performances of a double-head PET scanner previously implemented by the group of Medical Physics at INFN Pisa. Experimental results of the new readout board have confirmed that the dead time has been reduced from (270 ± 46) ns down to (129 ± 13) ns with a RMS time resolution decreased from 4 ns to 1.32 ns which leads to a higher precision in the event detection capability of the system. This has made it possible to employ the PET scanner during an in-beam acquisition because of the improved timing of the readout capable to sustain the high data rate. In addition, some studies have been performed to enhance the spatial resolution thanks to the use of ultra-transmitting glasses which are inserted between the crystal and the PMT in order to promote light spread and avoid overlap of responses. The CFD activity has been supported by the TPS project collaboration at INFN Pisa which aims to implement innovative treatment planning systems for hadrontherapy where in-beam PET is a powerful tool for non-invasive dose delivery monitoring. In addition, given the encouraging experimental results, a commercial version of the PET scanner is under development at INFN.
- The design of an integrated CMOS time to digital converter has been required for the implementation of a TOF PET/MRI module prototype with the support of the 4DMPET INFN project. An 8 channel prototype of 1.875 x 1.875 mm^2 has been submitted in UMC 65 nm LLLVT in March 2013; it features a unique ADDLL common to the whole chip and two 10 bits systolic counters running at 2.5 GHz which feed four channels each in pipeline fashion. Every channel communicates with a dedicated readout section designed in standard-cells which individually downloads and buffers time and energy data with a bin size of 100 ps and 400 ps, respectively. The system clock is generated by a ring oscillator that can be externally tuned with a resolution of 1%. A 47 bit output word is serially sent out of the chip at a measurement rate which is programmable between 31.25 MHz and 62.5 MHz with a double hit resolution of 170 ns. Measurements have to be performed in order to validate the simulated performances of the chip. Future improvements include the implementation of a PLL together with the design of ad hoc LVDS PADs in order to minimize the clock jitter and enable the use of the TDC in presence of magnetic fields.

PUBLICATIONS

The main experimental and simulation results of both the CFD and TDC have been reported in some journal and conference contributions which are listed below.

Journal contributions:

1. Sportelli G., Straub K., Aiello M., Attanasi F., Belcari N., Camarlinghi N., Cirrone G.A.P., Cuttone G., Ferretti S., Marino N., Nicolosi D., Romano F., Rosso V., Del Guerra A., "Full in-beam PET measurements of 62MeV protons onto a PMMA target", *Nucl. Instr. and Met. in Phys. Res. Sec. A*, ISSN 0168-9002, 10.1016/j.nima.2012.08.100.
2. Rosso V., Battistoni G., Belcari N., Camarlinghi N., Ferrari A., Ferretti S., Kraan A., Mairani A., Marino N., Ortuno J.E., Pullia M., Sala P., Santos A., Sportelli G., Straub K., Del Guerra A., "A new PET prototype for proton therapy: comparison of data and Monte Carlo simulations", submitted to JINST_014P_2012.
3. Straub K., Belcari N., Camarlinghi N., Ferretti S., Marino N., Rosso V., Sportelli G., Del Guerra A., "Study of UT glasses for pixel identification performance in multi-anode PMT-based detectors for PET", *Nucl. Instr. and Met. in Phys. Res. Sec. A*, ISSN 0168-9002, 10.1016/j.nima.2012.08.101.
4. Marino N., Ambrosi G., Baronti F., Bisogni M.G., Cerello P., Corsi F., Fanucci L., Ionica M., Marzocca C., Pennazio F., Roncella R., Santoni C., Saponara S., Tarantino S., Wheadon R., Del Guerra A., "An innovative detection module concept for PET", 2012, *JINST*, Vol. pp. 7 C08003.
5. Cerello P., Pennazio F., Bisogni M.G., Marino N., Marzocca C., Peroni C., Wheadon R., Del Guerra A., "An innovative detector concept for hybrid 4D-PET/MRI imaging", *Nucl. Instr. and Met. in Phys. Res. Sec. A*, Vol. 702, 2013, pp. 6-9.

Conference contributions:

1. Sportelli G., Camarlinghi N., Straub K., Belcari N., Bisogni M. G., Cirrone G. A. P., Cuttone G., Ferretti S., Marino N., Ortuno J. E., Romano F., Rosso V., Santos A., Del Guerra A., "Feasibility of a PET Acquisition System for Full in-Beam Monitoring in Proton Therapy", 2012 IEEE NSS/MIC/RTSD Anaheim, California, 27 Oct. – 3 Nov. 2012.
2. Pennazio F., Ambrosi G., Bisogni M.G., Cerello P., Corsi F., Del Guerra A., Ionica M., Marino N., Marzocca C., Morrocchi M., Peroni C., Pirrone G., Santoni C., Wheadon R., "SiPM-based PET Module with Depth of Interaction", IEEE Nuclear Science Symposium, Medical Imaging Conference, Anaheim, California, USA, 29 October - 3 November 2012.
3. Marino N., Saponara S., Baronti F., Bisogni M.G., Cerello P., Ciciriello F., Corsi F., Fanucci L., Ionica M., Licciulli F., Marzocca C., Morrocchi M., Santoni C., Roncella R., Wheadon R., Del Guerra A. , "TDC-based readout electronics for

real-time acquisition of high-resolution PET bio-images", IS&T/SPIE Electronic Imaging 2013, Burlingame, California, USA, 3 - 7 February 2013.

4. Morrocchi M., Ambrosi G., Bisogni M. G., Cerello P., Corsi F., Ionica M., Marino N., Marzocca C., Pennazio F., Pirrone G., Santoni C., Wheadon R., Del Guerra A., "Development of a PET detector module with depth of interaction capability", 13th Vienna Conf. on Instr., Vienna, Austria, 11 – 15 Febr. 2013.

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