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Tesi di Dottorato di Ricerca

Design and Testing of Electronic Devices for Harsh Environments

Autore:

Nico Costantino _____

Relatori:

Prof. Luca Fanucci _____

Prof. Sergio Saponara _____

Ing. Guido Magazzù _____

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SOMMARIO

Questa tesi riporta una descrizione sintetica ed i principali risultati dell'attività condotta nell'ambito del programma triennale (2010-2012) di dottorato di ricerca in Ingegneria dell'Informazione presso l'Università di Pisa. L'attività di ricerca scientifica si è sviluppata in differenti settori, tra i quali Automotive ed esperimenti di Fisica delle Alte Energie, seguendo tuttavia un denominatore comune: lo sviluppo di dispositivi e sistemi elettronici per applicazioni sotto condizioni operative critiche.

Sono molteplici le applicazioni che forzano l'adozione di metodologie e strategie di design dedicate a questa tipologia di ambienti operativi: militari, biomediche, automobilistiche, industriali e spaziali. Lo studio di soluzioni mirate al soddisfacimento dei requisiti operativi specifici, rappresenta di conseguenza un interessante ambito di ricerca.

La prima attività di ricerca è stata inquadrata all'interno del progetto ATHENIS, finanziato dalla commissione CORDIS della Comunità Europea e finalizzato allo sviluppo di un System-on-Chip, un regolatore per alternatori per auto, in grado di unire ad un'innovativa flessibilità la capacità di lavorare sotto le condizioni operative più estreme adottate dall'industria automobilistica. In particolare è stato sviluppato un dispositivo denominato Intelligent Power Switch, in grado di pilotare carichi di diversa natura, quali lampadine ad incandescenza e LED, offrendo allo stesso tempo un alto livello di configurabilità ed adattabilità alle più estreme condizioni operative. Le numerose funzionalità che sono state integrate, tra cui la limitazione di corrente, la regolazione della tensione, la protezione dall'inversione di polarità e sovratensioni, l'accensione con slope controllato in corrente, unite a strategie di Over Current ed Over Temperature Protection, hanno richiesto la progettazione di un'architettura circuitale innovativa.

Il primo test-chip, realizzato in tecnologia AMS CMOS High Voltage 0.35 µm, è stato validato grazie allo sviluppo di un ambiente di test dedicato, che ha permesso la completa caratterizzazione del dispositivo evidenziandone le ottime prestazioni.

Il secondo ramo di ricerca si è collocato all'interno del progetto FF-LYNX, che ha coinvolto la sezione di Pisa dell'Istituto Nazionale di Fisica Nucleare (INFN), il Dipartimento di Fisica dell'Università di California Santa Barbara (UCSB) ed il Centro Europeo per la Ricerca Nucleare (CERN). L'obiettivo di questo progetto multidisciplinare è stata la definizione di un protocollo per la distribuzione dei segnali di Timing, Trigger e Control e l'acquisizione dei dati di readout negli esperimenti di Fisica delle Alte Energie. Nello specifico, l'oggetto di studio è stato l'implementazione del protocollo in interfacce Transmitter-Receiver all'interno del test-chip FF-TC1, realizzato in tecnologia IBM CMOS 130 nm. Durante questa attività sono state studiate ed implementate tecniche di radiation hardening al fine di garantire il corretto funzionamento operativo in ambienti ad alto livello di radiazioni, come il Large Hadron Collider (LHC) presso il CERN di Ginevra. In aggiunta, è stato sviluppato un emulatore funzionale alla validazione del protocollo FF-LYNX, basato sulla board PLDA XpressGXII con interfacciamento PCI-Express ad un host-PC. Un'ulteriore attività ha riguardato l'adattamento dell'emulatore come test-bed per il test-chip FF-TC1, permettendone l'esecuzione di test funzionali estensivi. Sono stati infine effettuati test sotto irraggiamento presso la X-

rays facility del CERN, che hanno comprovato la bontà delle tecniche di radiation hardening implementate.

ABSTRACT

This thesis reports an overview and the main results of the research activity carried out within the PhD programme in Information Engineering of the University of Pisa (2010-2012). The research activity has been focused on different fields, including Automotive and High Energy Physics experiments, according to a common denominator: the development of electronic devices and systems operating in harsh environments.
There are many applications that force the adoption of design methodologies and strategies focused on this type of environments: military, biomedical, automotive, industrial and space. The development of solutions fulfilling specific operational requirements, therefore represents an interesting field of research.
The first research activity has been framed within the ATHENIS project, funded by the CORDIS Commission of the European Community, and aiming at the development of a System-on-Chip, a regulator for alternators employed on vehicles, presenting both configurability and the ability to work at the harshest operating conditions of the automotive industry. Specifically, a novel Intelligent Power Switch has been conceived, capable of driving different kind of loads, such as incandescent bulbs and LED, showing a high level of flexibility and adaptability to the most extreme operating conditions. Several features have been integrated, including current limitation, voltage regulation, reverse polarity and over-voltage capability, control of current slope, combined with strategies as over-current and over-temperature protection, that have required the design of an innovative architecture.
The first test-chip, realized in AMS CMOS High Voltage 0,35 µm technology, has been validated thanks to the development of a dedicated test-bed, which has allowed the deep characterization of the device, proving its excellent performance.

The second branch of research has been carried out within the FF-LYNX project, which has involved the section of Pisa of the National Institute for Nuclear Physics (INFN), the Department of Physics of the University of California Santa Barbara (UCSB) and the European Organization for Nuclear Research (CERN). The aim of this multidisciplinary project has been the definition of a protocol for the distribution of Timing, Trigger and Control signals and for the readout in High Energy Physics experiments. In particular, the focus of the activity has been the implementation of the protocol into Transmitter-Receiver interfaces within the test-chip FF-TC1, realized in IBM CMOS 130 nm technology. During this phase, novel radiation hardening techniques have been studied and implemented in order to ensure the proper functioning in operating environments with a high level of radiation, such as the Large Hadron Collider (LHC) at CERN in Geneva. Besides that, an emulator for functional validation of the FF-LYNX protocol has been developed, embedded on the XpressGXII PLDA board, equipped with PCI-Express to interface with a host PC. An additional activity has required the modification of the emulator as a test-bed for the test-chip FF-TC1, allowing the execution of extensive functional tests. Finally, irradiation tests have been performed at the X-rays facility at CERN, which have demonstrated the good yield of the radiation hardening techniques implemented.

CONTENTS

INTRODUCTION

Harsh Environment applications represent an exciting new frontier, challenging the capabilities of designers of electronic devices. Extreme wide ranges of operating temperatures, high vibration levels, fluid exposure, moisture, high electromagnetic fields and hard transient disturbances represent some of the requirements and constraints for devices and systems employed in certain fields of application. The most critical ones are: military field, oil exploration systems, biomedical applications, automotive and space missions.
In order to fulfill such severe requirements, electronic designers for harsh environments need to follow design flows characterized by continuous steps of validation, at various levels, that will be described hereafter.
This thesis reports the main issues that have to be faced in the design of electronic devices and systems for harsh environments. The two research activities performed, have been focused on two of the harshest fields of applications: the automotive and the High Energy Physics (HEP) experiments. Besides the area, also the type of electronic devices developed are different: an analogue mixed-signal cell is the core of the first research activity in the automotive field, while a digital integrated circuit has constitued the result of the second branch, within the HEP field. In addition to the description of the hardening techniques and strategies implemented to make designed electronic devices suitable for the harsh environments, the overview of the two project flows represents a valuable content of this work.
Chapter 1 includes an overview of the harshest applications of electronic equipments, summarizing the main contraints of the automotive, military and space fields. A particular focus on operating temperatures and particle radiations is reported, since they represent the most critical issues to cope with in the conduction of the two research branches carried out during the PhD programme.
The description of the development, design and testing flow of an integrated circuit to be employed in HEP experiments is the content of Chapter 2. An overview of the HEP experiments scenario is reported in Paragraphs 2.1, 2.2, 2.3. The main features of the novel FF-LYNX protocol have been reported in Paragraph 2.4, while Paragraph 2.5 shows the architecture of the FPGA-based emulator conceived to validate the main figures of merit of the protocol. Paragraph 2.6 presents the architecture of the TX and RX interfaces and of the test-chip FF-TC1, with details on the radiation hardening techniques applied during the design. Paragraph 2.7 is related to the test-chip characterization, describing the test-bed as well as some of the results of the functional test. The procedure used for the Total Ionizing Dose (TID) irradiation test and the behavior of the test-chip under X-ray irradiation are described in this paragraph as well.
The second case study is highlighted in Chapter 3, where a flexible device named Intelligent Power Switch (IPS) for automotive applications is described.
Paragraph 3.1 discusses the main advantages offered by this class of smart power modules and the relevant requirements to be faced when designing an IPS for automotive applications. Paragraph 3.2 presents the design-flow of the proposed IPS realized to safely handle ordinary or extraordinary electrical and environmental conditions. In Paragraph 3.3 the IPS implementation in HV-CMOS 0.35 µm process is shown as well as a description of the testing flow performed. Experimental measurements carried out on a test-chip in a lab and, exploiting a

mechatronic prototype, also in a real automotive environment, are described in Paragraph 3.4.
Finally, the conclusions of this thesis are presented.

1 ELECTRONIC DEVICES IN HARSH ENVIRONMENTS

1.1 HARSH APPLICATIONS

Design of devices and systems for harsh environment applications represents a stimulating challenge for electronic engineers. In the current scenario, characterized by a constant demand for increasing processing capabilities, higher bandwidths and stricter reliability requirements, operating in a harsh environment forces the adoption of novel technologies and statregies. Several categories of harsh environments can be reported: military field including land-based, shipboard, airborne, missile-based applications; oil exploration systems; biomedical applications; automotive; space missions. Among these applications, the last one provides the best match in terms of the diversity of harsh environments and the need for low mass, and low power devices. The high variable space mission scenarios involve extreme exposures to mechanical shock and vibration loading, temperature, pressure, radiation, and chemical attack [1].
A brief description of the main fields of harsh application will be analyzed hereafter.

1.1.1 Automotive

Electronics for automotive works in one of the harshest environments, fulfilling extreme electrical constraints and ensuring high levels of reliability and durability, as the automotive manufacturers are offering extended warranties to consumers for 350,000 km/15 years or even more. Robustness against mechanical vibrations (up to 10Grms on engine), fluid exposure such as petroleum vapors and other chemicals, moisture, high electromagnetic fields and hard transient disturbances makes the automotive field extremely tough for electronic devices. Besides that, operating temperature at 125 °C under-hood and locally up to 175 °C, high voltage and reverse polarity capability, are critical additional requirements and constraints for systems and ICs designed to operate aboard a motor vehicle [28]–[33]. Obviously, the operating requirements to be fulfilled by an on-board IC depend on its position inside the vehicle. Maximum operating temperature shows a large spread based on the localization, starting from a value of 70 °C outside the cockpit, reaching 125 – 155 °C in proximity and attached to the engine, and arriving up to 175 °C on the transmission [30], [31]. Usually the present maximum permanent junction temperature for automotive integrated circuit technology is 150 °C, with 125 °C as maximum ambient temperature under-hood, but, depending on the device power and on its equivalent thermal resistance, extremely high junction temperatures, up to 200 °C, can be reached during particular and time limited profile mission [30].
Besides the temperature range, another aspect to be taken carefully into account in a hostile environment as the automotive one, is Electromagnetic Compatibility (EMC). In particular the transient disturbances, produced by switching electronic devices connected directly to battery producing “load dump”, must be minimized as these disturbances may interfere with the correct operation of all electronic equipments sharing the same supply voltage. Moreover, Electromagnetic Interferences (EMI) can propagate by radiation too, with a general risk of premature failures or temporary loss of functions [45].

Additional constraints for ICs operating in the automotive environment are protections against high transient over-voltage and over-current. These conditions can be due to short-circuit faults or to inductive and non-linear resistive loads. In both cases there is a significant in-rush current absorption.
An extra requirement for the most recent driver ICs used in automotive is the reverse polarity capability, that is the ability of withstanding temporary negative voltages on external pins, without the risk of damaging the connected electronic devices and avoiding in other words the destructive latch-up phenomenon. Integrating such protection is made harder by the need of using a low-cost technology, since automotive applications are extremely cost sensitive [32], [47].
As previously explained, the quality represents a very important aspect to be taken into account in the automotive field, indeed the "Zero Defects" concept represents the final goal in the automotive industry. These several constraints oblige towards the use of mature technologies, creating a gap with other IC products for instance in communication or computers. Such conservative approach is in contrast to the high performance required by the hostile environment in which ICs and power devices operate.

TABLE I.

AUTOMOTIVE OPERATING CONDITIONS [30], [31].

Location	Typical Continuous Max Temperature	Vibration Level	Fluid Exposure
On engine On trasmission	140°C	Up to 10 Grms	Harsh
At the engine (intake manifold)	125°C	Up to 10 Grms	Harsh
Underhood (near engine)	120°C	3 – 5 Grms	Harsh
Underhood (remote location)	105°C	3 – 5 Grms	Harsh
Exterior	70°C	3 – 5 Grms	Harsh
Passenger compartment	70-80°C	3 – 5 Grms	Benign

Fig. 1. Thermal infrared image of an automobile engine in operation: the cylinders hot zones can be noticed.

Because of the very harsh automotive operating environment, electronics modules in a car are often separated from the mechanical systems which they control. Locations like vehicle “firewalls” and fender wells offer the possibility of sinking module-generated heat while reducing exposure to temperatures created by the mechanical systems and allowing some access to airflow available under-the-hood. In this scenario the adoption of proper thermal management systems seems to be the only solution, with the drawbacks represented by the increase in weight and cost.
To keep at minimum power dissipation and up-to-temperature-design-limit, a key component in automotive electronics is the Intelligent Power Switch (IPS), aiming at implementing power driving and management tasks with high efficiency and with integrated protection and diagnostic features. One of the reseach branch carried out within the PhD Program is about the development of an IPS integrating full diagnostic, allowing to detect and to signal extraordinary conditions such as over-current and over-temperature to digital ECUs, by means of a digital interface. Furthermore the IPS developed is configurable to have the capability of driving different and inter-changeable kind of loads efficiently.

1.1.2 Military

The operating conditions in military applications are extremely harsh: high reliability is required in severe conditions, including thermal and mechanical shock vibration, cycling, humidity, corrosive, chemical/biological, and radiation degradation, and altitude changes [1]. The functional lifetime of electronic devices is 20-30 years, more than that of rapidly obsolete consumer electronics, which have an average service life of less than 5 years. For example, missiles are required to be stored for 10 to 20 years in any location in the world and still meet safety and reliability requirements. Avionics must undergo severe changes in temperature, humidity, acceleration, and atmospheric pressure within very short periods of time. As regards aeronautical applications, the gas turbine environment represents one of the harshest ones: sensors are employed for accurate, real time measurements of velocities, pressure, temperatures and concentrations of chemical species, as well as stresses on rotating components. The sensors are required also for the active control of parameters such as, combustion stability, pollution reduction, engine health management, and exhaust profile. The typical environment where they have to operate foresees temperatures up to 2500K and at pressures of 30-40 bar in supersonic combustion areas. Mechanical sensors on rotating components may experience centripetal accelerations up to 75,000 - 100,000g [1].
The trend of military electronics develoment has been governed by performance-based specification for several years. High development cost, high reliability, and high density range, with few parts shared between military and consumer electronics industry. Since the electronics industry has been gradually shifting away from the production of military grade electronic parts, mainly due to high costs and very low volume production, the use of commercial off-the-shelf (COTS) electronic components, which have lower maximum temperature ratings than MIL-SPEC devices, has become more frequent, offering major benefits in the areas of supply and cost. The gradual shift in industry towards all COTS parts, the increasing chip-level temperatures, and the higher circuit density of next generation electronics, together with the need for high reliability and long life cycles of all the parts and materials, has introduced new challenges for harsh environment

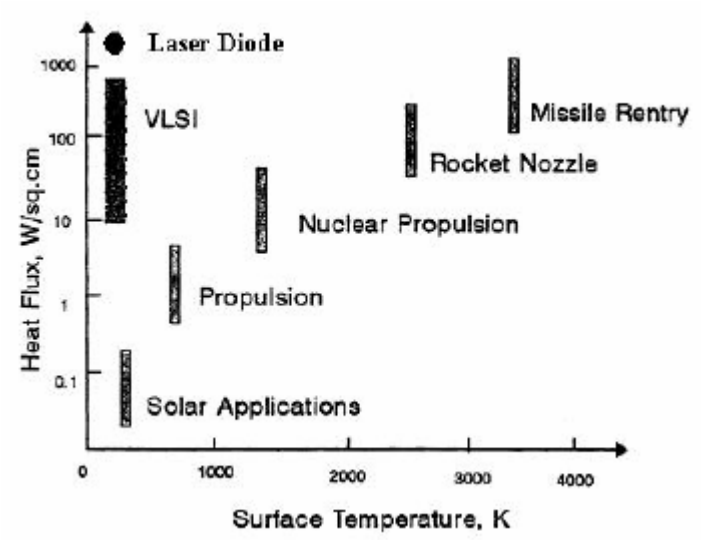


Fig. 2. Heat dissipation for various events [32].

applications. With miniaturization, the greatest dissipation requirement for high energy military lasers and MEMS devices is expected to be on the order of 100W/cm2 for high performance microprocessors and 1kW/cm2 for high power electronics components with a smaller allowable temperature difference (Fig. 12).
Heat dissipation has increased in every field of electronics, and in particular in the military one: as an example the heat flux associated with laser diodes is on the order of several kW/cm2 nowadays, comparable to the heat flux associated with ballistic missile entry.

1.1.3 Space

Space missions represent probably the harshest environment for electronic equipment: an interesting example is the Deep Space 2 (DS2) mission [1]. DS2 mission was constituted of two spacecraft systems with the aim to penetrate below the surface of Mars; the mission started in January in 1999 but unfortunately failed, indeed no transmission was received after the impact on the planet surface. The operating conditions in space missions are indeed extremely severe in temperature, pressure, radiation. Landed missions to the planet Venus [60], for instance, have to deal with an atmospheric ambient of 93 bars and 740K, with the presence of acid rain due to sulfuric acid clouds in the Venusian upper atmosphere. A third example is Europa, a moon of Jupiter, considered an interesting space exploration target due to the possible presence of a sub-surface ocean. The environment that electronic equipment should cope with, includes a combination of cryogenic temperature (100K) and intense radiation from being within Jupiter's magnetosphere. Estimates of the surface radiation exposure exceed 107 rad/month of mission life [61].
The environmental temperature in many space missions is significantly below the range for which conventional commercial-off-the-shels electronics is designed. Spacecraft operating in the cold environment of such deep space missions carry a large number of radioisotope or other heating units in order to maintain the

TABLE II

TYPICAL OPERATIONAL TEMPERATURES FOR UNHEATED SPACECRAFT [62].

Planet	Spacecraft Temperature
Mercury	175°C
Venus	55°C
Earth	6°C
Mars	-47°C
Jupiter	-151°C
Saturn	-183°C
Uranus	-209°C
Neptune	-222°C

surrounding temperature of the on-board electronics at approximately 20 °C. Indeed, as can be noticed in Table II, the operational temperatures for unheated spacecraft in the environment of outer planets would be not compatible with solid-state eletronic devices.

The primary power source on board of a satellite are the solar panels. When the panels are exposed to the sun they provide power to the load and to charge the on board batteries that are discharged when the satellite is in eclipse. The accumulators provide DC voltages in the 20 to 50V range (Power Bus), which supply few KW of power. Besides high power electronic unit (for Radar, Electrical Propulsion, etc.) the satellite is plenty of low power multi-output DC/DC converters, which convert the input voltage levels into a number of different output voltages from 2.2V up to few KV. To be taken into consideration that a typical "space" DC/DC converter is manufactured in few pieces so the minimisation of the cost design is necessary, unlike mass production where the recurring cost reduction is the main target. Flexibility is the second important aspect of these components: indeed, the DC/DC converters on-board supply several different kind of loads, digital, analogue, RF with very low noise requirement, scientific instrument and so on. Additional aspects to be considered in space applications are:

- The thermal management design is complicated by the fact that in space missions there is no air and therefore no convective heat transfer. Only conductive path are available for cooling the system to the satellite wall. Heat is then radiated to the surrounding space.
- The high vibration level during the launch, stress electrical components from a mechanical point of view. Heavier parts have therefore to be glued to the printed circuit board or to a mechanical frame.
- Obviously, reliability is a key factor in space application: that involves component de-rating and a continuous inspection during manufacturing phases. This means that every soldering and bonding have to be accessible and therefore often limiting the integration of different parts.

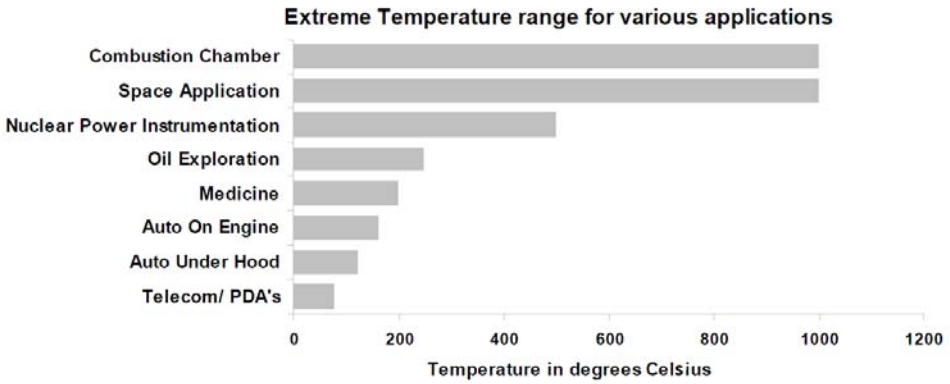


Fig. 3. Temperature range for various electronics applications.

- Radiation particles, as heavy ions, protons, electrons and γ ray continuously bombard electronic devices during flight operation. Shielding is sometime requested but it should be limited to sensitive items because it is made by high density materials.
- Redundancy is another key element in designing electronics for space applications. In case of failure of the nominal part, its redundant counterpart allows to operate nominally.
- Conducted emission/susceptibility requirements change for different satellites even though the Mil-STD461 is a common background. That makes difficult to define a standard EMI filter.

1.2 HARSH ENVIRONMENTS: REQUIREMENTS AND CONSTRAINTS

1.2.1 Operating temperature

A great deal of work has been spent over the years on the development of highly effective cooling systems for the heat removal in power electronics, optoelectronics, and telecommunication systems. Yet, electronic components and systems capable of high-temperature operation allow designers to eliminate, or at least minimize, the high cost for cooling systems currently required to protect electronics from extreme environments. In the automotive, for instance, the IPS are currently largely employed to drive the different loads placed on each vehicle. They aim at implementing power driving and management tasks with high efficiency and with integrated protection and diagnostic features.
In a typical electronic system operating in high temperature environment, the heat removal from the chip may require the use of several heat transfer mechanisms to transport heat to the coolant or the surrounding environment. Three basic heat transfer modes exist: conduction, convection and radiation. Thermal management techniques can be classified as either passive, active, or a combination of the two (hybrid).

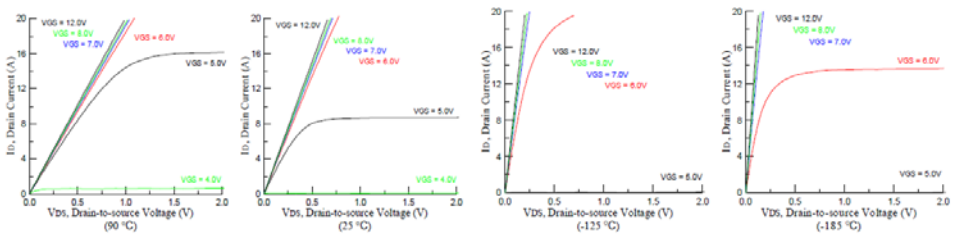


Fig. 4. Output characteristics of a power mosfet, by varying the operating temperature.

The passive modes, relatively reliable and simple to implement, are however performance-limited for many high power applications. The main passive thermal management techniques are:

- Conduction (metal spreader, interface materials, adhesives, pads, pastes, epoxy bond)
- Natural convection (finned heat sinks, ventilation slots, liquid immersion cooling)
- Radiation (paints, coatings, mechanical surface treatments)
- Phase change (phase change materials, heat pipes, thermosyphons, vapor phase chambers).

Active thermal management techniques, requiring input power, provide increased performance/capacity, but also:

- Reduced reliability and added complexity. The essential active techniques include:
- Forced convection (fans, nozzles)
- Pumped loops (heat exchangers, cold plates, jet/spray)
- Refrigerators & coolers (vapor-compression, vortex,thermoacoustic, thermoelectric/Peltier)

In the applications where conventional thermal management is employed, “smart cooling systems” integrating control loops consisting of the control chip, temperature sensors, and heat pumps, guarantee longer lifetime of the devices. In general, traditional air cooling semiconductor devices have been partly replaced by methods using liquid coolants. A classical example is power electronics where several switching components with variable frequency and voltage, require intensive cooling: in these cases, air cooling does not allow to cope with the high heat flux densities to be removed and therefore liquid coolants are used to handle high power losses, since the heat transfer coefficients from the component to the coolant are up to two orders of magnitude higher.
The temperature sensitivity of the electrical components parameters, needs to be carefully considered in the design of electronic systems operating in harsh environment. In [62] a deep analysis of semiconductor devices, capacitors, magnetic cores and pulse-width modulation chips has been performed. As reported in Fig. 4, there is a strong influence of operating temperature on family curves of drain current (I_D) versus drain-to-source voltage (V_{DS}) at various gate-source

TABLE III

IMPACT OF TEMPERATURE ON THE ELECTRICAL BEHAVIOR OF SENSORS AND SEMICONDUCTOR DEVICES [63].

Device	Effect of high temperature
Thermistor	Number of charge carriers and conductivity increases
Piezoresistive sensors	Sensitivity decreases
with pn-insulation of the piezoresistors	Junction leakage current increases
Schottky diodes	Forward voltage drop decreases
	Reverse current increases with T^2
Pn-diode	Voltage drop in forward direction decreases
	Leakage current increases exponentially
Bipolar transistor	Base-emitter voltage decreases at collector current
	Current amplification increases with T^x (1<x<2)
JFET	Channel mobility decreases with $T^{3/2}$
	Pich-off voltage increases
MESFET	Similar to JFET
MOSFET	Channel mobility decreases with $T^{3/2}$
	Leakage current of pn-junctions increases exponentially
	Threshold voltage decreases

voltages (V_{GS}). The first deviation noticeable with the temperature is the downward shift of the switching curves, for a given gate voltage, as the temperature is decreased. This behaviour is due to the increase in the gate threshold voltage with decreasing temperature. The second deviation is the increase in slope of the switching curves as the temperature is lowered. This trend is primarily caused by the decrease in the on-state resistance with decreasing temperature.

1.2.2 Particle radiation

Particle radiations represent a very critical aspect of electronic employment both in Space and High Energy Physics applications. Radiation effects are traceable to the interaction of radiation (photons, particles) with the materials composing the electronics. Energy can be released by the photon/particle via ionization or nonionization mechanisms. Depending on the operating environment different kind of radiation can be present:

- Protons and other hydrogen nuclei stripped of their electrons
- Positively charged alpha particles (α)
- Helium ions at high energy levels
- HZE ions, whose nuclei are heavier than helium
- Positively or negatively charged beta particles (β+ or β-)
- Photons (X, γ)
- Neutrons
- Neutrinos

- Hadrons

The energy released by photon/particle leads to different phenomena, via ionization or non-ionization mechanisms. Photons generate small density of e-h pairs, while heavy ions can cause large density of electron-hole pairs. Protons and neutron create high density charges for direct ionization, due to possible nuclear interaction of the particle with the semiconductor lattice. Finally, hadrons can lead to dislocation of atoms from lattice.
Two possible effects have to be distingushed in radiation environment: cumulative effects or single event effects.
Cumulative effects are gradual effects taking place during the whole lifetime of the electronics exposed in a radiation environment. A device sensitive to TID or displacement damage will exhibit failure in a radiation environment when the accumulated TID (or particle fluence) has reached its tolerance limits. The TID is the measurement of the dose, that is the energy, deposited in the material of interest by radiation in the form of ionization energy. The ionization dose is deposited by particles passing through the materials constituting the electronic devices. This happens during the whole time the device is exposed to radiation.
The level of radiation hardness against TID depends on the final application of the circuit, i.e. for an an interplanetary mission the TID required for the components are in the range of MRad [64], while in the case of low orbital satellites the required TID is ~100kRad. In HEP experiments such as SLHC the required TID hardness is up to 100 Mrad. In the LHC environment, ionization effects are induced by the ionization energy deposited by charged hadrons, electrons, gammas and neutrons (even though the last two are not directly ionizing, they can induce ionizing energy depositions).
The most important effect of TID is the trapping of charges within the oxide, mainly positive. The trapping of the charges is bigger in the transition region from gate oxide to field oxide, known as peak region in old technologies, and substituted by the shallow trench isolation (STI) in the sub-micron technologies. The accumulation of positive charges at the borders of the linear transistors produces the leakage current on the NMOS transistors in cut-off mode, while PMOS transistors are less sensitive to the accumulation of this charge. The use of Edge Less Transistors (ELTs) avoids the transition region between the drain and source, and eliminates the leakage between them.
Single Event Effects (SEE) are instead due to the energy deposited by one single particle in the electronic device. Therefore, they can happen in any moment, and their probability is expressed in terms of cross-section. A device sensitive to SEE can exhibit failure at any moment since the beginning of its operation in a radiation environment.
SEE can be classified as:

- Transient: spurious signals propagating in the circuit (Single Event Transient, SET).
- Static: errors overwriting information stored by the circuit (Single Event Upset, SEU).
- Permanent: destructive errors cause irreversible effects such as the latch-up of the device (Single Event Latchup, SEL) or dielectric breakdown of the gate oxide (Single Event Gate Rupture, SEGR).

SEE errors are related to the pass of a high energy particle that releases energy creating hole-electron pairs: the charge is collected in noded of the circuit causing a transitory spike (SET), the flip of the value (SEU), or the ignition of the latch-up effect related to the PNPN parasitic structure of the technology.
Transient errors are frequent in combinational logic, generating asynchronous signals, that can propagate through the circuit during one clock cycle and also sometimes propagate to a latch and become static.
Static errors can be corrected by outside control, by overwriting information stored in the circuit, but a rewrite or power cycle can correct the error with no permanent damage.
Permanent or hard errors are those leading to a permanent error, which can be the failure of the whole circuit. They cannot be recovered unless detected at their very beginning in some cases (as for Latchup). In that case, it is possible to interrupt the destructive mechanism and bring back the circuit to functionality.

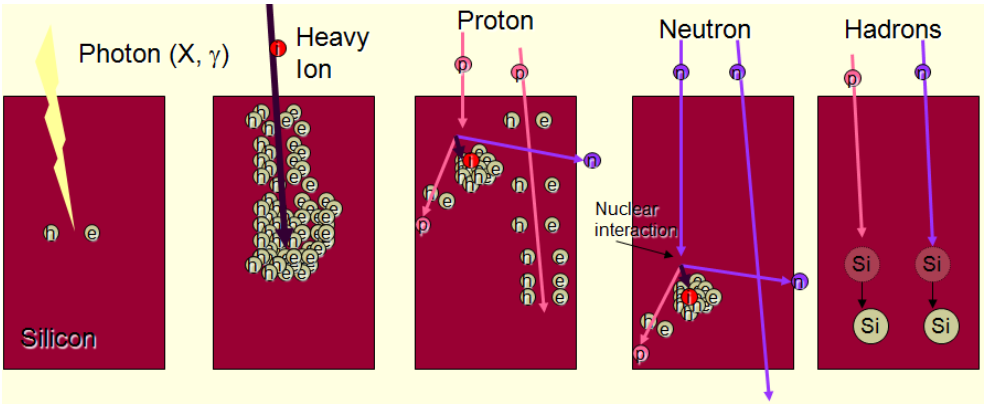


Fig. 5. Effects of different particle radiations on Silicon structure.

2 HIGH ENERGY PHYSICS EXPERIMENTS: DEVELOPMENT, DESIGN AND TESTING FLOW OF AN INTEGRATED CIRCUIT

2.1 Introduction

Particle physics is the branch of physics that studies the most basic constituents of matter and their interactions. Modern particle physics research is focused on subatomic particles, i.e. particles with /dimensions and mass smaller than atoms, including atomic constituents such as electrons, protons and neutrons and particles produced by radiative and scattering processes, such as photons, neutrinos and muons. Since many elementary particles do not occur under normal circumstances in nature, to allow their study they are created and detected by means of high energy collisions of other particles in particle accelerators: therefore, particle physics is often referred to as High Energy Physics (HEP).

The main instruments for HEP are particle accelerators, large and complex machines that produce beams of particles and provide them with the high energies needed for HEP experiments. Accelerators typically employ electric fields to increase kinetic energy of particles and magnetic fields to bend and focus the beam, which is then collided against a fixed target or with another particle beam: the high energy collision produces the new particles and events that must be detected and studied. Beside the use in particle physics, the applications of accelerators nowadays span from industry (e.g. ion implantation in electronic circuits) to medicine (radiotherapy), with different ranges of energy for the different fields application. Current accelerators for HEP work in the GeV and TeV energy range (referring to the energy provided to particle beams) and typically treat beams of electrons, hadrons and heavy atomic nuclei; the structure can be linear (LINAC, LINear ACcelerator), with the particle beam traveling from one end to the other and colliding against a fixed target, or circular (cyclotrons, synchrotrons), with the beams traveling repeatedly around a ring, gaining more energy at every loop and colliding with other beams running in opposite direction

HEP experiments thus consist in colliding particle beams in accelerators and studying the results of the collisions using particle detectors that surround the interaction point. Particle detectors are devices used to track and identify high-energy particles produced in collisions, also measuring their attributes like momentum, charge and mass. A particle detector is typically made up of different layers of sub-detectors, each specialized in revealing and measuring different particles and properties of particles. To help identify the particles produced in the collisions, the detector usually includes a magnetic field that bends the path of charged particles: from the curvature of the path, it is possible to calculate the particle momentum which helps in identifying its type. Particles with very high momentum travel in almost straight lines, whereas those with low momentum move forward in tight spirals.

To record and analyze events produced by collisions in an experiment, information about particles detected by sensors in the detector are converted into electric signals, which are then collected by dedicated electronic components embedded in the detector and located in close contact with the sensors themselves: these devices, usually called Front-End (FE) electronics, deal with the proper conditioning of signals (e.g. amplification, shaping, buffering, analog to digital

conversion) and their transmission to remote data acquisition systems that perform data analysis and storage. The number of interactions per second is very high (a typical order of magnitude is billions of particle interactions per second); a measure of collision rate is the so-called luminosity, which is usually expressed in $cm^{-2} \cdot s^{-1}$ and for a two-beam collider is defined as the number of particles per second in one beam multiplied by the number of collisions per unit area in the other beam at the crossing point. Collision rates of this order of magnitude produce amounts of raw data that range from tens of terabyte to a petabyte per second, which is beyond the possibility of any data acquisition and storage system. Therefore, since the interesting events are a very small fraction of the total, the total amount of data is filtered by means of a trigger system: raw data are temporarily buffered in the FE electronics while a small amount of key information is used by trigger processors to perform a fast, approximate calculation and identify significant events: the result of this processing is a trigger signal that is sent back to FE electronics to command a data readout, i.e. the transferring of a selection of the buffered data towards the remote system. This way, the amount of data to be transferred is reduced to rates that can be handled by the readout system (a typical order of magnitude is hundreds of MB/s from each FE device), and only the interesting events are selected.

HEP experiments constitute a very challenging application for electronics, since the equipment must deal with large amounts of data and high data rates, with tight timing and data integrity constraints and operate in an environment that is intrinsically hostile due to the high levels of radiation. In particular, electronic devices and systems employed in HEP experiments must tolerate high levels of ionizing radiations and the associated cumulative effects and SEE.

The LHC, the well known facility at the European Organization for Nuclear Research (CERN), located near Geneva in Switzerland is the world's most energetic accelerator. It currently allows to produce roduce proton–proton collisions at a centre-of-mass energy of 14 TeV and a luminosity of up to 10^{34} $cm^{-2} \cdot s^{-1}$, yet an upgrade of its performance will be gained within the sLHC project (super LHC), which aims for a tenfold increase in luminosity for 14 TeV proton–proton collisions, achieved through the successive implementation of several new elements and technical improvements that are scheduled for 2013–2018. The final luminosity will be 10^{35} $cm^{-2} \cdot s^{-1}$, providing a better chance to see rare processes and improving statistically marginal measurements.

Obviously, such upgrade in terms of luminosity will lead to complex challenges that have to be developed, not only in radiation hard detectors but in powering, cooling, thermal management and integration engineering. As radiation damage scales with integrated luminosity, the radiation environment inside the detector will increase.

Besides the previous highlighted point, the small size represents a very critical aspect to be taken into account for electronic devices working in HEP experiments: the space available for devices and cabling inside a particle detector is usually very limited due to the large amount of different components (readout and control systems, cooling systems, mechanical structures and so on) that must be integrated in a small area around the interaction point; in addition, bulky equipments are undesired because any non-sensor material interferes with the measure by deflecting and absorbing the particles that must be detected (the amount of material surrounding the interaction point, characterized with the

radiation thickness of each component/layer, is usually referred to as *material budget*).
Another important requirement of electronic devices for HEP experiments is low power dissipation: due to the high concentration of electronic equipment inside the detector, power density is a major issue because it dictates the cooling requirements; cooling systems represent a critical aspect in HEP experiments because they complicate the material budget and the mechanical requirements.

2.2 DAQ/TTC SYSTEMS FOR HEP EXPERIMENTS

HEP experiments have non-homogeneous latency and bandwidth requirements for data transfers between FE electronics and remote trigger processors and control/data acquisition systems. In most of the past and current HEP experiments, e.g. [2-6], different custom protocols have been used to distribute Timing, Trigger and Control (TTC) signals and to perform the Data Acquisition (DAQ) within the same experiment and, sometimes, within the same detector.
A typical control and readout system for a HEP experiment can be schematized as in Fig. 6.

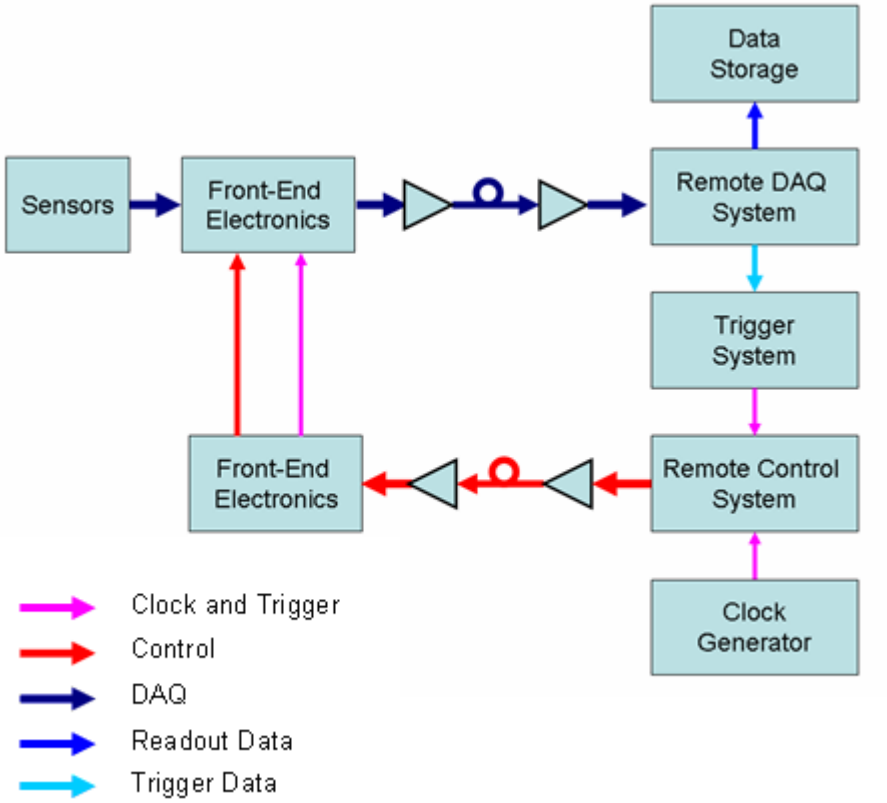


Fig. 6. Typical architecture of the control and readout system for a HEP experiment.

Signals generated by the interaction with sensors of particles produced in the beam collisions are handled by FE electronics embedded in the detectors and transferred to remote DAQ systems, located far away from the experiment area to keep them in an environment that is free from the intensive levels of radiation that are present in the proximities of the interaction point. Typically, the transfer is carried out by means of electrical links for a first stretch inside the detector, and then through optical links that allow to cover the long distances (hundred of meters) from the experiment area to the remote DAQ system, and provide the large bandwidth needed (up to tens of Gbit/s). A subset of the transferred data is used to perform trigger calculation, and the generated trigger command is sent back to FE electronics along with timing (clock) and control signals by a remote control system, also called TTC system, that manages the configuration and monitoring processes in the FE electronics.
In future experiments, the use of “standard” and flexible protocols will contribute to meet the mentioned requirements about latency and bandiwidth, with a reasonable impact on the development and production costs and with a reduction of the complexity of the control and readout systems (hardware, firmware and software).
The GigaBit Transceiver (GBT) project represents an example of what indicated above, aiming at the fulfillment of the high data rates and radiation doses foreseen in the physics experiments of the future upgrade of the LHC accelerator, the SLHC [19-22]. Indeed, because of the high beam luminosity planned for the SLHC, in this scenario the data rate expected is very high and, besides that, links and electronic components need to be capable of sustaining high radiation doses. The GBT ASICs address this issue implementing a radiation-hard bi-directional 4.8 Gb/s optical fibre link between the counting room and the experiments. In particular, the goal of the GBT project is to produce the electrical components of a radiation hard optical link, following the scheme described hereafter: one half of the system resides on the detector and hence in a radiation environment, therefore requiring custom electronics. The other half of the system is free from radiation and can use commercially-available components. Optical data transmission is via a system of opto-electronics components produced by the Versatile Link project. The architecture incorporates timing and trigger signals, detector data and slow controls all into one physical link, hence providing an economic solution for all data transmission in a particle physics experiment.
The FF-LYNX project, one of the research branch studied during the PhD program [8], shares the same goal with the GBT project, without focusing on specific physics experiments having fully defined bandwidth and radiation tolerance requirements. FF-LYNX aims at the definition of a fast and flexible protocol that allows the use of the same physical serial links for the transmission of TTC signals and the DAQ and the development of a full set of Transmitter (TX) and Receiver (RX) interfaces to optical and electrical serial links implementing this protocol. The main feature of the FF-LYNX project is its feasibility that makes it suitable for different HEP experiments, e.g. CMS End-Cap Muon detector in [23], as well as medical physics applications, e.g. block detector for Positron Emission Tomography (PET) in [24].

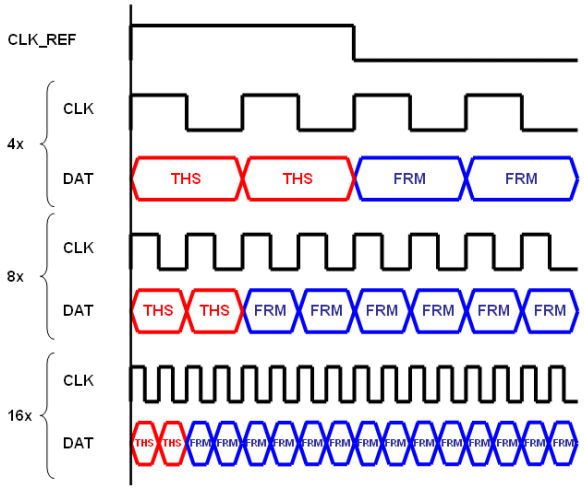


Fig.7. FF-LYNX serial data stream, fast and reference clock in the three speed options: the first two bits of each cycle are assigned to the THS channel, the remaining bit to the FRM channel.

2.3 DESIGN FLOW OF ELECTRONIC SYSTEMS FOR HEP APPLICATIONS

The methodology followed during the FF-LYNX project represents a case study of development flow for electronic systems and devices operating in harsh environment, such as HEP experiments.
The entire methodology has included design activities and successive phases of verification steps, in order to validate the results obtained in each stage. A key step characteristic of this methodology has been the use of a high-level software model of the link where the proposed FF-LYNX protocol would have been applied, allowing the comparison of different choices about the various aspects of the protocol itself on the basis of conveniently chosen cost functions and figures of merit (e.g. bandwidth efficiency, robustness to errors, etc.).
The project work flow is reported in Fig. 8; the main phases of the flow are hereafter described:

- Analysis of the requirements of the future TTC and DAQ systems: within this starting phase it has been performed an evaluation of trigger and data rates in different luminosity conditions and with different sensor geometries (e.g.: pixel and strips with different sizes) and detector architecture (e.g.: number of detector layers and distance of the layers from the interaction point).
- Protocol definition: starting from the detailed requirement analysis, the second stage of the activity is the definition of the FF-LYNX protocol in a first, tentative version to be submitted to successive verification, and open to refinements following suggestions and requests from FF-LYNX collaborators in the field of HEP experiments (physicists and engineers involved in the design of detectors). This first version of the protocol has been defined focusing on the requirements about data rate, trigger latency and error robustness by means

of a mix of custom and standard solutions typical of the data-link layer of the ISO/OSI model.

- Validation of the protocol in a high-level simulation environment: the cost metrics have been integrated within an Integrated Simulation Environment (ISE), based on System-C language [21]. This high-level software simulation environment has modelled the transmitter and receiver interfaces, implementing the defined protocol, and a surrounding test bench providing the expected stimuli and measuring various aspects of the link performance. This environment has been realized in System-C, offering a highly configurable model of the link in order to allow the test, during the phases of protocol definition and refinements, of different versions of the protocol. To validate the protocol and allow comparisons between different versions, the basic task of the high-level simulator has been the evaluation of specific cost functions and figures of merit (e.g. bandwidth efficiency, data loss rate, data latency) that has been defined on the basis of system requirements; furthermore, by evaluating these parameters, the high-level simulator has also offered valuable information about hardware aspects of the interfaces, such as optimum size of buffers.
- Definition of the interfaces architecture: after the protocol validation phase, the architecture of the hardware interfaces implementing the first version of the protocol has been defined, following indications from the high-level simulation phase. The overall architecture of the transmitter and receiver interfaces has been divided into functional blocks in order to simplify the implementation and to allow the separate verification, in the successive HDL simulation phase, of the correctness of each sub-function.
- VHDL modeling and simulation: following the definition of their architecture, a model of the interfaces using a Hardware Description Language (HDL) has been created for functional simulation and successive synthesis. This model has been built in a highly-parameterized form in order to allow quick changes to follow indications coming from the high-level simulator. Each block of the architecture has been separately modelled and tested in a specific test bench through functional simulation to verify its functionality, so to progressively build an overall model that was verified in all its parts. The final verification phase has been focused on the the complete transmitter-receiver model by means of a test bench including emulators of the transmitting and receiving hosts to verify the overall functionality of the system.
- FPGA prototype development: a phase of FPGA-based emulation has been foreseen, to provide additional verification of the system functionality (especially about the aspects that are difficult to assess in the software simulator, due to excessive simulation time: i.e. the evaluation of the effect of transmission errors on data integrity with realistic bit error rates – in the order of 10^{-9} or less – has required few days of simulation) and to evaluate different solutions for the physical layer. The HDL models of the interfaces have been synthesized on an FPGA along with the model of a surrounding test system that has provided test vectors to the interfaces model and recorded the test results.

- Test chip design: the design and implentation of a test chip has completed the overall development flow. The test-chip FF-TC1 has embedded the transmitter and receiver interfaces and the same test bench architecture previously synthesized on the FPGA emulator. This phase has required the application of Radiation By-Design Hardening techniques, in order to make the test chip suitable for the radiation dose foreseen in the operating environment. In order to deeply evaluated the functioning of the interfaces, as regards both timing and radiation requirements, an accurate validation flow has also been performed.

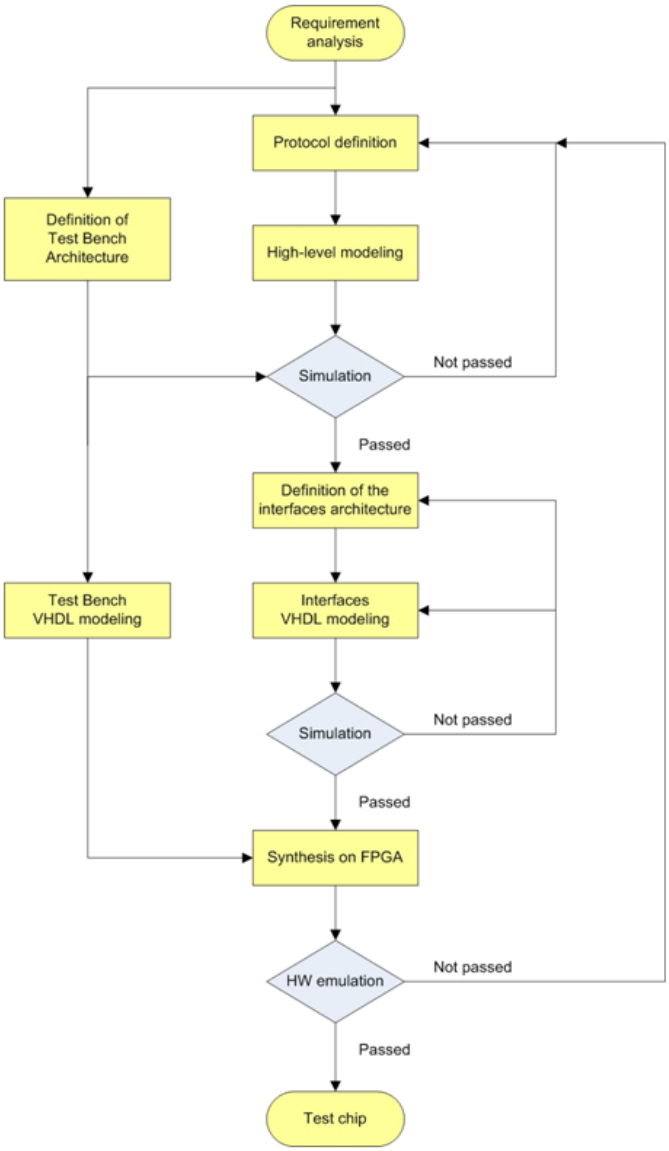


Fig. 8. The FF-LYNX project work flow.

2.4 THE FF-LYNX PROTOCOL

The FF-LYNX protocol is a “double wire” serial, packet based protocol with data structure independent w.r.t. data type (e.g.: configuration data, monitoring data, commands, row data). It has been developed with the aim of offering a high degree of flexibility with respect to various parameters and aspects of the transmission systems, such as the data rate and the data format. Regarding data rate, the protocol is proposed in different versions with different values of the data transmission speed, chosen as multiple of the reference clock frequency of the application. The three speed options are: 4xF, 8xF and 16xF (F = reference clock frequency) that, in the LHC scenario (F = 40 MHz), correspond to 160, 320 and 640 Mbps respectively. The reference clock used in the FE electronics is recovered in the destination devices from the high speed clock used in the transmission of the serial stream and its synchronization with the reference clock in the source device is guaranteed by the protocol itself.
The integrated distribution of TTC signals and DAQ represents another key feature of the FF-LYNX protocol, making it suitable both for the Up-Links from the FE electronics to the remote acquisition and elaboration system, and for the Down-Links from the trigger processor and the central control system to the FE electronics. This is obtained by multiplexing two channels in the time domain: the THS channel used for Triggers, frame Headers and Synchronization patterns and the FRM channel for data Frames. The THS channel employs the first two bits after the rising edge of the reference clock for the transmission of triggers, headers and synchronization commands, encoded with 6-bit patterns, transmitted in three consecutive cycles of the reference clock.
Triggers have higher priority with respect to frame headers and synchronization commands, that can be transmitted only when the THS channel is not used for triggers for at least three consecutive clock cycles. This choice is compatible with the minimum number (three) of clock cycles between two consecutive triggers foreseen for the upgrades of the LHC experiments and it prevents effects of single bit flips in the data stream on the pattern detection and on the correct reconstruction of its timing.
The remaining 2, 6 or 14 bits (FRM channel) are used for data frames tagged by frame headers transmitted in the THS channel. Such strategy allows the transmission of triggers to the FE circuits, as well as user data (configuration/control commands) on the same physical link.
The data format is transparent with respect to the data type (e.g.: commands in the Down-Link toward the detector or data from Front-End circuits in the Up-Link from the detector): the protocol transfers user information from the transmitter to the receiver without introducing any structure in the payload, thus accepting any kind of data format. Data frames in the FRM channel are tagged by frame headers transmitted in the THS channel and have the general structure shown in Fig. 9 and described below:

- Frame Descriptor (7 bits, encoded with Hamming in 12 bits)
  This field contains the following frame information:

1) Frame_Length (4 bits) → it indicates the length of the frame, including the Payload and an optional 16-bit field (Label) between the Frame Descriptor and the Payload; it is expressed in number of 16-bit words (1→16);
2) Label_On (1 bit) → it specifies whether the optional Label between the Frame Descriptor and the Payload is present or not; if a data packet with Label is fragmented in multiple frames, the Label is attached to the first frame only;
3) Data_Type (1 bit) → it specifies the data type: (e.g.: ”raw” data generated after the reception of a L1 trigger or configuration or monitoring data, generated after the reception of a command);
4) Last_Frame (1 bit) → it indicates, in the transmission of a data packet fragmented in multiple frames, whether the current frame is the last one of the sequence of frames or not.

- Label (16-bits)
  The Label can follow the Field Descriptor and precede the Payload. In the Down-Link it can be used to transmit destination address and operation code of commands (e.g.: reset, write/read access to registers). Data frames generated by read commands as well as empty data frames generated by write commands and used as acknowledgements can keep the Label of the original command frame. In the Up-Link the label can be used to transmit the time stamp or the trigger number associated to the transmitted “raw” data.
- Payload (N x 16-bit words)
  Different data types can be transmitted in the payload: configuration or monitoring data generated after the execution of a command, “raw” data generated after the reception of a L1 trigger, “trigger” data to be used in embedded or remote processors for the generation of the L1 Trigger. Long data packets can be fragmented into multiple data frames and a “Last Frame” flag in the Frame Descriptor identifies the last one. The maximum length of the data frames is determined by the depth of the input/output buffers in the transmitter and receiver interfaces.
- CRC (8 bits)
  The Cycle Redundancy Check (CRC) can be optionally applied to the Payload and the Label to increase robustness against transmission errors

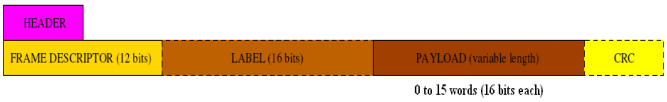


Fig. 9. Structure of data frames in the FF-LYNX protocol

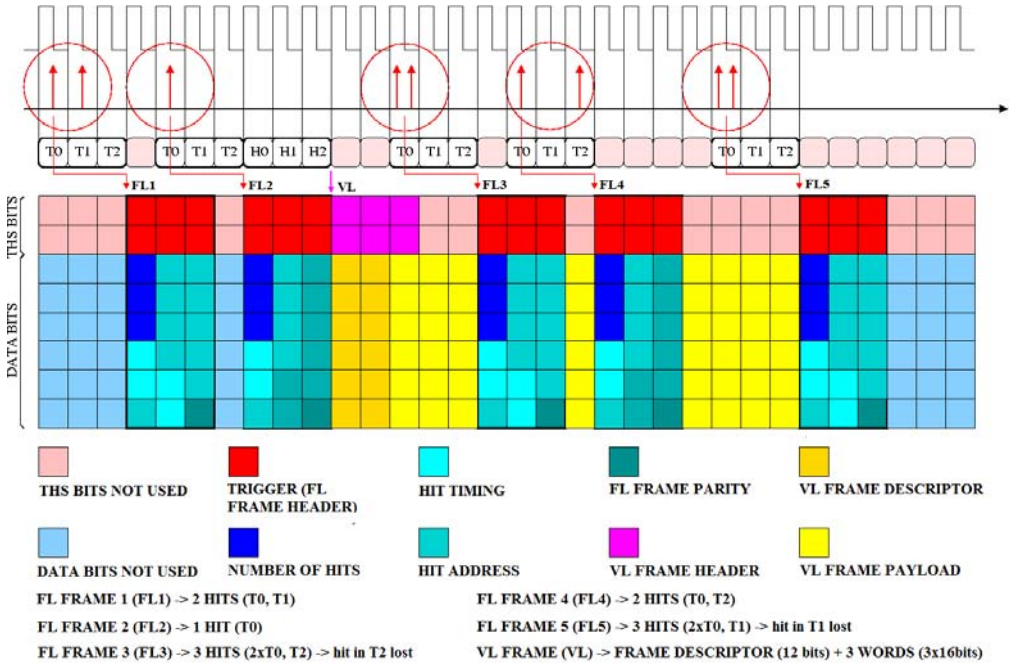


Fig.10. Possible up-link data stream in the 8xF link speed option: variable and fixed latency frames, carrying hit information, are transmitted through the THS and FRM channel.

The robustness of critical information against transmission errors is ensured by means of Hamming codes and custom encoding techniques. The custom 6-bit encoding applied to the THS channel allows the correct recognition of the transmitted commands and the reconstruction of their exact timing, while the Hamming code, used for the Frame Descriptors, corrects single bit-flips and detects burst errors, performing Single Error Correction (SEC) and Double Error Detection (DED).
Another important feature of the FF-LYNX protocol is represented by the easy coupling of the interfaces with the core of the host circuits, indeed interfaces to electrical serial links are provided with both serial and parallel ports implementing a very simple handshaking protocol with the core of the host circuits.
The most innovative element offered by the FF-LYNX protocol is the flexibility with respect to the latency of the frames: in addition to Variable Latency Frames (VLF), having no constraints in terms of latency, the transmission of Fixed Latency Frames (FLF), with fixed and low latency, is supported. This feature broadens the range of applications of the FF-LYNX protocol: an example is its applicability to the data transfers from FE electronics to embedded or remote trigger processors that will use “trigger” data in the generation of the Level 1 Trigger (L1T). The “trigger” data, as hit coordinates to be used for track finding or hit timing, can be encapsulated in FL frames and transmitted from the FE circuits to a remote trigger processor through the Up-Links. The transmission of the frame starts when

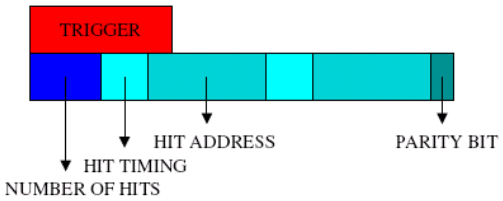


Fig. 11. Possible structure of data frames (fixed length) in the FF-LYNX protocol

"trigger" data to be used in the L1T Trigger generation are detected in the FE circuits. Frame length and link speed are fixed taking into account the number of hits that can occur during the clock cycles involved in the data transfer.
In Fig. 10 the possible structure of a 3-clock-cycle-long data frame is shown: 2 bits are used to identify the timing of the hits and 5 bits to encode the hit address (e.g.: the address of the cluster where the hit occurred in a FE ASIC with 128 channels grouped in clusters of 4 channel each). With a link speed of 8xF, 18 bits are available in the FRM channel to encode one or two hits: 1 bit encoded with Hamming in 3 bits is used to specify the number of transmitted hits, while the last available bit is used for parity check. Different possible configurations w.r.t. link speed and frame length have been simulated in order to evaluate their efficiency in the transmission of trigger data: values of the Trigger Transmission Efficiency (TTE) for different values of Link Speed (LS), frame length expressed in clock cycles (NC) and maximum number of transmitted hits (NH) are summarized in Table I. These results have been obtained assuming a Poisson distribution for hits (0.125 hits/clock cycle) and hits generated by one FE circuit in simulations with LS = 8xF and by four FE circuits in simulations with LS = 16xF.
A possible data stream in the Up-Link from the detector is shown in Fig. 12: two FLF (FLP1 and FLP2) interrupt the transmission of a VLF VLP1 that is then regularly completed (e.g: VLP1 = "raw" data generated after the reception of a L1 trigger $\rightarrow$ lbl = time stamp, w1 = 1st hit, w2 = 2nd hit). A second empty variable latency packet (VLP2) follows (e.g.: VLP2 = acknowledge of a command received through the Down-Link).

TABLE IV
TRIGGER TRANSMISSION EFFICIENCY.

LS	NC	NC	TTE
8xF	3	2	96.57%
8xF	5	3	98.53%
16xF	4	7	97.29%
16xF	8	13	98.94%

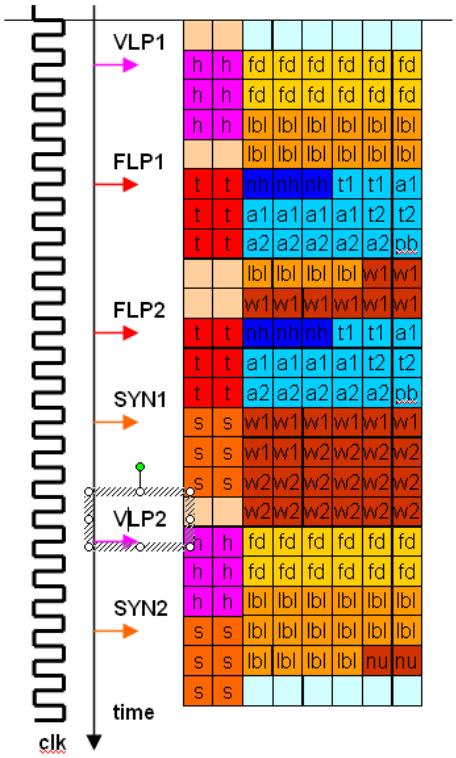


Fig. 12. Possible data stream in the Up-Link (h=frame header, t=trigger, s=synchronization pattern, fd=frame descriptor, lbl=label, w1 and w2=data words).

One FLF employs both the THS and the FRM channel for three cycles of the reference clock, transmitting data (i.e.: hit timing and address) associated to a maximum of two hits. The hits can occur at different instants of the three-clock-cycles window, but a possible third hit cannot be handled and, consequently, it is lost. The transmission of a VLF is stopped to allow the transmission of an incoming FLF and re-started after the completion of the transmission of the FLF. The scheduling strategy implemented for the transmission of FLF leads to a latency equal to three reference clock cycles.
The use of the same channel for triggers, fixed and variable latency frames allowed by the FF-LYNX protocol will bring to a significant reduction of the number of physical links and of the overall material budget that affects the detector performance and it is therefore one of the major concerns in the design of the detectors.
Finally, the flexibility of the protocol with respect to the architecture of the control and readout systems represents an additional strength point, since it is compatible both with “star” and “ring” architectures. A Data Concentrator Module (DCM) can be used in a star topology (see Fig. 13) to merge low speed input data streams from different sources into one high speed output stream.

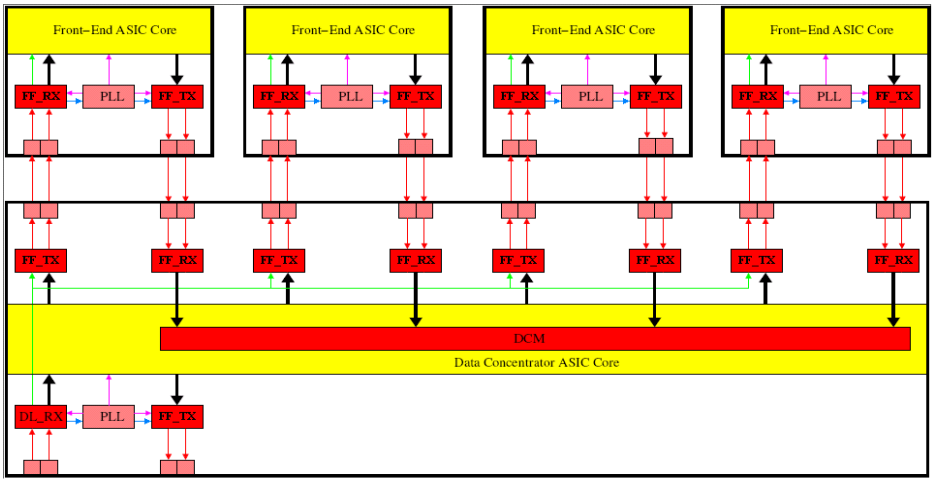


Fig. 13. "Star" architecture of a control and readout system based on FF-LYNX protocol and interfaces.

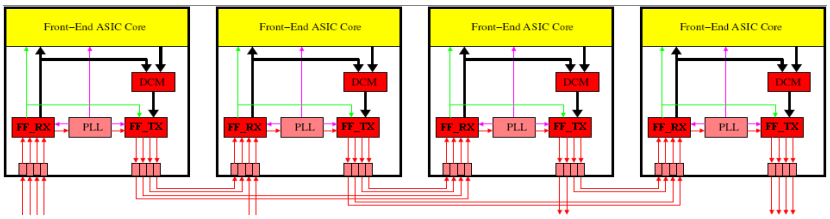


Fig. 14. "Ring" architecture of a control and readout system based on FF-LYNX protocol and interfaces (redundant connections to prevent effects of single component failures are included).

In a ring topology (see Fig. 14) the DCM would merge in each node locally generated data with data received from the previous node. Optional "event building" capabilities can be embedded in the data concentrator module: monitoring data generated by the execution of the same command in different Front-End circuits or "raw" data associated to the same trigger can be merged.

2.5 FPGA-BASED EMULATOR

2.5.1 Emulator system

The functioning of the TX-RX interfaces has been validated through a high-level simulation (ISE) during the first validation phase, and by means of a FPGA-based emulation at the final stage.
The architecture of the FF-LYNX Emulator is depicted in Fig. 15.

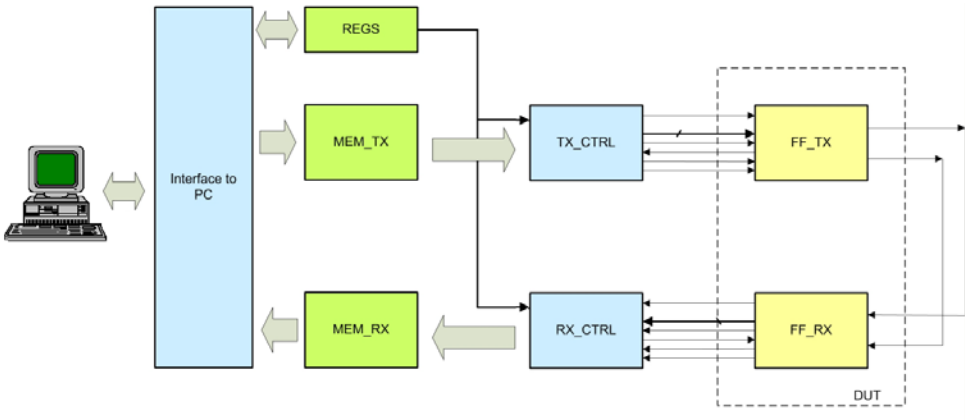


Fig. 15. Conceptual architecture of the FF-LYNX Emulator.

The TX-RX interfaces in the above reported scheme, represent the Device Under Test (DUT). The input signals to the TX interface are provided by the TX Controller (TX_CTRL) that reads test vectors (trigger commands and data packets) stored in a transmitter memory (MEM_TX). An RX Controller (RX_CTRL) reads triggers and data received by the RX interface and writes them into a receiver memory (MEM_RX).
A further comprehension of the emulator functioning is described in Fig. 16. As can be noticed, the TX and RX Controllers are parts of the overall Test Controller, that integrates also TC configuration registers containing test parameters as emulation window duration, number of VLF packets, FLF mode, size of the FLF packets, etc.
The TX controller controls the transmission of FLF packets, trigger or VLF packets at pre-defined clock cycles (TX Time Stamps), whose values are set and stored into a dedicated RAM. The arrival timing of the received triggers and frames is stored in a separate RAM: the contents of the TX-RX Time stamps RAMs are compared to evaluate trigger and the packet latency.

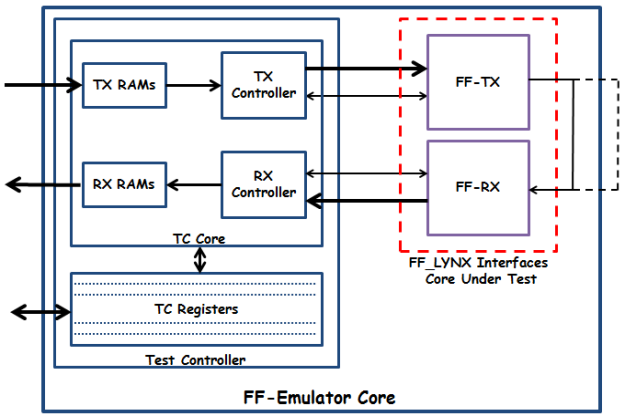


Fig. 16. FF-Emulator core block diagram.

Overall, the RAMs embedeed in the FPGA emulator are:

- VLF_TS (Variable Latency Frame Time Stamp) RAM: two 32x4k memories storing the time stamps (TS) associated to VLF data packets transmitted/received to/from FF-LYNX TX/RX interfaces.
- VLF_LEN (Variable Latency Frame Length) RAM: two 8x4k memories storing the length (number of 16bit words) of the VLF data packets transmitted/received to/from FF-LYNX TX/RX interfaces.
- VLF_DW (Variable Latency Frame Data Word) RAM: two 16x32k memories storing the VLF data packets transmitted/received to/from FF-LYNX TX/RX interfaces.
- TRG_TS (Trigger Time Stamp) RAM: two 32x4k memories storing the time stamps associated to triggers or FLF data packets (when they are enabled) transmitted/received to/from FF-LYNX TX/RX interfaces.
- FLF_DW (Fixed Latency Frame Data Word) RAM: two 8x32k memories storing the FLF data packets (when they are enabled) transmitted/received to/from FF-LYNX TX/RX interfaces.

Test vectors are generated by a software application running on a Personal Computer, and then sent to the FPGA-based emulator through the interface module that deals with data exchange between the PC and the Emulator system using the PCIe 2.0 8x bus. The FPGA-platoform is as Altera Stratix II GX FPGA device (EP2SGX130GF1508) [32] housed on a commercial PCIe board (PLDA XpressGXII board) [33]. The Stratix II GX FPGA provides about 133,000 equivalent Logic Elements (LEs), 7 Mbit Total RAM memory, 8 PLLs, 78 LVDS channels, 63 DSP (multipliers and adders) blocks and 20 Transceiver channels with a data rate from 600 Mbps to 6.375 Gbps. The PLDA FPGA development board has been chosen to guarantee a large bandwidth to perform extensive emulations with high data rates (about 1 Gbps) with an acceptable efficiency in terms of emulation time. This board, thanks to the PCIe 2.0 8x bus, can handle a 3.6 GB/s data rate (effective, full duplex).
The overall emulation procedure is controlled by a C++ Graphical User Interface (GUI), which configures the configuration registers embedded in the FPGA, provides test patterns to the interface and elaborates the performance figures, by comparing the output signals with the input generated.
Three main blocks constitute the software layer: the PLDA drivers to interface the Host-PC with the PCIe PLDA board, the Data Manager managing the emulator operations, and the GUI (Figure 12) that allows to set the emulation parameters and to display emulation results.
The Data Manager module is a container for all the objects providing data to the GUI, the interface modules using the PLDA API, the stimuli generator (StimGen) and figure-of-merit evaluator (Gauge).
The main blocks making up the Data Manager are:

- EmuRun module that acts as the controller for the emulation runs, by instructing the StimGen to produce the stimuli for the run and to store them in a particular memory area, on the base of a list of parameters set by user (data rate, emulation window duration, packet and trigger rate, number of triggers and packets, etc).

- StimGen module that generates the VLF/FLF data packets and the time stamps.
- Gauge block that, according to emulation results, evaluates the Figures of Merit of the emulation run.

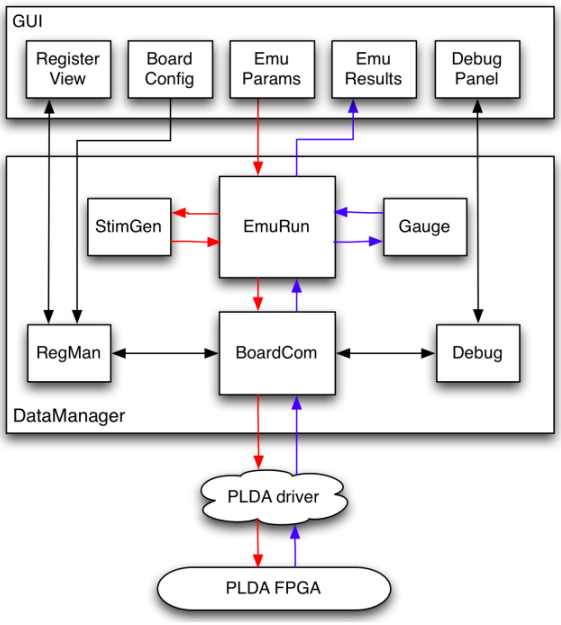


Fig. 17. C++ emulator software block diagram.

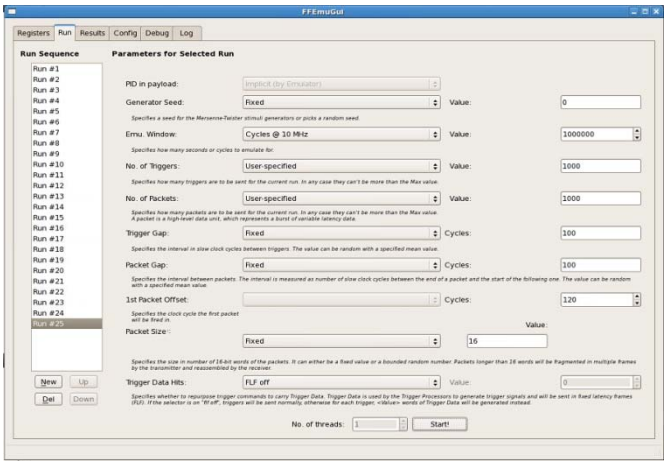


Fig. 18. GUI controlling the emulator functioning.

Summarizing, the overall emulation system is made up by a software layer, running on a host-PC, where an FPGA development board is mounted: the Fig. 19 Illustrates the global system.

Fig. 19. Emulation system.

2.5.2 Functional emulation results

The main figures of merit assessing the performances of the FF-LYNX protocol have been evaluated thanks to extensive emulation runs. One of the main characteristic of the protocol, the packet latency, has been characterized in Fig. 20: its behaviour, by varying the packet size, is reported for TX-RX interfaces implementing the 8xF speed option. It can be noticed that when the packet size exceed the 52 data words there is a sharp increase of the packet latency. This trend is due to packet queuing in the TX buffer of the interface under test.
Fig.21 shows the Packet latency, expressed in clock cycles, as a function of the trigger gap, i.e. the distance, still expressed in clock cycles, between consecutive triggers. Obviously, by increasing the trigger rate, also the packet latency raises. That is because trigger priority is higher than packet frame priority and therefore VLF packets are blocked into buffer for longer time.

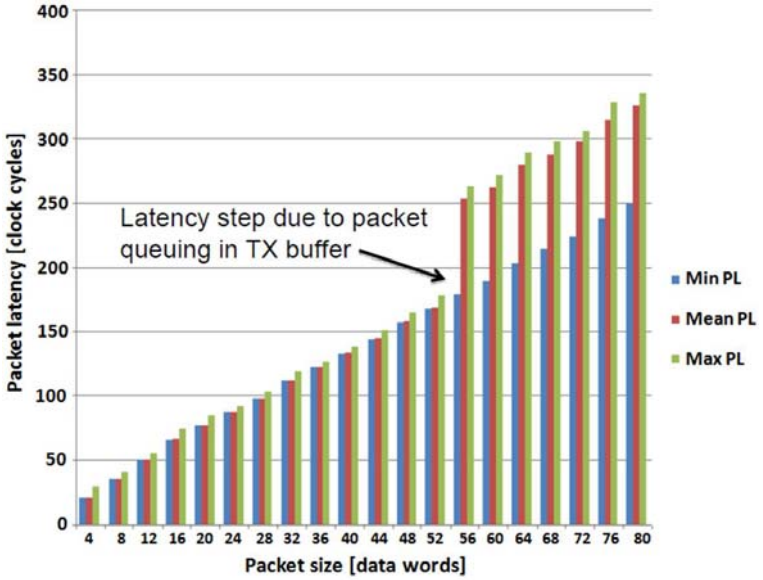


Fig. 20. Emulation tests on TX-RX-8x interfaces: packet latency vs. packet size.

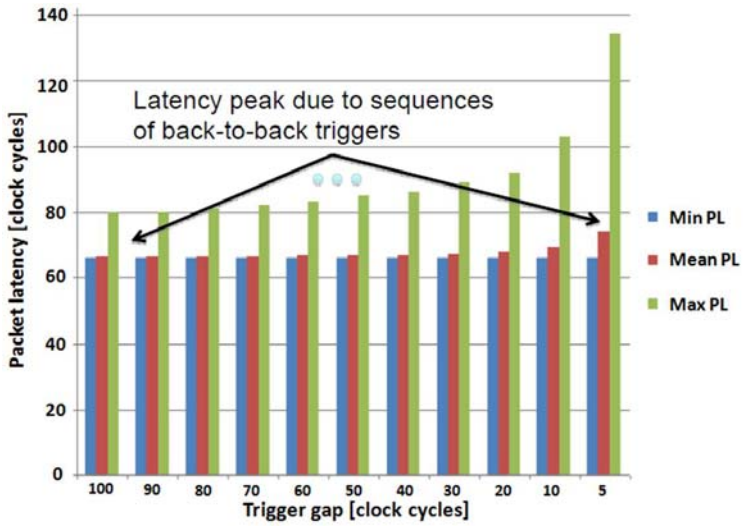


Fig. 21. Emulation tests on TX-RX-8x interfaces: packet latency vs. trigger gap.

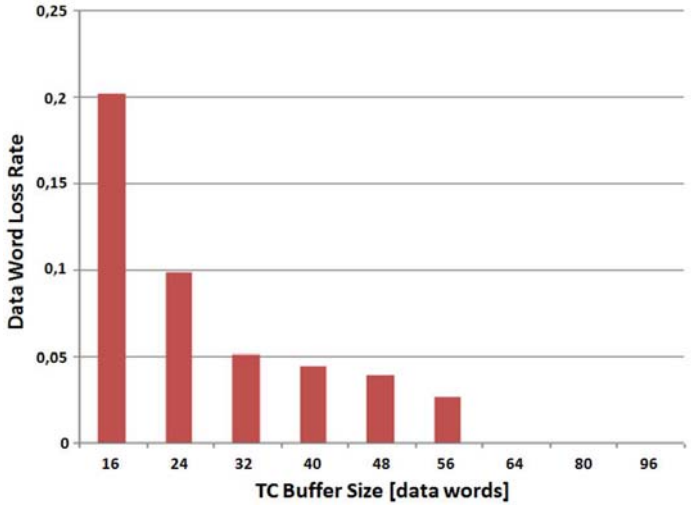


Fig. 22. Emulation tests on TX-RX-8x interfaces:
TC buffer size vs. data word loss rate.

In Fig. 22 the data words loss rate as a function of the TC buffer size is expressed. By increasing the TC buffer size it is possible to decrease data word loss, exploiting a higher data buffering. The rigth trade-off between data loss rate and area occupation has been exploited in the sizing of the buffer depth.
In Fig. 23 an important evidence of the differences between high level simulation and FPGA-based emulation is reported: the packet latency is evaluated as a function of packet gap, that is the distance (in clock cycles) of consecutive packet transmissions.

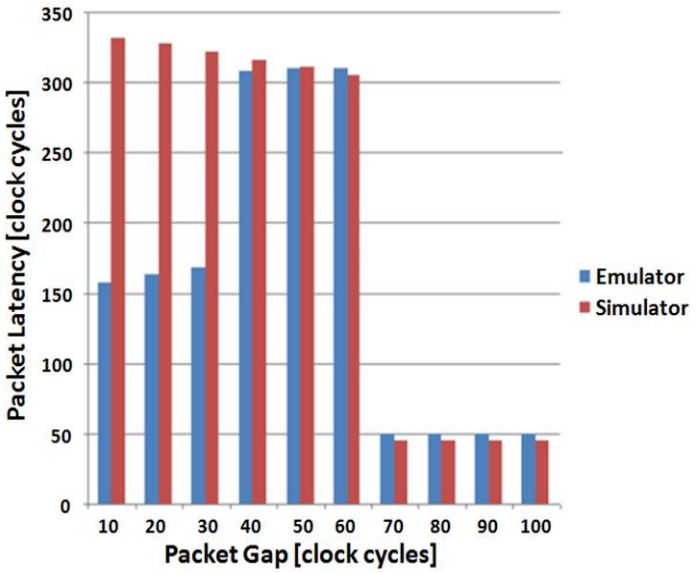


Fig. 23. Comparison between emulation and simulation results: packet latency vs. packet gap.

When packet gap decreases at 30 clock cycles or lower there is a mismatch between simulation and emulation results. That is due to the lack of accuracy in the high-level model as concerns the finiteness of TX buffer: the possible buffer overflow phenomenon cannot be represented in the software simulation w.r.t. the hardware emulation and in this way can be interpred the gap between columns in red and blue colors. Above the 60 clock cycles of packet gap, no overlapping between consecutive packets occurs, therefore the packet latency does not vary.

2.6 TX-R1 INTERFACES AND TEST CHIP DESIGN

2.6.1 FF-LYNX interfaces

The protocol has been implemented in TX and RX interfaces to serial links with two parallel ports to the host devices: a 16-bit parallel port for the data to be encapsulated into VL frames, and a 6-bit parallel port for the FL data.
The very simple handshake mechanism implemented is shown in Fig. 24. When new data (single bit or 16-bit word) is available as an input of the FF-TX interface or as an output of the FF-RX interface, the *data_valid* goes high and the next available data is provided at the next rising edge of the clock. If the *get_data* line remains high (i.e.: input buffers in the FF-TX interface or in the core of the destination device are not full) the data transfer proceeds, otherwise it is paused (if the *get_data* is enabled) as long as the *get_data* line is kept low. The trigger input in the FF-TX is used to start the transmission of a trigger (in the Down-Link) or of a fixed latency frame (in the Up-Link). The same line in the FF-RX interface is used to specify that a trigger or a fixed latency frame has been received.

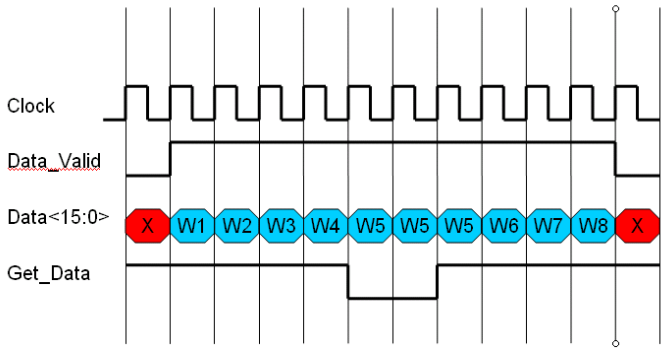


Fig. 24. Handshake on the parallel data port between a FF-TX or FF-RX interface and the core of host circuit.

The FF-LYNX interfaces are currently compatible with “double-wire” electrical links, but in some of future HEP experiments (e.g.: upgrade of CMS End-Cap Muon) encoded onto one serial line will be needed to guarantee communication reliability on high speed (>500Mbps) and long (>1m) physical connections. Long links, where “double-wire” connections are not employable because of skew issues between clock and data lines, can be required to keep power consuming and cooling demanding optical transceivers far away from sensing elements, limiting the impact on material budget. In that perspective, the development of an improved version of the protocol is already foreseen, which guarantees the compatibility of the TX and RX interfaces with “single-wire” links by means of a custom clock/data encoding, similar to the 8b/10b encoding used in most of the commercial standard protocols for serial communications.
The building blocks of the TX and RX interfaces are shown in Fig. 25-26-27 and described below.

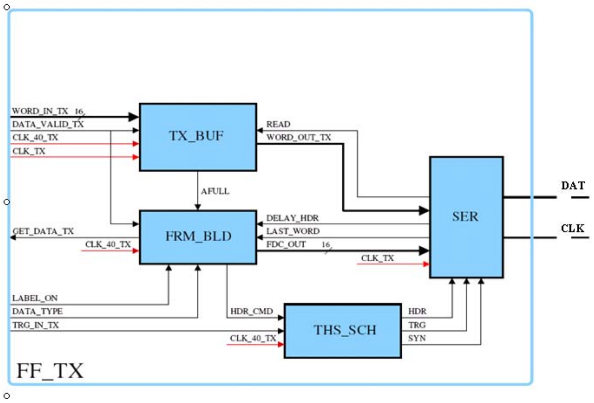


Fig. 25. Architecture of the FF-TX interface.

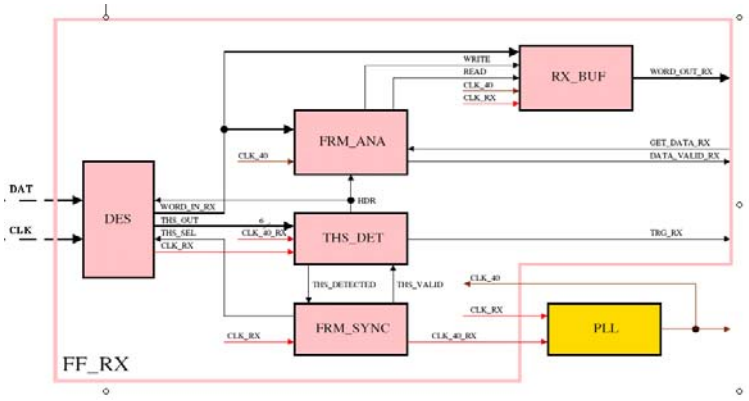


Fig. 26. Architecture of the FF-RX interface.

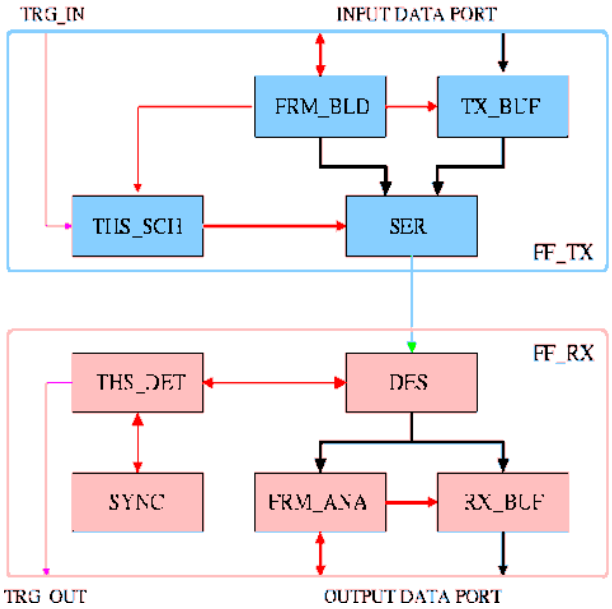


Fig. 27. Architecture of the TX and RX interfaces.

The TX interface includes the following modules:

- FIFO buffers → The TX interface relies on an independent FIFO buffer (TX_BUF) to store the data words to be associated to VL Frames and on a FIFO (FIFO_FLF) embedded in the Frame Builder module for the FL frames. Both the FIFO buffers are managed as circular FIFO structures, implementing a SEC/DED Hamming code.
- Frame Builder (FB) → This module controls the assembly of frames for the transmission of data stored in the FL and VL FIFOs. More in detail, it manages the handshake with the host system to acquire the data to be stored, creating the frames for the transmission of the data and preparing the Frame Descriptor

for each frame. Furthermore, the FRM_BLD controls the flow of data from FL/VL FIFOs to the Serializer during the transmission.

- Triggers, frame Headers, Synchronization patterns Scheduler (THS_SCH) → This block works out the arbitration between triggers (FLF headers) and VLF headers: it receives TRG and HDR commands, respectively from the TRG input port of the TX interface and from the Frame Builder, and passes them to the Serializer organizing their transmission in such a way that overlaps of the THS sequences never occur.
- Serializer (SER) → The Serializer generates the serial output stream by receiving the Frame Descriptor field from the Frame Builder and the frame words from the VL and the FL FIFOs. In addition, the Serializer transmits TRG and HDR sequences into the THS channel, according to the commands received from the THS Scheduler.

The RX interface includes the following modules:

- Deserializer (DES) → This block converts the FF-LYNX serial stream into parallel form, separating the THS channel and the FRM channel and providing the data words to be stored into the RX Buffer.
- Triggers, Frame Headers, Synchronization Patterns Detector (THS_DET) → The THS_DET block detects the sequences of triggers, headers and synchronization patterns in the THS channel.
- Synchronizer (SYNC) → This module generates the reference clock synchronized on the THS channel of the received serial stream: the synchronization is obtained according to the information coming from the THS Detector about the detected THS sequences.
- Frame Analyzer (FRM_ANA) → Its main functions are the control of the reception of data frames, their storing into the RX Buffer and the delivery of stored data to the receiver host.
- FIFO buffers → An independent FIFO buffer (RX_BUF) is used to store the received data words associated to VL frames and a FIFO embedded in the Frame Analyzer handles FL frames. These FIFO buffers, as the ones in the TX interface, are managed as circular FIFO structures, and make use of a SEC/DED Hamming code.

The TX and RX interfaces have been developed in the three different speed options 4xF, 8xF and 16xF and integrated into the test-chip FF-TC1, that will be described in the following paraghraph.
Table V shows the power and area occupation of the modules building up the TX-16x interface when realized in the 130 nm CMOS IBM technology. The most power and area demanding module is the Serializer, since it is the only one working with the high frequency transmission clock. The area occupied by the FIFO storing the FL frames is also sizeable, but smaller than the VL frame FIFO, developed as an external module, since the radiation hardening techniques applied to the two buffers are different, as well as their depth and width.

TABLE V

FF-TC1: TX-16X INTERFACE

POWER, AREA AND GATES OCCUPATION SUMMARY

Modules	# Gates	Area (μm^2)	Power (µW)
SER	1539	19713	2500
FIFO_FLF	656	11161	580
FRM_BLD	388	5274	257
THS_SCH	95	1434	59
Others	183	2579	265

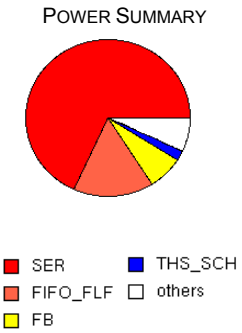
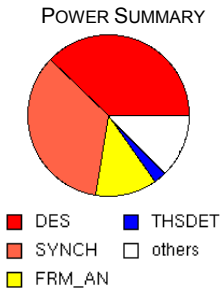


TABLE VI

FF-TC1: RX-16X INTERFACE

POWER, AREA AND GATES OCCUPATION SUMMARY

Modules	# Gates	Area (μm^2)	Power (µW)
DES	1540	22612	1523
SYNCH	1469	20315	1394
FRM_AN	440	5662	498
THS_DET	78	934	44
Others	307	4128	507



In Table VI, showing the power consumption and area occupation of the RX-16x interface when realized in the 130 nm CMOS IBM technology, it can be noticed that the Deserializer and the Synchronizer are the two most power demanding blocks, since they are clocked by the high frequency transmission clock.

2.6.2 Test chip architecture

The test-chip FF-TC1 implementing FF-LYNX IP-Cores has been designed in the IBM 130nm CMOS technology, integrating the Transmitter and Receiver interfaces, designed in three different speed options, 4xF, 8xF and 16xF (F = reference clock frequency), as well as different rad-hard FIFOs. The goal of this activity is the implementation of the protocol as Intellectual Property (IP) cores, made available to the designer of the integrated circuits for the HEP experiments.
The test-chip FF-TC1 has been implemented in the commercial process IBM 130nm CMOS8RF, since it represents a good trade-off between cost and performance and is the most used in the design of the Integrated Circuits (IC) prototypes for the LHC upgrades. The choice of the technology is a key element for an IC operating in HEP experiments: the 130nm CMOS process guarantees satisfactory intrinsic radiation hardness against TID effects typical of the low-dose-rate radiation level foreseen in the SLHC environment [3,4].

All the modules embedded in the FF-TC1 ASIC have been hardened against radiation effects, while managing the trade-off between radiation hardness and area. The test-chip (Fig. 28) is composed by TX and RX interfaces, a Built-In Test Module to control the testing phase, an I2C interface for the control and monitoring of the test-chip and, finally, rad-tolerant FIFO cores used as data buffers in transmission and in reception. The six FIFOs embedded in FF-TC1 (64 words each) implement the same radiation hardening techniques. As can be noticed in the layout of the FF-TC1 ASIC shown in Fig.6, FIFOs represent the largest components of the core, mainly because of the high level of radiation hardness implemented in these modules. The three TX interfaces (4xF, 8xF and 16xF) are interfaced to a FIFO (DW_FIFO) that stores the 16-bit data words encoded by a SEC/DED Hamming code into 22 bits and to an 18-bit FIFO (FD_FIFO) that memorizes the 12-bit frame descriptors, encoded by the same technique. An equivalent pair of FIFOs are used by the RX interfaces at the three speed options. These data buffers provide the FF-LYNX protocol with an innovative data flow control feature, not present in the protocols currently employed in HEP experiments. Data received through the link can be temporarily stored within the RX interface, so that data losses are avoided when the host device cannot accept the transfer temporarily. Similarly low priority data can be buffered in transmission when high priority data, embedded in FL frames, keep the link busy.
The Built-In Test Module has been introduced to support the test of the TX and RX interfaces in a chain loop configuration,

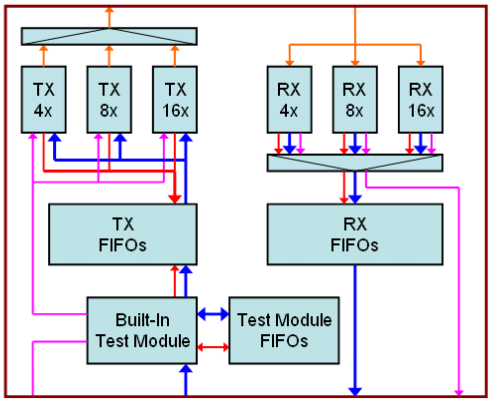


Fig. 28. Architecture of the FF-TC1 circuit: the three speed versions of the TX and RX interfaces, as well as the Test Module can be noticed. In addition, the FIFOs related to each unit are shown.

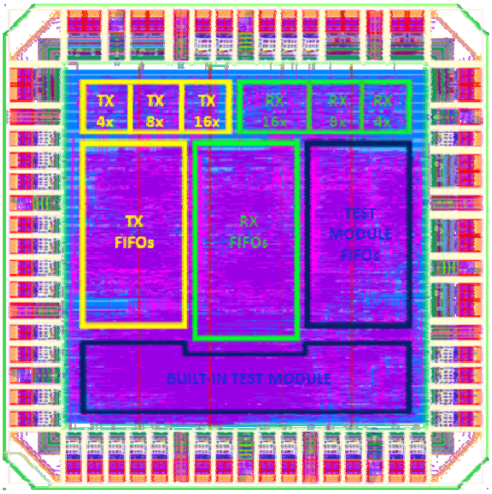


Fig. 29. Layout of the FF-TC1 test-chip: to be pointed out the small area of the TX and RX interfaces

by generating the test patterns and the control signals (Trigger and Data-Valid) to the TX interfaces.

In this test configuration the bi-directional parallel port available in the FF-TC1 ASIC is used as output port to have access to the outputs of the RX interfaces. The TX inputs are locally generated in the Built-In-Test module when a one–clock-cycle pulse is detected on the TX_TRG (trigger or start of a FLF) or on the TX_DAV (start of a VLF) input pins. More in detail, the main task of this module is to generate and present data words on the parallel ports of the TX interface, both for VL and FL frames; in order to accomplish that, three Pseudo Random Generators (PRGs) have been integrated into the Test Module. The first generates the lengths of the VL frames, that is the number of data words making up the payload of each frame. The second, according to the length defined by the previous PRG, provides the data words to the 16-bit parallel port of the TX interface. The last PRG supplies data to be transmitted as FL frames, whose length is not variable in order to guarantee a fixed and low latency in the transmission. Two FIFO buffers store the VL data words and lengths generated by the PRGs, supporting thus the testing phase.

The FF-TC1 has an overall area of 2.0 x 2.0 mm2, with a pad area of 1.865 mm2, and 2.135 mm2 as core area. As can be noticed in Fig. 6, the interfaces are placed in the upper part, close to the LVDS transmitter and receiver pads that are multiplexed between the different speed option interfaces. The FIFOs are located between the TX-RX interfaces and the Built-In Test Module, in order to optimize the area occupation and to reduce the length of the connecting metals, simplifying the timing closure of the design. The density placement set for the TX-RX interfaces is lower than for the other modules, since there are some parts (Serializer, De-serializer) working with high frequency: in this way the Place & Route tool can reach the timing closure easily, by taking advantage of wider area to add buffers and move the cells in the critical paths.The current absorbed by the core, with a reference frequency set to 10 MHz and a supply voltage of 1.5 V, is 4.5 mA, with a

power absorption of 6.8 mW. The I/O current absorption is 12.5 V @ 2.5 V, with 31.2 mW of power consumption.

2.6.3 Radiation hardening techniques

The increase of luminosity foreseen in the upgrade of the LHC [7], will make radiation induced events like SEE an issue that could compromise the proper behavior of the interfaces integrated in FF-TC1. In particular, among the SEE, the SET, spurious pulses generated in combinatorial logic, which can propagate through the overall system, might represent a potential risk already in digital ICs working at few hundreds of MHz. Indeed, the width of the transient pulses that are likely to occur in the circuit nodes is not negligible compared to the clock periods, especially for the 8xF and 16xF interfaces [12,13]. In medical physics applications, gamma rays and heavy ions represent examples of radiation particles commonly present in the operating environment. By taking into account the wide range of potential applications of the proposed interfaces, the radiation hardening techniques adopted have not been focused on specific radiation effects.

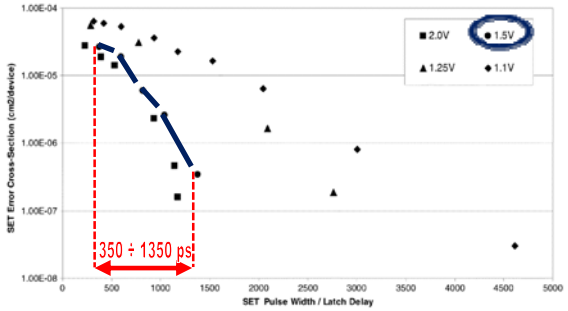


Fig. 30. SET cross-section versus pulse width for the IBM 130 nm technology, by varying the supply voltage. A significant cross section on the range 350 ÷ 1350 ps can be highlighted in the case study.

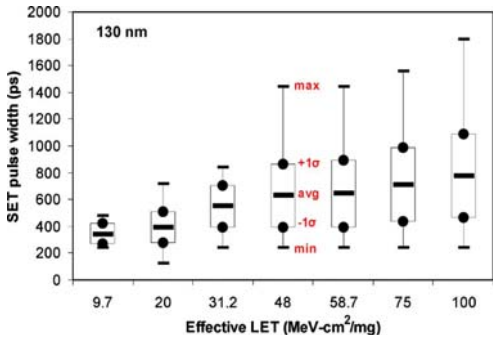


Fig. 31. Box plot indicating the average, standard deviation, minimum and maximum SET pulse width as a function of LET for the IBM 130 nm CMOS process [13].

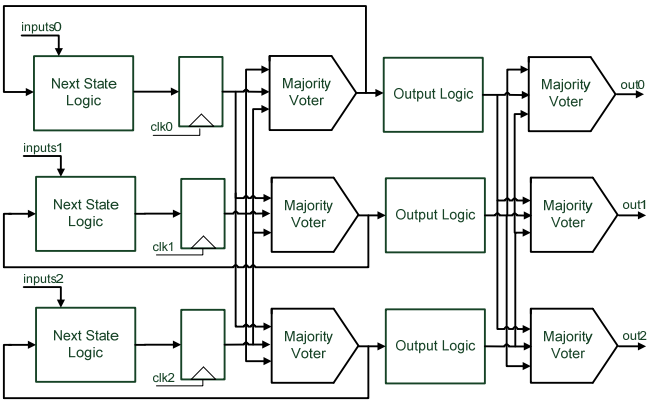


Fig. 32. Moore Finite-State Machine protected by Triple Modular Redundancy.

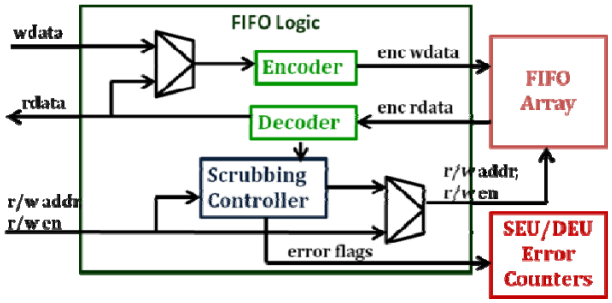


Fig. 33. Block diagram of the rad-hard FIFO embedded in FF-TC1.

The strategy employed in the radiation hardening of the FF-TC1 modules is the following: to maximize the hardness of all the modules that support the test and characterization of the FF-LYNX interfaces, like the Built-In Test Module, the I2C interface and the configuration and status registers, whereas a trade-off between radiation hardness and area overhead has been managed for the TX and RX interfaces, since area and power dissipation represent an important figure of merit of these IP cores.

The Triple Modular Redundancy (TMR) is a technique commonly used to protect sequential logic from Single Event Upset (SEU) and SET effects. It is based on three copies of the module where the upset could occur, with the introduction of a majority voter to select the correct value among the ones generated by the three copies, so that the failure signal can be ignored [14,16]. The TMR can be applied at different levels, considering the architecture of a Finite State Machine (FSM).

A first level of radiation hardening is obtained by replicating the state registers and applying a majority voter to reject the possible upset in one of the three copies. This solution provides a protection against SEU occurring in the state registers, without preventing a failure due to a SET in the combinatorial logic. The second approach requires three copies of both the next state logic and the output logic that is basically a redundancy of the overall FSM. A majority voter selects the correct value on the output of the FSM, protecting also against SET coming up in the combinatorial logic. Yet, a transient pulse could take place in the majority voter,

being transmitted on the output of the FSM. In order to avoid this possibility, the majority voter can be replicated as well (Fig. 32). Following this approach, all the signals in the module have three copies, with a significant increase in the overall area that is tripled as well. This solution allows a protection against SEU occurring in the overall system, as well as against SET occurring in the input signals of the FSM machines, with the drawback of an increase of the area sensitive to SEEs since a radiation event becomes more likely to happen in a larger circuit. In order to keep the area of the TX-RX interface small, the first TMR option has been adopted, while the third one has been chosen for the Built-In Test Module. Precisely, the most critical information, such as configuration and status registers, have been hardened also against Double Event Upsets (DEUs), that are two bit flips in the memory cells making up a register. That has required the adoption of the Multi Modular Redundancy, by instantiating five copies of the registers to protect.
The radiation hardening technique applied to the FIFO supporting the TX and RX interfaces, as well as the Test Module, is shown in Fig. 33. The SEC/DED Hamming Shortened Encoding [25] has been employed to correct single bit flips in each data word and to detect DEUs. By adding 6 parity-check bits on each data word and frame descriptor, the minimum distance between encoded data has become four bits, justifying therefore the SEC/DED property of the encoding technique applied. The Encoder and the Decoder, located in the FIFO Logic block, provide the encoding of the data stored in the FIFO Array. The encoding of the data, besides the related logic, has considerably increased the area of these modules, as can be noticed in Table VII.
The Scrubbing Controller, a module that makes periodic reading and correction of SEU in FIFO data, represents an additional feature. In fact, based on read/write external access, it makes a cyclic correction of the data words corrupted by a single bit flip, by decoding each data word and encoding it back into the FIFO array.

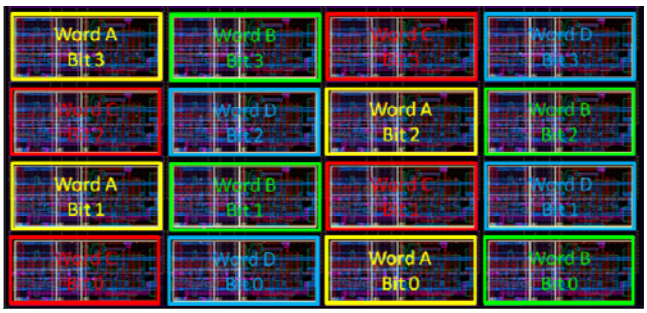


Fig. 34. Spatial interleaving of the storage elements in the FIFO array, foreseen in the upgrade of the radiation hardened module.

TABLE VII
FF-TC1 AREA AND GATES OCCUPATION SUMMARY

Blocks	# Gates	Area (μm^2)
TX 4x	2136	35845
TX 8x	2400	46664
TX 16x	2945	58594
TX FIFO	13769	299382
RX 4x	2201	38478
RX 8x	2790	57107
RX 16x	3957	82508
RX FIFO	15250	299382

The mechanism allows the scrub of the array even when the FIFO is read/written from the external modules, by executing the corrections in the memory area not accessed. Moreover, several radiation-monitoring features have been introduced in FF-TC1, in order to evaluate the impact of SEE on the FF-LYNX interfaces performance. SEU/DEU error counters permit the measurement of the occurrence of these events in each module of the test-chip. For instance, the FIFO has error counters to measure SEU/DEU detected in the stored data words. This feature will help to trace the guidelines in the improvement of the radiation hardening of digital IC realized with the IBM 130 nm CMOS technology. As an example, the occurrence of DEUs in storage elements will be a key element in identifying the most efficient radiation hardening techniques: indeed, it would not be worthy of the area overhead required by the protection against double bit flip, if they rarely happen. In addition, since SETs could represent an important issue in this application, an indirect method to estimate their frequency has been foreseen. SETs are spurious pulses that can propagate to a sequential cell and undergo capture as a soft error if the pulse fall exactly at the clock edge and its width meets the sequential cell timing requirement. It looks obvious that it is more likely to happen by increasing the clock frequency and, more accurately, the latching probability of a SET is proportional to the clock frequency, while the SEU do not depend on this parameter.

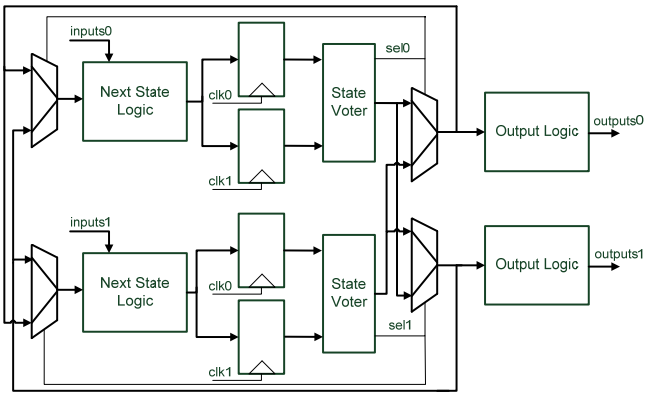


Fig.35. Innovative architecture to protect the Finite State Machines against SEE, SEU and DEU.

Therefore, by repeating the SEU counting with different clock frequencies, the actual impact of SET is extracted. Hereafter some ideas considered for possible future improvements in the radiation hardening are reported. Fig. 34 shows the spatial interleaving of the storage cells that could be introduced in the FIFO array: in this way the possibility that a particle hit determines a double bit flip, that can be detected without correction, is reduced since the bit related to the same data word are not contiguous.

The scheme shown in Fig.10 is an upgrade of the Duplication with Self Checking technique proposed in [16] to protect FSM against SEE. The One-Hot strategy is used for the state encoding, so that the State Voter can reject a single bit flip since it drives to an unused state. Each State Voter of the two branches carries the correct state on its output, as long as at least one of the states is not corrupted. The architecture proposed is hardened against SET in the combinatorial logic as in [11], thanks to the duplication of the FSM. It also adds the protection against DEUs. If there is a single bit flip per branch, the State Voters select the correct states that are driven to the next state and output logic. If two bit flips occur in the same part of the FSM, one per state register, the State Voter cannot select the correct state since both are unused states. In this case, it pulls up the sel# signal (sel# stands for sel0/sel1 if the DEU occurs in the upper/lower branch of the FSM) and the multiplexers select the state coming from the other branch. The sel# signal is pulled up also when a DEU happen in one state register, potentially driving the state to a valid one (if one of the two bit flips hits the One-Hot bit). The State Voter cannot detect which is the wrong state, but it points out the inconsistency between the couple of states, by pulling the sel# signal up. Once again, the multiplexers take the correct state from the other branch of the FSM.

2.7 Test Chip Characterization

2.7.1 Test-bed structure

The FF-TC1 test-bed has been developed to verify the correct behavior of the Devices Under Test (DUT) and to characterize the circuit performance during the functional test and the irradiation test. Its architecture has been conceived by modifying the FPGA-based emulator.

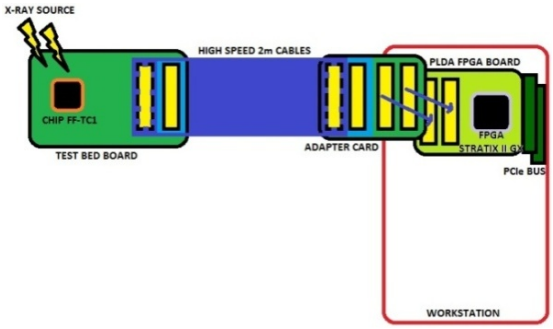


Fig. 36. Scheme representing the Total Dose Irradiation test setup.

Fig. 37. Test-bed employed in the characterization of the test-chip FF-TC1.

Its building blocks are shown in Figs. 36 and 37 and are listed below:

- High efficiency WorkStation: it runs the C++ based Graphic User Interface (GUI) that manages the entire test procedure and the software that generates the input stimuli for the TX interfaces and compares the outputs from the RX interfaces with the expected values.

- PCI-express (PCI-e) development board (PLDA XpressGXII): it houses an Altera Stratix II GX FPGA where the test-bed control logic is implemented.
- Custom Test Board (TB): it houses a socket for the DUT or the DUT directly soldered on board in case of irradiation tests.
- Custom Adapter Card (AC): it lets to interface the FPGA development board to the TB.
- Two high bandwidth cables (SAMTEC): they connect the AC to the TB (one cable with differential lines is used for LVDS clock and serial data, one cable with single-ended lines for the control signals and for the parallel port).

The main functional blocks of the test-bed control logic are the PLDA IP-core with the PCI-e interface that handles the communications between the host PC and the FPGA, the user-defined "application layer" module including the Test Controller (TC) and the "glue logic" that interfaces the PLDA PCI-e core to the "application layer" module. The TC contains two Time Stamp (TS) RAMs (4k x 32bits) that store the timing (clock cycle) of the input trigger and frames. A counter in the TX Controller (TXC) is enabled when the test is started and triggers or frame are transmitted to the TX interface when the counter output is equal to the value contained in the currently pointed RAM location. PRGs generate the test data vectors (VLF length and data words and FLF data words).
TX and RX FF-LYNX interfaces are used to communicate with the interface prototype embedded in the DUT. An RX Controller (RXC) stores data received from the RX interface. Four different test modes have been defined and are shown in Fig. 38, where the different color lines indicate the signal paths in the different modes:

- FF-TC1-TX Test Mode #1 → The TXC in the FPGA handles the test and uses its PRGs to generate test vectors (VL and FL frames) to be transmitted to the TX interface in the FF-TC1 whose serial output drives the FPGA RX interface. The received data are stored in the RX RAMs by the FPGA RXC.
- FF-TC1-TX Test Mode #2 → The TXC embedded in the FF-TC1 ASIC manages the test and operates its PRGs to generate test vectors for the TX interface in the FF-TC1 when triggers or frame start pulses are received from the FPGA TXC. The serial output of the TX interface drives the FPGA RX interface and received data are stored on RX RAMs by the FPGA RXC.
- FF-TC1-RX Test Mode → The TXC in the FPGA handles the test and uses its PRGs to generate test data vectors to send to the TX interface in the FPGA whose serial output drives the RX interface in the FF-TC1. Received data are sent to the Test Controller through the parallel port and stored in RX RAMs by the RXC.
- FF-TC1-TX/RX Test Mode → The TXC embedded in the FF-TC1 manages the test and operates its PRGs to generate test data vectors for the TX interface in the FF-TC1 when triggers or frame start pulses are received from the FPGA TXC. The output of the FF-TC1 TX interface drives the RX interface in the FF-TC1. Received data are sent to the Test Controller through the parallel port and stored in RX RAMs by the RXC.

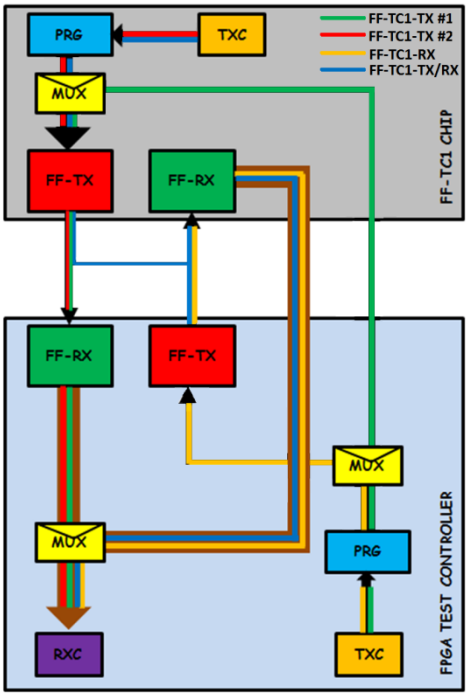


Fig. 38. Different test configurations allowed by the flexible test setup, detailing the modules involved in the test of the TX and RX interfaces on the chip.

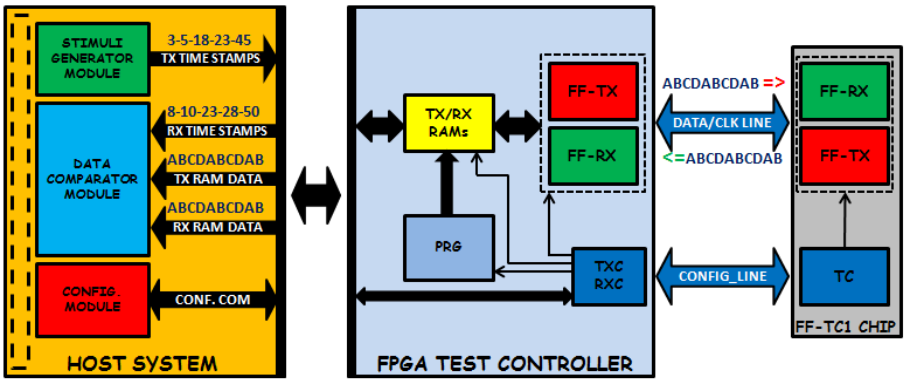


Fig. 39. Block diagram showing the modules embedded in each component of the overall test-bed, highlighting the data streams in the testing phase.

A block diagram of the test system is shown in Fig. 39. The test starts with the configuration of the Test Controller and of the DUT in order to select the test mode and to set the operating conditions (e.g.: the speed of the interfaces, the number of triggers and frames in each test run, the length of the FL frames). The stimuli generation software produces the time stamps of the triggers and of the frames according to the parameters specified in the GUI (e.g.: mean and standard deviation of trigger and frame rate and frame size). Time stamps are then

downloaded in the TS TX RAMs and the test run is started. When the test is over (i.e.: all the trigger and frames have been transmitted), the TX and RX Data RAMs and the RX TS RAMs are read and data are sent to host system where a data comparator software evaluates trigger and frame latencies from data from TS RAMs and verifies the matching between data in the TX and in the RX FRM RAMs and generates Figures of Merit (FoM) as Trigger Loss Rate, Frame Loss Rate or mean value of the VLF latency in order to estimate the efficiency of the links handled by the FF-TC1 interfaces.

2.7.2 Total dose irradiation test setup and procedure

After the functional test phase, an irradiation test has been planned in order to verify the TID hardness of the TX-RX interfaces embedded in the FF-TC1 ASIC. For this purpose, X-rays have been chosen as radiation source, because these elements are present in the future working environment where the interfaces could operate.

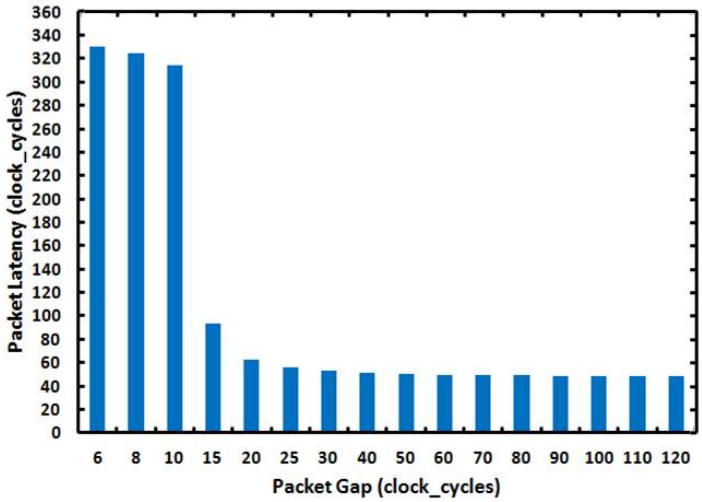


Fig. 40. Packet latency vs. packet gap (8xF, packet size = 6 data words), obtained from the functional test on FF-TC1: to be noticed the step between 10 and 15 clock cycles due to packet queuing in TX buffer.

This test has been conducted at CERN where, in the X-rays facility consisting in a SEIFERT RP149 X-rays generator, the following configuration has been set:

- Anodic Target: Molybdenum (19keV photon energy);
- Beam to chip distance: 1cm;
- Power supply voltage: 40kV;
- Tube current: 6-28-40mA (to change dose rate).

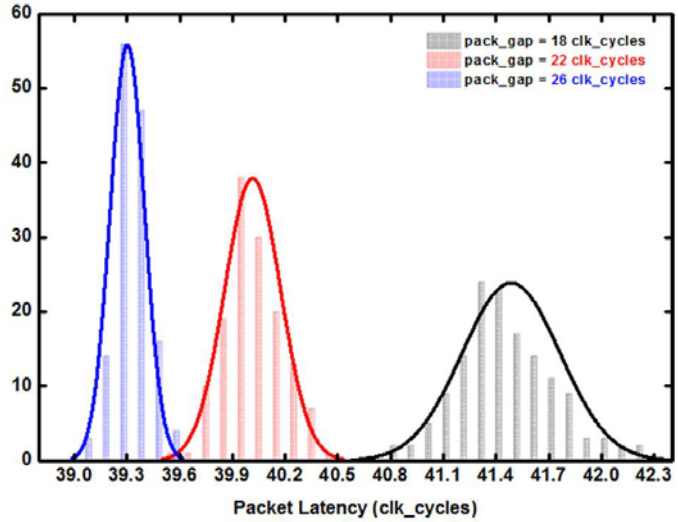


Fig. 41. Packet latency distribution (8xF, packet size = 4), by varying the mean value of the packet gap among 18-22-26 clock cycles, with the transmission of almost 700000 packets: by increasing the packet gap the occurrence of an overlap between following packets is reduced, narrowing the distribution around the average packet latency and decreasing its value.

TABLE VIII.

FF-TC1TID IRRADIATION TEST SUMMARY

Increment ($krad(SiO_2)$)	TID ($krad(SiO_2)$)	Dose Rate ($krad(SiO_2)$/min)	Anneal. Time (min)
10.00	10.00	6.70	25
40.00	50.00	6.70	10
50.00	100.00	6.70	10
400.00	500.00	6.70	10
500.00	1000.00	6.70	90

Increment ($krad(SiO_2)$)	TID ($krad(SiO_2)$)	Dose Rate ($krad(SiO_2)$/min)	Anneal. Time (min)
500.00	500.00	30.24	150
500.00	1000.00	30.24	10
4000.00	5000.00	30.24	10
5000.00	10000.00	30.24	20
30000.00	40000.00	43.08	180

The irradiation system has been calibrated by following the graphs [27] provided by CERN X-ray facility staff, which have allowed to define the dose rate by setting tube current, power supply voltage and distance between collimator and DUT. The test-bed system has been positioned outside the irradiation chamber apart the test board with the DUT that has been placed under the beam as shown in Fig. 42. The irradiation procedure has been defined on the base of [18], consisting in five Total Dose steps to reach, chosen with logarithmic increment as can be noticed in Table IV.

2.7.3 Functional characterization test

In order to test and characterize the FF-TC1 interfaces several tests have been performed. In Fig. 40 is reported a measurement of the variation of mean packet latency with the packet gap, considering a packet size of 6 data words. As previously described, the packet latency decreases when the packet gap increases, in particular there is a sharp decreasing when packet gap is higher than ten clock cycles because packets are less buffered on the TX interface buffer (as highlighted in the FPGA-emulation phase).
A statistical analysis of the packet latency for the 8xF interface on a sample of 150 test runs is shown in Fig. 41, where a Gaussian fitting curve is drawn for three fixed values of packet gap (18, 22 and 26 clock cycles). This figure underlines a decreasing of the mean packet latency value and of its variance in agreement with the expected behavior of the interface. At the beginning an irradiation test up to 1 Mrad(SiO2) at 6.704 krad(SiO2)/min has been performed on a first FF-TC1 sample chip as preliminary validation test. Subsequently, by using another FF-TC1 sample chip, the maximum Total Dose has been set to 40 Mrad(SiO2), since this TID level is in the LHC operative zone where the FF-TC1 chip has been designed to work. The different values of dose rates have been chosen step by step during the test, in order to evaluate chip response at both low dose rate and high dose rate. After every step a room temperature annealing phase has been conducted.

Fig. 42. Test setup used during the irradiation test, performed at the CERN 10-keV X-ray facility.

The FF-TC1 chip has been configured in standby mode during the irradiation time. For all test time (during and after irradiation) the chip absorbed current has been monitored and only after the end of a single irradiation step an automatic loop test has started from remote GUI. This automatic test consists in executing all four test modes cyclically within a settable time window of max 30 min while logging results on text file. In the course of these runs, no trigger or packet errors have been detected proving therefore the robustness of the test-chip against TID effects. The current absorption level (as seen in Fig. 43) after the last annealing phase is similar to the one measured before the irradiation, a sign that no destructive events have occurred.
In Fig. 43 the variation of total absorption current with TID during irradiation phase is shown; in every step there is an absorption current peak whose value decreases when TID step increases.

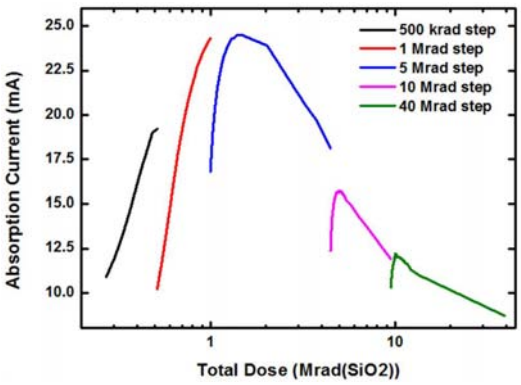


Fig. 43. Overall current absorbed with respect to TID during the irradiation phase (1.5 V core supply voltage, 2.5 V I/O supply voltage)

3 AUTOMOTIVE APPLICATION: DESIGN AND VALIDATION OF AN INTELLIGENT POWER SWITCH

3.1 Intelligent Power Switches

Intelligent Power Switches are smart power integrated circuits of wide-spread utilization in many fields of application such as industrial automation, automotive and consumer electronics [44], [48].
When designing an IPS, several performance requirements have to be targeted. A key specification for IPS is the ability to drive a load with high current at high efficiency, reducing the circuit complexity and improving the system reliability. A further performance requirement is the possibility to be interfaced directly with microcontrollers, DSP or other digital programmable devices, being like an appendix of intelligence of these control units inside the power output stages. Thanks to the shortening of design cycle times and improvement of system reliability, the employment of this kind of driver integrated circuits offers a remarkable cost reduction, especially in automotive where ICs development time is rather high. Indeed, the independence of such smart devices from the ECU and the wiring characteristics, allows to adapt the same IPS design to different vehicle platforms.
Yet, the distinctive quality of IPS is the flexibility, since they have to be designed in order to drive a large class of power demanding loads efficiently, in widely variable operating conditions.
Power loads such as incandescent lamps and relay coils have a distinguishing feature in common: during the turn-on phase they drain a current from the circuit driver much higher than during the steady-state [45], [49]–[54]. For example Fig. 1 presents experimental measurement in a real lighting automotive circuitry, showing the current drained by a 3 W incandescent lamp (*I_Lamp*) when a 12 V voltage step is applied, as captured from an oscilloscope screen. The voltage drop on the lamp (*V_Lamp*) has been also acquired and the resistance of the filament

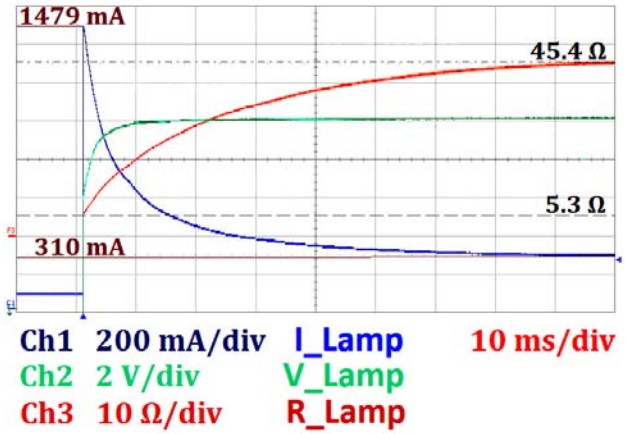
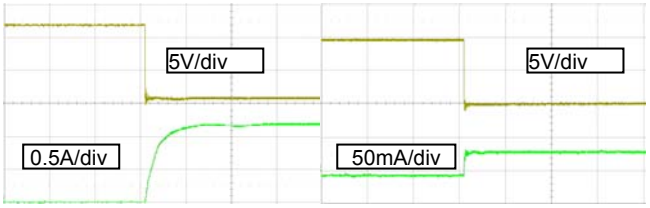


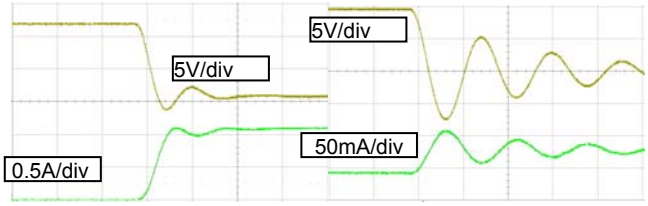
Fig. 44. Experimental measurement showing the current drained by a 3 W incandescent lamp (I_Lamp) when a 12 V voltage step is applied.
The lamp current is measured by means of a current probe.

evaluated (*R_Lamp*). In Fig.1 the current peak value is about five times the rated current due to the increase in the resistance from 5.3 Ω to 45.4 Ω. Indeed, the filament resistance can be considered roughly proportional to its absolute temperature, that starts from a value equal to about the room temperature (T_0 = 27 °C), reaching values up to hundred times higher (2250 ÷ 2750 °C) during the incandescence.
A such high in-rush current causes several problems both to the load and the integrated circuit driver. Indeed each switch is a thermal shock for the load: in an incandescent lamp, for instance, it leads to a deterioration of the structure of the filament over time. Even if the lamp is designed to withstand a number of switching cycles corresponding to the lifetime of the vehicle, it is better to decrease the stress on it, improving consequently the reliability of the corresponding function.
In addition, problems due to power dissipation have to be taken into account for the driver too, as well as possible electromigration phenomena in the metal inter-connections of the integrated circuit.
Moreover, EMI issues and a large voltage drop in the supply power net are additional consequences of the peculiar transient behavior of the class of loads described above. A similar behavior is shown by electromechanical devices (electrovalves, electric motors), largely used in automotive, increasing the value of IPS in this specific field of application [18], [28].
The EMI problems depend on environmental and parasitic components that are difficult to predict and simulate. An additional complication to the design is the ability of driving both incandescent lamp bulb and LED: while bulbs are easily modeled as linear PTC (Positive Temperature Coefficient) resistors, and are less sensitive to parasitic components, a LED is a special diode and follows the Shockley exponential I-V law. A very small fluctuation on the voltage across the LED can generate a very high variation on its current affecting, as proved in [3], both efficiency and life time and creating lighting disturbs. This behavior can generate ringing and high current spikes if the LED is not properly driven. By the same token, a bulb-designed driver, as shown in [10-12], cannot be directly used to drive efficiently LEDs. This is particularly true when the LED and the driver are separated by a few meter cable as in automotive connections. In this case the wiring parasitics can generate ringing and EMI.
A comparison based on experimental measurements, between a 2W bulb lamp and a 0.1W LED turn-on transient with very short wire (about 10 cm long) and with very long wire (about 3 m long) is shown respectively in **Figs. 1 and 2**. A simple relay is used as switch to highlight the different behavior of those loads. Those pictures show the necessity of using a well-designed driver for LEDs, to avoid unwanted effects due to wiring parasitics. In fact, the behavior of the current in the bulb does not change significantly with the wire length, see Figs. 1a and 2a, while the transient of the current in the LED shows significant differences, see Figs. 1b and 2b.



(a) Time, 2 μs/div (b) Time, 2 μs/div

Fig. 45. Bulb (a) and LED (b) behavior with 10 cm long connection cable without any kind of current/voltage control.



(a) Time, 2 μs/div (b) Time, 2 μs/div

Fig. 46. Bulb (a) and LED (b) behavior with 3 m long connection cable without any kind of current/voltage control.

IPS are usually connected directly to the battery and to the external world, being therefore subject to a variety of stresses that are difficult to foresee as short circuits, load disconnects, high voltage and current transients, reverse polarity of supply voltage. The above mentioned undesired effects of wiring parasitics have to be considered, such as ringing and consequent overshoots and undershoots, with the risk of unleashing latch-up phenomenon if output goes under ground potential.
It has to be considered that a wire from 2 to 3 meters long (usual length for under-hood electronic equipment) represents an inductance of 5 – 150 μH in series with less than 0.5 mΩ and a capacitance of 10 – 1000 nF [23]. The characteristic frequency f_0 and the quality factor Q of the RLC series resonator circuit that models the wire, are respectively:

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \tag{1}$$

$$Q = 2\pi \cdot f_0 \cdot \frac{L}{R} = \frac{1}{R} \cdot \sqrt{\frac{L}{C}} \tag{2}$$

A step signal starts ringing if the characteristic frequency f_0 of the parasitics is included into its frequency spectrum. By placing usual values of parasitic inductance and capacitance of a wire few meters long in (1), a characteristic frequency f_0 of about 13 – 712 KHz is obtained. The Fourier transform of a step signal presents an asymptotic behavior with a slope of -20 dB/dec up to the cutoff frequency f_t and then with a slope of -40 dB/dec:

$$f_t = \frac{1}{\pi \tau_r} \tag{3}$$

where τ_r is the rise time.

Fig. 47. Valeo mechatronic 3rd generation brush-holder (BH03G) regulator System on Chip (SoC). The IC is mounted on the leadframe without package.

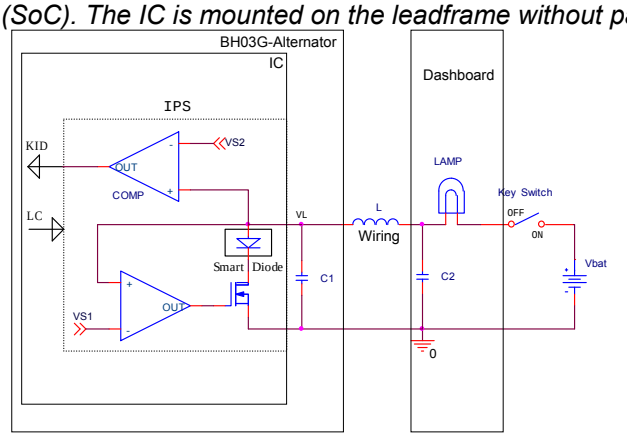


Fig. 48. Basic scheme of the IPS proposed, highlighting the wiring parasitics, the lamp and the key switch in series to the battery.

With τ_r of 10 ns – 1 µs, f_t is equal to 318 KHz – 31.8 MHz, values that are higher than those above evaluated for f_0 for almost all the wire lengths, with the result of starting ringing because the characteristic frequency is a spectral component of the step signal frequency spectrum. Avoiding, or at least reducing, ringing on the connecting wire from driver circuit to load is mandatory because, besides the issue represented by latch-up, it can cause high voltage spikes and unwanted EMI radiated.

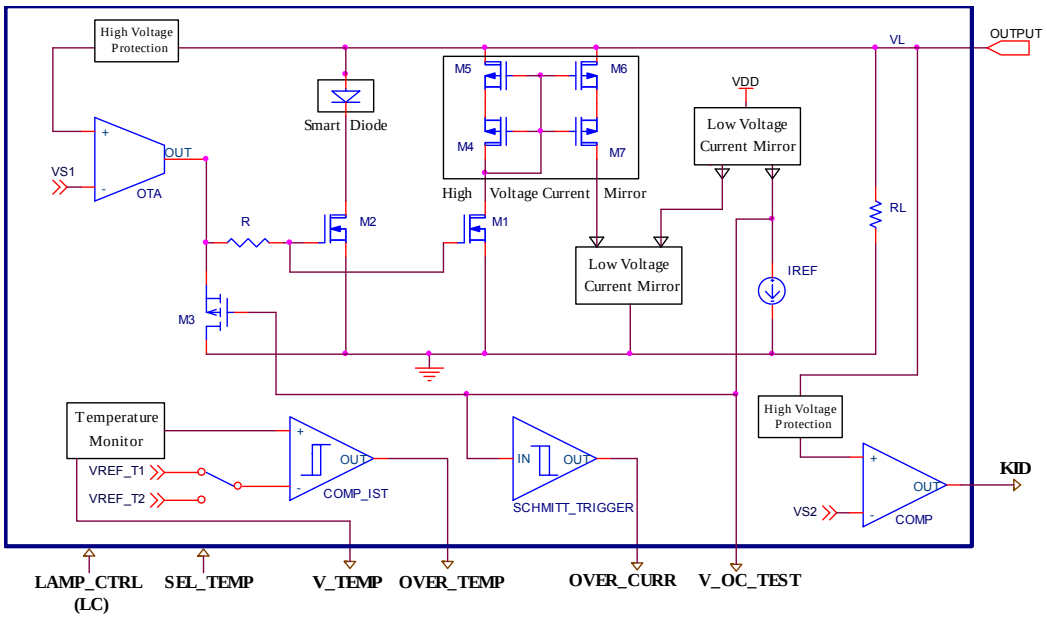


Fig. 49. IPS schematic view.

To manage the ringing issue, and more in general high transient over-current and over-voltage, techniques such as *Soft Start* [45] and *Control Slope* [48] have to be implemented when designing the IPS. The ability of handling a critical condition like the one just described by means of configurable functions, as well as many others that will be shown in the next section, is the surplus value of the designed IPS in the harsh automotive environment. Finally, full diagnostics on-chip have to be also integrated to help the control unit to quickly identify and isolate faults, improving safety of the entire system.

3.2 Design Flow of an IPS for Automotive Harshest Operating Conditions

The IPS proposed has been embedded in a regulator SoC for an automotive alternator as an example of application, although it would be used in a wide range of fields besides the automotive one, like in the industrial automation or computer peripherals.

The SoC where the IPS is embedded, is described in [46]: by combining Austriamicrosystems AG (AMS) HV-CMOS 0.35 µm ASIC technology and Valeo Engine and Electrical Systems mechatronic 3rd generation brush-holder (BH03G) regulator (Fig. 47), mounted on an alternator, a demonstrator has been implemented. This demonstrator represents a proof of concept for a new type of smart and flexible regulators which implement many additional programmable functions that give the car maker a better control to reduce vehicle fuel consumption and CO2 emissions. The main function of this SoC is the regulation of the voltage on the output of an alternator sensed at the alternator or the battery side, as well as the handling of the communication with the *Engine Control Unit*.

The starting point for the development of the IPS designed is the circuit described in [56], a patent of Valeo. The basic scheme is shown in Fig. 48: the circuit is designed to drive a small filament bulb lamp, which is mounted on the dashboard and has to be switched on to alert the car driver in case of alternator malfunction. The circuit also monitors the voltage on its output to inform the alternator regulator when the ignition key is plugged and engaged and, at the same time, to detect the internal low side switch state. The output pin of the designed IPS is then exploited both in driving and sensing to handle these required functionalities.
Even two apparently trivial tasks like the ones described above, represent a challenge for a designer because of the harshness of environmental conditions where ICs for automotive have to work.
Indeed the SoC, and in particular the IPS described, have to fulfill the following hard operating and absolute maximum conditions:

- Capability to drive two inter-changeable loads efficiently: a LED or an incandescent lamp, by avoiding issues due to its in-rush current behavior.
- Robustness against effects of wiring parasitics: ringing, high voltage spikes, risk of instability.
- Low EMI.
- Operating Junction Temperature Range: -40 – 150 °C, up to 190 °C during short periods.
- High Voltage (up to 55 V) and Reverse Polarity Voltage on output pin (up to -15 V).

Each constraint of the above listed ones has compelled to adopt a specific strategy and to integrate a proper block. Fig. 48 shows the main components of the IPS and the external configuration: the output *VL* is connected to the battery through the series of the load and the key switch. Significant and variable wiring parasitics complicate the design, since the length of the wire can fairly change depending on the car model where the system is embedded.
The whole architecture of the proposed IPS, including functions, protections and diagnostic, is presented in Fig. 49. The core of the scheme in this figure is the power MOS *M2*: it represents the low side main switch that controls the state of the load, characterized by a high aspect ratio *W/L* in order to minimize its drain-to-source on-resistance. It is placed within a regulation voltage loop consisting of the Operational Transconductance Amplifier (OTA) and the two blocks *Smart Diode* (for Reverse Polarity Protection) and *High Voltage Protection*, having the aim of regulating the output voltage *VL* to the reference level *VS1* when load (LED or incandescent lamp) is turned on by means of the digital input signal *LAMP_CTRL* (*Incandescent Lamp Control*).
When the external key switch is off, the internal resistance *RL* pulls down the output pin to ground potential. On the contrary if the key switch is on and the power switch *M2* is off, the output voltage goes up to the battery level, since no significant current flows through the load and, consequently, zero voltage drop occurs on it. In the first case the circuit has to detect the open position of the key switch, while in the second case it has to signal that the key has been plugged and engaged and an ignition condition has happened. A third different situation occurs when the key switch, controlled by the external user, and the power switch *M2*, driven by the internal digital circuitry through the *LAMP_CTRL* signal, are both on: the

implemented loop acts to keep the lamp on, maintaining, at the same time, the output voltage on *VL* almost equal to the reference *VS1*. In this third case the circuit has still to detect the ignition condition and the voltage regulation function on *VL* makes it feasible: a comparator with a threshold *VS2*, few hundreds of mV lower than *VS1*, monitors the output voltage of the designed IPS and signals the key switch state outwards by means of the digital signal *KID* (*Key Ignition Detection*).
It should be noted here that *VS1* has to be a little bit higher than the threshold *VS2* but not too higher than it. This is because a large voltage drop on the load has to be guaranteed in order to make it work properly and, furthermore, the internal power dissipation, due to the current that the IPS sinks from the load when the power switch *M2* is on, has to stay below a certain limit. In this specific case for automotive alternators the threshold *VS2* has been fixed to 0.8 V and the regulated voltage *VS1* to 1.2 V, but, in general, they can be adapted to the requirements of other possible applications.
The first distinctive feature of the proposed IPS in comparison with the state of the art [48]–[50] is the voltage regulation of the output when the load is turned on: the solutions proposed in [48]–[50] do not show a voltage control of the output that therefore depends on the load current and on the drain-to-source on-resistance R_{DSon} of the main power switch[1]. As a result, the output voltage varies with the output current that flows through the load resistance and the key status detection is not possible. In the proposed scheme instead, both with a 3 W incandescent lamp, that shows a steady state resistance equal to about 45 Ω, and a LED with a current limitation resistance of 460 Ω, the output voltage is regulated to the same value (1.2 V).
An additional advantage of this solution is the possibility of detecting, besides the key switch condition, the state of the power MOS *M2*, which determines the load state, by adding another comparator generating a hypothetical output *LID* (*Lamp Ignition Detection*) from the comparison of the output voltage with a threshold *VS3*. This threshold has to be set higher than *VS1* and the correspondent *LID* signal can be used as a self-diagnostic bit to monitor if the output of the designed IPS responds properly to the *LAMP_CTRL* command. By combining *LID* and *KID* the following cases can be distinct and indicated outwards: key switch off, key switch on – power switch off, key switch on –power switch on.
The other components of the overall architecture have been added to fulfill the abovementioned requirements a) – e), providing the following features to the system:

3.2.1 Current limitation & over-current protection

In addition to the voltage regulation loop described above, a linear current limitation loop has been integrated in the designed IPS too. It has been introduced considering two main objectives: to handle and limit the in-rush current behavior, distinctive of the switching of a bulb lamp filament and to avoid die destruction in case of a short circuit of the lamp wiring to the battery voltage.

[1] since a MOS fully turned on (in the Ohmic region) behaves like a resistor its drain-to-source voltage is equal to the product between R_{DSon} and the drain current

In order to protect the silicon from the large self-heating caused by the short-circuit current, the linear current limitation is time-limited and its maximum duration can be programmed, as described hereinafter. A mirror current sensing has been exploited (see Fig. 49): the MOS *M1*, having an aspect ratio much lower than *M2*, mirrors a small fraction of the output current I_{out} inside the loop. This current sensing solution presents a better accuracy with respect to the adoption of the R_{DS} sensing technique [44]. When compared to the use of a sense-resistor in series to the power MOS the adopted current-sensing strategy offers the following advantage: no additional voltage drop above the power MOS *M1,* which helps the designer to avoid the risk of exceeding the output voltage range and to keep the internal power dissipation below the required limit.
The mirrored current I_{mirr} is a small fraction of I_{out} in order to limit the internal power dissipation. The level of the limitation I_{lim} is a trade-off between the need of reaching the proper value to switch on the lamp and the necessity of keeping the junction temperature below the limit (around 180 – 190 °C) fixed by technology, even with the maximum operating ambient temperature (up to 150 °C for short periods). The current I_{mirr} is compared with an internally generated current (by means of a band gap scheme) I_{REF}; the difference I_{mirr} - I_{REF} drives the gate of a MOS (*M3* in Fig. 49) that closes the feedback loop: if $I_{mirr} < I_{REF}$ the loop is open and no current limitation is applied, whereas if $I_{mirr} \approx I_{REF}$ the gate of the power MOS *M2* is pulled down, V_{GS2} and consequently I_{out} decreases.
For a full diagnostics and monitoring of the IPS state, the voltage of the node where the difference I_{mirr} - I_{REF} is evaluated *V_OC_TEST* (*Voltage Over Current Test*), is sent to an external pin, as well as the digital signal *OVER_CURR* (*Over-Current*), generated by a Schmitt trigger from the same node of comparison. It should be noted that the over current condition, due to the effect of the current limitation loop, increases the output voltage above the regulation range and could also be detected by the *LID* signal already described.
The innovative aspects of this solution compared to the ones employed in literature [48]–[50], are two: the first one is the inclusion of the linear feedback loop in an architecture integrating a regulation voltage loop too, therefore implementing both voltage and current controls; the second one is represented by the configurability of the current limitation, in this way being adaptable to different power loads.
Electrical simulations in Fig. 50 show current drained by a 5 W incandescent lamp during the start up transients, varying the reference current I_{REF} and, consequently, the level of the current limitation (from 623 mA to 1226 mA in this example). The higher is the current limitation, the shorter is the thermal transient because the filament bulb reaches its incandescent temperature earlier. A *VHDL-Analog Mixed-Signal* model of a 5 W bulb filament has been exploited for the electrical simulations, taking into account the power dissipation for thermal conduction and radiation, as well as its thermal capacitance to evaluate the thermal and electrical transients.
In addition to the configurable *Current Limitation* a configurable *Over-Current Protection* has been implemented so as to improve the overall reliability: providing the *Current Limitation* to the system does not

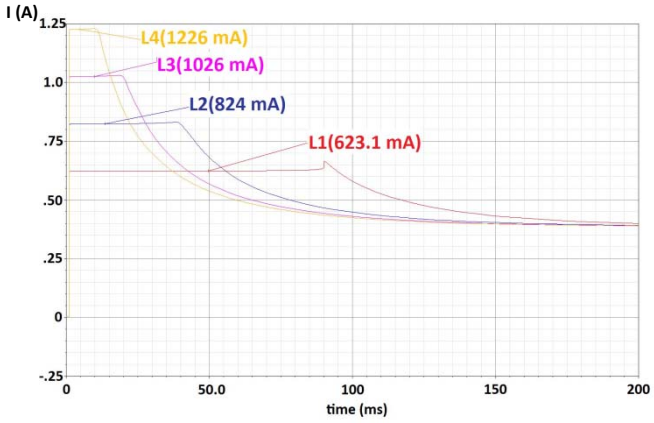


Fig. 50. Electrical simulations showing the current drained by a 5 W incandescent lamp varying the level of current limitation: the higher is the current level, the shorter is the thermal transient.

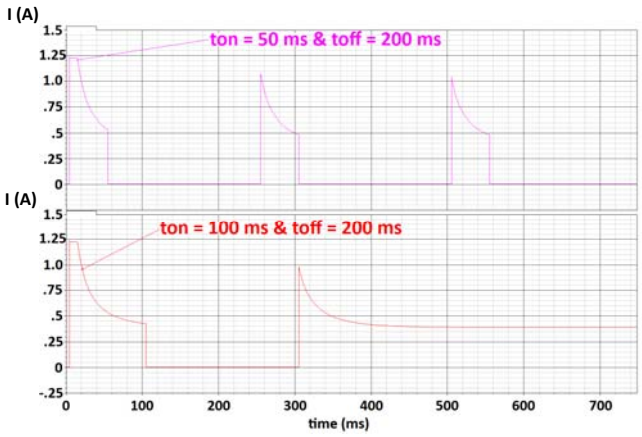


Fig. 51. Electrical simulations showing the transient current drained by a 5 W incandescent lamp during the start up: by increasing duty cycle the steady state is achieved after two cycles.

preserve it from thermal issues in case of short circuits or long transients with low resistive loads. As a matter of fact, the high current supply, for instance when a short-circuit occurs, would lead to the over-heating of the die. If an output over-current lasts more than a configurable lapse of time, a *Soft Start* strategy is adopted switching the load by means of a configurable control signal, both in frequency and duty cycle. In Fig. 51 the above mentioned *Soft Start* strategy is shown: in the upper graph, the duty cycle set to 0.2 impedes the lamp to reach the steady state, because the temperature of the filament does not rise up to the incandescence level. On the contrary, by increasing the duty cycle to 0.33 the incandescence is reached after two pulses, as illustrated in the lower graph.
Such flexibility, not present in [48]–[50], leads to an overall improvement of the adaptability of the system to different operating conditions and loads.

By combining the configurability of *Current Limitation* and *Over-Current Protection* the proposed IPS can efficiently drive also electrovalves, power limited electric motors and incandescent lamps, with operating temperature ranging from -40 °C to 150 °C, so fulfilling harsh automotive requirements completely.

3.2.2 Robustness against wiring parasitics effects

The wiring parasitics included in Fig. 48 consist of an inductance *L* in series to a resistance, negligible with respect to the load resistance and a capacitance *C2*; in addition the connector capacitance *C1* has to be considered too. By using a specific wire suitable for automotive application, few meters long, values of the magnitude of 10 nF for *C1*, 100 nF for *C2* and 1 – 10 µH for *L* have to be considered. Of course values of parasitics vary as function of the length and the quality of the wire. The resistance of the load can change too, since the IPS has to be able to drive a LED or an incandescent lamp, which presents a non-linear resistive behavior as it is described in the previous section. Such variability in the wire and load parameters causes a spread of the zeros and poles of the transfer function that makes hard the stability of the system, since it is based on a double feedback loop. As shown in Fig. 52, by sweeping through different values of the wiring parasitics and of the equivalent resistance for different LED-based load configurations, the phase margin of the voltage regulation loop in Fig. 49 changes in

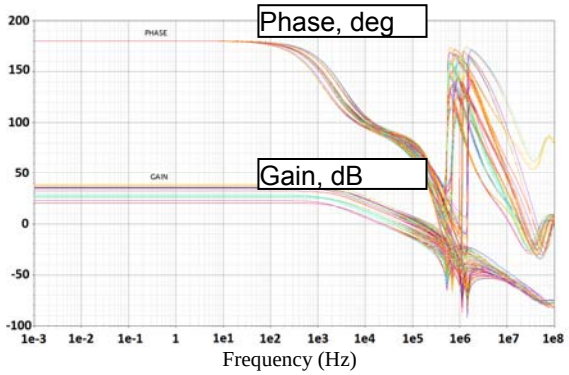


Fig 52. Simulations showing the gain and phase of the voltage regulation loop among all the PVT corners and varying load and wire parameters.

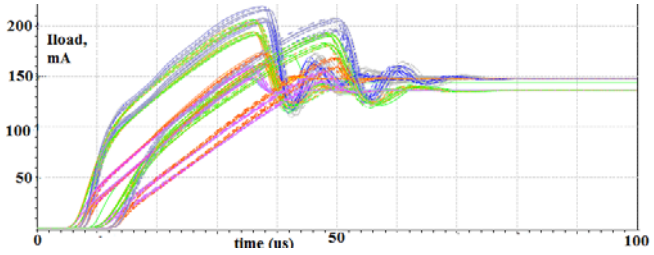


Fig. 53. Transient current when driving a LED before tuning the current slope. Simulations over all PVT, parasitic capacitance and inductance corner,

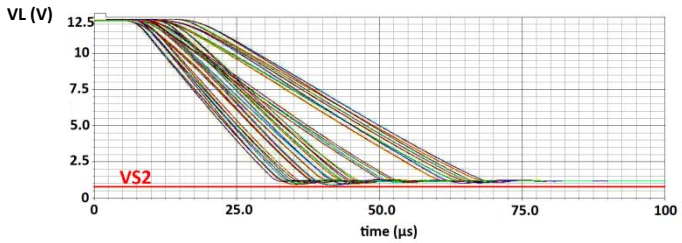


Fig. 54. Electrical simulations evaluated for all process and temperature corners, showing the transient output voltage during the driving of a LED: the comparator threshold VS2 is never crossed.

a relevant way. As a consequence, the susceptability to instability of the overall circuit varies, along with the entity of the ringing, as illustrated in Fig. 53.
An accurate tuning of the internal design parameters has allowed to get a sufficient phase margin of the regulation voltage loop (45°), for all the temperature and process corners. The achieved phase margin, combined with the controlled current slope transient described in the following paragraph III.c), limits the ringing on the output voltage and avoids that it crosses *VS2*, the comparator threshold used to discriminate the key switch state. In order to aim that, Fig. 54 shows the output voltage transients driving a LED for all process and temperature corners, where ringing has been minimized avoiding undershoots overstep the *VS2* threshold.
It is important to note that the ringing of the output voltage caused by the wiring parasitic elements can have a serious effect on the functionality of the block in the implemented alternator application. If, during the lamp switch on transient, the voltage becomes lower than the threshold *VS2* for a while, the IPS detects the open status on the key switch and the *KID* signal delivers to the alternator regulator the information to switch off the circuit. For instance Fig. 55 shows the transient voltage measured on a lamp driver stage mounted on vehicle, causing the switching off of the circuit (output voltage becomes even lower than ground). The wire connecting the lamp driver to the dashboard where the lamp is placed is 5 meters long: measurements of its parasitics have showed that the inductance is equal to 6 µH while the self-capacitance is negligible if compared to the dashboard connector capacitance, equal to 100 nF. The wiring resistance is also negligible.
The global architecture can also be simulated taking into account a more accurate model, compared to the one depicted in Fig. 48, of wiring and parasitic components. The simulation result is close to the measurement one and is shown in Fig. 56.
An anti-glitch filter, masking the *KID* information for a certain time after the switch on of the driver, should be used to filter the effect of ringing, but it is not necessary in the proposed IPS, integrating also a current slope control during the transients.

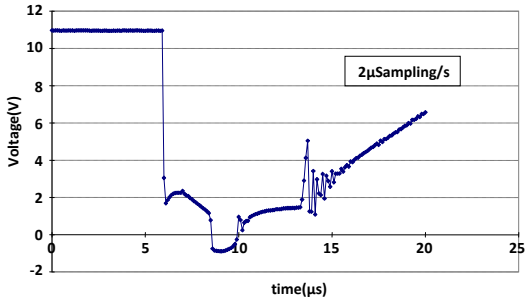


Fig. 55. Measurement of lamp switching behavior on vehicle causing untimely a reset of the alternator regulator circuit.

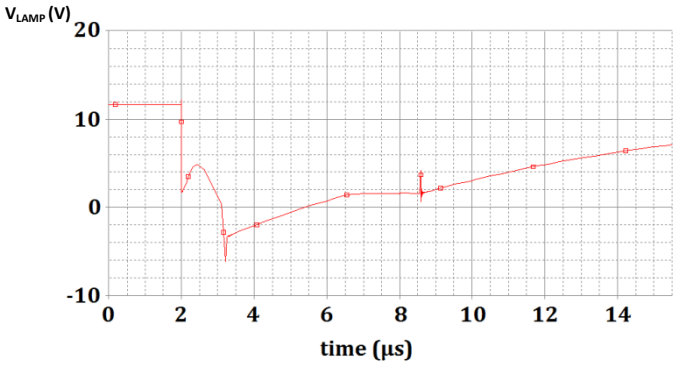


Fig. 56. Simulation carried out by exploiting an accurate model of the wiring parasitics and lamp stage, showing the output voltage transient (to be noted the undershoot at -6V).

3.2.3 Limitation of EMI – Control of current slope

The output current control, allowing to realize the *Current Limitation*, is performed also during the transients by means of the *Control of Current Slope*. Thanks to the architecture adopted, such strategy is easy to be implemented: the output current slope during the turn on phase of the load depends on how fast the power MOS *M2* is switched on. Since *M2* is driven by the output of the OTA, by controlling its slew rate[2] it is possible to control the load current slope. That leads to a double advantage, since a limitation both of EMI and ringing is obtained. Indeed the increase of the rise time τ_r decreases the cutoff frequency f_t, that is the limit above which the spectral density decreases as the square of the frequency. Such smoothness of the waveforms edges reduces the risk of starting ringing, since it does not occur if the characteristic frequency f_o of the wiring parasitics is above f_t. Ringing itself can be a cause of EMI and high transient current spikes: its

[2] The slew-rate can be controlled by tuning the dimensions of transistors that make it up and by regulating its bias current.

minimization is mandatory, since it can lead both conducted and radiated interferences.

Obviously, output current slope $\partial I_{out}/\partial t$ changes with the resistance of load R_{load} (an increase of R_{load} causes a decrease of $\partial I_{out}/\partial t$) and therefore an upper bound of $\partial I_{out}/\partial t$ has to be defined by design for the load having the lower resistance, so that any other value of R_{load} is improver for EMI. In this case, the upper bound of $\partial I_{out}/\partial t$ for a cold bulb filament showing a resistance of about 3 Ω is 62 mA/µs.

3.2.4 Harsh operating temperatures – Over-temperature protection

In a field of application such as the automotive, characterized by a wide operating temperature range [50], [51] and high power demanding electronic equipment, an essential feature for the reliability of the overall system is the *Over-Temperature Protection*. It starts when the junction temperature exceeds a threshold, fixed by technology, pushing to a standby-mode the entire IPS until a sufficient cooling of die has occurred. This effect is similar to the already described *Soft Start* strategy that acts switching off for a while the driver in case that an over-current lasts for more than a configurable time. In this case the thermal transients, due to internal power dissipation and cooling of the die, determine the period and the duty-cycle of driver switching pulses.

The over-temperature shutdown of the IPS is implemented to protect the die and avoid its damaging in case of high ambient temperature and/or high power dissipation, but it could also be used to realize a sort of *Soft Start* of the load, based on the temperature variations of the die when it has to provide large inrush currents. The effectiveness of this unconventional *Soft Start* strategy depends on the die and load thermal transients: the thermal time constant of the load should be higher than the one of the die to achieve its steady state, without damaging the die itself.

In the proposed IPS an integrated temperature sensor is placed near the power MOS *M2*, which is the hottest spot of the smart power module, because of the high output current that can flow through it. The generated voltage *V_TEMP*, proportional to junction temperature, is compared to a configurable threshold. If it exceeds the limit, a digital signal *OVER_TEMP* (*Over-Temperature*) is triggered outwards, in order to turn off the entire driver. The critical junction temperature threshold is made configurable between two possible values, by means of the signal *SEL_TEMP* (*Temperature Selection*), in the perspective of improving the overall flexibility.

3.2.5 High voltage protection & reverse polarity capability

In the state of the art a hard complication of the design is typically due to the need of protecting the output against high voltage, both transient and permanent. In [48], [50] a high voltage clamp is exploited in order to prevent failures of the system when a surge occurs on output, for instance during the turn-off of the load. In both the solutions the main power switch and current limitation are disabled during over-voltage, activating proper clamp circuits.

Such a solution represents an important advantage on the others, since together with the current limitation also the load protection is guaranteed.

Furthermore, to withstand reverse polarity voltages up to -15 V on output, every block of the overall scheme connected to the output terminal of the IPS has to

integrate solutions fit to limit the reverse current flowing out the pin and to prevent substrate charge injection that can lead to the conduction of the BJT parasitic devices present in the CMOS layout.
According to Fig. 49, the blocks needing to be hardened against high and reverse voltage are: *Smart Diode*, *High Voltage Current Mirror* and *High Voltage Protection*. The design of the *Smart Diode* block in series to the main power MOS *M2* has been made more complicated by the need of limiting the voltage drop between its terminals, since a voltage regulation on 1.2 V has to be guaranteed when the driver switch *M2* is on. An innovative design (AMS's patent pending) allows to minimize the voltage drop during forward conduction and to present a high resistive current path when reverse voltage is applied to the output, avoiding substrate charge injection and, de facto, ensuring reverse polarity capability.

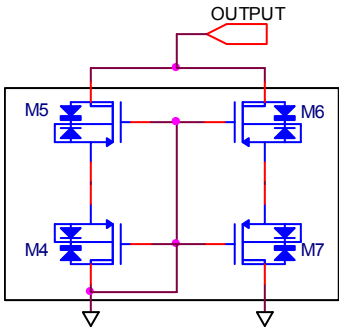


Fig. 57. High Voltage Current Mirror with reverse polarity capability.

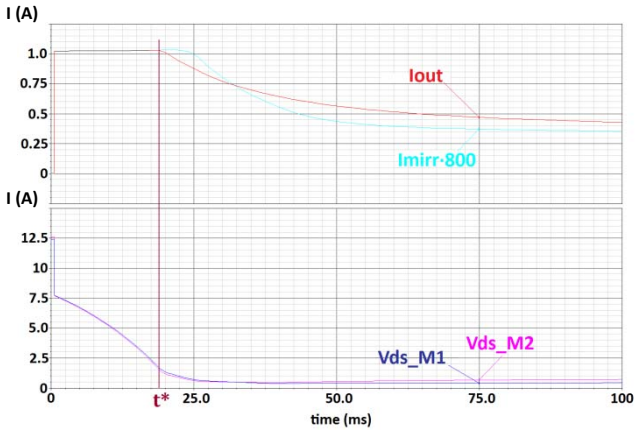


Fig. 58. Electrical simulations showing on top I_{out} and I_{mirr} multiplied by the mirror ratio, and the drain-to-source voltages of M2 and M1 below.

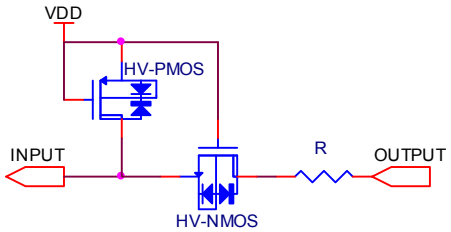


Fig. 59. Schematic of the High Voltage Protection block.

The adoption of the mirror current sensing technique, already described in the current limitation paragraph, imposes the use of an innovative solution because of the needed precision of the sensing and the high-voltage requirement on the IPS output. In order to have a good accuracy on the current mirrored by *M1*, and consequently on the current limitation, a good matching between *M2* and *M1* has to be guaranteed, but it is not enough. Indeed the drain-to-source voltages of the two MOS should be equal to eliminate the current mirror non-ideality resulting from channel length modulation. The drain terminals of mirroring NMOS *M1* and power NMOS *M2* can be kept to quite balanced voltage levels if the *High Voltage Current Mirror* on the top of *M2* is connected to the output of the IPS, as it is shown in Fig. 49 (the voltage drops on the *Smart Diode* and on the left side branch of the *High Voltage Current Mirror* are quite similar and the accuracy of the current mirror sensing technique is improved).

The consequent need of hardening the classic current mirror scheme against high voltage and reverse polarity, pushed towards the design of the new current mirror scheme shown in Fig. 57. HV-PMOS are able to withstand source-to-drain voltages up to 50 V [58], [59]; therefore stacking one HV-PMOS on each branch of the classic current mirror scheme and connecting the gate terminals of each couple of stacked MOS, can represent a valid solution if reverse polarity capability and high voltage protection are required. The high-voltage hardiness of the lower MOS (*M4* and *M7*) is exploited when the current mirror is active, while the upper MOS protect the circuit when a reverse voltage is applied to the output and thereby the MOS are in the inversion region. Indeed, thanks to those MOS, a back-to-back diode configuration is present in each branch of the current mirror (see Fig. 57), avoiding reverse current.

In Fig. 58 simulation results show the effectiveness of the solution: the drain-to-source voltages of *M1* and *M2*, illustrated in the lower part, during the turn-on transient of a 5 W bulb filament lamp overlap, allowing the current mirrored to be accurate. In the upper part of Fig. 11 the current mirrored by *M1*, multiplied by the mirror ratio $(W_1/L_1)/(W_2/L_2)$, is shown in the red colour, whereas the output current flowing through *M2* is illustrated in the light blue one (W_1, L_1, W_2, L_2 represent channel width and length of *M1* and *M2*). Note that, thanks to the overlap of the drain-to-source voltages of *M1* and *M2*, the currents are also equalized during the initial phase of the transient ($t < t^*$), when the current loop is active, fixing the current limitation level with precision. The difference between the two waveforms in the upper part of Fig. 58 for $t > t^*$ does not affect the functionality of the system, since the current limitation loop is no longer active.

A further solution used to protect the scheme against high voltage on output terminal is shown in Fig. 59: since an input terminal both of the comparator that

generates the signal *KID* and of the OTA for the voltage regulation are connected directly to the output, the gate oxide break-down of their input transistors would occur during turn-on transient without a proper protection block.
The *High Voltage Protection* block limits voltage on the input of the above mentioned circuits below *VDD,* that is the supply voltage equal to 3.3 V, when the output voltage is higher, allowing the input to follow the output for lower voltages. Once again the HV-MOS are exploited: a HV-NMOS having the gate connected to *VDD*, is placed as a pass-transistor in series to a high resistance for the limitation of the current flowing when negative voltage is applied to the output. A HV-PMOS, in diode configuration, links the input terminal to *VDD* when the HV-NMOS is off, preventing that node from being floating.
Finally, to protect the circuit when sudden surges, such as sparkling pulses due to harness coupling, are applied, the standard ESD protection structure has been improved to limit the voltage on *VL* between -25 V and 55 V and, at the same time, to be capable of sinking or providing a 500 mA current for at least 1 ms.

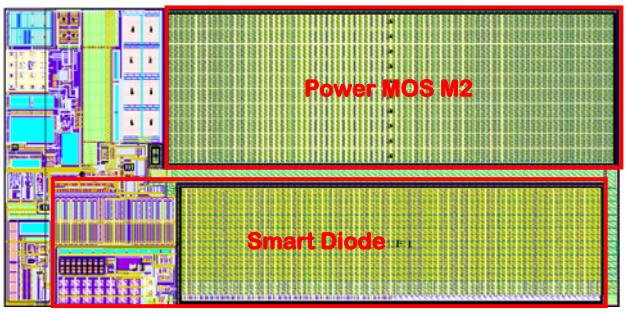


Fig. 60. Layout of the IPS realized in HV-CMOS technology.

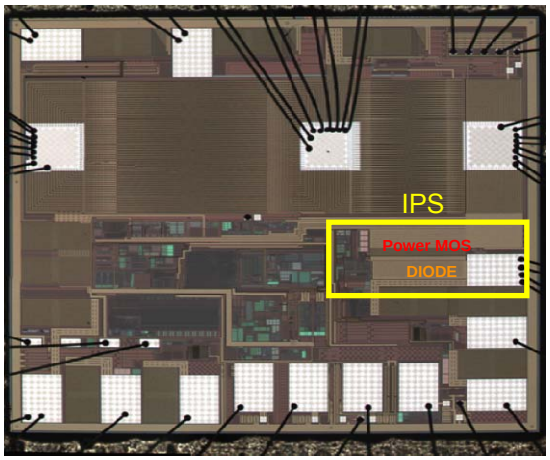


Fig. 61. Photo of the die of the automtove IC with the IPS (power MOS and its protection diode are highlighted)

3.3 IPS Implementation In HC-CMOS and Test Set-Up

3.3.1 IPS implementation in HV-CMOS technology

The IPS proposed has been realized within the SoC regulator system in AMS HV-CMOS 0.35 µm technology. The layout of the IPS is shown in Fig. 60-61, where the main power MOS *M2* and the *Smart Diode* are highlighted: note they are occupying the most of the IPS area in order to minimize the resistance of the electrical path formed by the series of those devices, when the driver is on. The other components of the IPS, such as comparators, OTA and temperature sensor, are placed on the left side of the layout. Table IX shows the environmental and electrical operating ratings at output voltage *VL* regulated on 1.2 V.

3.3.2 Verification flow

The verification and characterization of the IPS performed have been carried out according to the following steps:

- **Electrical Simulations**

In order to evaluate the IPS performance, verifying the compliance with all specifications, electrical simulations have been performed during the design. The development of the circuit has been carried out in *Virtuoso Cadence Analog Design Environment*, exploiting *Spectre* for the analog-mixed signal simulations.

- **IPS Component-Level Characterization**

The characterization of the innovative IPS herewith proposed has been included in the testing phase of the overall SoC programmable regulator system where it is integrated. The first validation phase of the prototype system has been performed by reproducing the harsh environmental conditions, typical of automotive, by means of a Thermal Stream System able to push test ambient temperature to the extreme values required by automotive environmental constraints. During this phase, nine samples of the SoC prototype have been tested at the

TABLE IX.

ELECTRICAL AND ENVIRONMENTAL RATINGS.

	Min	Typ	Max
Configurable Current Limitation (A)	0.5	1.0	1.5
Current Slope - Lamp (mA/µs)	10	50	80
Current Slope - LED (mA/µs)	0.4	–	35
Load (Ω)	3	10	460
Operating Temperature (°C)	-40	27	150
High Voltage on Output (V)	–	–	55
Reverse Voltage on Output (V)	-15	–	–
ESD – HBM (kV)	-8	–	8

MIN–TYP–MAX temperature corners (-40 °C, 27 °C and 150 °C). A 3-wire serial synchronous interface embedded in the SoC has been exploited to manage and validate all its functions. Fig. 62 shows the equipment used for this verification: the test-chip, placed on an evaluation board specifically realized for extreme temperature tests, communicates by means of the above mentioned serial synchronous interface with a DAQ Board (*Data Acquisition*), in turn interfaced to a host PC through a *PXI* link (***P**CI e**X**tensions for **I**nstrumentation*).
A *VI* (*Virtual Instrument*), developed in the *LabVIEW* environment, allows to manage the communication with the SoC prototype, handling its functionalities and checking signals generated on chip, such as the signal *V_TEMP* equivalent to die-temperature produced by the sensor integrated in the IPS. In order to complete the description of Fig. 62 it is to be noted that the host PC is linked through the *GPIB* interface (*General Purpose Interface Bus*) to the Measurement Instrumentation, such as multimeter and waveform generator, so creating a semi-automated test equipment.
Hardiness against wiring parasitic effects has been verified by reproducing on the evaluation board the LC model of the wire and connector, as shown in Fig. 48: since *L*, *C1*, *C2* change with the length and quality of the wire, discrete inductors and capacitors of different values have been used to ensure the stability of the IPS. Besides the distinctive features described in the previous section, such as ringing minimization and *Control of Current Slope*, the proposed IPS allows varying the load configuration too (LED or bulb filament lamp).

- **IPS System-Level Testing**

An additional testing phase has been accomplished by a Valeo team in a real automotive environment, placing the mechatronic 3rd generation brush-holder (BH03G) regulator SoC attached to an alternator in the car under-hood. This test on vehicle has allowed to verify the real strength of the IPS against electromagnetic disturbances, due to harness coupling, and its capability to drive an

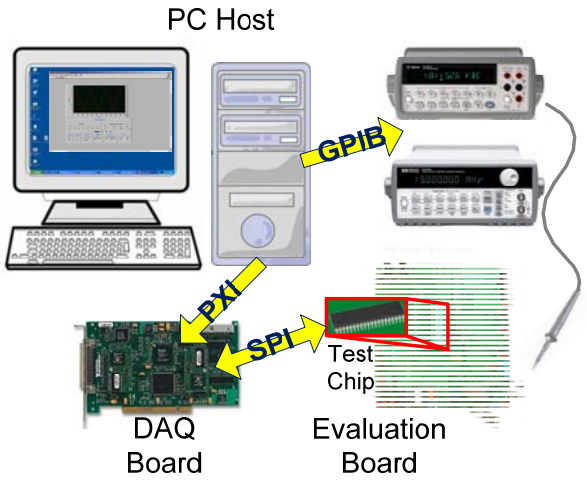


Fig. 62. Test equipment.

incandescent lamp as well as a LED, with real wiring from alternator to the dashboard, properly and without ringing.
This final test permits to complete the verification flow, proving the full compliance with all specifications in every possible condition required by automotive, also evidencing the high reliability of the realized IPS.

3.4 Experimental Results

The IPS behavior has been checked very carefully, by means of many measurements in order to analyze all the features integrated inside.
The experimental result reported in Fig. 63 shows the output voltage and current during the first part of the turn-on transient of a 3 W filament bulb lamp, as captured from the oscilloscope screen, highlighting rise time and current limitation level. The same measurement, repeated using a LED with a current limitation resistance of 460 Ω, is illustrated in Fig. 64. From a comparison between the two measures, different current slopes can be noticed; moreover, the absence of ringing in both the measures is easily observable, demonstrating the effectiveness of the *Current Slope Control* strategy, even in presence of high values of wiring and connector parasitics.
The working of the current limitation loop is observable in Fig. 65: the loop gets active during the turn-on of a 3 W bulb lamp, limiting the load current until the gate voltage Vg_3 of *M3* (the PMOS that carries the feedback signal back on the output of the OTA) is low.
In order to prove the high flexibility of the IPS realized, its operating with a higher power demanding load has been tested. The load used as an example for the analysis of the potentiality of the circuit proposed, is a 10 W incandescent lamp. By using the default value for the current limitation level (800 mA) and setting t_{on} and t_{off} (the time intervals during which the main power switch is on and off when the *Over-Current Protection* is active) equal to about 25 ms, the bulb filament is not able to reach its incandesce temperature, lighting intermittently (Fig. 66).
The steady state of the 10 W lamp is achieved in 210 ms, after 8 pulses, by increasing the current limitation level to 1.5 A and setting the duty cycle on 0.5 (t_{on} = 15 ms; t_{off} = 15 ms), as shown in Fig. 67.
In an application where a quick turn-on of the load is required, the duty cycle can be increased in order to speed the load driving: in Fig. 68 the steady state is reached after only 70 ms, configuring t_{on} equal to 80 ms and t_{off} to 8 ms. The risk of increasing the duty cycle of the *Soft Start* strategy is represented by the die-overheating. Fig. 69 presents the junction temperature measured by the temperature sensor embedded in the IPS. The thermal transient depends on the ambient temperature, in this experiment equal to 30 °C, as well as on the setting of the *Current Limitation* and *Over-Current Protection* and on the load characteristics (10 W bulb lamp). By increasing the duty cycle, a faster thermal transient occurs, reaching higher steady state junction temperature.
The experimental results shown in Fig. 69 explain the high flexibility and adaptability to different environmental conditions and loads of the IPS proposed. Indeed, depending on the ambient temperature and on the load characteristics, the key parameters of Current Limitation and Over-Current Protection techniques can be changed, even run- time, in order to adapt the system to the specific situation, limiting thermal stress. The transient response of the IPS with a 1.5 W bulb lamp is

represented in Fig. 70, while Fig. 71 shows the same waveforms, output voltage and current, during the driving of a LED stage. By comparing these experimental results with the same measurements made by mounting the test-chip on an evaluation board in a lab, an identical behavior can be noticed. Once again the parasitics, not modelled as in the previous measurements but introduced by real wire and connector, do not start ringing, demonstrating the robustness of the design.

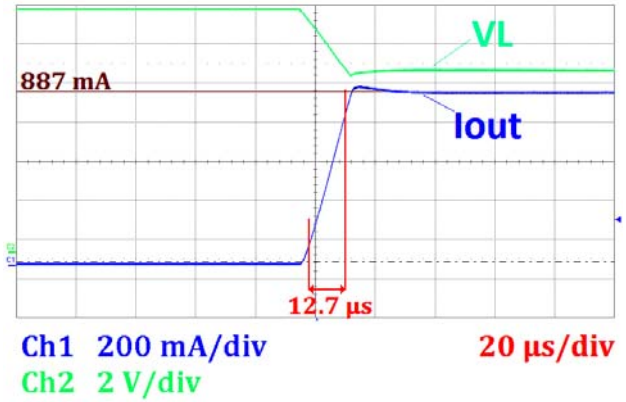


Fig. 63. Experimental measurement showing output voltage and current during the turn-on transient of a 3 W bulb lamp.

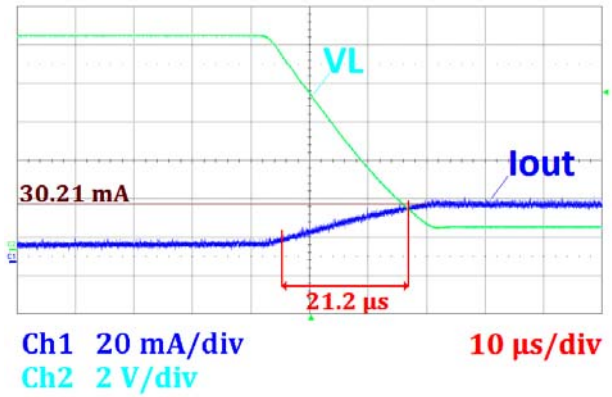


Fig. 64. Output voltage and current during the turn-on transient of a LED (a current limitation resistance is placed in series), as captured from the oscilloscope screen.

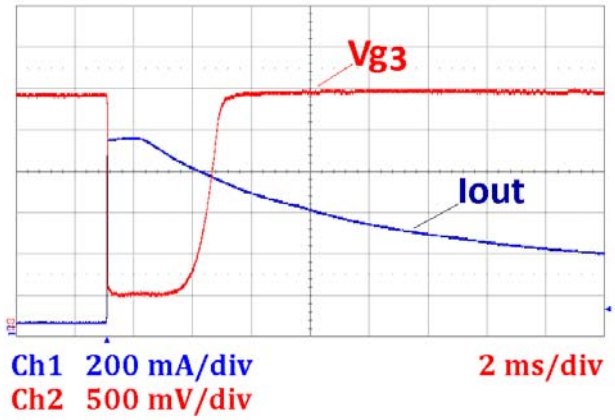


Fig. 65. Experimental results showing the behavior of the current limitation loop driving a 3 W bulb lamp: the waveform in light blue color is the gate voltage of the MOS M3 and the one in yellow color is the output current.

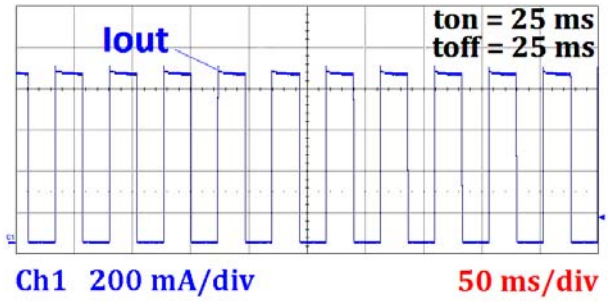


Fig. 66. Experimental measurement showing the current flowing through a 10 W bulb lamp with ton= toff = 25 ms and current limitation level equal to 800 mA: note that no steady state is reached.

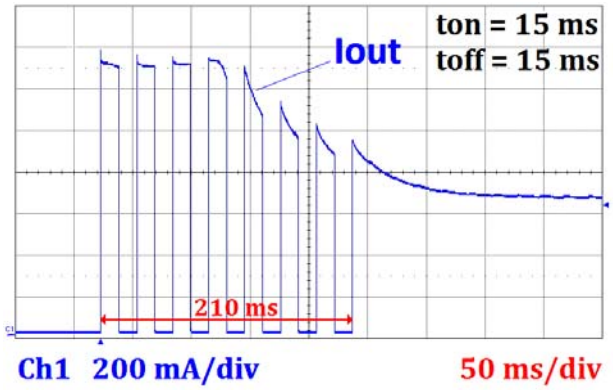


Fig. 67. Current flowing through a 10 W bulb lamp during the turn-on, setting t_{on}= t_{off} = 15 ms and current limitation level equal to 1500 mA: with respect to Fig. 18 the steady state is achieved after 8 pulses.

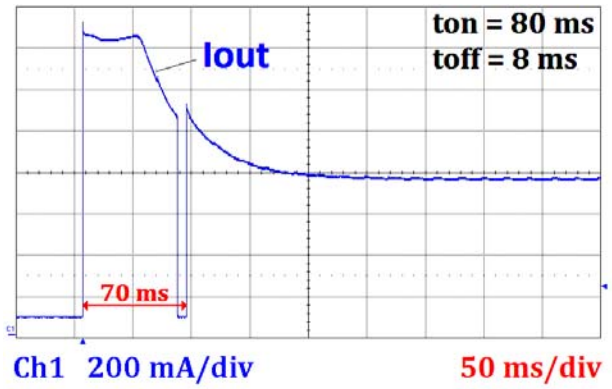


Fig.68. Experimental result showing the current flowing through a 10 W bulb lamp, setting t_{on}= 80 ms, t_{off} = 8 ms and maintaining the same current limitation level used in the measurement shown in the previous figure: the steady state is reached earlier.

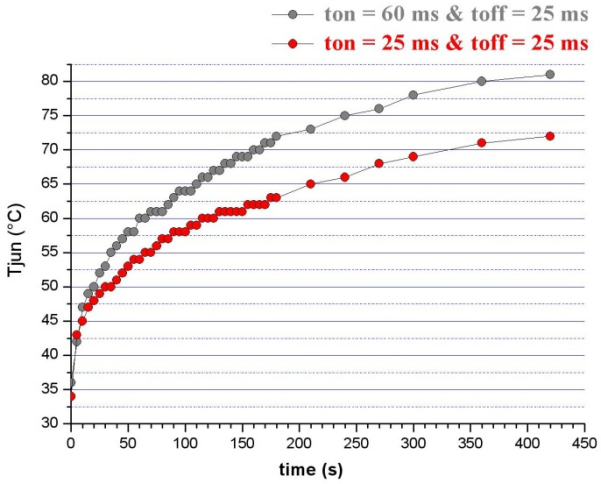


Fig. 69. Long-term thermal transient of the junction temperature measured by the sensor embedded inside the IPS, during the turn-on of a 10 W bulb lamp with ambient temperature equal to 30 °C. The measurement has been repeated increasing t_{on} with the consequent higher die-overheating.

Additional experimental results are shown in Fig. 70 and 71, realized during the IPS system-level testing phase, by mounting the test chip on the proper mechatronic brusholder and carrying out the measurements inside the car under-hood.

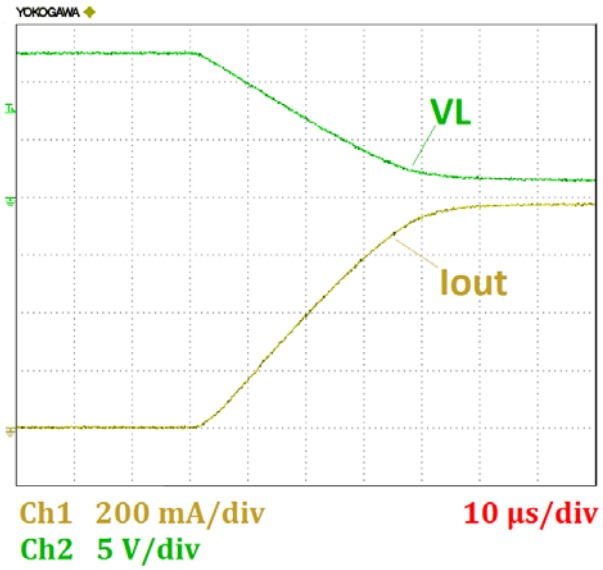


Fig. 70. Short-term behavior (10 µs/div) of the 1.5 W lamp voltage and current at the turn-on, measured in the car under-hood.

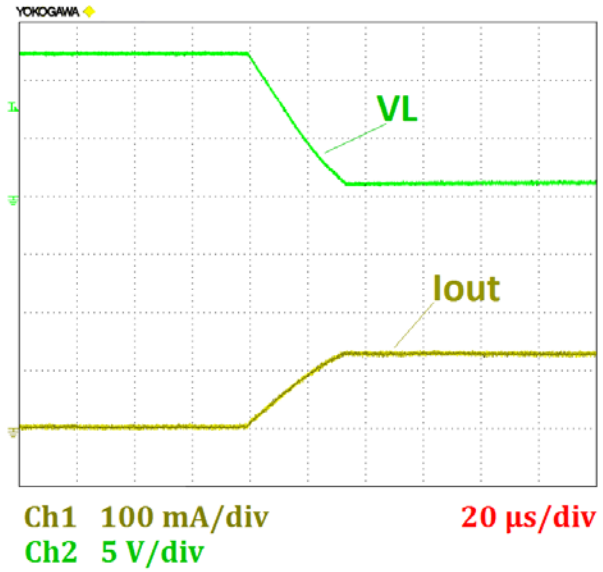


Fig. 71. Experimental measurements, taken out of a real automotive environment, show the turn-on transient during a LED driving.

CONCLUSIONS

In this thesis an overview of the research activity focused on development, design and testing of electronic devices and systems for harsh environments has been reported. The scope of the work has been the design and validation flow of Integrated Circuits operating in two harsh applications: Automotive and High Energy Physics experiments.

In order to fulfill the severe operating electrical and environmental conditions of automotive applications, a systematic methodology has been followed in the design of an innovative Intelligent Power Switch: several design solutions have been developed at architectural and circuital level, integrating on-chip self-diagnostic capabilities and full protection against high voltage and reverse polarity, effects of wiring parasitics, over-current and over-temperature phenomena. Moreover current slope and soft start integrated techniques has ensured low EMI, making the Intelligent Power Switch also configurable to drive different inter-changeable loads efficiently. The innovative device proposed has been implemented in a 0.35 µm HV-CMOS technology and embedded in mechatronic 3rd generation brush-holder regulator System-on-Chip for an automotive alternator. Electrical simulations and experimental characterization and testing at component-level and on-board system-level has proven that the proposed design allows for a compact and smart power switch realization, facing the harshest automotive conditions. The smart driver has been able to supply up to 1.5 A to various types of loads (e.g.: incadescent lamp bulbs, LED), in operating temperatures in the wide range -40 °C to 150 °C, with robustness against high voltage up to 55 V and reverse polarity up to -15 V.

The second branch of research activity has been framed within the High Energy Physics area, leading to the development of a general purpose and flexible protocol for the data acquisition and the distribution of Timing, Trigger and Control signals and its implementation in radiation tolerant interfaces in CMOS 130 nm technology. The several features integrated in the protocol has made it suitable for different High Energy Physics experiments: flexibility w.r.t. bandwidth and latency requirements, robustness of critical information against radiation-induced errors, compatibility with different data types, flexibility w.r.t the architecture of the control and readout systems, are the key features of this novel protocol.

Innovative radiation hardening techniques have been studied and implemented in the test-chip to ensure the proper functioning in operating environments with a high level of radiation, such as the Large Hadron Collider at CERN in Geneva.

An FPGA-based emulator has been developed and, in a first phase, employed for functional validation of the protocol. In a second step, the emulator has been modified as test-bed to assess the Transmitter and Receiver interfaces embedded on the test-chip. An extensive phase of tests has proven the functioning of the interfaces at the three speed options, 4xF, 8xF and 16xF (F = reference clock frequency) in different configurations.

Finally, irradiation tests has been performed at CERN X-rays irradiation facility, bearing out the proper behaviour of the interfaces up to 40 Mrad(SiO_2).

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