Continuous-Caliber Semiconductor Components

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***Abstract*— The needs in terms of power electronics has evolved and for high power applications, the increase of efficiency mainly goes through the increase of the voltage of the system. However, this is not possible with a conventional two-level topology because the semiconductor ranges are limited to 6.5 kV which approximatively corresponds to a blocking voltage of 3.6 kV. To overcome this semi-conductor limitation, multilevel topologies can be used and allow to extend the range of the DC bus input voltage while using smaller and more efficient components. Yet, the sizing of an optimal power converter with high efficiency and power density is hard to realize due to the discretization of semiconductor components calibers. Moreover, if we want to find the optimal value of the DC bus voltage for a specific application using an optimization algorithm, the use of continuous caliber for components will give better results. This paper aims to explain the used method to overcome this discretization by creating virtual components with exact suitable caliber, using the database parameters available from manufacturers. To do so, the used power converter losses and thermal models are recalled in order to specify the needed parameters. These parameters will be generated as to create the needed virtual component.**

Keywords—Semiconductor; switching losses; conduction losses; thermal resistance; power converter; efficiency

I. INTRODUCTION

HASTECS (Hybrid Aircraft Academic reSearch on Thermal and Electrical Components) project studies the possibility of electric propulsion hybridization in an aircraft. Besides the global architecture represented in Fig. 1, the different work packages aim to increase the specific power of the different components of a high-power electric chain incorporating a high-voltage DC bus, its wiring and power electronics interfacing the bus and the electric motor in order to have a solution that can be fitted in an aircraft [1].

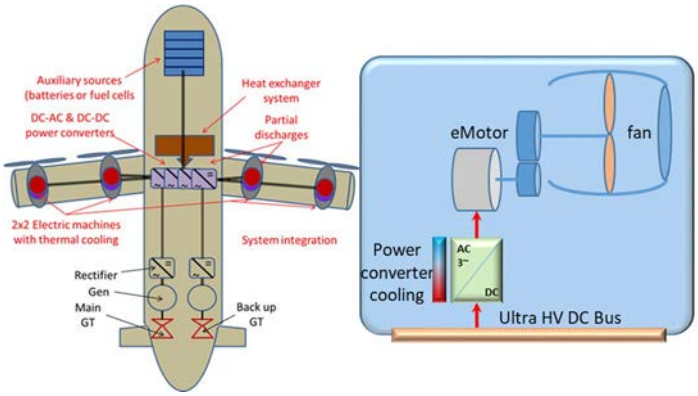

Fig. 1: Global Electrical point of view for Hybrid Electric Aircraft

This study will lead to an optimization of the complete chain that will propose the interesting structure (s) integrating all aeronautical constraints such as partial discharges for electrical equipment placed in non-pressurized zone or in case of high operating voltage even in pressurized zone. In this study, power electronics topologies, smart control and modulation strategies and also semiconductor technologies will be taken into account. HASTECS project has set itself the challenge of doubling the specific power of electric machines including their cooling, while the power electronics, with their cooling system, would evolve from 15 kW/kg for 2025 to 25 kW/kg in 2035. This would reduce the inverter and motor weights, resulting in a reduction in fuel consumption of about 3.5% on a regional flight.

One of the work package focus on the static converters and the DC bus. In order to guide the work of the various work packages of the project, a first step is to determine an optimal DC bus voltage range. This has a direct impact on the study of partial discharges but also in the design of motor windings. Then, it is necessary to compare the efficiency and power density of several multilevel topologies. Using the simulation tool and the available database detailed in the second and fourth parts of this paper, the efficiency is plotted for several studied inverter topologies (Fig. 2). The noticed jumps of efficiency are due to the change in the used component calibers.

Therefore, it is made difficult to find the optimal DC bus voltage due to the discretization of available voltage ratings. To overcome this problem, we created a continuous components database that suits the needed voltage rating by fitting and extrapolating the existing database components. Of course, these components may never exist, but it allows to see the effect of the choice of the static conversion architecture on the efficiency over the voltage range considered, while removing a bias (discretization of ratings).

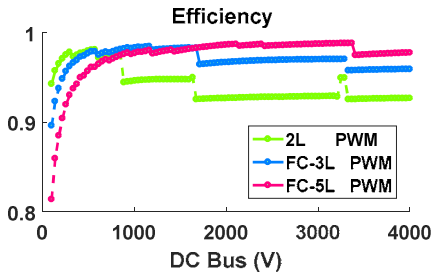

Fig. 2: Efficiency for several topologies using available database components

This solution will help us explore several possible solutions. Validation of the results will be done by simulation so as not to limit the number of proposed architectures. The experiment will be done in a second time, after this project, to verify the solutions that will come from the overall optimization.

II. SIMULATION TOOL

The research project [2] aims to develop a simulation tool which allows to pre-size converters. It computes different results for different conversion architectures. Its entries are the design constraints (DC bus voltage, output power, …), the foreseen converter topologies, and the semiconductor family or manufacturer choice from the available components database. The results such as the efficiency, number of semiconductor devices (series, parallel, total), voltage rating selection, maximal junction temperature, losses (conduction and switching), voltage and current margins, switching and apparent frequencies, total losses, semiconductors, heat exchanger, DC bus capacitor and flying capacitor weights, and also the power density are shown as figures for different parameters of different architectures behaviors.

The tool makes it possible from a specification to size the converter according to the chosen topology. It also makes it possible to carry out parametric studies by varying the DC bus voltage, the requested power or the modulation index to determine the optimum operating point. It can also take into account a mission profile that allows checking the performances of the converter for a given mission[3].

For each design point, it selects from the available database, the most appropriate semiconductor components that fit well the desired voltage and current. In order to do so, an adapted algorithm was developed (Fig. 3). The first step of this algorithm is selecting the manufacturer chosen by the user to extract the corresponding components from the database. It is then determined whether the requested voltage rating can be achieved by the available components. If none of the components is adapted and therefore the biggest component is too small, components are connected in series to obtain the desired size. Otherwise, if several component calibers are suitable, the smallest caliber is chosen among those which are suitable so to have the best performing component.

Then the tool computes the different results. It is realized in *Matlab* and is based on analytical calculations of the losses in the semiconductor components for the various integrated multilevel architectures considering mainly a sinusoidal PWM (Pulse Width Modulation) control. These losses result in heating up the semiconductors. The thermal rising in the semiconductor will affect its functionality and its lifetime. Moreover, the losses impact the size of the cooling system needed in the design.

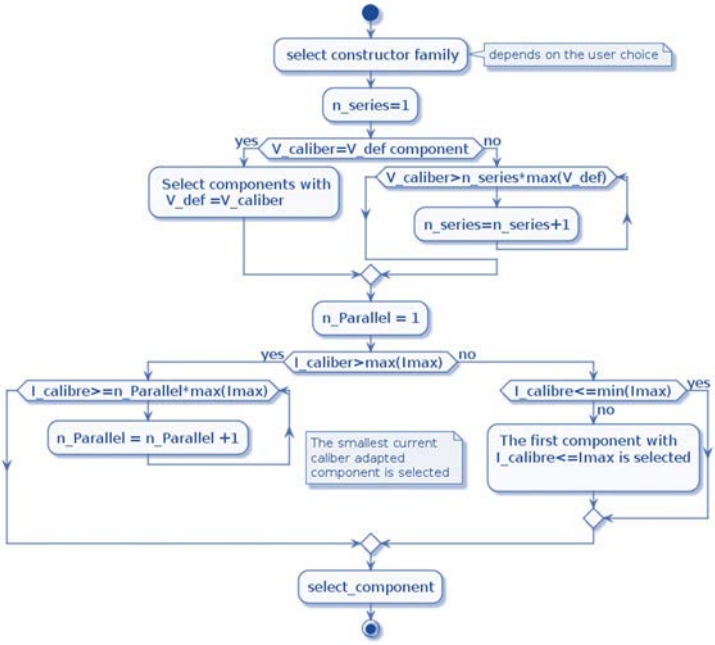

Fig. 3: Available component selection algorithm

It uses *Matlab* script and object programming to model converters architectures. It allows a great flexibility and a large degree of freedom for different designs and their behaviors during studies. This adds many advantages regarding multiple methods implementations and desired parametric sweep modeling.

III. POWER LOSSES AND THERMAL MODELING

A. Modeling principle

In order to model the losses in the semiconductor, we need to calculate the switching and conduction losses. Both losses depend on the circuit parameters and the device characteristics.

To calculate the conduction losses, the voltage between the collector and emitter of the transistor must be taken into account during its conduction phase. The transistor can be modeled with a voltage drop and an internal resistance connected in series[4] [5]. The voltage is obtained with the relation (1).

$$V_{ce} = V_{ce_0} + R_{dson} * I_c \quad (1)$$

Then the conduction losses can be computed using (2):

$$P_{cond} = V_{ce_0} * I_{average} + R_{dson} * {I_{rms}}^2 \quad (2)$$

Where $I_{average}$ and I_{rms} are respectively the average and RMS values of the current.

To calculate the switching losses, the curves of the energy losses versus the switched current given for a switched voltage, present in the datasheets, are used. They can be approximated by a second-order equation with three parameters A_x, B_x, and C_x with: $E_x = A_x + B_x * I + C_x * I^2$ (3)

For a switching frequency f_{sw} and a modulation period $T_{modulation}$, the switching losses are computed with:

$$P_{sw} = \frac{1}{T_{modulation}} \frac{1}{T_{sw}} \int_{t_1}^{t_2} \frac{V_{sw}}{V_{def}} E_{V_{def}}(I_{load}).\, dt \qquad (4)$$

$$P_{sw} = f_{sw} * \frac{V_{sw}}{V_{def}} * (A \frac{\Delta sw}{T_{modulation}} + B * I_{sw_{average}} + C * I_{sw_{rms}}{}^2) \qquad (5)$$

Where $I_{sw_{average}}$ and $I_{sw_{rms}}$ are respectively the average and RMS values of the switched load current, v_{sw} is the switched voltage of the semiconductor that depends on the topology, v_{def} is determined from the datasheet ($v_{def} = \frac{v_{max}}{2}$) and $\Delta_{sw} = t_2 - t_1$ the switching time interval.

The previous equations for the conduction and switching losses are also valid for the diode, knowing that the diode has only recovery losses as switching losses.

The equations stated before are given for one switch (transistor + diode). For all switches in the converter topology, the total power losses will be factored then by the number of switches.

$$P_{total} = (P_{cond} + P_{sw})\, n_{switch} \qquad (6)$$

Because of the semiconductors losses, a thermal model is needed in order to determine and manage the chip temperature. As for the electrical circuit analysis, the thermal analysis integrates power sources which represent the losses, temperature at different nodes and thermal resistors depending on the thermal conductivity and chip sizes.

In our architecture, a single power switch contains a transistor with an antiparallel diode that ensures a path for the reverse current. So the thermal model circuit will include two thermal resistors as in Fig. 4. Each resistor has a heat energy flow caused by the losses of each component. The temperatures of the different points in the switch package can be determined using the following equations:

$$T_{Transistor} = P_{losses_{transistor}}.\, R_{th_{jc}T} + T_{case} \qquad (7)$$

$$T_{Diode} = P_{losses_{diode}}.\, R_{th_{jc}D} + T_{case} \qquad (8)$$

$$T_{case} = (P_{losses_{transistor}} + P_{losses_{diode}}).\, (R_{th_{ch}} + R_{th_{ha}}) + T_{ambient} \qquad (9)$$

Where R_{th-jc} is the junction to case thermal resistance, R_{th-ch} is the case to heatsink thermal resistance and R_{th-ha} is the heatsink to ambient thermal resistance in K/W. Here, the case of the chips package is connected directly to the ambient (80°C or 90°C), so the heatsink to ambient thermal resistance (R_{th-ha}) is forced to zero. Then the assembly will be cooled down by a heat exchanger whose specification is written in order to fix the case temperature to the ambient (80°C or 90°C in our example).

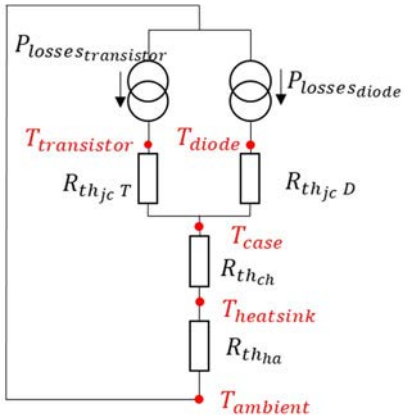

Fig. 4: Equivalent thermal model of an IGBT component with antiparallel diode [4]

B. *Needed parameters*

In order to evaluate losses and components temperature, we need the following parameters:

- Thermal resistance: R_{th-jc_T}, R_{th-jc_D}, R_{th-ch}
- Conduction parameters for IGBT and diode: V_{ce0} R_{dson}, V_d, R_d.
- Switching losses parameters (E_{on}, E_{off} et E_{rec}): A_x, B_x and C_x
- Component surface: Surface (mm^2)

These parameters are extracted from semiconductor manufacturer datasheets and used to create a database.

IV. CONTINUOUS-CALIBER COMPONENT

The simulation tool uses a created database that sums up the semiconductors technological parameters obtained from the manufacturer datasheets. The components are classified as families according to their manufacturer. In this case, only Silicon IGBT components are studied.

A. *Components' families*

Semiconductor manufacturers can offer relatively low IGBT devices rates but can reach as high as 6.5 kV/0.75 kA.

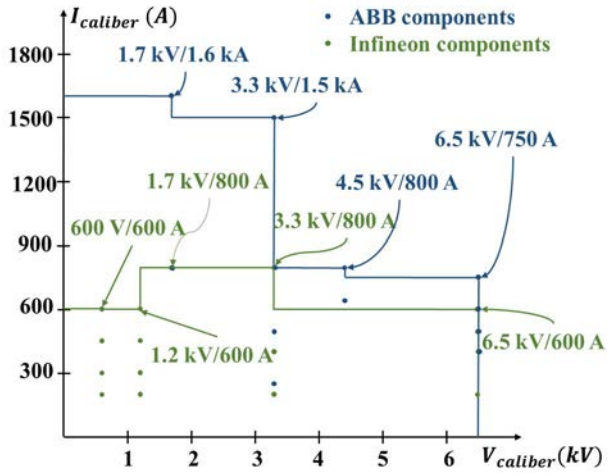

Fig. 5: Voltage and current ratings of high-power semiconductor devices

As shown in Fig. 5, the used database has two families of silicon components. The first consists of ABB components with four available voltage ratings (1700 V, 3300 V, 4500 V and 6500 V). Current ratings vary from 250 to 1600 A.

The second family is made up of Infineon components whose voltage ratings are: 600 V, 1200 V, 1700 V, 3300 V and 6500 V. For current calibers, they are smaller than those of the previous family and range from 200 to 800 A.

B. Generated components

There are discontinuities in the resulted curves due to the discretization of the components. These jumps are due to the change in component size used since the selected family (ABB components for example, has only four calibers (1700 V, 3300 V, 4000 V and 6500 V)).

The manufacturer does not make a customized component. However, using discrete components in our simulation brings up jumps in the resulted performance curves. Since it is an exploratory study, it is interesting to have components for all voltage and current ratings which will involve determining component parameters for sizes that vary continuously. In order to have a continuous database, we have to create components for the different desired ranges. The user will still have the choice of using real components instead of the created ones.

To create a component that does not exist in our database, we first select the family or manufacturer to which the created component will belong. For this purpose, all the parameters of the components belonging to this family are extracted from the *Excel* file. The desired current and voltage ratings are then defined to identify the variation law of this family components' parameters by selecting the closest existing current caliber components.

Once the various components have been selected, they will be used to generate the parameters of the desired component. The laws of variation of all the parameters are then identified as a function of the voltage caliber or current-voltage calibers product and then applied to the desired one.

For the switching energies E_{on}, E_{off} and E_{rec}, we can model the variation of their parameters (A_x, B_x, and C_x seen in equation (3)) using a polynomial function which is the function that fits the best our data. We chose second-degree polynomial functions because we do not have enough points in order to pick higher degree polynomial functions.

For the conduction losses, for both the IGBT and the diode, we need the on-state voltage drop at zero current condition and resistive elements which variations are also approximated by first-degree polynomial functions. We search a function that fits the variation of these parameters depending on the voltage and current calibers.

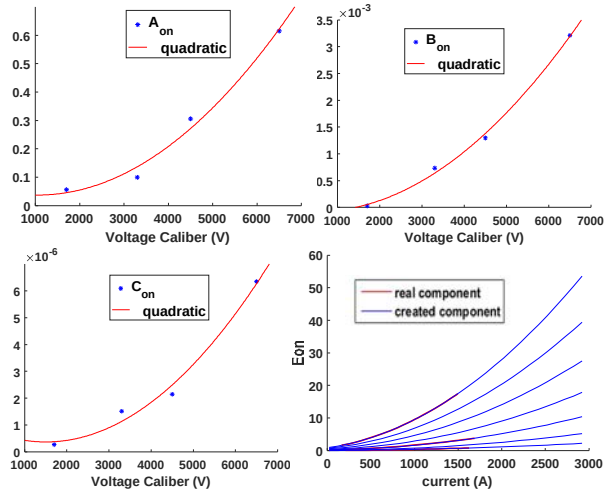

Fig. 6: Variation of Aon, Bon et Con versus voltage rating and E_{on} versus the current

The same method is used to generate the thermal resistors (heatsink-case, junction-case for both transistor and diode) as a function of the voltage and current calibers.

In order to generate the surface of the component, we search a function that fits the variation of this parameter depending on the current-voltage calibers. We can approximate this parameter also with a polynomial function. The value of the created component surface will be very helpful to design the cooling system allowing the computation of the thermal density.

Table I summarizes the order of the polynomial functions for the different parameters modeled.

TABLE I. SUMMARY OF GENERATED PARAMETERS

Generated parameter	**Depending parameter**	**Approximation function**
Switching losses parameters A_x, B_x and C_x	Voltage rating	Second-degree polynomial $f(x) = ax^2 + bx + c$
Conduction parameters for IGBT and diode V_{ce0} R_{dson}, V_d, R_d.	Voltage rating * Current rating	First-degree polynomial $f(x) = ax + b$
Thermal resistance R_{th-jc_T}, R_{th-jc_D} and R_{th-ch}	Voltage rating * Current rating	Second-degree power $f(x) = ax^b + c$
Surface	Voltage rating * Current rating	First-degree polynomial $f(x) = ax + b$

The generated semiconductor components will make it possible to compare the different parameters of the studied topologies in order to choose the optimum voltage range which will minimize the losses and increase the power density.

C. Comparison of real and generated components

The first studies will verify that the results with the generated components are coherent with the ones obtained with the real components. A DC voltage sweep is carried out using

Infineon components and the component choice is fixed manually in the simulation tool. Due to the limitation of the existing voltage calibers, the sweep range is limited to 4000 V due to the limitation of the existing components' voltage calibers which corresponds to 6500 V so a definition voltage of 3600 V. The power is fixed to 1 per unit.

1) Fixed component choice

For this study case, the voltage and current calibers are fixed for both real and generated components in order to check the validity of the generated components and also compare the impact of component calibers on the inverter performances. Fig. 7 represents the efficiency for fixed components allowing direct series association.

In order to have the adapted component, series and parallel connection are made if the needed component ratings are beyond the available current and voltage rating. The series connection is used to adapt the input voltage while the parallel connection is needed to adapt the current of the transferred power.

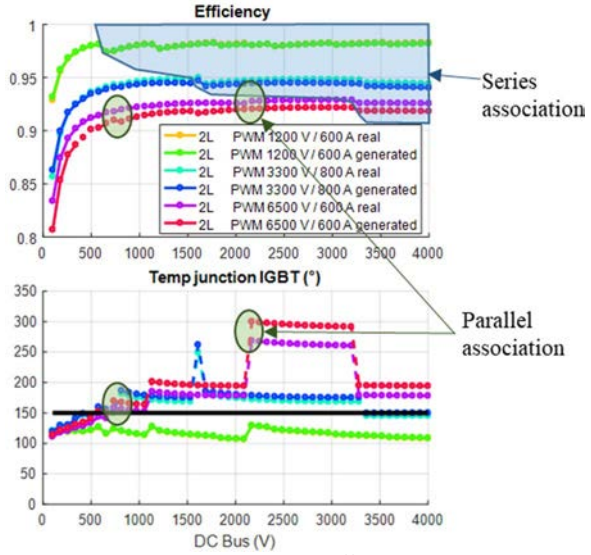

Fig. 7: Real versus generated components efficiencies and maximal junction temperatures for fixed calibers

For the tested components, the generated components have the same properties as the real ones. The difference between components conduction losses remains low compared to switching losses which is higher for larger voltage caliber components.

When comparing the properties of the resulted design based on the voltage calibers of used components, we notice that using small component is better than higher voltage ones which represent more switching losses even if we use more components in series in order to withstand the required voltage. The direct series association is hard to realize but seems to be the best option, efficiency-wise.

2) Fixed choice of the components' voltage caliber and adapted current

For the next simulation, the voltage calibers are fixed however the current ones are chosen in order to respond to the needed current with both real and generated components, so the last ones will always have a good use of the Silicon surface.

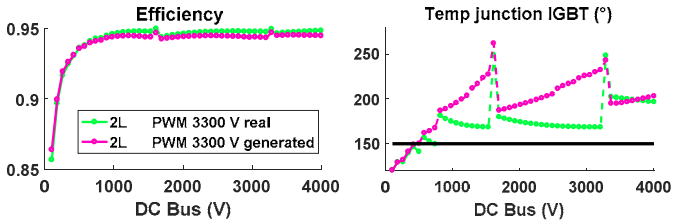

Fig. 8: Real versus generated components efficiencies and maximal junction temperatures for fixed voltage calibers and adapted current calibers

In this case, the real components have smaller thermal density due to the surface of the component which is bigger than the generated components ones. The bigger surface is, the lowest the current density is so the component junction temperature will be lower.

The jumps noticed for the temperature of the generated components are mainly due to the thermal resistor which does not correspond to the optimal value. The generated components have a higher thermal resistance as shown in Fig. 9. This is linked to the distribution of the thermal resistances that do not follow an obvious mathematical law. This data spread is related to the gap between the selected components which result in noise, sampling errors and nonlinearity of the distribution law.

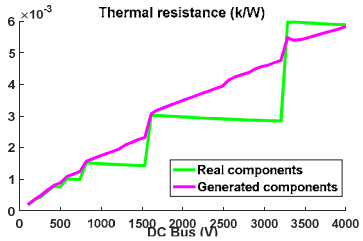

Fig. 9: Thermal resistance for real and generated used components

3) Adapted voltage and current calibers

For the third case, the voltage and current calibers are chosen in order to respond to the needed voltage and current to both real and generated components.

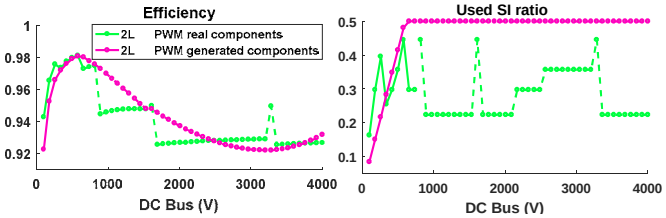

Fig. 10: Real versus generated components efficiencies and used Silicon ratio for adapted voltage and current calibers

The very high switching losses and maximal junction temperature for the first points of the simulation are due to the very low voltage calibers (100 to 500 V) that are lower than the smallest available caliber which is 600 V.

The efficiency curves overlap for the points that match a used Silicon ratio of 50% for the real components. This ratio is computed as follows:

$$Used_{Si_{ratio}} = \frac{V_{DC_{bus}} * I}{n_{switch} * \frac{V_{caliber}}{2} * I_{caliber}} \quad (10)$$

Where $V_{DC_{bus}}$ is the DC bus voltage, I is the load current, n_{switch} is the number of the used switches depending on the studied topology.

The generated components are optimized in order to use 50% of the installed Si all the time. The same remarks about the junction temperature can be made again.

V. USE OF CONTINUOUS-CALIBER COMPONENTS

In this approach, evaluation of converters specifications is studied for different DC bus voltages. The converters under study are the 2-level topology, 3-level FC, 5-level FC[6] and 5-level ANPC [7]. A parametric sweep of the DC bus voltage is implemented starting from 100 V to 4 kV for an imposed power of 1 per unit. The junction temperature is calculated using equations (7), (8) and (9) with a fixed ambient temperature of 90°C.

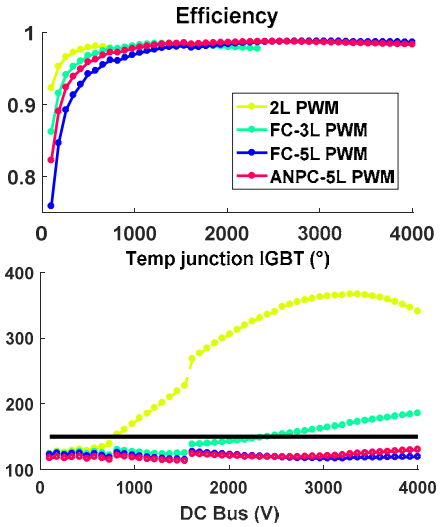

Fig. 11: Efficiencies and maximal junction temperature of 2-level, 3L FC, 5L FC and 5L ANPC topologies for DC voltage parametric sweeps

The high voltage components that are used for the 2-level topology have more switching losses due to their properties and also to the high switching frequency which is lower for 3 and 5-level topologies.

The 2-level topology maximal temperature is higher than the fixed thermal limit of 150°C for almost all the design point so it should not be taken into consideration. If we want to use the 2-level topology for a DC bus voltage higher than 1 kV keeping the temperature lower than the fixed thermal limit, we should reduce the switching frequency from 4 kHz to 800 Hz.

In the other hand, High-level topologies have better efficiencies than 2-level one and still have an acceptable junction temperature.

VI. CONCLUSION

The first step of this project was to define the DC bus voltage. The discretization of voltage and current ratings has introduced a bias in the study. To avoid this phenomenon and to be able to design an optimal system, adapted components are generated and multilevel topologies are used. The generated components have the same properties as the real ones. For both generated and components, the optimal response is noticed for used Silicon voltage ratio of 50%.

The generation method has its limits and still to be developed in order to get a better fitting of the thermal resistors. This could be done by taking into account not only the voltage and current calibers but also the semiconductor module packaging that is different within a component's family.

Based on the voltage calibers, the small components are better than the high-voltage ones in order to reduce switching losses even if more components should be used in series in order to withstand the required voltage. The direct series association is hard to realize but seems to be the best option. That is where the multilevel architectures seem interesting.

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