

Investigating the effect of large SMD components on heating during vapour phase soldering

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Abstract— The paper presents fundamental investigations into the field of vapour phase soldering, specially focusing on the effect of large surface mounted components (e.g. shadowing and possible consequent tombstoning). During the vapour phase reflow the heat transfer processes are based on condensation and the temperature distributions are affected by the geometry and thermal masses of the heated assemblies. The paper investigates the problem from the aspect of components with high thermal mass, which may affect the process of condensation, due to their increased thermal requirements. The experimental is based on FR4 type printed circuit boards, where large packages (SMD capacitors) are attached with SMD adhesives on the top surface of the board at specified locations. The thermocouples are fixed in bores inside the PCB at given locations to highlight any possibility of shadowing (caused by condensate flow blocking effect or vapour consumption) and inside the components where any significant transient effects serve information about the process itself. The measurements are logged with a custom data logger device, which was developed specifically for the investigations. The initial results show that shadowing might not be a problem even near large components, however the overall heating characteristics of the board and the components are affected by the relatively large thermal masses of the applied packages.

Keywords— vapour phase soldering, solder profile, heat transfer, shadowing

I. INTRODUCTION (*HEADING 1*)

Vapour phase soldering (VPS) is an alternative method for reflow soldering, where the surface mounted electronic assembly (the PCB, the deposited solder, and the components) is heated by condensation of the Galden type heat transfer fluid [1]. Due to the condensation based heat transfer, not only the phase change from vapour to liquid affects the heating, but the state and flow of the filmwise condensate on the surfaces of the PCB (also on and around the surfaces of components).

The whole vapour phase soldering process with given assembly steps can be described with the help of Figure 1, where: an assembled PCB, with printed paste and placed components (steps a-c), is lowered into the vapour space of the oven, which has a dedicated zone for a saturated vapour blanket. Nowadays the state of the art VPS ovens use non-saturated vapour for better heating control, but to understand the process, the fundamental aspects must be taken into consideration. As the cold surfaces of the PCB and the components are in contact with the hot vapour, condensation forms a continuous and flowing film layer on the PCB. The phase change causes the release of the latent heat during the condensation which is transferred from the film to the solid board. The board can be considered as a horizontal plate. The heating depends on many aspects, such as the density of the heat transfer medium in vapour form, the operating specifications of the used oven, the materials used in the assembly, the surface dimensions and the consequent flow of the film layer condensate.

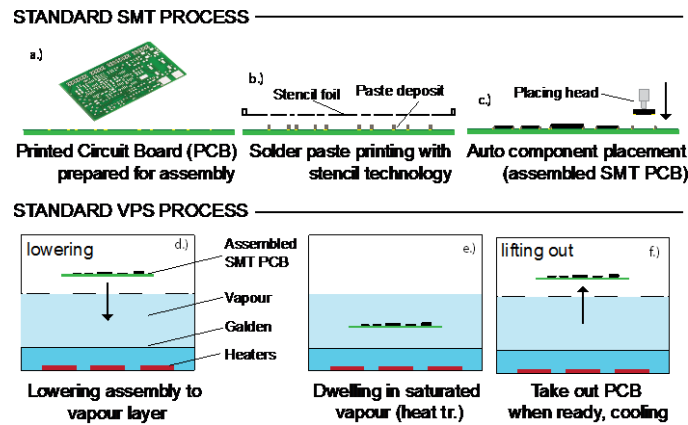


Fig. 1. Assembling (a-c) and reflow with VPS (d-f) [2]

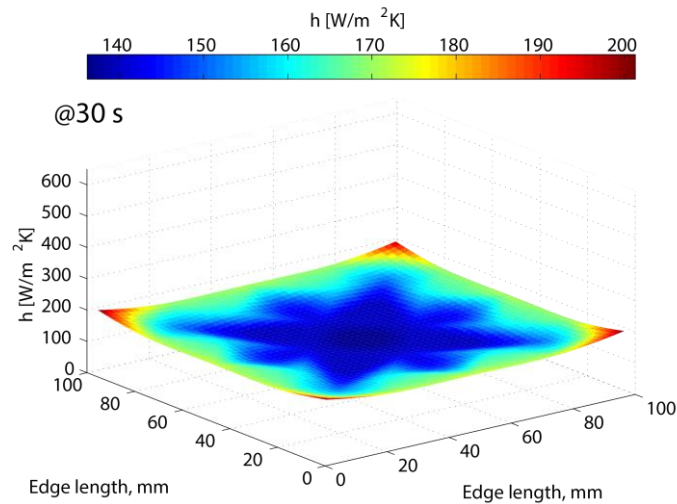


Fig. 2. Heat transfer coefficient map during VPS on a bare FR4 laminate plate [2]

While VPS is considered to be an ideal method for equalized heat transfer along the whole assembly, the flow of the condensate may cause slight temperature differences a PCB [2]. The problem is presented on Figure 2: a measurement revealed that due to the condensate layer thickness decrease and the flow velocity increase to the edges, significant differences in heating can occur between the middle and the corners/edges of the PCB.

Recent research papers explored special applications of the technology. The vacuuming VPS process was investigated by different research teams focusing on joint quality [3] [4] [5]. The results pointed to better overall joint quality with careful profile setting and void reduction with vacuum. Others inspected the microstructures of lead-free joints formed in vapour space [6] [7], where the metallic structure is affected by the vapour reflow profile. Direct investigations are focusing on the profile setting as well [8] where optimizations may also involve statistical methods too, like Grey-Taguchi [9]. The field of power electronics [10] [11] [12] [13] and research on reflow energy efficiency [14] is also actively studied field in VPS. The fundamentals of the process however are still not widely studied in the literature.

Shadowing effect of larger components can be a serious problem in electronics assembling, causing uneven heating and consequent soldering errors. In specific discussions, VPS is considered to be devoid of the problem (as Figure 3 also shows) [15] however shadowing is not yet investigated from the aspect of the condensate flow. Due to a possible blocking effect of the flow for the large packages, significant differences may occur in the heating, ultimately leading to soldering failures (e.g. tombstoning) of smaller scale SMD components surrounding the larger ones. Tombstoning is a typically reported problem [17] of the basic and moderately advanced VPS ovens, so it is important to investigate this failure possibility from practical aspects. Our paper aims to present our first experiments and analysis of gathered data from the given aspect.

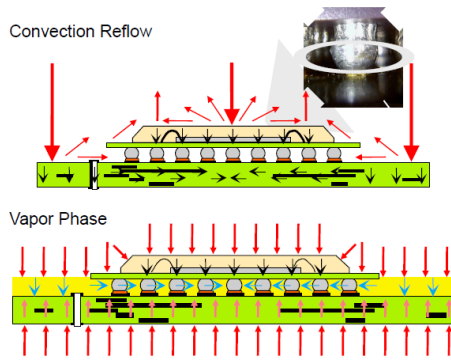


Fig. 3. BGA heat transfer with convection (up) - the component shadows out the heat flow from the solder balls, while VPS (bottom) eliminates the problem. The capillary flow enables hot Galden to flow under the component. [15]

II. EXPERIMENTAL

To investigate the shadowing effect during VPS, large SMD packages, namely LN0 (dimensions are shown on Figure 4.) and 4036 PET (length: 10.2 mm, width: 9.1 mm, height: 5.5 mm) type packages (capacitor components) were attached to the top of bare FR4 substrates (8x8 cm) with Loctite 3621 SMD adhesive. The components are presented on Figure 5. According to the heat capacity of the given components, vapour consuming and perturbing effect around LN0 type capacitor ($C_{LN0} \sim 10,5 \text{ J/K}$) must be more significant than around the 4036 type capacitor ($C_{4036} \sim 0,035 \text{ J/K}$).

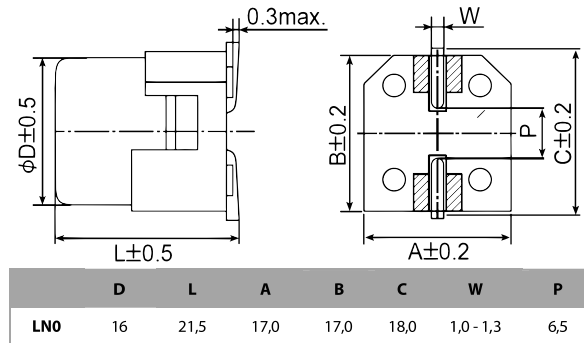


Fig.4. LN0 component dimensions



Fig.5. LN0 (left) and 4036 (right) sized SMD capacitors.

The component positions were chosen according to the flow direction on the board from the center to the edges. The components are placed along one bisecting line of the PCB along Y axis. The board surface is 100x100 mm, the thickness of the laminate is 1.5 mm. Three component positions are defined, A, B and C, where the distances from the center of the board to the center of the components are consequently 15, 25 and 35 mm. The component distances are identical for both types, where the distance is calculated between the center of the board and the center of the components. Two distinctive batches of thermocouples are 1-5 and 6-10, (according to the two components per setup) are presented. Figure 6 b.) also denotes the supposed flow direction of the condensate from the center to the edges. It is supposed that a flow is present on the components, however at this point the effect of this phenomenon is less significant than the flow on the board.

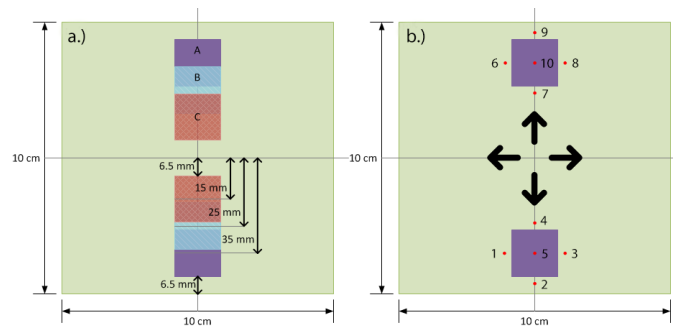


Fig.6. a.) Component placement at A, B and C positions with dimensions; b.) locations and numbering of thermocouples around and inside the components.

Figure 6 a.) and b.) presents the setup with the positioning and numbering of the thermocouples. The thermocouples are placed ~5 mm from the edges of the components. For the investigation, K-type thermocouples were used. They are attached into the middle of the components (in drilled blind vias) from the bottom side of the PCB. (Operating range: -75°C to $+250^{\circ}\text{C}$; precision: $\pm 1^{\circ}\text{C}$). The wire leading was solved from the bottom side of the board to minimize perturbing the vapour above the assembly. The four thermocouples around the component serve in mapping the heating differences in the near vicinity. With the setup shown on Figure 6, and assuming that the flow of the condensate usually points from the center of the board to the edges, this setup should reveal possibilities of shadowing (flow alteration around the component) during heating. Figure 7 shows the thermocouple attachment to the bare FR4 PCB laminates (which were used as a flat, horizontal plate for the experiment) The fixing was also investigated with X-Ray analysis (Fig 7. b.) with oblique scanning angles, to ensure that the non-insulated wire ends near the welded spot were separated without any possibility of shorting.

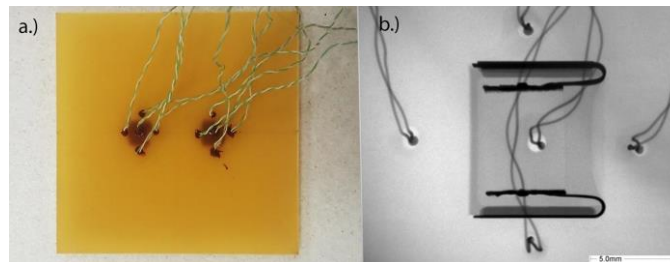


Fig.7. a.) Thermocouple attachment to the assembly and b.) X-Ray analysis of fixed TCs in 4036 SMD capacitor.

The assembly is immersed into an experimental VPS system with HT170 Galden (boiling point: 170°C), enabling faster measurement cycles than standard LS230 types. HT170 is also relevant from the aspect of reflow soldering with SnBi type alloys ($\sim 138^{\circ}\text{C}$ melting point).

To ensure best performance during measuring at such high amount of channels, the deviance of batched thermal DAQ loggers was avoided with a custom developed measurement system, which uses an LTC2983 component and enables measurement of ten channels for K-type thermocouples. The system connects to a PC where data is logged via USB. The assemblies were positioned in the vapour space on a sample holder fixture, with ICT needles serving as support with minimal heat coupling. The fixture was aligned to a horizontal position with a Clinometer ($< 1^{\circ}$ error). For each component position setup (A-B-C), three measurements were recorded and averaged with careful time point synchronizing. The temperature measurement results were analyzed at time points of the transient plots at given select temperatures (100 and 138°C)

III. RESULTS

Figure 8 presents a temperature measurement analysis of the heating up of the experimental PCB assembly with LN0 component at position B. It is apparent that the two component temperatures (plot no. 5 and 10) are much slower than the heating of the board positions. Around 100°C , the transient plots are still in a fast rise, while at 138°C the temperature is relevant from the aspect of the melting point of the SnBi type lead-free alloy suitable for the used Galden (HT170). With this temperature the results can be connected to tombstone failure origins.

As Figure 8 shows, significant time differences appear after 130°C in the given case in the transient plots.

Also note that slight differences are recognizable between given close batches of thermocouples (1-5; 6-10). It was shown in [16] that heat transfer in VPS constructions are extremely sensitive for any inclination of the soldered board. So slight transient differences between the temperature profile of the two components (the two distinctive batches of thermocouples) may occur due to sub-degree imprecisions of the sample holding.

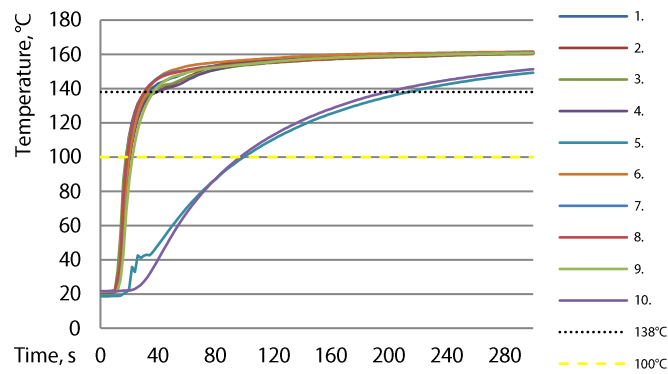


Fig. 8. Select temperature run of components (5,10) and PCB temperatures (1-4, 6-9) according to Figure 6. Two selected temperature lines are highlighted: 100 °C and 138 °C.

Figure 8 shows the time investigation from ambient temperature to 100 °C with LN0 component from A to C cases respectively. It can be seen that at 100 °C the transients are running close to each other and the plots suggest that no significant and consequential differences are observable between the inner sides or the outer sides of the components, considering the direction of the flow. However, it was found, that the outer points (eg. 2 and 9 – according to Fig. 6.b) are a bit faster compared to their pairs (2-4; 7-9). This effect may be due to the nature of the flow (where the film layer is the thickest in the middle and the thinnest at the edges). Also it can be assumed, that the flow from the center is shadowed, allowing thinner layer (meaning faster recondensation and heating) at these outer points. However the observed delta 1-4 seconds are observable on point pairs parallel with X axis like (1-3 and 6-8) as well, possibly suggesting that the measured differences are near to the precision of the used measurement setup.

Figure 9 shows the investigation from ambient to 138 °C with LN0 component from A to C cases respectively. A similar phenomena is observable as in the case of Figure 8, however the differences are a bit more significant. Please note that for B positioning, the slightly higher differences are due to a run where inclination effects may occurred.

Also the differences between the component transient times can be accounted to slight inclinations and the relatively high thermal capacities of the LN0 components.

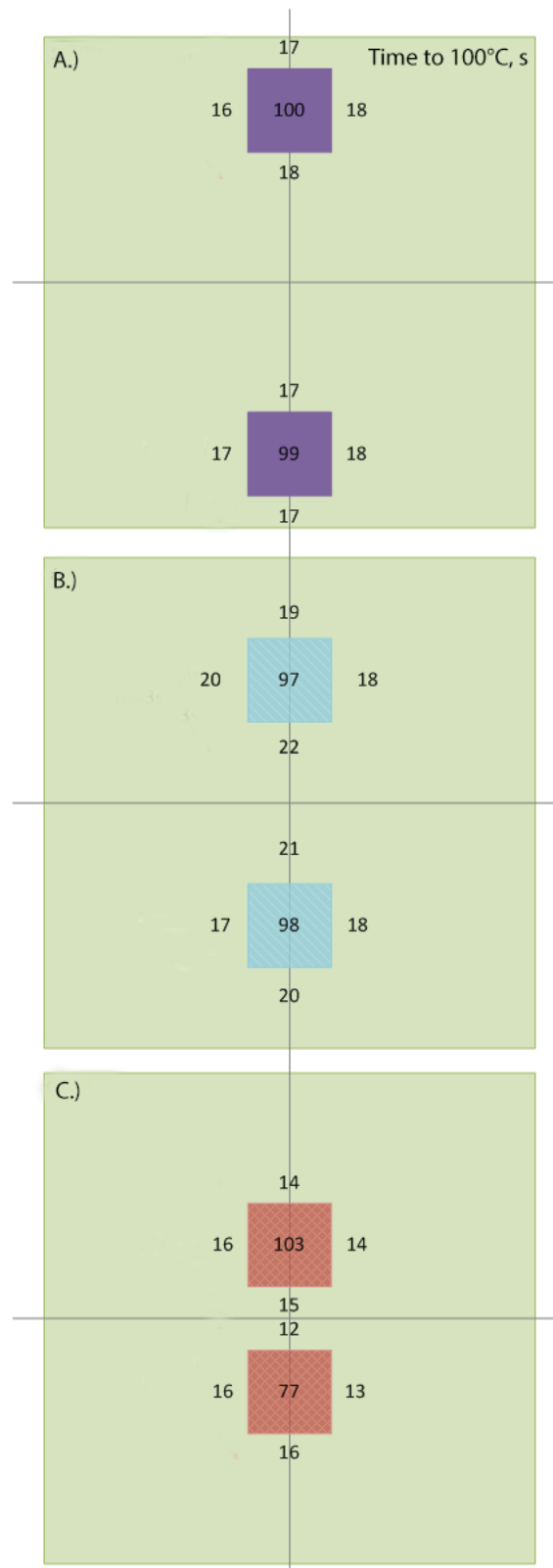


Fig. 9. Investigation of transients (time, s) from ambient to 100°C on and around LNO type of components

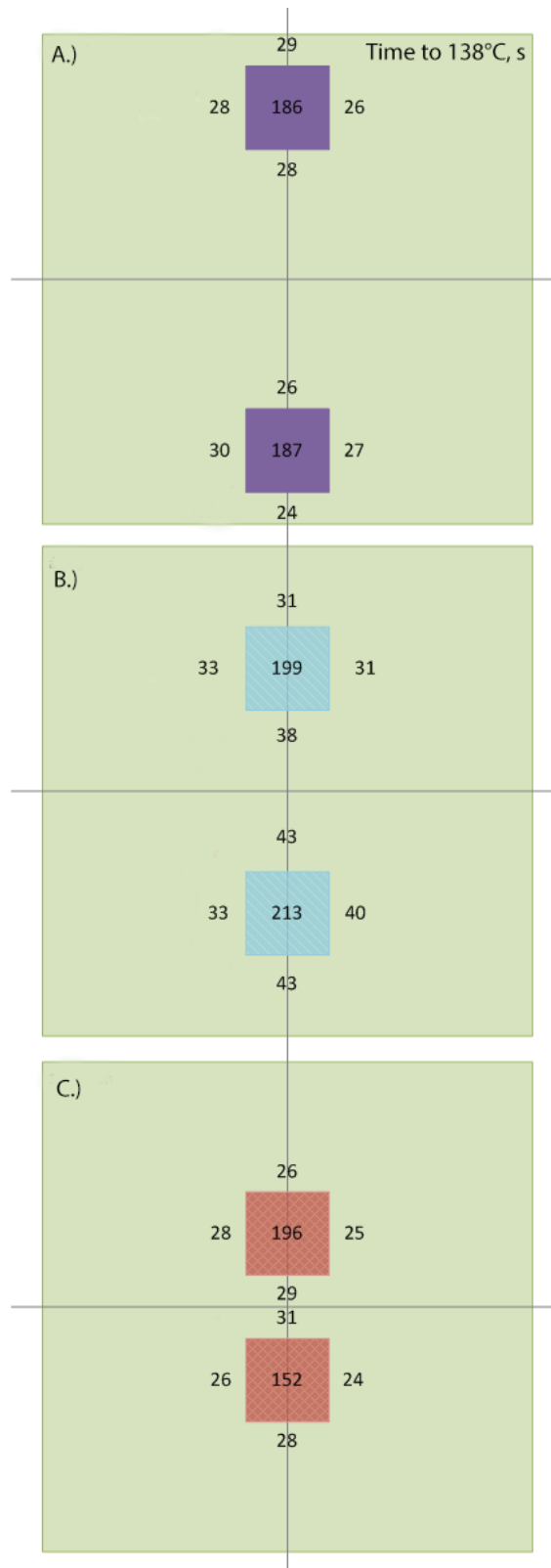


Fig. 10. Investigation of transients (time, s) from ambient to 138°C on and around LN0 type of components

Summing up: while there is observable time differences on transients at the selected temperatures, the temperature measurement precision and the physical nature of the setup with a possibility of sub degree inclinations, are limiting finer discussion of the results.

It seems that while the heat transfer to the component surroundings are definitely affected by the components, it is not clearly denoted, whether the differences are due to the perturbation of the flow in the condensate layer by the large size components or the uneven consuming and reproduction of the vapour layer around the components.

The investigations were performed with 4036 type components as well, where Figure 11 is discussing the obtained results in summarized manner focusing on one select example (position B). Other positions yielded similar results.

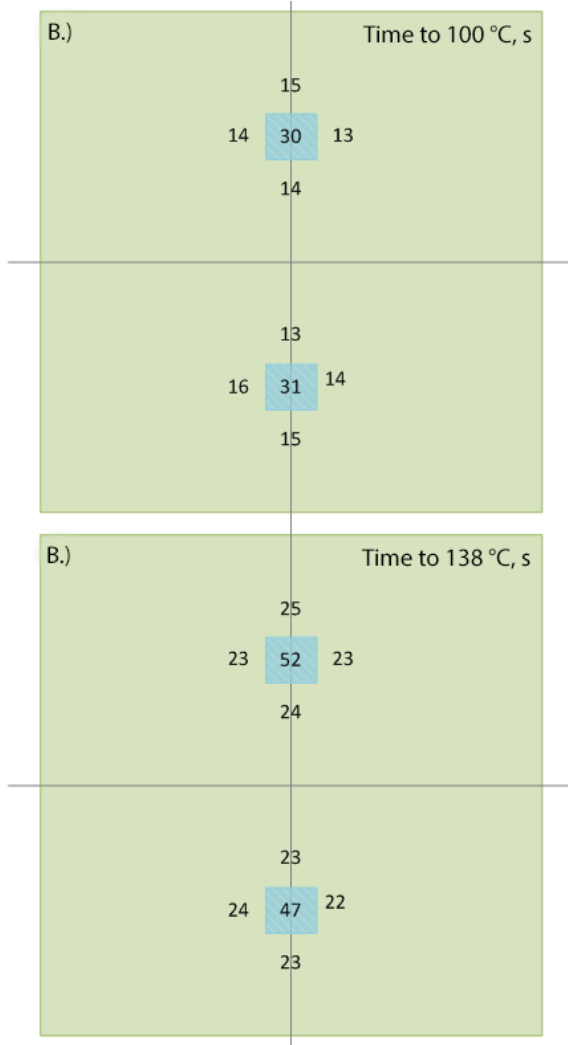


Fig. 11. Investigation of transients (time, s) from ambient to 100°C (top) and 138 °C (bottom) on and around 4036 type components (B position)

On Figure 11, the results of B positions are highlighted – it is shown that the transient time differences reaching the given time points have similar delta values as in the case of LNO components. However it was consequently also shown that due to the smaller component size and much smaller thermal capacitance of 4036 SMD capacitor, slightly smaller differences in the transients of component and board temperatures can be observed. While differences of thermocouple pair transients surrounding the LNO were around 1-7 seconds, the differences are consequently around 1-2 seconds around the 4036 components. It is supposed that the larger overall thermal capacity of the LNO component may cause local perturbing in the vapour around the component, causing more uneven heating and uneven condensation around them. Also, the larger heat capacity means more intense condensation on the components, so that the condensate which is flowing down from the large components may also affect heat transfer more significantly in the surroundings.

IV. CONCLUSION

Overall, it was shown that the transient differences around the components are detectable, but not in a clear and significant manner with classical measurement techniques (thermocouples, data logging). Clear correlation between shadowing and these differences can not be concluded, while the noted differences are hard to characterize with measurement approach; any side effect (e.g. a slight sub-degree inclination of the board) may slightly perturb the heating, introducing any non-wanted, but detectable differences. It was found that the differences were actually less significant around the components with smaller geometry and thermal

capacity. It is supposed that around even smaller components (such as chip size capacitors), the effect would be practically non-detectable.

However for larger components, differences are still present, and point to more precise requirements for future investigation. The given experiment highlights the serious sensitivity of VPS for physical characterization of the process. So, our work aims for further analysis of the matter with simulation approach. As it was noted, a few seconds of transient difference during rapid heating may be critical around the melting point of the solder alloy, causing failures with the joined components. To further investigate the differences (eg. to avoid tombstoning at small scale chip resistors around larger components like LNO) modelling methodology is aimed for future considerations.

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