

## Component level modelling of heat transfer during vapour phase soldering with finite difference ADI approach

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### Abstract

In this paper the complex heat transfer process of the vapour phase soldering has been investigated on the level of electronic components. VPS is gaining increased attention lately, and the process needs different approach of modelling, compared to conventional soldering processes in electronics mass manufacturing. Component level modelling was not studied deeply in the literature before, so our focus pointed to heat transfer on large size surface mounted electronic components. Applying the Fourier type heat conduction equation, a detailed 3D thermal model of a polyester capacitor on a printed circuit board was implemented based on x-ray images of an actual assembly. Our model incorporates inner geometry, material inhomogeneity, composite materials and anisotropic thermal conductivity as important thermal features. Transient heating was calculated with Finite Difference Method combining an alternating direction implicit (ADI) approach, using averaged heat transfer coefficient. Validation measurements were taken in our VPS system. The measured data show good agreement with the calculation results and points to possible application for use in advanced engineering environment.

### Keywords

Vapour phase soldering; Condensation; Thermal simulation; 3D ADI; Component modelling

### 1. Introduction

Vapour phase soldering (VPS) is a reflow soldering method used in electronics manufacturing. It is an alternative to the widely used forced convection and nowadays less significant infrared heating processes [1-3]. During reflow soldering, solder paste is printed onto the pads of the printed circuit board (PCB), and then the electrical components are positioned and placed onto the deposits of the solder. The solder alloy is then melted by heat to form solder joints. In case of infrared or forced convection heating, electromagnetic radiation or hot air stream is responsible for energy transfer, respectively. On the contrary, during VPS process a special heat transfer fluid is boiled to form a saturated vapour in closed space. The PCB assembly is immersed into the saturated vapour, indicating condensation on the assembly surface. The latent heat of the condensation provides energy for heating, while a continuous condensate film is formed. Then heat transfer occurs through this thin layer on the surface. Nowadays the most widely used fluid in VPS applications is called Galden (perfluoropolyether – PFPE type fluid), which is considered as an inert material, and do not produce any harmful gases during the process. The main advantages of VPS technology are rapid heating, the reduced risk of overheating, due to the fixed boiling point of the fluid, and the oxygen-free environment. Oxidation-free solder joint forming is achieved due to the presence of continuous condensate film layer.

VPS is studied mainly from the practical aspects originated from the needs of the industry, such as the aspect of soldering with lead-free materials [4]. The general comeback of the method was described in [5]. Recently VPS was compared directly with more conventional convection type reflow by Dziurdzia [6], while the others focused more solely on VPS. It was

found by Pietrikova [7] and Liu [8] that the microstructure of the joints formed in VPS ovens are dependent of the given setting and mode of the applied ovens.

Real time temperature profiling [9] or optimizations with statistical methods [10] were also investigated by Livovsky and Tsai, respectively. Power electronics manufacturers utilize VPS due to the efficient soldering of large components [11-16]. Research of the energy efficiency is also under active investigations [17]. Special applications, such as Pin-in-Paste technology [18] or vacuum suctioning during reflow also fits in the focus of VPS studies. It was found by Synkiewicz [19] and Lungen [20] that VPS process with a vacuum step, after reflowing the solder alloy, is effective in eliminating voids and improving joint quality.

In the last few years, the process of VPS itself was also investigated on multiple levels. The basics of saturated vapour generation, condensation and film layer formation were investigated through detailed multi-physics modelling. Also, simpler models were applied to describe the heating of PCBs as 2D objects [1-2]. Continuing this line of research, we introduce 3D thermal modelling on component level during VPS. Modelling of electronic assemblies was presented recently for infra-red radiation based heat transfer on board level by Najib [21] and convection type heat transfer during reflow on component (package) level by Deng [22]. We considered a novel approach for VPS regarding inner geometry, material inhomogeneity, composite material content and anisotropic thermal conductivity. These component level aspects were not widely studied together in case of VPS before. We used the finite difference method with alternating direction implicit scheme (FDM ADI) due to its highly customizable implementation possibilities and computation speed.

The proposed method may be able to reveal different quality aspects (such as failures during assembly), and an extension of overall knowledge on the process of VPS.

## 2. Experimental

### 2.1 VPS system and component specification

To prepare verify and fine tune our proposed model, several measurements were carried out in an experimental model VPS system, which was described in our previous work [23]. A simplified overview is shown on Fig. 1. The system is based on a closed stainless steel tank with a removable lid. An immersion resistor heater boils the Galden fluid at the bottom. A cooling tube circuit is positioned on the top of the tank with circulated ambient temperature water inside. In our experiment Galden HT170 [24] with 170 °C nominal boiling point was used to form saturated vapour blanket with the same temperature. The material is exchangeable with higher temperature fluids.

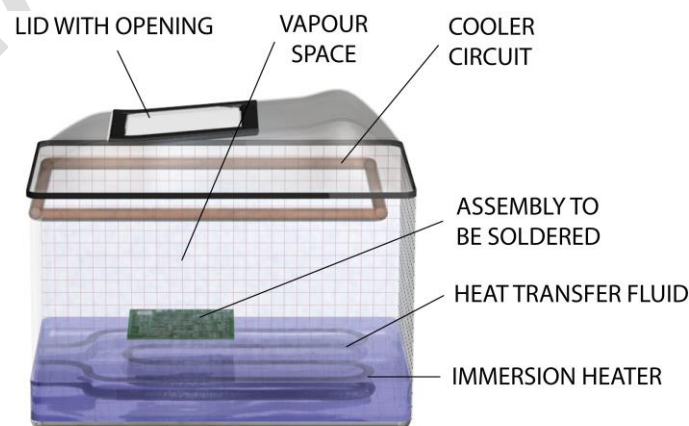


Fig. 1 – Experimental VPS system with electronic assembly immersed in vapour space

For modelling purposes, we chose a multilayer polymer (MLP) surface mount (SMD) capacitor (4036, 5.5x10x9 mm). In MLP capacitors the core is constructed of metal film electrodes with a dielectric material (polyethylene terephthalate (PET) in our case) sandwiched in between. The metal film layers and contact metallization are made of aluminium (Al); the film layers are 100-300 Angstrom thin, while the dielectric layers have the thickness between 0.9-1.2  $\mu\text{m}$ . These extremely thin film layers make possible to stack several thousand layers to form the capacitor core, which is encapsulated in epoxy case (epoxy encapsulant and thin plastic box) with Al contact termination on both sides. The MLP capacitors are popular in high frequency applications [25-26].

We used XiDAT XD6600 x-ray microscope imaging to chart the build-up and inner geometry of the capacitor, where the results can be seen on Fig. 2.

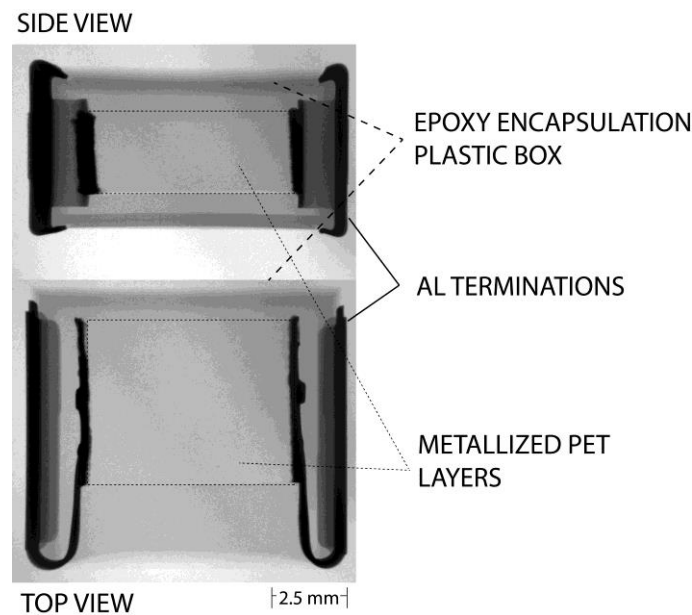


Fig. 2. - X-ray images of the capacitor's inner structure with highlighted core (top: side view, bottom: top view)

Two capacitors were assembled onto a bare laminate 1.6 mm thick PCB of FR4 (standard PCB material) with  $\sim 60 \mu\text{m}$  thick layer of epoxy adhesive (Loctite 3621 [27]) between the component and the PCB. The PCB was 10 cm x 10 cm in size, and the capacitors were 5 cm apart from each other. From the PCB side a small bore of 0.5 mm diameter was prepared through to the center of the capacitors. A 0.2 mm thin K-type thermocouple ( $\pm 1 \text{ }^\circ\text{C}$  precision) was positioned into each bore with aforementioned epoxy adhesive. The adhesive gives good thermal coupling, enabling accurate temperature monitoring of the surrounding body. Later, the measurements will be used for verification of the FDM model with averaged transient temperature data of the two capacitors.

We also measured the time delay between the beginning of the condensation and the temperature rise in the center of the capacitors. An additional thermocouple was attached 1 cm below the board to indicate the start of the process.

The average heat transfer coefficient of the condensation process was derived from the transient heating curve of a bare PCB as an approximation. Multiple thermocouples with different positions were placed into the board with the same technique as described above. The heat transfer coefficient was obtained from the averaged data using lumped system calculation. For our model, we assumed that the capacitor is heated with the same average heat transfer coefficient as the PCB.

All material properties we used in our calculations can be found in Table 1.

Table 1

Properties of base materials in the capacitor model [27, 34, 39-44].

	$\rho$ [kg/m <sup>3</sup> ]	$c$ [J/(kg °C)]	$\lambda$ lateral [W/(m °C)]	$\lambda$ vertical [W/(m °C)]
PET (1 $\mu$ m layer)	1400	1200	0.1	0.1
FR4	2100	600	0.76	0.53
Epoxy encapsulant + plastic box	1900	1100	0.5	0.5
Epoxy adhesive (60 $\mu$ m layer)	1160	300	0.3	0.3
Al (bulk)	2700	900	210	210
Al (120 Angstrom layer)	2000	900	20	20

## 2.2 Average heat transfer coefficient during condensation

The heat transfer coefficient of the condensation can be calculated from transient temperature data if the interior temperature of the body remains nearly uniform during the heating process with lumped (concentrated) system modelling [28-29]. It was shown previously, that PCB plates can be treated such way in most cases [2]. The lumped model is written as [28-29]:

$$c \cdot m \cdot \frac{dT}{dt} = h \cdot A \cdot (T_{sat} - T) \quad (1)$$

where  $c$  [J/kg °C] is the specific heat capacity,  $m$  [kg] is the mass,  $t$  [s] is the time,  $h$  [W/(m<sup>2</sup> °C)] is the heat transfer coefficient,  $A$  [m<sup>2</sup>] is the total heated surface,  $T$  [°C] is the temperature of the body and  $T_{sat}$  is the temperature of the saturated vapour.

When the temperature changes with time only and the other variables are considered to be constant, the analytic solution of Eq. (1) is:

$$T(t) = T_{init} + (T_{sat} - T_{init}) \cdot \left( 1 - \exp\left(-\frac{t \cdot h \cdot A}{c \cdot m}\right) \right) \quad (2)$$

where  $T_{init}$  is the initial temperature of the body.

We fitted Eq. (2) to the measured heating transient data of the PCB using weighted least squares method. The results are shown in Fig. 3 with  $h=240$  W/(m<sup>2</sup> °C) which can be accounted as the average heat transfer coefficient during the condensation process.

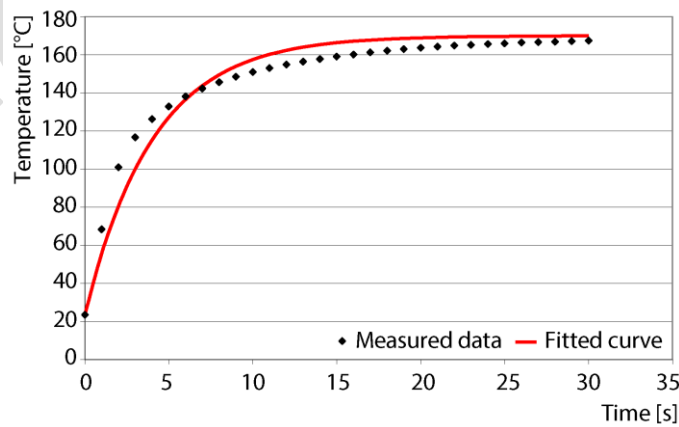


Fig. 3. - Averaged transient heating curve of the PCB.

During the first few seconds the fitted curve underestimates, later exceeds the measurement data. In the very beginning, for a small (<1 s) time interval actual heat transfer coefficient can jump up to ~320 W/(m<sup>2</sup> °C). This is correlated with the initial lack of the condensate film layer, which boosts heat transfer when the cold PCB is inserted into the vapour space. After it is quickly formed, the layer serves as a thermal barrier during the rest of the process, lowering the heat transfer efficiency. These values agree well with previous works [2-3], and clearly show the rapid heating capability of the VPS.

The validity of lumped system modelling is generally accepted for all geometries when the Biot number is below 0.1 as a rule of thumb [28-29]. For a plate that is heated from both side, the Biot number is given by [29]:

$$Bi = \frac{h \cdot L}{2 \cdot \lambda} \quad (3)$$

where  $L$  [m] is the thickness and  $\lambda$  [W/(m °C)] is the thermal conductivity of the plate. In our case  $Bi \sim 0.3-0.4$  and we used the 1D analytic solution of the interior temperature distribution to approximate the error of the uniform heating assumption. In a plate that is heated by saturated vapour with constant heat transfer coefficient, and the dominant heat flows perpendicularly to the surface, the interior temperature is given by [29]:

$$\frac{T(t) - T_{sat}}{T_{init} - T_{sat}} = \frac{4 \cdot \sin \sigma}{2 \cdot \sigma + \sin(2 \cdot \sigma)} \cdot \exp\left(-\sigma^2 \cdot \frac{\lambda \cdot t}{c \cdot \rho \cdot (L/2)^2}\right) \cdot \cos\left(\frac{\sigma \cdot x}{L/2}\right) \quad (4)$$

where  $\sigma$  is the first root of  $\sigma \cdot \tan(\sigma) = Bi$ ,  $\rho$  is the density [kg/m<sup>3</sup>],  $-L/2 \leq x \leq L/2$  [m] is the inner spatial position perpendicularly to the surface. The equation is valid in the time domain where the Fourier number  $Fo = (\lambda \cdot t) / (c \cdot \rho \cdot (L/2)^2) > 0.2$ . This value is ~0.27 s in our case. We defined the error as percentage of the maximal deviation from the average temperature in the plate. Calculations were carried out with  $T_{sat} = 170$  °C and  $T_{init} = 25$  °C. For  $Bi < 0.1$ , the error remains under 10% for the whole transient. For  $Bi \sim 0.3-0.4$ , it grows up to 35% during the first 1 s duration, but decreases to 10% after 2 s and shows rapid decline afterwards. Consequently, the lumped system modelling is still acceptable for the PCB in our experiment. While the error may be significant at the beginning of the investigated time window, it is reduced insignificant at the practical regions around the actual melting point temperature for selected solder alloys. (For example: Galden HT170 fluid combined with 58Bi42Sn alloy of 138 °C melting point.)

### 3 Applied finite difference model

#### 3.1 ADI scheme for non-homogeneous material

Heat penetration into the body can be described with the Fourier type heat conduction equation. In 3D, it has the expression [28-31]:

$$\rho \cdot c \cdot \frac{\partial T}{\partial t} = \frac{\partial}{\partial x} \left( \lambda \cdot \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( \lambda \cdot \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( \lambda \cdot \frac{\partial T}{\partial z} \right) \quad (5)$$

where  $x$ ,  $y$  and  $z$  refer to the Cartesian dimensions. Compared to the lumped system, the interior spatial temperature change is now part of the calculation.

To solve this equation with FDM we used the effective Douglas-Gunn Alternating Direction Implicit (DG ADI) scheme, where the implicit equations are solved separately along each dimension in 3 phases [30-33]:

$$\left(1 - \frac{1}{2} \cdot S_x \delta^2\right) \cdot \blacklozenge T_{ijk}^{n+1} = \left(1 + \frac{1}{2} \cdot S_x \delta^2 + S_y \delta^2 + S_z \delta^2\right) \cdot T_{ijk}^n \quad (6)$$

$$\left(1 - \frac{1}{2} \cdot S_y \delta^2\right) \cdot \blacklozenge\blacklozenge T_{ijk}^{n+1} = -\frac{1}{2} \cdot S_y \delta^2 \cdot T_{ijk}^n + \blacklozenge T_{ijk}^{n+1} \quad (7)$$

$$\left(1 - \frac{1}{2} \cdot S_z \delta^2\right) \cdot T_{ijk}^{n+1} = -\frac{1}{2} \cdot S_z \delta^2 \cdot T_{ijk}^n + \blacklozenge\blacklozenge T_{ijk}^{n+1} \quad (8)$$

where  $i, j$  and  $k$  are step indexes of the thermal nodes along the Cartesian dimensions, and the  $n$  index stands for the time-step. The  $\blacklozenge T^{n+1}$  and  $\blacklozenge\blacklozenge T^{n+1}$  values are gradual approximations to the real  $T^{n+1}$ , as Eq. (6) is a predictor phase followed by two correction phases in Eq. (7) and (8). The  $S_x \delta^2$ ,  $S_y \delta^2$  and  $S_z \delta^2$  symbols are operators for central second difference with respect to the material inhomogeneity. For  $x$  dimension, it gives:

$$S_x \delta^2 \cdot T_i = S_i^- \cdot T_{i-1} - (S_i^- + S_i^+) \cdot T_i + S_i^+ \cdot T_{i+1} \quad (9)$$

where  $S_i^+ = (\lambda_i^+ \cdot \Delta t) / (\rho_i \cdot c_i \cdot \Delta x^2)$ ,  $S_i^- = (\lambda_i^- \cdot \Delta t) / (\rho_i \cdot c_i \cdot \Delta x^2)$ ,  $\Delta x$  is the spatial and  $\Delta t$  is the temporal step size, respectively. Also,  $\lambda_i^+ = (2 \cdot \lambda_i \cdot \lambda_{i+1}) / (\lambda_i + \lambda_{i+1})$  and  $\lambda_i^- = (2 \cdot \lambda_i \cdot \lambda_{i-1}) / (\lambda_i + \lambda_{i-1})$  are harmonic mean values and serve as the intermediate thermal conductivity between the right and left adjacent nodes. They describe abrupt material changes at the interfaces, which appear in thermal RC network modelling [34]. The  $y$  and  $z$  dimensions can be treated in the same way.

Applying Eq. (6), (7) and (8) along with the boundary conditions to all nodes using continuous indexing result in a system of simultaneous (implicit) equations in every phase. It can be expressed with matrices in the general form of  $\underline{\underline{A}} \cdot \underline{T}^{n+1} = \underline{\underline{B}} \cdot \underline{T}^n + \underline{C}$ , where double underline refers to square matrices and single underline represents column vectors. The system can be solved by Gaussian elimination to yield the unknown  $\underline{T}^{n+1}$  vector.

All three equations have only one three-point central second difference term on the left side. Thus, with reordered node indexing, it is possible to construct simple tridiagonal matrices to solve in each phase. As a result, this method provides very fast computation even with high node count. The truncation error of the DG ADI scheme is  $O(\Delta t^2, \Delta x^2, \Delta y^2, \Delta z^2)$ .

### 3.2 Composite materials and anisotropic heat conduction

Besides common base materials like aluminium or epoxy, practical thermal modelling requires the application of composites. In our case, we approximated the FR4 PCB with epoxy adhesive and the capacitor core in this way. Volume and mass fraction were used to obtain the density and heat capacity values of the composite, respectively [35-36], according to Table 1. Moreover, layered structures can be modelled with orthotropic anisotropy, where the heat conduction independently differs along each dimension. Hence, the vertical and lateral heat conduction values can be calculated using the series and parallel models [37-38].

Note that, the ultra-thin Al layers in the capacitor core were treated with separate properties from its bulk variant, as shown in Table 1. Literature data pointed out that the thermal properties, mainly the heat conductivity of metal thin films show considerable decrease from the bulk value below  $\sim 100$  nm thickness [39-43].

### 3.3 Boundary conditions for VPS process

To describe the heat transfer to the surface of the body we used Robin type boundary conditions. For  $x$  dimension and interior domain  $0 \leq x \leq L$ , the boundary conditions are [28-31]:

$$\left. \frac{\partial T}{\partial x} \right|_{x=0} = -\frac{h}{\lambda} \cdot (T_{\text{sat}} - T_{\text{srf}}) \Big|_{x=0} \quad (10)$$

$$\left. \frac{\partial T}{\partial x} \right|_{x=L} = \frac{h}{\lambda} \cdot (T_{\text{sat}} - T_{\text{srf}}) \Big|_{x=L} \quad (11)$$

To keep  $O(\Delta x^2)$  accuracy, we used centered difference with ghost nodes to discretize the boundary conditions. Thus, the central second difference operator can be applied to the boundary nodes as:

$$S_x \delta^2 \cdot T_i \Big|_{x=0} = -(2 \cdot S_i^+ + 2 \cdot H_i) \cdot T_i + 2 \cdot S_i^+ \cdot T_{i+1} + 2 \cdot H_i \cdot T_{\text{sat}} \quad (12)$$

$$S_x \delta^2 \cdot T_i \Big|_{x=L} = 2 \cdot S_i^- \cdot T_{i-1} - (2 \cdot S_i^- + 2 \cdot H_i) \cdot T_i + 2 \cdot H_i \cdot T_{\text{sat}} \quad (13)$$

where  $H_i = (h_i \cdot \Delta t) / (\rho_i \cdot c_i \cdot \Delta x)$ . The boundary points along  $y$  and  $z$  dimensions can be treated similarly.

The PCB carrier is also part of the thermal structure. To limit the size of the model we used only the part directly under the capacitor (Fig. 6 - bottom layers). Boundary conditions must be assigned to the side planes of the fictitious board cut-out. We assumed that the lateral heat distribution is locally homogeneous during the simulated time interval and the heat flow through the side planes can be neglected. Thus, we used  $\partial T / \partial x = 0$  and  $\partial T / \partial z = 0$  as boundary conditions on these surfaces by choosing  $h = 0$ . Similar technique was used in [34].

During calculation, we neglected the convection and radiation heat loss because they are estimated to be at least one order of magnitude lower than the heat coupled by the heating process [34].

### 3.4 Programming considerations and stability

For best correlation with the measurement, the material properties listed in Table 1 were adjusted in their generic domain in agreement with the MatWeb database [44], other literature data and the information received from the component manufacturer.

The simulation was written in Matlab environment. We applied the built-in tridiagonal solver for Gauss elimination and used sparse matrices to decrease the memory demand, also double words for variables to minimize rounding error. Two models were built with distinct spatial resolution, shown on Fig. 4. The low definition variant works with the minimal resolution to represent the inner physical structure of the capacitor and contains 5985 thermal nodes ( $\Delta x = \Delta y = \Delta z = 0.5$  mm). The high definition variant contains 84456 thermal nodes ( $\Delta x = \Delta y = \Delta z = 0.2$  mm) to investigate the effect of higher spatial resolution and slight structure refinement. We accounted the transient data of the thermal node nearest to the position of the thermocouple sensing point as the simulation result.



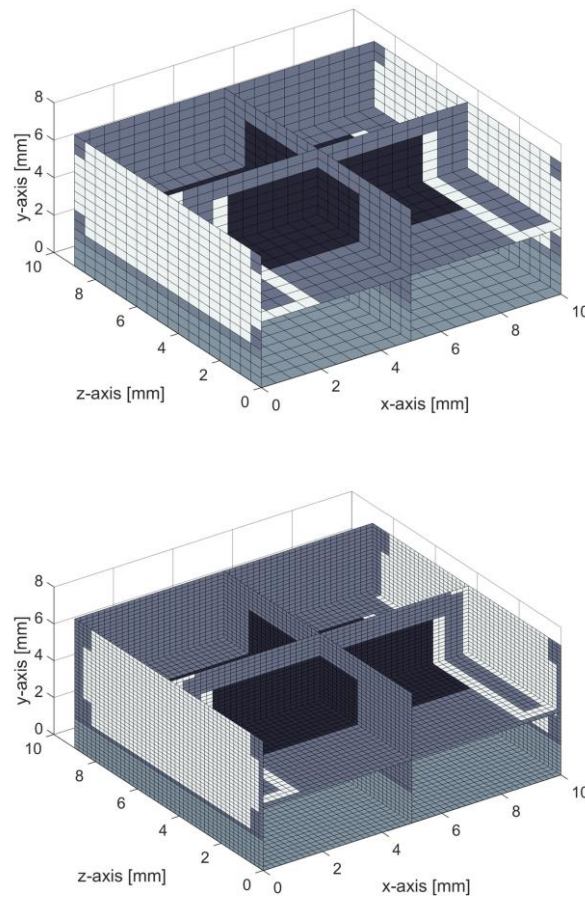


Fig. 4. - Finite difference capacitor models containing 5985 thermal nodes (top) and 84456 thermal nodes (bottom). Inner structure is shown. Lateral axes:  $x$ ,  $z$ ; vertical axis:  $y$ .

As claimed by the von Neumann stability analysis, the DG ADI method is unconditionally stable with constant coefficients [30-31]. However, material inhomogeneity indicates variable coefficients, which terminates the symmetry at the material interfaces and causes conditional stability [45]. We determined the stable time-step sizes heuristically. Stable solution was found when  $\Delta t < 0.8$  s for the low definition model and  $\Delta t < 0.1$  s for the high definition model. For increased accuracy, we used  $\Delta t = 0.1$  s and  $\Delta t = 0.05$  s, respectively for each solution. The simulated time interval was 150 s with calculation duration 17 s for the low and 19 min for the high definition model.

## 4. Results and discussion

### 4.1 Transient heating curves and node count evaluation

According to our measurement, the time delay between the beginning of the condensation and the onset of temperature rise in the center appeared to be  $\sim 4$  s. It corresponds to the speed of heat propagation into the solid, which is characterized by the thermal diffusivity, i.e.  $\lambda/(\rho \cdot c)$ , of the assembly. During simulation, the process starts with the first time-step, and the measured transient curve should be shifted with this delay for valid fitting with the calculated results.



The initial condition was 25 °C uniform temperature in the whole assembly. The  $T_{sat}$  temperature of the saturated vapor is equal with the boiling point of the heat transfer fluid. By our experience, the Galden HT170 has less than 7% boiling point drift around the nominal value, usually between 165 °C and 181 °C according to the state and usage of the Galden. Simulation results of both models, with  $T_{sat}=174$  °C and  $h=240$  W/(m<sup>2</sup> °C) for all free surfaces, are compared to the measurement data on Fig. 5 as a validation. Temperature curve of the center of the Al termination is also included.

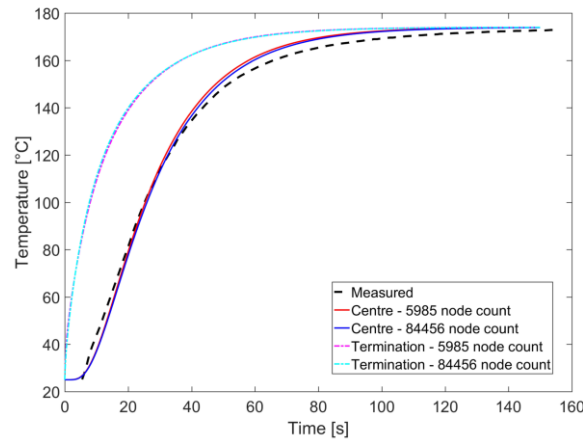


Fig. 5. - Calculated transient heating curves for the central region of the capacitor, and the center point of the termination.

Both models were capable to suitably reproduce the measured temperature transient. The differences between the results of the low and high definition models are appeared to be negligible, suggesting strong convergence with little spatial and temporal grid dependency.

We got similar agreement with the measurement for different saturation temperatures caused by boiling point drift. This indicates that using the average heat transfer coefficient predicted by the PCB is also appropriate for components of given size on the board with acceptable limitations. Also, the calculated transient underestimates the measured data in the beginning, and exceeds it near the saturation temperature. As in Chapter 2.2, this indicates higher heat transfer coefficient at the start, which decreases during the process. It is clear, that the capacitor assembly does not act like a lumped system during rapid heating. Under the given circumstances, its thermal behaviour should be modelled with distributed physical parameters, as presented here.

For further investigations, we used the high node count model.

#### 4.2 Temperature mapping in 3D

As an overview, Fig. 6 shows the 3D temperature distribution of the capacitor as time evolves during the heating process. At  $t=1$  s, the free peaks and edges experiences the highest temperature elevation, which is the consequence of the outer rectangular geometry. The Al terminations can conduct the heat to the inner region that is relatively well insulated from other directions, because of the weak heat conduction ability of the epoxy encapsulation material. Thus, the terminations and the interior body show little temperature rising in the beginning. After 10 s, the terminations have comparable temperature as other parts of the surface, but the interior region remains considerably colder. A very large temperature gradient can be observed across inner and outer regions of the assembly. At  $t=50$  s, this temperature gradient decreased greatly and will be rapidly smaller as the whole structure approaches the

thermal equilibrium at the saturation temperature. Proportionally the inner region of the capacitor experiences the greatest delay in temperature rising.

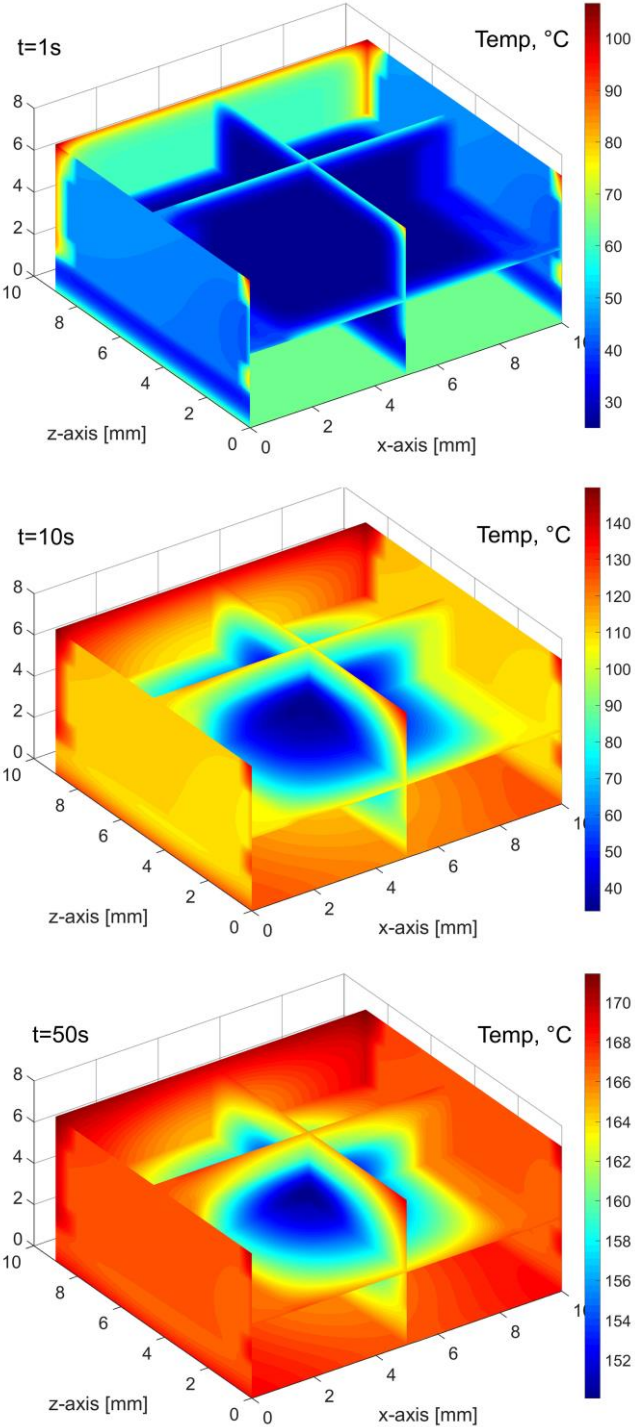


Fig. 6. - Interpolated temperature distribution during heating at 1 s (top), 10 s (center) and 50 s (bottom).

After several heating and cooling cycles, we observed the separation of the encapsulant at the interface with the adjacent plastic material on one capacitor, shown on Fig.7. The delamination phenomenon is usually caused by poor adhesion and mismatch of coefficient of thermal expansion (CTE). During heating or cooling, the CTE mismatch between the encapsulant and the adjacent material can lead to thermo-mechanical stresses that may eventually result in warpage, consequent cracking or delamination between the layers [46].

The large thermal gradient during rapid heating strongly points to this kind of component failure. This also points to the fact that immediate immersion into high temperature saturated vapour could be harmful for such structures. As a solution, more sophisticated VPS systems apply heat transfer control by regulation of the power for the heating elements, or by adjusting the penetration level of the specimen in the vapour [5].

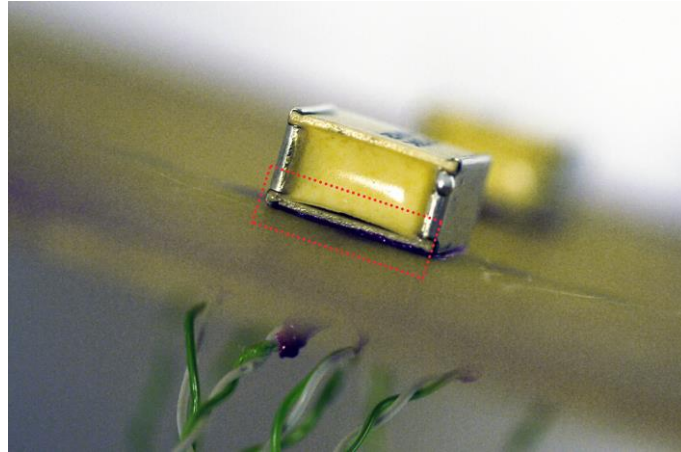


Fig. 7. – Delamination of the encapsulant material.

#### 4.3 Structural analysis

The PCB, the epoxy body and metallized PET core shows similar plastic-like thermal behaviour during the heating process, and the material interface between them do not causes major imprint in the temperature distribution. However, the Al terminations with very high thermal conductivity can be easily distinguished from the surroundings. Figures 8 and 9 are focusing on thermal aspects of the termination, which plays crucial role during the wetting of the solder material. Despite the homogenous heating, there are significant temperature differences across its surface. This can be accounted to the structural asymmetry, namely the metallic leads only on one side of the terminations, that reaching into the structure (as seen on Fig. 2). The metallic leads conduct the heat away from one side of the terminations into the plastic body. This is clearly depicted in Figure 8. The effect is slight, because the lids are heated too from the outside, but still able to produce considerable temperature gradient, shown on Fig. 9.

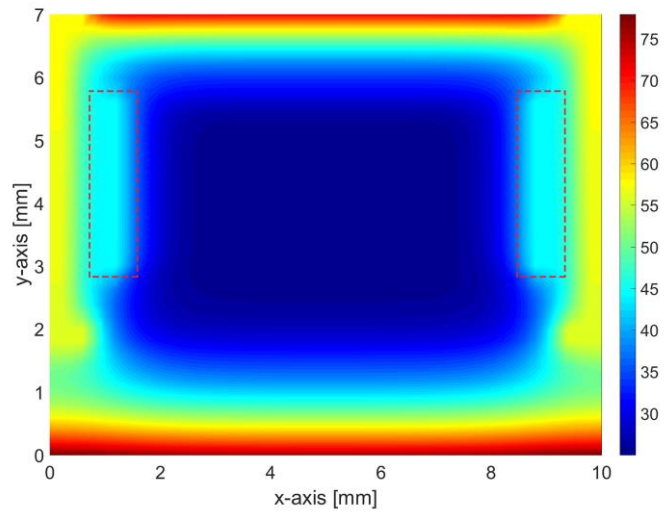
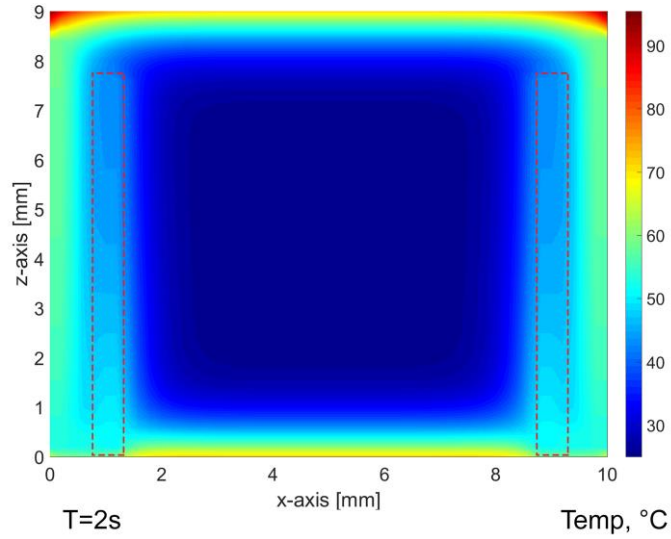


Fig. 8. – Temperature map of component at an inner section revealing the effect (highlighted) of inner metallic lead (top, front views, respectively).

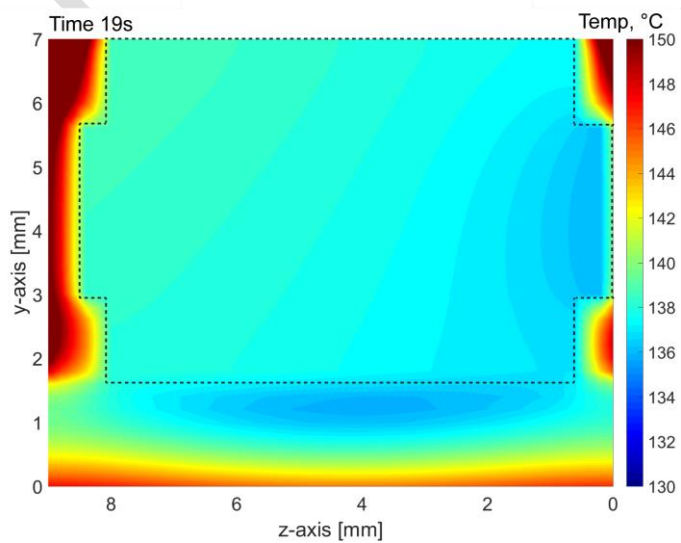


Fig. 9. – Temperature distribution of the termination (highlighted) around the melting point of the given solder (138 °C).

Figure 10 also emphasizes the finding. It shows the average absolute temperature difference between the left and right side of the same termination during the transient. The difference quickly rises and peaks in the first few seconds, while slowly decreases to zero as the temperature of the whole structure is advancing to the saturated vapour temperature.

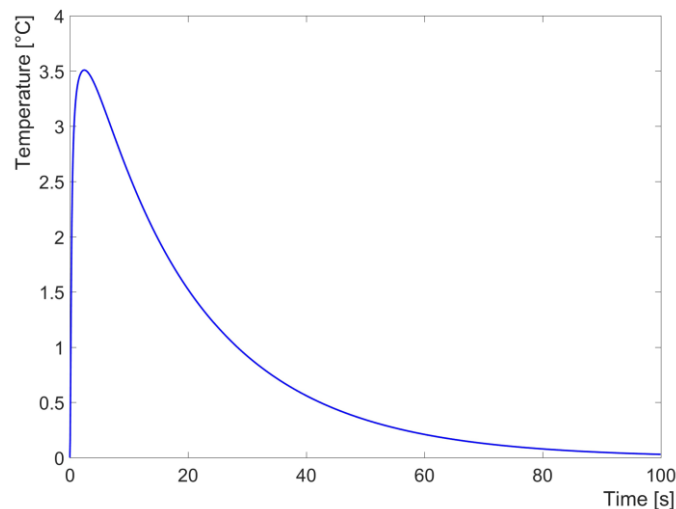


Fig. 10. – Absolute temperature difference between the left and right side of a termination.

While the solder only wets the terminal surface after reaching the melting point (138 °C – in the given case, 217 °C in the case of more common SAC305 alloy and LS230 Galden), the lateral differences may affect wetting related issues, or the so called self-alignment effect of the component [47, 48]. Eventually this can alter the quality and reliability of the joint as well. This effect is not widely studied for such components in VPS, so this might point to a future research path with an emphasis on practical evaluation of the alignment.

## 5. Conclusions

In our paper, we present a novel FDM modelling method with ADI approach to simulate surface mounted component heating during vapour phase reflow soldering in saturated vapours. The method is applicable as a fast and efficient way of presenting the process of heating, also showing exact thermal distribution in surface mounted component packages during VPS reflow.

We determined the average heat transfer coefficient of the condensation process in an experimental VPS system set for soldering in saturated vapours, using lumped system modelling. Applying this characteristic, we developed and verified a detailed 3D finite difference model of a surface mounted capacitor that accurately simulates the thermal behaviour of the real component.

It was shown that the method can present overall differences in the temperature of the SMD component during the process. It was presented, that high temperature differences are observable (~100°C) in the relatively large structure of the SMD component, pointing to thermal stresses that may damage the component. A related damage was also observed and analysed on the component structure during the validation experiments.

The results also revealed that the internal structure of the component may result in uneven temperature distribution along the terminations, which may affect soldering from the aspect of wetting at the transition of solidus-liquidus phases. Non-even melting can affect the alignment of the components during soldering, leading to quality and reliability concerns.

The current research opens further paths of experiments. In the future, it is possible to investigate thermomechanical behaviour of the given component structure, highlighting possible stresses that may damage the component. Dynamic heating may also be included to our model in improve precision of future calculations.

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## Figures list

Fig. 1. Experimental VPS system with electronic assembly immersed in vapor space.

Fig. 2. X-ray images of the capacitor's inner structure with highlighted core (top: side view, bottom: top view).

Fig. 3. Averaged transient heating curve of the PCB.

Fig. 4. Finite difference capacitor models containing 5985 thermal nodes (top) and 84456 thermal nodes (bottom). Inner structure is shown. Lateral axes:  $x$ ,  $z$ ; vertical axis:  $y$ .

Fig. 5. Calculated transient heating curves for the central region of the capacitor and the center point of the termination.

Fig. 6. Interpolated temperature distribution during heating at 1 s (top), 10 s (center) and 50 s (bottom).

Fig. 7. Delamination of the encapsulant material.

Fig. 8. Temperature map of component at an inner section revealing the effect of inner metallic lead (top, front views, respectively).

Fig. 9. Temperature distribution of the termination (highlighted) around the melting point of the given solder (138 °C).

Fig. 10. Absolute temperature difference between the left and right side of a termination.