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Quantum Transport Investigation of Threshold Voltage Variability in Sub-10 nm Junctionless Si Nanowire FETs

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***Abstract*—In this paper, we use the Non-Equilibrium Green's Function formalism to study the dependence of the threshold voltage variability on the cross-section shape and the gate length in JunctionLess Field Effect Transistors. Each configuration, i.e. gate length and cross-section, was investigated using a statistical ensemble of 100 samples. We found that the variability in threshold voltage is increased independently of the cross-section shape when the gate length is shrunk down to 5 nm. We attribute this results to the higher wave function "randomization" in longer gate lengths.**

Keywords—JLFET, NEGF, Discrete Dopants, Statistical simulation, threshold voltage, Variability

I. Introduction

Junctionless Si Nanowire field-effect transistors (JLFETs) are being investigated as a cheaper solution for sub-7 nm CMOS technology node. Indeed, their fabrication does not require advanced doping technics to precisely define their source and drain regions [1]. However, proper scaling of the JLFET for sub-7 nm CMOS applications requires the use of nanowires with only few nanometres diameter to limit the impact of short channel effects. Consequently, the variability arising from the discreteness of charge in these confined and heavily doped devices must be investigated quantum-mechanically [2-3]. Indeed, JLFETs for sub-7nm technologies are expected to possess a width below 10 nm and the quantum interference between the reflected waves by the discrete dopants should be taken into account.

There have been several quantum-mechanical statistical simulations in the past that aimed at assessing the impact of Random Discrete Dopants (RDD) on the variability of different figures of merit of JLFETs [3-5]. However, all these studies were conducted at low source-to-drain bias and considering only few tens of samples. Moreover, the dependence of the variability on the shape of the JLFET cross-section was not investigated.

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In this work we investigate the threshold voltage (V_{th}) variability in ultra-scaled JLFET with square and circular cross sections for different sub-10 nm gate lengths (L_G) using Non-Equilibrium Green's Function (NEGF) under high source-to-drain bias. We use an important statistical ensemble of one hundred samples for each device and found that V_{th} variability distributions for both cross sections are very similar. Our results also indicate that the variability of sub-10 nm JLFETs is very high and increases as L_G is shrunk from 10 to 5 nm independently from the cross section shape.

II. Methodology

The simulated square and circular JLFETs, which have a width of 3 nm and a diameter of 3.8 nm respectively, are depicted in Fig. 1. They are all oriented along the [100] direction and have a 10 nm uniformly n-doped source/drain regions with doping $N_D = 10^{20}$ cm^{-3} to ensure continuous injection in the RDD region which is 20 nm long for all devices [2]. The RDD in this region are generated with an average doping concentration N_D using the rejection technique [6]. The gate is assumed to have a work function of 4.55 eV and is always located at the centre of the RDD region. The equivalent oxide thickness is 1 nm. For a given cross section and gate length, we have carried out statistical simulations employing an ensemble of 100 devices at $V_{DS} = 0.6$ V.

The current and charge distributions were obtained by solving self-consistently Poisson and Non-Equilibrium Green's Function (NEGF) transport equations in coupled mode space approximation [7]. The conduction band in silicon was modelled using the effective mass approximation. As we are interested in V_{th} variability, we have solved the transport equations in the ballistic limit. Indeed, for such short gate lengths, electron-phonon interactions have an important impact only for ON-state current [8].

It is important to note that all devices have the same perimeter of approximately 12 nm and that V_{th} for each device was computed at a fixed current $I_D = 0.3$ nA.

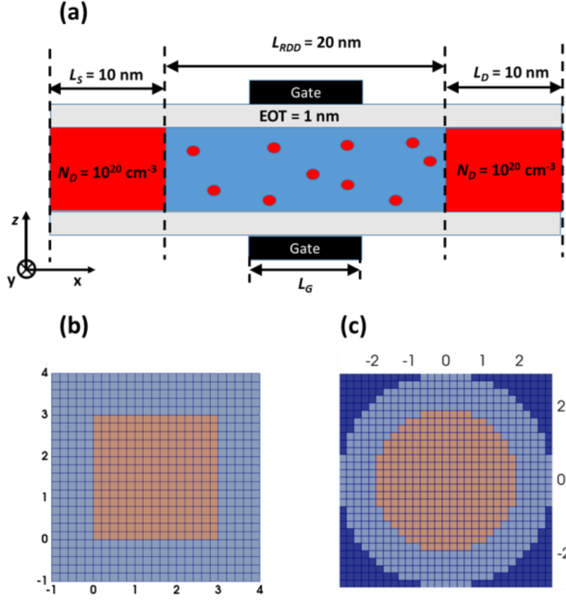

Fig. 1. (a) Schematic view of the devices in the transport direction. (b) JLFET with the 3x3 nm^2 square cross-section and (c) JLFET with the circular cross-section with 3.8 nm diameter. The Si is represented in orange and the SiO_2 in light blue. The discretisation step is 0.2 nm in all three directions.

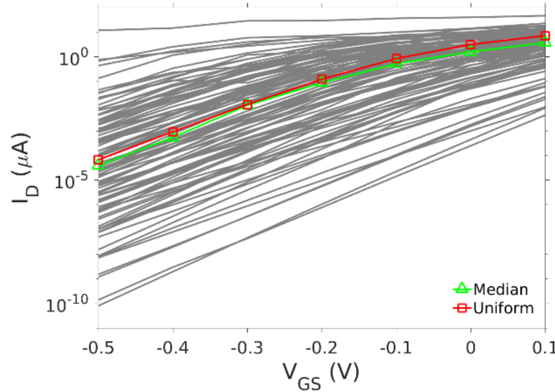

Fig. 2. I_D-V_G characteristics at V_{DS} = 0.6 V for the device with square cross section and L_G = 5 nm.

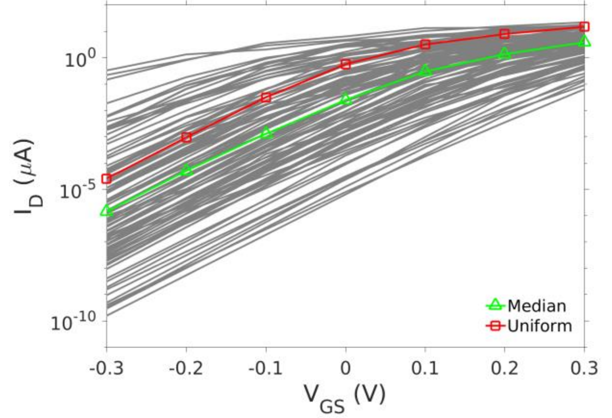

Fig. 3. I_D-V_G characteristics at V_{DS} = 0.6 V for the device with square cross section and L_G = 10 nm.

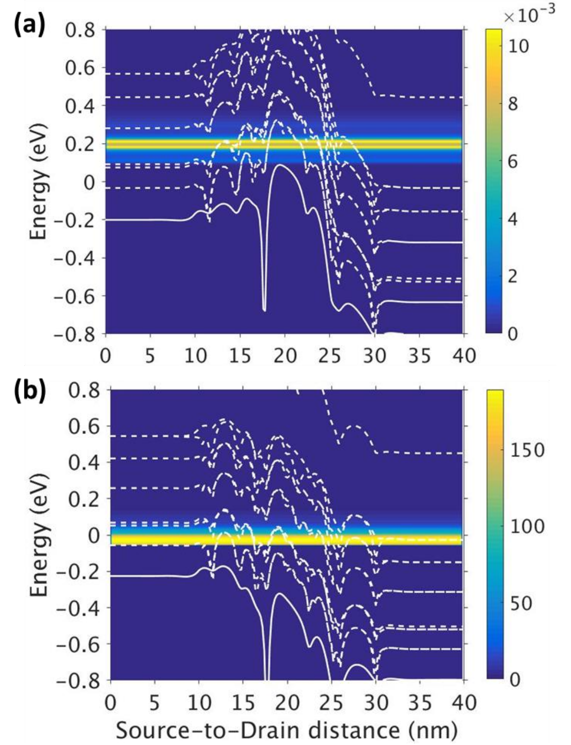

Fig. 4. Current spectrum in μA/eV for the square JLFET with RDD in (a) OFF-sate, i.e. V_{GS} = -0.3 V and I_D = 0.7nA and (b) ON-state, i.e. V_{GS} = 0.3V and I_D = 13.53μA. The Fermi levels at the source and drain are respectively at 0 and -0.6 eV. The subbands are plotted in dashed lines. The solid line is the bulk conduction band in the middle of the device.

III. RESULTS

A. I_D-V_G Variability

Two examples of the obtained drain current vs gate voltage characteristics (I_D-V_G) are presented in Figs. 2 and 3, which correspond to the square JLFETs with 5 and 10 nm gate lengths respectively. These figures highlight the importance of considering the discrete nature of dopants for the ultra-scaled nanowires considered herein. Indeed, both figures show very high variations of the I_D-V_G characteristics with respect to the one obtained with the continuous doping assumption. Moreover, Fig. 3 shows clearly that the latter assumption fails to capture the behaviour of the median device for L_G = 10 nm.

The current spectra for the square JLFET with L_G = 10 nm at V_{DS} = 0.6 V in both OFF and ON states are shown in Fig. 4a and Fig. 4b respectively. In both cases, one can notice the impact of the RDD on the subbands, the flatness of the potential in the uniformly doped source/drain regions and the continuity of the current along the whole device. It is worth mentioning that the

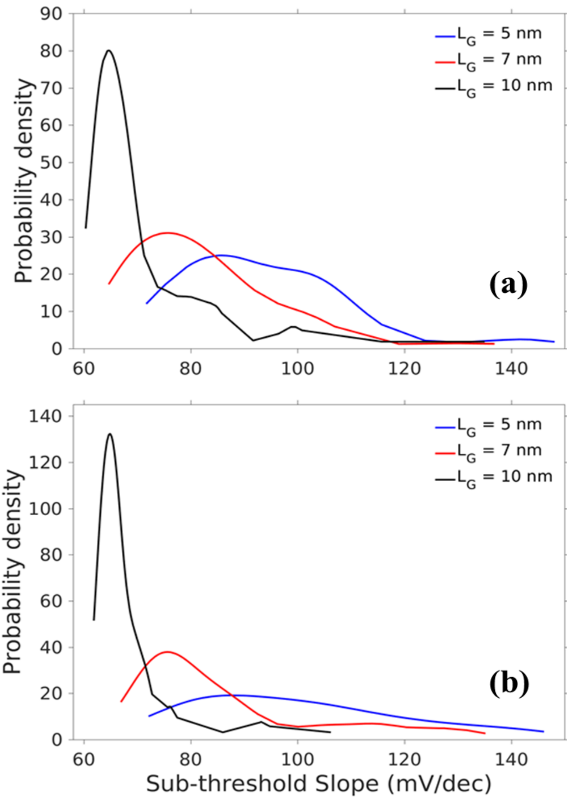

Fig. 5. Subthreshold slope probability density for (a) square (b) circular JLFETs for 3 different gate lengths.

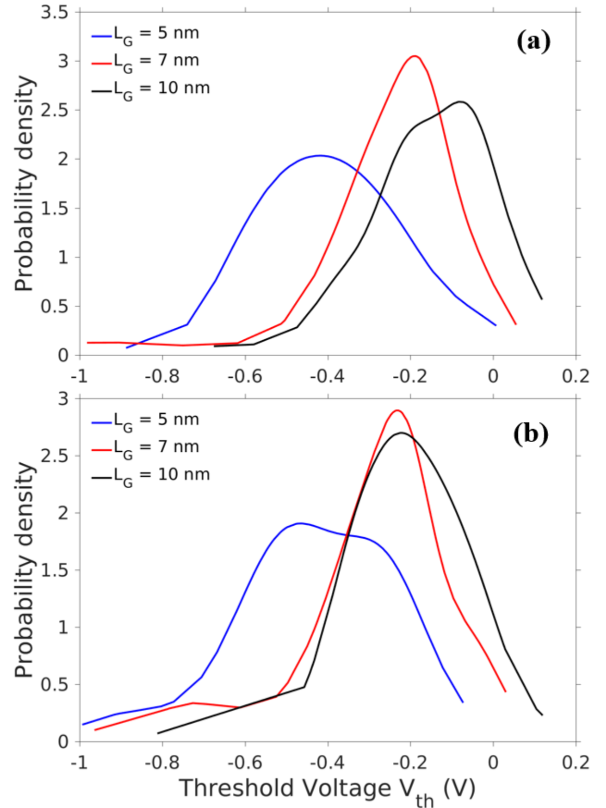

Fig. 6. Threshold voltage probability density for (a) square (b) circular JLFETs for 3 different gate lengths.

splitting of the spectrum in Fig. 4a into two bright lines is an indication that OFF-state current for this device is governed by the tunnelling through two different impurity states. Together with the good electro-neutrality – not shown here, this figure shows that our simulation tool is well adapted for this type of study.

B. Sub-threshold slope variability

The probability distribution functions (PDF) of the subthreshold slope (S_{th}) for L_G = 5, 7 and 10 nm for square and circular NWs are shown in Figs. 5a and 5b respectively. As expected, it shows a better electrostatic control of the channel in the circular JLFET, especially for L_G = 10 nm. However, as L_G reaches 5 nm, the subthreshold slope variability is considerably increased by RDD effect.

C. Threshold Voltage Variability

Figs. 6a and 6b show the PDFs of the V_{th} for different gate lengths for the square and the circular JLFET respectively. The evolution of the PDFs as the gate length is shrunk from 10 to 5 nm is similar for both cross section shapes. While V_{th} variability is similar for L_G = 10 and 7 nm, it is dramatically increased when the gate length is reduced from 7 to 5 nm. We attribute this broadening of PDF of the threshold voltage – whose value is mostly governed by the barrier height/shape under the gate – to the quantum interferences between the reflected waves by the coulomb potentials generated by the RDD under the gate.

Indeed, as the length of the RDD region L_{RDD} is the same for all gate lengths, the Poisson distributions of the RDD for all gate lengths are centred on approximately the same average value for a given cross-section. For a high doping as the one considered here, a longer gate contains a larger number of discrete dopants. Consequently, their spatial distributions under the gate is more likely to present "equivalent" quantum configurations – in the sense of wave function randomization – thus reducing V_{th} variability. On the other hand, when L_G in shrunk the number of discrete dopants under the gate is reduced and both individual and relative RDD positions become important, thus increasing the broadening of the threshold voltage PDF.

IV. Conclusion

We conducted a statistical study of the threshold voltage variability in ultra-scaled JLFETs with different gate lengths and cross section shapes using NEGF formalism. Our results show that for both cross section geometries the variability which is large but comparable for L_G = 10 and 7 nm is further degraded when the gate length is shrunk to 5 nm. We attribute this degradation to the importance of the quantum reflections and interferences of the electrons wave function with the Coulomb potential generated by the randomly distributed discrete dopants under the gate.

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