Physical Investigation into Effective Voltage Balancing by Temporary Clamp Technique for the Series Connection of IGBTs

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Abstract—The series connection of IGBTs is essential for high voltage applications where fast switching performances need to be maintained. However, unbalanced voltage sharing is a major resistance to the converter application of this structure. There are a number of causes leading to voltage unbalance, such as different signal delays, parasitic parameters, and tail currents and so on. A temporary clamp scheme performed by Active Voltage Control (AVC) has been proven to be effective in solving the unbalanced voltage-sharing issue. However, the basic physics has not been investigated. In this paper, the physical principle of voltage unbalance within IGBTs series operation is discussed. The carrier storage region differences are concluded to be the intrinsic cause of unbalanced voltage sharing. By using an accurate Fourier-series-based IGBT simulation model with appropriate assumptions, a physical explanation for temporary clamp is provided in detail. At the end of the tail current period when the excess carrier concentration becomes close to the intrinsic doping density, the temporary clamp is able to achieve satisfactory equal voltage sharing.

Index Terms—IGBT; Active Voltage Control (AVC); Series connection; Voltage unbalance; physical model;

I. INTRODUCTION

Series connection of IGBTs is an effective way to increase the rated voltage of power electronic converters. This approach is increasingly widely used in high-voltage and high-power power conversion systems such as HVDC transmission system [1-4], pulsed-power applications [5] and et al. It could result in a real improvement of the total weight, volume, and cost of the whole converter, thanks to the possibility of both reducing energy losses and increasing operating switching frequency. The advantages have been presented when compared with the well-known modular multilevel converter (MMC) with much easier control strategy and half device number [3]. Moreover, for the series connection operation, lower voltage, higher performances, latest-technology IGBTs can achieve the maximum switching performances [6].

However, the main problem with such a promising scheme is unequal voltage distribution among IGBTs in both static and dynamic operations. Matched IGBTs and gate drives do not guarantee balanced voltage sharing. This unequal voltage sharing is mainly due to the spread of IGBT static and dynamic parameters, gate drive delays and external parameters [7-8]. Voltage unbalance may make series-connected IGBTs exceed their voltage ratings. The subsequent failure of one IGBT resembling the chain-reaction leads to final failure of the entire series string of IGBTs.

There are several methods to minimize the voltage

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difference across individual IGBT in the series string [1-15].

Careful selection of IGBTs to have low parameter spread and synchronizing gate-drive signals will both help minimize voltage difference. There are some other solutions that are able to meet the requirements of IGBTs in series, which could be divided into three groups: passive snubbers, active gate control and active clamp circuits [7]. Passive snubbers are simple to implement. A resistor network in parrallel with each series-connected IGBT is used for static voltage balancing , and a resistor-capacitor or a resitor-capacitor-diode circuit in parallel with each IGBT used for dynamic voltage sharing. The use of a resistor network increases static power losses during static phases; the use of large snubber circuits minimizes voltage unbalance during dynamic phases but increases the transient power losses due to the increased commutation time [9-10]. These components are large in size and very costly. Active gate control methods act on the gate side controlling the way that the gate terminal is charged. It can modify the behavior of the IGBT during the switching process in the IGBT's active region. Among the different active gate control methods the following ones can be found: (1) reference voltage control method [1-2]; (2) gate signal delay control [3, 11]; (3) auxiliary circuits [6-8]; (4) master slave control method [12]; (5) gate balancing magnetic core method [13]. The active voltage clamp technique widely used for voltage overshoot clamping could also be helpful for voltage balancing [5, 14]. Clamps are simple circuits to limit the maximum blocking voltage of any IGBT but the extra losses generated when the IGBT operates in the active region makes the clamps unattractive to be used in high-power/high-frequency applications [10]. A novel hybrid voltage-balancing technique is proposed to achieve voltage balancing with minimum total losses [7]. A quasi-active gate control is proposed to provide dynamic and static voltage sharing by using a simple RC balancing network and a single gate drive with the parameter optimization discussed in [4].

For the active gate control methods or active clamp methods, one issue is that the voltage divergence in the steady-state (off-state) cannot be eliminated or it needs extra components, although the transient voltage synchronization is much improved. The static voltage divergence is reported in [2-8, 9-10,12-16] where the voltage divergence reaches as high as half of the operating DC voltage [10].

A temporary clamp technique performed by the closed-loop Active Voltage Control provides a nice solution to eliminate the static voltage unbalance. Experiments have been carried out to examine the performance of this successful technique [17]. The robustness of such a technique is considered [18]. Comparatively, this technique is more attractive in achieving static and dynamic balanced voltage sharing because such a closed-loop gate drive technique is able to improve system stiffness with the nice voltage balancing function when the disturbance of the converter application cannot be easily observed. However, the basic physics of this technique has not been investigated. The operating condition of this technique needs further investigation.
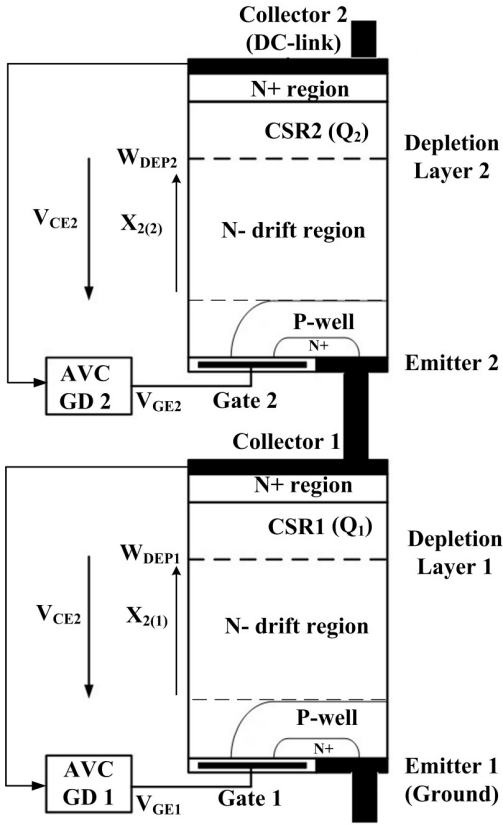
Fig. 1. Connection of two IGBTS in series showing the internal structures and the corresponding physics.

In this paper, the physical principle of voltage unbalance within series-connected IGBTs operation is discussed. The carrier storage region differences are concluded to be the intrinsic cause of the voltage unbalanced sharing. By using an accurate Fourier-series-based IGBT simulation model with appropriate assumptions, a physical explanation for temporary clamp is provided in detail. The temporary clamp is proved to be very effective in achieving equal voltage sharing at low-level excess carrier concentration (on the order of intrinsic doping density) of series-connected IGBTs.

II. CIRCUIT AND DEVICE MODELING

In order to investigate the mechanism for voltage divergence between series-connected IGBTs and the physical operating principle of temporary clamp, a detailed circuit and IGBT model describing the carrier physical dynamics is required. The key part here is the IGBT and its AVC gate drive circuit modeling, as it is shown in Fig. 1. In the previous work [17], the validation experiments for temporary clamp are performed under a clamped inductive load test by a double pulse. The device simulator such as Atlas cannot implement closed-loop control simulations such as the AVC technique. To exam the controlled series-connected IGBTs' switching under temporary clamp, a clamped inductive load test is built in Matlab/Simulink [20-21].

A. IGBT Modeling

The behavior of IGBT is mainly dependent on the excess carrier distribution in the wide lightly doped N- drift region. A 1-D solution is adequate for physical investigation into the voltage divergence phenomenon of IGBTs' series connection and the principle for temporary clamp. This is also a compromise between simulation accuracy and computation speed.

Other assumptions could be made:

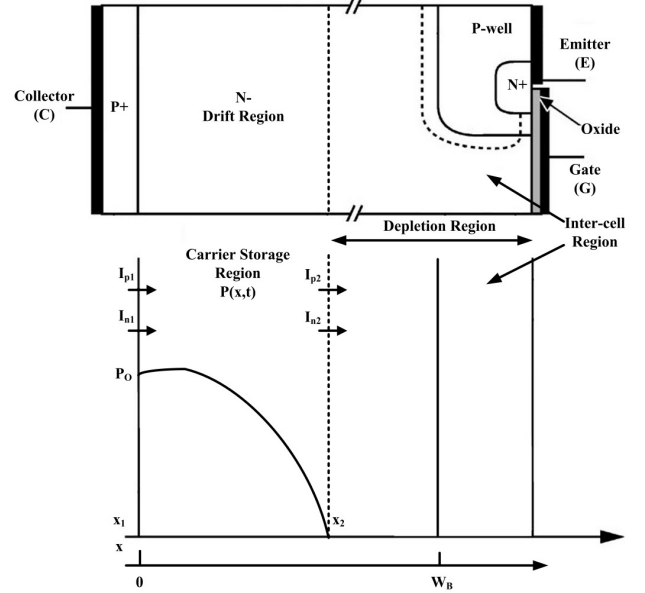a) The base is quasi neutrality;

b) The doping is uniform;

Fig. 2. The structure of a planar NPT IGBT and undeleted drift N- region carrier profile showing boundary currents.

c) The base high-level lifetime is assumed to be constant.

The IGBT model discussed in this paper is 1700 V/ 800 A FF800R17KF6C NPT IGBT from Infineon. The structure of such a planar NPT IGBT and its simplified carrier profile are shown in Fig. 2. Under high-level injection conditions, the carrier's dynamics in the base is governed by the ambipolar diffusion equation (ADE):

$$D\frac{\partial^2 P(x,t)}{\partial^2 x} = \frac{P(x,t)}{\tau_{HL}} + \frac{\partial P(x,t)}{\partial t}$$

(1).

D is the ambipolar diffusivity, $P(x,t)$ is the concentration of excess carrier and τ_{HL} is the high-level carrier lifetime. By using the Fourier-series solution for the carrier distribution, the second-order partial differential Equation (1) is converted into a set of ordinary differential equations [19]. The boundary conditions determining the accuracy of simulation are given by the gradients of the carrier distribution at the boundaries of the N- drift region (x_1 and x_2) as shown in Fig. 2, which can be expressed as a function of the hole and electron currents at x_1 and x_2

$$\frac{\partial P(x,t)}{\partial t}\bigg|_{x_1} = \frac{1}{2qA}[\frac{I_{n1}}{D_n} - \frac{I_{p1}}{D_p}]$$

$$\frac{\partial P(x,t)}{\partial t}\bigg|_{x_2} = \frac{1}{2qA}[\frac{I_{n2}}{D_n} - \frac{I_{p2}}{D_p}]$$

(2).

A is the active cross sectional area of the device, D_n and D_p, the electron and hole diffusion coefficients, I_{n1} and I_{p1}, the electron and hole currents at $x=x_1$, and I_{n2} and I_{p2}, the electron and hole currents $x=x_2$. Since by current continuity

$$I_C = I_{n1} + I_{p1} = I_{n2} + I_{p2}$$

(3),

it is sufficient to find each current component at the boundaries. At the right side of the N- drift region x_2, the electron current I_{n2} consists of the MOS channel current and two displacement currents given by the current charging the collector-emitter depletion capacitance and the gate current charging the gate collector capacitance. A reasonable correction method on the Miller capacitance is proposed to improve the simulation accuracy [21]. For the NPT strcuture,

$$I_{p1} = qAh_pP^2_0$$

(4)

where h_p is the hole recombination rate and P_0 is the excess carrier density at the collector side. The accurate IGBT parameters are extracted by using the parameter optimization method proposed in [20-21].

B. AVC Gate Drive

The AVC gate drive is able to synchronize the series-connected IGBT switching transients [1-2, 16-19]. It is a classic feedback control method that reduces the dependence of the performance on the IGBT. By considering the IGBT nonlinearity and parameter uncertainties, AVC is designed to be robustly stable and well-damped [18]. The AVC drivers are independently applied to each IGBT in the circuit as shown in Fig. 1. Direct constant control via feedback loops is implemented on the IGBT collector-emitter voltage V_{CE}. V_{CE} of each IGBT is regulated to follow the pre-designed reference voltage V_{REF}. The schematic of Active Voltage Control is shown in Fig. 3. In the traniesnt switching control part, the reference signal is identical to the previous versions as shown in Fig. 4 [17]. At turn-OFF, the reference starts with a pre-conditioning step, at V_{RISE}, for a period, t_{RISE}. The turn-OFF dv/dt will be controlled. V_{OFF} is used to clamp the transient voltage overshoot. The reference in the turn-ON period begins with a slow ramp, t_{FALL}. It allows the FWD to have sufficient time to recover and at the same time synchronizes all devices to be ready for the subsequent process. The following steeper ramp (short t_{ON}) regulates the devices during rapid transient to complete their turn-ON and avoid excessive power losses.

The temporary clamp is performed during the IGBT OFF-time with a special designed reference to enable all the IGBTs to share identical voltages. This U-shaped reference section in OFF-time regulates the voltages with different magnitudes gather towards the temporary clamp voltage V_{TC} level as shown in Fig. 4. As a result, individual IGBT can share the same voltage that is defined by the number of devices connected in series and the DC link voltage. The temporary clamp duration t_{TC} is to ensure the voltage balancing effect and stability of the operation. The optimal reference settings have been discussed in [18].

III. Voltage Divergence Analysis

There are many factors that cause voltage unbalanced sharing for IGBTs connected in series, such as gate drive delays, external circuit parameters, and the spread of various IGBT dynamic and static parameters. Even if IGBTs have the same design but are manufactured in different batches, there will still be some variations in their respective parameters [22], e.g. intrinsic capacitances and gate resistances. In principle, the intrinsic causes for dynamic and static voltage divergence are closely related to the excess carrier distribution in the N- drift region of IGBT [14]. The excess carriers exists in the Carrier Storage Region (CSR) located between the edge of the depletion region and the P+ junction. There is substantial charge stored (Q_1 in IGBT1 and Q_2 in IGBT2) as shown in Fig. 1. Since this charge cannot be removed by the electric field from the depletion region, the dominant way to eliminate this charge is by a relatively slow recombination process [20]. This process is known as "tail current". During this process, the gate drive has already been turned OFF. Therefore, external factors including external circuit parameters have limited impact on tail currents.

There are three causes for excess carrier distribution difference at the tail curent stage [16]: 1) different V_{CE}; 2) different IGBT inner structure parameters; 3) different durations of time in the active region. As the gate timing has
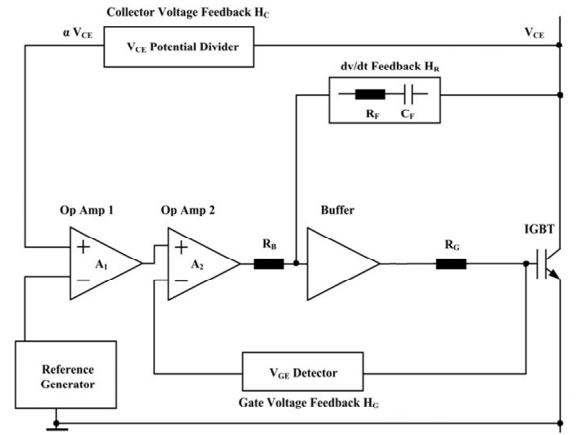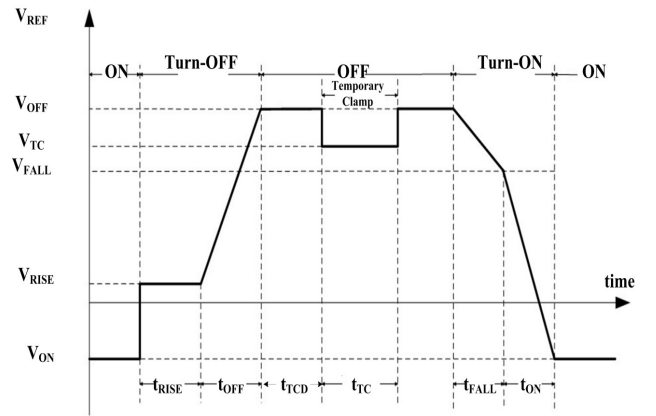

Fig. 3. The schematic of AVC.

Fig. 4. The temporary clamp reference for IGBTs connected in series.

been carefully considered by an adpative reference gerenation method [2], the transient rise/fall of V_{CE} has been synchronized in [17]. As a result, difference V_{CE} and different durations of time in the active region are believed to have limited influence on the internal CSRs in this case. Different IGBT inner structure parameters are believed to be the trigger for the tail current difference. This result is also found in the experimental results in [2] that matched IGBTs and gate drives do not ensure balanced dynamic voltage sharing between switching IGBTs.

The difference in the high-level lifetime τ_{HL} is believed to make the difference of CSRs in series-connected IGBTs. With high-level injection prior to the OFF state, the high-level lifetimes from the same IGBTs likely have the highest percentage variation [17]. It should be noted that there is an important assumption here for the IGBT physical model in use. To increase the model accuracy, differnet injection conditoins could be further considered by modifying the lifetime equation as it is done in [16, 23]. It has been concluded that the lifetime of Auger and radiation recombination decreases with the increase of carrier concentration while the lifetime of Shockley-Read-Hall recombination remains constant. When the tail current starts, the lifetime is low with high excess carrier concentration. With the excess carrier decreasing, the lifetime becomes larger and the tail curren will influence the voltage balance for a long period. The description of excess carrier distribution is more complex when the effect of concentration on lifetime is considered [16]. This paper mainly focuses on the machenism behind the temporary clamp technique where one typical operating condition (60 A) is considered for investigation. Constant high-level lifetimes for this operating condition are used an effective index to describe how the excess carrier distributions of IGBTs in series differ and how
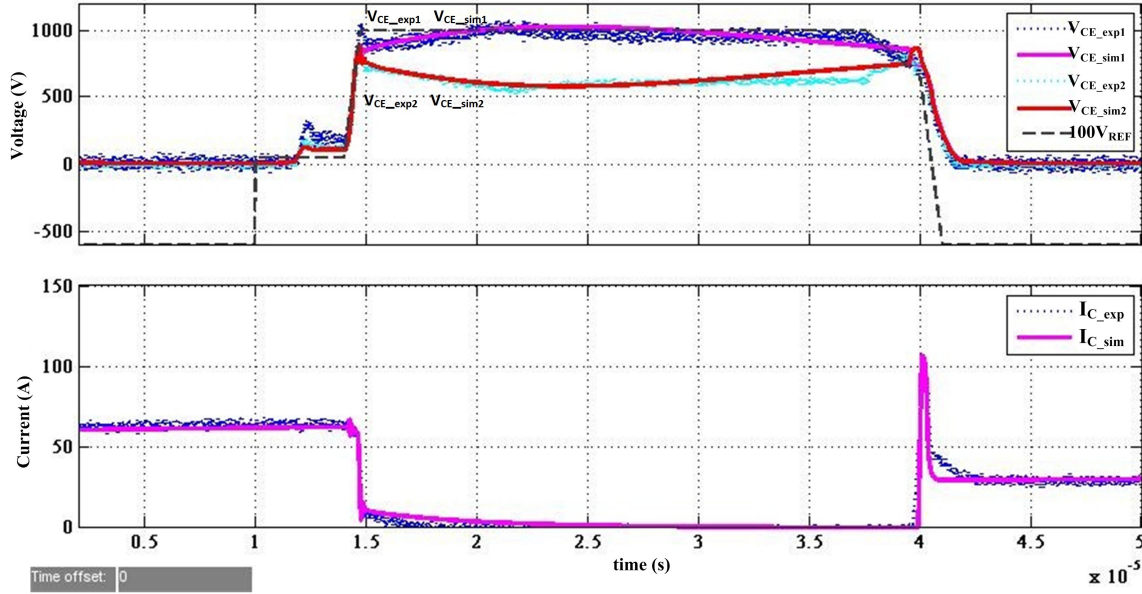
Fig. 5. IGBT switching comparisons under AVC without temporary clamp between the experimental data and simulation results.
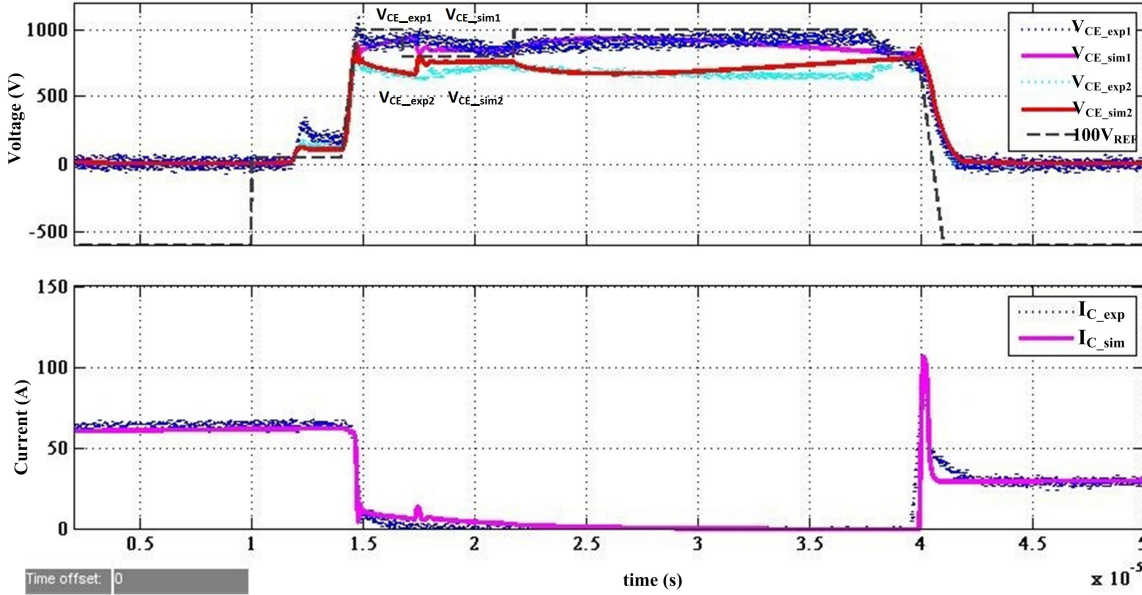

Fig.6. IGBT switching comparisons under AVC with temporary clamp (t_{TCD} = 2 μs) between the experimental data and simulation results.

the temporary clamp take effects on the re-distribution of CSRs to achieve balanced voltage sharing.

In order to simulate the switching of series-connected IGBTs, the high-level lifetime of each IGBT is assumed to have 20 % difference ($\tau_{HL(2)}$ of IGBT2 is larger). Accordingly, it is assumed that

$$\tau_{HL(1)} < \tau_{HL(2)}$$

(5)

The original rate of total charge change can be expressed by the charge control equation

$$\frac{dQ}{dt} = I_{n2} - I_{n1} - \frac{Q}{\tau_{HL}} = I_{mos} + I_{GC} + I_{DISP} - I_{n1} - \frac{Q}{\tau_{HL}}$$

(6)

At the tail current stage, the MOS channel current I_{MOS} is switched off. The C_{CE} and C_{GC} displacement current I_{GC} and I_{DISP} develop with the development of the depletion growth. As the depletion capacitances C_{CE} and C_{GC} are very small at this stage, the recombination dominates and the equation can be approximated for each IGBT as follows.

$$\frac{dQ_1}{dt} \approx -I_{n1(1)} - \frac{Q_1}{\tau_{HL(1)}} < 0$$

$$\frac{dQ_2}{dt} \approx -I_{n1(2)} - \frac{Q_2}{\tau_{HL(2)}} < 0$$

(7)

It could be estimated that [17]

$$I_{n1(1)} = I_{n1(2)}$$

(8)

Therefore, the total change of Q1 and Q2 could be obtained as follows,

$$\frac{dQ_1}{dt} - \frac{dQ_2}{dt} = -\frac{Q_1}{\tau_{HL(1)}} + \frac{Q_2}{\tau_{HL(2)}}$$

(9)

Therefore, Equation (9) could be expressed that that the amounts of stored charges Q1 and Q2 are both reducing and Q1 is shrinking faster according to Equation (5).
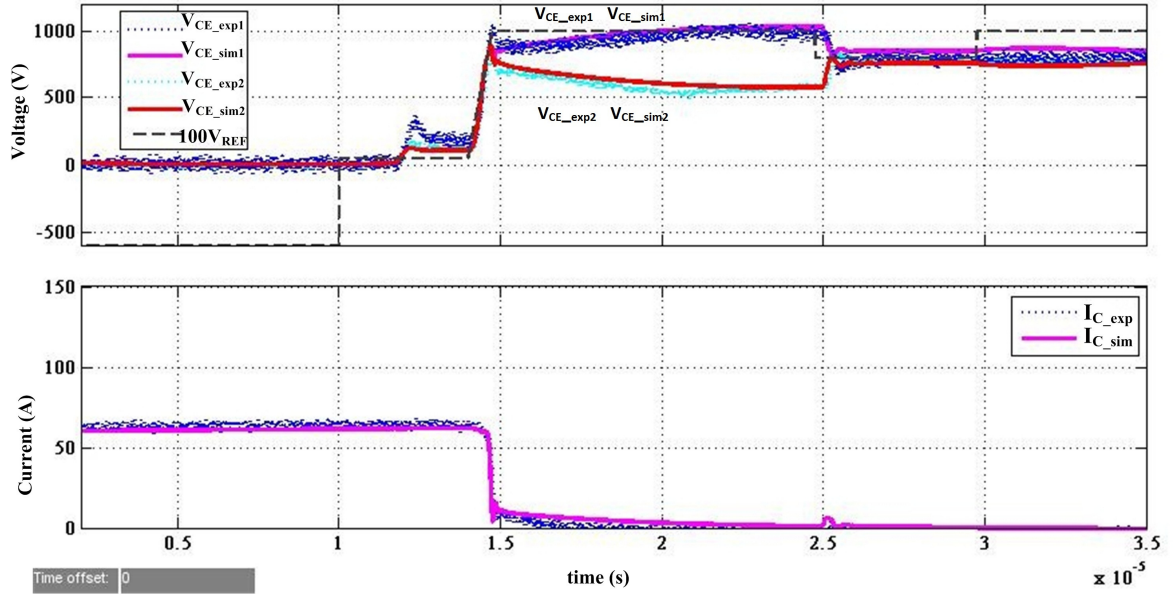
IV.   RESULTS

Fig. 7. IGBT switching comparisons under AVC with temporary clamp (t_{TCD} = 10 μs) between the experimental data and simulation results.

Using the physical IGBT model described in Section II, IGBT switching behaviors are well simulated. The simulation and experimental waveforms for two NPT IGBTs in series connection under AVC without temporary clamp are shown in Fig. 5 where the simulated waveforms agree with the experimental results. Without temporary clamp, AVC regulates IGBTs nicely for the two transient parts (turn-OFF and turn-ON). It controls the IGBTs' switching to ensure their voltages react synchronously, although there is observable differences on the voltage overshoot at the pre-conditioning step. The voltage divergence occurs when the main transient voltage rise finishs. The difference between experimental waveforms V_{CE_exp1} and V_{CE_exp2} increases from 15 to 22 μs. When V_{CE_exp1} reached $100V_{REF}$ (1000 V) at around 22 μs the difference does not increase. Because of the series connection of IGBTs V_{CE_exp2} stay at a lower voltage level. Hence, AVC does help the IGBTs share the DC link voltage better by avoiding the divergence of their voltages growing excessively. However, the two IGBTs have unbalanced voltage sharing at the very start of the OFF-state. Their voltages start diverging from the instant when IGBTs are turned OFF. The voltage divergence is as high as 500 V. The simulated traces(V_{CE_sim1} ,V_{CE_sim2} and I_{C_sim}) followed the experimental results nicely. Slight differences can be observed at around 35μs when the simulated traces V_{CE_sim1} and V_{CE_sim2} begin to gather, which justifies the analysisthat the voltage difference will vanish if the OFF time is long enough [16].

Then, modified for voltage-balancing purpose, the temporary clamp shows its capability to balance the OFF-state voltage between series-connected IGBTs. The design of temporary clamp has to be considered carefully. With the effect of different durations of temporary clamp already being analyzed in [17], here Figs. 6 and 7 illustrate the effects of different positions of the temporary clamp applied to the series-connected IGBTs. It is straightforward that the temporary clamp applied after 2 μs into the OFF time cannot balance the voltage sharing as well as in the situations as shown in Fig. 7. It tries to regulate IGBT and makes their different voltage magnitudes to meet at V_{REF}. V_{CE_exp1} and V_{CE_exp2} do come close but did not meet. V_{CE_exp1} and V_{CE_exp2} start to diverge as soon as the temporal clamp finished. It should be noted that the tail current I_C during t_{TC} is still large, around 10 A.

The simulated traces are very agreeable to the experimental. Fig. 7 shows that both V_{CE_sim1} and V_{CE_sim2}

closely follow V_{CE_sim1} and V_{CE_sim2} respectively. Fig. 7 is also representative of well-designed temporary clamp operation. It is used to exam the success of the modeling. Both IGBTs are sharing the voltage equally. Even after the temporary clamp finishes, the voltage difference between the two IGBTs is negligible compared to that before the temporary clamp is applied. For turn-ON, the errors between simulation and experimental results become slightly larger as the diode parameters have not been optimized.

V.   PHYSICAL INVESTIGATION INTO TEMPORARY CLAMP

The simulated CSR dynamics are able to reveal the actual IGBT physics under temporary clamp. The CSR profile of IGBT2 during turn-OFF without temporary clamp are plotted in Fig. 8(a). To analyze the CSR dynamics of the two IGBTs, three simulated CSR charges of both IGBTs are presented at three typical instants as shown in Figs. 8(b), 8(c) and 8(d). When both IGBTs are in the on-state, the stored CSR charges Q_1 of IGBT1 and Q_2 of IGBT2 are similar in Fig. 8(b). With a higher lifetime, Q_2 is larger than Q_1.

Both IGBTs start turning OFF with the identical reference to their gate terminals. In each IGBT, the gate current discharges the gate capacitance removing excess carriers at the boundry W_B. The depletion layer necessary to support the device voltage expends into the base width and the CSR shrinks with the charge removed. The approximate flat shape of Q_1 and Q_2 is lost. The collector voltage starts to rise. During this time, the depletion layer sweeps out the stored charges as it expands towards the collector. Therefore, the stored charges of IGBT1 Q_1 and IGBT2 Q_2 are forced to reduce. From 10 to 14.75 μs, there is very little difference in the depletion widths of both IGBTs.

At the start of tail current, CSR profiles become parabola-shaped as shown in Fig. 8(c). Q_1 and Q_2 still remain close to each other. From this moment on, the eventual disappearance of the MOS channel means that MOS electron current stops flowing. The current tail in NPT IGBT normally lasts tens of microseconds. The stored charges of both IGBTs are reducing but Q_1 is leading due to the higher decay rate. This could be well reflected in Fig. 8(c) and (d). At 20.00 μs, the width of Q2 ($X_{2(2)}$) is about 220 μm, compared with 200 μm in Q1($X_{2(1)}$). A difference ΔW is formed. The depletion region of IGBT1 is longer than that of IGBT2. V_{CE1} is larger than V_{CE2}. Towards the end of tail current, Q_1 approaches zero but IGBT1 still has a greater amount of excess carriers, as illustrated in Fig. 8(d). In this case, V_{CE1} stops rising up
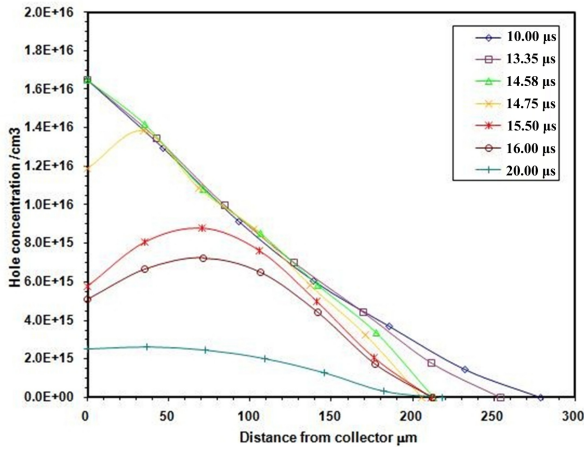
Fig. 8 (a). IGBT1 Q2 charge profiles during inductive turn-OFF simulation (note: Collector metal at 0 μm, Emitter at 280μm).
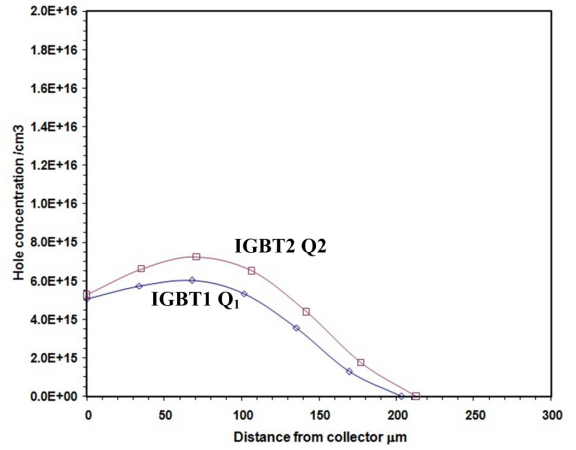

Fig. 8 (c). IGBT CSR charge profiles comparison at 16.00 μs (note: Collector metal at 0 μm, Emitter at 280μm).
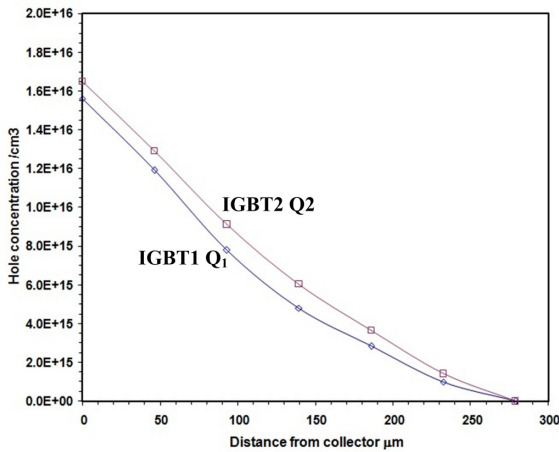

Fig. 8 (b). IGBT CSR charge profiles comparison at 10.00 μs (note: Collector metal at 0 μm, Emitter at 280μm).
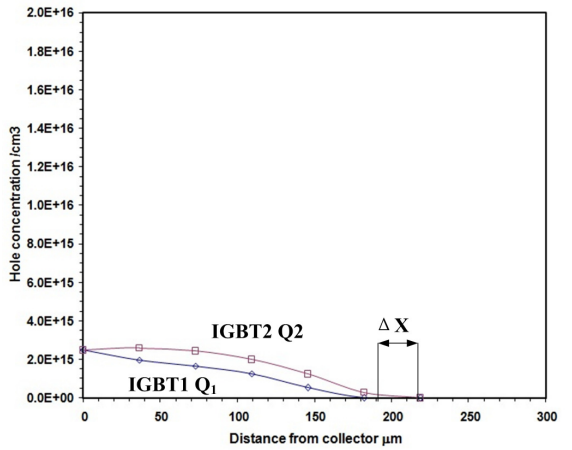

Fig. 8 (d). IGBT CSR charge profiles comparison at 20.00 μs (note: Collector metal at 0 μm, Emitter at 280μm).

and V_{CE2} stops falling. $X_{2(1)}$ stays unchanged after 20.00 μs. At the very low level of current, both Q1 and Q2 are slowly reducing. The majority of the charge has been removed from the IGBTs by this point.

To analyze the stored charge variations of series-connected IGBTs during temporary clamp, a simulation result that contains traces of I_G, V_{CE} and I_C are presented as shown in Fig. 9. The corresponding CSR width X_2 is plotted in Fig. 10. When the temporary clamp starts, the behavior observed at each IGBT's gate terminal is different. Fig. 9 shows that at the beginning of temporary clamp V_{CE_sim1} of IGBT1 is higher than the reference voltage V_{REF}. This leads the gate voltage to exceed the threshold voltage. Hence the MOS channel is re-opened, and I_{G1} start to charge the input capacitance. Electrons flow into the N- drift region and IGBT1 is turned ON. This could be observed in I_C, a spike as shown in Fig. 9. The depletion layer of IGBT1 shrinks towards the emitter end as Q_1 expands in Fig. 10 (a sharp increase of $X_{2(1)}$ at 25.43 μs). An increased amount of Q_1 is shown in Fig.11 (a). As a result, V_{CE1} fall quickly. For IGBT2, before V_{CE_sim1} and V_{CE_sim2} meet, V_{CE_sim2} is currently below the temporary clamp voltage V_{REF}, so it is still in OFF-state. However, as V_{CE_sim1} decreased sharply and the total voltage for the series-connected IGBTs is unchanged, V_{CE_sim2} is forced to rise. A sharp increase of $X_{2(2)}$ can be observed in Fig. 10. The depletion width of IGBT2 increased to stand the increased voltage. Part of Q_2 at the MOS side has been removed to the collector side, as shown in Fig. 11(a). After V_{CE_sim1} and V_{CE_sim2} met at V_{REF}, I_{G1} turn to discharge IGBT1 while I_{G2} starts to charge IGBT2. However, until 26.81μs, both IGBTs stay OFF as no MOS channel is opened. There is no spike in I_C as shown in Fig. 9. IGBT1 has a lower lifetime so Q_1

decays faster. There is another decrease for $X_{2(1)}$ as shown in Fig. 10 although the total charge has decayed to a lower value. Then V_{CE_sim1} increased quickly over V_{REF} again while V_{CE_sim1} decreased correspondingly. $X_{2(2)}$ of IGBT2 dereased. At 26.81μs , when IGBT2 is re-opened, a similar pattern would happened. Such a process will be repeated until Q1 and Q2 become identical before the temporary clamp ends. When the temporary clamp ends at around 29.80 μs , both the gate charges of both IGBTs are extracted by the gate currents, Fig. 9.

VI. DISCUSSION

In this paper, the temporary clamp technique has been investigated on the balanced voltage sharing effect of series-connected IGBTs via a physical IGBT simulation model. Eliminating gating delays for unbalanced voltage sharing, our experimental results confirmed the IGBT manufacture tolerances also directly casued intrinsic physical parameters variations. This leads to the uneven distributions on the CSR charges. There are many physical parameters whether they are dynamic or static having impact on the switching transient. The closed-loop AVC removes the effects of parameter variation at the MOS channel side by regulating MOS current. As a result, the influence of gate threshold variation, MOS channel conductance variation, input capacitance variation are fairly limited. Nonetheless, physical parameter variations at the collector end are hardly affected by AVC. For NPT or FS IGBTs, the sensitivity to lifetime variation is high at the collector side and the control in manufacture does possibly present the greatest variation between similar IGBTs. To reflect such a physical insight, different high-level lifetimes have been applied to two IGBTs
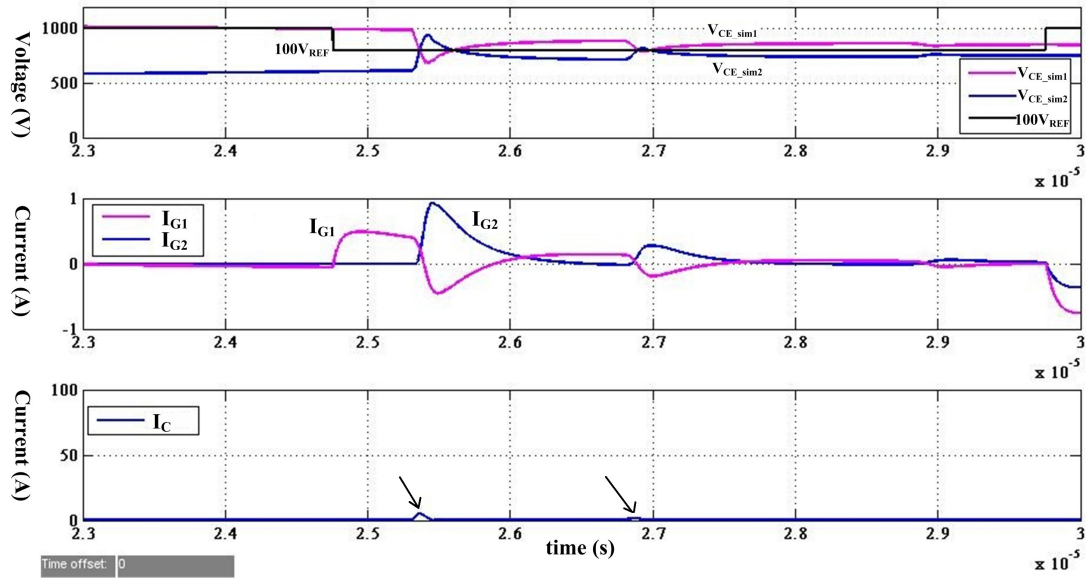
Fig. 9. Simulation result for temporary clamp section. Note that for clear observation, the second sub-figure shows the changes of difference between gate currents I_G.
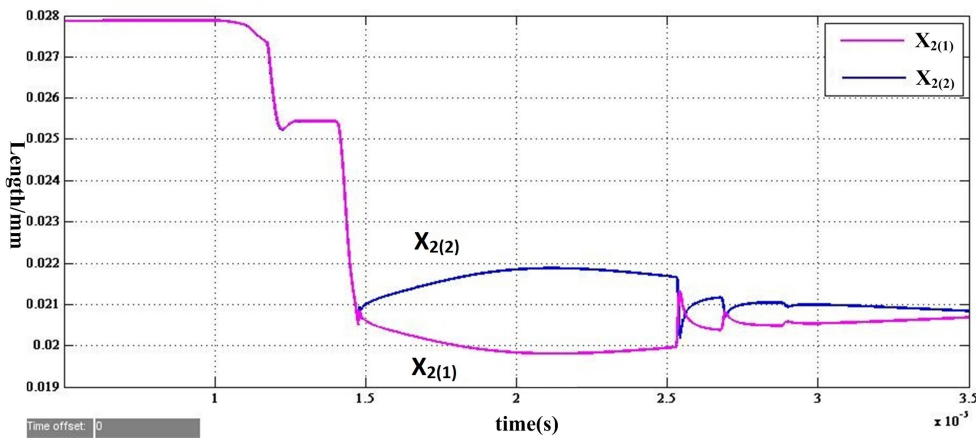

Fig. 10. Simulation result for the moving CSR boundary X2 ($X_{2(1)}$ for IGBT1 and $X_{2(2)}$ for IGBT2).

showing the simulated waveforms match the experiment traces nicely.

The timing to start temporary clamp is of great significance in achieving balanced voltage sharing for NPT/FS IGBTs. Inappropriately positioning the temporary clamp during the tail current stage could reduce the voltage divergence during the clamp section but after the section finishes the voltage divergence tends to increase again as it is shown in Fig. 5. At that time, both IGBTs are still at the early tail stage so there are still a great amount of excess carriers within IGBTs. As it has been discussed in the previous sections, temporary clamp re-opens the MOS channel to balance CSR charges of both IGBTs. With a slow recombination speed, the depletion region variation of both IGBTs are limited. The overlapping of both depletion widths cannot happen as show in Fig. 10. As a result, the even voltage sharing cannot be achieved. The temporary clamp is concluded to be successful at the end of the tail current stage when the excess carrier concentration becomes very low. The excess carriers of both IGBTs in Fig. 11 are on the order of intrinsic doping densities (around $2E14/cm^3$). An experimental demonstration of such a successful voltage balance by temporary clamp is shown in Fig. 12.

This stabilization process is well presented in the simulation results of Figs. 9, 10 and 11. A sharp depletion layer variation at 25.43 and 26.93 μs leads to a large dV_{CE}/dt causing a large displacement current of $I_{n2(2)}$ or $I_{n2(1)}$. This

also corresponds to the MOS channel current introduced by temporary clamp at series-connected IGBTs. Both current contribute to the two small spikes in I_C of Fig. 10. During the temporary clamp, the depletion widths of both IGBTs swapped with each other. Such a similar swapping process repeats. IGBT1 and IGBT2 take turns turning ON and OFF. Their collector voltages take turns to rise above and fall below the temporary clamp voltage level. Eventually these two device voltages would stabilize at the temporary clamp voltage. This will put a requirement on the the controller as it must be well-damped to ensure stability as that in Fig. 12 where the experimental damping waveforms can be observed.

During the temporary clamp, remaining charges of IGBTs will re-shaped and retreat to the collector side. This could be observed in Fig. 11. The amount of stored charge in each IGBT is much smaller than that at the beginning of current tail time. The carrier concentration may downgrade to low-level at this stage and the carrier lifetime may increase greatly. This cycle will make CSR charges of IGBTs damped to become indentical nicely. In the simulation model, a constant lifetime is assumed so the simulation cannot emulate the experiment results at the eventual voltage balancing. This is why the simulated results are worse than experimental results in the volate sharing balanceing as it is shown in Figs 7 and 10.
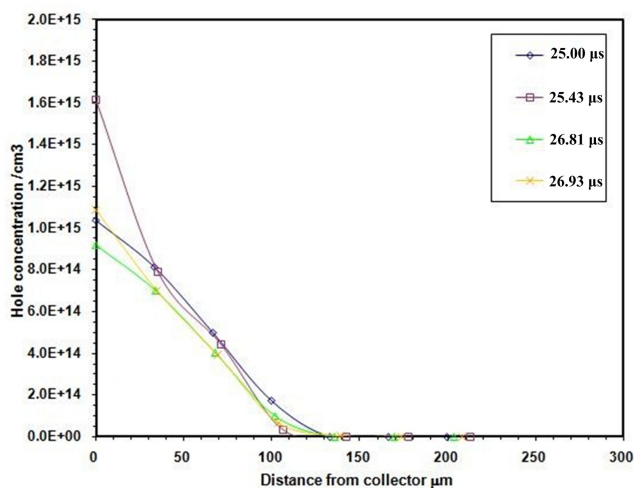
Fig. 11(a). IGBT1 Q1 charge profiles during inductive turn-OFF simulation at temporary clamp (note: Collector metal at 0 μm, Emitter at 280μm).
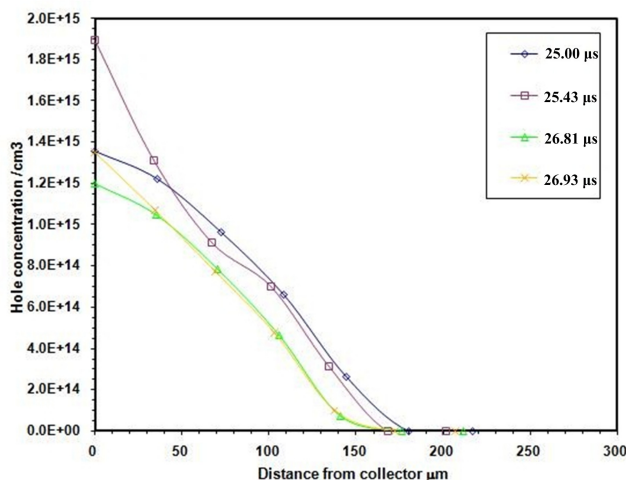

Fig. 11(b). IGBT1 Q2 charge profiles during inductive turn-OFF simulation at temporary clamp (note: Collector metal at 0 μm, Emitter at 280μm)..
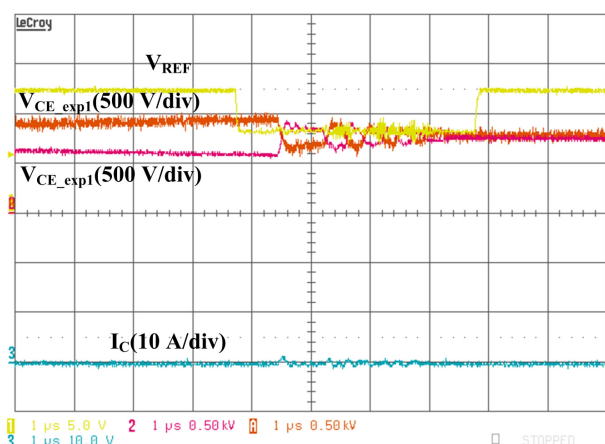

Fig.12. Experimental result for temporary clamp section, V_{CE} of two IGBTs swapped with each to achieve even voltage sharing.

VII. CONCLUSION

The temporary clamp technique is able to effectively balance voltage sharing of series-connected IGBTs after switching transients. In this paper, the physics behind this method has been fully investigated. The physical principle of voltage unbalance within IGBTs series operation is discussed. The CSR charge differences are concluded to be the intrinsic cause of the voltage unbalanced sharing. An accurate Fourier-series-based IGBT simulation model that is used to explain the effect of temporary clamp. The analysis provided accounts for the behavior during and shortly after the

temporary clamp is applied. By making the assumption that high-level lifetimes of the IGBTs are different, the simulated excess carrier distributions with or without temporary clamp performed by AVC are presented. By appropriately adjusting the MOS-channel currents of series-connected IGBTs when the excess carrier concentration becomes low at the end of tail current, the voltage balancing among series-connected IGBTs would eventually be achieved with a well-damped AVC gate drive. Such a promising method can be utilized in practical high voltage application bringing great advantages.

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