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Design and Measurement Considerations for WBG Switching Circuits

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Keywords

Wide bandgap devices, Silicon Carbide (SiC), Gallium Nitride (GaN), Measurement, Current sensor.

Abstract

Wide Band Gap (WBG) transistors using materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) offer superior electrical and thermal properties, as well as fast switching capability. However, the high dv/dt and high di/dt may cause ringing with the parasitic inductances and capacitances in the switching loop, increasing overshoot voltages and reducing confidence in the design. Also, making accurate measurements of the switching behaviour without unduly loading the circuit under test is challenging and further impedes the development of WBG applications. This paper presents a prototype WBG Development Platform, built around a half-bridge switched inductive load test circuit. Additional circuits are integrated on to the main PCB for test and measurement purposes: These include a high bandwidth linear current gate-drive circuit and a high bandwidth on-board measurement system. These sub-circuits are described in detail in this paper, together with the switching waveforms that have been achieved during tests with SiC MOSFETs. The authors demonstrate a practical implementation for high frequency WBG power circuits.

I. Introduction

Wide Band Gap (WBG) transistors using materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) offer superior electrical and thermal properties, such as higher critical electric field and thermal conductivity, over conventional Silicon (Si) devices. For the same voltage and current rating, a WBG power semiconductor device offers smaller die area, provides higher operating temperature, higher operating frequency with lower switching losses and lower part-load conduction losses compared to an equivalent Si power device [1]. For example, SiC power devices only require a thin highly doped drift region to withstand a high blocking voltage. In this way, a SiC MOSFET device can be competitive in terms of electrical performance, whilst offering greater benefits at high switching frequencies when compared to conventional Si IGBTs. The increased operating frequency reduces the size of filter components which reduces the overall system cost and may also improve the converter efficiency.

Operating a SiC MOSFET device at high switching frequency imposes significant challenges: (1) The high dv/dt and high di/dt generated cause significant ringing issues with parasitic inductance and capacitance in the switching loop, (2) accurate measurements of the switching behaviour with high bandwidth and low phase lag are required to appraise performance during development, (3) stringent power circuit layout and gate-drive design are required to reduce the effects of parasitic inductances in order to approach ideal switching waveforms [2]–[6].

This paper presents a prototype WBG Development Platform, built around a half-bridge switched inductive load circuit, using SiC MOSFET power devices. Additional circuits are integrated on to the main PCB for test and measurement purposes: These include: (1) a high bandwidth linear current gate-drive circuit and (2) a high bandwidth on-board measurement system. These subsystems are described in detail in this paper, together with the switching waveforms that have been achieved during tests.

II. Parasitics and PCB Design

Parasitics in device packaging and the application circuit remain significant barriers to the wider adoption of WBG devices in power converter applications. At high switching frequencies, a successful converter design using these WBG power devices needs to involve considerations from both power electronics and RF design, with techniques from both fields being used to first understand and then eliminate the effect of parasitics. The main parasitic inductive elements are:

1. Common source inductance (CSI), is the inductance shared between the gate-drive and power circuit, both inside the device package and the external connectivity on the PCB. This can be extremely detrimental, since adding as little as 1 nH of CSI in a fast switching circuit can increase losses by 50% over an ideal case [7].
2. Gate loop inductance (GLI), is the area enclosed by the gate-drive current path to the switching die and the return path from the source connection back to the gate-drive 0 V. It can be reduced by careful PCB layout, with consideration given to cancellation of the magnetic field generated by this loop. A GLI above 5 nH can decrease the switching efficiency significantly and cause overshoot of the gate voltage at the switching die [7], [8]. Also, critical gate damping may not be achieved, resulting in switching instability and device failure [9].
3. Switched current commutation loop inductance (SCCLI), caused by the magnetic field generated when switching the load current from the top device to bottom device (or vice-versa) in a half-bridge switching topology. A SCCLI of 2 nH has been achieved in this work through careful PCB layout. The measured results are shown on a Smith Chart in Fig. 2(a). It has been found from previous work that loop inductances beyond this can be extremely detrimental to the circuit operation, causing voltage overshoot spikes and subsequent oscillations during fast switching transitions.

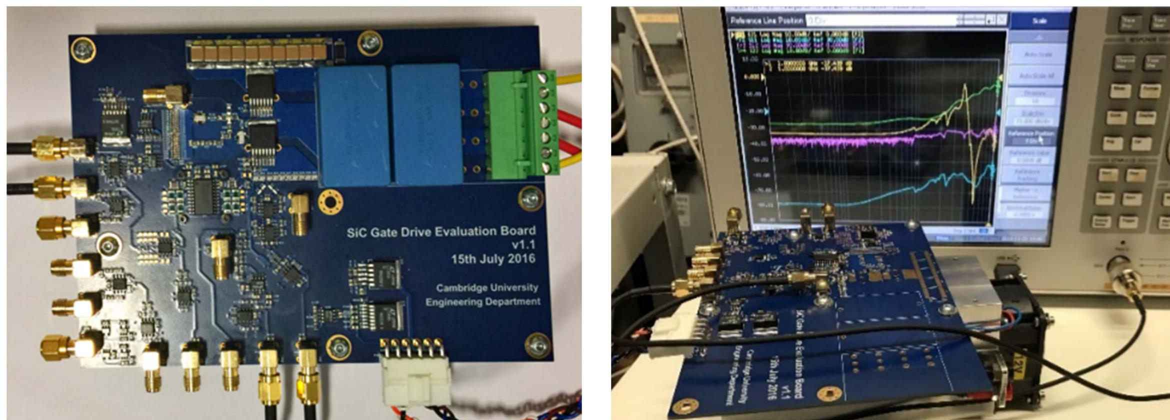

Fig. 1 (a) WBG development platform, and (b) testing sub-circuits with a Vector Network Analyser.

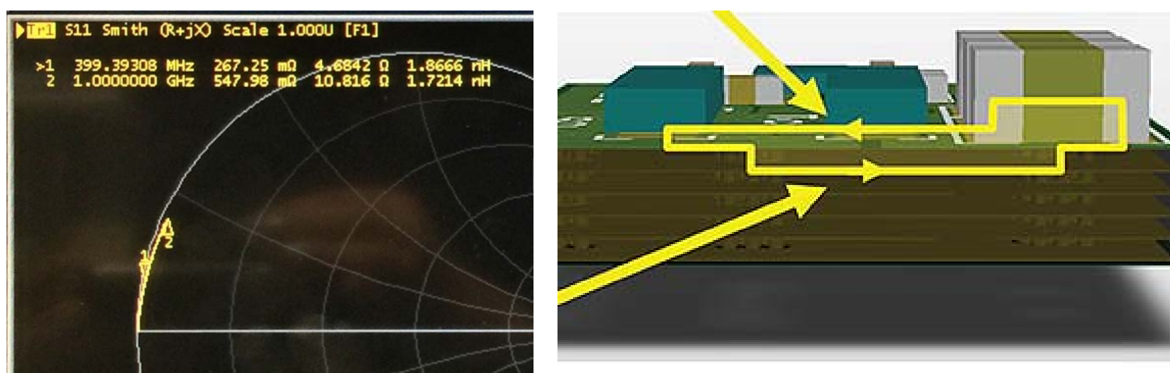

Fig. 2 (a) SCCLI measured on VNA (<2nH), (b) optimum loop inductance PCB layout cross-section.

The gate-loop and power-loop inductances have been measured using an Agilent E5061B Network Analyzer. The PCB and test-set up are shown in Fig. 1. The SiC MOSFET used is the low-impedance package C3M0065090J from Wolfspeed, rated for 900 V and 65 mΩ at 25 °C. The loop inductance has been optimised using magnetic field cancellation in a multi-layer PCB structure with currents flowing along the top-side of the board and returning through a mid-layer, as shown in Fig. 2(b).

III. Integrated Measurement

There is a limited choice of commercially available test equipment capable of accurately measuring the switching waveforms of WBG power circuits without significantly degrading the performance of the test setup. On-board measurement circuits have been developed here as solutions to the significant challenges posed by WBG switching circuits and are explored in this paper, as follows:

1. Very low inductance resistive-shunt circuit for high bandwidth I_S current measurement, offering minimal resistive power insertion loss or switching performance degradation.
2. V_{DS} measurement circuitry using a resistor-capacitor array to achieve high bandwidth and high precision with minimum propagation delay.
3. V_{GS} measurements are buffered by an on-board high bandwidth circuit, so as not to unduly load the gate-node or otherwise introduce unwanted noise or feedback effects.

All measurement circuits are integrated in to the test PCB, and offer high bandwidth, low propagation delay, and the capability to correctly drive 50 Ω cables and terminated scope inputs.

I_S Current Measurement Circuit

Measuring the current in the power switching devices without introducing undesirable commutation loop inductance is a challenging problem. There are many methods explored in literature to deal with these issues [10]. Most of these rely on measuring magnetic flux as a proxy for current, which introduces inductance as a by-product [11]. For WBG devices, where the current slew rate can be in the order of 100 A/ns, the inductance necessary for any practical magnetic flux measurement system will have a detrimental effect on the efficient and reliable operation of the switching circuit.

One solution to overcoming these limitations is to measure the voltage drop across a low inductance resistive shunt. The problems encountered by a practical implementation of such a circuit are that there will always be some amount of stray inductance, which will give an exaggerated gain lift at high-frequencies in the current measurement spectrum, and resistive power dissipation.

For these sorts of experiments, coaxial restive shunts are often employed, where the concentric current paths cause the magnetic fields to be negated and therefore there is at least theoretically zero inductance. In a practical implementation, the un-cancelled effects at the end of the coaxial shunt are considerable for the geometries needed for WBG circuits.

Instead, the current measurement solution used in this paper is as follows:

1. The resistive shunt is made as small as practicably possible, whilst still giving a reliable signal. A good target value in this study has been found to be 100 mV at full current.
2. The inductance of the resistive shunt has been reduced by paralleling small SMD resistors, with the return current path run directly underneath with a very thin dielectric insulator material (approx 100 μm thick) between. This gives an insertion inductance of around 300 pH.
3. The increase in measurement gain at high frequencies (>1 MHz) due to the small amount of remaining inductance is compensated for with a filter incorporated into the amplifier circuit.

Fig. 3 shows the current measurement circuit (without the added compensation filter, which is obfuscated and the subject of on-going research work). Fig. 4(a) shows the LT Spice simulation results frequency response and Fig. 4(b) shows the actual small signal measurement results using the Network Analyser. The real-world results have a little less bandwidth (150MHz) when compared to simulation.

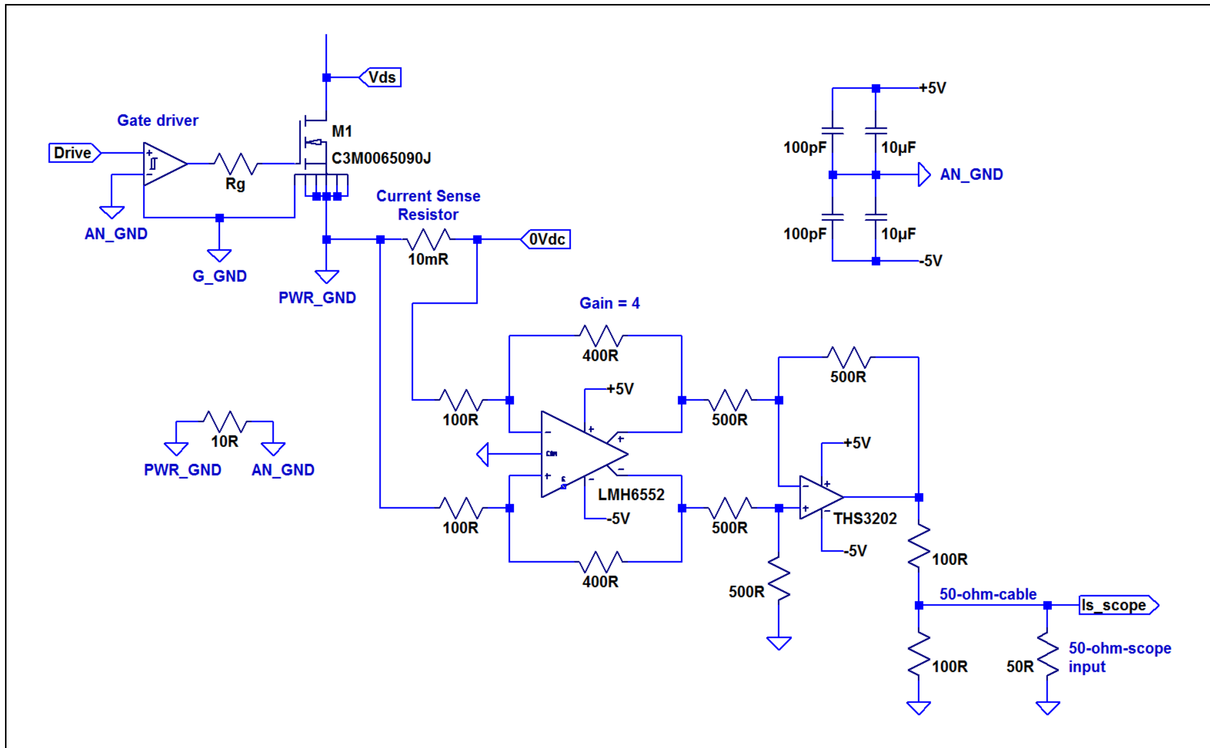

Fig. 3 Switched current I_S measurement circuit, with 50 ohm impedance output.

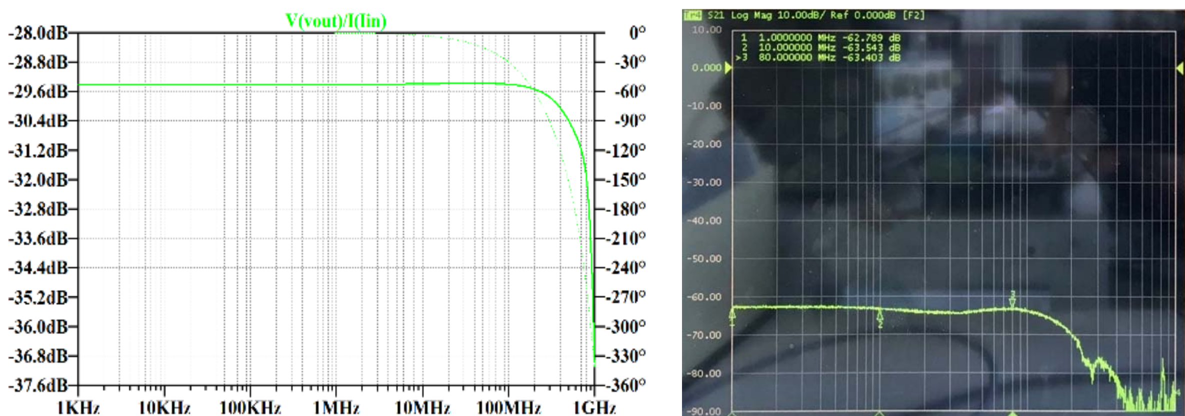

Fig. 4 (a) Current measurement circuit frequency response in LT Spice simulation, and (b) test results on Network Analyser (small signal).

V_{DS} High Voltage Measurement Circuit

The V_{DS} measurement of the switching-node in a typical half-bridge switched inductive load test setup can present significant challenges, such as:

1. High bandwidth to capture the fast slew rates and overshoot ringing of WBG devices.
2. Probe capacitance can load the switching node of the circuit.
3. Probe ground connections and shielded cable act as unterminated loops and antenna.

The measurement circuitry presented in Fig.5 is capable of achieving high performance measurement at high voltages without significant parasitic loading or power dissipation. It is based on a variable impedance potential divider buffered by a high impedance input op-amp and 50 ohm output circuit, which is impedance matched when driving a 50 ohm cable and 50 ohm terminated scope channel.

Due to practical component limitations, the parasitic capacitive effects of the op-amp, passive components and PCB become significant at high frequency requiring low signal path impedance. However, the impedance needs to be high at low frequency in order to minimise the power dissipation.

The solution presented here is a high resistance potential divider with a capacitor-resistor network connected in parallel. As the capacitors decrease in impedance with increasing frequency, but there remains some series resistance to limit the minimum impedance and dampen any effects due to the inductance of the capacitors. The frequency response in LT Spice simulation and actual circuit measurements on a Network Analyser are presented in Fig. 6.

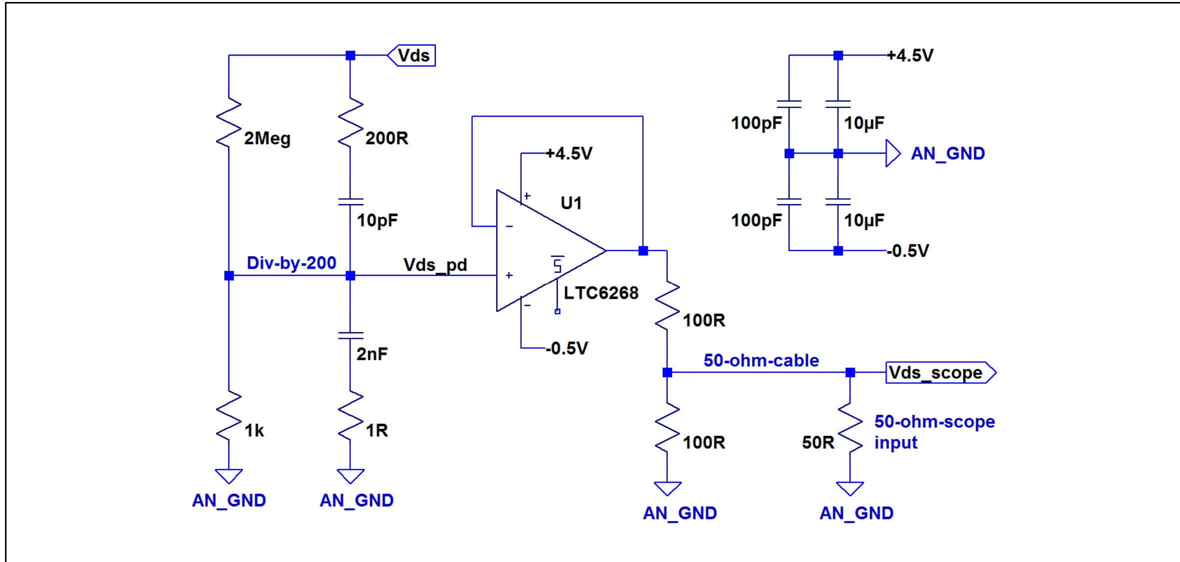

Fig. 5 Switched voltage V_{DS} measurement circuit, with 50 ohm impedance output.

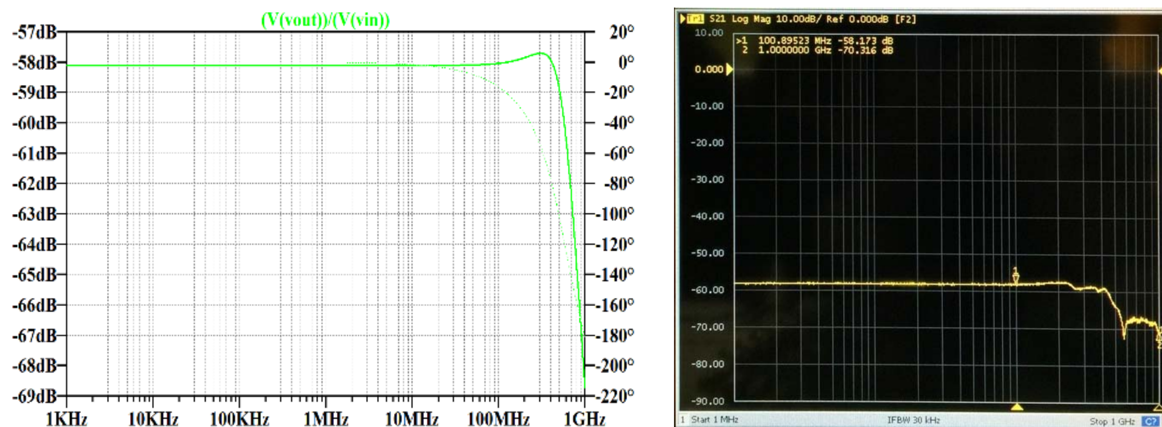

Fig. 6 (a) Voltage measurement circuit frequency response in LT Spice simulation, and (b) test results on Network Analyser (small signal).

IV. Linear Current Gate-drive Circuit

The most common problems associated with conventional resistive gate drives are:

1. The gate voltage during the Miller plateau region will vary with load current, so the voltage across the gate resistor, and therefore the gate current, will be dependent on load current. Thus, dv/dt will also vary with load current, and this effect can be more or less noticeable depending on the device type and design.
2. This Miller voltage also varies with junction temperature and gate drive temperature.
3. There is a complex relationship between these factors, gate resistor and switch timing.

The solution to these issues is to drive the gate with a controllable current source. As such, the gate current during the Miller plateau is independent of gate voltage and therefore load current.

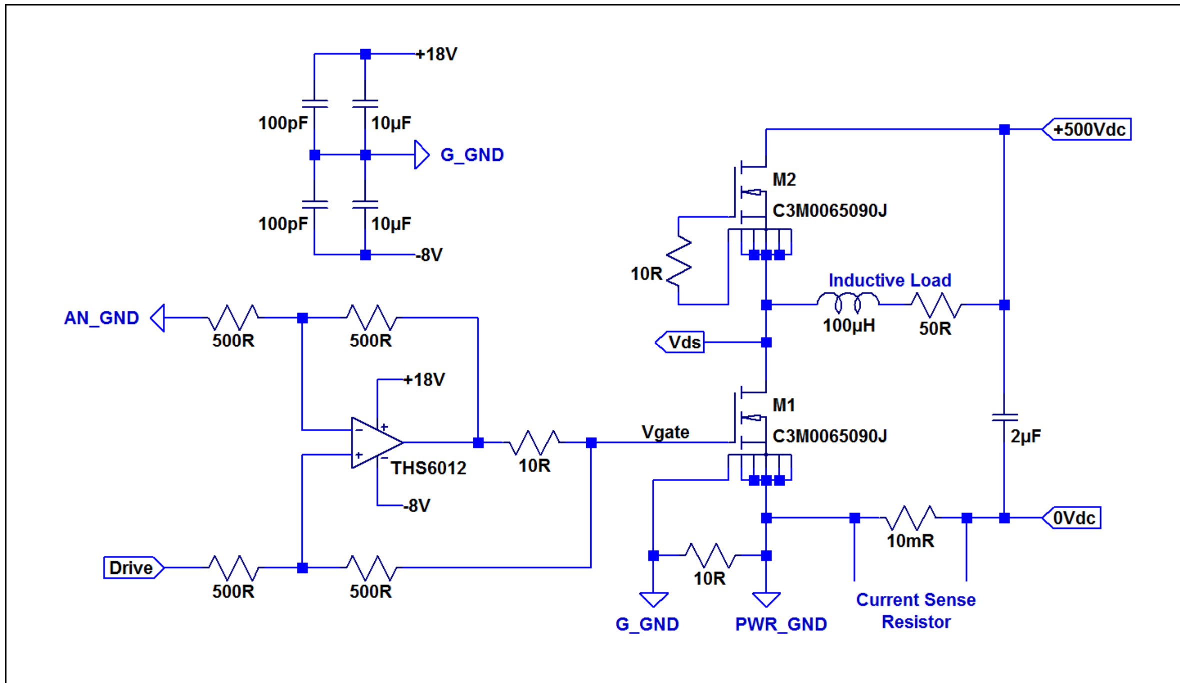

Fig. 7 Linear current gate drive circuit and half-bridge switched inductive load test topology. Gate drive has +/- 800mA output capability, over +18V / -8V V_G range.

A further improvement on this is to make the current drive controllable. This offers the possibility to vary the gate drive current according to a pre-set signal profile during the switching event or a feedback control signal. Such a feedback mechanism could be used to limit over voltage transients or over-current during short-circuit current conditions, and is the subject of further research.

The gate drive circuit presented here in Fig.7 can achieve a constant (defined) gate drive current. The simulation and test results (Fig.8) show that the proposed circuit is capable of driving a current into a capacitive gate load with a bandwidth in excess of 150 MHz. The test results in Fig.9 were carried out at varying values of V_G to show that the drive current and gain remains unaffected by gate voltage.

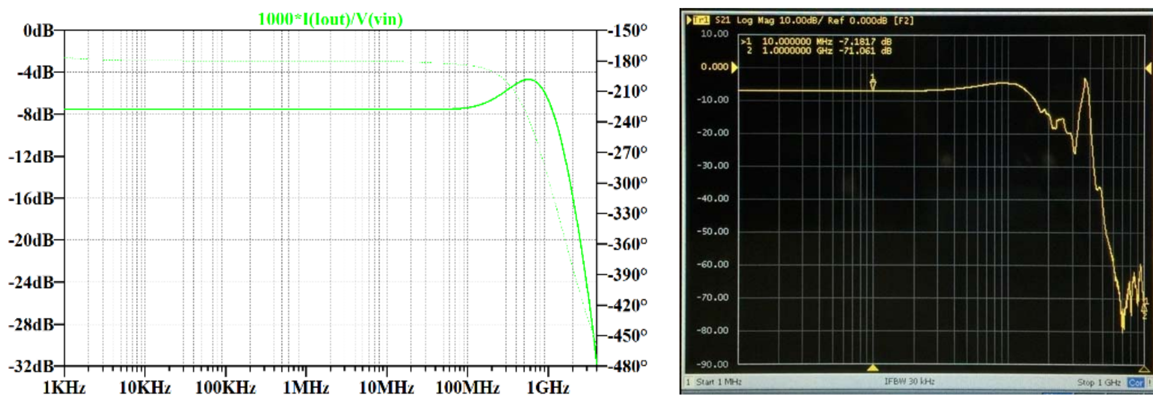

Fig. 8 (a) Current gate drive frequency response in LT Spice simulation, and (b) test results on Network Analyser (small signal) driving into a simulated capacitive gate load.

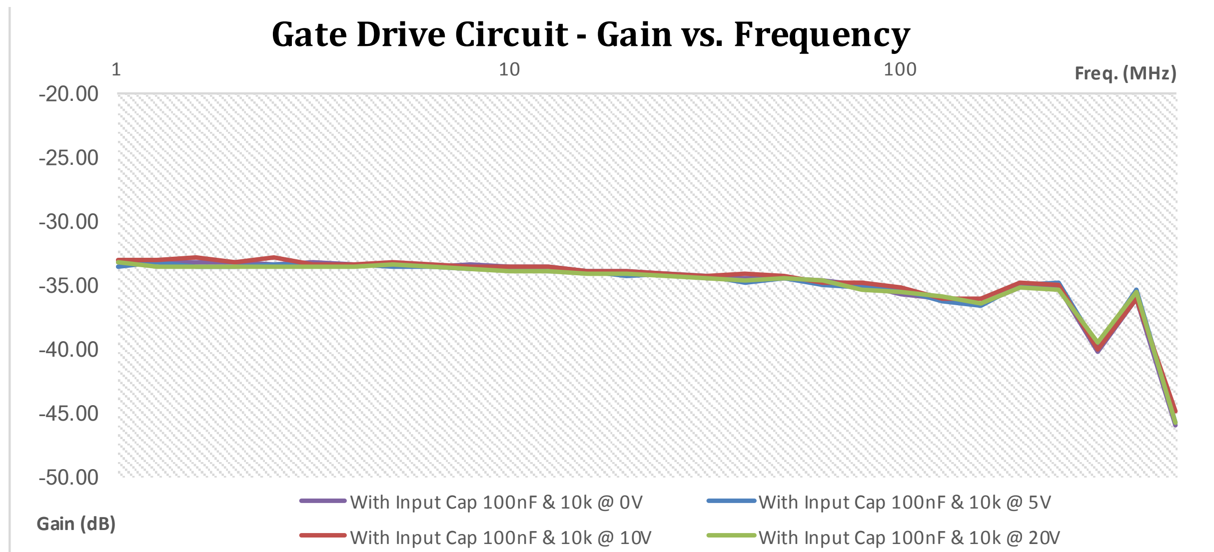

Fig. 7 Current gate drive (small-signal) response, tested at different V_G gate voltages.

V. Hard-switching Tests

The high performance switching and measurement circuit designs presented in this paper have been built and tested by the authors in order to verify their effectiveness. The test results achieved from switching this circuit at high-voltage and high-current are presented in this section.

The test set-up is as follows:

1. Two 900V Wolfspeed SiC MOSFETs in a half-bridge configuration. Switched inductive load of 100 µH, with a 50 Ω series resistor to dissipate the stored inductor energy after each switch cycle. Test cycle is a double-pulse at low duty to remove the need for thermal consideration.
2. 500 Volts DC bus provided by a bench-top DC power source, with sufficient localised de-coupling capacitance to adequately buffer the high peak demand current of 25 Amps.
3. Outputs from the various on-board measurement circuits, along with external measurement probes are included for comparison. Signals are measured on a 500 MHz LeCroy oscilloscope.

The turn-OFF and turn-ON waveforms are presented in Fig.10 and Fig.11 respectively.

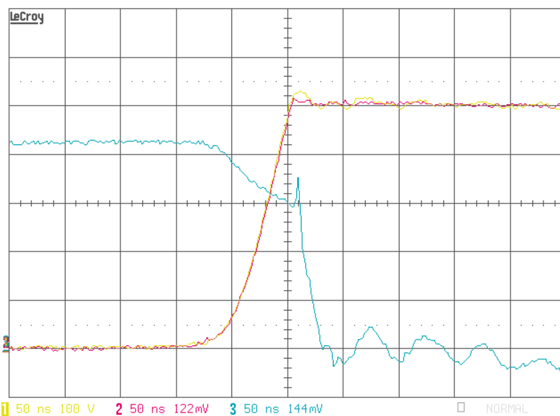

Fig. 10 Turn-OFF waveforms (50 nsec/div)
Ch.1 (yellow): 100:1 scope probe V_{DS}
Ch.2 (red): On-board V_{DS}
Ch.3 (blue): On-board I_S

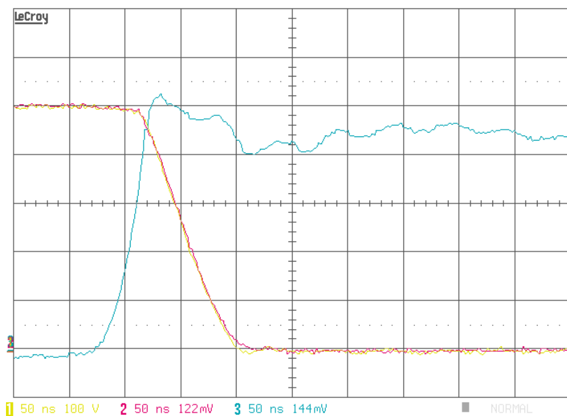

Fig. 11 Turn-ON waveforms (50 nsec/div)
Ch.1 (yellow): 100:1 scope probe V_{DS}
Ch.2 (red): On-board V_{DS}
Ch.3 (blue): On-board I_S

At turn-OFF, there is a slow initial rise of V_{DS} due to the large inherent output and reverse transfer capacitances of the SiC MOSFET at low V_{DS} voltage. As the voltage increases, these capacitances

drop dramatically and the device enters the main part of the V_{DS} switching region, which is both rapid and linear. The V_{DS} over-shoot at the end of this transition is small, with an absence of noticeable ringing. This is a result of the low parasitic circuit inductances, and clearly demonstrates the effectiveness of the techniques described in this paper. Interestingly, the rapid rise in V_{DS} causes a momentary drop in the measured device current I_S: This is due to the voltage change across the output capacitance of the top MOSFET device (which is in an OFF-state) and the resulting discharge current, which will be looked at in more detail in the next section. After the switch event, current ringing in the I_S waveform can be clearly seen, but the amplitude is small and the oscillations die away quickly, suggesting that the energy dissipated is also small.

At turn-ON, the waveforms are similarly well defined, as shown in Fig.11. The fall in V_{DS} remained smooth and linear during the entire turn-ON process, with no obvious ringing. The current rise in I_S is well controlled, followed by a small amount of overshoot beyond the load level. This is due to the output capacitance of the MOSFET devices and is discussed in more detail below.

It can be seen from both sets of waveforms that the calibrated on-board V_{DS} measurement showed good correlation with the 100:1 high-voltage scope probe, with the detail in the on-board measurement showing higher fidelity. The voltage measurement circuit shows less ringing than the scope probe.

The on-board current measurement circuit was checked and calibrated against an Agilent Hall-effect current probe. Since the Hall-effect current probe cannot be inserted into the Drain or Source connections without dramatically increasing the commutation loop inductance and therefore degrading switching performance, instead the load current was measured for comparison. Fig.12 shows that once calibrated, the correlation between the two measured currents is good during the on-state of the measured lower power device.

The waveforms at zero load current are shown in Fig.13: There is a ‘bump’ in the current waveform resulting from charging the drain-source capacitance of the upper device in the bridge leg during switching. This effect is seen in Fig.10 and Fig.11 superimposed on to the switching waveforms.

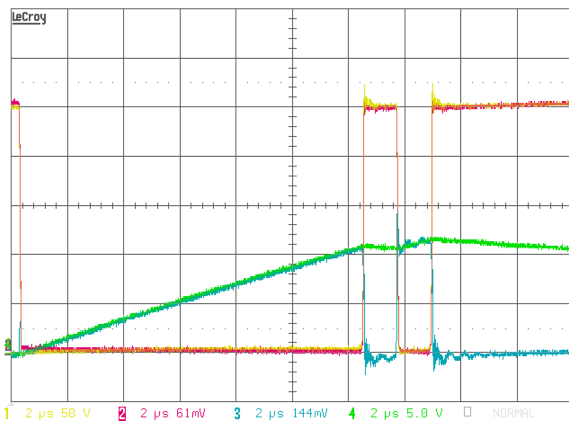

Fig. 12 Calibration of on-board current measurement circuit (Ch.3 blue) against an Agilent hall-effect current probe (Ch.4 green). Waveform shows double-pulse test cycle.

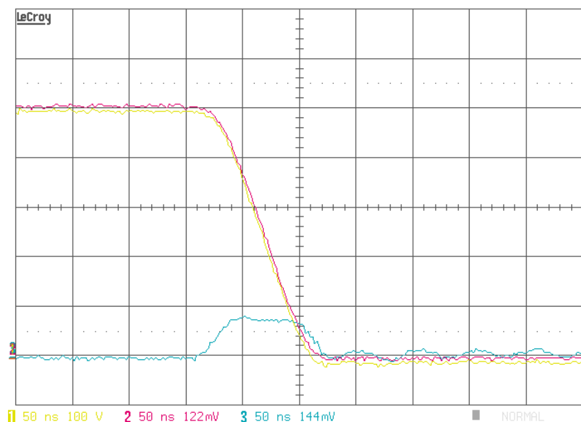

Fig. 13 Switching at zero current: Ch.3 (blue) shows switch node capacitance discharge current during dv/dt region at switch-ON.

VI. Discussion

High switching frequencies require rapid and efficient switching edges, therefore the PCB design must have minimal inductance in the switching loop, gate drive loop and common source connection. The techniques for reducing the critical parasitic inductances in the circuit through careful component selection and optimised PCB layout are not unusual in circuit design, but considerable extra care is required when deploying circuits designed for WBG power devices.

A method is described in this paper for cancelling magnetic fields resulting from looped current paths in the gate-drive and switched-current-commutation circuits, although here the underlying approach is to minimise the contained area of these current loops by minimising the dielectric between the opposing current paths. It is also necessary to consider the extra capacitance added to the switching node when minimising loop inductance by this method. As a result of the decreased parasitic inductance, the reduced ringing in current and voltage helps to mitigate EMI and the stress on the insulation in the packaging, load and circuit board. The work reported here represents a practical implementation to such requirements for SiC MOSFETs. The same methodology can also be applied for GaN devices.

Taking this approach results in the near-ideal switching waveforms, as demonstrated in the switching test results presented in this paper. Significantly, no voltage overshoots can be seen, indicating that the flux cancellation in the main switching loop has been successful in eliminating parasitic inductance. Similarly, the current source gate driver is also largely immune to the effects of stray inductance in the gate loop, and this is helped by the relatively low gate charge required. It should be noted that the full on-state in a SiC MOSFET is only achieved when the gate is fully charged to around 18V. The drain current and voltage slew rates are controlled during switching by the current source gate driver.

The non-intrusive measurement techniques do not adversely affect the performance of the switching circuit, and allow the investigation of the circuit performance, giving new insight into the switching behavior of these SiC MOSFET devices. Confidence in the on-board voltage measurement system comes from the good agreement with the external measurements and simulations. Indeed it is likely to have a superior bandwidth and is without doubt less prone to RF pick up (as demonstrated in Fig. 10 to 13). It can be seen that the on-board current measurement may be subject to some unwanted internal ringing due to parasitic capacitances associated with the op-amps, as indicated by Network Analyser tests. This unfortunately added ringing to the measured currents in the test waveforms. Also the bandwidth is limited to around 150 MHz, which falls short of what the simulation results suggest should be possible. Improved PCB layout and compensation of the op-amps is expected to resolve this in the next design iteration, but the approach remains valid.

The high performance linear current source gate drive circuit offers a high level of controllability over the switching trajectory of the SiC MOSFET tested. The tests shown in this paper have been initially carried out with a fixed drive amplitude, but it is anticipated that future work will demonstrate the benefits that can be achieved with a profiled gate drive signal and active feedback control. The optimisation of the control scheme can potentially reduce the effects of EMI, improve parallel current sharing and speed up the time taken to settle into the on-state. The use of digital systems to control the drive circuitry would enable increased accuracy, flexibility and scalability.

The integration of on-board measurement with stringent PCB layout and a customised gate-drive design forms the foundation of a SiC Development Platform, that can be used for power devcie performance appraisal. The principles demonstrated here for SiC can be adapted to GaN devices, which offer a further increase in switching speed. It is anticipated that this WBG Development Platform will be further developed to include protection systems and status monitoring, maximising the advantages, usability and reliability of WBG devices in real-world converter applications.

VII. Conclusions

The benefits of using SiC power semiconductor devices can only be realised when the power circuit, gate-drive and PCB layout are all properly optimised for fast switching. In this paper, the performance of such an optimised circuit is successfully demonstrated, showing that SiC MOSFETs can be built into practical circuits without slowing their switching and without incurring ringing. The circuit and PCB layout methods presented can be implemented with practical design and manufacturing techniques, with the test results showing excellent performance.

The circuits were designed after extensive studies focusing on minimising the impact of parasitics, with LT Spice simulations to model their effects. The parasitics were further investigated using a

Network Analyser. It is clear from the test results that the effects of parasitics do not need to dominate or limit the circuit behavior when correct design is employed.

The circuit design for the linear current source gate drive presented has the possibility to perform optimised gate controlled switching and it is anticipated that more sophisticated profiled drive strategies, closed-loop control and digital control systems will yield further benefits in the future, for improved performance, EMI and circuit protection. These developments require the high performance embedded non-intrusive measurement system presented. Clearly the final design in any application would eliminate some aspects of the measurement system, although some could be retained for control and protection purposes.

The test results show that SiC application development can be performed with an appropriate test platform and SiC MOSFETs have considerable potential for reliable high frequency power converters.

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