Temperature Evolution in Nanoscale Carbon-Based Memory Devices due to Local Joule Heating

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***Abstract*—Tetrahedral amorphous (ta-C) carbon-based memory devices have recently gained traction due to their good scalability and promising properties like nanosecond switching speeds. However, cycling endurance is still a key challenge. In this paper, we present a model that takes local fluctuations in sp^2 and sp^3 content into account when describing the conductivity of ta-C memory devices. We present a detailed study of the conductivity of ta-C memory devices ranging from ohmic behaviour at low electric fields to dielectric breakdown. The study consists of pulsed switching experiments and device-scale simulations, which allows us for the first time to provide insights into the local temperature distribution at the onset of memory switching.**

I. Introduction

ONE of the emerging candidates to bridge the gap between fast but volatile DRAM [1] and non-volatile but slow storage devices is tetrahedral amorphous carbon (ta-C) based memory [2]–[5]. It offers a very good scalability, data retention and sub-5 ns switching speeds [3], [4]. Amorphous carbon memory devices can be electrically and optically switched from the high resistance state (HRS) into the low resistance state (LRS) [6]. The electrical conduction in the LRS is thought to be through sp^2 clusters that form a conductive filament [5], [6].

Joule heating is assumed to be a primary contributor to resistive switching in ta-C [6]. The conductivity varies locally on the nanometer scale due to randomly distributed sp^3 and sp^2 sites [7]–[11] and hence, large local differences in current densities and hence in Joule heating can be expected.

A key challenge for carbon-based memory is endurance that is the number of cycles devices can be switched between LRS and HRS [4].

Excessive Joule heating could lead to the formation of large spatially-extended conductive filaments that make reversible switching back to the HRS difficult to achieve [10]. High temperatures and high current densities could also degrade the electrodes as the devices are switched back and forth multiple times.

Here, we investigate Joule heating and the resulting temperature distributions within ta-C memory devices at the onset of memory switching. This is essential to gain further insights into the switching mechanism and to address the key challenge of cycling endurance. The model we present accounts for both electric field and temperature dependence of the electrical conductivity in ta-C. We also consider local distributions of sp^2 and sp^3-rich clusters. The simulations are validated with experimental data.

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II. Memory Device and Characterisation

The memory devices consist of Pt (W) bottom (top) electrodes and a SiO_2 layer with cylindrical openings ranging from 50 nm, 100 nm and 200 nm into which 5 nm ta-C is deposited by the filtered cathodic vacuum arc. The sp^3 content is determined to ≈50 % using multi-wavelength Raman spectroscopy [12]. On-chip load resistors in series with the memory device limit the current flowing through the device during the SET (i.e. switching to LRS) process. The series resistors, 3 kΩ to 14 kΩ, are fabricated (e-beam lithography) next to the t-aC device and have a very small footprint to reduce their parasitic capacitance and hence the capacitive current flowing through the device during the SET process.

The reverse (RESET) switching process from LRS to HRS is reported to be induced by a large temperature gradient [4], [13] that arises between the conductive filament and the insulating matrix once an electric pulse is applied. Hence, no load resistor is used during the RESET process. The read out of the current during the programming is done across a 50 Ω resistor using an oscilloscope. The device resistance is read out

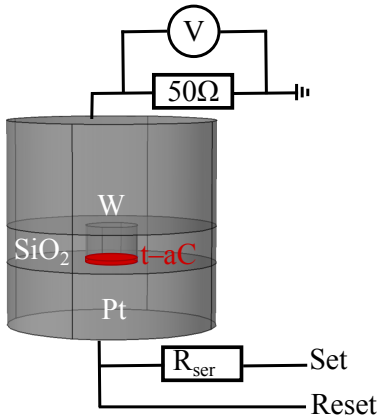

Figure 1. Schematic of the t-aC memory device with the electronic connections. SET and RESET pulses are applied to the bottom electrode. A load resistor limits the current during the SET process.

using a Source Measurement Unit (SMU). A schematic of the memory device and the electrical circuit is shown in Fig. 1. More fabrication details and information on the electrical equipment used for the switching studies can be found in [4].

To study both the field dependence and the temperature dependence of the t-aC conductivity, we measure the low-field conductivity of pristine devices (HRS) for temperatures from 85 K to 300 K using a cryogenic probing station (JANIS ST-500-2-UHT). The conductivity is plotted against $T^{-1/4}$ in Fig. 2 [14], [15]. The conductivity can be fitted by a straight

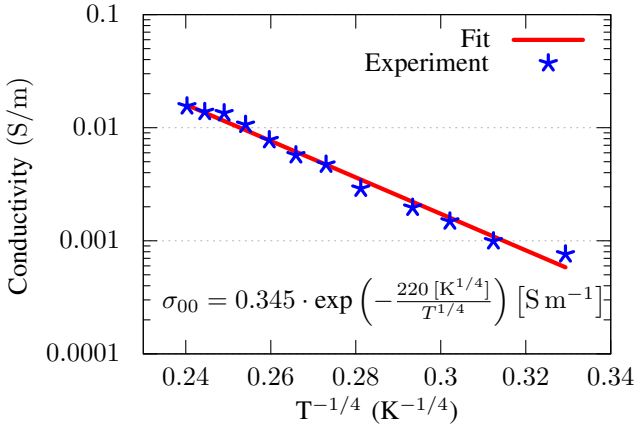

Figure 2. Conductivity of a carbon memory device measured at low voltages from 85 K to 300 K.

line over the whole temperature range which indicates that the electrical transport is mainly governed by hopping between localised states [16]–[18].

For intermediate and high electrical fields we found agreement with a Poole-type conduction behaviour ($\log\sigma \sim E$) for the field-dependent part of the conductivity (see section IV-B) [19], [20]. A Poole-type conduction behaviour is in agreement with reports of a high defect density in ta-C [21]. The transition from ohmic conduction to exponentially field-dependent conductivity can be described with a hyperbolic sine function as reported in [22], [23].

First, we look at experimental switching curves for voltage pulses of different durations. This allows us to examine the time response of the current on the applied voltage and, as a consequence, enables us to select a pulse long enough to exclude any 'un-desirable' transient effects prior to memory switching (e.g., due to thermal capacitances [24]). This, in turn, allows us to obtain a realistic temperature profile of the memory device at the onset of memory switching.

Therefore, we compare device I-V characteristics for a typical trapezoidal voltage with a 15 ns leading edge (LE) followed by a 45 ns plateau and a 15 ns trailing edge (TE) [4] with a quasi-static triangular pulse with 5 µs LE and TE. The AC voltage outputs were supplied by an Agilent 81150A Arbitrary Waveform Generator and captured with a Tektronix TDS3054B oscilloscope. The voltages applied across the device are plotted (blue) in Fig. 3 together with the voltage drop across the ta-C cell (black) and the corresponding currents. For noise reduction a 200 MHz software filter is applied to

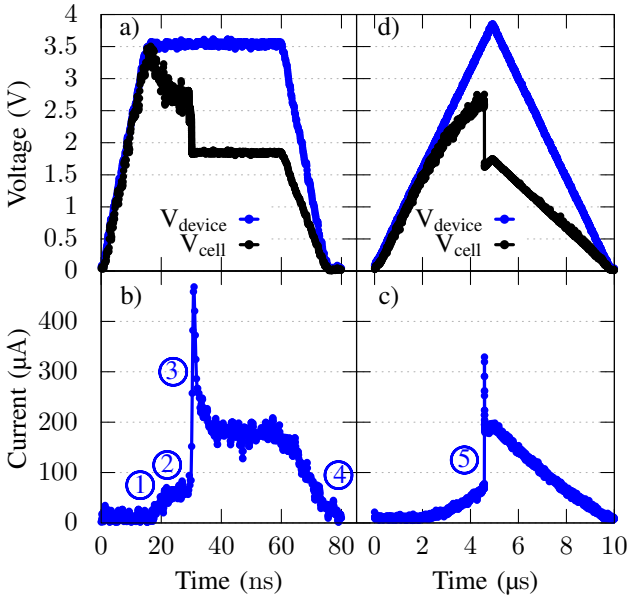

Figure 3. Applied voltage over devices (blue) and cells (black) together with the corresponding current response for a),b) fast (80 ns) and c),d) slow (10 µs) pulses.

the current and voltage signals during post-processing with the exception of the actual switching event.

The voltage pulse in Fig. 3a) reaches the plateau of the trapezoidal pulse after 15 ns, during which little or no increase in current is noted (1). The current then begins to increase (2) and a dielectric breakdown sets in after 30 ns (3). From then on the current follows the voltage pulse (4). This indicates that the electric field alone, in the absence of sufficiently large currents, does not trigger memory switching.

No such time lag can be observed for the slow, quasi-static pulse. There, the current, see Fig. 3c), always follows the voltage pulse Fig. 3d) until dielectric breakdown occurs after 4.8 µs (5) and the device is switched from its HRS into the LRS. Therefore, to validate the simulations we used a quasi-static pulse with 5 µs leading and trailing edge.

III. Model Implementation

To obtain the temperature distribution in the device when a voltage is applied we use a finite element software package (COMSOL®) to solve the coupled heat and Laplace equations.

To reflect local sp^2 variations in our model we randomly distribute different sp^2-rich cluster concentrations within the simulation cells.

To ensure that a relatively small number of sp^3-defects within a graphitic plane suffices to interrupt a conjugated π-network (see [8]) and to account for the sp^2 bonded clusters that do not participate in the conduction, we set the threshold for sp^2-like conduction to 92 % within each simulation cell. The simulated initial conductivity for a ta-C cell with randomly distributed sp^2 clusters is shown in Fig. 4.

An electric circuit was added to the electro-thermal model to account for a load resistor which, as seen in section II, is typically used to limit the current in the device after it has switched into the LRS.

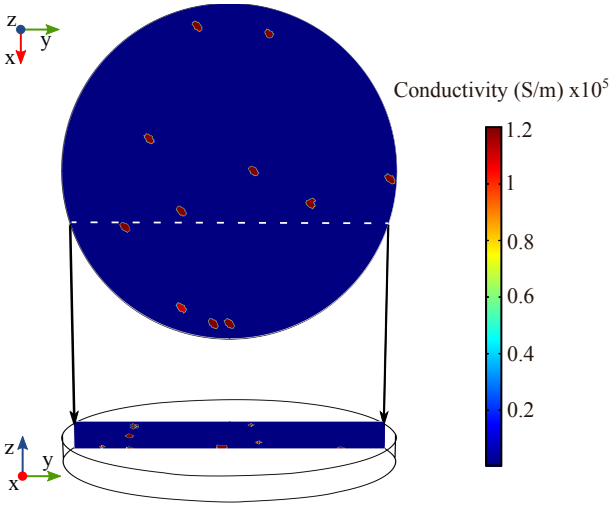

Figure 4. Initial conductivity for randomly distributed sp^2-like conductive clusters (red) close to the mid-plane at $z = 3.3\,\mathrm{nm}$ (top) and in the cross-section indicated by the dotted line (bottom).

The most important material properties used in the simulation are given in Table I.

Table I
MATERIAL PARAMETERS

sp^3-content (%)[1]	50
Beta (α, β)[2]	2.65, 2.65
$\sigma_{sp^2}\,(\mathrm{S\,m^{-1}})$ (cf. [13])	1.2×10^5
$\sigma_{sp^3,\mathrm{ohmic}}$ @ 300 K $(\mathrm{S\,m^{-1}})$	0.0115
$\sigma_{00}\ (\mathrm{S\,m^{-1}})$	$0.345 \cdot \exp\left(-\frac{220\,[\mathrm{K}^{1/4}]}{T^{1/4}}\right)$
$\sigma_{sp^3}\,(\mathrm{S\,m^{-1}})$	$\sigma_{00} \cdot \sinh\left(\frac{E}{9.5 \cdot 10^9 \left[\frac{\mathrm{V}}{\mathrm{m}}\right]}\right) + \sigma_{sp^3,\mathrm{ohmic}}$
Threshold σ_{sp^2} (%)	92
$\rho\ (\mathrm{kg\,m^{-3}})$ [25]	$3460 - 1880 \times sp^2$
$\lambda\ (\mathrm{W\,K^{-1}\,m^{-1}})$ [26]	$1.77 \cdot \rho - 2.82$
$C_{p,avg}\ (\mathrm{J\,kg^{-1}\,K^{-1}})$ [3]	2050

[1] Determined using multi-wavelength Raman spectroscopy
[2] Beta distribution with parameters α and β
[3] Average heat capacity of a memory cell computed from molecular dynamic simulations

IV. Results & Discussion

A. Isothermal Field-Dependent Conductivity

To validate our model and to determine the field-dependent part of the conductivity we compare our simulation results with an experimentally measured device conductivity (Keithley 2636B SMU). We use voltages high enough ($\approx 0.1\,\mathrm{V}$) to observe the exponential dependence of the conductivity on the applied voltage, but low ($\approx 1.1\,\mathrm{V}$) enough to keep the Joule heating below 1 K.[4] The maximum temperature within the cell is plotted as function of the applied voltage in Fig. 5. The simulated conductivity is compared with experimental data in Fig. 6. The simulation (red) describes the isothermal part of the conductivity (blue) very well up to electric fields of around $2 \times 10^8\,\mathrm{V\,m^{-1}}$.

[4]The temperature increase was verified a posteriori with simulation results.

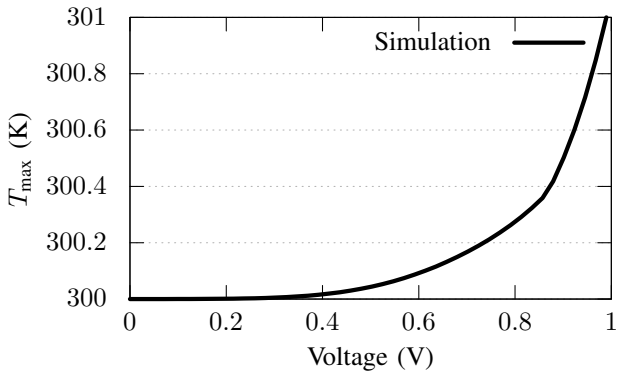

Figure 5. Local temperature evolution as function of the applied voltage.

B. Joule Heating Effects at Dielectric Breakdown

To investigate Joule heating effects at the onset of dielectric breakdown we apply the triangular switching pulse shown in Fig. 3d). For both, experiment and simulation a $13.3\,\mathrm{k\Omega}$ load resistor is used. The oscilloscope is programmed to ensure to capture the currents present at dielectric breakdown and as a consequence is insensitive to low currents at low voltages. Therefore, we only present here experimental high-field data for voltages from $|V| = 2.2\,\mathrm{V}$ until the onset of the dielectric breakdown (i.e. $|V| = 2.7\,\mathrm{V}$). The whole current vs. time response is depicted in Fig. 3c). The experimental and simulated conductivities are shown in Fig. 6.

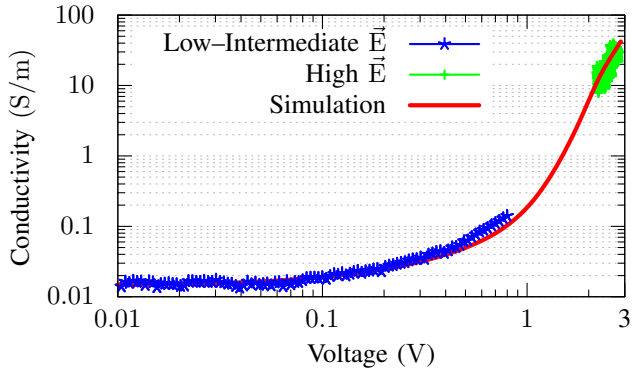

Figure 6. Measured and simulated conductivity of a carbon memory device as a function of the absolute value of the applied voltage.

The simulation describes the experimentally determined conductivity (blue, green) for all electric field ranges up to the point where dielectric breakdown ($|V| = 2.7\,\mathrm{V}$) occurs very well. The current flowing through the device at the onset of the dielectric breakdown is $|I| = 40\,\mu\mathrm{A}$.

The very good agreement between simulated and experimentally determined conductivity allows us for the first time to confidently investigate the local temperature distribution on the device-scale using a realistic switching pulse (see Fig. 3d). The temperature distribution within the memory cell is thus presented in Fig. 7.

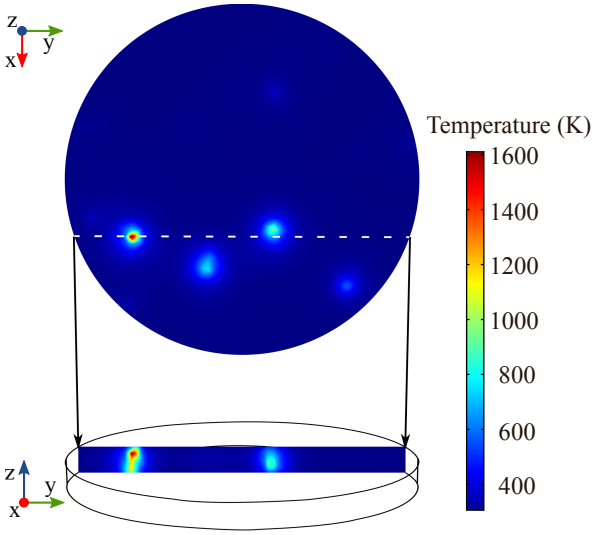

Figure 7. The temperature distribution of the x,y-plane (top) of the ta-C layer is shown at $z = 3.3\,\mathrm{nm}$ and in the y,z-cross-section (bottom) indicated by the dotted line; applied voltage is $-3.2\,\mathrm{V}$.

The highest temperatures are obtained at $z = 3.3\,\mathrm{nm}$, close to the mid-plane of the $5\,\mathrm{nm}$ thick ta-C layer. The electrodes remain close to room temperature, $311\,\mathrm{K}$ at the Pt//ta-C interface and $337\,\mathrm{K}$ at the W//ta-C interface which is expected as the metal electrodes act as heat sinks [4]. The observed high temperatures close to the mid-plane of up to $1615\,\mathrm{K}$ are in agreement with reports from molecular dynamic (MD) simulations [4]. The obtained hot spots are likely to indicate the origin where filament formation(s) after dielectric breakdown take(s) place.

These findings emphasise the relevance of taking local variations in conductivity into account and underline the importance of numerical modelling to obtain a detailed temperature profile of the memory cell which is not accessible otherwise. To illustrate this, a comparison between the average temperature in the memory cell and the maximum temperature is plotted in Fig. 8 as a function of the absolute value of the voltage drop across the memory cell.

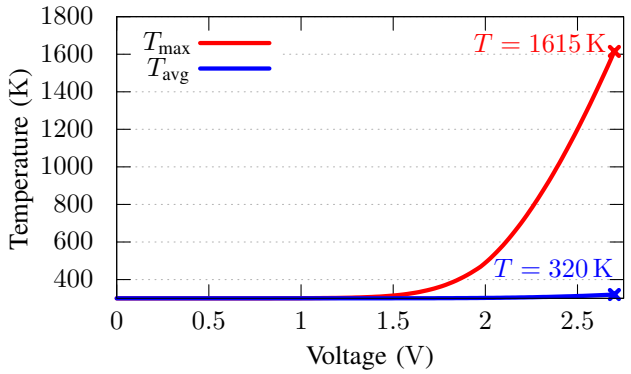

Figure 8. The maximum temperature inside the memory cell is plotted together with the average temperature as a function of the absolute value of the voltage across the memory cell.

The average temperature of the cell remains at moderate temperatures and reaches a maximum value of $320\,\mathrm{K}$, which agrees well with values reported in [27].

This finding is important as it emphasises that localised Joule-heating does not significantly affect the average temperature within the memory cell as long as the size of the hot spot is negligible in comparison to the lateral dimensions. Also, the highly localised hot spots prior to a filament formation provide evidence that memory switching in carbon-based devices is a temperature activated process which is in agreement with reports from MD simulations [4], [28], [29]. Note that an increase of the sp^2 content would lead to a reduced distance between the sp^2 conducting clusters in the sp^3 matrix. This in turn would result in larger currents and higher temperatures due to Joule heating being more effective. Once the lateral dimensions of the device approach the filament dimensions, it is suggested that the whole device can be re-amorphized using a standard reset pulse, which would increase the cycling endurance significantly [3].

V. Conclusion

We have successfully developed a simulation model that uses randomly distributed sp^2 and sp^3-rich clusters to constitute the material composition of ta-C memory devices. We have shown that by carefully taking the temperature and field-dependence of the sp^3 conductive clusters into account we are able to reproduce an experimentally obtained conductivity ranging over ≈ 4 orders of magnitude, all the way from ohmic conduction until dielectric breakdown. The simulation takes the overall sp^3 content into account and therefore reflects that an increasing sp^3 content will increase the resistivity and in turn a higher voltage will be required to produce a sufficiently high current density to induce dielectric breakdown.

As a result we have shown that Joule heating causes locally very high temperatures that, in turn, trigger a temperature activated process leading to material modifications. This temperature dependence emphasises the importance of adequate current control during the SET operation, so that sufficient current passes through the device for memory switching to occur and, at the same time, the current is limited to improve the cycling endurance. For further endurance improvements our findings suggest to decrease the gap between the electrodes, which increases the temperature gradient within the device during reverse switching. Future work aims to describe the full cycling dynamics including dielectric breakdown and reversible switching by implementing a cluster re-organisation that is based on a rate equation approach.

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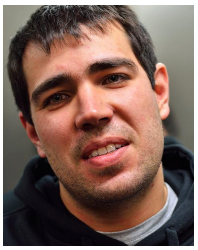

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