On the Specific On-state Resistance of Superjunction MOSFETs with a Compensated Pillar

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***Abstract*— In this paper, we report an analytical model for the on-state characteristics of a superjunction MOSFET featuring a compensated pillar between the n-pillar and the p-pillar is established. Since a large amount of lateral electric field is sustained in the compensated region, the doping concentration in the n-pillar can be enhanced significantly, leading to a substantial reduction in the on-state resistance of the superjunction. Simulation results proved that the use of an extra compensated pillar within the superjunction structure reduces the on-state resistance by 25% compared to that of a conventional superjunction for the same breakdown voltage.**

***Index Terms*—Superjunction, JFET, Compensated.**

I. Introduction

The reduction in specific resistance, R_{sp}, of superjunction (SJ) metal-oxide-semiconductor field effect transistors (MOSFETs) is a key factor in meeting application requirements, such as high energy efficiency and reducing the fabrication cost [1]. For this, several novel ideas have been suggested, such as the use of an oxide field plate between the n-pillar and p-pillar (p/oxid/n) [2], p/n/high-k dielectric pillar [3], a gate-driven accumulated pillar [4], p/n/oxide/undoped poly-Si/oxide pillar [5] and three-dimensional hexagonal pillar [6]. However, the above structures require additional fabrication steps (increased cost) and/or are subject to reliability challenges such as hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB).

Here we discuss an alternative structure to reduce the R_{sp} in a superjunction MOSFET while maintaining a conventional fabrication process. As shown in Fig. 1, a compensated pillar is inserted in between the p-type and the n-type pillar. The compensated pillar can be formed by deep diffusion or overlapping implantations to yield the same amount of the n-type dopant and the p-type dopant in a certain width, γd ($0 < \gamma < 1$). Even though the compensated (intrinsic) region decreases the conducting path of the n-pillar, the parasitic depletion width toward the n-pillar can be reduced by increasing the doping concentration. Also, a large amount of the drain to source voltage, V_{DS}, is to be sustained across the compensated region as shown in Fig. 1 and, therefore, the parasitic depletion width in the n-pillar can be reduced more than that of the conventional superjunction structure ($\gamma = 0$). This study provides an analytic model for a superjunction MOSFET with a compensated pillar and investigates the advantages over the conventional superjunction MOSFETs. For this, we do not take into account the channel resistance and we assume that the doping concentrations (N_D and N_A) and the widths of the p-pillar and the n-pillar are the same for the charge balance.

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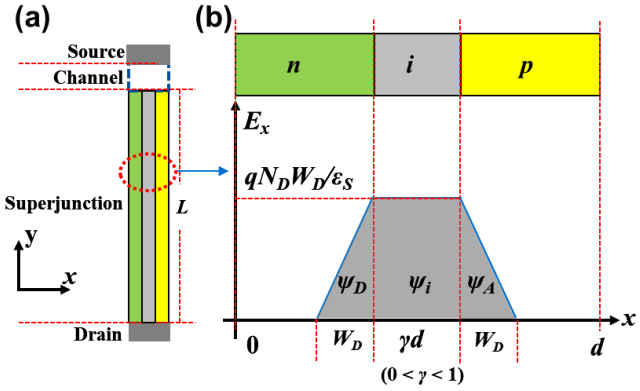

Fig. 1. A schematic illustration of (a) a compensated pillar superjunction structure and (b) the lateral electric field and the depletion width in a compensated superjunction at a given potential.

II. Ideal Approach

The width of the compensated pillar is γd ($0 < \gamma < 1$) and the compensated pillar is located in the centre of the superjunction structure as shown in Fig. 1. The depletion width towards the conducting n-pillar, W_D, was ignored. The ideal $R_{sp.ideal}$ of this structure can be written as

$$R_{sp.ideal} = \frac{1}{qN_D\mu_n}\frac{L}{Z(d-\gamma d)/2}dZ = \frac{2L}{qN_D\mu_n}\frac{1}{(1-\gamma)} \quad (1)$$

where q, μ_n, Z, and L are unit charge, doping dependent electron mobility, depth of the pillar (the 3rd dimension into the paper), and the length of the pillar, respectively. When the superjunction is fully depleted, the lateral electric field, E_x should be less than the critical electric field, E_C [7]:

$$E_x = \alpha E_C = \frac{qN_D}{\varepsilon_S}\left(\frac{d-\gamma d}{2}\right), (0 < \alpha < 1). \quad (2)$$

where ε_S is the permittivity of the semiconductor material. Since the square of the critical electric field, E_C^2, is the sum of the square of the lateral electric field, E_x^2, and the square of the vertical electric field, E_y^2, the vertical electric field becomes

$$E_y = \sqrt{(1-\alpha^2)}E_C . \quad (3)$$

The breakdown voltage, V_B, is the sum of the voltage drops across the doped pillar region V_L, the compensated region V_i, and the vertical voltage drop V_V. Assuming the length of the superjunction, L, is relatively long compared to the cellpitch, d, the breakdown voltage, V_B can be written as

$$V_B = V_L + V_i + V_V$$
$$= \alpha E_C\frac{(1+\gamma)}{2}d + E_C L\sqrt{1-\alpha^2} \approx E_C L\sqrt{1-\alpha^2} . \quad (4)$$

By inserting equations (2) and (4) into (1), the ideal R_{sp} has the following material form,

$$R_{sp.ideal} = \frac{V_B}{\alpha\sqrt{1-\alpha^2}\,\mu_n \varepsilon_S E_C{}^2} d = \frac{2V_B}{\mu_n \varepsilon_S E_C{}^2} d \,, \tag{5}$$

where α is $1/\sqrt{2}$ to minimize the $R_{sp.ideal}$. The material figure of merit (FOM) V_B/R_{sp} given by equation (5) is the same as the previously reported ideal FOM of a conventional superjunction MOSFET ($\gamma = 0$) [7]–[9].

III. JFET Approach

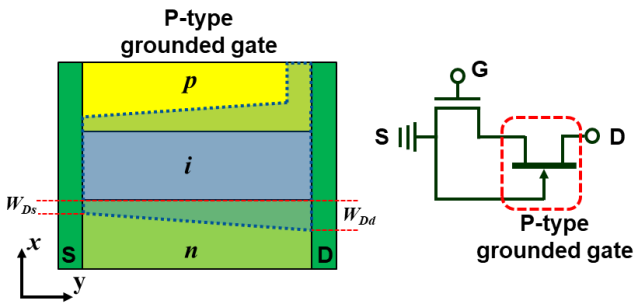

Fig. 2. A schematic illustration of depletion width profiles in a compensated pillar superjunction and its JFET inner circuit.

For a V_{DS} dependent analysis of a compensated pillar superjunction R_{sp}, a grounded gate junction field effect transistor (JFET) model is provided in Fig. 2 [8], [9]. The p-pillar of the superjunction is the gate of the JFET (grounded) and the n-pillar is the channel of the JFET. The depletion width, W_{Ds}, is formed by the built-in potential, ψ_{bi}, and W_{Dd} is formed by $\psi_{bi} + V_{DS}$. As shown in Fig. 1 and 2, the potential, $\psi(y)$, induced by $\psi_{bi} + V_{DS}$ is sustained across the p-i-n region and, the depletion width (before pinch-off of the pillars), W_D, has the following relationship:

$$\psi(y) = \psi_D + \psi_A + \psi_i = \frac{qN_D}{\varepsilon_S} W_D{}^2 + \frac{qN_D}{\varepsilon_S} W_D \gamma d \,. \tag{6}$$

Where the ψ_D and ψ_A are the same due to the symmetrical structure. From equation (6), W_{Ds} and W_{Dd}, become

$$\sqrt{\frac{\varepsilon_S \psi_{bi}}{qN_D} + \frac{\gamma^2 d^2}{4}} - \frac{\gamma d}{2} = W_{Ds} \,, \tag{7-1}$$

$$\sqrt{\frac{\varepsilon_S (\psi_{bi} + V_{DS})}{qN_D} + \frac{\gamma^2 d^2}{4}} - \frac{\gamma d}{2} = W_{Dd} \,. \tag{7-2}$$

Based on the above depletion widths, the sheet charge density, Q_n (cm^{-2}), in the n-pilar leads to

$$Q_n(y) = qN_D\left(\frac{d-\gamma d}{2} - W_D(y)\right). \tag{8}$$

The drain current, I_D, has the following relationship

$$I_D = \frac{Z}{L}\int_0^L Q_n(y) v(y) dy \,, \tag{9}$$

where $v(y)$ is the electron velocity in the n-pillar:

$$v(y) = \mu_n \frac{\partial \psi}{\partial y} \,. \tag{10}$$

By inserting equations (6), (7), (8) and (10) into (9), and solving equation (9), the drain current leads to

$$I_D = \frac{Z\mu_n q^2 N_D{}^2}{\varepsilon_S L} \times \left\{ -\frac{2}{3}\left[\left(W_{Dd} + \frac{\gamma d}{2}\right)^3 - \left(W_{Ds} + \frac{\gamma d}{2}\right)^3\right] + \frac{d}{2}\frac{\varepsilon_S V_{DS}}{qN_D} \right\}. \tag{11}$$

From equation (11), the R_{sp} with respect to the applied V_{DS} for a compensated superjunction can be obtained as

$$R_{sp} = \frac{V_{DS}}{I_D} dZ = \frac{\varepsilon_S dL}{\mu_n q^2 N_D{}^2} \times \frac{V_{DS}}{-\frac{2}{3}\left[\left(W_{Dd} + \frac{\gamma d}{2}\right)^3 - \left(W_{Ds} + \frac{\gamma d}{2}\right)^3\right] + \frac{d}{2}\frac{\varepsilon_S V_{DS}}{qN_D}} \,. \tag{12}$$

When the V_{DS} approach zero, the R_{sp} given by equation (12) has a minimum value:

$$\lim_{V_{DS}\to 0} R_{sp}(V_{DS}) = \frac{2L}{\mu_n qN_D}\frac{1}{1-\gamma}\frac{d-\gamma d}{d-\gamma d-2W_{Ds}} = R_{sp.ideal} \times \frac{d-\gamma d}{d-\gamma d-2W_{Ds}} \,. \tag{13}$$

Equation (13) is the multiplication form of $R_{sp.ideal}$ by the conducting path ratio where the conducting path is narrowed by the built-in depletion width, W_{Ds}. If the width of the compensated pillar becomes zero, equation (13) leads to the conventional superjunction R_{sp} [8], [9]:

$$\lim_{\gamma\to 0} \frac{2L}{\mu_n qN_D}\frac{1}{1-\gamma}\frac{d-\gamma d}{d-\gamma d-2W_{Ds}} = \frac{2L}{\mu_n qN_D}\frac{d}{d-2W_{Ds}} \,. \tag{14}$$

Therefore, the R_{sp} forms given by equations (12) and (13) are compatible with the conventional superjunction (without a compensated pillar) MOSFETs.

Fig. 3 shows the R_{sp} ratio of the compensated SJ ($0 < \gamma < 1$) and the conventional SJ ($\gamma = 0$). The concentration of the pillars at a given cellpitch can be calculated from equation (2):

$$\frac{1}{2}N_D = \frac{1}{2}\left(\frac{1}{\sqrt{2}}\frac{E_C\varepsilon_S}{q}\left(\frac{2}{d-\gamma d}\right)\right). \tag{15}$$

For a practical approach, the concentrations of the pillars were the half of the optimum value. The critical electric field models were borrowed from Baliga's study [10]:

$$E_C(Si) = 4010\times(N_D)^{1/8} \,, \tag{16}$$

The electric field dependent mobility at a given V_{DS} follows a previously established empirical model [8], [9],

$$\mu_n(V_{DS}) = \mu_{n0} \Big/ \left(1+\left(\frac{V_{DS}}{E_C L}\right)^{\frac{1}{m}}\right)^{3m} \,, m = 1.32 + 4\gamma \,. \tag{17}$$

Where μ_{n0} is the mobility when V_{DS} is 0V.

As shown in Fig. 3, the Si SJ with a compensated pillar shows a reduction in the R_{sp} by 10 ~ 30 % compared to the conventional SJ and the reduction is further enhanced as V_{DS} increases up to 3 V. This is due to the fact that the parasitic JFET effect, which obstructs the current conduction path, is less significant in the compensated pillar SJ than in the conventional SJ. The reason for this can be easily understood from Fig. 1 where a large portion of the potential is dropped across the compensated pillar region, rather than in the n-pillar.

Fig. 4 shows the drain current simulation with respect to the applied V_{DS}. The analytical model given by equation (11) showed a good agreement with the simulation result and the compensated pillar structure showed R_{sp} reduction of ~25% over the conventional structure owing to the high n-pillar doping concentration. Fig. 5 shows the breakdown voltage simulation. The compensated superjunction V_B was very similar to that of the conventional superjunction and this should be attributed to the flat lateral electric profile in the compensated pillar. As can be seen in Fig. 5(a), the electric field profile in the compensated region is flat with a high value and, therefore, it can sustain more drain voltage even with a high doping concentration.

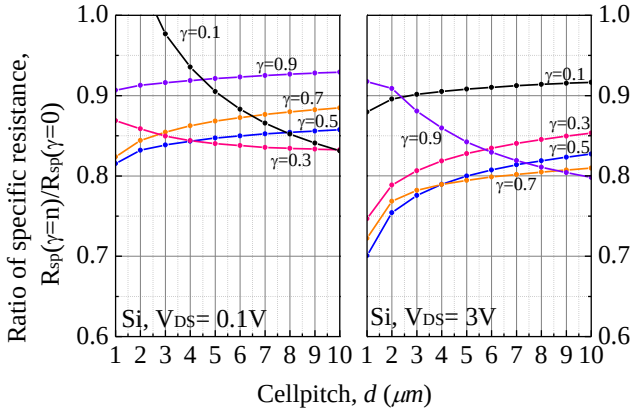

Fig. 3. R_{sp} ratio of the compensated SJ ($0 < \gamma < 1$) and the conventional SJ ($\gamma = 0$) with respect to the cellpitch.

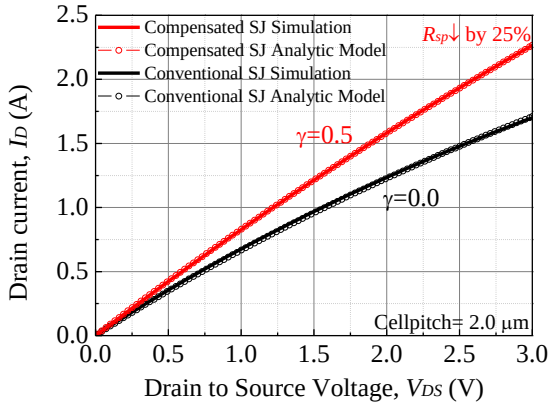

Fig. 4. TCAD drain current simulation result and analytic model in this study for the compensated pillar (red) and the conventional pillar (black) when the cellpitch is d= 2 μm. The length of pillar, L= 40 μm, the number of cells: 2.0 ×10^5, N_D (γ = 0.5) = 2.19 ×10^{16} cm^{-3}, and N_D (γ = 0) = 9.91 ×10^{15} cm^{-3}.

Fig. 6 presents inductive switching characteristics for the devices given by Figs. 4 and 5. The parasitic inductances were ignored. Both devices show similar dv/dt and di/dt during turn-on and turn-off. The only difference, though not significant, is the rapid drain voltage rising point (conventional pillar: 14 V and compensated pillar: 26 V) during the turn-off where the accumulation region below the gate oxide becomes depleted. As previously reported [11], a highly doped n-pillar below the gate oxide requires a higher drain voltage to be depleted.

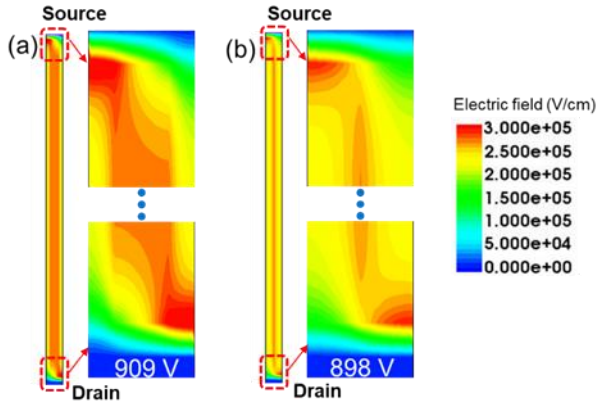

Fig. 5. 2D TCAD breakdown voltage simulation result and the electric field profile for (a) the compensated pillar (b) the conventional pillar when the cellpitch is d= 2 μm. The length of pillar, L= 40 μm, N_D (γ = 0.5) = 2.19 ×10^{16} cm^{-3}, and N_D (γ = 0.5) = 9.91 ×10^{15} cm^{-3}.

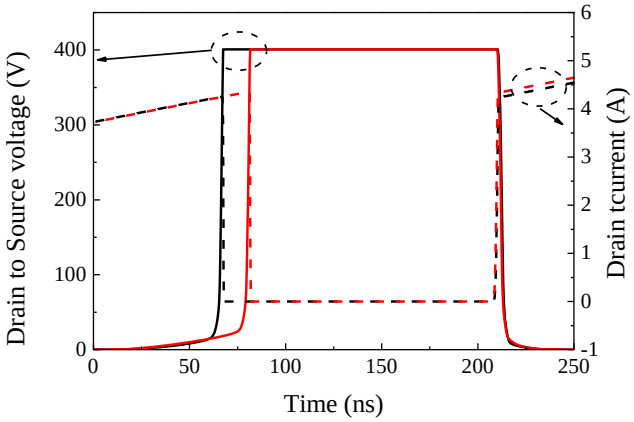

Fig. 6. TCAD inductive switching simulation result for the conventional SJ (black, γ = 0) and the compensated pillar (red, γ = 0.5) when the cellpitch is d= 2 μm. The length of pillar, L= 40 μm, the number of cells: 4.0 ×10^6, N_D (γ = 0) = 9.91 ×10^{15} cm^{-3} and N_D (γ = 0.5) = 2.19 ×10^{16} cm^{-3}.

IV. Conclusion

An analytical model for a compensated pillar SJ MOSFET has been developed by using a grounded JFET theory. This model accurately predicts the on-state resistance and the drain current at a given drain voltage. Also, this model is compatible with the conventional SJ MOSFET. It has been found that the compensated pillar SJ MOSFET can reduce the R_{sp} by 10 ~ 30 % compared to that of conventional SJ MOSFET.

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