Derivation and analysis of a novel bi-directional non-isolated multi-level DC-DC (MLDC) converter

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Abstract

A novel non-isolated Multi-level DC/DC (MLDC) converter using vertical interleaving technique is reported in this paper. This MLDC offers a wide range of voltage transfer ratio by using reduced number of low voltage power electronic devices and reduced size of the DC inductor, making this converter a potential candidate solution for high power Medium to Low Voltage (MV to LV) DC/DC conversion such as energy storage connection to Medium Voltage (MV) systems or drives. The derivation of the generic topology and power electronic device voltage rating selection have been given. Design considerations and all possible arrangement of the vertical interleaving sequences used in this MLDC has been introduced with mathematical expressions.

1 Introduction

Emerging applications of DC distribution networks used in renewable energy generation and transportation require DC-DC converters capable of converting voltage with a high ratio between the input and output, e.g. from LV (<1.5 kV) to MV (10 kV) and delivering high power (hundreds of kWs or MWs). Many research activities focus on using isolated AC transformers to increase voltage change ratio in the intermediate stage in the form of DC-AC-transformer-AC-DC. To reduce the footprint of the transformer and losses from power electronic devices, the high-frequency transformer (tens of kHzs) and soft-switching strategies have been preferred and intensively investigated, such as the Dual Active Bridge (DAB).

However, it is challenging to design high-frequency transformers for high voltage and power applications due to limitations from magnetic materials and high costs. Non-isolated DC-DC converters without transformers, therefore, show benefits but voltage constraints of power electronic devices and the large DC inductor have become two main challenges for conventional non-isolated DC-DC converters [1]. The common solution to overcome the voltage constraint of the individual device for high voltage is to have multiple switching devices connected in series and switched synchronously. The high voltage change ratio requires very high or low duty cycles, resulting in large ripple currents at the

DC inductor. Parallel interleaving techniques have been commonly adopted to overcome current ripple without largely oversized DC inductors. However, this conventional topology using the series device with parallel interleaving solution employs a large number of switches and exhibits many issues such as unequal sharing of voltage among devices and challenges for inductor design to optimise parallel interleaving.

In this paper, a novel multi-level DC-DC converter (MLDC) using vertical interleaving technique has been proposed and investigated. The derivation of the generic MLDC has been firstly introduced with a comparison to conventional half-bridge based buck or boost converters. A four-level (4L) MLDC has been used as an example to show modulation arrangement. The concept and operation have been validated by both the simulation and experiments.

2 Converter topology

The MLDC topology can be considered as a cascaded multiple Boost/Buck converters. Each sectional converter operates similarly to the conventional Boost/Buck converter. A novel vertical interleaving technique is used to ensure only a sectional DC voltage is applied to any individual power electronic device so low voltage rating devices can be used for high voltage applications. The current ripple is also reduced without increasing device switching frequency by using this vertical interleaving technique. Low voltage power electronic devices and smaller DC reactor are used to increase the efficiency and power density of the DC/DC converter for large DC transfer ratio, especially connection between LV and MV.

2.1 Topology derivation of generic multi-level topology

The architecture of MLDC is shown in Fig 1, which is derived from the three-level (3L) DC-DC converter by introducing the Middle Branch (MB) in which two active power electronic devices with their freewheeling diodes are connected in series with opposite direction so the current can be controlled flowing bi-directionally [2], [3], [4]. Two MBs with one Vertical Branch (VB) in which one power electronic device is used comprise a Middle Section (MS). The Top Branch (TB) and Bottom Branch (BB) are formed by multiple devices connected in series in the same polarity so the current flows unidirectionally at these two branches. The number of switches at the TB and BB depends on the number of sections used in

the MLDC in order to ensure equal voltage stress at the individual device of the top and bottom branches [5].
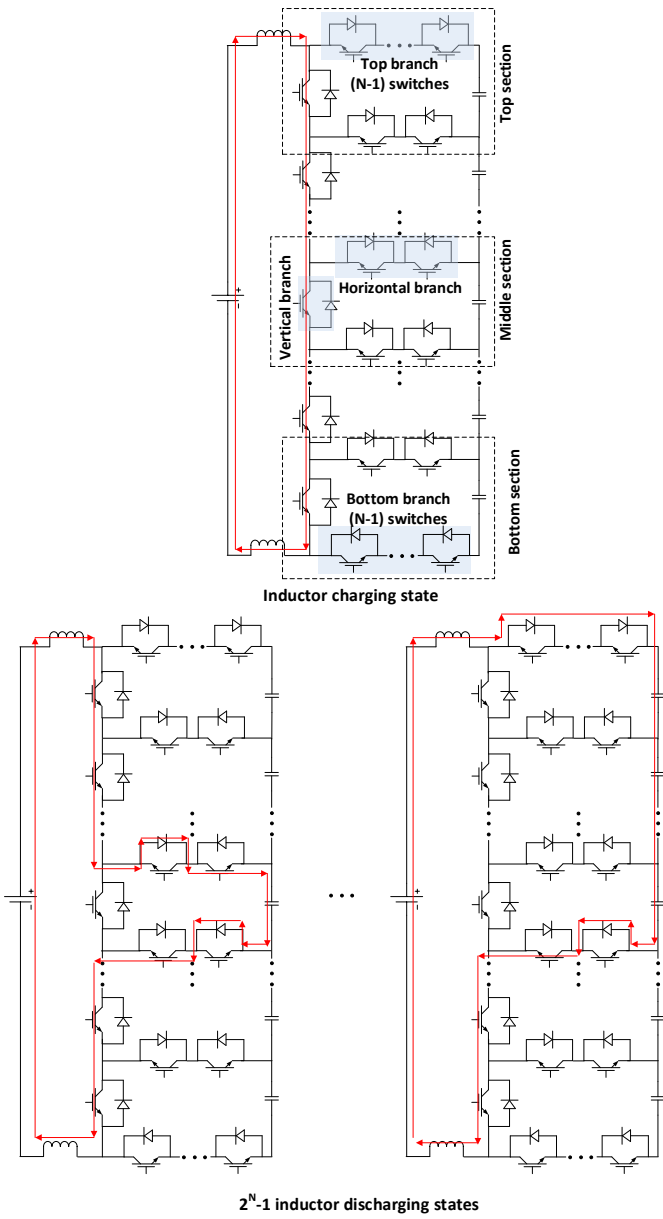

Figure 1 Inductor charging and discharging states (step-up)

Top Section (TS) is formed by the TB, one VB and one MB and the Bottom Section (BS) is formed by the BB, one MB and one VB. The capacitor at the high voltage DC side is equally divided into all sections and each TS, MS and BS are connected to one sectional capacitor. The nominal voltage of each sectional capacitor should be same to any single power electronic device at the VB, HB, TB and BB. It is worth noting that the singular device and capacitor can comprise multiple homogeneous components connected in parallel or series depending on the rating. In this paper, the singular device in this paper means one component only.

Assuming *N* sections, the design rules can be summarised as:
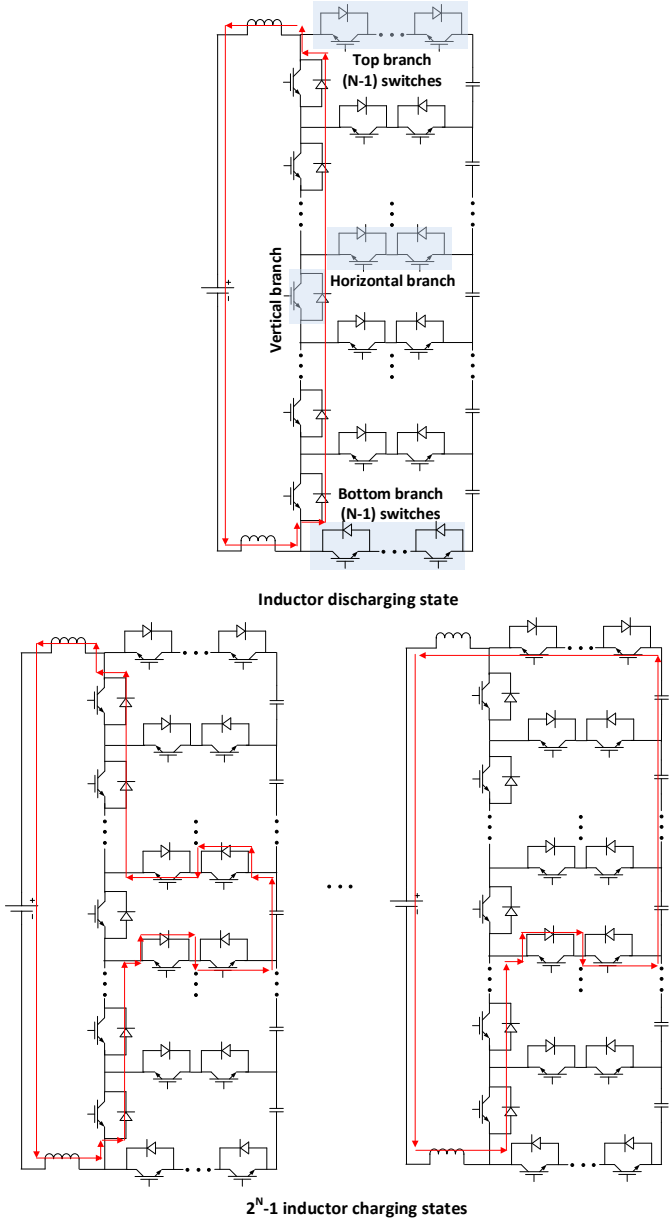1) *N* capacitors and the net voltage at the high voltage end is the sum of all sectional capacitor voltages.

2) Each VB has one device (active device with freewheeling diode) and *N* vertical devices are used to form *N* VBs
3) *(N-1)* MBs are used and each MB has two devices, total *(2N-2)* devices are required for all MBs
4) The TB and BB require *(N-1)* devices each, total *(2N-2)* devices are required for TB and BB.
5) Total *(5N-4)* devices are required for *N* sections and all devices can be identical.
6) The nominal voltage of any individual device should be as same as the voltage of the sectional capacitor.

Figure 2 Inductor charging and discharging states (step-down)

2.2 Vertical switching interleaving technique

The operation principle of the MLDC is based on the vertical switching interleaving in which the charging state is embedded between any two discharging states. Due to the special structure of the topology, a number of different

discharging/charging states exist and they can be interleaved in a sequence in one cycle to increase the equivalent switching frequency, giving inductor ripple current in a reduced amplitude without increasing the actual switching frequency of the device.

As shown in Fig 1, at the voltage step-up mode, the inductor is charged when all VBs are switched on and all TBs and BBs are switched off. There is only one charging state, in step-up mode but a large number of discharging states exist. The number of the sections in one discharging state is determined by the minimum output voltage at the high voltage side. For example, if one section is engaged at each discharging state, the minimum output voltage is N times of the input voltage. In general, if the minimum output voltage is (N/k) times of the input voltage, the number of discharging states, n_{dk}, equals to the binomial coefficient:

$$n_{dk} = \binom{N}{k}, 1 \leq k \leq N \qquad (1)$$

The charging state can be denoted as $\binom{N}{0}$, hence the total number of charging and discharging states, n, is:

$$n = \sum_{0 \leq k \leq N} \binom{N}{k} = 2^N \qquad (2)$$

The number of total discharging states, n_d, is:

$$n_d = 2^N - 1 \qquad (3)$$

If the charging state is denoted as C, and discharging state is denoted as $D(i)$ where i indicates one of discharging state when k sections are used, one interleaved cycle can be expressed as: *C, D(1), C, D(2), ..., C, D(n_{dk}),C, D(1), C,...*

Here, we define the natural interleaving sequence (NIS) in which every cycle has the same discharging state, the total number of NIS, R, when k sections are used, follows permutation rule:

$$R = n_{dk}! \qquad (4)$$

Taking any R number of NIS and allowing repetition, the total interleaving sequence, S, is:

$$S = R^R \qquad (5)$$

It is obvious that a large number of interleaving sequences can be used in this MLDC converter. Each interleaving sequence gives n_{dk} ripples of the inductor current if k sections are used. A smart selection of sequence can improve voltage balancing of the sectional capacitor, which will be investigated in future.

A similar analysis can be applied to the step-down operation as shown in Fig 2. The conclusions of interleaving sequence are same to the step-up operation.

2.3 Voltage transfer ratio expression

The voltage transfer ratio is determined by both the duty ratio, ρ , between each charging and discharging process and the number of sections used in operation, k. For the step-up operation, the output voltage is expressed as:

$$V_{out} = \frac{N}{(1-\rho)k}V_{in}, \qquad 1 \leq k \leq N, \qquad (6)$$

For the step-down operation, the output voltage becomes:

$$V_{out} = \frac{N}{k}\rho V_{in}, \qquad 1 \leq k \leq N, \qquad (7)$$

The use of vertical interleaving in MLDC can reduce the individual device voltage stress and the amplitude of the inductor ripple current, offering a reduced number of devices and the size of the inductor for the high voltage transfer ratio DC/DC conversion compared with conventional Boost and Buck converters.

For example, if using 1.7 kV IGBTs and the rated sectional capacitor voltage is set to be 1.1 kV. In order to have N times 1.1 kV at the high side voltage with N interleaved inductor current ripples, conventional Boost/Buck converter needs $2N^2$ IGBTs but only *(5N-4)* devices required for MLDC because the series connected IGBTs in MLDC are switched in the fashion of vertical interleaving. The conventional topologies have to synchronise switching of series connected IGBTs due to limitation from the topology as shown in Fig 3
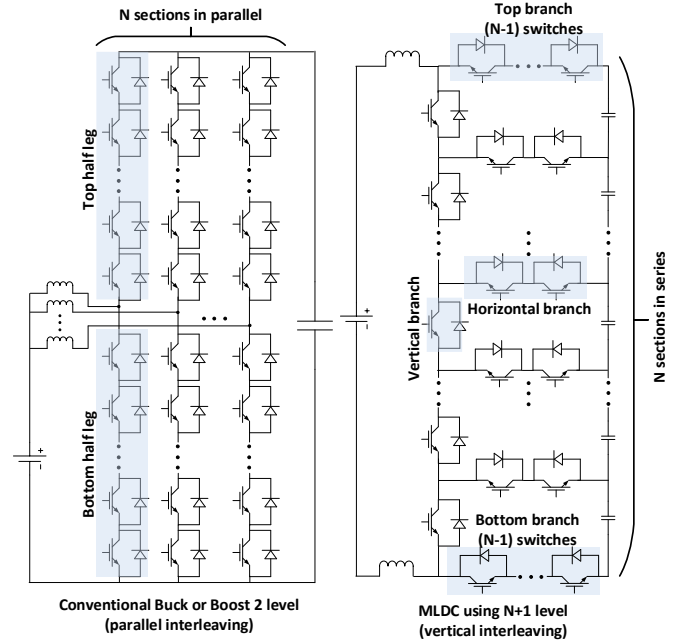

Figure 3 Comparison with conventional Boost/Buck topology

Examples of devices reduction at different high-end side voltages are shown in Table 1.

Interleaved ripples	Voltage	MLDC (5N-4) IGBTs	Buck/ Boost (2N²) IGBTs
3	3.3 kV	11	18
4	4.4 kV	16	32
5	5.5 kV	21	50

Table 1 Comparison of number of active devices

2.4 Four-level topology

A 4L-MLDC where 3 capacitor sections (*N=3*) MLDC converter is used to validate the derivation of the topology and the vertical interleaving. The number of devices at the TB and BB equals (*N-1*) so two identical IGBTs with their freewheeling diodes are connected in series at the TB (St1, St2)

and BB (Sb1, Sb2) as shown in Fig 4. Three VBs (Sv1, Sv2, Sv3) and two MBs (Sh1+ Sh- and Sh2+ and Sh-) are also required to form this 4-L MLDC converter. Three sectional capacitors (C1, C2, C3) are identical and expected to share the same fraction of the net DC voltage at the high voltage side.
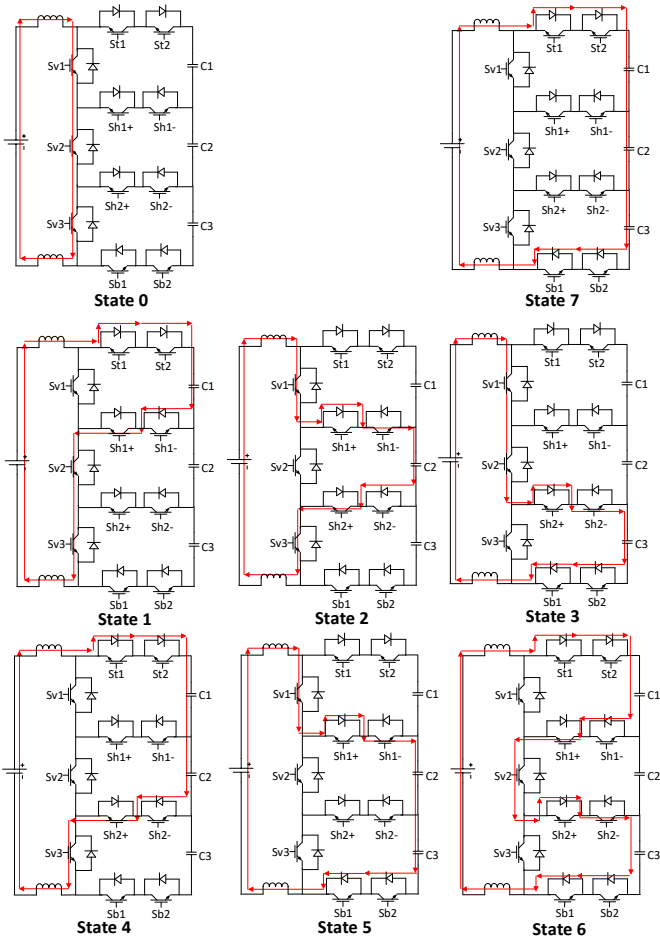

Figure 4 charging and discharging states of 4-level MLDC at step-up operation

From (3), there are seven discharging states and one charging state as shown in Fig 4., when operating at the voltage step-up mode. State 0 is the charging state. State 1, 2 and 3 are discharging states and the minimum output voltage is $3V_{in}$; State 4, 5 and 7 are discharging states when two sectional capacitors ($k=2$) are used and the minimum output voltage is $(3/2)V_{in}$; State 7 is the discharging state when three sectional capacitors ($k=3$) are used and the minimum output voltage is V_{in}. The number of discharging states follows the expression (2) and the voltage transfer ratio follows the expression (6). When one sectional capacitor ($k=1$) is used, the number of NIS when one sectional capacitor is used is 6 and the number of all interleaving sequences is 46656. Details of interleaving sequences are shown in Fig 5.

The same principle can be applied to the voltage step-down mode with power flow from the high voltage side to the low voltage side.
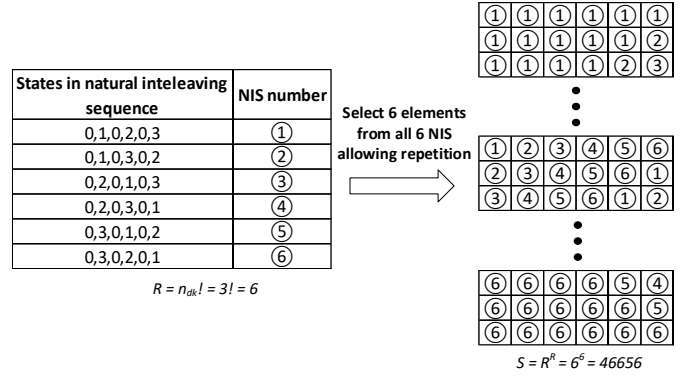

Figure 5 Interleaving sequences for 4-L MLDC using one sectional capacitor

3 Prototype and results
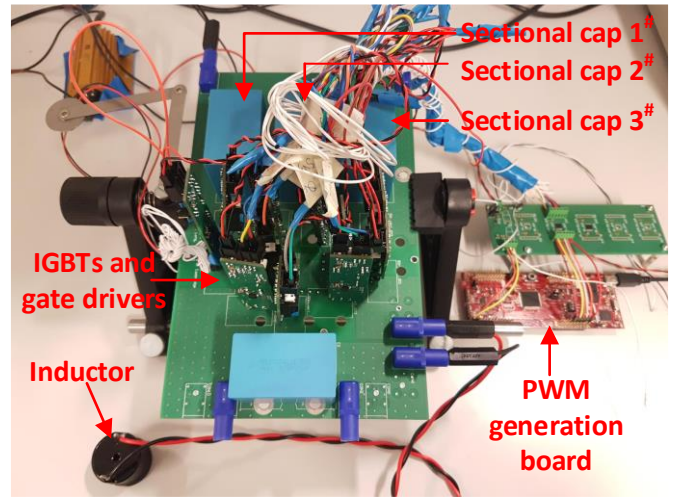
3.1 Hardware

Figure 6 the 4-L MLDC prototype

A 4-L prototype is made to validate the concept and operation principle of this MLDC as shown in Fig 6.. The schematic of the circuit and the denotation of devices are shown in Fig 4. Discrete 1.2 kV IGBTs with freewheel diodes in the TO-247 package are used. The DC inductor is 330 µH. The PWM is generated by a DSP based control board.
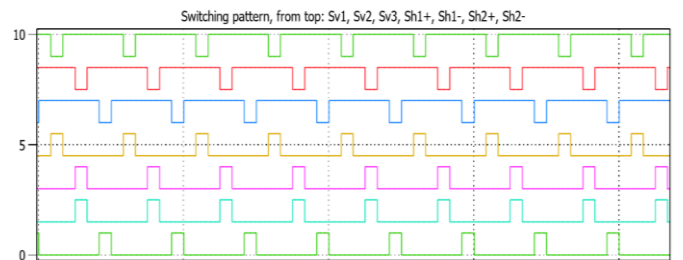
3.2 PWM

Figure 7 PWM of switches in 4-L PWM for step-up operation; from top to bottom are Sv1, Sv2, Sv3, Sh1+, Sh1-, Sh2+ and Sh2-. Duty ratio is 50%.

In this paper, one sectional capacitor ($k=1$) was selected for both the simulation and experiment thus the minimum output voltage should be 3 times of the input voltage. The NIS, 0, 1, 0, 2, 0, 3, 0, 1,…was selected and the duty ratio was set at 50% The switching frequency was set at 10 kHz. The PWM patterns of the MLDC operated at the voltage step-up mode is shown in Fig 7. It is worth noting that devices at the TB and BB are permanently switched off when voltage step-up operation.

3.3 Simulation results

A PLECS based simulation was developed. The MLDC operation was modelled with an open-loop control. The control design of the MLDC is beyond of this paper. The input voltage was 50 V so the sectional capacitor voltage was expected to be 100 V with a 50% duty ratio. Therefore all of the devices should have a maximum voltage (Vce) of 100 V, which has been proved as shown in Fig 8. Two series connected devices at the TB and BB shared the branch voltage equally.

The ripple current at the inductor was expected to be three, which was proved by the simulation as shown in Fig 9 where three ripples with a peak-peak value of 2 A in every 100 μs (10 kHz switching frequency) were counted. The load was a 1 kΩ resistor so the input average current was expected to be 1.8 A which has been proved as shown in Fig 9 too.

Due to the lack of closed-loop control, the voltage across each sectional capacitor was not identical. As shown in Fig 9, the simulation results show 91 V, 100 V, and 103 V so there was approximate 10% miss-sharing. The net voltage was 304 V. The miss-sharing can be addressed once the closed-loop control has been implemented, which will be reported in other articles in future.
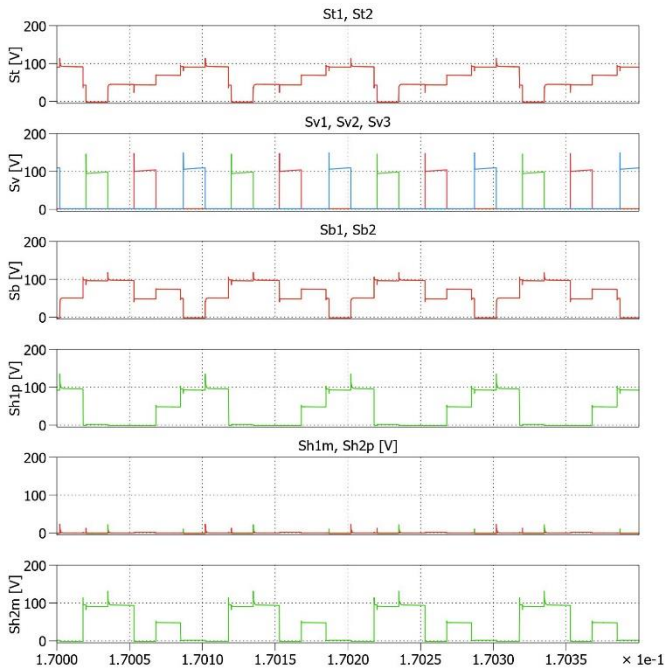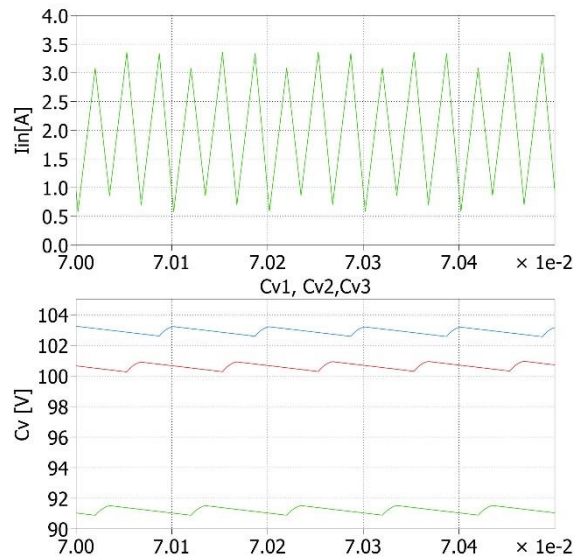

Figure 9 Simulation results of inductor current and voltage at each sectional capacitor

3.4 Experimental results

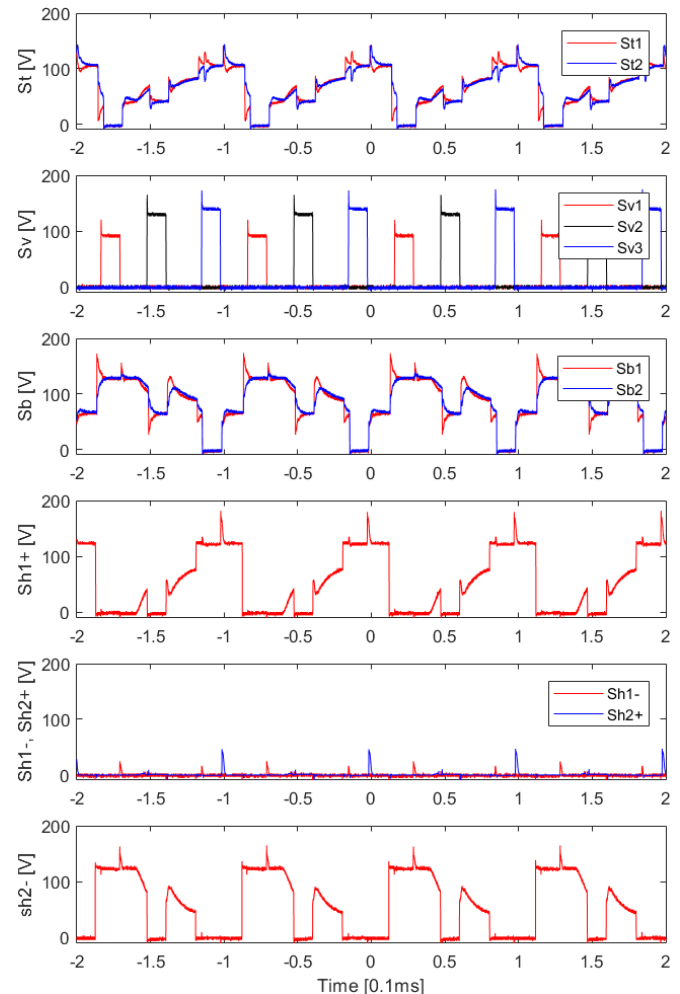

Figure 8 Simulation results of the Vce of all IGBTs
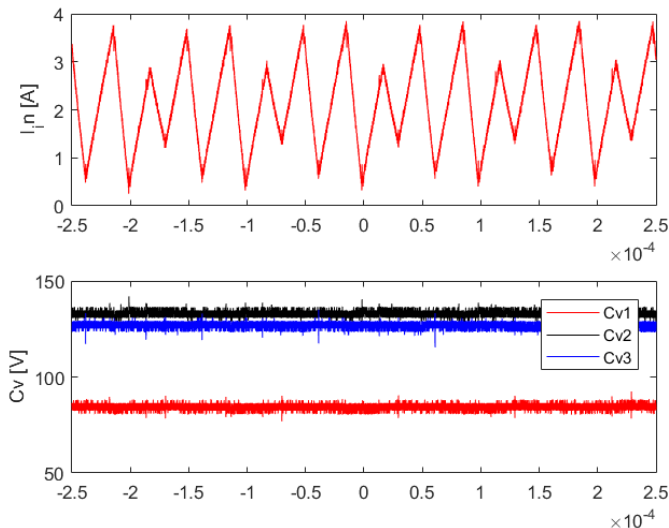
Figure 10 Experimental results of the Vce of all IGBTs

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Figure 11 Experimental results of inductor current and voltage at each sectional capacitor

Same input voltage (50 V) and load (1 kΩ) were applied to the prototype and the duty ratio was set at 50%. In order to avoid overvoltage, i.e. larger than nominal section voltage, on the devices caused by switching delays from the devices, an extra 2 μs has been added to each ON time to create an overlapped ON pulse between certain pairs of devices thus the actual, which results in an extra 13% sectional voltage as 113 V. The additional voltage is determined by the switching frequency and can also be eliminated if the closed-loop control is implemented. Details of this overvoltage protection measure will be introduced in other articles in future.

All device voltage of IGBTs were measured by using differential probes as shown in Fig 10. The devices at the TB had approximately 105 V each and shared the voltage equally. The devices at VBs had a voltage of 90 V, 115V and 134V, indicating some miss-sharing of the sectional voltage due to the lack of closed-loop control. The devices at the MBs and the BB had 125 V. In general, all devices were close to 113 V and the discrepancy was caused by the miss-sharing of the sectional voltage which can be solved once the closed-loop control has been implemented. Voltage spikes have also be captured which was caused by the stray inductance of the PCB and can be mitigated by optimising the circuit layout.

The input current of the experiment showed expected 3 ripples per 100 μs and the mean value was 2.3 A which agreed with a 1 kΩ load with a net voltage of 339 V at the output. The sectional voltage of the capacitor was same to the corresponding VB voltage at 90 V, 115V and 134V respectively. Again, this imbalance was due to the lack of the closed-loop control.

The experimental results agreed with the simulation results within an acceptable discrepancy and both results have demonstrated the concept and operation of the MLDC.

4 Conclusions and future work

A novel non-isolated Multi-level DC/DC (MLDC) converter using vertical interleaving technique is reported in this paper. This MLDC offers a wide range of voltage transfer ratio by using a reduced number of low voltage power electronic devices and reduced size of the DC inductor, making this converter a potential candidate for high power DC power converters such as energy storage connection to Medium Voltage (MV) systems or drives. The derivation of the generic topology has been given. Design considerations and all possible arrangement of the vertical interleaving used in this MLDC has been introduced with mathematical expressions.

A 4 level (4-L) example of this MLDC has been built. The operation of voltage step-up has been validated with both simulation and experimental results with an open-loop controller.

This paper has possibly introduced a new research area of this novel MLDC topology and only the derivation of the topology and operation principle have been given. The novelty and complexity of this MLDC require intense investigation in future including topology mathematical modelling and stability analysis, interleaving sequence selection, control design, protection, reliability, etc..

5 Acknowledgements

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