NELSON MANDELA UNIVERSITY

MITIGATION OF SINGLE EVENT UPSETS IN A XILINX ARTIX-7 FIELD PROGRAMMABLE GATE ARRAY

BY

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Declaration

I, JOSHUA OMOLO, student number 209080203, in accordance with rule G4.6.3, hereby declare that this research project dissertation for Master of Engineering in Mechatronics is my own work and that it has not previously been submitted for assessment to another university or for another qualification.

SIGNATURE: 

DATE: 6 November 2018

Dedication

I dedicate this dissertation and the work involved to my late father, Mr Dawson Oburu.

Acknowledgements

Foremost, I give all the glory to God, the author of my life. Without His favour, I would not have the strength, wisdom, knowledge and understanding to accomplish this work.

I would like to thank my mother, Grace and sisters: Tina, Irene, Connie and Eva for all the support and sacrifices made behind the scenes.

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Lastly, thank you Ms Funeka Mbatha for being by my side and always encouraging me to tirelessly pursue this dream.

Abstract

Field programmable gate arrays are increasingly being used in harsh environments like space where high energy particles from radiation affect the integrity of the data. Before deployment of satellites in space, characterisation and consequently mitigation of radiation effects is necessary to avoid failure.

By irradiating a digital microelectronic device, using accelerated energetic particles, it is possible to predict the likelihood of an event effect happening. Such irradiation tests can only be done at a particle accelerator facility such as iThemba LABS in Cape Town. It is the one of the few particle accelerators in the southern hemisphere and offers the capacity to perform these event effect characterisation tests.

Triple Modular Redundancy (TMR) is a commonly used mitigation technique in microelectronics. Although effective, it has the downside of increased resource area. A DMR-Filter combination mitigation technique was developed at the Nelson Mandela University. It uses fewer resources than TMR and it is envisaged to significantly reduce event upsets in a FPGA.

This research project seeks to investigate the effectiveness of the DMR-Filter combination mitigation technique in reducing the likelihood of event upsets occurring in Xilinx's Artix-7 FPGA when exposed to highly accelerated particles, similar to those in space.

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List of abbreviations used

FPGA	Field Programmable Gate Array
ASIC	Application Specific Integrated Circuit
VHSIC	Very High Speed Integrated Circuit
VHDL	VHSIC Hardware Description Language
HDL	Hardware Description Language
PAL	Programmable Array Logic
CPLD	Complex Programmable Logic Device
SEEs	Single Event Effects
SEB	Single Event Burn-out
SEGR	Single Event Gate Rapture
SET	Single Event Transient
SEU	Single Event Upset
SEL	Single Event Latch-up
DUT	Device under Test
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
TMR	Triple Modular Redundancy
DMR	Double Modular Redundancy
LET	Linear Energy Transfer
TID	Total Ionization Dose
TTL	Transistor-Transistor Logic
PMOD	Peripheral Module
MOSFET	Metal Oxide Semi-Conductor Field Effect Transistor
EPD	Electronic Personal Dosimeter
MeV	Mega electron Volt

GeV	Giga electron Volt
SRIM	Stopping and Range of Ions in Materials
TRIM	Transport of Ions in Matter
LUT	Lookup Table
BUFG	Global Buffers
IO	Input/output
FF	Flip Flops
DPR	Dynamic Partial Reconfiguration

1. CHAPTER 1

1.1. Background to the research problem

Space technology has overcome numerous problems in the attempt to improve the overall efficiency of memory-based digital devices aboard satellites; one such problem is the mitigation of the negative effects of radiation [1]. Such radiation increases the risk of failure and thus high costs are involved when designing and consequently deploying digital circuitry in space [1].

The field programmable gate array (FPGA) is one advanced programmable logic device which has been used in space technology over the years [2]. For low volume production and prototyping applications, it compares better to Application-Specific Integrated Circuits (ASIC) in terms of design cycle time, re-programmability, cost and overall performance. Despite these inherent advantages, deployment of the FPGA in the space environment is still a challenge due to the existence of radiation originating from solar wind, particles trapped in the Van Allen belts and cosmic rays [1]. Such radiation can lead to incorrect voltage levels, broadly known as single event effects (SEEs), in the logic circuitry of digital devices deployed in space [1].

SEEs are caused by ionization when a highly charged particle, such as a neutron, proton or heavy ion strikes a circuit element leading to incorrect logic values [3]. Such effects can either be permanent or temporary, more commonly referred to as hard or soft errors respectively. The permanent effects include: Single event burn-out (SEB), single event gate rapture (SEGR) and single event latch-up (SEL) while some of the temporary effects include: single event upsets (SEU) and single event transient (SET) [3].

This unpredictable nature of the space environment thus calls for a lot of thought and consideration to be taken before deployment of digital devices in space. One such consideration is the need for effective techniques to mitigate the SEEs [1]. Radiation hardening of the raw materials used in manufacture of digital devices is sometimes carried out for certain missions. However, it is very expensive and not commercially viable; especially for research and deployment of smaller missions like Cube Sat. In this regard, less costly redundant and filter mitigation techniques have been developed by researchers in the field with great success [4].

This research aims to investigate the effectiveness of a mitigation technique in correcting errors that affect digital logic applications of the FPGA when exposed to highly accelerated particles, similar to those in space.

1.2. Research question

How effective are the SEU mitigation techniques developed at the Nelson Mandela University in reducing the errors which occur in the user logic of an SRAM based FPGA that is exposed to highly energised ionising radiation?

1.3. Research statement

SEU mitigation techniques have varying effectiveness in reducing the errors which occur within the user logic of SRAM based FPGAs exposed to highly energised ionising radiation, similar to the space environment.

1.4. Hypothesis

It is envisaged that by applying the DMR-filter combination to a hardware circuit design implemented on Xilinx's Artix-7 FPGA, the probability of single event upsets caused by highly energised ionising radiation, similar to that in the space environment shall be reduced.

1.5. Aims and objectives of this research project

1.5.1. Aim

This research project aims to validate a procedure for mitigation of single event upsets which was developed at the Nelson Mandela University.

1.5.2. Objectives

i. To investigate the impact of highly energised ionising radiation, on a digital circuit application implemented on an SRAM based FPGA device.
ii. To compare the effectiveness of a single event upset mitigation technique developed at the Nelson Mandela University to known mitigation techniques.
iii. To become proficient in hardware description language, most notably VHDL for the modelling of digital circuits.

1.6. Significance of this research project

Radiation hardened digital devices refer those whose structure has been altered to ensure that their functionality withstands the effect of highly energised particles by modifying their material composition of the material during manufacture [5]. An alternative to radiation hardening in memory-based digital devices is achieved using mitigation techniques which modify the application designs using software [5].

There are a number of mitigation techniques against single event upsets in SRAM based digital devices which were developed at the Nelson Mandela University. This project shall validate the effectiveness of the DMR-filter combination mitigation technique when applied in a commercial Field Programmable Gate Array (FPGA) which is exposed to high energy ionising radiation. This validation is significant in that, it shall support the argument for reduced reliance on radiation hardened semiconductor materials in memory-based digital devices which are bound to be used in the space environment.

1.7. Limitations/Scope

The space environment consists of various forms of radiation at different energies. However, at iThemba LABS testing facility, only a single energy level was available and therefore all testing was carried out at maximum proton beam energy of 66 MeV.

The mitigation techniques tested were used to reduce the single event upsets and not other effects caused by highly energised radiation.

1.8. Assumptions

The highly energetic accelerated particles used for irradiation collided with the device under test at a perpendicular angle. Furthermore, it was also assumed that a considerable amount of these particles cause ionization on collision with the microelectronic chip used.

1.9. Definitions of key terminologies used

Cube Sat – These are relatively small satellites manufactured in multiples of approximately 10x10x10cm in volume and weigh less than 1.33kgs. They are most often launched by universities and private companies as part of a larger payload for research, earth observation and communication among other applications.

Linear Energy Transfer (LET) – refers to the energy deposition per unit length. It is commonly represented in kiloelectron volts per micrometer (keV/μm) or megaelectron volts per centimetre (MeV/cm), and describes the mean energy lost by an ion per unit length of the material through which a radiation beam penetrates.

Cross Section Area, σ - is defined as the ratio of the number of errors counted to the area over which they occurred on the surface of the semiconductor material

Van Allen belt – is a region of high radiation that extends on two sides of the earth asymmetrically and have nulls at the poles. It is known to trap charged particles from solar wind.

South Atlantic Anomaly (SAA) – is a region of high flux for energetic particles in the inner Van Allen belt where it reaches closest to the earth's surface and exposes satellites to very high radiation levels.

Particle flux- refers to the number of particles penetrating an area per second. It is often calculated for an area of $1cm^2$ for a period of 1 second.

Fluence – is the ratio of the particles penetrating an area and is obtained as the integral of flux over a period of time.

Dosimetry – refers to the assessment and measurement of the quantity of ionising radiation which penetrates a device or body.

Ionising radiation – refers to any form of electromagnetic wave or particle with sufficient energy to cause the removal of electrons from an atom's structure.

1.10. Brief chapter overview

Chapter 1 gives background information of this research. Here, the research problem is introduced and the hypothesis stated. Furthermore, it introduces the aims and objectives of the project and also the significance of embarking on this study. The chapter concludes by defining the: research project's scope, assumptions made and key terminologies used.

Chapter 2 introduces the literature reviewed from various sources that are significant to this research project. It introduces the: field programmable gate array, ionising radiation environment and the effects caused in such environment on digital devices. The chapter presents literature about known SEE testing methods and facilities available, specifically iThemba Labs. It then concludes with SEE mitigation techniques used by other researchers thus far.

Chapter 3 introduces the approach used to achieve the aims and objectives of this research through the design and methodology.

Chapter 4 presents the results obtained from the methodology used in testing and mitigating the single event effects in the FPGA.

Chapter 5 presents conclusions that were drawn from this research and offers recommendations that could be made to improve the methodology and system that was used in this study.

2. CHAPTER 2

Literature review

This chapter describes: an overview of digital logic design, the field programmable gate array (FPGA), particle radiation in space and its effect on digital devices, single event effect (SEE) testing and mitigation techniques.

2.1. Overview of digital logic design

Whether digital designs are part of the data path or the control area of a circuit, they can all be broadly characterised as either combinational or sequential in nature. Combinational circuits are defined as those whose output value depends only on the circuit's present inputs [6]. Memory is not involved here and a common example is an adder, which uses two or more inputs that sum these values and eventually gives an output value. In digital logic devices, combinational circuits include: Arithmetic Logic Unit (ALU), comparators, next state logic circuits, tri-state buffers and many others [6].

Sequential circuits are defined as those whose output depends on both the circuit's present input value and also the previous input values [6]. They must involve memory and it's because of this that, they must "recall" their previous values. A common example of a sequential circuit is a television remote control's volume or channel +/- digital circuit. If a user presses the +/- buttons on this circuit, the new value depends on the previous one and not only on adding or subtracting. Sequential circuits in digital logic devices include: data path registers, flip flops and all other registers which control the controller's state memory [6].

Both combinational and sequential circuits consist of the main logic gates: AND, OR and NOT which are made using transistors. The transistors inside a circuit switching ON and OFF are indicative of logic levels 1 and 0 which are commonly used in digital logic design to develop large and powerful circuits [6].

2.2. The Field Programmable Gate Array (FPGA)

The FPGA's origin can be traced from digital logic circuits which implemented Boolean logic from gates such as the AND, OR, NOT, NOR, flip flops and so on which were commonly used in transistor-transistor logic (TTL). From this came the programmable array logic (PAL) devices which evolved into complex programmable logic devices (CPLD) and then eventually the FPGA [7].

FPGAs are a family of semiconductor logic devices made up of a matrix of logic blocks and programmable switches which are reprogrammed to a desired application or functionality after manufacture [7]. The ability to have designs reconfigurable after manufacture distinguishes the FPGA from Application Specific Integrated Circuits (ASICs) and has thus made them popular for use in: automotive, aerospace, military, broadcasting industries among others for various applications [8].

In the past, the user was able to specify a desired circuit by using either schematic entry or hardware description language (HDL) like Verilog or VHDL. More recent advances in digital logic technology have allowed users to also program newer generation FPGAs in higher level languages like C, SystemC, Python and OpenCL among others [7]. Schematic entry is still suitable for simple designs while HDL and the higher level languages have more unlimited ability. Regardless of the designer's choice of logic description, all designs must be entered into the logic elements of the FPGA by a process called synthesis before they are simulated and eventually run [7].

FPGAs can be broadly categorized based on their form of memory into: SRAM and flash based types. They can also be characterised based on their level of re-programmability as either one-time programmable fuse or anti-fuse technologies. SRAM FPGAs though faster and denser, are more expensive and susceptible to bit flips caused by radiation compared to their flash based counterparts. Studies have previously been carried out at the Nelson Mandela University on flash based FPGAs, but this study is focused on a SRAM device. Major manufacturers of FPGAs today are: Altera, Xilinx and Lattice Semiconductor for SRAM based FPGAs, while Micro-Semi produces most of the flash based type [9].

2.2.1. Architecture of the FPGA

The generic architecture of an FPGA device consisting of a two dimensional matrix of configurable logic blocks is shown below in figure 1 [10]

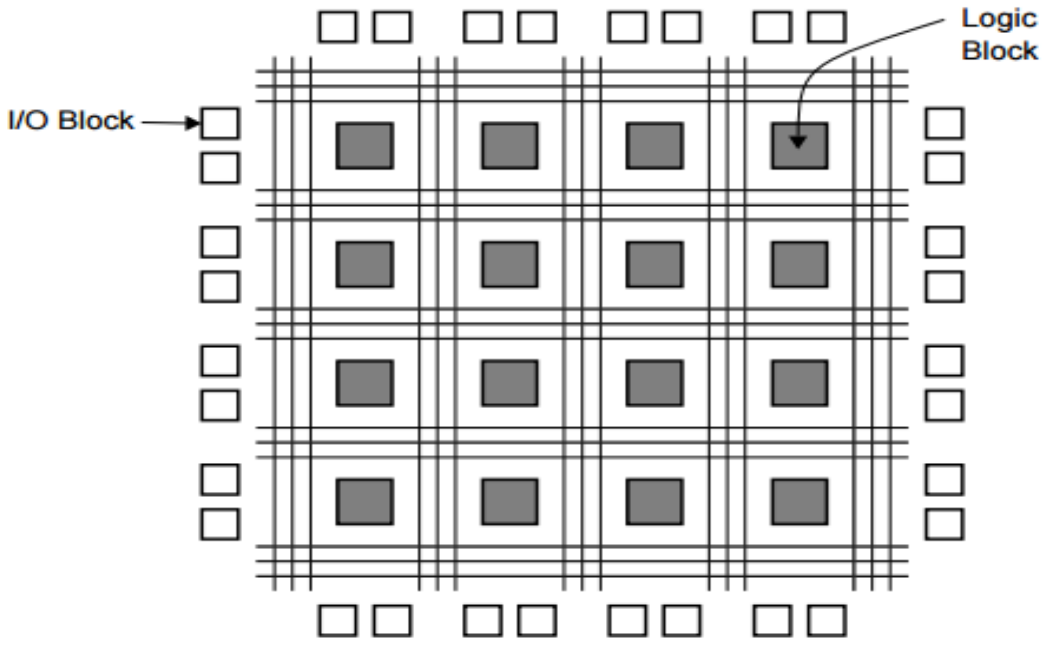

Figure 1 - Generic architecture of the FPGA [10]

The FPGA's general structure is divided into different sections namely: the configuration structure, which consists of interconnects between its logic blocks that's responsible for identification of a particular cell, the functional structure, which consists of the user's combinational and sequential logic, input and output blocks and finally the global routes structure, which consists of the reset, clocks and fan out nets [10].

At the array level, the FPGA is made up of an embedded array and a logic array. The embedded array includes peripherals like the digital signal processor (DSP) and the microcontroller, which are used to carry out more complex operations and also its memory functions [10]. The logic array on the other hand consists of combinational components like multiplexers, arithmetic logic units (ALU), comparators, counters and so on which are used to carry out more basic operations [10].

2.2.2. Memory in the FPGA

Memory is described as a circuit which can store a bit data. One such simple circuit is the D-latch shown in figure 2, capable of storing a bit or if arranged as an array, can store more bytes of data.

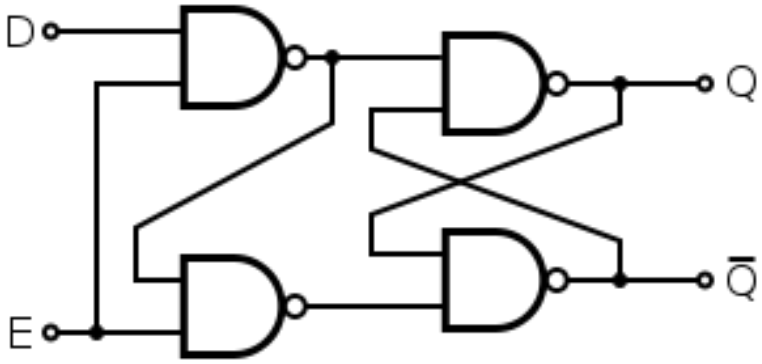

Figure 2 - D type latch

Classification of memory could be by the way it is accessed - sequential or random, or more commonly as either read-only or read/write [6]. Digital electronics and computer science lingo generally classifies memory as either Read Only (ROM) or Random Access (RAM) with the latter further divided as either static or dynamic.

Static RAM (SRAM) is fast and utilises an array of transistors to store data and control its read/write operations. It is volatile, more expensive and thus more practically used in cache memory. Dynamic RAM (DRAM) on the other hand implements capacitors to store memory bits which discharge over time and thus need periodic refreshing. Although slower than SRAM, it is cheaper and has the advantage of larger density. It is mostly used in the main memory and like SRAM is volatile. Another commonly used type of memory is the flash, which is a type of reprogrammable ROM that is highly popular due to its non-volatility and large capacity [6].

FPGAs are classified depending on the type of memory sequence they implement, hence nomenclature like SRAM based FPGAs and flash based FPGAs among others. Figure: 3 shows a basic SRAM array [11]

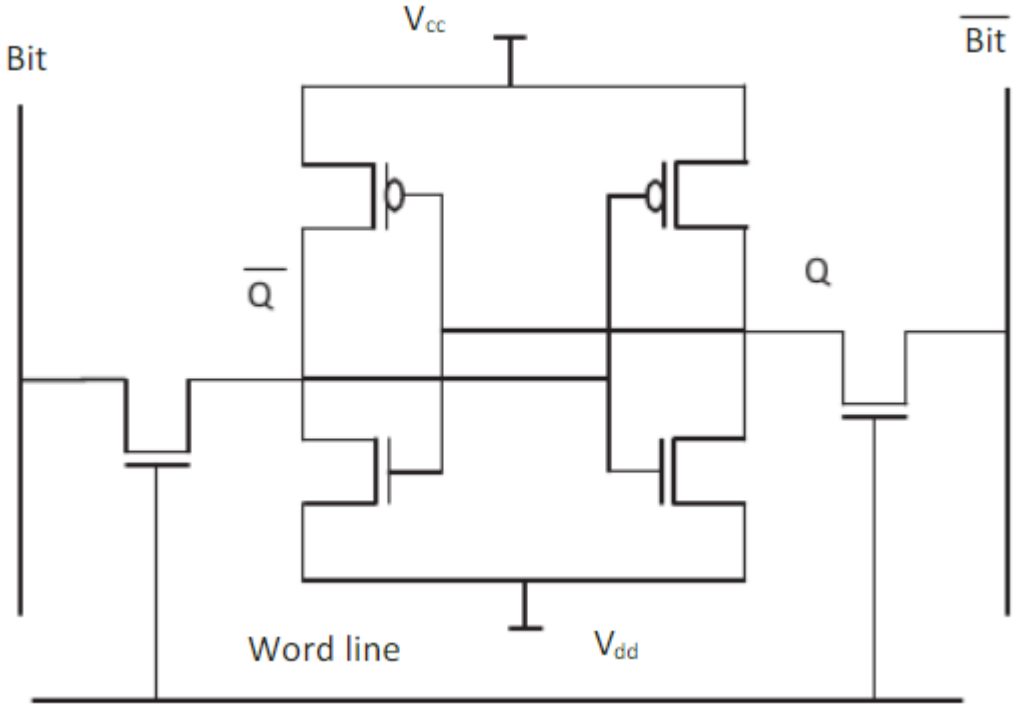

Figure 3 - A basic SRAM array [12].

The SRAM cells could be made using transistors (both Bipolar Junction and MOSFET type) or simply by implementing flip flops as mentioned earlier. Figure 3 above shows a RAM cell which is capable of storing a bit. It could be arranged in a particular pattern say, as a 512 x 8192 row-column rectangle array [6]. When a particular address is applied to the address lines, the row and column decoders select the corresponding SRAM cell in the memory array for a read or write operation. The column output must then be amplified before it is passed to the read buffer [11]. The columns could also be further subdivided into groups of eight to enable one column address to select a byte for a read or write operation [6].

2.3. Radiation in the Space Environment

The earth's environment contains natural radiation, whose particle flux mainly depends on altitude and latitude. Flux has been seen to also depend on longitude, although to a lesser extent [13]. These radiation particles have a wide energy spectrum and are able to deposit energy in semiconductor material as a result of various interaction mechanisms. [13]One such mechanism is radioactivity in some impurities that exist in the material used to manufacture semiconductor devices. This radioactivity leads to emission of particles which can cause disturbances [13].

The study of SEE characterisation requires correct quantification of particle interaction mechanisms. Also, the recoils that are produced as a result of high energy spallation reactions need to be correctly understood [13]. This energy loss per unit length of the material penetrated is an important parameter that is used in characterisation of SEEs and will be introduced in later literature.

This subsection introduces the space environment with a focus on the satellite path (orbits) and potential sources of radiation that cause effects in semiconductor devices deployed in space.

2.3.1. Orbits

Another problem with elliptical orbits is exposure to radiation – satellites here cross the high radiation van Allen belts twice during orbit and at a lower altitude, they are exposed to low energy plasma [14].

2.3.2. Radiation sources in space and the earth's atmosphere

FPGAs are commonly deployed in radiation exposed environments [2]. Radiation is classified as either non-ionising or ionising, with the latter qualifying generally by possessing energy greater than 10eV, which is sufficient to form ions [2]. Ionization is defined as the formation of ions due to the interaction of coulombs and electrons found in the semiconductor material, such as Silicon [13].

In Silicon, 3.6eV is the average amount of energy required to form a free electron-hole pair [13]. Non ionising radiation like radio, ultra-violet or micro waves have little or no effect on the functionality of microelectronics [15] and are thus not the focus of this study. Radiation on land is generated and used in hospitals, airports and military through radioactive decay, nuclear reactors, nuclear weapons, particle accelerators, nuclear fusion and fission among others to produce particles like protons, neutrons, electrons, x and gamma rays [16].

A process like radioactive decay produces radiation with insufficient energy to greatly affect a digital microelectronic device which is deployed nearby [17]. However, particle accelerators, nuclear reactors and processes like nuclear fusion and fission are able to generate sufficient energy to affect the functionality of FPGAs and other digital devices [17].

Radiation in space is ionising and originates from galactic cosmic rays, solar wind and particles trapped in the Van Allen belt. Galactic cosmic rays (GCR) mainly originate from the sun and consist of atomic nuclei and high energy protons [18].They generally have high energy and their collision with microelectronics causes sporadic current pulses through ionization known as single event effects (SEEs) [18].

Secondary particles like photons and hadrons are generated when the highly energetic galactic cosmic rays from the sun collide with oxygen and nitrogen in the earth's atmosphere [13]. The physical size of micro-electronics has been reduced over time due to optimization and a single particle strike is more dangerous due to increased device sensitivity [14].

Neutrons in particular have been of great concern because their flux is not constant with altitude. It varies with altitude in that, the higher one travels across the earth's atmosphere, the more attenuation is seen in both cosmic rays and neutrons [14].

Neutron flux also varies with latitude and to a smaller degree, with longitude, because of the difference in magnetic shielding between the equator, north and south poles [13].The strength of neutron flux in the atmosphere is generally controlled by solar eruptions and the extent of solar activity, hence making the study of their effect even more unpredictable [13].

Solar wind refers to a wave of non-uniform charged particles made of plasma that travel from the sun [18]. Plasma refers to a form of gas which is partly ionised. It consists of a sheath mixture of protons and electrons left as a result of some molecules being partly stripped of electrons [14].They possess lower energy compared to galactic cosmic rays and are thus less likely to cause disruptions in microelectronics.

In space, when there is extreme solar activity, proton flux with very high energy up to hundred MeV and sometimes even the GeV range are generated due to more common solar eruptions [14]. This sort of high energy over time causes an accumulation of electrons and protons over time known as Total Ionising Dose (TID) which also leads to microelectronics failure. It is introduced in section 2.7.

The other sources of space radiation are the particles trapped in the Van Allen radiation belt. [18] This belt is a region which extends on two sides of the earth and possesses energetic charged particles mainly electrons, neutrons and some heavy ions. They were discovered in 1958 by a team lead by an American scientist, James van Allen and are divided into two regions; the inner and outer belt. [19] The inner belt is located at an altitude of approximately 1600-12875km, whereas the outer belt is located at approximately 19000-40000km above the earth's surface. Figure 4 shows the van Allen belts and their relative position to satellites in different orbits [19].

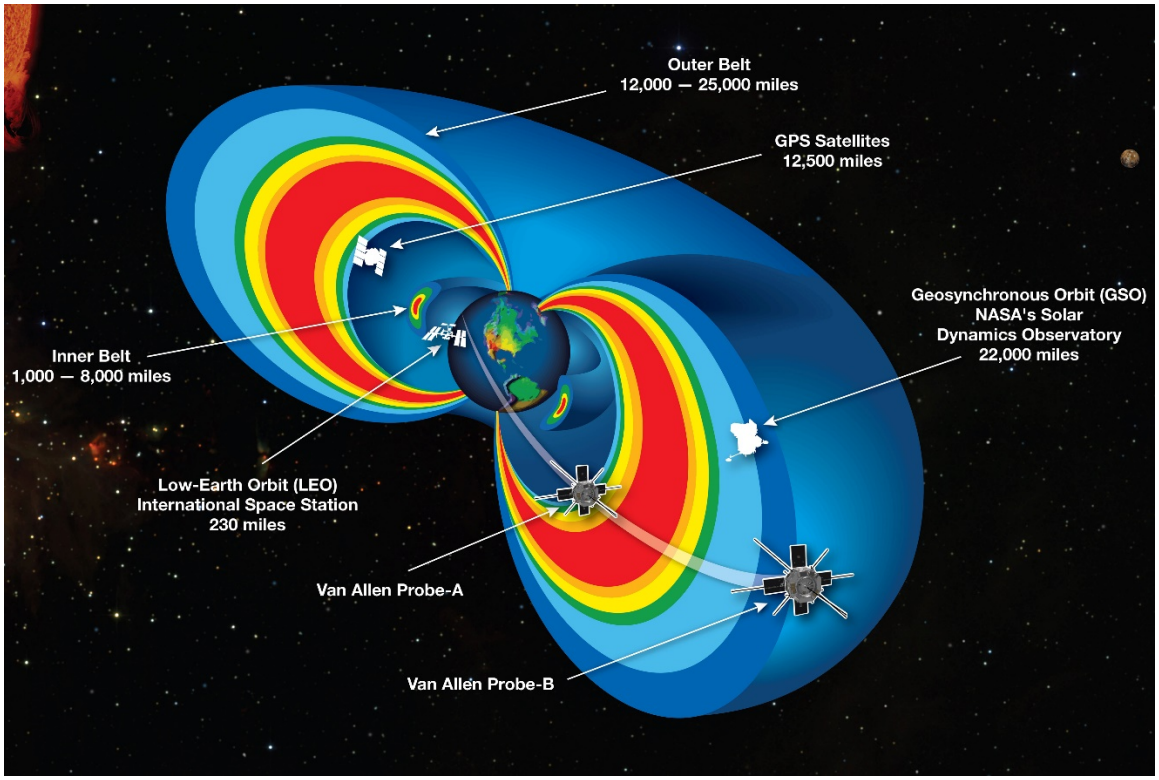

Figure 4 - van Allen belts and their relative position to satellites in orbit [19]

There is a special geographical region called the Southern Atlantic Anomaly [20], where the inner Van Allen belt extends closer to the surface of the earth. The British satellite, UOSAT-3 and avionics in high flying aircraft were observed by the European Space Agency to experience upsets in this region [20]. It is shown in figure 5 below represented by the large concentration of dots.

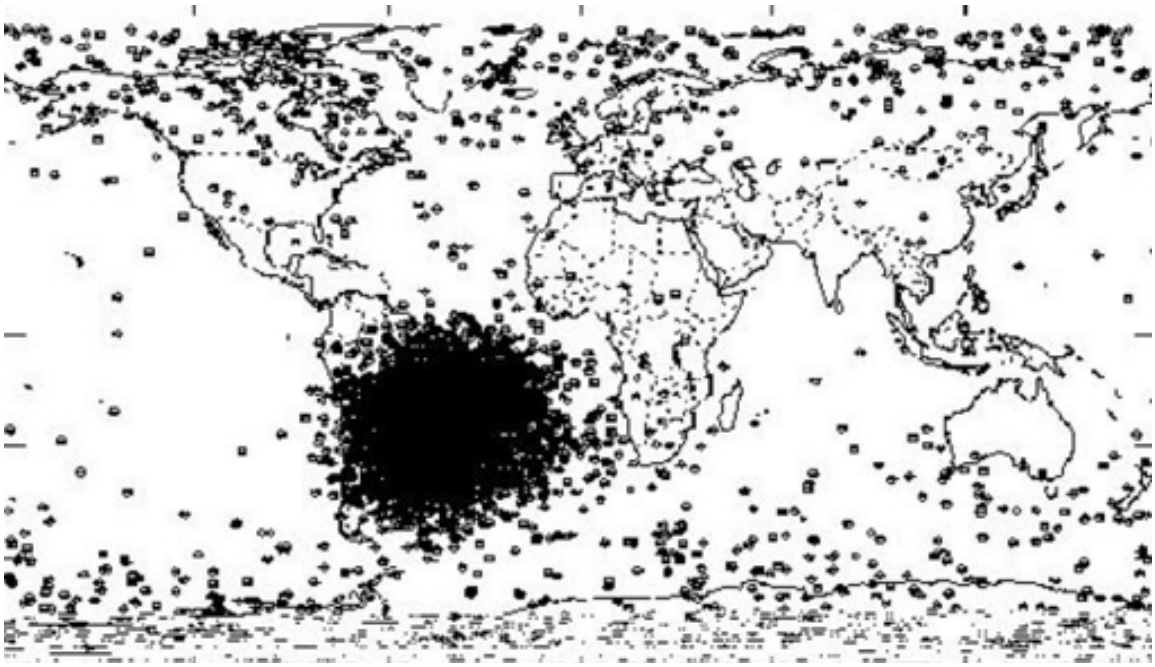

Figure 5 - Southern Atlantic anomaly, represented by the large concentration of dots [20]

2.4. Influence of High Energy Particles on Microelectronics

There are two main effects of high energy radiation in silicon which is the material generally used in the manufacture of most micro-electronics. These effects are: ionization and displacement damage [21]. Both these effects can occur on a device depending on the composition of the high energy radiation [21]. Protons and neutrons are known to have an approximately equal mass of 1amu, which is $1.660539x10^{-27}$kg. They however differ in that neutrons do not possess any charge whereas protons have a positive charge of 1e ($1.602176x10^{-19}$C) and this leads to a difference in behaviour [21]. Neutrons for example have the primary effect of causing displacement damage in Silicon when they first collide with the nucleus and thereafter cause ionization as a secondary effect if they possess sufficient energy [21].

Neutron interaction with matter occurs through collision with other particles due to their relative mass. The displacement caused has been seen to have a major effect on the substrates that make up the structure of semi-conductor devices [21]. There can be secondary ionization effects when they collide with matter and generate more particles like gamma rays or protons [21]. Figure 6 shows the results of an experiment carried out by [15] to ascertain the secondary ionization caused by high energy neutrons.

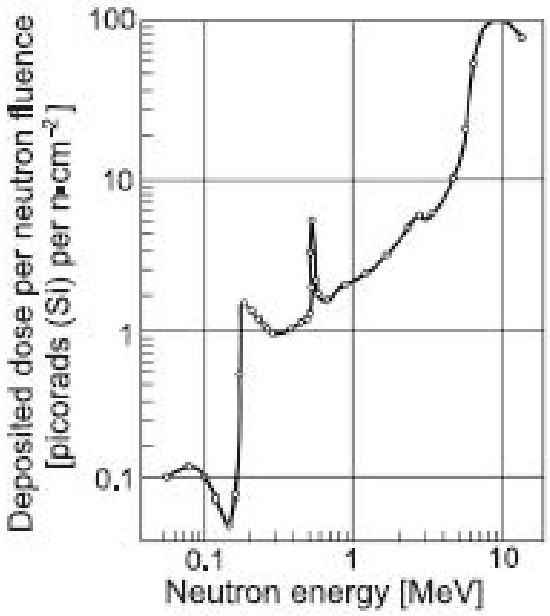

Figure 6 - Deposited dose of high energy neutrons in Silicon [15]

It can be seen from figure 6 above that at low energies, less than 1MeV, neutrons did not possess sufficient ionization energy when they collided with silicon. However, when the energy was increased closer to 10 MeV, there is an exponential rise in the amount of dose deposited, possibly due to the secondary effect of ionization [21] [15].

High energy gamma rays have also been seen to affect the structure of micro-electronics made from silicon dioxide through the accumulation of positive charges at the Si-SiO2 boundary [22]. This sort of build-up of charge causes interaction with matter through an occurrence known as the Compton Effect, whereby electron-hole pairs are generated by free electrons which possess sufficient energy [21].

Regardless of the nature of high energy particles, when ionization occurs due to the collision, they can generally cause disruptions in microelectronics. These disruptions are broadly categorized as single event effects (SEEs) and if this occurs over a period of time leads to total ionization dose (TID) and space craft charging. These three phenomena are introduced in this subsection.

2.5. Single Event Effects (SEEs)

SEEs are errors caused by ionization from the impact of accelerated heavy ions with elements in microelectronics [13]. They manifest in different ways and are broadly classified as either permanent or temporary, based on the level of reversibility in devices. Sometimes, they are classified as soft or hard errors [3].

Temporary Effects

Temporary SEEs are reversible errors which occur when high energy radiation particles cause ionization upon collision with microelectronics. They corrupt data in microelectronic circuits but do not cause permanent damage like the permanent effects introduced earlier. In analogue circuits, these effects occur in operational amplifiers and comparators as transient pulses and are referred to as Analogue Single Event Transients (ASETs) [13].

They manifest as single event upsets (SEUs), single event function interrupts (SEFIs) and single event transients (SETs) and are introduced in this subsection.

2.5.1. Single Event Transient (SET)

A Single Event Transient (SET) refers to a voltage or current disturbance which occurs when accelerated particles deposit charge on circuitry during ionization, leading to incorrect logic readings [13]. SETs are reversible and generally affect combinational logic in devices.

The study of the effect of SETs is often inter-linked to SEUs because when SETs propagate through logic gates into the logic elements like flip flops, they result in SEUs. Some conditions should be fulfilled in order for SETs to cause SEUs and these are:

i. The incident energetic radiation should have sufficient energy in terms of duration and amplitude to produce a transient which can propagate across large areas of the circuit [13].
ii. A path must exist between the incident point of the particle strike and the memory element [13].
iii. If the device is running sequential logic, an SEU can be generated if the particle strike is propagated to the latch at the clock edge [13].

In combinational circuits running at lower frequency, the probability of capturing SETs to give credible data is low, due to a lower number of clock edges happening over time [13]. Therefore, in order to correctly assess the effect of transients, an increase in clock frequency is required to increase the gate speed which decreases the number of logic levels for each pipeline stage in a device [13].

2.5.2. Single Event Upset (SEU)

When ions formed by the collision of energetic particles pass through a sensitive part of a semi-conductor chip, they generate a charge, which if sufficient may cause a bit flip (change in a P-N junction's state) [13]. If this change in state happens during a clock's rising or falling edge and is thereafter saved in memory, it is known as a Single Event Upset (SEU) and if that single particle upsets many memory elements, it is called a Multi-Cell Upset (MCU) or Multiple Bit Upset (MBU) [13]. SEUs may be viewed as SETs that propagate through to memory and consequently affect sequential logic devices like registers and flip flops [3].

When high energy particles like protons possess sufficient energy, they may cause a direct single event upset through ionization or if they are neutrally charged like neutrons, their secondary interaction with the device matter may still cause an SEU [21].

SEUs may also be caused by energetic ions colliding with the nucleus of an atom in a sensitive component location leading to the splitting of a nucleus (spallation) [20]. This spallation leads to ionization which consequently leads to the upsets.

2.5.3. Single Event Functional Interrupt (SEFI)

Single Event Functional Interrupts (SEFI) are a category of event effects which affect the sequence of more complex digital circuits such as state machines. SEFIs generally occur in the device's monitor circuitry and push its operation to a halt state. They indicate a disruption in support circuits like the configuration memory, JTAG modules or the signal clock generator [23]. SEFIs are reversible through power reset but should not be left unmitigated because they may lead a digital circuit to enter an undefined state.

Permanent Effects

These effects are irreversible and cause failure in circuits deployed in high energy radiation environment like space. They include some of the following:

2.5.4. Single Event Gate Rapture (SEGR)

Single Event Gate Rapture (SEGR) is a potentially catastrophic effect on microelectronics that occurs due to the breakdown or rapture of the gate dielectric due to a high electrical field. They are mainly caused by heavy ion strikes and generally affect power MOSFETs [13]. SEGRs are dependent on angles of incidence of the particle strike and the electric field in the metal gate oxide [13].

It occurs when a higher voltage than normal is used at transistor gates and is commonly observable in memory which is non-volatile namely, EEPROM.

2.5.5. Single Event Burnout (SEB)

Single Event Burnout (SEB) occurs when an ionising strike leads to a transition from a stable low current to a stable high current bias point on the current-voltage curve [13]. According to [21], electron-hole pairs of a high density are produced when there is a high energy particle ionization in a silicon device.

If a drop in voltage occurs at the transistor's base-emitter junction, greater than its cut-off, occurs, it will switch it on and lead to a high power density situation which may cause an increase in junction temperature [21]. Such a condition is catastrophic and leads to a device's permanent damage. SEB has been known to affect high power MOSFETs, BJTs and N-power transistors such as the VDMOS transistor whose cross-section area is shown in figure 7 [13].

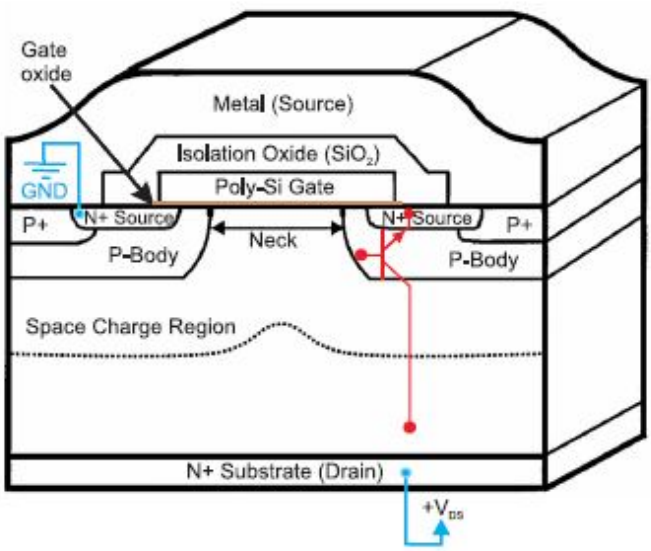

Figure 7 - VDMOS transistor showing its cross section [21]

2.5.6. Single Event Latch-up (SEL)

Single Event Latch-up (SEL) is a permanent form of SEE which occurs when there is excess current in the base of a transistor due to charge deposited by a highly energised ionising particle. [13] It leads to the CMOS logic getting latched to a high state and can potentially be destructive to the microelectronic device. A device's latch up state can be reversed by disconnecting its power.

An investigation of the effect of Single Event Latch-up in a CMOS device was carried out by [24] using pulsed laser technology. In the study, it can be noted that characterisation of SEL is similar to that of event upsets, in that the relationship between the cross section and the energy is analysed using a graph. The generated graph is then used to give an indication of the probability of an SEL occurring in the device [24]. One such graph was derived from a Weibull distribution and is shown in figure 8.

The probability of an SEL happening is obtained by dividing the pulses which cause latch-up by the overall pulses which occur at certain energies as seen in equation 1

$$\text{Latch up probability} = \frac{\text{number of pulses resulting in latchup}}{\text{total pulses in energy range}}$$

Equation 1 - Latch up probability [24]

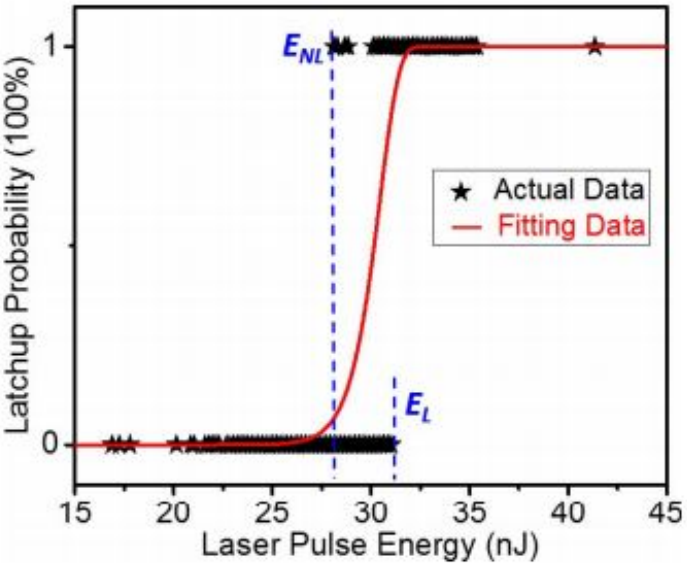

Figure 8 - latch up probability at different energies for a laser pulse [24]

From the figure 8 above, the experimental test made use of 3500 laser pulses and it can be noted that the region between E_{NL} and E_L is the range of laser energy whereby latch-up is most likely to occur [24].

2.6. Spacecraft charging

Another effect by high energy ionising radiation in space is spacecraft charging. It has been defined by [18] as the accumulation of charge in and around the materials used in spacecraft, specifically inside the dielectric. It is caused by a difference between the flux of ions and the ambient electrons due to the accumulation of charge on the surface or interior of a spacecraft when exposed to an environment with high energy electrons, magnetic fields, ambient plasma or solar radiation [18].

Spacecraft charging is of great concern in geosynchronous orbits because sometimes, a spacecraft may travel from a region of high plasma density and low-energy plasma to another with low plasma density and high energy plasma. It is even a greater concern in observation satellites which are generally launched in the sun synchronous orbits, where they always pass through the poles [25]. The geomagnetic field induces coupling to the polarised surface charge of the spacecraft hence making it effectively a dipole. This in turn makes the spacecraft rotate to always align itself to the earth's magnetic field as it propagates through the orbit [25].

Figure 9 below shows the relative position of the earth, plasma sphere and the geosynchronous orbit where spacecraft are most susceptible to charging.

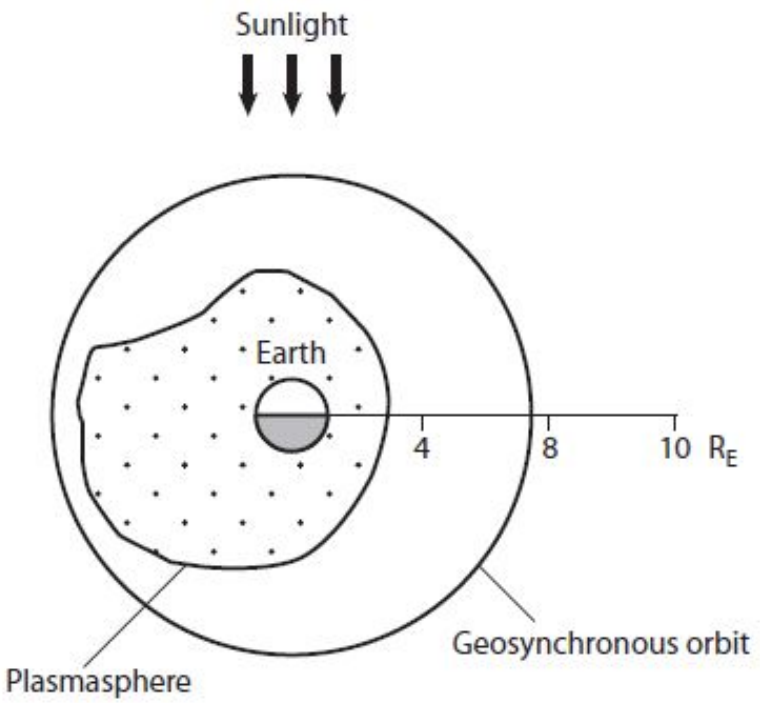

Figure 9 - Position of the geosynchronous orbit and plasma sphere relative to earth [26]

The plasma sphere region around the earth possesses low energy but high flux density and surface charging hardly occurs in spacecraft [26]. It has been seen to occur less in low earth orbits as compared to medium and geosynchronous earth orbits which possess lower plasma flux densities but high energies [18].

Before launch, it is important to determine appropriate altitude at which spacecraft will fly to reduce the effect of spacecraft charging when crossing high energy Van Allen belts. However, of greater concern in this region is dielectric charging, which is a similar phenomenon to spacecraft charging but has been seen to sometimes occur [18].

All in all, when compared to SEEs and TID, spacecraft charging is generally of lesser concern in microelectronics but cannot be ignored because it can cause damage to on-board microelectronics and telemetry systems and eventually lead to inaccurate measurements in spacecraft [18].

2.7. Total Ionization Dose (TID)

Total Ionization Dose (TID) refers to failure or degradation of semiconductor devices especially MOSFETs due to an accumulation of high energy ionising radiation like electrons, protons (from solar flares) and heavy ions trapped in the earth's field [21]. In the space environment, Galactic Cosmic Rays do not cause TID due to their low flux. TID failure differs from SEEs in that; it is caused by a deposition of highly charged particles over a long period compared to the instantaneous SEEs [21].

Devices under continued radiation exposure suffer from an increase in leakage current and eventually become unresponsive due to failure from TID. In order to characterise the effect of TID, heavy ion sources like Cobalt-60 are used to radiate a device and its leakage current is monitored over a period of time. One example of such an experiment was conducted using a Silicon-on-Sapphire (SOS) CMOS device and thereafter the current-voltage relationship in graphs seen in figure 10 (a) and (b) was analysed [27].

(a) (b)

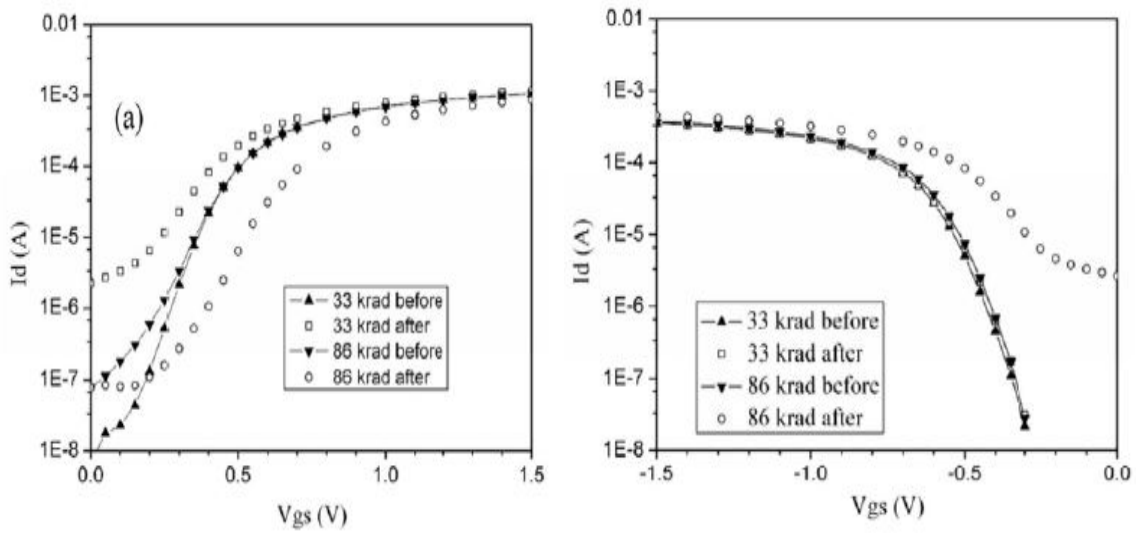

Figure 10 – trapped charge before and after radiation in NMOS and PMOS devices [27]

An increase in current with voltage occurs when the Co-60 gamma radiation hits the device and there is an accumulation in leakage charge [27]. In figure 12 above, the NMOS and PMOS device's current-voltage curves have different polarities because of trapped positive and negative charges respectively but it can be seen that there is an increase in current with voltage as radiation occurs [27].

2.8. Probability of radiated ionising particles causing SEEs

It is important to note that not every particle that collides with a semiconductor device will cause an event upset. The probability of a radiated ionising particle causing a SEE depends on two parameters: cross sectional of the device and the linear energy transfer (LET). Cross sectional of the device, σ is defined as the ratio of the number of upsets counted to the area over which they occurred on the surface of the semiconductor material. It can also be seen as the reciprocal of fluence required to cause a SEE and is shown in equation 2. Cross section per bit (shown in equation 3) is the ratio of the device cross section to the number of flip flops in the design.

$$\sigma = \frac{\text{number of upsets}}{\text{number of particle per given area } (\frac{\text{ions}}{\text{cm}^2})}$$

Equation 2 - cross section of the device

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops in design}}$$

Equation 3 - cross section per bit

Different particles react differently with energetic collisions. As seen in section 2.4, protons for example may travel randomly in an elastic manner away from the nucleus or may cause the excitation of the nucleus when they interact with matter at high energies. According to [28], when a particular form of interaction occurs to a section of material, the cross section ratio may be known as a partial cross section whereas, a summation of all the partial cross sections may be called the total cross section. Furthermore, another instance of cross section characterisation is sometimes used known as the differential cross section. It is calculated using equation 4 as shown [28]

$$\sigma(total) = \int \frac{d\sigma}{d\Omega} \, \mathrm{d}\Omega$$

Whereby $d\Omega = \sin\theta \mathrm{d}\theta \mathrm{d}\varphi$, θ is the scattering angle which is measured between the incident and scattered radiation whereas φ is the azimuthal angle

Equation 4 - Differential Cross Section [28]

Linear Energy Transfer (LET) is a measure of the energy transferred across a semiconductor material per unit length while it's penetrated by an ionising particle [21]. Often, LET is referred to as the stopping power of the particle [21]. Different materials have different LET thresholds, above which a SEE is seen as increasingly likely to happen. It is therefore a factor of the type of particles which collide with the material, energy and its atomic mass. LET is an important parameter for characterisation of SEEs because it gives an indication of a particle's ability to deposit sufficient ionising energy to cause a disruption [21].

By plotting the cross section, σ against LET on a curve, conclusions may be drawn to establish the probability of a SEE happening in a particular semiconductor material. Figure 11 illustrates one such curve for different devices using heavy ions [29]. The information in this curve is used to calculate the error rate by integrating the cross sectional, σ with respect to LET.

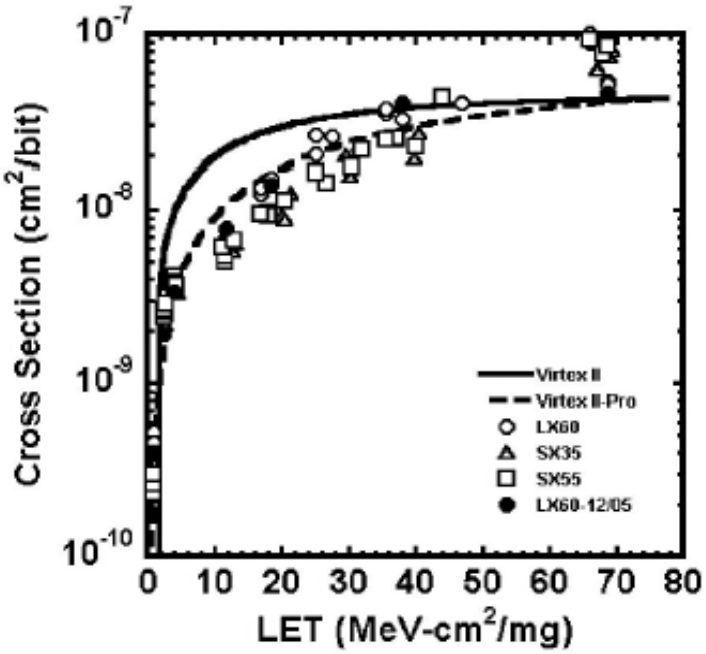

Figure 11 - Cross section, σ verses LET for different devices using heavy ions [29]

In figure 13, the Virtex II FPGA device was considered as the test device. The SEU cross section, σ threshold is approximately $4x10^{-8}$ cm²/bit after 20-30 cm^2/mg meaning that sensitive nodes of the device shall be increasingly affected by a SEU beyond that energy level. Generally, for cross section area versus LET curves, the threshold LET can be arbitrarily considered as the LET value where the cross-section is 10% of the saturation (maximum) cross-section area [22].

From this information, other important parameters can be calculated and analysed such as: error signature trends, SEU rate per bit per unit time and the LET spectrum which can be used to give a better indication of the device sensitivity [13].

The major material element in microelectronic devices is Silicon, and it is often the assumed target material used when characterising the device's sensitivity to SEEs [13]. However, in order to obtain more elaborate results, it is important to take into consideration the other materials that exist in the microelectronic device. Also during testing, it should be irradiated with different particles at different energy levels using varying orientation [13].

Since every particle colliding with a device will not cause an upset, it is advisable to expose it to sufficient radiation particles in order to produce a larger number of observable errors; say ≥100 upsets for each LET. This increases the credibility of the SEE characterisation test results.

2.9. Models for Prediction of event upset rate

Due to the limited beam time when carrying out event upset characterisation, there have been a number of models used to predict the event upset rate. It is often not practical or financially viable to use a variety of energy levels and one such model was developed by W.L Bendel in 1983 [30]. The Bendel-1 parameter utilises a single energy parameter to fit the information onto a cross section versus linear energy graph using equation 5 shown below:

$$f(e) = (\frac{24}{A})^{14}[1 - \exp(-0.18\mathrm{Y}^{0.5})^4$$

$Y = \left(\frac{18}{A}\right)^{0.5} (e - A)$ 'A' refers to the apparent threshold and e is measured in MeV.

Equation 5- Bendel-1 parameter function [30]

The Bendel-1 parameter equation utilises a parameter 'A' known as the apparent threshold which gives a measure of the rapid rise in a device's cross section σ from its threshold energy [30]. It is a constant which is dependent on the type of equation used to fit data onto a graph.

W.L Bendel further improved the original Bendel-1 parameter equation by utilising two energy parameters. By doing so, it improved the accuracy of the original parameter [31]. However, this could come at a cost of limited accelerator time and money because of beam downtime during setup of the second energy [31]. The Bendel-2 function as it came to be known has two parameters A and B shown in equation 6 below.

$$f(e) = (\frac{B}{A})^{14}[1 - \exp(-0.18\mathrm{Y}^{0.5})^4$$

$\mathrm{Y} = \left(\frac{18}{A}\right)^{0.5} (e - A)$ Where 'A' and 'B' are fit parameters and e is measured in MeV.

Equation 6 - Bendel-2 parameter function [31]

An investigation on the effectiveness of modelling upset cross section data using the Bendel-1 and Bendel-2 functions was carried out by [31]. Five different energies were used between 30MeV and 149MeV and it can be observed from the graph in figure 12 that the Bendel-1 function deviated from the data a lot more compared to the Bendel-2 function. It is because of this sort of inaccuracy that the Bendel-1 parameter is not favoured for characterising upset cross section area [31]. An even more accurate function is the Weibull fit which utilises three energies to model upset cross section.

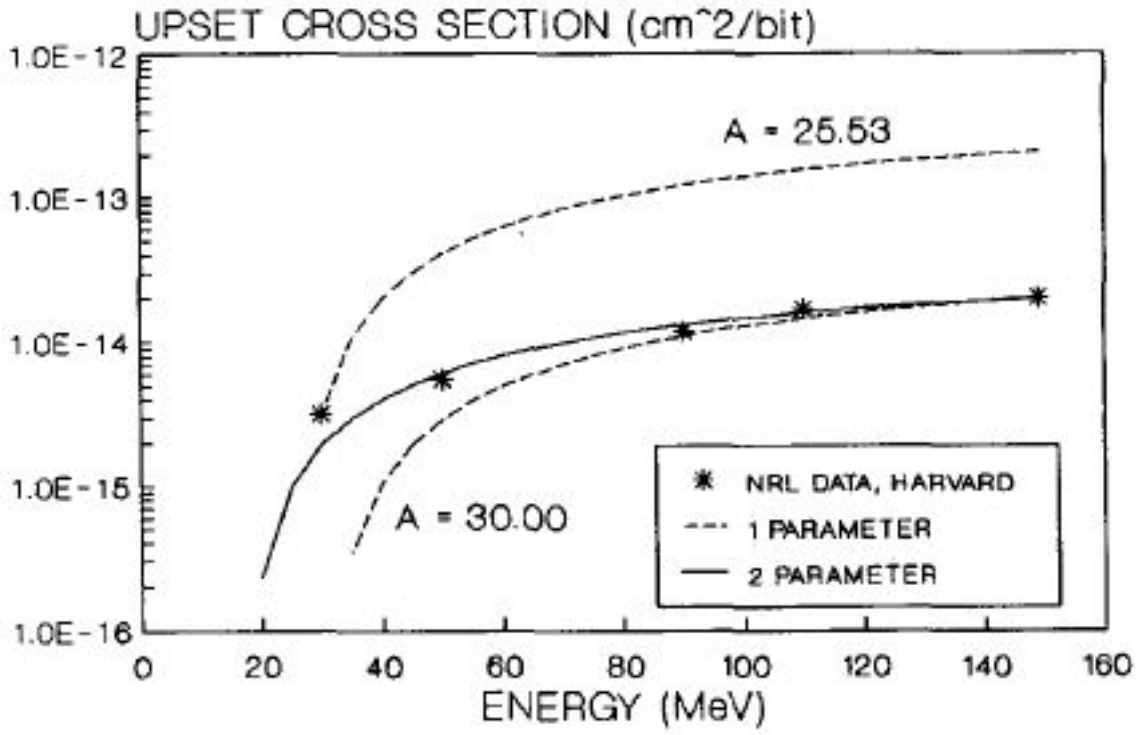

Figure 12 - Cross Section versus energy data using Bendel-1 and Bendel-2 functions [31]

It should be noted that when these models are used to plot a curve of cross section versus varying energy, one cannot accurately predict the device's cross section [30]. However, they do show the energy at which a change in the cross-section of a device will be very negligible [30].

Another model known as PROFIT was developed by [32]. Unlike the semi-empirical Bendel models introduced earlier, PROFIT is a purely empirical function which can be used to accurately model upset cross section when experimental data is not available. Figure 13 shows the results of the model when compared to the Bendel function [32]. It should be noted that the PROFIT model function should be used to complement experimental data generated by either the Bendel function parameters or if possible, the Weibull function [32].

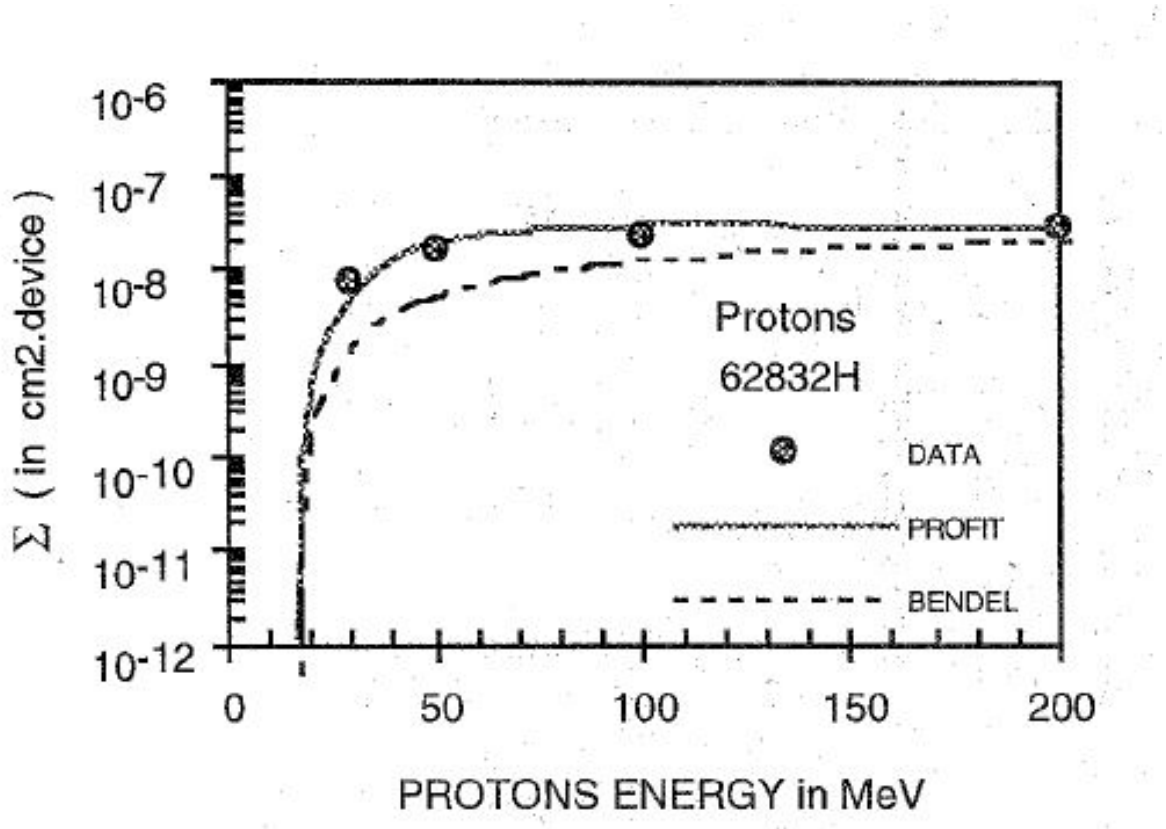

Figure 13 - Cross section modelling using the PROFIT empirical function [32]

2.10. Test Setup for SEU Detection and Mitigation

The goal of radiation testing is to calculate the cross section area, σ in relation to the linear energy transfer. There are various testing approaches to doing this, but they all depend on a number of factors which include, but not limited to: the device type, hardware design, methodology of results logging among others.

Upon understanding the critical elements of the device to be tested, a testing structure must be developed. A test structure for evaluating the effectiveness of a mitigation technique against SEEs would be different from that used against TID for example [17]. When testing for a device's susceptibility against SEUs, it is important to consider the size of the hardware to be designed because the more complex a circuit becomes, the higher its probability to mask upsets which would mean void results and hence an inconclusive test. [17]. The most common structure for testing the effect of SEUs in a device is using a series of shift registers connected in a long serial pattern back to back as seen in figure 14.

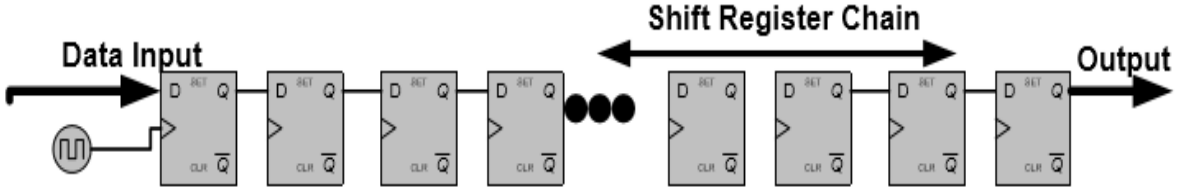

Figure 14 - Test Structure used for SEE characterisation in FPGA devices [22]

The testing structure shown in figure 14 does not entirely depict a real design because most real designs would contain both sequential and combinational elements [17]. If high frequencies are to be tested, it would therefore not give optimal results due to the high speed switching [17]. For this reason, the serial register structure would only be ideal for the characterisation of susceptibility against SEEs in low frequency designs [17].

A variation of the shift register test structure introduced in figure 14 can be considered whereby counter circuits replace the flip flops so that it operates like an accumulator circuit [17]. By doing this, the simplicity of the shift register would be reduced since the new circuit would incorporate both sequential and combinational logic elements.

When a reliable test structure has been developed, the device must be placed on a rig or test bench where it shall be radiated by the high energy ionising particles. Such a rig should be dynamic in the sense that it can hold the device in different orientations, possibly hold multiple devices to allow for concurrent testing and also allow easy setup [17]. One such test rig was developed at the Nelson Mandela University by previous undergraduate engineering students and is shown in figure 15.

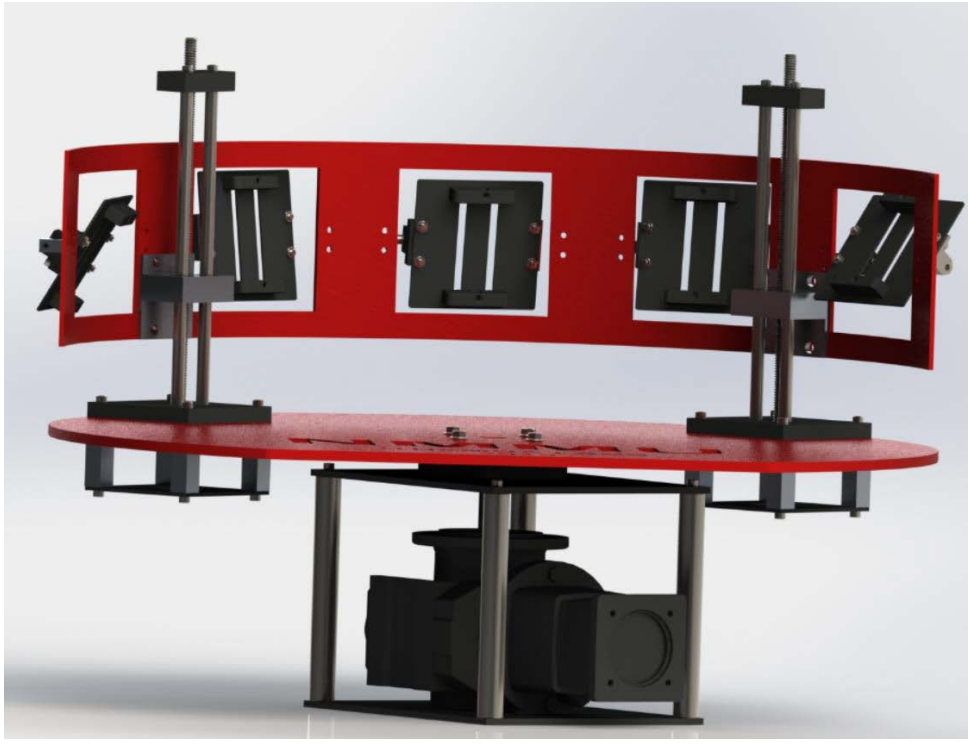

Figure 15 - PCB rig developed at the Nelson Mandela University

The test rig in figure 15 possessed a number of features that are ideal for device testing against radiation effects which included: allowing multiple devices to be tested at a time, orientation control using an independent program from a remote PC, protection against some noise resulting from radiation among others.

Whether dynamic or static testing is to be used, the counting of upsets should be reliable and this involves ensuring that the counting device has sufficient speed to log every upset that occurs. There are a number of methods which have been used to count the number of upsets which occurred during radiation testing.

There are two common methods used to ascertain the probability of a SEE happening in the semiconductor material of a digital logic device, these are: particle irradiation technique and the pulsed laser technique. In both these methods, testing can be done in static or dynamic modes. In static mode, a device's registers are given a pattern of predetermined data, and then the testing carried out and subsequently checked to see whether the data has changed. In dynamic mode, testing is carried out while using another device to continuously check whether data loaded in the tested device's registers is altered. This subsection explores the particle radiation technique, pulsed laser and also introduces modelling of errors using fault injection.

2.10.1. Particle irradiation technique

The irradiation technique involves accelerating particles towards a digital logic semiconductor device and counting the resultant number of SEEs at a particular energy level. The main particles used for irradiation testing are: protons, neutrons and heavy ions. The choice of particles depends on the application where the device shall be used, for example, satellites in the UoSAT orbit are greatly exposed to heavy ions and as such, it is more logical to use them for testing as opposed to neutrons [22]. Heavy ions have the advantage of possessing sufficient LET to cause SEEs through direct ionization. Protons on the other hand require interaction with the particle nuclei to produce secondary particles which possess sufficient energy to cause a SEE and such consideration needs to be made before carrying out tests [22].

Testing for SEEs using particle irradiation is done either under a vacuum chamber or in open air. Vacuum chamber particle irradiation is more commonly associated with heavy ion tests [22]. It has the advantage of maintaining a high energy beam and thus provides a more accurate set of results. However, it requires a longer set up period and is thus better suited for testing which requires less equipment changeover [22].

Open air radiation is more associated with proton and neutron tests and has a quicker set up time. It produces a wider diameter beam compared to vacuum testing and this is a major disadvantage as it might damage components that are not part of the target area. It also has reduced beam energy due to losses and is less representative of the space environment than vacuum testing. Figure 16 shows a generic SEE testing setup [3]

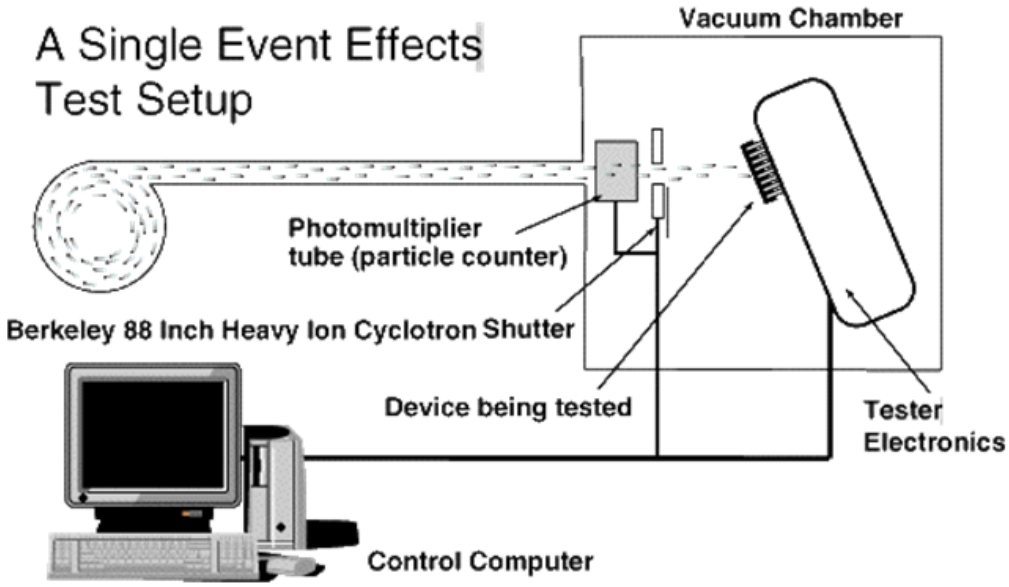

Figure 16 - a generic SEE test setup [3]

2.10.2. Pulsed laser technique

Pulsed laser method uses a laser source, such as a laser diode to direct a pulsed beam towards a DUT in order to create an upset. The beam is pulsed at frequencies in the GHz range and its intensity is kept low to allow one to describe the interaction between light and the semiconductor material [33]. The technique involves monitoring parameters such as: the beam's radius and confocal length, material absorption, surface reflections and optical wavelength in order to determine the charge density profile of the semiconductor of the DUT [3].

In comparison with the ion irradiation technique, it is less costly, less destructive (when the laser's intensity is limited) and allows for the testing to be focused on a smaller area. Also, it is very convenient because it does not require setting up a vacuum. However, it has limitations on the penetrative power through some metal materials [33].

Pulsed laser method, like the particle acceleration technique can be used to obtain the threshold of SEUs if the laser is well calibrated, but cannot be used to accurately characterise the cross section area versus the effective Linear Energy Transfer (LET). [33] It is for this reason that the technique is better suited to provide additional information about SEE characterisation and detection, and not as an independent test like the ion accelerated irradiation technique [33].

2.10.3. Modelling using fault injection

When radiation is not readily available, simulation of the radiation environment can be carried out by fault injection to characterise the effectiveness of a mitigation technique against high energy ionising particles [34]. It is a commonly used method to assist in predicting the way a design will respond under radiation and it has been used to offer valuable information about the effect of high energy ionising particles on devices like:

- Which sections of the device are more susceptible to radiation and thus require more effective mitigation, i.e. whether the memory or combinational logic.
- How many errors are masked by the hardware design and if so, should the design topology be altered.

Fault injection involves using a simulation application to intentionally add errors into sections of the hardware design model and thereafter observe the response on an interface like a PC. It generally offers a good enough estimate of a circuit's upset susceptibility but has the downside of missing the accurate statistics on a design's critical elements. Literature from [34] states that larger and more complex designs require more faults to be injected at different sections of the circuit in order for the simulation to provide more accurate statistics.

A reliable fault injection methodology should have a high upset rate and it is for this reason that FPGAs have been favoured recently due to their high speed. Furthermore, when designing a fault injection tool, the following considerations should be taken in order to correctly characterise the probability of an upset occurring in a device:

i. Since upsets caused by high energy radiation occur randomly, the fault injection tool should be capable of introducing faults at any point in the circuit in a random manner.
ii. The period over which a fault is introduced at any point in the circuit should be alterable, i.e. how long the errors are injected should be a variable value so as to cause variation in the nature of upsets. In the experiment conducted by [35], upsets in the SRAM had faults inserted at the input nodes for a period of 20ns whereas those inserted further down the circuit had different times for their insertion [35].
iii. Since it is a difficult process to accurately simulate an ionising radiation environment, some assumptions have to be made. One such assumption is that all signals within the hardware design, with the exception of the inputs and outputs, are prone to upsets [35]. In so doing, the designed fault injection tool shall ensure that it only generates a corresponding quantity of outputs as the number of signals [35].

In SRAM based FPGAs which are used in a radiation exposed environment like space; errors injected to the flip flops can acceptably be used to characterise the effect of upsets in the design [36].

Xilinx utilises a mechanism known as FLIPPER which has been used to evaluate event upsets (both single and multiple) in some models of their FPGAs (specifically Virtex-II) by injecting upsets in the configuration memory [8] [36]. The tool can be used to characterise a device's sensitivity by either flipping each bit in the memory or by randomly injecting errors into each section of the configuration memory and thereafter analysing the likelihood of an error propagating through the entire design [37].

The FLIPPER tool consists of hardware such as an FPGA prototyping board and an application implemented on an interface such as a PC. When errors are injected to the target device, the software works by comparing the output of the device with the simulated vectors from ModelSim and when they are not similar, a fault packet is flagged and transmitted to the PC. The general software process flow to inject errors into the design is shown in figure 17.

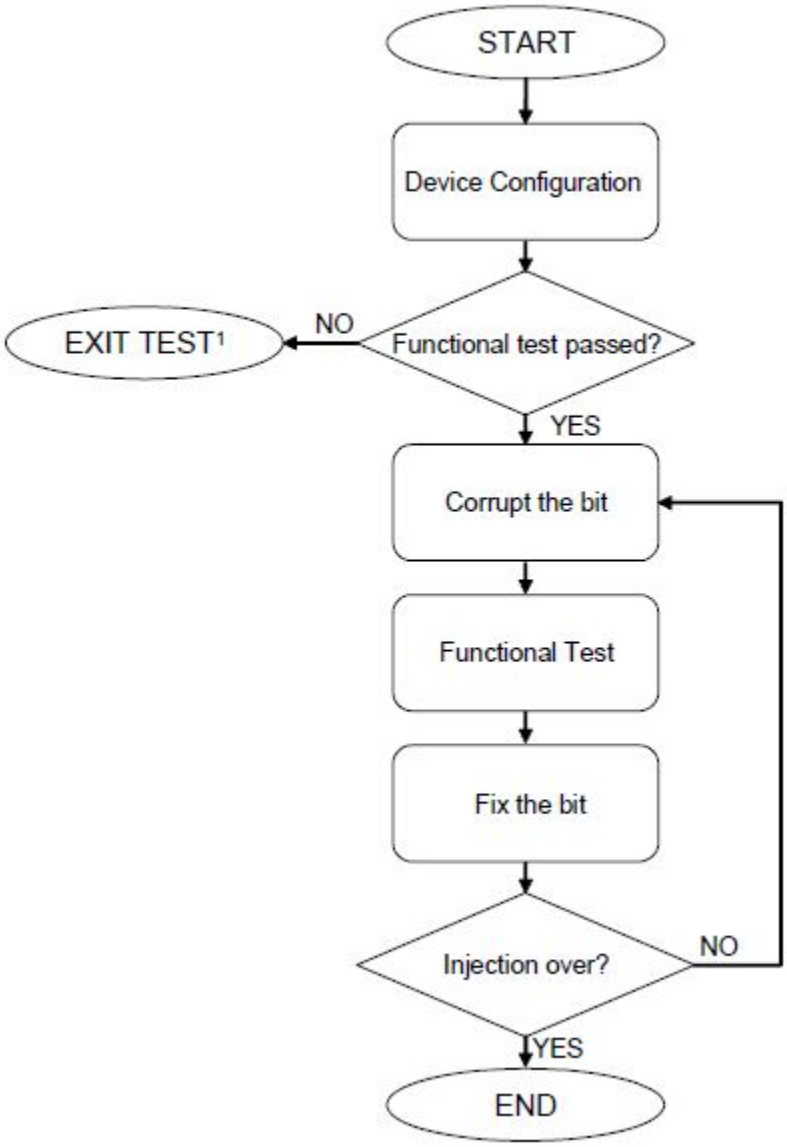

Figure 17 - Process flow of the FLIPPER tool for fault injection [37]

The Flipper system allows one to alter the specifications of the fault injection test through changing features like [37]:

i. the target device
ii. the experiment mode, whereby the user has the liberty to inject faults in a more predictable and sequential manner or in a totally random pattern
iii. nature of injected faults, whereby one can choose between single or multiple bit upsets
iv. clock speed running on the target device
v. Registers where the bit flipping shall be carried out. Flipper allows one to use an external simulation software package like ModelSim for importation of data which is used as input and output vectors [37].

For accurate characterisation of a device's susceptibility to event upsets, it is advised that modelling using fault injection is used as a precursor to particle irradiation. In so doing, the radiation testing will then serve as confirmation of the results from the simulated fault injection experiment [36].

2.11. SEU Mitigation Techniques in Digital Logic Devices

A digital logic device can be hardened against radiation during manufacture or after it has been manufactured. During design and manufacture phase, the material used can be structurally hardened using substrates or its internal electronics can be modified [4]. After manufacture, this hardening is left to the discretion of the end user and there are several techniques which include mitigation using hardware modelling and memory scrubbing among others [4]. Both categories of hardening are presented in this subsection including some techniques developed by prior researchers.

2.11.1. Structural radiation hardening

Structural radiation hardening is the process of altering the physical composition of the components used in the manufacture of the digital logic device to ensure that it reduces the effect of radiation [4].

Previous work carried out by [5] explored the use of structural radiation hardening using a substrate bias to reduce the effect of TID in a CMOS device. The method involved modification of the manufacture process of a semiconductor chip by adding a layer with a low shunt resistance below the active device known as high dose buried layer (HDBL) [4]. Such a layer prevents deposited charge from building up and consequently reduces the pulse width of a potential SET.

This reduction in pulse width is advantageous in high frequency applications where temporal mitigation techniques are not very effective. Therefore, when used along with temporal mitigation techniques, it can be very effective in reducing SETs in devices [4].

Event effects like SEUs mainly affect digital logic devices in memory elements like RAM and flip flops [4]. As such, if these elements of the design are hardened, the overall device's susceptibility to potential upsets or failure can be considerably reduced [4].

Memory elements of an FPGA can be modified through enhancing critical charge [21]. This is achieved by creating a low pass filter using increased resistance along the memory element's feedback path which reduces the effects produced in the signal and hence reduces the probability of the latch or RAM's voltage changing from 0 to 1 or vice versa [21].

2.11.2. Mitigation techniques based on hardware modelling

There are currently numerous mitigation techniques based on hardware description modelling that are used to detect and consequently correct SEEs. Upsets in semi-conductor memory cells have successfully been corrected using techniques like the Hamming codes, Single Error Correcting and Double Error Detecting (SEC-DED) codes [38]. They are often used as the first line of defence and when coupled along with other mitigation techniques, provide improved protection to digital logic devices [38]. Mitigation methods in digital logic design include redundant and filter techniques. This section shall explore some commonly used mitigation techniques and others developed more recently by researchers.

2.11.2.1. Redundant Mitigation

The most dominant redundant mitigation techniques for detecting and correcting SEEs is Triple Modular Redundancy (TMR), which involves duplicating the circuit three times and subjecting the output to a majority voter seen in figure 18 [39]. The majority voter is a comparator and could be as simple as an OR gate or XNOR gate. If an upset occurs, the comparator (majority voter) ignores the upset value of the affected module but allows the right value from the other duplicated (unaffected) modules.

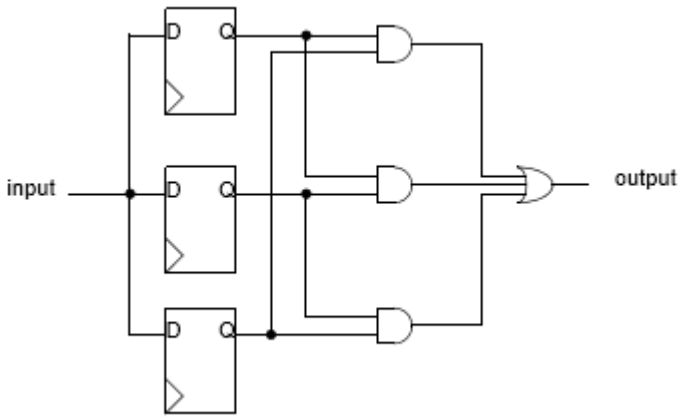

Figure 18 - A simplified TMR design using D- flip flops with a voter

Assuming the comparator circuit does not fail, a TMR design's reliability will be a function of the reliability of one of the modules. Therefore, it assumes that the failure of each of the three modules is independent. A system implementing TMR will only withstand one upset at a time and therefore won't be effective if the other two redundant modules suffer an upset at the same time [35].

TMR is generally considered one of the most effective techniques which can be used to protect large parts of a digital design like the combinatorial and sequential logic, global clock, and global control lines among others. It however has a downside of increased circuit area. A design implementing TMR may have as much as 200% more area than its original circuit [38], which also leads to a high overall power consumption and increased overall cost [40]. It is thus better used for critical applications where failure is fatal.

Many modifications to full TMR have been implemented to improve on the overall overhead savings and one such implementation is the Selective Triple Modular Redundancy (STMR) by [35]. The method implements an algorithm which identifies nodes that are sensitive to upsets and thereafter TMR is applied to only those nodes [35]. This method has a trade-off for area savings in that it does not guarantee near perfect protection of the chip like full TMR.

A modification of TMR is the Dual Modular Redundancy (DMR), which as the name suggests, involves duplicating a sequential circuit and subjecting the output to a majority voter in order to detect an SET or SEU [23]. The difference in value of the majority voter (or comparator) is an indication that an upset has occurred. Figure 19 illustrates DMR where an XNOR gate is used for voting.

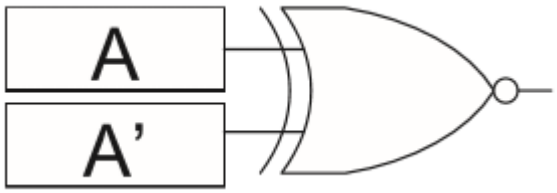

Figure 19 - DMR with a XNOR gate for voting [23]

DMR in the conventional sense only detects an upset but may not necessarily correct the error caused and thus like TMR, many modifications have been made to DMR to incorporate error correction, improve the area overhead saving and also make the technique more effective; one such modification is Diverse Double Modular Redundancy (DDMR) [41]. This modification works by implementing different input data patterns so that each module produces a different upset pattern at the output instead of simply doubling each module like the traditional DMR [41]. The modification could also be done by having another totally distinct implementation of the original module or in sequential circuits, having the two distinct error patterns happen over time [41].

Redundancy can also be implemented in time whereby one circuit's outputs differ from the other by a factor of time. This technique is used by [40] and also seen in [21] and has an advantage over spatial redundancy in that it uses less area. The technique however compromises on the overall speed of the system which could be a major problem for time critical applications [21]. Both forms of redundancy can be combined and this has the advantage of ensuring good system speed without increasing the overall size overhead [40].

2.11.2.2. Memory Scrubbing

Scrubbing is a technique which is used for verification and restoration of the original configuration in micro-electronic chips including FPGAs. A simplified technique of scrubbing was explored where sections of an FPGA's SRAM were re-written repeatedly from a memory bank which was less sensitive to upsets from high energy radiation [21]. It utilised a counter as part of the memory scrubbing circuit to observe the SRAM and configuration memory of the FPGA and thereafter replaced it with a correct version of the data [21].

Memory scrubbing can be used in conjunction with redundant techniques like TMR or DMR to ensure more effective mitigation whereby both the user logic and memory blocks of an FPGA are protected from radiation event effects [21].

2.11.2.3. Example variations of the common mitigation techniques by researchers

Digital technology is constantly shifting towards the use of smaller, more efficient integrated circuits and the excessive area overload of TMR and to some extent DMR has led many researchers to seek mitigation techniques which have an area savings with respect to TMR. Many of the techniques still implement some aspects of modular redundancy while others implement filter technology or a combination of both. Some of these techniques developed in later research are introduced in this subsection.

Guard gate mitigation

This methodology was proposed by [42]which utilised a guard gate circuit for mitigation against single event transients. The circuit is made up of four Field Effect Transistors which have one output and two inputs. It operates on the principle that the output impedance is latched high when the gate's inputs are different but the same output behaves like a normal inverter if the inputs are similar [42]. A modification of this guard gate technique was implemented using a delay element as seen in figure 20 which ensured that the gate's inputs differ in time and not in value [40]. By doing this, when a transient occurs at one input of the user logic, delay circuitry ensures that it varies from the other input.

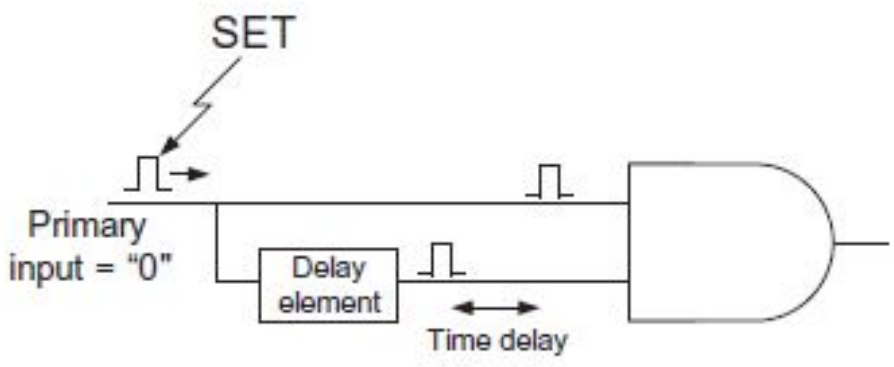

Figure 20 - Delay element added to the input of a gate [40]

This technique's level of efficiency was dependent on the pulse width of the transient. It was generally seen to be effective in mitigating FPGAs against SETs which could cause SEUs and also offered better area usage compared to TMR [40]. However, it compromises on the overall speed of the system which could be a major problem for time critical applications [21]. All in all, using the guard gate in conjunction with a delay element was seen as an optimal mitigation technique for COTS components used in small applications in space [40].

The guard gate technique presented was a variation of a similar technique which uses a AND-OR gate and multiplexer combination to each primary output of combinational circuits to eliminate SEUs [40]. It works on the basis of using an AND gate to suppress an SET reaching the primary output when the primary output's logic is 0 and an OR gate when the primary output's logic is 1. The multiplexer selects the AND or OR gate when the primary output from the combinational circuit is 0 and 1 respectively. This technique is configurable using DMR or using a delay element to detect the upset depending on the application. Figure 21 shows a configuration when using the DMR.

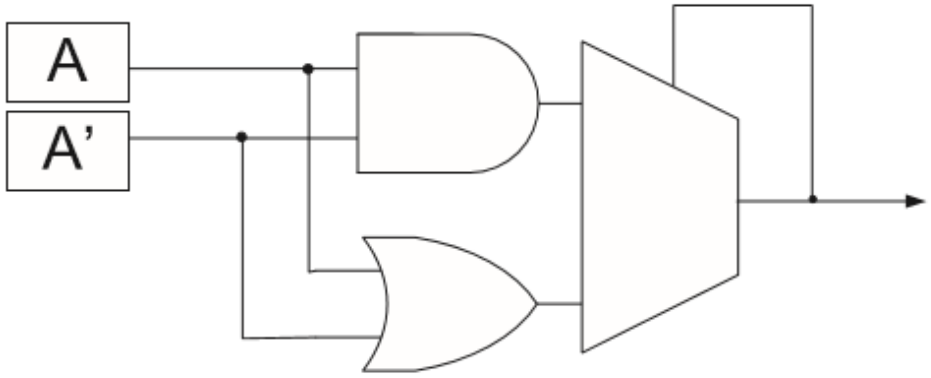

Figure 21 - AND-OR, Multiplexer combination utilising DMR [40]

A SET suppressor was designed to protect circuits against single transients originating from combinational circuits that affect flip flops [38]. The mitigation technique works on the basis of adjusting the timing of the clock edge in order for the flip flop to capture or record data when it reverts to its correct state. It is a reliable technique for mitigation of SETs which have a relatively short pulse width [38].

The SET suppressor shown in figure 21 was modified by F. Smith using an OR and AND-gate in place of the multiplexer as seen in figure 22. It works based on a similar principle as the AND-OR multiplexer. However, the OR gate acts as the comparator for the two AND gates.

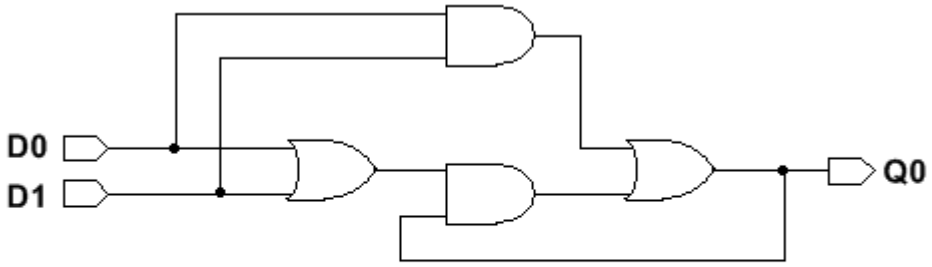

Figure 22 - SET filter

Sequential circuit state freeze

Another novel technique for mitigation against SETs and SEUs was developed at the Nelson Mandela University which utilised DMR to detect an upset and thereafter pauses or 'freezes' the sequential circuit during a particular state if a transient or upset is detected [23]. When the SET or SEU dissipates, the circuit is 'unfrozen' and it is allowed to carry out its usual operation. It is a technique more suited for applications where a time delay is not of great consequence and works only in non-volatile FPGAs and ASICs [23].

Fault recovery using evolutionary techniques

More recently, evolutionary fault recovery techniques have increasingly been developed by researchers to aid in the mitigation of event upsets in FPGAs [21]. These utilise artificial intelligence algorithms like genetic algorithms (GA) to dynamically alter and adapt a circuit design in order to conceal upsets [21]. One major downside in implementing these techniques is that they are time consuming when converging to a better solution in larger designs and hence they may only be better suited for smaller circuits and not large complex circuits [43].

Dynamic Partial Reconfiguration

A section of the FPGA can be reprogrammed after its original configuration while other sections of the design continue functioning normally using a technique known as dynamic partial reconfiguration (DPR) [44]. As such, errors can be corrected in flip flops affected by upsets using memory scrubbing while the rest of the logic functions uninterrupted [44]. It is an efficient technique for improving fault tolerance where device area is limited and critical sections of the design must run continuously. It can also have the added benefit of reduced cost through dynamic power consumption. An example of this technique was implemented in the Mars Rover where 6 Virtex chips were used to dynamically correct each other upon detection of errors [44].

3. CHAPTER 3

3.1. Research design and methodology

This subsection introduces the device under test and monitor circuitry, and then illustrates how the upsets were counted for the different implementations in the test structure. Furthermore, this chapter also presents the testing facility and procedure used at iThemba LABS.

3.1.1. Device under Test (DUT) Selection

Chapter 2 introduced the various types of micro-electronics and their suitability in different conditions, particularly the radiation exposed environment like space. The device under test (DUT) refers to the particular micro-electronic component where digital sub-designs were implemented, synthesized and thereafter tested for reliability under high energy radiation conditions.

Before selecting the DUT for single event upsets testing, numerous factors had to be considered. Specifications of the devices in the data sheet had to be thoroughly studied and comprehensively understood. Such specifications included: the overall power consumption, speed of switching, input/output capabilities and the device's internal elements among others. With this in mind, some questions had to be considered, such as:

- What kind of combinational or sequential logic shall be available for testing?
- Is some sort of mitigation already provided for some of the device's elements?
- Shall cooling be required in the event of high power consumption by the device?
- What switching speed does the device's IO blocks run at and can this speed ensure that the signals have integrity? [17]

In order to answer these critical questions, comparisons are made between different micro-electronics and their suitability in different environments. It can be noted that Digital Signal Processors (DSPs) are reprogrammable and generally have low power consumption which would be ideal for space bound usage but they have the downside of limited application use. FPGAs allow a designer to specify various combinational and sequential logic designs and provide very high switching speeds which would ensure that signals always maintain their integrity [8]. Also, because of their re-programmability, event upset mitigation techniques can always be added and altered after a design has already been specified [17]. This major advantage over ASICs affirms that FPGAs offer a great compromise selection as a suitable DUT even at the expense of higher power consumption.

Since there is a variety of FPGAs in the market, further parameters like density, speed, power and IO count had to be taken into account when selecting a suitable FPGA. Very high speed was not a determinant factor in this selection because a simple non time-critical application would be tested.

Therefore, the IO ports in use could be low speed but have an adequate number for connectivity to the logging circuit. The density of the device also had to be looked into to avoid an instance of over-specifying which would increase the cost of the device. Finally, the power dissipation would predictably be low due to the nature of the application and its operating mode and hence a low power device could be specified which also would eliminate the need for special thermal control. If TID was to be tested, high currents would be anticipated, hence the need for a device which is able to handle higher power.

Xilinx Artix-7 50T FPGA

Based on the considerations, Avnet's Artix-7 50T evaluation board shown in figure 23 was selected to host the DUT for this research. It is developed by Avnet and runs the Xilinx XC7A50T-1FTG256C FPGA whose HDL designs can be synthesized and implemented using the Vivado Design Suite through schematic entry, VHDL or Verilog. [8] It is a low cost device which is suitable for low power applications and thus ideal as a commercial off the shelf component for small scale space applications. It is easily powered via +5v micro USB and some of its major features include:

- 256 MB DDR3 SDRAM
- 32 MB of QSPI Flash
- 32 KB of I2C EEPROM
- 6 Digilent PMOD compatible headers
- Dual 10/100 Ethernet interfaces offering IEEE 1588 support
- JTAG programming/configuration port
- USB-UART interface

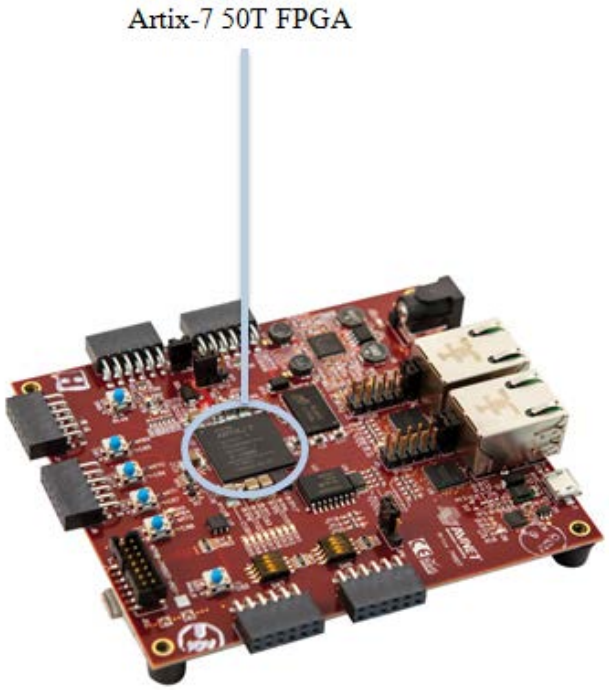

Figure 23 - Avnet's evaluation board showing the Artix-7 50T DUT [8]

The Artix-7 50T FPGA is an unmitigated device. Xilinx however does provide a tool known as TMRTool for automatic implementation of a TMR scheme into the FPGA design. It is implementable in the more expensive Virtex family of FPGAs and is thus suitable for high density devices in high radiation environments where robustness may be leveraged by triplicating the design. This project was meant to validate the use of low cost commercial off the shelf devices, typically under R4000 (at the time of this writing) and the FPGAs capable of running this tool were out of this project's budget range and were hence not considered.

3.1.2. Monitor Circuitry and Error Logging

The purpose of the monitor circuitry was to detect and flag for any upsets that occurred in the DUT during testing. A simple Exclusive OR (XOR) logic gate was implemented via VHDL and synthesized on a similar Avnet Artix-7 50T FPGA to compare the output signals of the replicated benchmark circuits from the DUT. When the inputs of the comparator are similar, a low signal was given which signified that no errors were detected whereas, when the outputs differed, a high signal was generated signifying that an error was detected. This is illustrated in the truth table in figure 24.

Truth Table		
B	A	Q
0	0	0
0	1	1
1	0	1
1	1	0

Figure 24 - Exclusive OR gate truth table

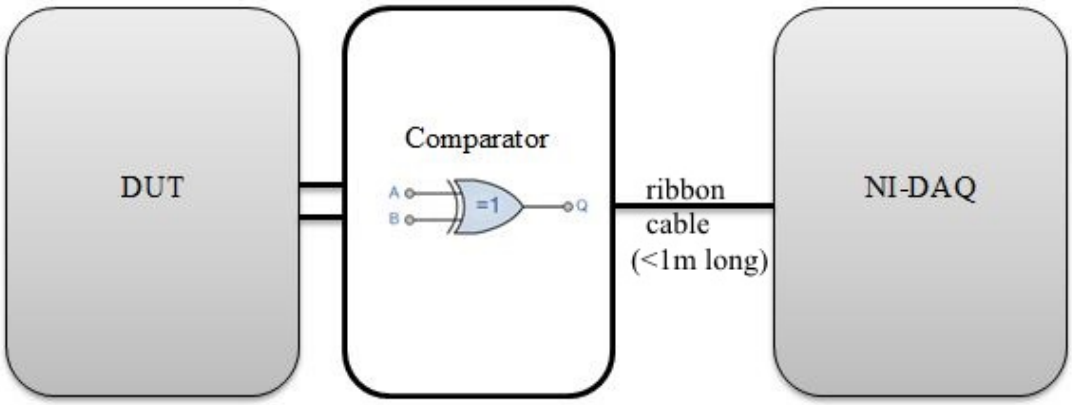

Figure 25 – Block diagram description of the setup showing the monitor circuit comparator

The monitor circuit was connected to the DUT through the Peripheral Module (PMOD) expansion interface on the Artix-7 development boards by the use of ribbon cable as seen in figure 25. An overall schematic showing the connection between the DUT, monitor circuit, NI-DAQ and PC is shown in Appendix B.

The monitor circuit was placed away from the beam and shielded from direct radiation by lead blocks (marked A) as seen in figure 26 below. Lead was used as it generally has excellent stopping power against high energy radiation.

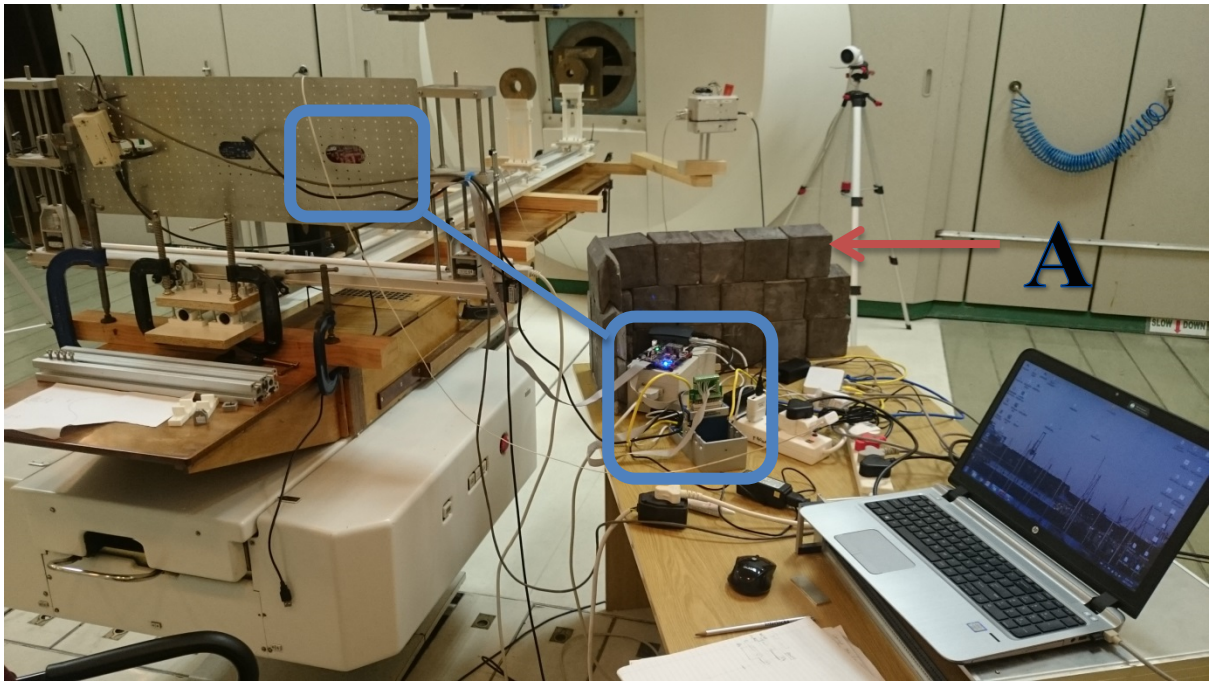

Figure 26 - The monitor circuitry and error counter shielded by Lead blocks

Data acquisition and error counting was carried out using the CDAQ-9184 model of the CompactDAQ Ethernet from National Instruments. It is a modular data acquisition system which comprises of four removable input/output modules mounted on chassis and communicating via Ethernet shown in figure 27 [45]. Since only digital measurements were required for the error counting circuit, a single 32 pin digital input/output module was sufficient.

Figure 27 - National Instrument's Compact DAQ used for error counting

The module selected for this application was the NI-9403, which is a bi-directional digital input/output module running 5V TTL signals whose pin out is shown in figure 28 [45]. It also allowed easy connectivity via ribbon cable to the monitor circuit FPGA with the help of an additional terminal connector. The length of the ribbon cable between the monitor circuit FPGA and the NI CompactDAQ was kept less than 1m to reduce potential electrical noise as illustrated in figure 25 and seen in figure 26.

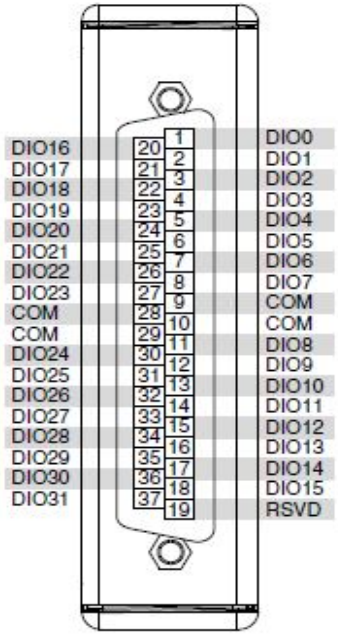

Figure 28 - NI 9403 Digital input/output module [45]

The error counting code was written in LABVIEW, which is National Instrument's graphical programming language. It provides a user interface on the PC known as the front panel whereas the code is specified in the background. The front panel for the error counter interface seen in figure 29 showed the number of upsets which were to be counted from three hardware designs implemented on the DUT. These designs are introduced in section 3.1.4.

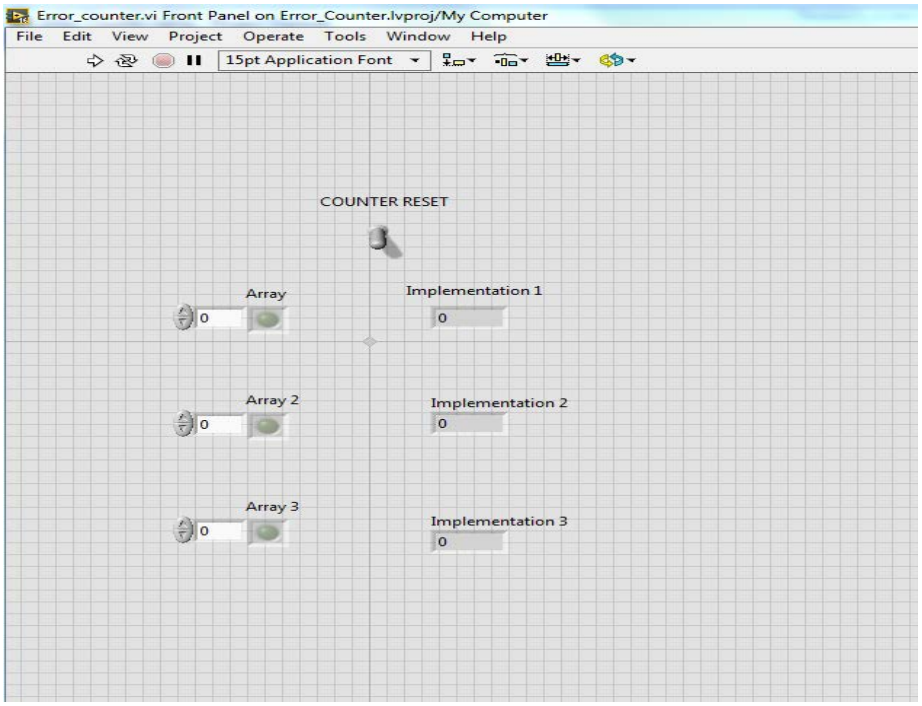

Figure 29 - Front panel of the LABVIEW program

When the monitor circuit detected an SEU, it was latched and then the counter incremented by 1 as seen by the True condition of the code in the figure 30. The loop's false condition would reset the count for each of the three implementations.

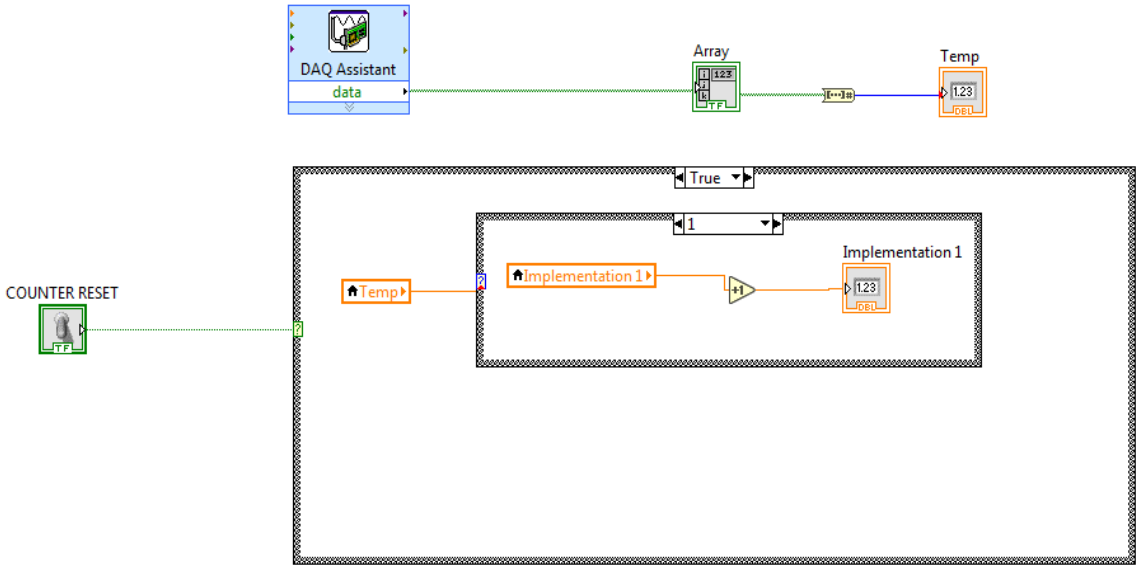

Figure 30 - True condition statement which executes when an SEU is detected

3.1.3. iThemba LABS Testing Facility

iThemba Laboratory for Accelerator Based Sciences, commonly referred to as iThemba LABS is a National Research Facility operated by the National Research Foundation of South Africa. [46] It has a site in Gauteng and another in the Western Cape Province which provide a platform for research in the treatment of cancers, production of radioisotopes and also facilitates some training programs in the fields of sub-atomic physics. [46]

The testing for SEEs in this research was carried out at the Western Cape facility, located about 35km outside Cape Town. It houses one of the largest Separated Sector Cyclotrons (SSC) in the southern hemisphere capable of accelerating protons up to 200MeV. It also includes a 6MeV van de Graff electrostatic accelerator and two injector cyclotrons, one which provides intense beams of light ions and the other provides beams of polarized light ions or heavy ions. [46]

Researchers (and former patients) from various parts of the world make scheduled bookings to use the facility and as such, beam time is stringent. The facility has a medical section, at the former Faure hospital which utilises the main SSC at variable energy levels for radiotherapy treatment. It contains two energy vaults, namely: the proton therapy and neutron therapy units.

The proton vault contains a fixed 200MeV proton beam which was used for treatment of tumours located near critical body organs whereas the neutron vault contains a neutron beam produced as a result of reacting 66MeV protons on Beryllium. The latter was typically used for treatment of larger resistant malignant growths. Although the facility ceased treatment of patients, the equipment still exists (at the time of this writing) and is used for research purposes.

All individuals are required to sign a consent form shown in appendix ‘A’ prior to admission into the radiation areas. While in the radiation vault, each individual is required to wear an electronic personal dosimeter (EPD) which measures the amount of radiation in the room and beeps if dangerous thresholds are reached.

The experimental setup of this study was carried out at the N-Line beam vault shown in figure 31 below.

Figure 31 – N-Line beam vault where the single event effects testing was carried out

During medical treatment, the beam would be directed vertically from the top using strong electro-magnets. However, for the purpose of this test, the beam was redirected so that it would travel horizontally from the exit point.

Maximum proton beam energy of 66 MeV was used because it generally provides a sufficient upset rate. Similar radiation characterisation tests were previously carried out at a maximum energy of 63MeV at the Los Alamos National Laboratory in New Mexico, USA [47]. During the tests, it can be noted that at very low energies between 5-20MeV, the protons did not cause noticeable upsets on the SRAM FPGA under test [47]. Heavy ions on the other hand required higher energy levels in the order of 100 MeV and above to provide sufficient upsets [47].

There are a number of control rooms where the characteristics of the beam are controlled and monitored by the iThemba LABS staff along with the researchers. The main control room is shown in figure 32 whereas the neutron therapy control room in the medical facility is shown in figure 33. Characteristics which are monitored and varied accordingly include: the beam current, time of radiation exposure and energy level. However, the latter was to be kept at a relatively constant energy of 66 MeV since that was the maximum available energy at the N-line therapy vault.

Figure 32 - Main Control room

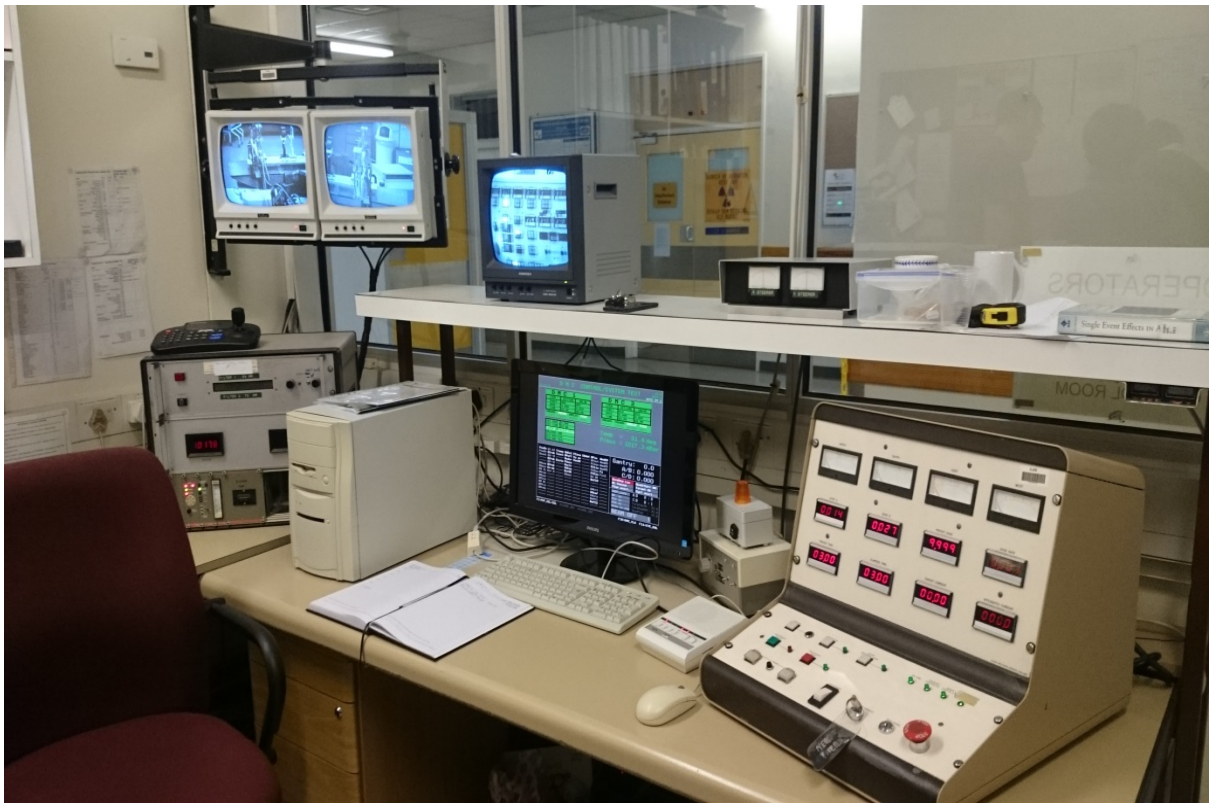

Figure 33 – Neutron Therapy Control room

3.1.4. SEU Detection and Mitigation Test Structure

Upon understanding and selection of the test DUT FPGA device, the testing structure had to be implemented. The challenge in creating a functional and reliable test structure was to ensure a balance between a real hardware design application and maintaining a simple design. This was particularly important because a complex design like a thermal controller would typically be applicable in the space environment but would create the potential of masking errors [48]. Reliable data for event upset cross-section is generally more difficult to obtain in larger complex designs because they contain more input gates which when obstructed by a logic value would prevent another gate's inputs from producing the desired output [17].This phenomenon is referred to as logic masking. It refers to the ability of a logic gate such as AND, OR, NOR or NAND et cetera to continue normal functionality despite an error happening at its inputs [48].

If errors were to be masked in the implemented hardware, then high energy radiation testing would be in vain. Therefore the design's ability to prevent such masking had to be well understood and taken into consideration.

The SEU test structure applied to ensure reliable data (i.e. consistent and sufficient error rates) would be achieved involved implementing three different designs in the DUT. A series of shift registers was used at the user logic instead of a complete design as stated in section 2.10 to prevent logic masking. The first implementation involved no mitigation on the entire design (shown in figure 34), implementation two had the combinational logic mitigated by the SEE filter developed by [40] used in combination with DMR (shown in figure 35) and the last design utilized TMR applied to the entire design, i.e. user logic, clocks and the flip flops (shown in figure 36). The schematic designs for each of the three implementations are shown in the figures below:

Implementation one

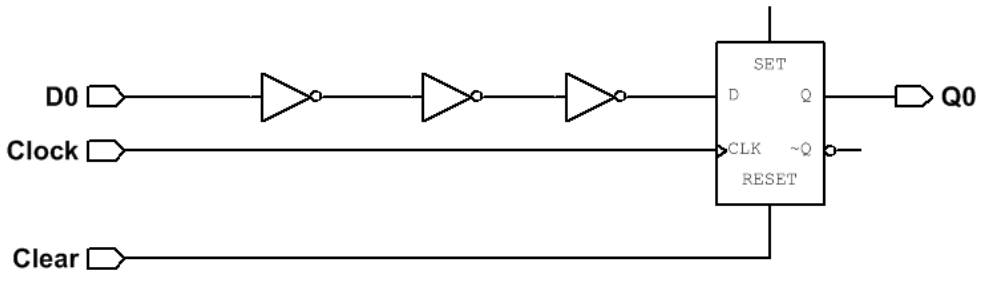

Figure 34 – Implementation one showing the unmitigated design of the serial shift register

Implementation two

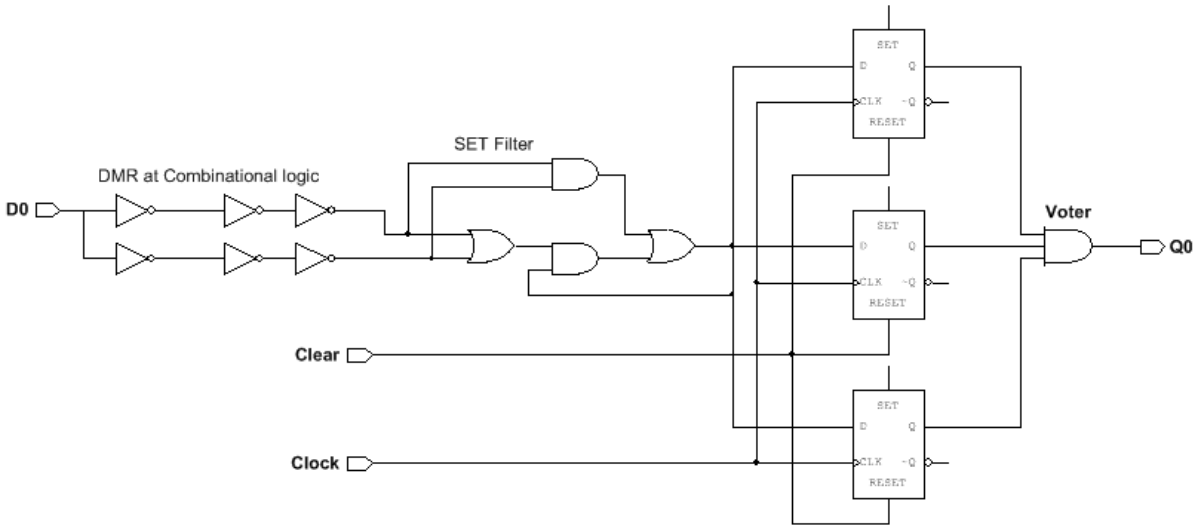

Figure 35 - Implementation two showing the filter and DMR combination

Implementation three

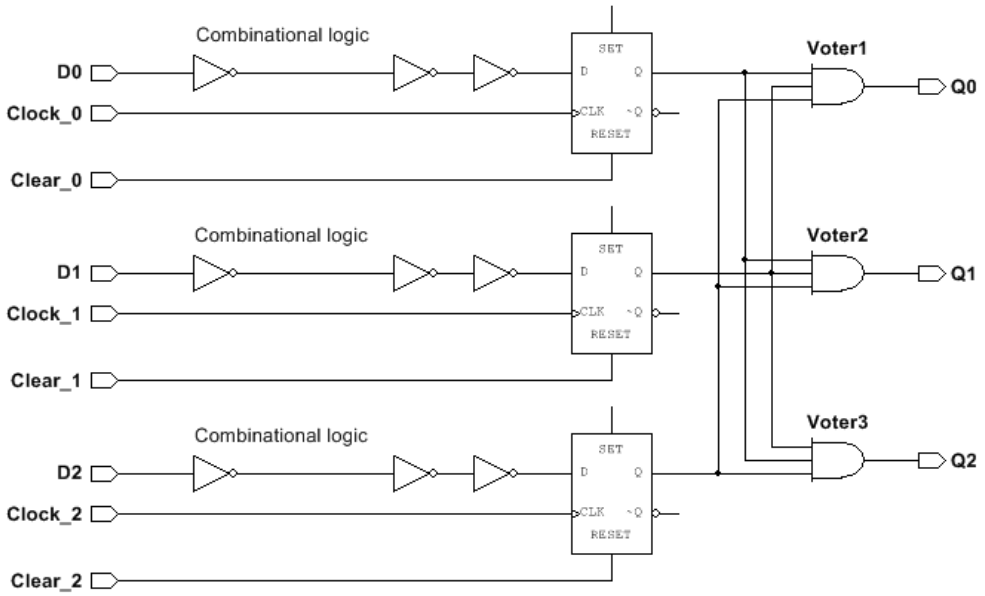

Figure 36 - Implementation three illustrating Full TMR

A program written in C# was used to replicate the three implementations of the serial shift register string by requesting the prompt window shown in figure 37. By doing so, the user is able to utilise more flip flops to fill up the board area as much as possible and increase the probability of a particle hit causing an upset.

A screenshot of the replicated design after synthesis is shown in figure 38 whereas an overall schematic drawing is provided in a separate soft copy.

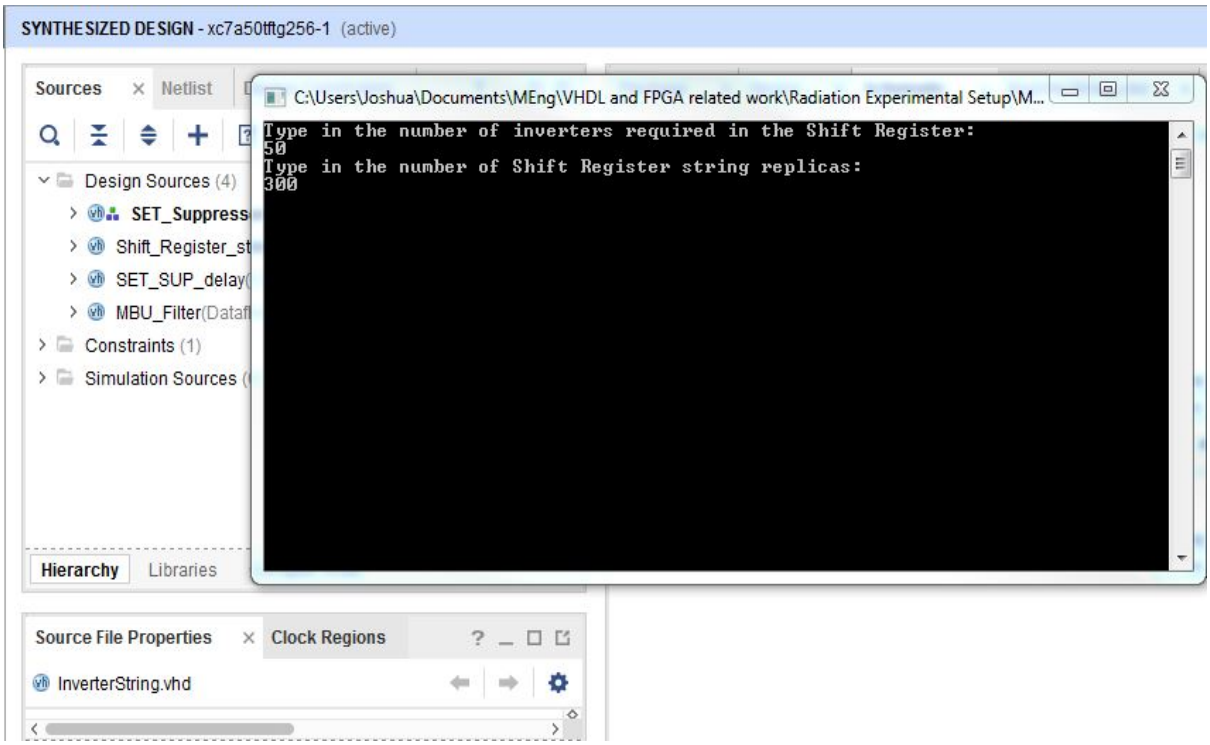

Figure 37 - C# program prompt for replication of the design across the device

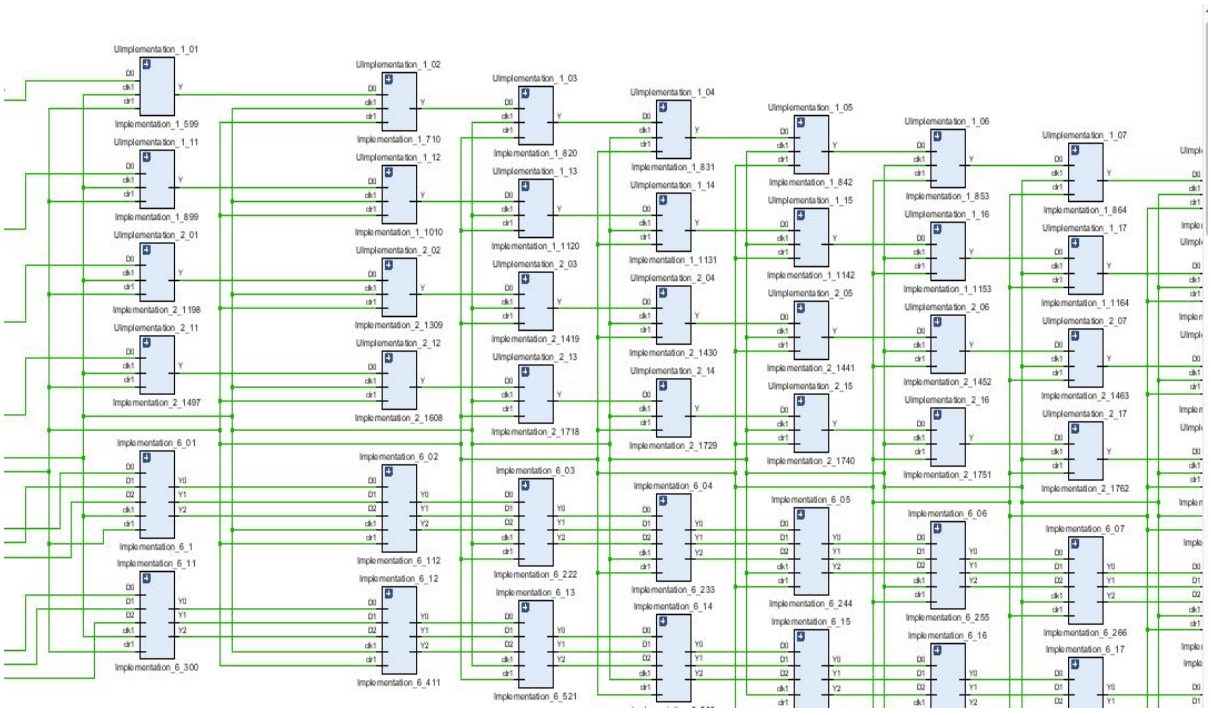

Figure 38 - the screenshot of the resulting replicated design after synthesis

The three separate designs were implemented using VHDL on Xilinx's Integrated Development Environment (IDE) software known as Vivado Design Suite 2017.2 and then mapped onto the Xilinx Artix-7 FPGA core. The board's overall cell usage is shown in table 1. This table shows which elements in the device were utilized as a percentage of the total device area.

Resource	Utilization	Available	Utilization %
LUT	9569	32600	29.35
FF	4194	65200	6.43
IO	26	170	15.29
BUFG	1	32	3.13

Table 1 - Overall cell usage of the DUT

Event effects generally affect the combinational logic and memory area of a device exposed to radiation. Table 2 shows the resource distribution of the Lookup Tables (LUT) and Flip Flops (FF) which were used as primitives during the design of the three implemented circuits.

Resource	**Unmitigated**		**DMR-Filter**		**TMR**		**Total Cell Resources**
LUT	1172	3.595%	2994	9.184%	5403	16.574%	32600
FF	602	0.923%	1790	2.745%	1802	2.764%	65200
Total	1774	1.814%	4784	4.892%	7205	7.367%	97800

Table 2 - DUT resource usage of the three different implementations

Of the 29.35% LUT chip utilization, the three different implementations tested on the DUT occupied the resources as follows:

- Implementation 1 (unmitigated design) – 3.60%
- Implementation 2 (mitigation of the SEE filter and DMR combination) – 9.18%
- Implementation 3 (mitigation of the entire design using TMR) – 16.58%

The flip flops occupied a total of 6.43% of the DUT and were distributed among the three implementations as follows:

- Implementation 1 (unmitigated design) – 0.92%
- Implementation 2 (mitigation of the SEE filter and DMR combination) – 2.75%
- Implementation 3 (mitigation of the entire design using TMR) – 2.76%

An ideal case scenario when testing a device for SEU susceptibility would be to increase the board utilization to a near maximum in order to maximize the possibility that every particle strike on the device is accounted for.

3.1.5. Experimental Test Setup

The test setup was carried out in open air. The first day at iThemba LABs was spent setting up the test equipment and support infrastructure which firstly involved performing infrared alignment of the beam path as seen in the figure 39. It was important to ensure that the particle fluence was maximized by ensuring that the surface of the device under test was perpendicular to the incident proton beam.

Collimators, made of the easily machinable brass, were used to direct the beam into the device's path. They provided good stopping power and were placed at distances which were pre-determined by iThemba LABS during calibration to ensure the beam was evenly scattered across the device. The distance between the beam exit and the device was approximately 3.8m as seen in the test log in Appendix C.

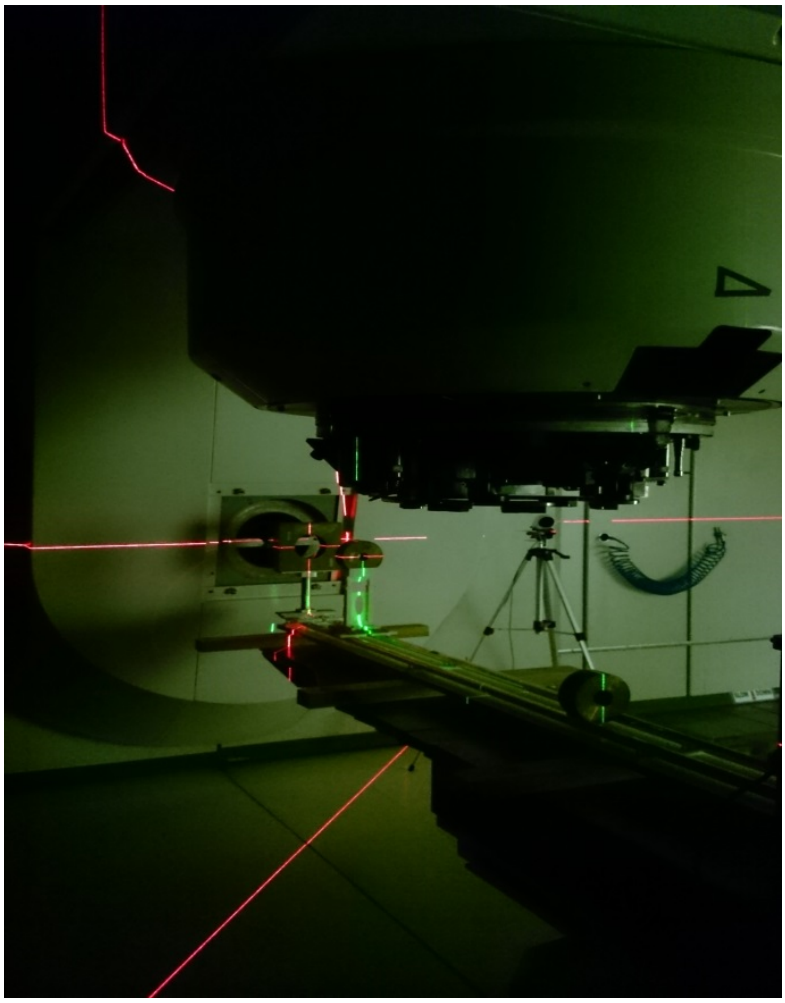

Figure 39 - Infrared alignment of the beam

Two beam loss monitors were used for radiation dosimetry logging which worked on the principle of continuous relative current measurement while there is radiation exposure by the beam. One was placed in direct line of the beam, while another outside the beam. The in-line beam loss monitor was set up to provide the peak current whereas the out-of-line beam acted as a reference.

Along with the current loss monitors, two cameras connected via the network were also set up to provide live footage of the chamber from the control room during radiation testing. This live footage was important for safety purposes in case of an emergency within the chamber. One of the cameras can be seen in figure 42 marked B.

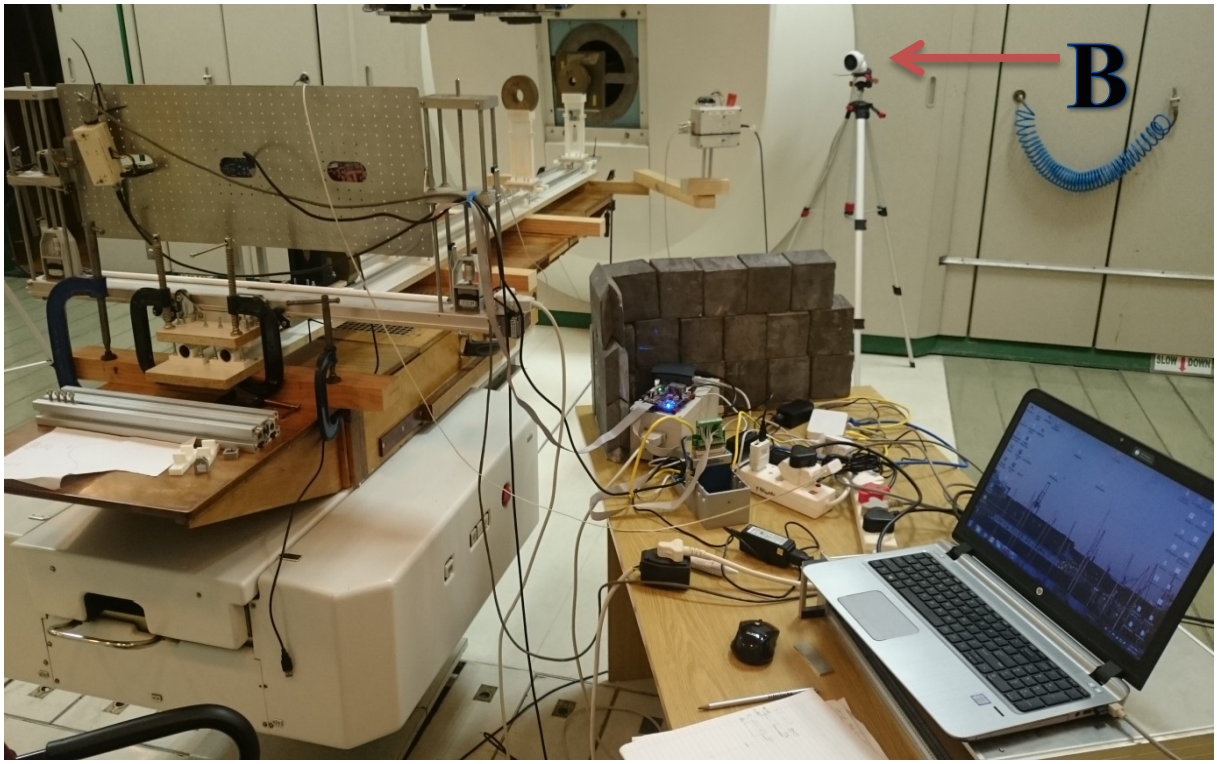

Figure 40 – Test setup showing the SCS built PCB rig and some support infrastructure

Space Commercial Services (SCS) designed a dedicated printed circuit board (PCB) to mount the DUT and aid in its positioning prior to commencing any SEE testing. It was similar to the rig designed by previous students at the Nelson Mandela University (NMU) in that it allowed horizontal and vertical adjustment using two stepper motors and also rotation about the horizontal axis. It was decided that the SCS rig would be used because it was readily available in Cape Town, unlike the NMU multi-board rig which would have to be transported to iThemba LABS.

Along with the learner's device, Mr Arno Barnard, from Stellenbosch University was to carry out tests to characterise a separate device's reliability under radiation on the same rig. Therefore, the beam time was to be shared and it was envisaged that both boards be mounted onto the rig and tests carried out interchangeably. This was done to minimise setup time because the beam was only available for 8 hours on the 18 December, 2017.

The PC running the LABVIEW application for data acquisition was situated in the control room and connected to the NI-DAQ chassis via Ethernet. A top level block diagram of the setup is shown in Figure 41 below:

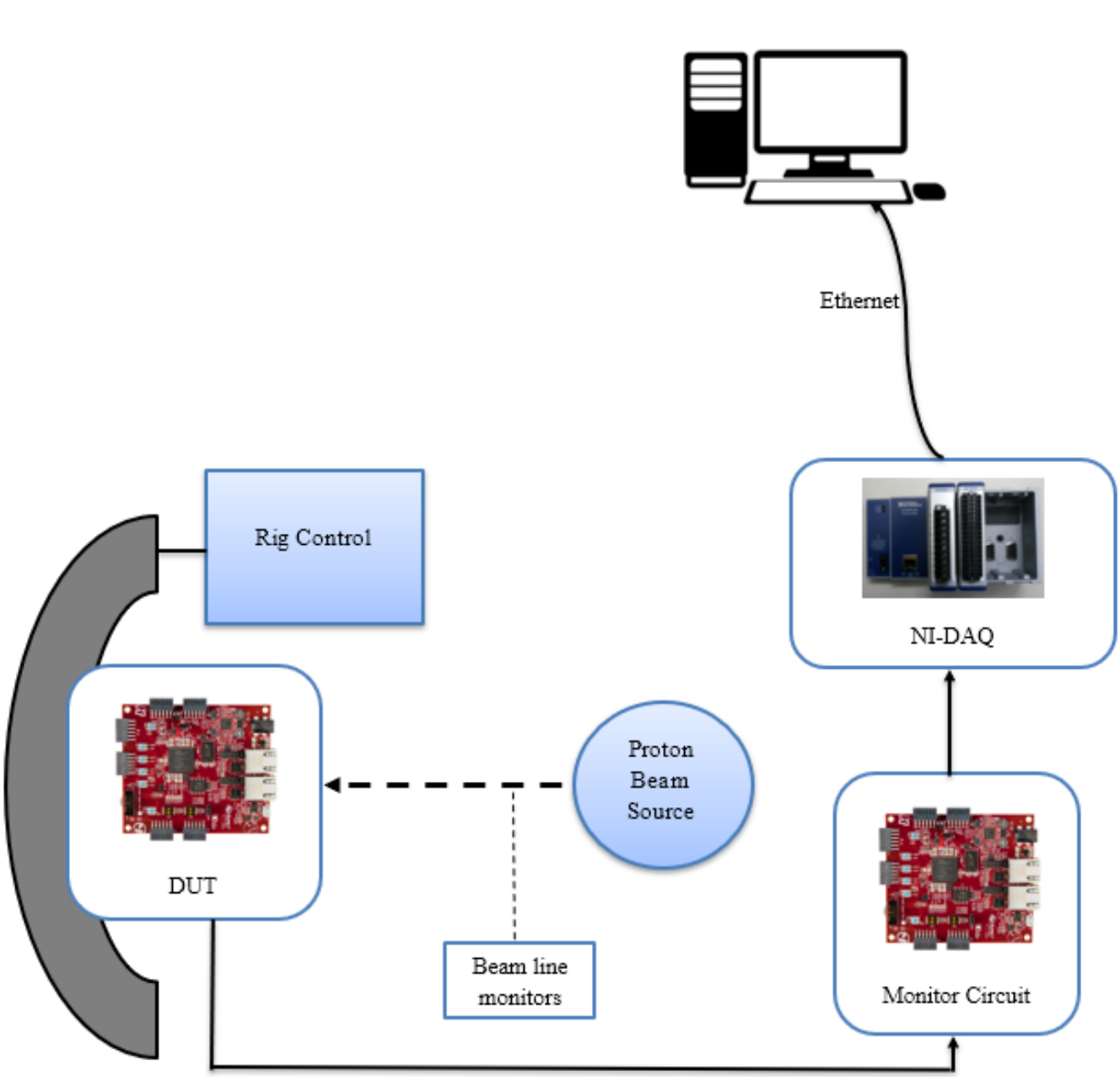

Figure 41 - Experimental test setup

SRIM simulation and Variation of the proton beam

Simulation of the proton beam's energy spectrum was carried out by iThemba LABs using a software package known as Stopping and Range of Ions in Materials (SRIM). It has been widely used by researchers and scientists among others to calculate ion deposition rates and formulate profiles of materials which have been affected by ion interaction. [49]

SRIM is a Monte Carlo technique, similar to its predecessor known as Transport of Ions in Matter (TRIM) which utilises computer programs that have inbuilt algorithms to calculate parameters like: the loss of energy by ionised particles on a device, charge distribution across a device, back scattering and energy transfer among others. [49]These calculated parameters can then be plotted on a 2 or 3 dimensional graph for further analysis.

An example of the generated spectrum developed using SRIM is shown in figure 42. It indicates the number of protons deposited per 200keV for different energy

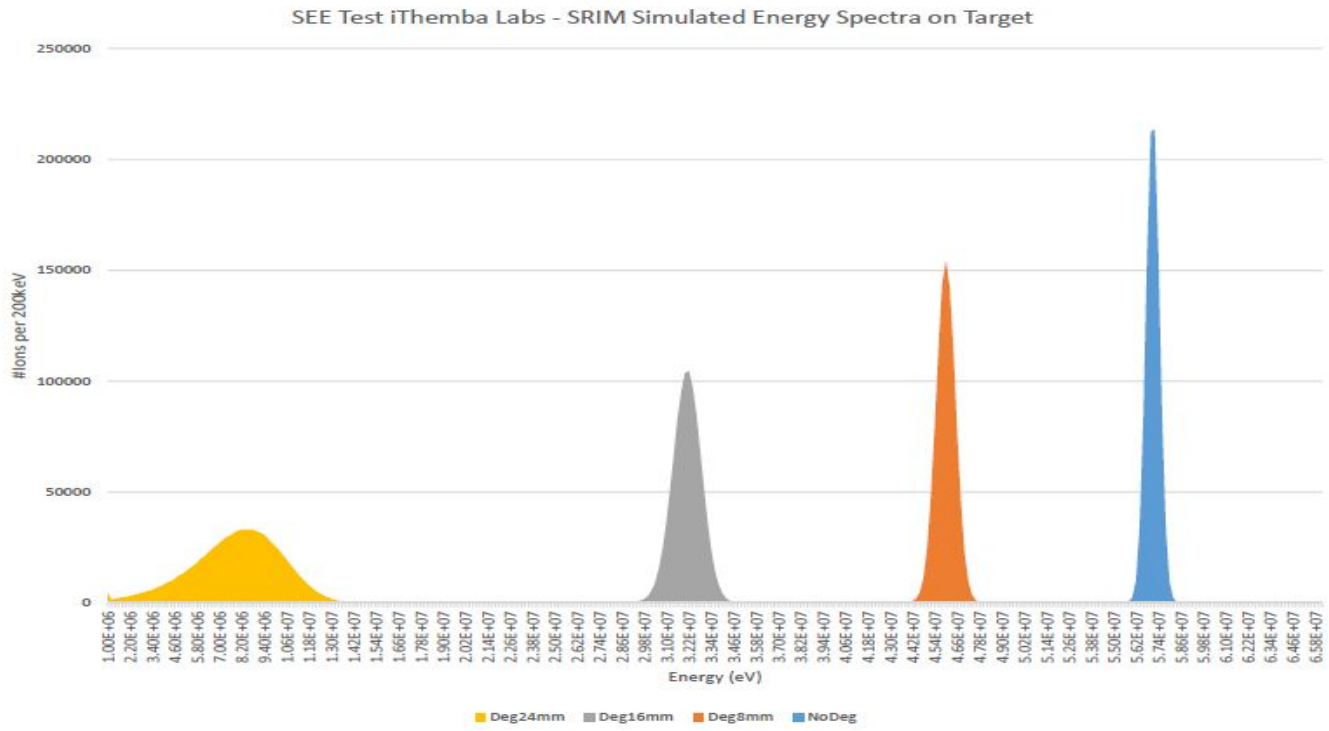

Figure 42 - SRIM simulated energy spectrum on the DUT of varying thickness.

Variation of the testing setup was carried out by manually degrading the beam energy level using Perspex placed in the line beam right ahead of the DUT. Perspex is a trade name for non-shattering acrylic glass which is known to prevent energy scattering and can be used to degrade energy of highly accelerated ions like protons which were used in this study [50]. There were three Perspex plates, each with different thickness (8mm, 16mm and 24mm) to allow a different amount of particles through it while allowing minimum scattering. According to the SRIM simulation at iThemba LABS, no Perspex translated to maximum energy available (i.e. 66MeV). The 8mm thick plate degraded the beam energy to 45.9MeV; 16mm thick plate degraded the energy to 31.969MeV while the 24mm plate degraded the energy to 7.79MeV.

3.1.6. Testing Procedure

Two different devices (one FPGA and another by Mr Arno) were mounted on the PCB rig holder and their testing was to be carried out interchangeably. It is for this reason that the testing procedure at the N-Line therapy vault was altered slightly from previous similar tests carried out by [51] which was at the A-Line therapy vault. The testing procedure was therefore combined to incorporate both devices and generally followed the following steps:

- The device which was to be tested was placed in line of the proton beam and aligned accordingly using the horizontal and vertical motors. It was hoped that this would be carried out remotely from the control room with the assistance of the cameras, but it wasn't the case and was thus done manually inside the radiation chamber. After the positioning was complete, it was required that the vault be evacuated for safety reasons.
- Beam current and the pre-determined time for radiation exposure was determined and entered using the computers within the control room.
- When the vault was deemed safe, the beam was switched on to run with the pre-set parameters (current and exposure time).
- While there was radiation exposure on the device, logging of the number of upsets was done and recorded using the PC running LABVIEW application in the control room until the pre-set time for radiation exposure was reached.
- The beam was then switched off and the vault's radiation was left to diffuse to a level deemed safe for an individual's entry. The time for re-entry into the vault was determined by the iThemba LABS staff EPD and was generally roughly 15 minutes after the end of each test run.
- The other DUT (belonging to Mr Arno Barnard) would then be placed in line with the beam, its radiating parameters set and testing would be carried out, similar to the previous device, until sufficient results are observed from the control room.
- The tests were repeated under similar parameters, for repeatability, until fairly consistent results were obtained.
- When the varying beam current versus time was completed, the setup was altered to allow for testing of the devices under degrading beam energies by placing different thicknesses of Perspex ahead of the device. This followed a similar principle to the previous tests with the difference being that in-between each beam exposure session, the Perspex thickness would physically be changed.
- Upon overall completion of the testing, the devices were left in the N-line chamber for a period of over two weeks to allow the radiation to dissipate. This was a pre-cautionary measure stipulated by iThemba LABs to prevent individuals who worked in their radiation environment from being negatively affected by the radiation. Contact with the devices immediately after radiation could raise the risk of malignant growth among other health complications.

4. CHAPTER 4

This chapter introduces the reader to the proton beam characteristics and the results obtained from experimental testing which was carried out by irradiating protons onto a Xilinx Artix-7 FPGA at the iThemba LABS. The results are then analysed with the objective of ascertaining the effectiveness of the mitigation techniques applied on the DUT.

4.1. Proton beam characterisation

The benchmark beam was without any Perspex degradation and it had a total number of ions transmitted of 999858 at mean peak energy of 56.994MeV. Minimum energy of the beam recorded was 2.352MeV whereas the maximum was 58.76 MeV at a dispersion of 1.868E11eV^2. Number of protons transmitted to the varying centre areas of the device is shown in table 3:

Area (mm²)	Ions	(%) of total ions	per nA	Energy (MeV)
5x5	495	0.04951	3.09E+06	56.994
10x10	2080	0.20803	1.30E+07	56.994
15x15	4584	0.45847	2.86E+07	56.994
20x20	8133	0.81342	5.08E+07	56.994
30x30	18354	1.83566	1.15E+08	56.994

Table 3 - number of ions transmitted for varying device centre areas without degradation

Variation of the beam was later introduced by degrading its energy using Perspex of a different thickness. The first variation utilised a plate thickness of 8mm and the beam transmitted a total number of ions of 999758 at mean peak energy of 45.875MeV. Table 4 below shows the varying number of ions and the charge per unit of current (nA) which collided with the device at different centre areas:

Area (mm²)	Ions	(%) of total ions	per nA	Energy (MeV)
5x5	537	0.05371	3.35E+06	45.875
10x10	2013	0.20135	1.26E+07	45.875
15x15	4564	0.45651	2.85E+07	45.875
20x20	8125	0.81270	5.07E+07	45.875
30x30	17954	1.79583	1.12E+08	45.875

Table 4 - number of ions transmitted at Perspex thickness of 8mm

The second variation of the proton beam was carried out using a thicker Perspex plate of 16mm. It transmitted a total of 999324 ions at a maximum energy of 31.969MeV. The number of ions deposited across varied centre areas on the DUT and the charge per nA of current is shown in table 5.

Area (mm²)	Ions	(%) of total ions	per nA	Energy (MeV)
5x5	499	0.04993	3.12E+06	31.969
10x10	2022	0.20234	1.26E+07	31.969
15x15	4585	0.45881	2.86E+07	31.969
20x20	8051	0.80564	5.03E+07	31.969
30x30	17870	1.78821	1.12E+08	31.969

Table 5 - number of ions transmitted at Perspex thickness of 16mm

The final variation of the beam was carried out by degrading the energy using the thickest available Perspex plate of 24mm and it allowed a total number of 957455 ions to be deposited onto the device at mean peak energy of 7.79MeV. Table 6 below shows the actual number of ions which were deposited over varying areas on the device. It also shows the ions deposited for every unit of current (nA) across the varying device centre areas.

Area (mm²)	Ions	(%) of total ions	per nA	Energy (MeV)
5x5	435	0.04543	2.84E+06	7.79
10x10	1867	0.19500	1.22E+07	7.79
15x15	4237	0.44253	2.76E+07	7.79
20x20	7448	0.77790	4.86E+07	7.79
30x30	16668	1.74087	1.09E+08	7.79

Table 6 - number of ions transmitted at Perspex thickness of 24mm

The radius of the beam for both the benchmark and degraded tests was kept constant by the iThemba LABs staff at 1cm² whereas the length and width of the device over which radiation was incident (centre die) was 1.5cm respectively. Since the beam was generally circular, its cross section area was calculated using equation 7 as follows:

Beam area, $A_{beam} = \pi r^2$, where r is in cm

Equation 7 - cross sectional area of the beam

Therefore, beam area, $A_{beam} = \pi (1)^2$

$= 3.142$ cm²

After testing was completed and radiation on the board (and in the chamber) had dissipated, the device was decapsulated as seen in figure 43 in order to obtain its centre die area using equation 8 as follows:

Centre die area, A_{die} = length x width

Equation 8 - centre die area

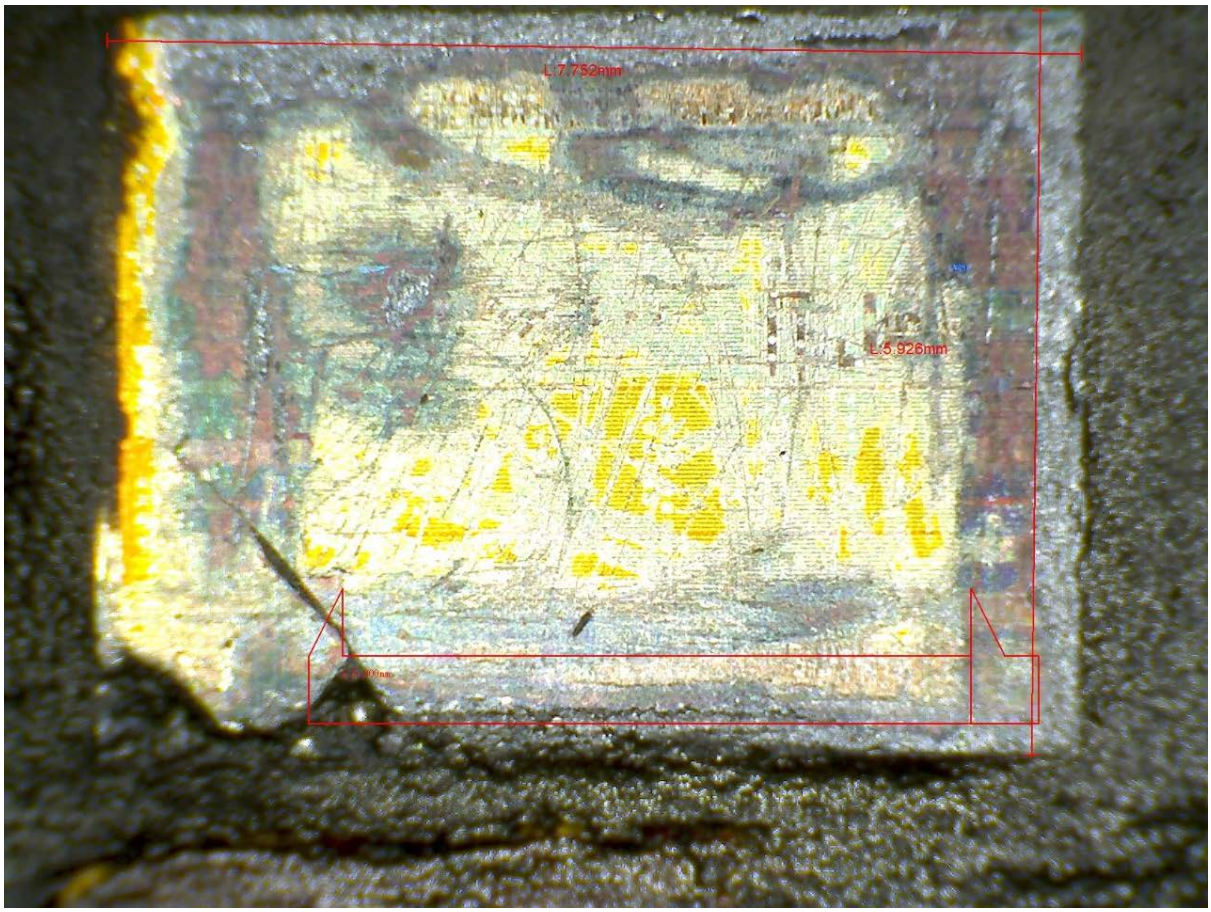

Figure 43 - Decapsulated device to obtain the die area

Therefore, centre die area, A_{die} = 0.7752 x 0.5926 cm²

=0.459cm²

From this information, it was possible to calculate the number of particles which hit the device using equation 9 below:

$$\text{Number of particles hitting DUT} = \frac{A_{die}}{A_{beam}} \text{ x Total proton ions}$$

Equation 9 - number of particles hitting the device

Where the total proton ions was established from equation 10 below:

Total proton ions = coulomb x beam current x time

Equation 10 - total proton ions

Chapter 2 introduced the concept of a cross section which is an important parameter for characterisation of SEU susceptibility in microelectronic devices which are exposed to radiation. Two parameters need to be established: linear energy transfer and the device cross section per bit. The latter is a ratio of the number of upsets counted to the particle fluence.

The upset count is introduced in subsection 4.2 for the different tests which were carried out, whereas the particle fluence is obtained after establishing the number of protons which hit the DUT using equation 9. Particle fluence is dependent on the device area which in this case is the total combinational logic (sum of the look up tables and the flip flops) in each implementation as a percentage of the overall device resources. Table 2 in chapter 3 showed the device area for the three implemented designs and it can be summed as follows:

$$\text{Device area} = \frac{\text{total combinational logic}}{\text{total cell resources}} \text{x} 100\%$$

$$\text{Device area}_{(\text{unmitigated})} = \frac{1774}{97800} \text{x} 100\%$$

$$= 1.814\%$$

$$\text{Device area}_{(\text{Filter and DMR})} = \frac{4784}{97800} \text{x} 100\%$$

$$= 4.892\%$$

$$\text{Device area}_{(\text{Global TMR})} = \frac{7205}{97800} \text{x} 100\%$$

$$= 7.367\%$$

From this information, the proton particle fluence is calculated by using equation 11 shown below for each implementation:

$$\text{Fluence} = \text{ions per given area x device area}$$

Equation 11 - Proton particle fluence

4.2. Results

4.2.1. Benchmark beam

First test run

Using the benchmark beam (no degradation), the first test run was carried out for 3 minutes and the current was set to 5nA after which the number of upsets recorded during each cycle for the three implementations was recorded in table 7 below:

	Errors Counted	Time(s)	Current(A)
Unmitigated	50	180	5.00E-09
DMR with SEE filter	27	180	5.00E-09
TMR	25	180	5.00E-09

Table 7 - number of upsets counted after radiation exposure of 5 minutes

	Total Ions	Particles hitting	Device Area	Fluence
Unmitigated	5.62E+12	8.20E+11	1.814%	14881295795
DMR with SEE filter	5.62E+12	8.20E+11	4.892%	40130845030
TMR	5.62E+12	8.20E+11	7.367%	6.04E+10

Table 8 - Fluence of the first test run using the benchmark beam

From the information in tables 7 and 8, the cross section area of the device and consequently the cross section area per bit for implementation one (unmitigated design) at 5nA was calculated as follows

$$\sigma_{device} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{device} = \frac{50}{14881295795}$$

$$\sigma_{device} = 3.35992\text{x}10^{-9}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{device}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.35992\text{x}10^{-9}}{602}$$

$$\sigma_{\text{per bit}} = 5.581\text{x}10^{-12}\ \text{cm}^2/\text{bit}$$

The cross section and consequently the cross section per bit for implementation two (mitigated design using a combination of SEE filter and DMR) at 5nA for 3 minutes was calculated as follows

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{27}{40130845030}$$

$$\sigma_{\text{device}} = 6.72799\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{6.72799\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 3.759x10^{-13}\ \text{cm}^2/\text{bit}$$

Similarly, the cross section and the cross section per bit for implementation three (full TMR across the entire circuit, including the clock and reset signals) at 5nA and run for 3 minutes was calculated as shown.

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{25}{6.04x10^{10}}$$

$$\sigma_{\text{device}} = 4.1364\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{4.1364\text{x}10^{-10}}{1802}$$

$$\sigma_{\text{per bit}} = 2.295x10^{-13}\ \text{cm}^2/\text{bit}$$

Table 9 shows the calculated cross section based on the experimental data for the three different design implementations and the Bendel-1 ‘A’ parameters ascertained.

	$\sigma_{\text{per bit}}$	**A at 56MeV (5nA)**
Unmitigated	$5.581x10^{-12}$	18.9
DMR with SEE filter	$3.759x10^{-13}$	22.57
TMR	$2.295x10^{-13}$	23.3

Table 9 - Cross section and Bendel-1 ‘A’ parameters at 56MeV (5nA)

Using the information above, the cross section area versus proton energy graph is formulated using the Bendel-1 function and it is shown in figure 44 below. Figure 45 shows the cross section as a function of proton energy for the DMR and global TMR designs.

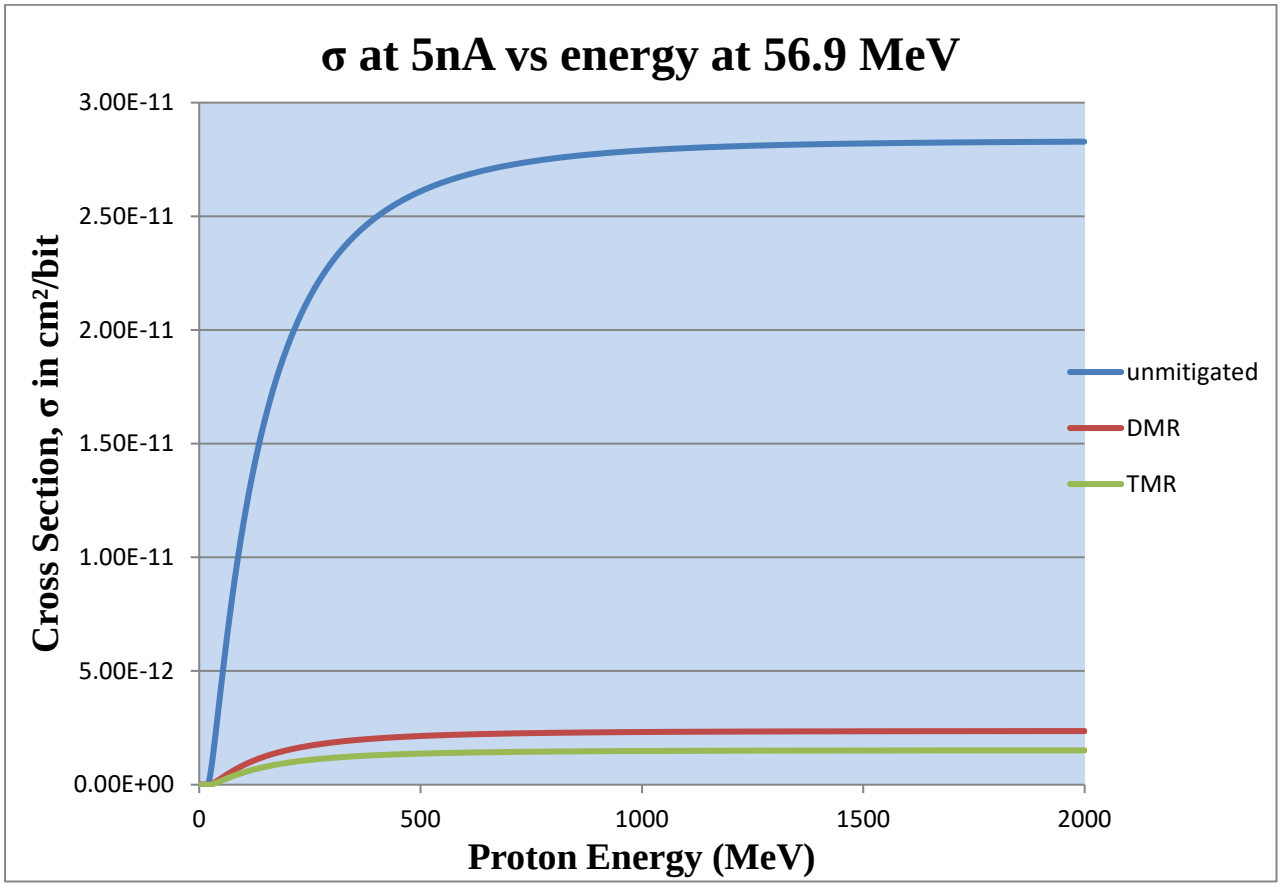

Figure 44 - Cross Section as a function of proton energy for the first test run using the benchmark beam

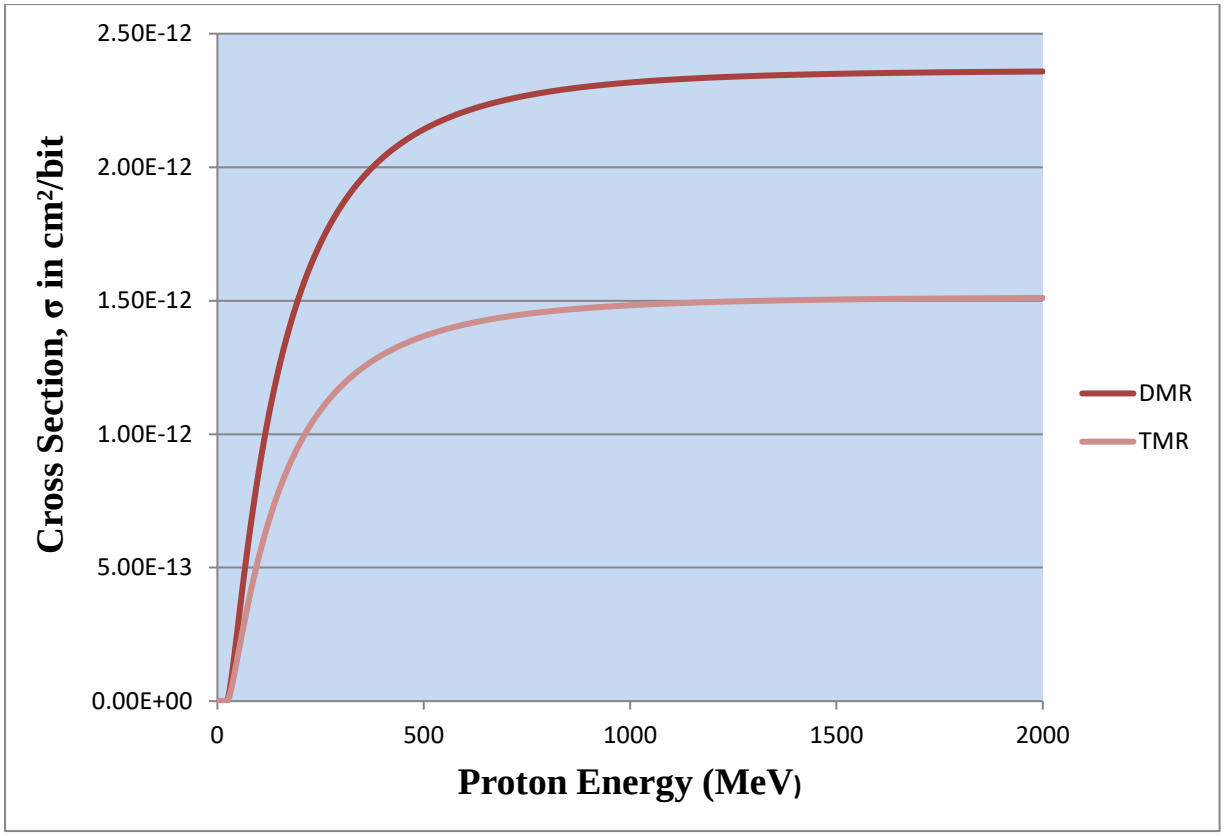

Figure 45 - Cross Section as a function of proton energy of DMR and global TMR designs

Second test run

The second test run was also carried out using the benchmark beam (mean peak energy of 56.994MeV) for 3 minutes at an increased current of 10nA after which the number of upsets was counted across each of the three implementations and shown in table 10 below.

	Errors Counted	Time(s)	Current(A)
Unmitigated	103	180	1.00E-08
DMR with SEE filter	46	180	1.00E-08
TMR	28	180	1.00E-08

Table 10 - number of upsets counted during the 2nd test run at 10Na

	Total Ions	Particles hitting	Device Area	Fluence
Unmitigated	1.12E+13	1.64E+12	1.814%	2.98E+10
DMR with SEE filter	1.12E+13	1.64E+12	4.892%	8.03E+10
TMR	1.12E+13	1.64E+12	7.367%	1.21E+11

Table 11 - Fluence of the second test run using the benchmark beam

The cross section and the cross section per bit for implementation one (unmitigated design) at 10nA was calculated as follows using the fluence information from table 11 and the beam characteristics.

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{103}{2.98x10^{10}}$$

$$\sigma_{\text{device}} = 3.4607\text{x}10^{-9}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.4607\text{x}10^{-9}}{602}$$

$$\sigma_{\text{per bit}} = 5.749x10^{-12}\ \text{cm}^2/\text{bit}$$

The cross section and cross section per bit for implementation two (mitigated design using a combination of SEE filter and DMR) at 10nA for 3 minutes was calculated as follows

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{46}{8.03x10^{10}}$$

$$\sigma_{\text{device}} = 5.73125\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{5.73125\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 3.202x10^{-13}\ \text{cm}^2/\text{bit}$$

Similarly, the cross section and cross section per bit for implementation three (full TMR across the entire circuit, including the clock and reset signals) at 10nA and run for 3 minutes was calculated as shown.

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{28}{1.21x10^{11}}$$

$$\sigma_{\text{device}} = 2.31636\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{2.31636\text{x}10^{-10}}{1802}$$

$$\sigma_{\text{per bit}} = 1.285x10^{-13}\ \text{cm}^2/\text{bit}$$

Table 12 shows the calculated cross section based on the experimental data for the three different design implementations and the Bendel-1 ‘A’ parameters ascertained.

	$\sigma_{\text{per bit}}$	**A at 56MeV (10nA)**
Unmitigated	$5.749x10^{-12}$	18.865
DMR with SEE filter	$3.202x10^{-13}$	22.81
TMR	$1.285x10^{-13}$	24.2

Table 12 - Cross section and Bendel-1 ‘A’ parameters at 56MeV (10nA)

Using the information above, the cross section versus proton energy graph is formulated using the Bendel-1 function and it is shown in figure 46 below. Figure 47 shows the cross section as a function of proton energy for the DMR and global TMR designs.

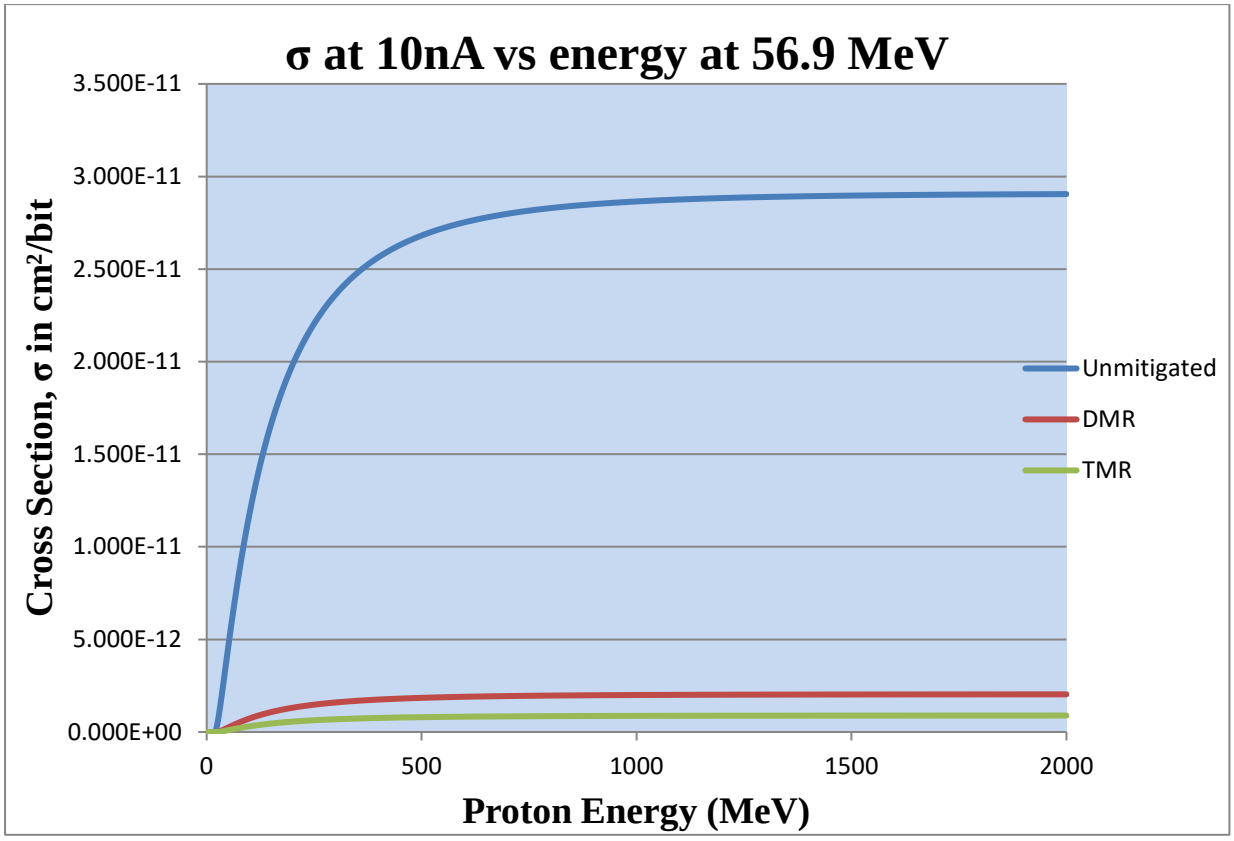

Figure 46 - Cross section as a function of proton energy for the 2nd test run using the benchmark beam

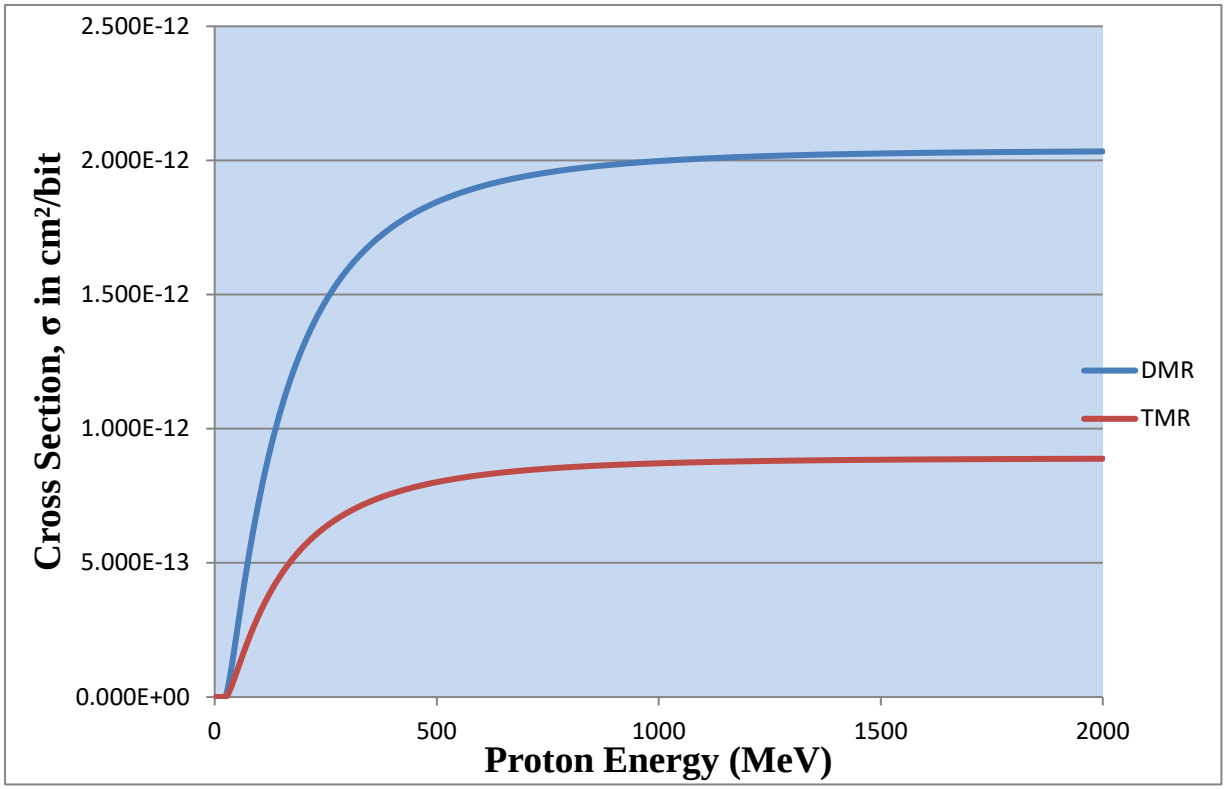

Figure 47 - Cross section versus proton energy of the DMR and global TMR designs

4.2.2. Degraded beam

The next set of testing was carried out using the same proton beam but this time its energy was degraded by placing Perspex plates of varying thickness in the beam path ahead of the DUT. It involved three separate tests which were each carried out for 3 minutes at a uniform current of 10nA. The first test utilised a plate of 8mm thickness, the second used 16mm while the third used 24mm. For each test, the number of upsets were counted and logged in each of the three hardware designs running on the DUT. This subsection introduces the reader to the results obtained in these test runs.

Degradation using 8mm Perspex

The first degraded beam utilised an 8mm plate of Perspex, which translated to approximate proton energy of 45.875MeV. The number of upsets was counted across each of the three implementations and the respective fluence calculated as shown in tables 13 and 14 respectively.

	Errors Counted	**Time(s)**	**Current(A)**
Unmitigated	98	180	1.00E-08
DMR with SEE filter	50	180	1.00E-08
TMR	39	180	1.00E-08

Table 13 - Number of errors counted when beam was degraded to 45.875MeV

	Total Ions	**Particles hitting**	**Device Area**	**Fluence**
Unmitigated	1.12E+13	1.64E+12	1.814%	2.98E+10
DMR with SEE filter	1.12E+13	1.64E+12	4.892%	8.03E+10
TMR	1.12E+13	1.64E+12	7.367%	1.21E+11

Table 14 - Fluence when proton beam was degraded to 45.875MeV

Cross section area and cross section per bit of the three designs was then calculated as follows using the information from tables 13 and 14:

Unmitigated design

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{98}{2.98x10^{10}}$$

$$\sigma_{\text{device}} = 3.29\text{x}10^{-9}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.29\text{x}10^{-9}}{602}$$

$$\sigma_{\text{per bit}} = 5.47x10^{-12}\ \text{cm}^2/\text{bit}$$

DMR and filter combination

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{50}{8.03x10^{10}}$$

$$\sigma_{\text{device}} = 6.23\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{6.23\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 3.48x10^{-13}\ \text{cm}^2/\text{bit}$$

Full global TMR

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{39}{1.21x10^{11}}$$

$$\sigma_{\text{device}} = 3.23\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.23\text{x}10^{-10}}{1802}$$

$$\sigma_{\text{per bit}} = 1.79x10^{-13}\ \text{cm}^2/\text{bit}$$

The Bendel-1 function was used and table 15 below shows the estimated A fitting parameters which were obtained and used for the cross section versus proton energy graph.

	$\sigma_{per\ bit}$	A at 45.87MeV (10nA)
Unmitigated	$5.47x10^{-12}$	18.39
DMR with SEE filter	$3.48x10^{-13}$	22.01
TMR	$1.79x10^{-13}$	22.95

Table 15 – Bendel-1 'A' parameters when the beam was degraded using 8mm Perspex

The cross section versus proton energy graph is formulated using the Bendel-1 function and it is shown in figure 48 below whereas figure 49 shows the detailed cross section as a function of proton energy for the DMR and global TMR designs.

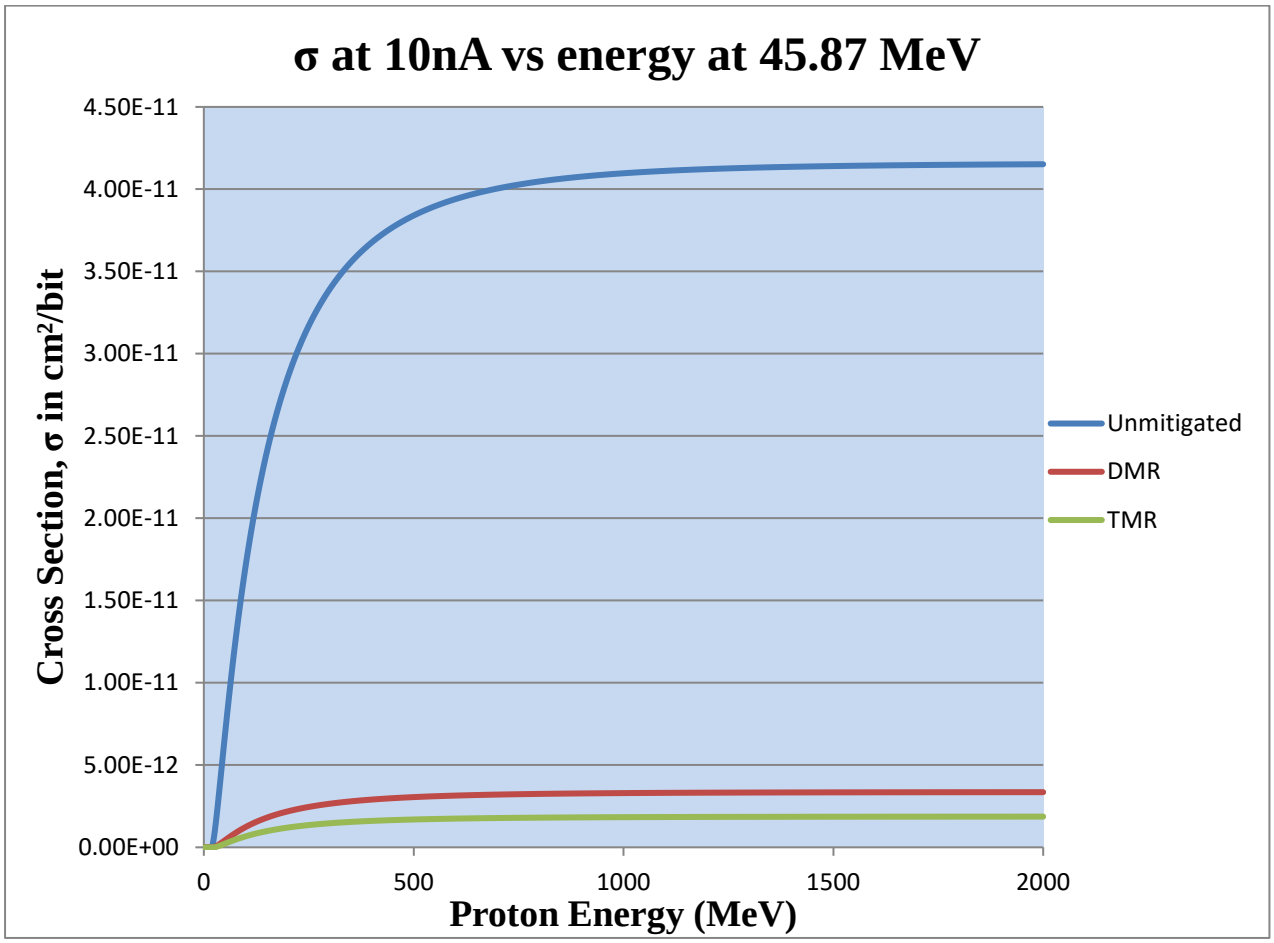

Figure 48 - Cross section as a function of proton energy when the beam was degraded using 8mm Perspex

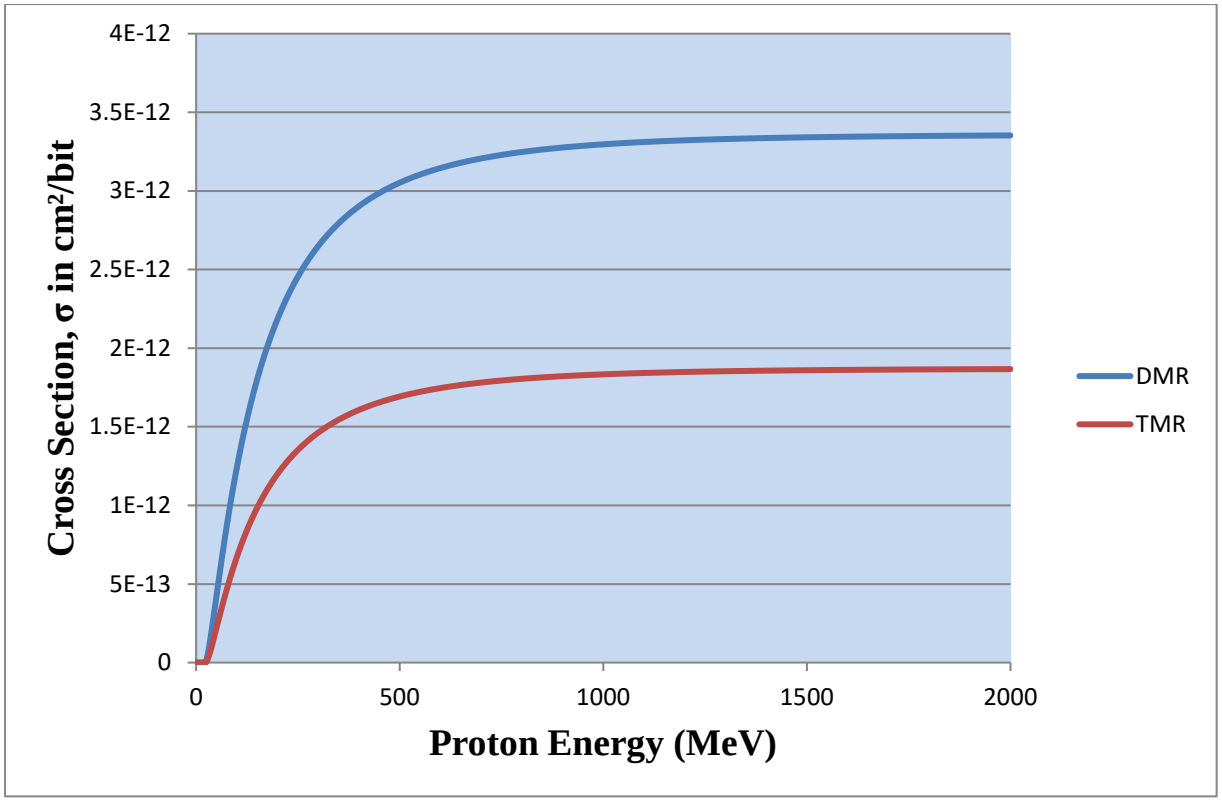

Figure 49 - Cross section versus proton energy of the DMR and global TMR designs when the beam was degraded using 8mm Perspex

Degradation using 16mm Perspex

The second degraded beam utilised a 16mm plate of Perspex which translated to approximate proton energy of 31.969MeV. The number of upsets was counted across each of the three implementations and the respective fluence calculated as shown in tables 16 and 17 respectively.

	Errors Counted	Time(s)	Current(A)
Unmitigated	90	180	1.00E-08
DMR with SEE filter	31	180	1.00E-08
TMR	28	180	1.00E-08

Table 16 - Number of errors counted when beam was degraded to 31.969MeV

	Total Ions	Particles hitting	Device Area	Fluence
Unmitigated	1.12E+13	1.64E+12	1.814%	2.98E+10
DMR with SEE filter	1.12E+13	1.64E+12	4.892%	8.03E+10
TMR	1.12E+13	1.64E+12	7.367%	1.21E+11

Table 17 - Fluence when proton beam was degraded to 31.969MeV

Cross section area and cross section per bit of the three designs was then calculated as follows using the information from tables 16 and 17:

Unmitigated design

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{90}{2.98x10^{10}}$$

$$\sigma_{\text{device}} = 3.02\text{x}10^{-9}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.02\text{x}10^{-9}}{602}$$

$$\sigma_{\text{per bit}} = 5.02x10^{-12}\ \text{cm}^2/\text{bit}$$

DMR and filter combination

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{31}{8.03x10^{10}}$$

$$\sigma_{\text{device}} = 3.86\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{3.86\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 2.16x10^{-13}\ \text{cm}^2/\text{bit}$$

Full global TMR

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{28}{1.21x10^{11}}$$

$$\sigma_{\text{device}} = 2.32\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{2.32\text{x}10^{-10}}{1802}$$

$$\sigma_{\text{per bit}} = 1.29x10^{-13}\ \text{cm}^2/\text{bit}$$

The Bendel-1 function was also used and table 18 below shows the estimated 'A' fitting parameters which were obtained and used for the cross section versus proton energy graph.

	$\boldsymbol{\sigma_{\text{per bit}}}$	**A at 31.97MeV (10nA)**
Unmitigated	$5.02x10^{-12}$	17.53
DMR with SEE filter	$2.16x10^{-13}$	21.11
TMR	$1.29x10^{-13}$	21.73

Table 18 - Bendel-1 'A' parameters for the three designs when using 16mm Perspex

Using the information in table 18, the cross section per bit as a function of energy was plotted in figure 50. Detailed graph data is shown for the DMR-filter combination and global TMR designs in figure 51.

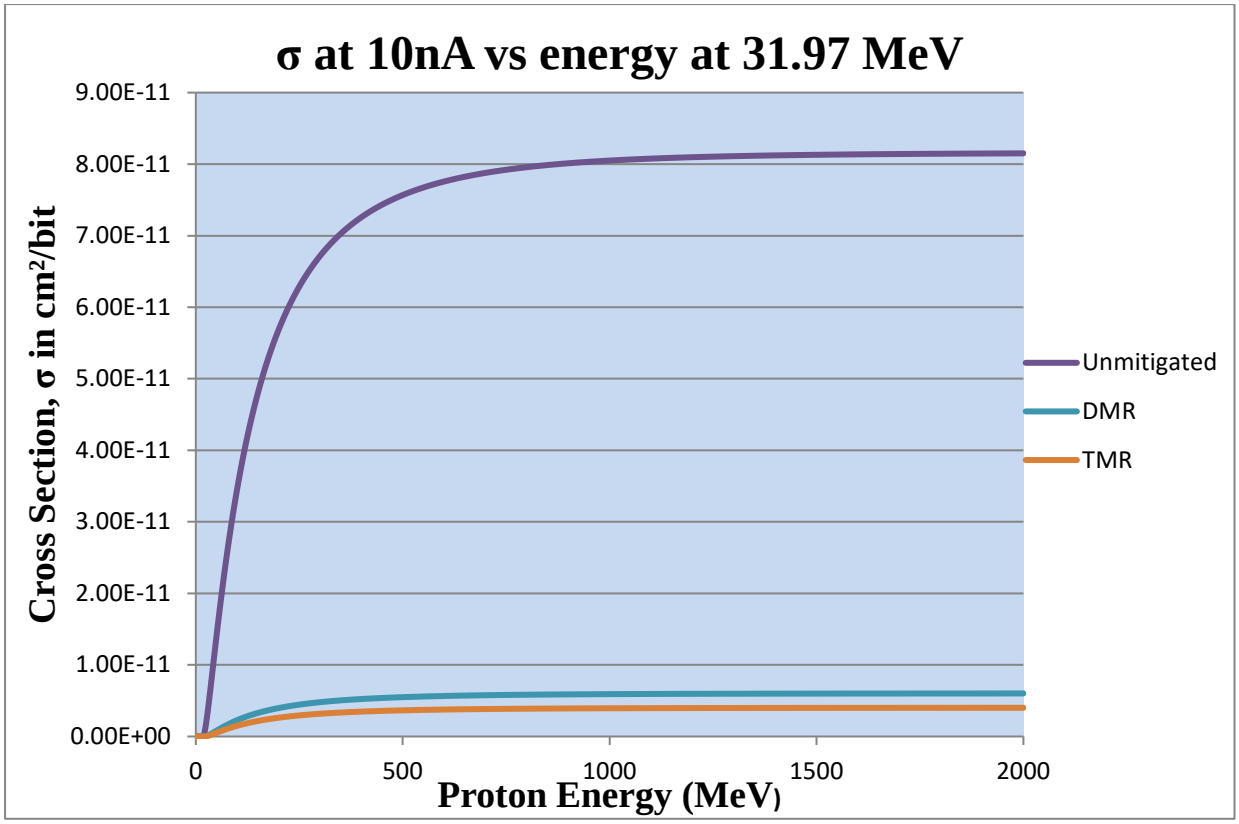

Figure 50 - Cross section as a function of proton energy when the beam was degraded using 16mm Perspex

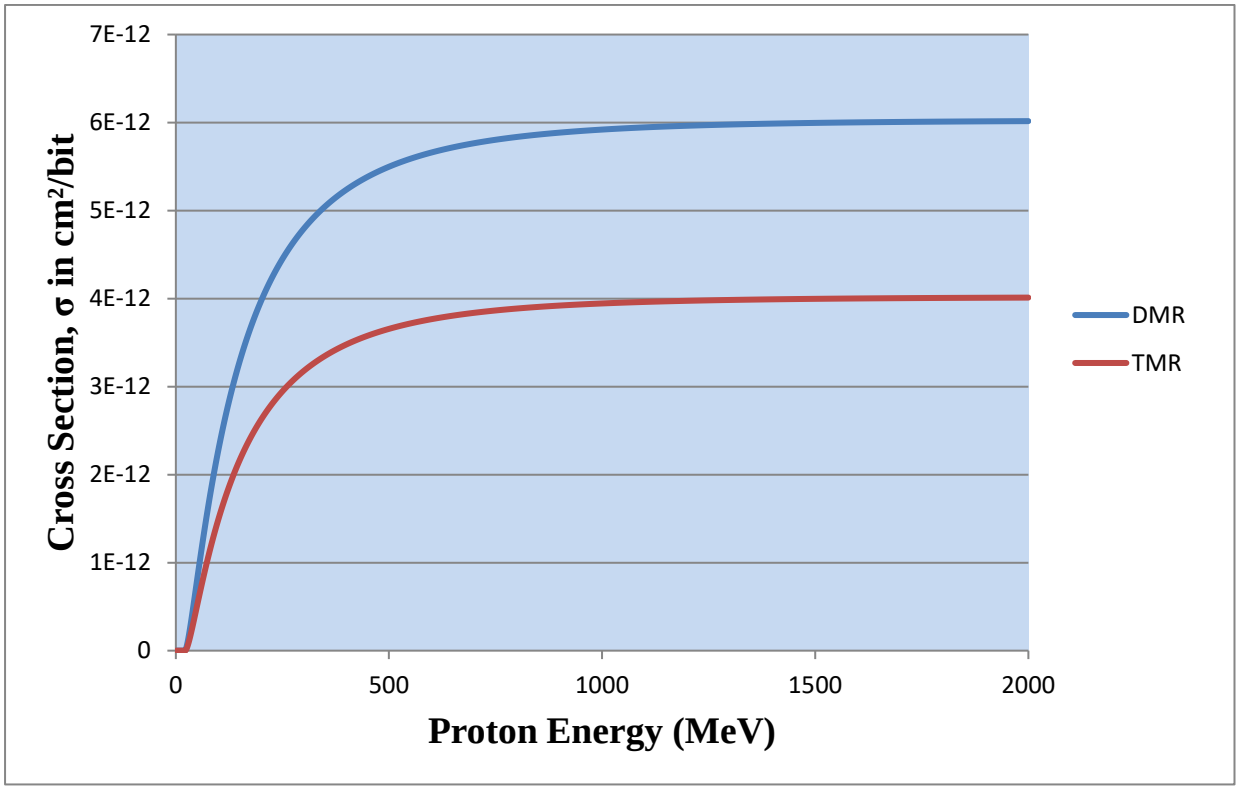

Figure 51 - Cross section versus proton energy of the DMR and global TMR designs when the beam was degraded using 16mm Perspex

Degradation using 24mm Perspex

The third degraded beam utilised a 24mm plate of Perspex which translated to approximate proton energy of 7.79MeV. From this test run, the number of errors was counted and then each implementation's fluence calculated as seen in tables 19 and 20 respectively.

	Errors Counted	Time(s)	Current(A)
Unmitigated	85	180	1.00E-08
DMR with SEE filter	21	180	1.00E-08
TMR	20	180	1.00E-08

Table 19 - Number of errors counted when proton beam was degraded to 7.79MeV

	Total Ions	Particles hitting	Device Area	Fluence
Unmitigated	1.12E+13	1.64E+12	1.814%	2.98E+10
DMR with SEE filter	1.12E+13	1.64E+12	4.892%	8.03E+10
TMR	1.12E+13	1.64E+12	7.367%	1.21E+11

Table 20 – Proton fluence for the three designs when the beam was degraded to 7.79MeV

Using the information from tables 19 and 20, the cross section area and cross section per bit of each design was then calculated as follows:

Unmitigated design

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{85}{2.98x10^{10}}$$

$$\sigma_{\text{device}} = 2.86\text{x}10^{-9}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{2.86\text{x}10^{-9}}{602}$$

$$\sigma_{\text{per bit}} = 4.74x10^{-12}\ \text{cm}^2/\text{bit}$$

DMR and filter combination

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{21}{8.03x10^{10}}$$

$$\sigma_{\text{device}} = 2.62\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{2.62\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 1.46x10^{-13}\ \text{cm}^2/\text{bit}$$

Full global TMR

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{20}{1.21x10^{11}}$$

$$\sigma_{\text{device}} = 1.65\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{1.65\text{x}10^{-10}}{1802}$$

$$\sigma_{\text{per bit}} = 9.18x10^{-14}\ \text{cm}^2/\text{bit}$$

The Bendel-1 function was also used and table 21 below shows the estimated 'A' fitting parameters which were obtained and used for the cross section versus proton energy graph.

	$\sigma_{per\ bit}$	A at 7.79MeV (10nA)
Unmitigated	$4.74x10^{-12}$	7.979
DMR with SEE filter	$1.46x10^{-13}$	7.996
TMR	$9.18x10^{-14}$	7.997

Table 21 - Bendel-1 'A' parameters when the beam was degraded using 24mm Perspex

The cross section versus proton energy graph is drawn using the Bendel-1 function and it is shown in figure 52 below whereas figure 53 shows the detailed cross section as a function of proton energy for the DMR and global TMR designs.

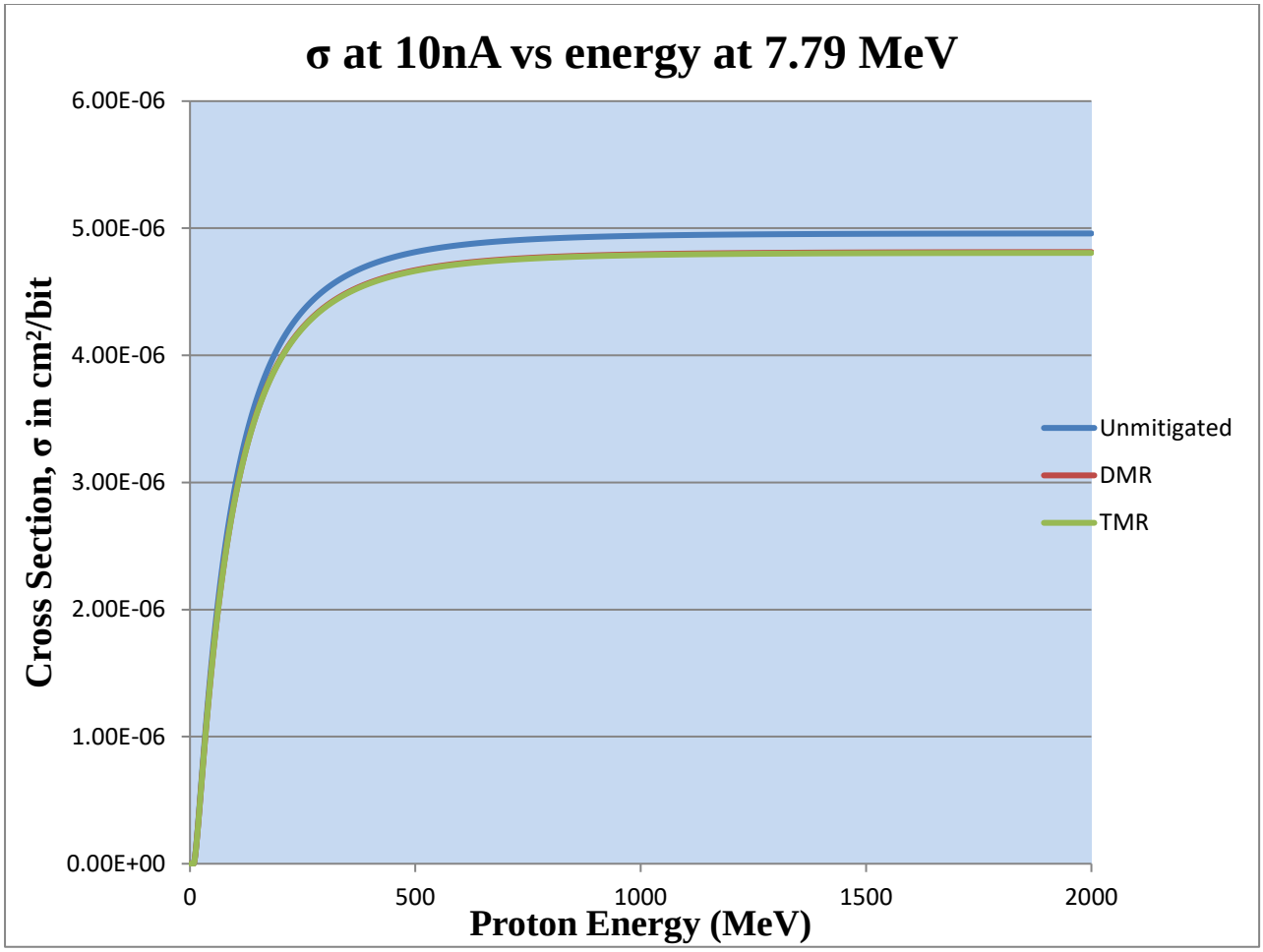

Figure 52 - Cross section as a function of proton energy when the beam was degraded using 24mm Perspex

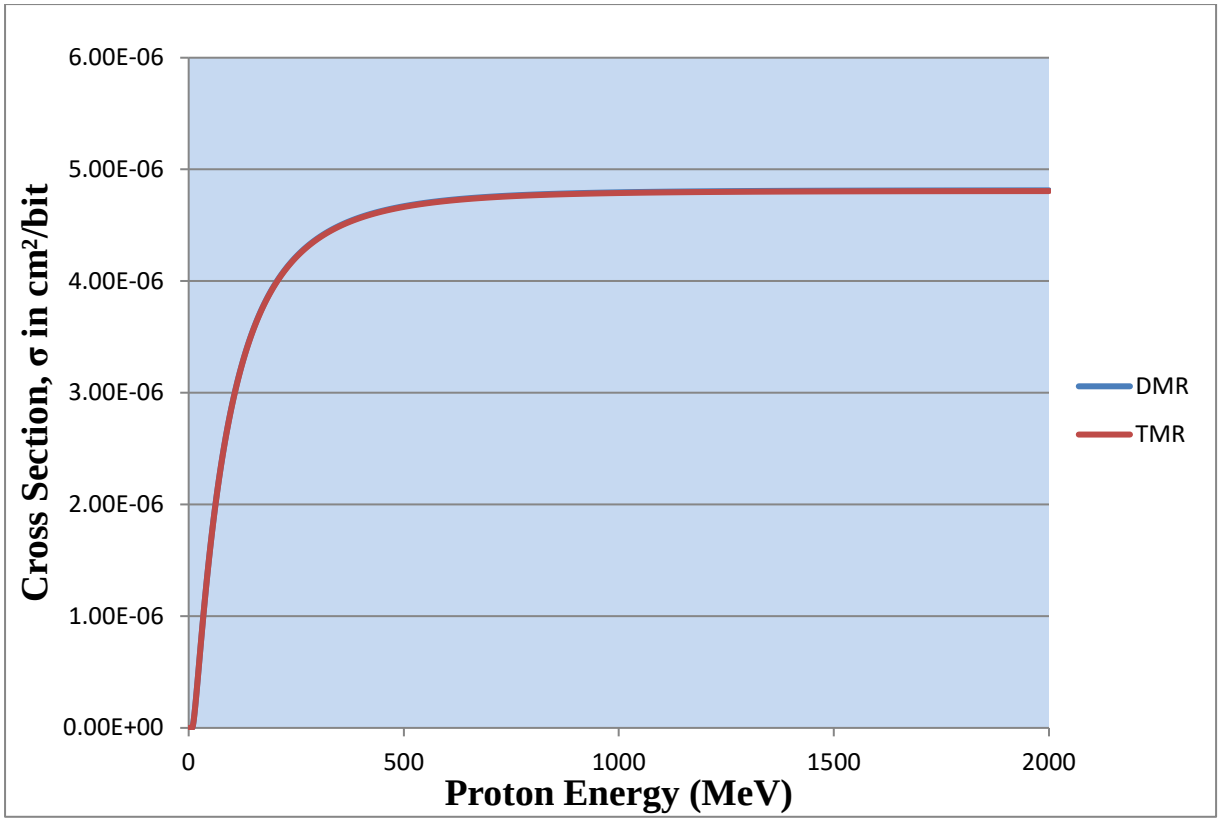

Figure 53 - Cross section versus proton energy of the DMR and global TMR designs when the beam was degraded using 24mm Perspex

In order to obtain a comparison between the results of the benchmark beam and the degraded beam, the cross section data was combined and extrapolated using the Bendel functions. The 2nd test run of the benchmark beam test was used because it was run at similar specifications to all three tests run using the degraded beams, i.e. current of 10nA.

Cross section information at proton energy of 7.79MeV was not included in the combined graph because the saturation values were very high compared to the rest of the data. However, using figures 52 and 53, one can make comparisons to the data shown in the combined graph. Figure 54 shows the cross section per bit data when the degraded beam results are combined with the 2nd test run of the benchmark beam using the Bendel-1 prediction until saturation at 2000MeV. Figure 55 shows the combined cross section at four different energies (7.79, 31.969, 45.79 and 56.9MeV) where the experimental data was overlaid onto the Bendel-1 predicted data.

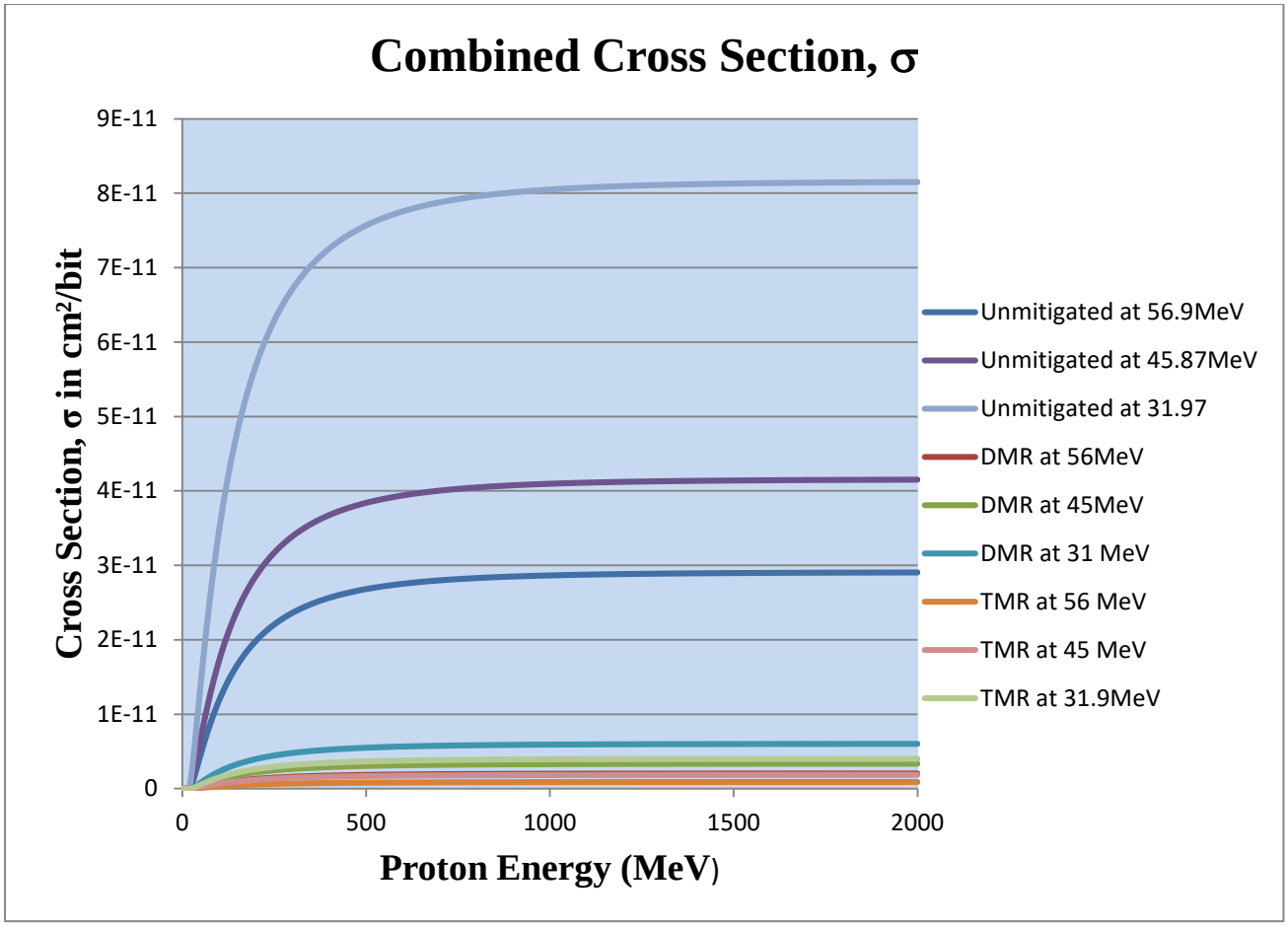

Figure 54 - Cross Section per bit data of the tests combined.

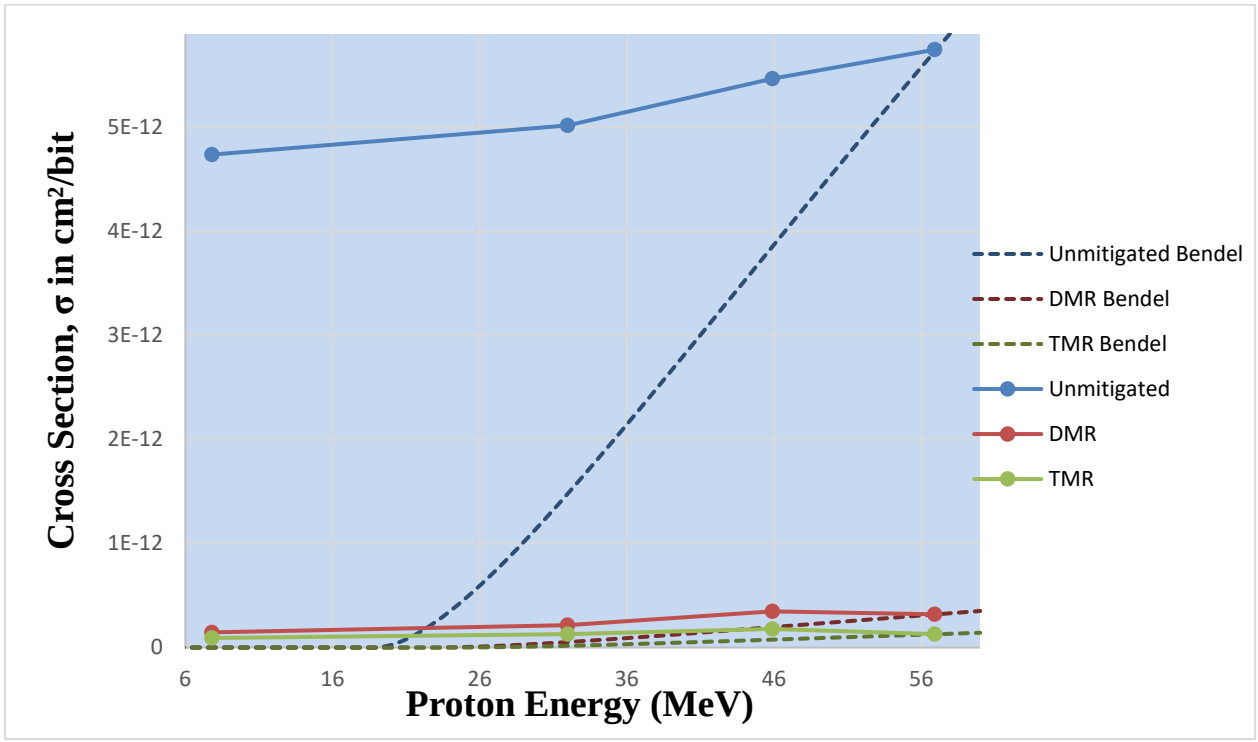

Figure 55 – Combined experimental cross section area overlaid onto the Bendel-1 prediction

4.2.3. Increased current run

The final test run involved keeping the beam current constant at 20nA for 10 and 15 minutes. The number of errors observed and fluence across the three different implementations was logged and shown in tables 22 and 23 respectively. During the 15 minute run for the unmitigated design, the board was noted to be unresponsive after approximately 3 minutes, 50 seconds.

	Errors Counted	Time(s)	Current(A)
Unmitigated	176	600	2.00E-08
DMR with SEE filter	124	600	2.00E-08
TMR	78	600	2.00E-08

Table 22 - number of upsets observed after 10minutes at a current of 20nA

	Total Ions	Particles hitting	Device Area	Fluence
Unmitigated	7.4869E+13	1.09E+13	1.81%	1.98E+11
DMR with SEE filter	7.4869E+13	1.09E+13	4.89%	5.35E+11
TMR	7.4869E+13	1.09E+13	7.37%	8.06E+11

Table 23 - Fluence of each implementation when current was increased to 20nA

Using the error count and fluence information from tables 22 and 23 respectively, cross section and cross section per bit were calculated for the 10 minute run of the three implementations in a similar way to the previous tests as follows:

Unmitigated design

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{176}{1.98x10^{11}}$$

$$\sigma_{\text{device}} = 8.87\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{8.87\text{x}10^{-10}}{602}$$

$$\sigma_{\text{per bit}} = 1.473x10^{-12}\ \text{cm}^2/\text{bit}$$

DMR and filter combination

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{124}{5.53x10^{11}}$$

$$\sigma_{\text{device}} = 2.317\text{x}10^{-10}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{2.317\text{x}10^{-10}}{1790}$$

$$\sigma_{\text{per bit}} = 1.295x10^{-13}\ \text{cm}^2/\text{bit}$$

Full global TMR

$$\sigma_{\text{device}} = \frac{\text{number of upsets}}{\text{fluence } (\frac{\text{ions}}{\text{cm}^2})}$$

$$\sigma_{\text{device}} = \frac{78}{8.06x10^{11}}$$

$$\sigma_{\text{device}} = 9.6791\text{x}10^{-11}$$

$$\sigma_{\text{per bit}} = \frac{\sigma_{\text{device}}}{\text{number of flip flops}}$$

$$\sigma_{\text{per bit}} = \frac{9.6791\text{x}10^{-11}}{1802}$$

$$\sigma_{\text{per bit}} = 5.371x10^{-14}\ \text{cm}^2/\text{bit}$$

5. CHAPTER 5

This chapter introduces the reader to the discussion regarding the results obtained in chapter 4 and then summarises the analysis. It concludes with recommendations for future research and the references used throughout this study.

5.1. Discussion

This subsection discusses the results obtained from the experimental testing of the DUT at iThemba LABs presented in the previous chapter. It is broken down into two sub-categories: when the device was irradiated using the benchmark beam energy of 56.9MeV and the other when using degraded beam energies of approximately 45MeV, 31MeV and 7.9MeV.

The first test run was carried out at a current of 5nA and it was expected that this run would have the lowest number of upsets observed across all the three implemented designs. The unmitigated design recorded 50 upsets, DMR recorded 27 while the global TMR design recorded 25. From this information and the cross section data seen in figures 44 and 45, it can be seen that the DMR mitigated design reduced the calculated cross section by 93.3% whereas global TMR reduced the probability of an upset happening by 95.9%.

Data in table 10 shows that the number of upsets increased for all three implemented designs when the beam current was doubled to 10nA. This was anticipated because increasing the current implied more protons were likely to cause an upset through ionization or secondary particle collision. The unmitigated design consequently had a calculated cross section per bit of $5.749 \times 10^{-12} cm^2/bit$. This was higher than the first test run cross section per bit of $5.581 \times 10^{-12} cm^2/bit$. Data in table 12 along with the graph information in figures: 46 and 47 further show that DMR and global TMR designs lowered likelihood of upsets happening in the device by 94.4% and 97.8% respectively.

Degradation of the beam was carried out to vary the statistics with the hope of obtaining more accurate results. When 8mm Perspex was used, the estimated beam energy transmitted to the device according to SRIM was 45.875MeV and it was anticipated that less upsets would be observed because the protons would have less energy when they collide with the DUT.

The unmitigated design recorded 98 upsets and this resulted in a cross section per bit of $5.47 \times 10^{-12}\ cm^2/bit$. This was lower than the cross section per bit of the similar test run at a current of 10nA using 56.9MeV by 4.9%.

Mitigation using the DMR and filter combination resulted in a cross section per bit of $3.48 \times 10^{-13} cm^2/bit$ after 50 upsets were observed. This was a reduction of 93.6% with respect to the unmitigated design. Global TMR recorded a lower upset count than both the unmitigated circuit and the DMR and filter combination. This resulted in an even lower cross section of $1.79 \times 10^{-13} cm^2/bit$ which signified a 96.7% reduction.

Similarly, degradation of the beam energy using a thicker Perspex plate of 16mm led to an even lower energy for the protons. Therefore, upsets were expected to be less for all the three designs. The unmitigated design recorded 90 upsets, DMR and the filter combination recorded 31 while full global TMR recorded 28. From this information, the resulting cross section was anticipated to be lower than when 8mm plates or when the beam was still at maximum energy.

The unmitigated design had a calculated cross section per bit of 5.02×10^{-12} cm^2/bit which was a reduction of 12.6% with respect to the second test run of the day which was also carried out at 10nA but using the benchmark beam energy of 56.9MeV. The DMR-filter combination had a resulting cross section of 2.16×10^{-13} cm^2/bit whereas global TMR had 1.29×10^{-13} cm^2/bit. This can be translated as 95.7% and 97.4% reductions with respect to the unmitigated design carried out at an estimated energy of 31.969MeV.

Using 24mm Perspex plates led to the anticipated lowest degraded energy of 7.79MeV according to the simulations from SRIM software. Therefore, the number of upsets was expected to be the lowest of all tests run during the day. As illustrated in table 19, the unmitigated design was seen to generate 85 upsets while the DMR-filter combination and global TMR recorded 21 and 20 respectively. From this information, cross-section per bit of the unmitigated design was calculated as 4.74×10^{-12} cm^2/bit which was much lower than the similar unmitigated design carried out with the benchmark beam energy in the second test run by 17.5%.

Due to the fact that the DMR-filter combination and global TMR designs recorded almost similar number of upsets at such low energy, it was anticipated that they would have almost equal cross sections. The DMR-filter combination had 1.46×10^{-13} cm^2/bit whereas full global TMR had a calculated cross section per bit of 9.18×10^{-14} cm^2/bit. This can be translated as a reduction of 96.9% and 98.1% with respect to the unmitigated design carried out at 7.79MeV. These are significantly larger reductions of the cross section per bit than at the higher energies, possibly, because at high energies, protons possess more accelerating power to cause ionisation upon collision with matter as discussed in chapter 2.

The final test run of the day involved irradiating the device at an even higher current of 20nA for longer periods of 10 and 15 minutes. This test run was also carried out using the benchmark beam (56.9MeV) and there was increased fluence in all three designs and this led to more upsets observed. When the DUT was irradiated at 20nA, the board was responsive after approximately 4 minutes. It can be noted that the unresponsiveness of the device was possibly due its destruction by the effect of Total Ionising Dose, which occurred as a result of continuous exposure of the device to highly energised protons over long periods.

The combined device cross section per bit information shown in figure 54 indicates that the unmitigated designs consistently achieved higher saturation compared to the designs mitigated using both DMR and TMR. Also, the lower energy led to a higher saturation compared to the higher energies. This could be attributed to the fact that lower energies led to higher ionization which led to increased single event upsets.

Experimental device cross section area per bit at four different energies (7.79, 31.969, 45.87 and 56.9 MeV) is shown in figure 55 where it is overlaid with the Bendel-1 prediction. It can be seen that the unmitigated design consistently had a significantly higher cross section per bit followed by the DMR-filter combination and finally the TMR mitigation technique. This is consistent with the Bendel-1 prediction used in figure 54 up to 2000MeV. However, it should be noted that the Bendel-1 predicted cross section increases exponentially after approximately 20MeV for the unmitigated design and after approximately 28MeV for the DMR filter combination and TMR designs.

Overall, when the cross section per bit data of both the DMR-filter combination and global TMR are analysed using the graphs in subsections 4.2.1 and 4.2.2, it can be seen that both implementations consistently reduced the probability of an upset happening by approximately 93% for the DMR-filter combination and 97% for global TMR.

5.2. Conclusion

Xilinx Artix-7 FPGA is a low cost device which can be used for a variety of advanced applications. In this study, its suitability for use in radiation exposed environments like space was assessed by implementing three hardware designs and then exposing it to radiation using highly energised protons at the iThemba LABs facility in Cape Town.

The goal of radiation testing was to obtain a relationship between the device cross section per bit and proton energy. A higher device saturation cross section per bit implied that the design was more susceptible to single event upsets at that particular energy. Altering between energies at iThemba LABs would have been time consuming and potentially costly. It is for this reason that single proton energy of approximately 56.9MeV was used and then degraded to 45.87MeV, 31.969MeV and 7.79MeV using Perspex plates of varying thickness placed in the path of the beam. Using Bendel equations, the single energy was extrapolated to model the device cross section relationship over energies up to 2000MeV.

There were three designs implemented on the Xilinx Artix-7 FPGA. The reference design was un-mitigated against the effects of such radiation whereas the second design was mitigated using a technique developed at the Nelson Mandela University known as the DMR-filter combination while the final design was mitigated using the well-known triple modular redundancy (TMR).

The DMR-filter combination utilised a smaller area compared to the global TMR while still achieving noticeably low saturation cross section per bit results. Based on this, it is a suitable mitigation technique against single event upsets which occur in combinational circuits while saving resource area on a micro-electronic device for more critical applications.

Full global TMR still remained the most effective mitigation technique used as it resulted in the lowest saturation cross section. It however used 33.6% more resources as compared to the DMR-filter technique. In this regard, therefore, it should be used to mitigate single event upsets if area resources on a device are not a major concern.

5.3. Recommendations for future research

After a test was carried out in the radiation chamber, some of the radiation did not dissipate immediately. This was a challenge in that, the next set of measurements was offset and did not give a true representation of the actual number of particles that actually caused an upset. Therefore, in order to improve the accuracy of the testing and provide a better representation of the event upset counting, future researchers should consider taking a measurement of the beam line monitors between each set of test runs. Additionally, there should be ample time between the testing to allow the radiation to dissipate from the chamber.

Instead of degrading the beam using Perspex plates, pre-set calibrated beam energy levels should be made available by the testing facility so as to provide more accurate statistics since it won't require estimation of the energy using calculations. It is an expensive and time consuming process to provide different energies for testing but it would have the advantage of allowing the use of better models for fitting data as opposed to the Bendel functions.

The test rig should allow for dynamic change of orientation while testing; as this would vary the angle of incidence at which the beam collides with the DUT and thus provide a more representative scenario of particle collision which leads to event upsets in the space environment.

Finally, future testing should also be carried out under a vacuum chamber as this ensures that the beam maintains a higher energy and can thus guarantee more accuracy with the results. .

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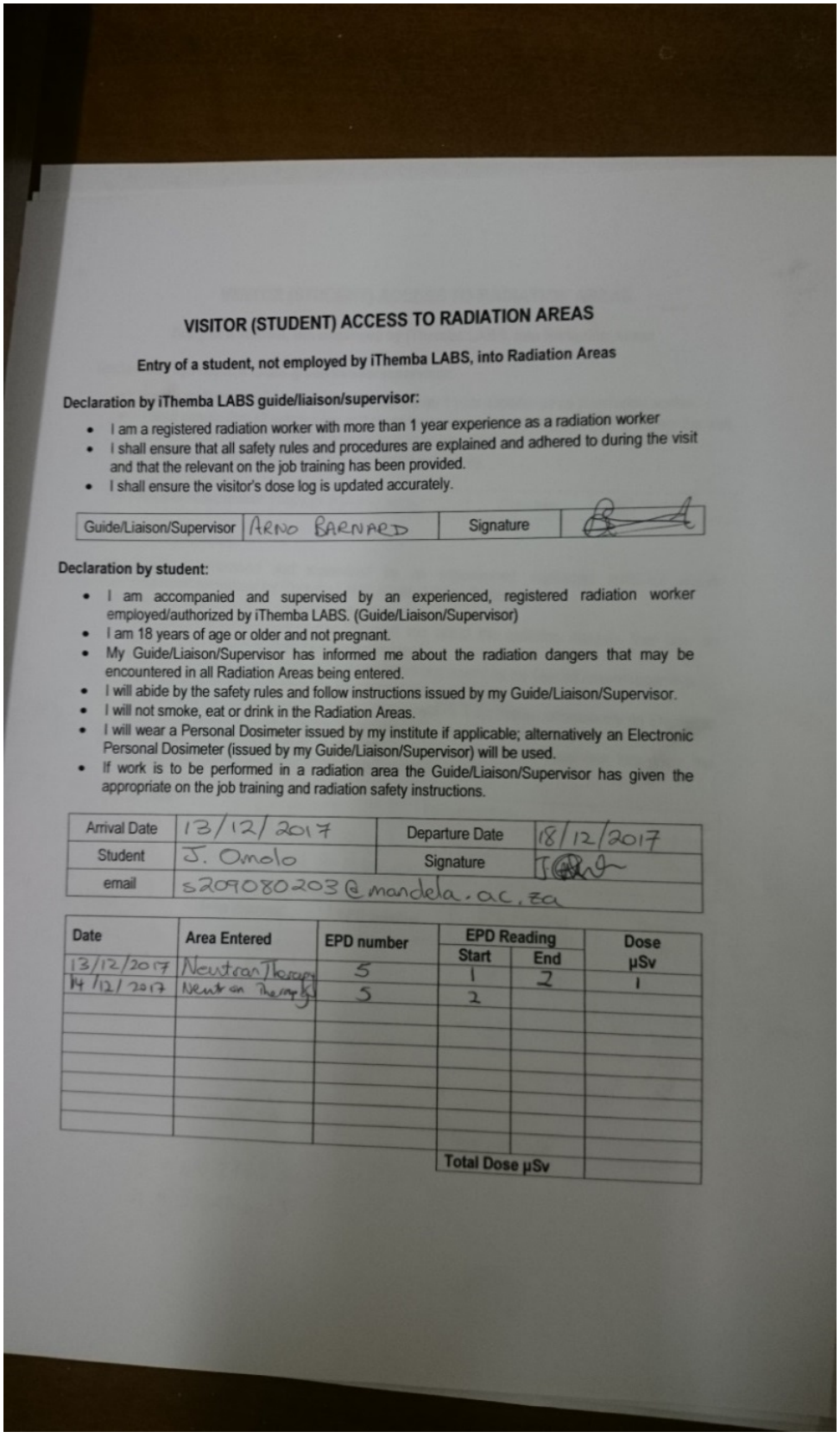
Appendices

Appendix ‘A’	iThemba LABs consent form for non-registered radiation workers
Appendix ‘B’	Schematic of the setup
Appendix ‘C’	Test log at the N-Line radiation vault

Appendix A



VISITOR (STUDENT) ACCESS TO RADIATION AREAS

Entry of a student, not employed by iThemba LABS, into Radiation Areas

Declaration by iThemba LABS guide/liaison/supervisor:

- I am a registered radiation worker with more than 1 year experience as a radiation worker
- I shall ensure that all safety rules and procedures are explained and adhered to during the visit and that the relevant on the job training has been provided.
- I shall ensure the visitor's dose log is updated accurately.

Guide/Liaison/Supervisor	ARNO BARNARD	Signature	

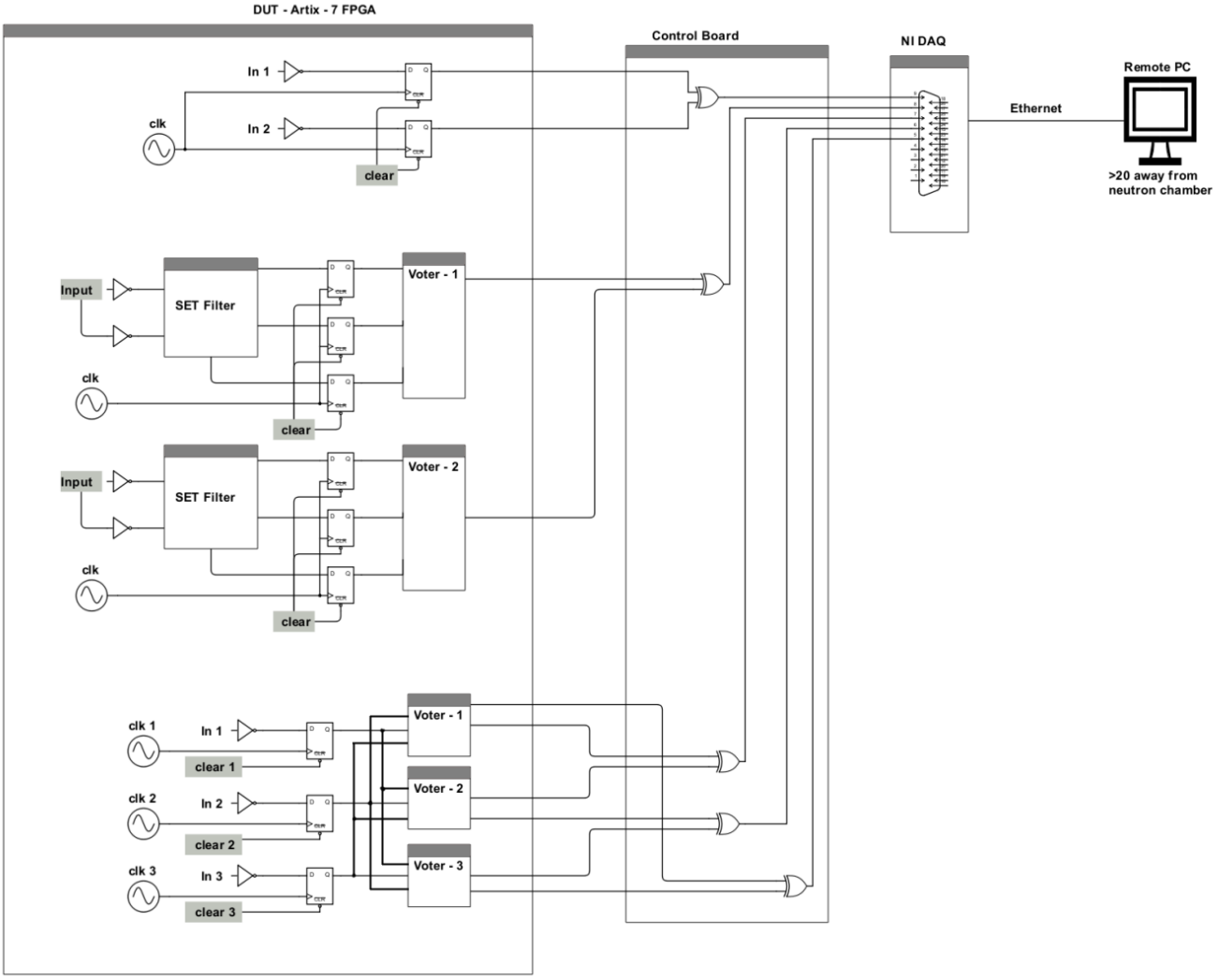
Declaration by student:

- I am accompanied and supervised by an experienced, registered radiation worker employed/authorized by iThemba LABS. (Guide/Liaison/Supervisor)
- I am 18 years of age or older and not pregnant.
- My Guide/Liaison/Supervisor has informed me about the radiation dangers that may be encountered in all Radiation Areas being entered.
- I will abide by the safety rules and follow instructions issued by my Guide/Liaison/Supervisor.
- I will not smoke, eat or drink in the Radiation Areas.
- I will wear a Personal Dosimeter issued by my institute if applicable; alternatively an Electronic Personal Dosimeter (issued by my Guide/Liaison/Supervisor) will be used.
- If work is to be performed in a radiation area the Guide/Liaison/Supervisor has given the appropriate on the job training and radiation safety instructions.

Arrival Date	13/12/2017	Departure Date	18/12/2017
Student	J. Omolo	Signature	
email	s209080203@mandela.ac.za		

Date	Area Entered	EPD number	EPD Reading		Dose µSv
			Start	End	
13/12/2017	Neutron Therapy	5	1	2	1
14/12/2017	Neutron Therapy	5	2		
			Total Dose µSv		

Appendix B


DUT - Artix - 7 FPGA
Control Board
NI DAQ
Remote PC
Ethernet
>20 away from neutron chamber
In 1
In 2
clk
clear
Input
SET Filter
Voter - 1
Voter - 2
Voter - 3
clk 1
clk 2
clk 3
clear 1
clear 2
clear 3

Appendix C

Transcribed from SEE logbook # 1 - pages 1 to 8

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Page 1:

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Arno's beam test

18 December 2017

Monday

Scalar ch 0 = Reference BLM on beam left

Scalar ch 3 = BLM on chip frame for test of beam profile

Laptop: pr166@k600

Runs 26-29

Characterizing beam profile with BLMs.

See Arno's logs for position.

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Page 2:

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BLM rates

Centre BLM count rate (Hz)	I (nA)	ratio (counts / I)
~2m	10	2/10 = 0.2
1.55m	5.6	1.55/5.6 = 0.27
0.900m	2.2	0.9/2.2 = 0.4

0.550 1 0.55/1 = 0.55

At same time

Reference I

~500Hz 5.6 ~89

~230Hz 2.2 =40% ~104

van 5.6

230/500 ~ 0.46

~120Hz 1 120

1.55 x 500/5.6 = 138

0.9 x 230/2.2 = 94

055 x 120/1 = 66

(Two graphs drawn)

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Page 3:

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Run 30 12:23 - 12:35

5.5nA

1st SRAM test

Reference BLM ~ 550Hz

Ask for increase of beam @ 6min 16 sec

10.4nA

BLM @ 1050Hz

Beam stopped at 9min 38sec

Raspberry Pi giving problems?

Run 31 13:02 - 13:14

9.6nA

2nd SRAM test

Reference BLM ~850-900Hz

After 4min 11sec move to 20.7nA

Reference BLM @ 1970 Hz

After 9min 17sec move to 30.3 nA

Reference BLM @ 2800Hz

Stopped run since "network is down".

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Page 4:

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Note on Profile runs (ran earlier this morning)

Run # 26 10nA

~100 Hz on reference BLM

After 11min 20sec go to 5.6nA

Centre BLM @ 1.55 MHz

Reference counter 480-520Hz

#27 Started 9:34

#28 Started 10:00 -> 10:20

2.2nA

Reference counter ~200Hz at 2.4Na

Asked for alignment check

#29 1nA

Reference BLM ~124Hz

During this run we also moved vertically through the centre.

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Page 5:

==========

Run 32 13:56 -

FPGA test

5.3nA

~540Hz on BLM monitor / reference

Start 3min beam cycles

Ask or 10nA after two beam cycles

At 7:39 got to 10.3nA

BLM reference @ ~980 Hz

at ~ 12m 10sec goes to 2nd 10nA cycle

5min

at 19min 40sec go for 1st 20.3nA cycle

BLM reference @ ~1980Hz

at 26min 33sec go for 2nd 20.3nA cycle

BLM reference @ ~1900Hz

at 39min go for another 20nA cycle

at ~43min Farouk's board dies

Wait a few min before going in.

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Page 6:

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8mm Perspex degrader in position before final square collimator

Asked for 10nA, got 10.1nA

Run 33 15:18 - 15:22 8mm Perspex degrader

~900Hz on BLM reference

10.1nA

FPGA test

1 x 3 min run

Run 34 16mm Perspex degrader

15:23 -

BLM reference ~920Hz

Run 35 24mm Perspex degrader

15:40 -

BLM reference ~930Hz

3min run

then 5min run

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Page 7:

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End of beam time.

26/1/2018 AB: Notes on Setup Geometry for 18/12/2017 test

See photos

-> Distance -> HAVAR windows (rim - window is ~10mm deeper) -> Scatterer = 230 mm

200 x 200 mm Pb = 1 mm -> Pb scatterer (B) -> col 1 (F) = 235 mm

Hole diameter = 100 mm col = 50 mm -> col 2 = 21 mm

Diameter 120, hole diameter = 30 mm col 2 = 50 mm -> col 2 -> col 3 = 575 mm

Diameter 120, hole diameter = 40 mm col 3 = 50 mm -> col 3 -> degrader = 1120 mm, degrader was a bit skew

Diameter 120, hole square = 30 x 30mm Col 4 = 50 mm -> col 3 -> col 4 = 1230 mm

100 x 100 mm degrader (various thickness) -> degrader -> col 4 = 110 mm

-> col 4 -> PCB/Jig = 353mm/370mm

BLM -> Fixed -> from scatterer = 460mm

Right-angle to rail = 279 mm

Right-angle to scatterer = 285 mm

Angle (calculated) =

Height difference = negl.

-> scanning => Casing -> Jig = 13mm

Table height (measured) 878mm

+ 43mm supports = rail base

+ 16mm rail base

+ 8mm 3D printed support clamps

+ 20mm rail

+ 8mm clamps

+ 10mm plywood support

-> Stand base

+189mm -> stand collimator holder base (col4)

->

193mm for col 3

199mm for col 2

Table @ 856mm @ col 2

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