A novel photodiode array for astronomical spectroscopy

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A NOVEL PHOTODIODE ARRAY FOR ASTRONOMICAL SPECTROSCOPY

by

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ABSTRACT

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Imaging arrays can be constructed from photodiode sensor elements using integrated circuit fabrication techniques. Such imaging arrays have proved to be useful in the field of observational astronomy, chiefly because of their linearity and good spectral response in the near infra red region.

A photodiode array has been developed by the Plessey Co. Limited, in collaboration with the Royal Greenwich Observatory. This array incorporates certain novel techniques, including an "on-chip" charge amplifier on each element, and a multiplexing scheme that allows correlated double sampling and non-destructive readout. The array was originally designed to be used in an electron counting mode, installed in an electronographic tube.

The Nuclear Instrumentation Group of Durham University has investigated the application of this array to direct optical imaging, in particular for astronomical spectroscopy.

The characteristics of the array when used in the photon integration mode have been investigated, and measurements have been made of responsivity, thermal leakage, linearity, noise components, and other properties.

A CAMAC based computer control system has been designed and constructed, and the required software developed, to operate the array as an observing instrument.

The array has been used in observational tests at the Coudé spectrograph of the 30 inch telescope of the Royal Greenwich Observatory, and a quantity of spectral data has been obtained.

CONTENTS

CHAPTER ONE

The Development of Silicon Detector Arrays and their use in Astronomical Imaging

Solid state silicon photodetectors possess several characteristics which make them eminently suitable for astronomical use. These are chiefly a very high quantum efficiency and a linear response to light in the visible and near infra-red regions. Of equal importance is the ability to fabricate large multielement detector arrays, taking advantage of the enormous advances in silicon integrated circuit technology made since the mid 1960's

This thesis describes such a multi-element array based on photodiodes, manufactured by Plessey in collaboration with the Royal Greenwich Observatory.

Firstly, the need for such a device within the realm of astronomical instruments is established, and this is followed by a review of the development to date of solid state imagers. Following chapters describe the principles of operation of photodiode arrays, the development of the Plessey array and its computer based control system, the initial laboratory experiments on the device and the incorporation of the array into an astronomical spectrograph.

1.1. The Detector in Astronomy

The growth of interest over the last few decades in the development of detectors for use with telescopes can be explained by considering the ways in which the "power" or limiting magnitude of a telescope can be improved. Simplistically, the limiting magnitude of a telescope is defined by the detector sensitivity and by the light collecting ability of the optical system. In order to raise the system "power" by a factor of two, it is necessary to double the area of the primary mirror. The cost of constructing large telescopes tends to increase somewhat faster than the square of the primary mirror diameter.

The same advantage can be achieved by a factor of two improvement in detective quantum efficiency, usually at considerably lower cost.

1.1.1. Detector Requirements

Prior to the further discussion of the type of detectors used in astronomy, some mention should be made of the type of work for which such detectors are required, and the constraints so imposed.

The two fields for which detectors are most widely used in astronomy are Photometry and Spectroscopy. Photometry is the measurement of the intensity of light emitted from stellar and extended objects. A detector for photometric work should therefore have a response as linear as possible. However, there is usually no requirement for spatial imaging. In Spectroscopy, the incoming light is "split" by some diffractive element, usually a grating, and the relative intensities of the component wave-lengths are measured. This can be achieved by mechanically scanning the spectrum with a single channel detector, but ideally the detector itself should be capable of resolving the spectrum spatially. Such resolution is usually only required in one direction, that is "along" the spectrum.

Many more fields of astronomy have developed as suitable detectors have become available. Many of these, such as polarimetry require detectors capable of 2 dimensional resolution.

One fundamental property of many (but not all) astronomical detectors which should be mentioned here is the ability to integrate a signal between readouts. There is usually associated with a optical detector a certain amount of noise involved in the readout process.

It is thus advantageous to integrate and store the signal until the magnitude of the stored signal is large compared with the noise incurred by the readout mechanism. This will obviously reduce the ability of the detector to respond to time varying signals, but in many astronomical applications, this limitation is not critical.

As will be seen in a later section, the requirements of astronomy are such that a good detector for commercial imaging is not necessarily suitable for astronomical use. Solid state detectors are, however, almost invariably developed for commercial use, and the astronomical user must often make the best of what is available.

1.1.2. Traditional Detectors

The traditional detectors employed in conjunction with telescopes, are, in historical order, the Photographic Plate, the Photoelectric Cell and the Photomultiplier.

The Photographic emulsion, or plate, has been in use now for astronomical observation for over a century and is still probably the most popular and often used detector. It suffers, however, from several inherent problems. Photographic plates have a quantum efficiency of usually less than 1%, although values as high as 4% have been reported[1]. A further problem, and perhaps the most crucial, is that the quantum efficiency is dependent on the light intensity, and the image produced by a long exposure to faint light is fainter than that produced by a short exposure to strong light

even when the total number of incident photons is the same in both cases.

Despite problems associated with its use, the photographic plate is still widely used. Its spatial resolution is difficult to match, it is cheap and relatively simple to use.

The photoelectric cell is the simplest of the electronic detectors utilising photoemissive cathodes. The quantum efficiency can be as high as 20%[27], and the linearity is extremely good. The spectral response depends on the composition of the photocathode, but very few photocathodes have a significant response above about 10,000 Å. Figure 1.1. shows the responses of three types of photocathode known as S20, S1 and Ga As.

The short coming of the photoelectric cell lies in its very low signal output. Each photoelectron emitted by the photocathode produces only one electron charge at the output, and the output current must be greatly amplified before it can be recorded. Nevertheless, considerable studies have been made in both photometry and spectroscopy using such devices. An immediately apparent disadvantage is that the photoelectric cell is a single element detector. Consequently, for spectroscopy it is necessary to construct either a multiplexed array of several tubes, a scanner in which the detector is scanned along the direction of dispersion, or alternatively a scanner in which the dispersing element is rotated. The last two systems obviously suffer the disadvantage that at any one time only a small fraction of the available light is presented to the detecting element.

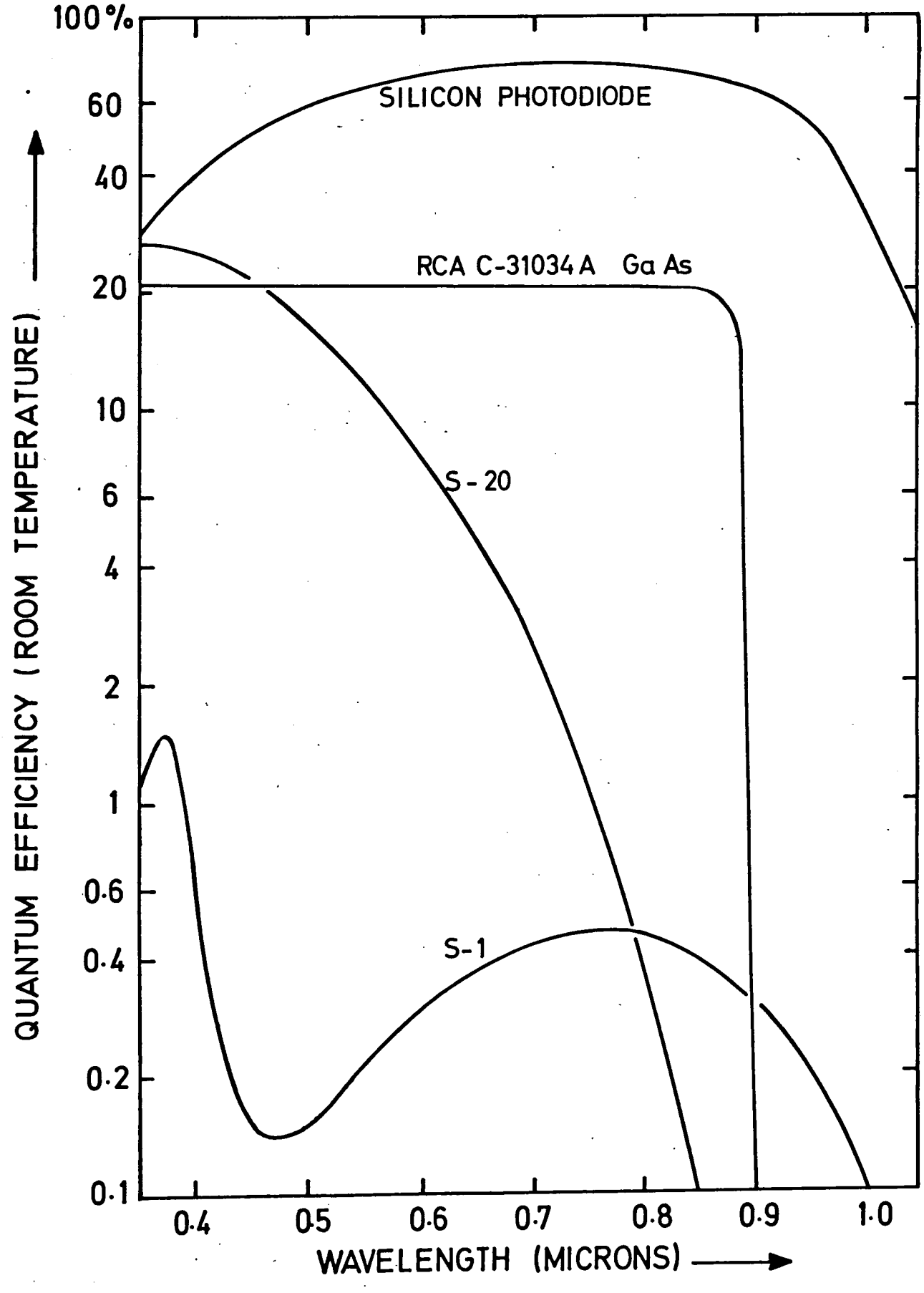


FIG.1.1. SPECTRAL RESPONSES

Photomultipliers, which have internal gain in the dynode chain, can be considered as being similar to a photoelectric cell with an integral, very low noise amplifier having a gain of between 10^6 and 10^9. This has led to their extensive use in astronomy in situations previously using photoelectric cells. The statistical fluctuations in gain in the dynode chain lead to a reduction in the signal to noise ratio, but this can be overcome to a considerable extent by the use of pulse counting techniques rather than simple current integration methods.

There is clearly a demand in astronomy for a detector that will combine the linearity and dynamic range of the photomultiplier with the spatial coverage of the photographic plate. A wide variety of approaches have been followed including electronography, image tube scanners using both analog storage in the phosphor and external digital storage, and television type systems. More recently, interest has been focussed on a variety of solid state image detectors. A major problem in the development of "high technology" astronomical detectors is that even the most successful system is likely to be operated at maybe a dozen sites at the most, and the research and development costs may prove prohibitive. However, the enormous funding devoted to solid state imaging by the military (for the development of surveillance and guidance systems) and by commercial companies (for the development of a television camera replacement) has made such detectors available at relatively low cost, and this has made them very attractive for astronomical work.

The following section will describe the historical development and principles behind the most promising of these devices.

1.2. The Development of Solid State Imagers

The solid state multielement imager first became an attractive prospect with the development of silicon integrated circuit technology. By the use of integrated circuit techniques it would be possible to implement both the detector elements and their readout electronics using the same technology, offering all the traditional advantages of low cost and high reliability associated with integration. The variety of detector schemes which have arisen can be subdivided into two families according to the mode in which information is extracted from the detector element and transferred to the output. It is worth noting here that the vast majority of solid state imagers employ serial readout. Parallel readout of multielement detectors becomes uneconomic both in terms of leadouts and readout electronics for more than a few elements. In the first class of detectors, readout is accomplished by "interrogating" each element in turn. When selected, the output of the element is gated onto a video output line. These are termed addressed arrays. Such arrays can be constructed with a random access organisation, but it is more common to implement the addressing function with a shift register and thereby create a sequential access structure.

The second class of detector array makes use of an analog shift register into which the element signals are loaded, and then clocked through to the output end of the register. This technique was not feasible until the invention of Charge Transfer Devices enabled the construction of good analog shift registers.

The following sections review the development of each type of array

1.2.1. Addressed Mode Arrays

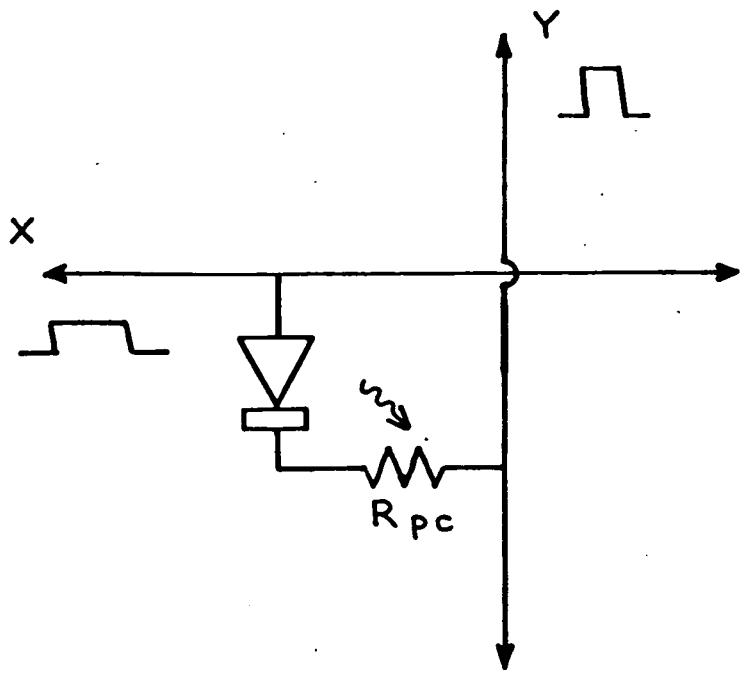
(i) Photoconductive and Phototransistor Arrays

The earliest attempts at producing solid state image sensors were begun before silicon integrated circuit technology was well established. These first devices employed thin film transistor shift registers to scan arrays of photoconductive sensors. The circuit of a single element of such an array is shown in Figure 1.2. (a). As silicon technology improved, this approach was abandoned, although not before working arrays of 180 x 180 [3], 256 x 256 [4] and 512 x 512 [5] elements had been demonstrated by RCA.

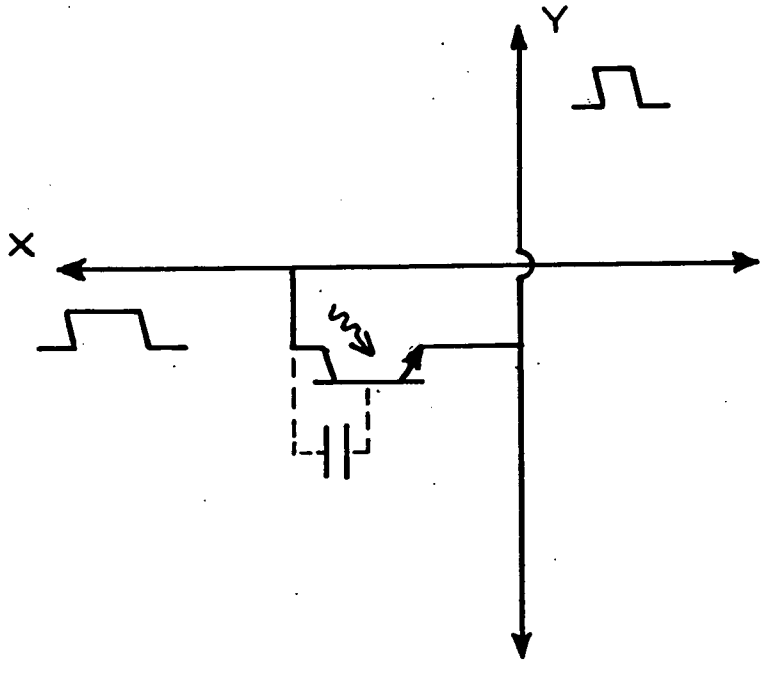
At about the same time, an alternative approach was being followed using bipolar arrays. A 400 x 500 element array was manufactured by Westinghouse [6], using the circuit of Figure 1.2. (b) as the basic element. Problems were encountered with wide variations in transistor gain and with the non-linear emitter-base characteristics, which led to a threshold effect at low light levels. Meanwhile, improvements in MOS technology caused a loss of interest in photoconductive and phototransistor arrays in favour of the simpler MOS photodiode arrays.

(ii) Photodiode Arrays

Interest in Photodiode sensors began when the charge storage mode of operation was suggested by Weckler [7]. In this mode, a p-n junction is first reverse biased and then open circuited. In the dark, the voltage across the junction will decay due to the thermal generation - recombination current in the depletion region. If the junction is illuminated, photocurrent adds to this dark current and increases the rate of discharge of the depletion layer capacitance.



(a) PHOTOCONDUCTIVE ELEMENT



(b) PHOTOTRANSISTOR ELEMENT.

FIG 1:2 EARLY TYPES OF PHOTOSENSOR ELEMENTS

If the photocurrent is very much larger than the dark current then the rate of decay of charge is linearly related to the incident illumination, and hence the total charge lost is proportional to the integral of the illumination.

Early arrays consisted of photodiodes each with a MOS transistor as the switch to open circuit the diode, with each transistor scanned by an element of an external shift register, and single line arrays of several hundred elements were constructed in this way. The next development was the integration of the shift register onto the same silicon chip. The circuit diagram of such an array is shown in Figure 1.3. Linear arrays of this type have been commercially available for several years, chiefly from the Reticon Corporation [8], who at present market arrays of up to 2048 elements.

In such linear arrays, the sensor elements are often elongated to give a large area and therefore high capacitance.

This leads to a large stored signal but without reducing spatial resolution along the direction of scan. Obviously this cannot be done in two dimensional arrays where high resolution is required in both dimensions, and the consequently small signal levels available have proved troublesome. The addition of a voltage sampling MOS amplifier at each element has been experimented with, but the resulting structure is too complex and wasteful of active area to be usable in large arrays. However, 10 x 10 element arrays of this type have been constructed by Plessey [9], and 100 x 100 arrays are available using simpler elements [8]. For area arrays, though, the simpler structure of charge transfer devices has proved more competitive, and consequently development effort in area diode arrays has largely been discontinued.

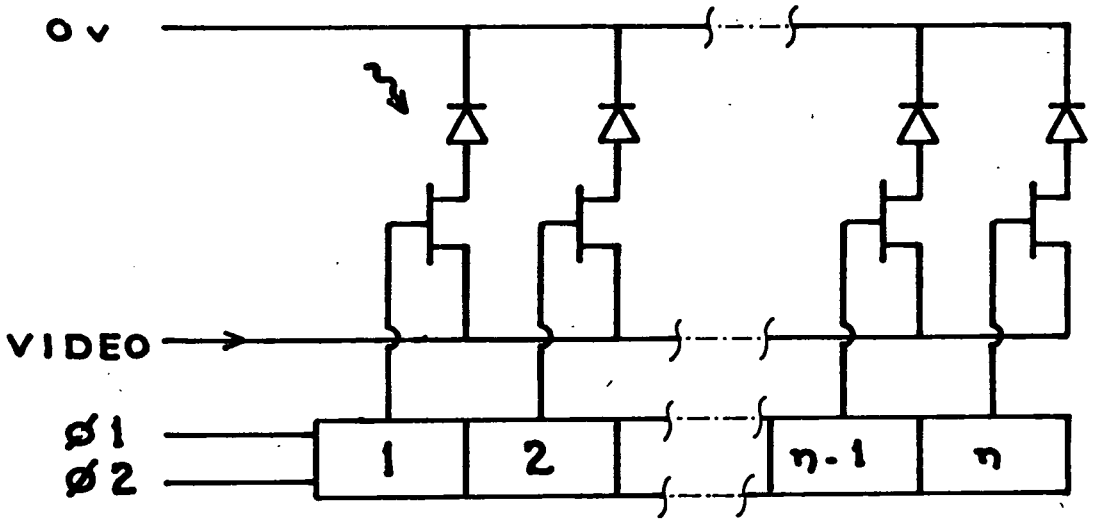


FIG 1:3 n - ELEMENT MOS PHOTODIODE ARRAY.

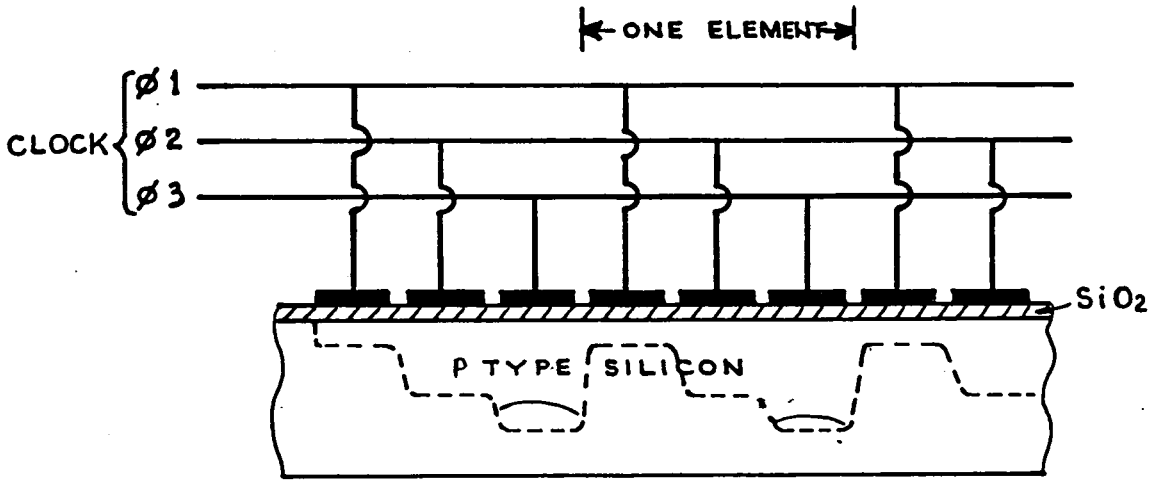


FIG 1:4 STRUCTURE OF A 3 PHASE CCD SHOWING THE PROFILE OF THE POTENTIAL WELLS

1.2.2. Charge Transfer Mode Arrays

Historically the first practical charge transfer device was the Bucket Brigade Device (BBD) developed at Philips by Sangster and Teer [10] in 1969. Considerable interest arose in the potential application to imaging devices. However in 1970, Boyle and Smith of Bell laboratories proposed a device using the charge coupling principle [11]. These Charge Coupled Devices (CCD's) rapidly overtook the BBD in terms of charge transfer efficiency and have since completely dominated the BBD in imaging applications. Consequently the CCD will here be described first and then a brief comparison of the BBD will be given.

(i) Charge Coupled Devices

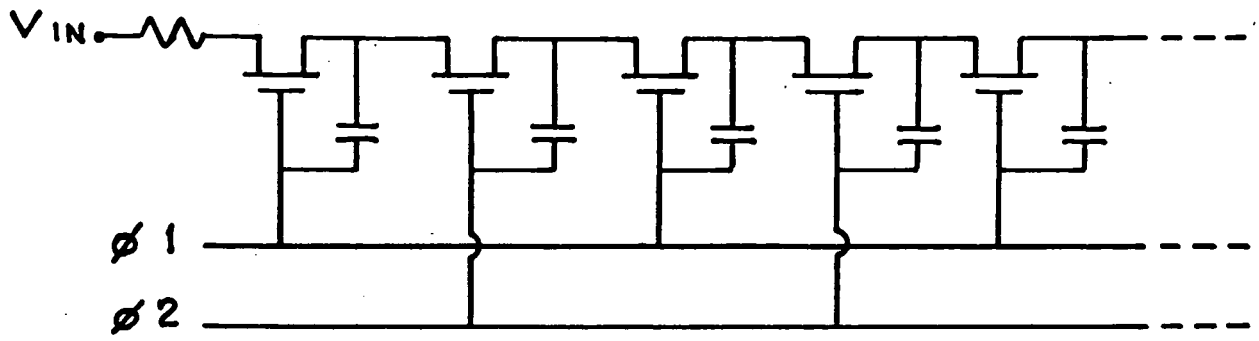
The simplest type of CCD is the p-type 3 phase surface channel device as shown in Figure 1.4. It is essentialy an analog shift register in which a charge packet is stored in potential wells in the MOS structure. These potential wells are created under the electrodes by applying a positive voltage in excess of the threshold voltage to the electrode. If an adjacent potential well is made deeper by applying a higher gate potential, the stored charge can be transferred from the first well to the second. By using a three phase clock, charge can be transferred along a linear arrangement of electrodes. Used as an imaging device, carriers are generated thermally and optically in an analogous way to in the reverse biased diode, and similarly the accumulated charge is proportional to the time integral of the illumination (for illumination levels greatly in excess of the thermal leakage). Thus a linear C.C.D. imaging array can be fabricated which can be compared with a linear photodiode array. The absence of addressing circuits enables a higher packing density to be achieved, and facilitates the construction of area arrays.

(ii) Bucket Brigade Devices

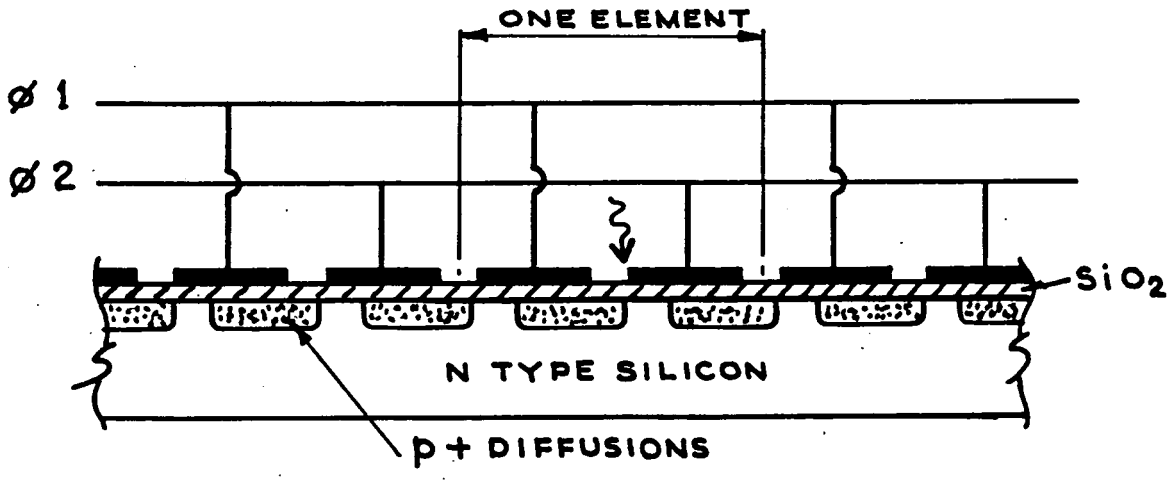
The circuit concepts behind the Bucket Brigade Device as an analog shift register were described as long ago as 1952 [12], but at the time there were no physical components that could approach the idealised switching circuits required. Their successful implementation had to await the development of MOS technology [13], although some initial work was carried out using bipolar circuitry [10].

In contrast to the CCD, the Bucket Brigade Device can be represented by a network of discrete components as shown in Figure 1.5. (a). Also shown (figure 1.5 (b)) is the physical structure of a typical BBD array. Charge is transferred from element to element under the control of a two phase clock (the BBD is a unidirectional register only). The transistors function as source followers which cut themselves off when the transfer to the next stage is complete. Each element of the shift register comprises two transistors and two capacitors. For use as an imager, photosensors must be added to introduce a charge pattern into the capacitors before the application of the clock waveforms. In theory any type of photo-detector can be used, but the photodiode is an obvious choice since these already exist beneath the source and drain diffusions in the MOS structure. It is interesting to note the similarities between the BBD and CCD as shown on Figures 1.4 and 1.5. (b).

Two dimensional arrays using BBD's were successfully produced at RCA [14]. In the early stages of BBD imagers, the CCD was developed which at the time had a very much superior charge transfer efficiency. Consequently interest focussed on the CCD, and Bucket Brigade imager development was abandoned. However, a novel application of the BBD was suggested [14] in which it is used as a scan generator for an addressed mode device such as a photodiode array. By the use of suitable clocks the BBD can be used as a digital



(a) DISCRETE COMPONENT REALISATION OF A BUCKET BRIGADE DELAY LINE



(b) STRUCTURE OF A MOS BUCKET BRIGADE IMAGER

FIG 1:5 BUCKET BRIGADE DEVICES

shift register with only a single transistor and capacitor per stage, a reduction in component count by a factor of about 5 over a conventional MOS register.

The development of CCD technology has made possible the development of a third type of charge transfer device, known as the Charge Injection Device (CID).

iii) Charge Injection Devices

This device combines the addressed mode readout of the photodiode array with the potential well storage concepts of the CCD. Thus although truly this device belongs under the heading of addressed arrays, it is included here because the concepts and technology associated with the charge injection device (CID) are closely related to the CCD.

The first of these devices to be reported was a 32 x 32 element array produced by General Electric [15]. The sensor element consists of two electrodes under which minority carriers are stored, as in a CCD, connected by a diffused link, as shown in Figure 1.6 (a). Potential wells are created beneath the electrodes by application of gate potentials, and charge generation and storage mechanisms are exactly as for a CCD. What is different is the way in which stored charge can be manipulated by varying the potentials on the electrodes. If the gate potential is removed from either electrode, the charge is transferred to under the other electrode (Figure 1.6 (b)). When the potential is simultaneously removed from both electrodes, the charge is injected into the substrate (Figure 1.6. (c)). By measuring the injection of charge into the substrate, an area scanned array can be made, in which the element to be read out is selected by "row" and "column" electrodes being simultaneously returned to zero volts.

The structure of a simple 4 x 4 element CID imager of this type is shown in Figure 1.7.

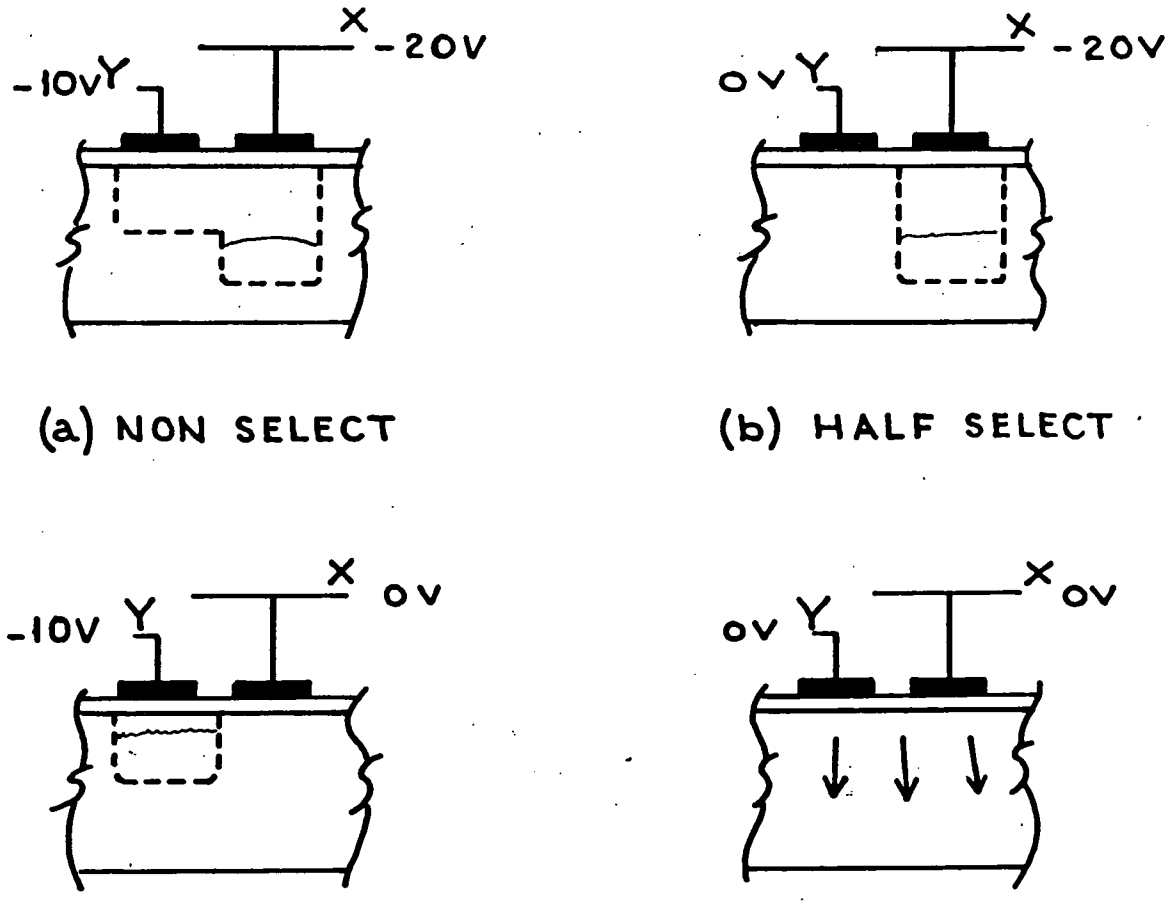


FIG 1:6 ELEMENT STRUCTURE OF A CHARGE INJECTION DEVICE

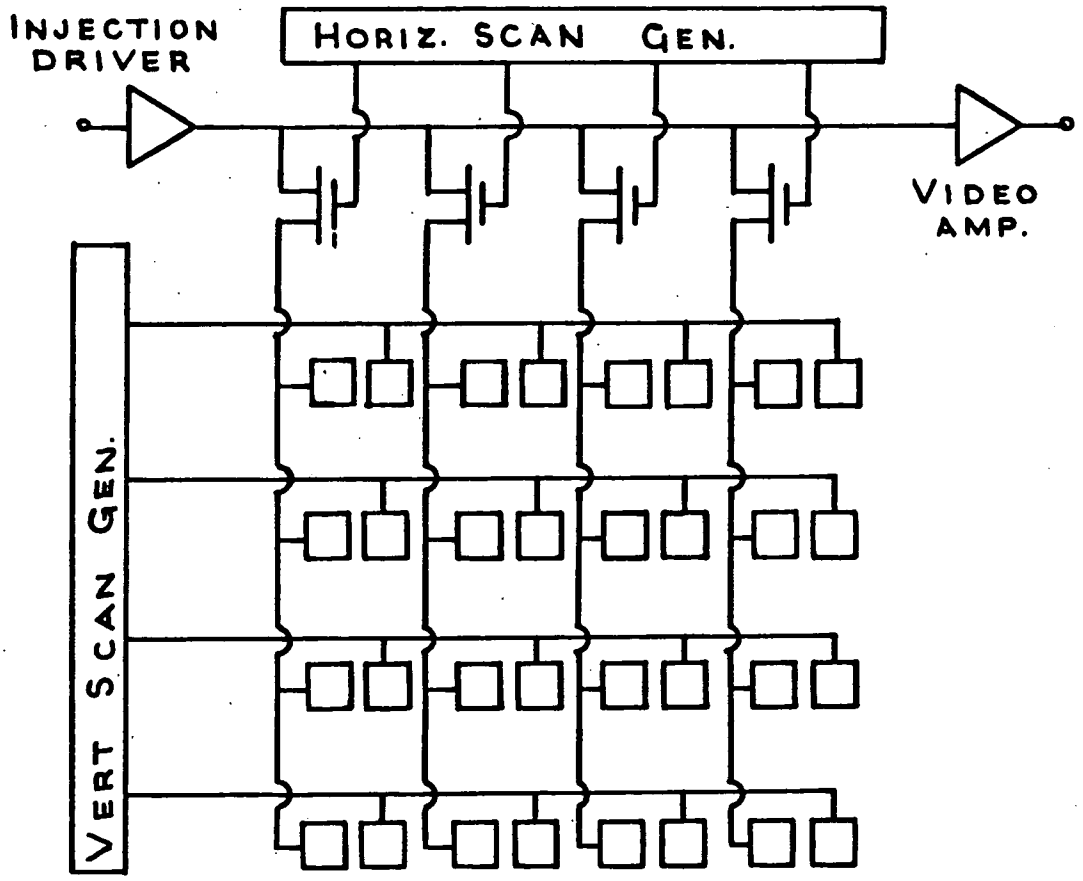


FIG 1:7 SEQUENTIAL INJECTION CID ARRAY

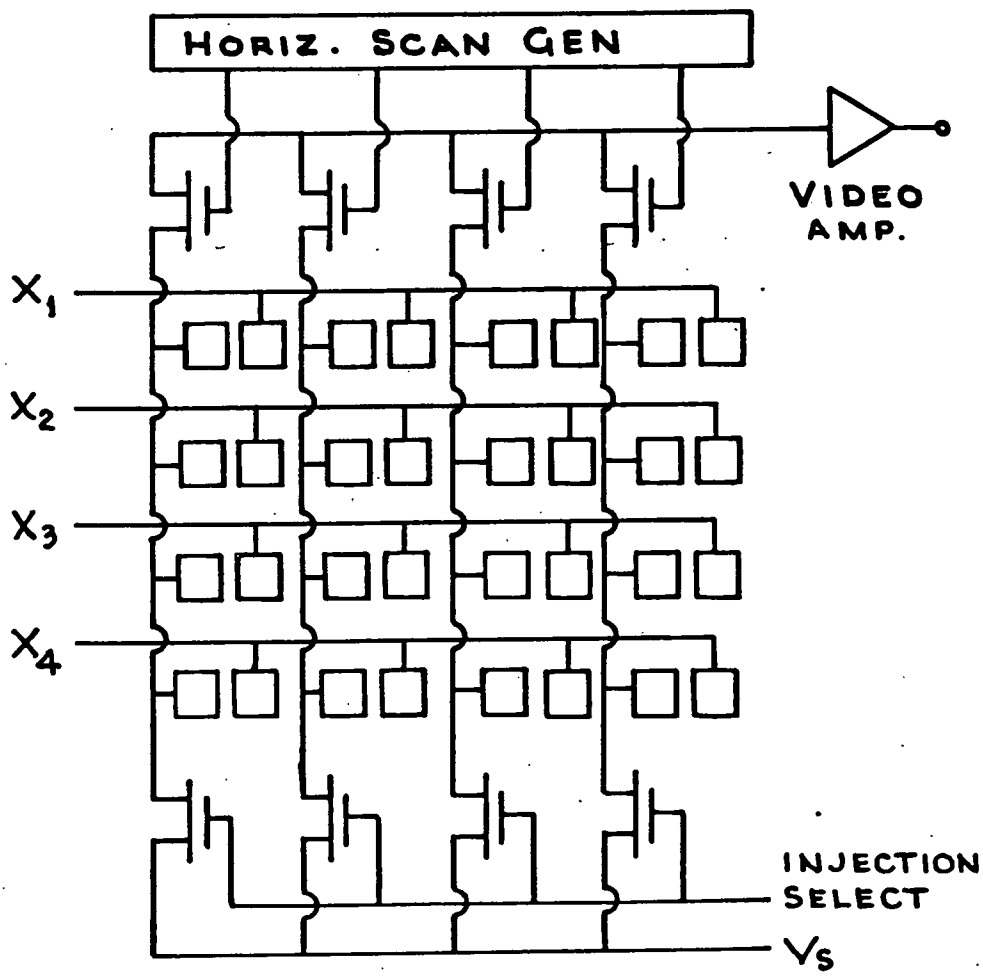


FIG 1:8 PARALLEL INJECTION CID ARRAY

A further development of the CID concept has been demonstrated in General Electric's 244 x 248 element imager [16], which they have termed parallel injection. In this mode, the signal charge at each element is measured by an "intracell" transfer between the two electrodes. After completing readout the array can be cleared of accumulated charge by injection into the substrate (or epitaxial layer). This operation can be illustrated by considering the circuit of a 4 x 4 parallel injection array as shown in Figure 1.8. Initially, all "row" elements have a gate potential applied to them, and the "column" elements are charged to a potential V_s and then allowed to float. A row is selected for readout by removal of the control potential from that row, and all the charges under the electrodes of that row are transferred to the column sites. Since the column lines are floating each experiences a voltage change equal to the signal charge divided by the column capacitance.

The horizontal scan register then connects each column potential (in turn) to the video amplifier. At the end of the line scan, the column potentials can all be returned to zero through the switches S1 to S4, resulting in injection of the charges in the selected row. Alternatively, the row potential can be re-established, returning the signal charge to under the row electrodes. This last option constitutes a non destructive read out (NDRO) and as will be seen, this has considerable advantages for astronomical imaging.

1.2.3. Current Trends in Solid State Imaging

Of the various types of solid state imager described, only three are still currently attracting interest. These are the linear photodiode array, the CCD and the CID.

For applications requiring only single line detectors, the diode array is still in many cases the most attractive choice because of the low cost, ready availability and simplicity.

Devices of up to 2048 elements long are available "off the shelf" [8], and manufacturers are offering complete kits for such applications as industrial process control [17].

For area arrays, photodiode x-y addressed devices are available with moderate numbers of elements (up to about 100 x 100).

For larger area arrays, CCD's take the lead over diode arrays and experimental devices of 800 x 800 have been demonstrated by Texas Instruments.[18] General Electric are still pursuing their CID imager technique and have produced an array of 400 x 300 elements [19].

1.3. An Evaluation of the Suitability of Solid State Arrays for Astronomical Imaging

The astronomical community has shown interest in all three of the detectors listed above, the diode array, the CCD and the CID, and it is of interest to compare their performance and limitations with special reference to astronomical application. The critical tests of performance are spectral response, dark signal, noise, detective quantum efficiency, linearity, lag and detector geometry. These will be treated in turn.

1.3.1. Spectral Response

The Spectral Response of all three devices is, as would be expected, very similar. The response is limited at the red end by the silicon band gap energy E_g, and at the blue end by the opacity of the silicon to short wave-lengths, and by the tendency for electron-hole pairs to recombine with the surface states near the surface of the silicon. Typical quantum efficiency curves obtained from diode arrays[20], CCD's[21,22] and CID's[23] are shown in Figure 1.9. Of the two curves presented here for the CCD, curve (b) shows the interference effects encountered in front illuminated CCD's, due to the polysilicon electrode structures on the front surface. Curve (c) shows the smoother response obtainable from back illuminated CCD's if the device is thinned in the sensor area. This technique is being developed primarily by R.C.A & Texas Instruments and is virtually a necessity if CCD's are to be used in astronomical spectroscopy. The CID shown here has a transparent metal oxide electrode structure and therefore exhibits a higher quantum efficiency than CID's with polysilicon electrodes.

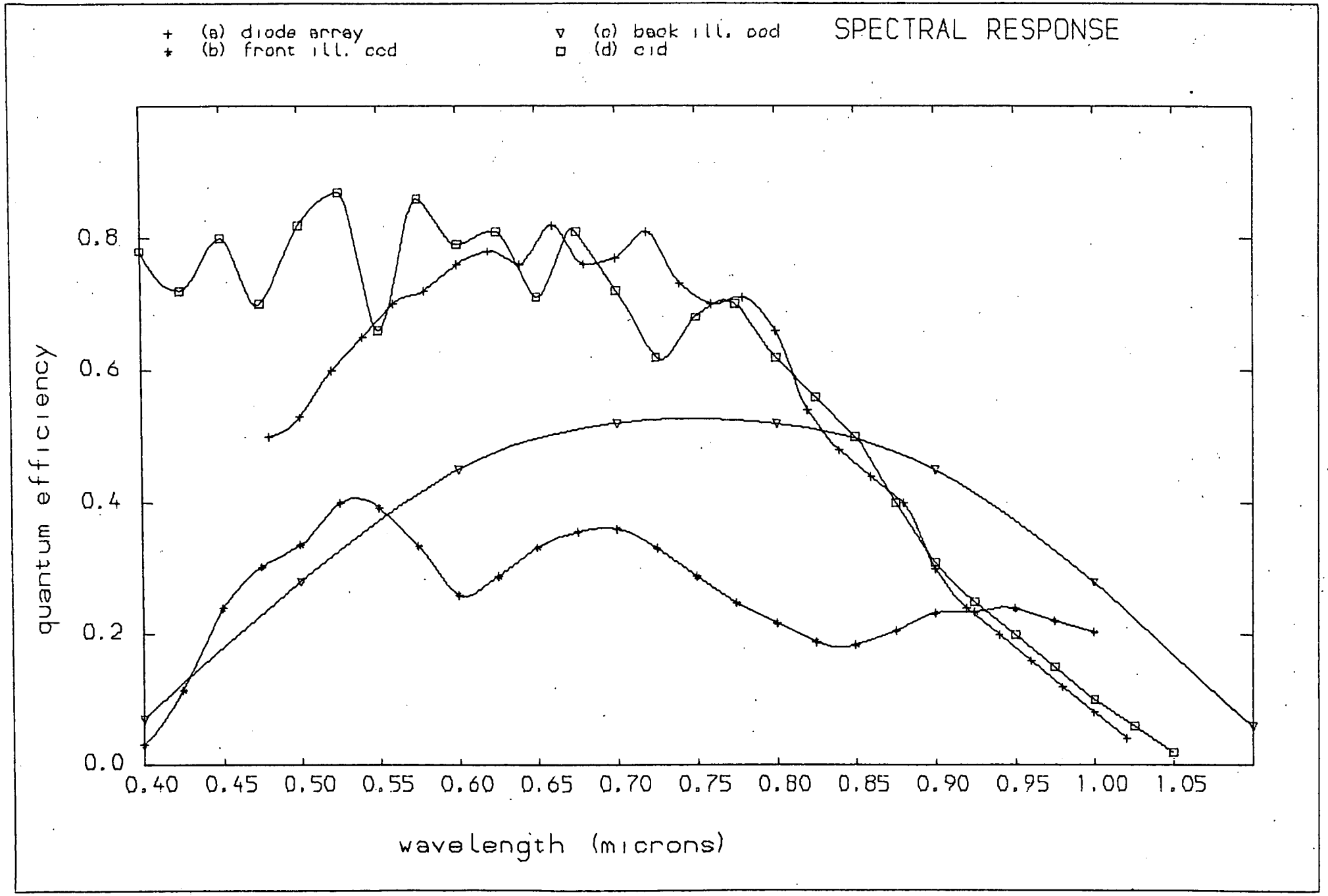


FIG.1.9. COMPARISON OF SPECTRAL RESPONSES

The mechanisms contributing to the spectral response of diode array detectors will be discussed in more detail in the following chapter.

1.3.2. Dark Signal

All silicon devices suffer from dark leakage currents caused by thermally induced electron-hole pair production. In the photodiode, the majority of the signal is generated in the depletion layer region and the leakage current is largely dependent on the junction perimeter. Typical current densities encountered are of the order of $40 \mu A.cm^{-2}$ at room temperature. The leakage current in CCD's and CID's is lower, with a value of $10 \mu A.cm^{-2}$ or better. The dark current decreases by a factor 2 for every decrease in temperature of about 10^{o} C.

The low light levels encountered in astronomy necessitate long total exposure times in order to achieve a reasonable signal-to-noise ratio, and it is generally necessary to reduce the dark signal by cooling in order to be able to achieve suitable integration times.

An early approach to the problem, as used by Tull and Nather [24] with Reticon diode arrays, is to cool the array by liquid nitrogen boil-off to -20^{o} to -40^{o} C.
Following a star exposure, a second, dark, integration is made for an equal time, and this exposure is then subtracted from the first. Three problems arise here. Firstly, observing times are effectively doubled, secondly, there is a need for extremely close control of the operating temperature, and thirdly, there is a shot noise component on the leakage current itself. All these problems can be removed by cooling to below about -100^{o} C, where the thermal leakage is so reduced that it can be ignored completely [25]. Cooling, however, causes a slight decrease in band gap energy E_g, which leads to a reduction in red end response. This will be treated in more detail later.

1.3.3. Noise

It is in the evaluation of noise characteristics of silicon detector arrays that the differing requirements of commercial video imaging and astronomy are best illustrated. Noise sources can be categorised into two types, spatial and temporal, also, and perhaps better, known as fixed pattern noise and random noise respectively. For the commercial video system designer, light levels are usually high enough to dominate a moderate amount of random noise. However, fixed pattern or spatial noise is visually extremely objectionable, resulting in a striped or speckled appearance on the final displayed image [26]. The astronomer however, is able to spend computing time and effort either on-line or in post processing of data to reduce the fixed pattern noise on a signal, whereas the random noise level determines directly the dynamic range available and consequently the exposure times required and the signal-to-noise ratio's achievable.

a) Fixed Pattern Noise

Fixed pattern noise is the term used to describe the way in which individual pixels (picture elements) possess different characteristics. It is a time invariant phenomenon and can, given sufficient calibration data, be "computed out" of the raw signal. It has three forms, offset variation, responsivity variation and synchronous noise.

Even for an array in the dark, the output signal is not identical for all elements, and this is know as offset variation. In most types of array this is chiefly due to variations in thermal leakage current. As described above, in some applications this can be reduced by cooling and also by subtraction of "dark integrations".

It can also be reduced by a technique known as correlated double sampling [27], originally introduced to reduce reset noise (a random noise source).

This technique measures the signal level on each element before and after reset during a scan.

Variations in individual pixel responsivities are caused by differences in quantum efficiency and device geometry. Responsivity variation can be corrected for by comparison with an integration on a well defined source, such as a flat field exposure.

Synchronous noise, the third form of spatial noise, arises from capacitative feed-through from the addressing circuits, and appears in the form of spikes on the output wave-form at times when the clocks change states.

CCD imagers are much less prone to synchronous noise than are diode arrays and CID's because there is only a single clock electrode from which coupling to the output gate can occur. In diode arrays, synchronous noise can be minimised by subtraction of successive scans [28].

With the exception of synchronous noise, diode arrays, CCD's and CID's all have similar sources and levels of fixed pattern or spatial noise. As mentioned above, however, for the astronomer it is not the spatial noise which ultimately limits performance, but the random noise.

(b) Random Noise

Noise sources in diode arrays will be discussed more fully in the next chapter. The noise sources of major interest when comparing arrays are the amplifier noise arising from the video line capacitance, capacitor reset noise and dark current shot noise. The shot noise on the dark current is not a significant noise source if the array is cooled and will therefore not be described further.

The video line capacitances of CID's and diode arrays are high (and related to the number of pixels) because of the addressing structure, and this leads to high levels of amplifier noise when compared with CCD's which have an output capacitance due to a single element only.

Capacitor reset noise is a noise caused by the uncertainty in the level to which a capacitor is recharged, and will be described in greater detail in the following chapter in connection with diode arrays. It occurs in all three types of array, but can be minimised by correlated double sampling as mentioned above, a technique applicable to CCD's [27] and CID's [16], and, as will be shown, to some types of diode array.

Typical reported noise figures for silicon imaging arrays show the inherently higher noise levels of diode arrays and CID's. Order of magnitude estimates are 1000 electrons for a photodiode array, 500 electrons for a CID and 100 electrons for CCD's. It may be possible to approach a figure of 10 electrons for cooled CCD's using buried channel technology. The implications of random noise levels can be seen when the detective quantum efficiency is considered.

1.3.4. Detective Quantum Efficiency

One of the most useful figures of merit for an astronomical detector is the Detective Quantum Efficiency (DQE).

The DQE can be defined as :-

$$DQE = \frac{(S/N_o)^2}{(S/N_i)^2}$$

where

S/No = signal to noise ratio of the output signal,

and

S/Ni = signal to noise ratio of the input signal.

The method of calculating the DQE is described in Appendix A. Several interesting points arise.

(a) Figure 1.10 shows the DQE plotted against total exposure for silicon detectors with noise levels of 1000 e^- (representing a diode array), 500 e^- (a CID), 100 e^-(a CCD), and 10 e^-which is representative of the limit obtainable with CCD's. The DQE is calculated at a wavelength of 7000 Å and is compared with the DQE of a photon counting system employing a S-20 photocathode. In a photon counting system the incoming photon is converted by a photocathode and the resultant photoelectron is accelerated through say 20 - 40 kV. When detected, the signal produced by the photoelectron is greatly in excess of any detector readout noise and consequently the DQE approches the quantum efficiency of the photocathode. DQE is limited to about 0.8 of RQE by multiple events and backscattering of electrons. As can be seen from the graph, the photon counting system has a superior performance at low light levels. At high light levels (or long exposures) the higher quantum efficiency of the silicon detector dominates.

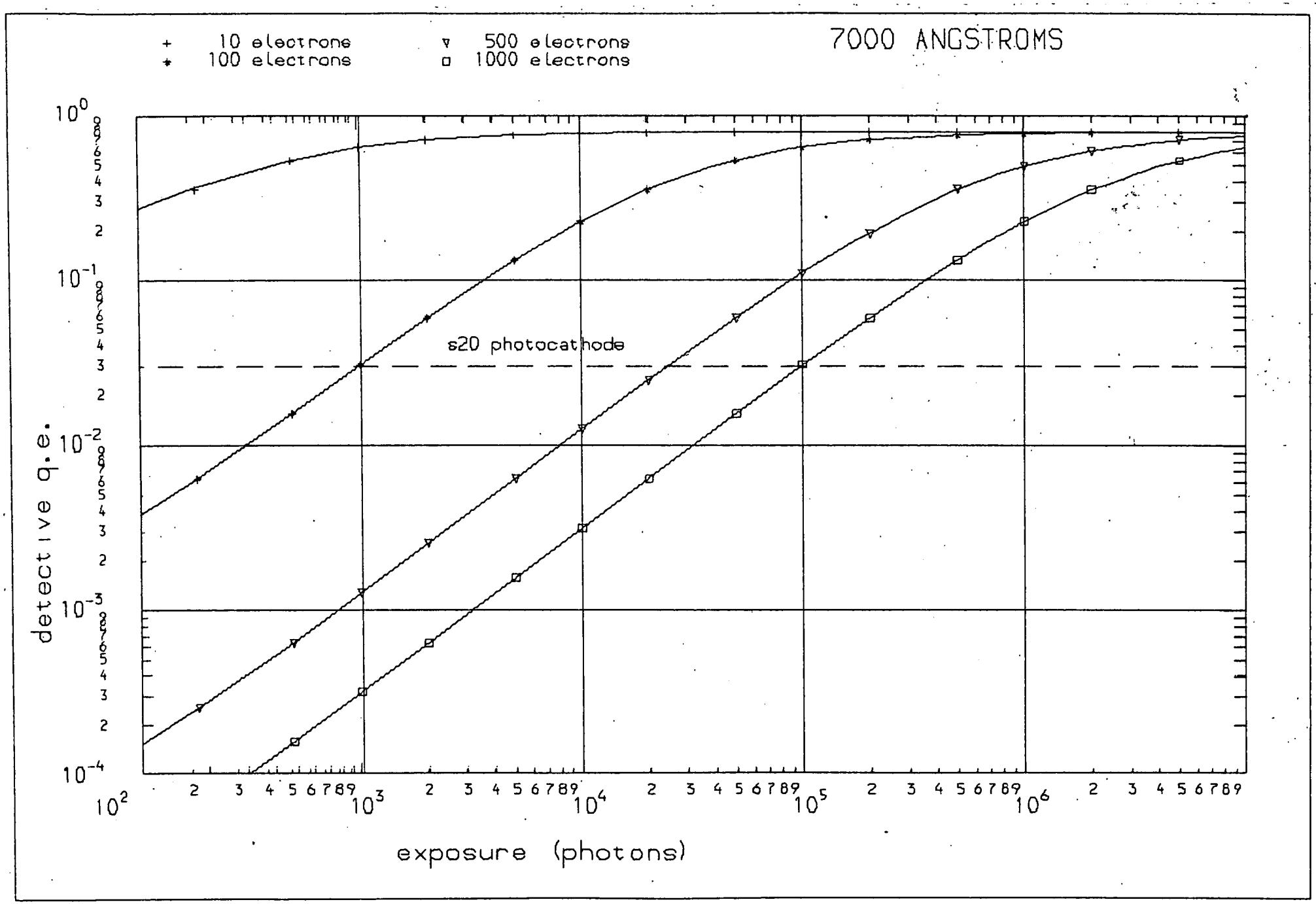


FIG.1.10. PREDICTED DQE FOR SOME TYPICAL NOISE LEVELS

For a detector with a noise level of 1000 e^- this break point comes at an exposure of 10^5 photons. In Figure 1.11, this "break point" exposure is plotted as a function of the readout noise of the detector for different wave-lengths. There is of course no reason why a solid state array should not be used to detect the photoelectrons in a photon counting detector, as will be described later.

The usefulness of a detector with a non destructive readout (NDRO) facility can be seen in Figure 1.12. By averaging successive non destructive readouts at the end of an exposure, the random component of readout noise can be reduced. The graph shows the improvement possible in DQE for a detector noise of 500 e^-, and a wave-length of 7000 Å, for 5,20 and 100 samples of the signal

Note that the reduction in noise assumes that there is no correlation in random noise between samples.

1.3.5. Linearity and Dynamic Range

It appears that there are no inherent sources of non-linearity in the signal generation process in either diode arrays, CID's or CCD's. In CCD's charge transfer inefficiency is signal dependent and can cause non-linearity at low charge levels. The transfer inefficiency is largely due to the existence of traps and can be reduced by the use of a "fat zero.". The fat zero is a technique by which sufficient "background" charge is maintained in the array elements to fill the traps even in the absence of photosignal.

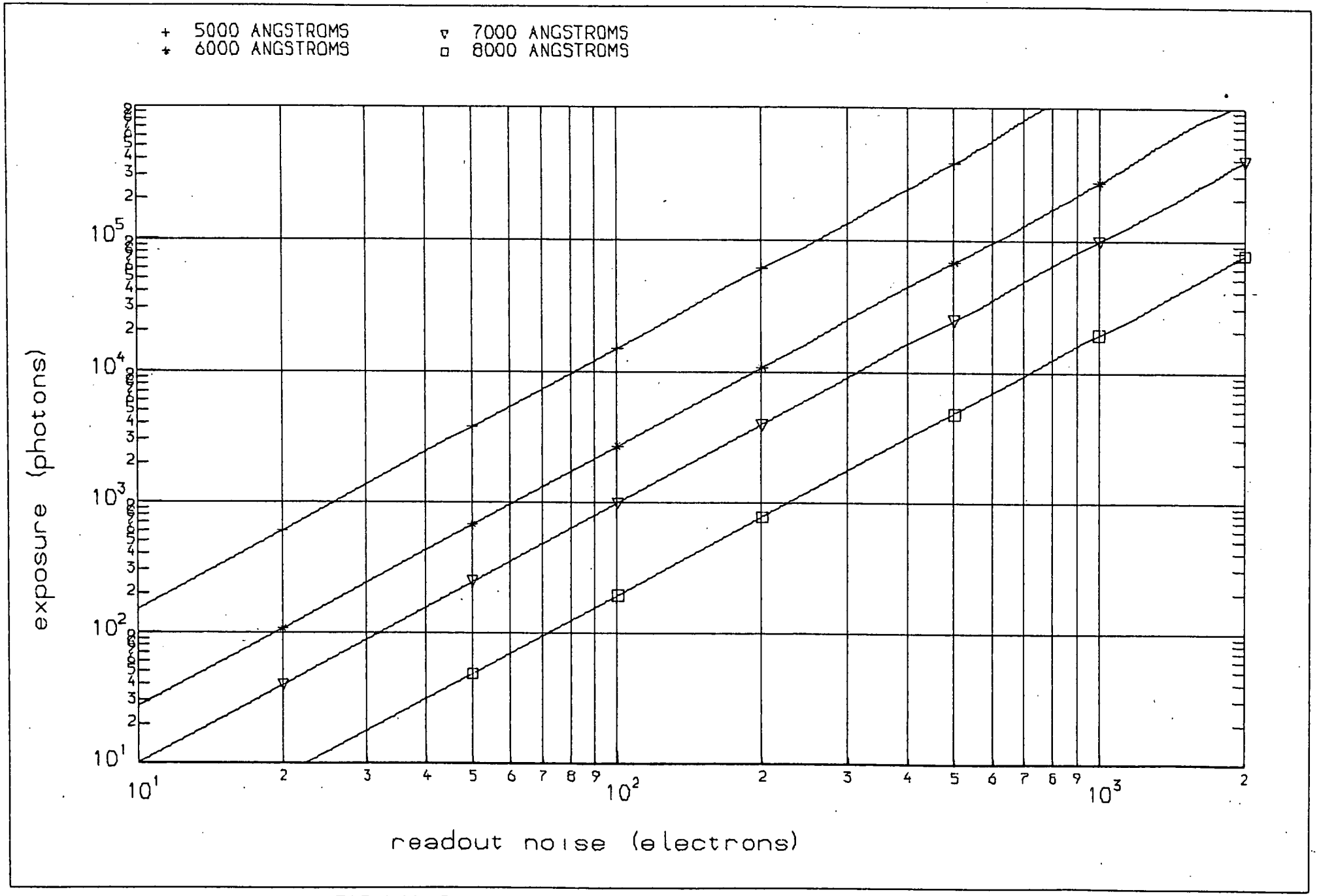


FIG.1.11. BREAKPOINT EXPOSURE - PHOTODIODE vs, S20

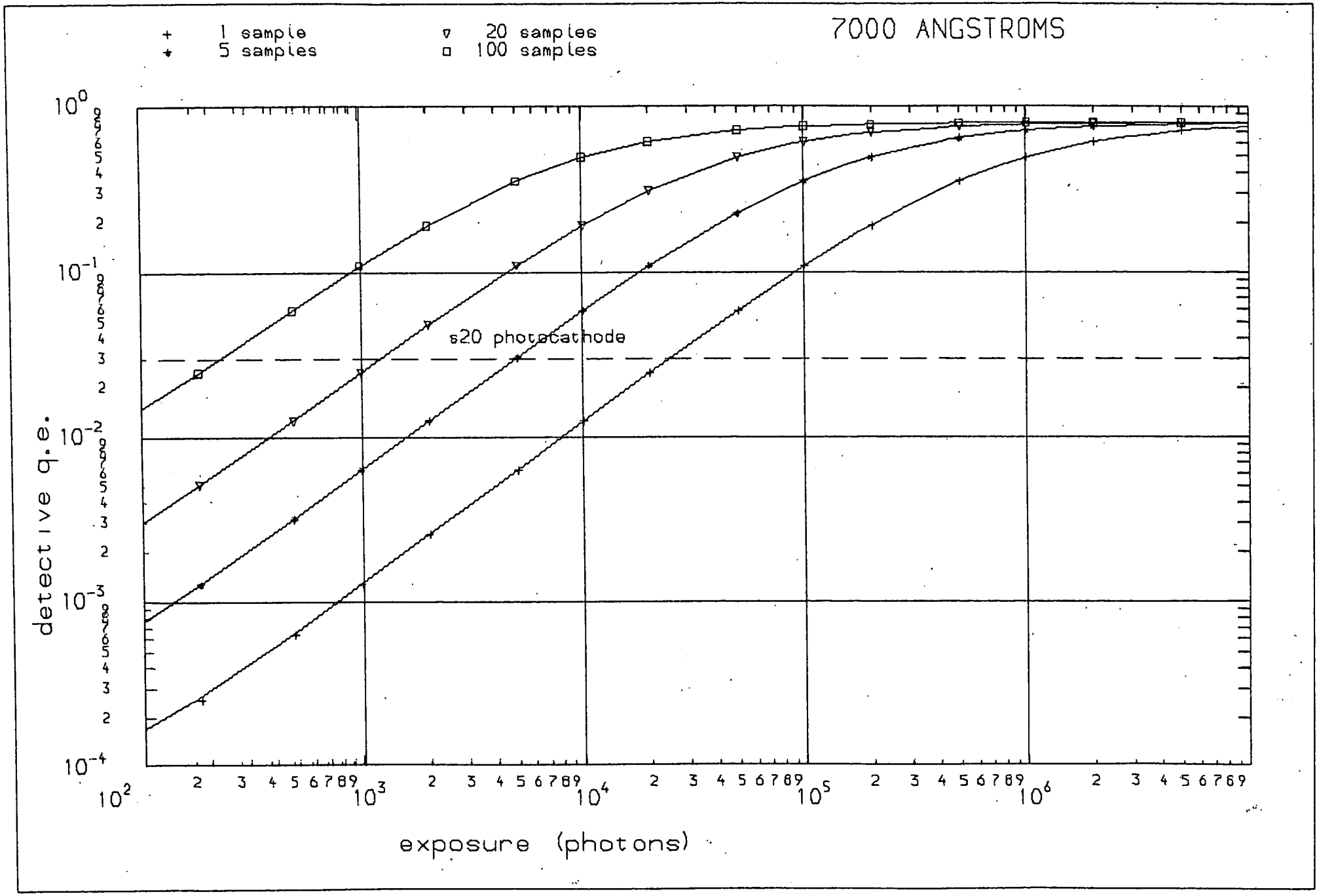


FIG 1.12 PREDICTED DQE - NON DESTRUCTIVE READOUT

Saturation levels are determined in diode arrays by the diode capacitance and in CCD's and CID's by the site storage capacity. For a photodiode of 1pF capacitance biased to 5V, the saturation level will be about 3×10^7 electrons Coupled with a noise level of 1000 electrons this represents a dynamic range of 3×10^4. For a CCD the saturation level is that which reduces the surface potential to zero, and for a 20μm x 20μm element this can be shown to be about 0.3×10^7 electrons. Considering the lower noise level of about 100 electrons, the CCD has a similar dynamic range to the diode array.

1.3.6. Lag

Lag is the term used to describe any tendency for an imager to retain a part of the image from a preceeding frame or readout and superimpose it on the current frame.

In diode arrays, this could occur due to incomplete recharge through the multiplexing transistor, and in the CCD from charge transfer inefficiency. In practical imagers, such problems have generally been found to be negligible, and the lag is usually quoted as zero. With the wide dynamic range of exposures encountered in astronomy even very small lag levels can be a problem, for example, when changing to a faint star after a calibration exposure on a bright standard star. Tull et al [24], found for example that because of the long time constant in their preamplifier feed-back loop, a residual charge of 1% was present after recharge from saturation. Even so, this class of detector suffers very much less from lag than most t.v. type detectors which use an electron beam for readout.

1.3.7. Detector Geometry and Spatial Resolution

Of interest to the astronomical user is both the total number of pixels in a detector and the geometry of the individual pixels.

For the observation of extended objects such as galaxies, it is obvious that area arrays are required, and with as many pixels as possible. This dictates the use of CCD's or CID's.

In astronomical spectroscopy, however, the image to be detected is elongated and very narrow, with the information content along the long axis, and the linear diode array appears to be eminently suitable for such applications. Single line CCD or CID arrays might appear to offer the same geometrical characteristics but with reduced noise. However, most commercially available single line CCD arrays have element sizes in the region of 20μm x 20μm, with a trend towards reducing this. Whereas this gives high resolution in the direction of dispersion, it poses considerable optical and mechanical problems of accurate alignment of the image onto the array. Diode arrays are now becoming available with more suitable element geometries, such as the Reticon "H' series with a centre-to-centre diode spacing of 15μm and a diode width of 300μm.

The spatial resolution of silicon detector arrays is approximately the geometrical size of the element at short wave-lengths where the absorption depth is small. At longer wave-lengths the carriers generated deep in the substrate can easily diffuse to adjacent elements, thus introducing crosstalk between elements. Studies have recently been made at Hewlett Packard [29] into reducing this crosstalk by incorporating subsurface electric fields that accelerate the carriers towards or away from the surface, thus minimising the chances of collection by a neighbouring site.

So far the discussion of the application of these silicon detectors has been restricted to use in a light integrating mode. There is a second, very powerful technique of imaging useful particularly at low light levels, known as image intensification. Image intensifiers alone are not strictly detectors, but can be combined with a variety of optical and electron detectors.

1.4. The Use of Solid State Arrays for Intensified Imaging

The concept of the intensified detector has been in existence for a long time and has been applied to most forms of detector from the eye upwards.

Two modes of intensification are possible. The first retains the principle of detecting photons and uses an image intensifier comprising an input photocathode, an amplifying tube and an output phosphor. A conventional detector records the light pulses from the output phosphor. Variants include devices with fibre optic input and output windows to facilitate cascading of tubes, and image tubes with various magnetic and electrostatic focussing schemes. Detectors employed to record the light output range from photographic plates to television type sensors. The principle shortcoming of such systems is the degradation introduced by the output phosphor and its coupling lens or fibre optic window.

In the electronographic type of intensifier the output phosphor is eliminated and the detector is located either inside the image tube or behind a thin, usually mica window. The detector records directly the impact of the photoelectron which typically has an energy of 20 - 40 KeV after acceleration. When used with a photographic emulsion this has an added advantage, in that when used in this fashion the emulsion has very much improved linearity and dynamic range, and does not suffer reciprocity failure [30].

Silicon detectors are attractive for use in such a mode since high energy electrons incident on a silicon detector will liberate one electron-hole pair for every 3.6 eV of energy lost. Thus a single 20 KeV electron stopping in an array will generate a signal of about 6000 electrons, which is in excess of the readout noise of virtually all silicon array detectors. Before the advent of self scanned arrays such as diode arrays, CCD's and CID's, "digital image tubes" employing silicon diode readout had been constructed. These tubes, known as Digicons[31] have a leadout from each diode and the external electronics consists of one channel of discriminator and scaler for each diode, with sequential readout of the scalers by computer. Digicons with greater than 200 elements have been manufactured. With the development of self scanned arrays, the possibility of incorporating these into a digicon was realised. Such "self scanned digicons" have been manufactured by Electronic Vision Corporation using diode arrays (Reticon 1024 element linear devices) and 100 x 100 element Fairchild CCD's.[32]

Two modes of operation are applicable when such detectors are used in the intensified mode. Photon counting can be achieved by simple discrimination of the output signal (photon/no photon). Some resolution of multiple photon events is achievable with multi level discrimination. The count rate per channel will be limited by the scanning rate. Alternatively, the charge can be integrated on the diode and an analog measurement made of the total charge collected in each channel. Systems employing Reticon based Digicons operated in this fashion have reached within 15% of shot noise limited performance, i.e. DQE 0.75 RQE[33].

Problems have been encountered with radiation damage when using digicons, which has the effect of increasing the dark current. This has been minimised with diode arrays by protectively masking the scanning circuits, but this is not possible with CCD's, which can have a life expectancy of as little as 10^7 electrons/element[34]. Damage mechanisms are complex and still under investigation, but it has been shown that under some circumstances damage can be reversed by an annealing process involving bombardment with low energy electrons.[35] It is also hoped that backside illuminated CCD's will be more robust, since it appears to be the Si-SiO_2 interface at the top surface that is most susceptible to damage.

1.5. Summary

It has been shown that three types of self scanned silicon imager have emerged from the many projects followed in the late 1960's and early 70's, namely the MOS diode array, the charge coupled device and the charge injection device. They have the advantages over other existing detectors of higher quantum efficiency, absolute geometrical stability, zero lag and good linearity. They are especially useful in the near infra-red region where most photocathodes have reached their limit of usefulness.

When used in the direct mode they are unable to compete with photon counting systems at very low light levels, but at moderate and high levels their high quantum efficiency makes them attractive, especially at near infra-red wave-lengths.

The importance of reducing readout noise has been seen, and two techniques employed to reduce this have been mentioned, namely correlated double sampling and non destructive readout. Neither technique is applicable to conventional MOS arrays of the Reticon type.

This thesis describes the development of a novel diode array incorporating both these techniques and also on-chip pre amplification.

It is necessary to consider in more detail the principles behind diode array operation.

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CHAPTER TWO

A Study of Linear MOS Photodiode Arrays

The operational characteristics of an MOS photodiode array can largely be separated into those relating to signal generation and those concerned with readout of the stored charge, and these will be treated in turn. It will be seen that in fact the mode of readout can significantly affect the signal generating process, and the effect on overall performance will be shown. The influences of these characteristics on the development of diode arrays will be discussed.

2.1. Signal Generation

All photodiode array detectors of the type described here are based around a reverse biased p-n photodiode. For the purpose of this discussion it will be assumed that the diode is a p^+ type diffusion in an n-type substrate, which is usually the case.

The signal in a photodiode of this type has two origins. There is a photocurrent, generated by light incident on the diode, and a thermal leakage current. Both have the same sign and are "leakage" currents which tend to discharge the junction capacitance of the reverse biased diode. The characteristics of these two components will be described as a function of the physical properties of the junction, the intensity and wave-length of the incident light, the reverse bias voltage applied to the diode and the operating temperature.

2.1.1. Photocurrent and Quantum Efficiency

If a photon of sufficient energy is incident on silicon, it is absorbed and the energy is given up to excite an electron from the valency band into the conduction band. Excess energy and momentum appear in the form of a phonon. Such excitation can also be achieved thermally. The optical absorption and subsequent production of a photon are shown in Figure 2.1. When in the conduction band, the electron and the associated hole are free to contribute to the conductivity of the material. The electron will eventually recombine with a hole in the valency band.

Only incident photons with an energy greater than E_g the band gap energy, are capable of causing such transitions. Photons with an energy $< E_g$ will not be absorbed. For silicon at room temperature E_g = 1.09 eV, which corresponds to a photon wavelength of 1.1 μm.

In a reverse biased diode, the photocurrent is generated by the diffusion of the minority carriers towards and across the junction. In a typical photodiode the junction depth is 1-2 μm. The depth at which the photon is absorbed is wave-length dependent.

Consider an incident photon rate F_o entering the surface of the silicon. The density of electron hole pairs created at a depth x is :-

$$\Delta p = F_o \alpha \exp(-\alpha x) \qquad (2.1)$$

for n-type material, where

Δp = concentration of excess holes

and α = absorption co-efficient.

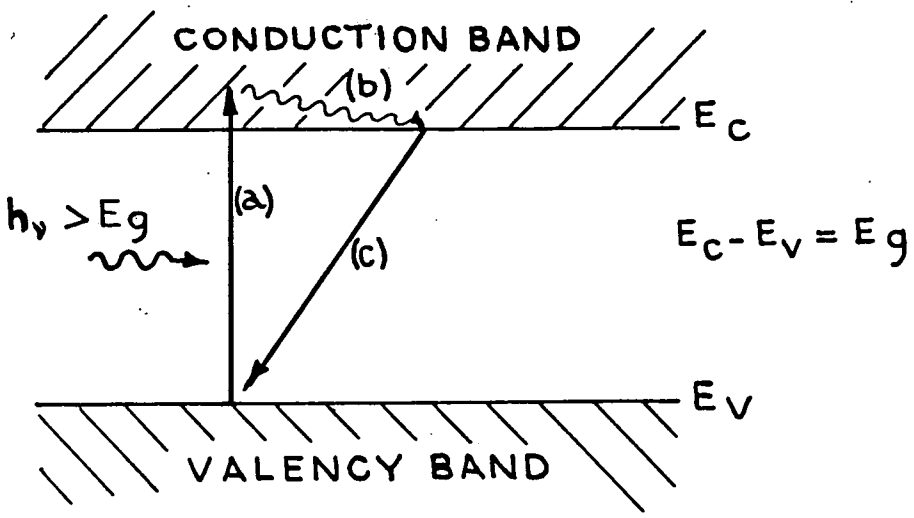


FIG 2.1 OPTICAL ABSORPTION IN A SEMICONDUCTOR

(a) EXCITATION OF ELECTRON TO CONDUCTION BAND

(b) EXCESS ENERGY RELEASED TO LATTICE AS A PHONON

(c) RECOMBINATION

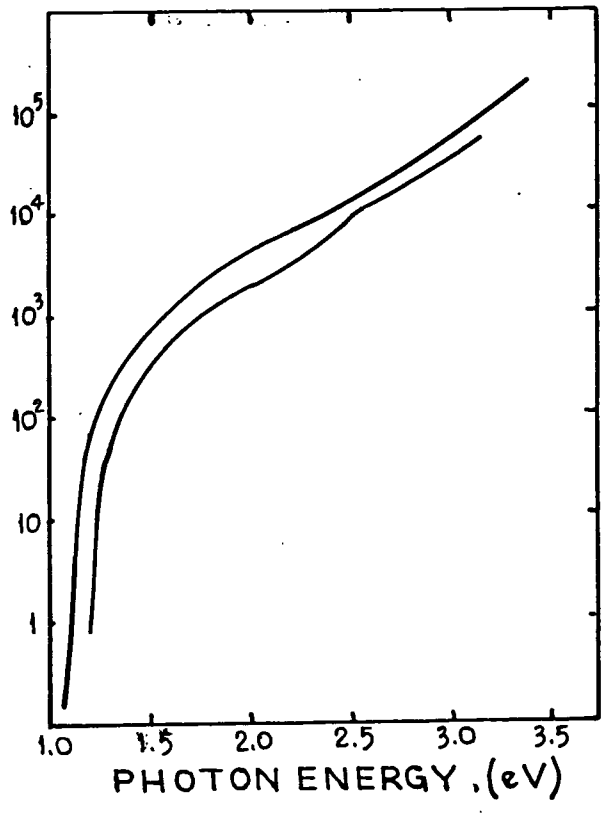


FIG 2.2 ABSORPTION COEFFICIENTS IN SILICON (AFTER DASH & NEWMAN)

The absorption co-efficient of silicon is shown as a function of wave-length in Figure 2.2. for room temperature ($300^{o}K$) and liquid nitrogen temperature ($77^{o}K$) [1]. In the region of interest, the absorption depth ($1/\alpha$) varies from about 0.1 μm at wave-lengths of 0.4 μm to 96 μm at a wave-length of 1.0 μm at room temperature. Thus carriers are generated throughout the depth of the diode, in the bulk of the substrate at long wave-lengths, in the depletion layer for intermediate wave-lengths, and in the p^{+} diffusion at shorter wave-lengths. The three components of the photocurrent that correspond to the absorption in these regions can be treated separately.

It is convenient to treat the photocurrent as being the sum of the individual photocurrent contributions from these three regions. Thus :-

$$J_T = J_{dep} + J_{sub} + J_{p+}$$

where J_T is the total photocurrent density,

J_{dep} is the contribution from the carriers generated in the depletion region,

J_{sub} from those generated in the substrate and

J_{p+} from those generated in the p+ type diffusion.

Also, the photocurrent can be related to the quantum efficiency by :-

$$J_T = qF_o\eta$$

where q is the electronic charge
η is the quantum efficiency
and F_o is the incident photon rate

The contribution from the three absorption regions can be expressed as quantum efficiency components, thus :-

$$J_T = qF_o\ (\eta_{dep} + \eta_{sub} + \eta_{p+}) \qquad (2.2)$$

This is the most convenient form in which to work, since the properties of the three regions can be described independently of variables such as F_o, the incident photon rate.

The derivations [2] of the quantum efficiency components are lengthy and will not be included here. The expressions will be quoted, and the physical significance of the various terms will be described.

(a) The component of quantum efficiency from the depletion layer is given by :-

$$\eta_{dep} = (\exp(-\alpha x_{jp})\ (1 - \exp(-\alpha d)) \qquad (2.1\ (a))$$

where x_{jp} = depth of depletion layer edge in p-type material (see Figure 2.3.)

d = depletion layer width
($= x_{jn} - x_{jp}$)

It is interesting to note that this expression contains absorption terms only, and no terms representing the recombination of carriers. The electrostatic fields inside the reverse biased depletion layer are so high that any carriers generated therein are rapidly drifted out in a time very much less than the carrier life time, and thus recombination is negligible.

(b) For the n-type substrate, the component of quantum efficiency is given by :-

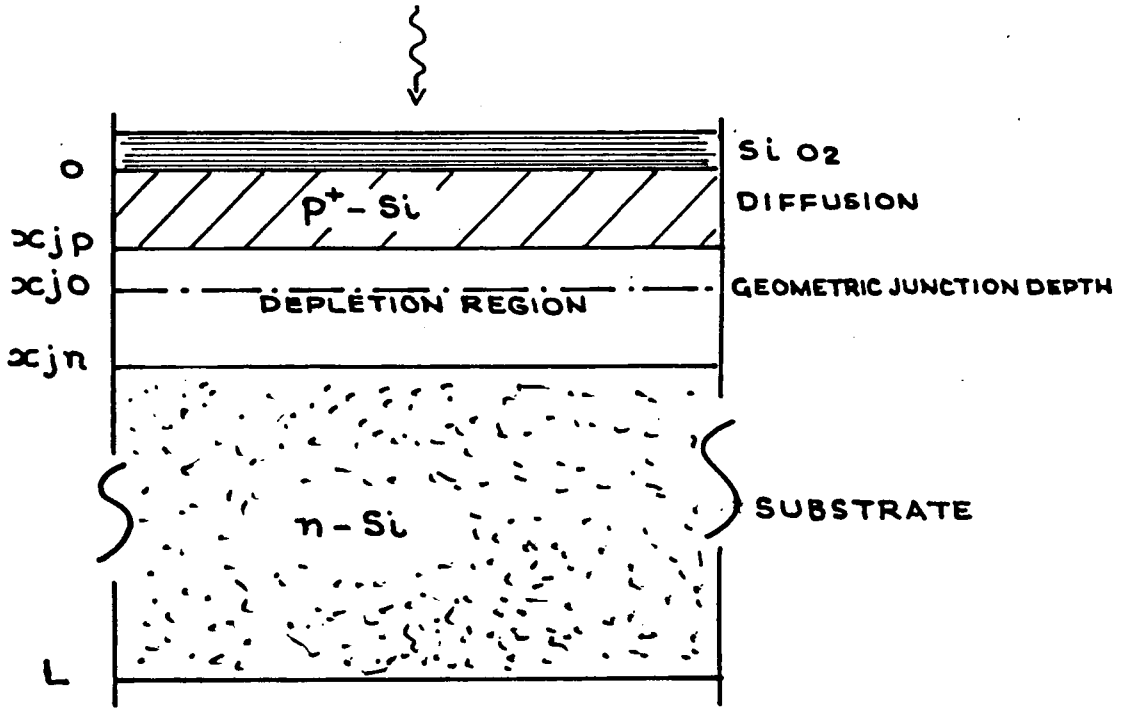


FIG 2.3 ONE DIMENSIONAL
P^+ - N PHOTODIODE

(2.3(b))

$$\eta_{sub} = \frac{\alpha L_p^2}{\alpha^2 L_p^2 - 1}\left[\alpha \exp(-\alpha x_{jn}) + \frac{\exp(-\alpha L) - \exp(-\alpha x_{jn})\cosh(L-x_{jn}) / L_p}{L_p \sinh((L-x_{jn}) / L_p)}\right]$$

where L_p = diffusion length of holes in the n-type material

L = total depth of substrate (see Figure 2.3.)

For an infinitely deep substrate (i.e. as $L \to \infty$) this component becomes proportional to L_p at longer wave-lengths. The physical significance of this is that only carriers which are generated within about one diffusion length of the depletion layer boundary contribute to the photocurrent. Thus for good red response, high lifetime (i.e. large diffusion length) silicon is essential.

(c) For the p^+ diffused region, surface recombination becomes significant and limits the quantum efficiency at the blue end, as carriers generated near the surface recombine before they can diffuse to the junction. The partial quantum efficiency of this region is :-

$$\eta_{p+} = \frac{\alpha L_n^2}{1 - \alpha^2 L_n^2}\left[\alpha \exp(-\alpha x_{jp}) - \right.$$

(2.3 (c))

$$\left. \frac{1}{L_n} \frac{L_n (s+D_n) - \exp(-\alpha x_{jp})(sL_n \cosh(x_{jp}/L_n) + D_n \sinh(x_{jp}/L_n))}{s L_n \sinh(x_{jp}/L_n) + D_n \cosh(x_{jp}/L_n)}\right]$$

where L_n is the diffusion length for electrons

s is the surface recombination velocity

and D_n is the diffusion co-efficient for electrons

The boundary depths x_{jp} and x_{jn} are a function of the reverse bias voltage applied to the junction and can be expressed as [3].

$$x_{jp} = x_{jo} - \frac{2\epsilon (V_c + V)}{q} \quad \frac{N_d}{N_a (N_a + N_d)} \qquad (2.4\ (a))$$

for the boundary in the p^+ diffused region, and

$$x_{jn} = x_{jo} + \frac{2\epsilon (V_c + V)}{q} \quad \frac{N_a}{N_d (N_a + N_d)} \qquad (2.4\ (b))$$

for the boundary in the n-type substrate, where

x_{jo} = physical junction depth

ϵ = permittivity of silicon
V_c = equilibrium contact potential
V = reverse bias potential
N_a = acceptor density
N_d = donor density

Figure 2.4. shows the partial and total quantum efficiences calculated from the above, for a typical p-n junction with a junction depth of 1.5 μm, a substrate thickness of 200 μm and a reverse bias potential of 10V. Other parameters used in the calculations are listed in the figure.

For any given p-n junction, two external variables will affect the photoresponse curve, these being bias voltage and temperature.

As the reverse bias changes, it is apparent from Equations (2.4.) that the boundary depths will vary with reverse bias potential. It is also apparent that the changes will be greater inside the material with the lower doping density, in this case the n-type substrate. Thus as the bias voltage increases, the depletion region extends further into the substrate, boosting the partial quantum efficiency of this region.

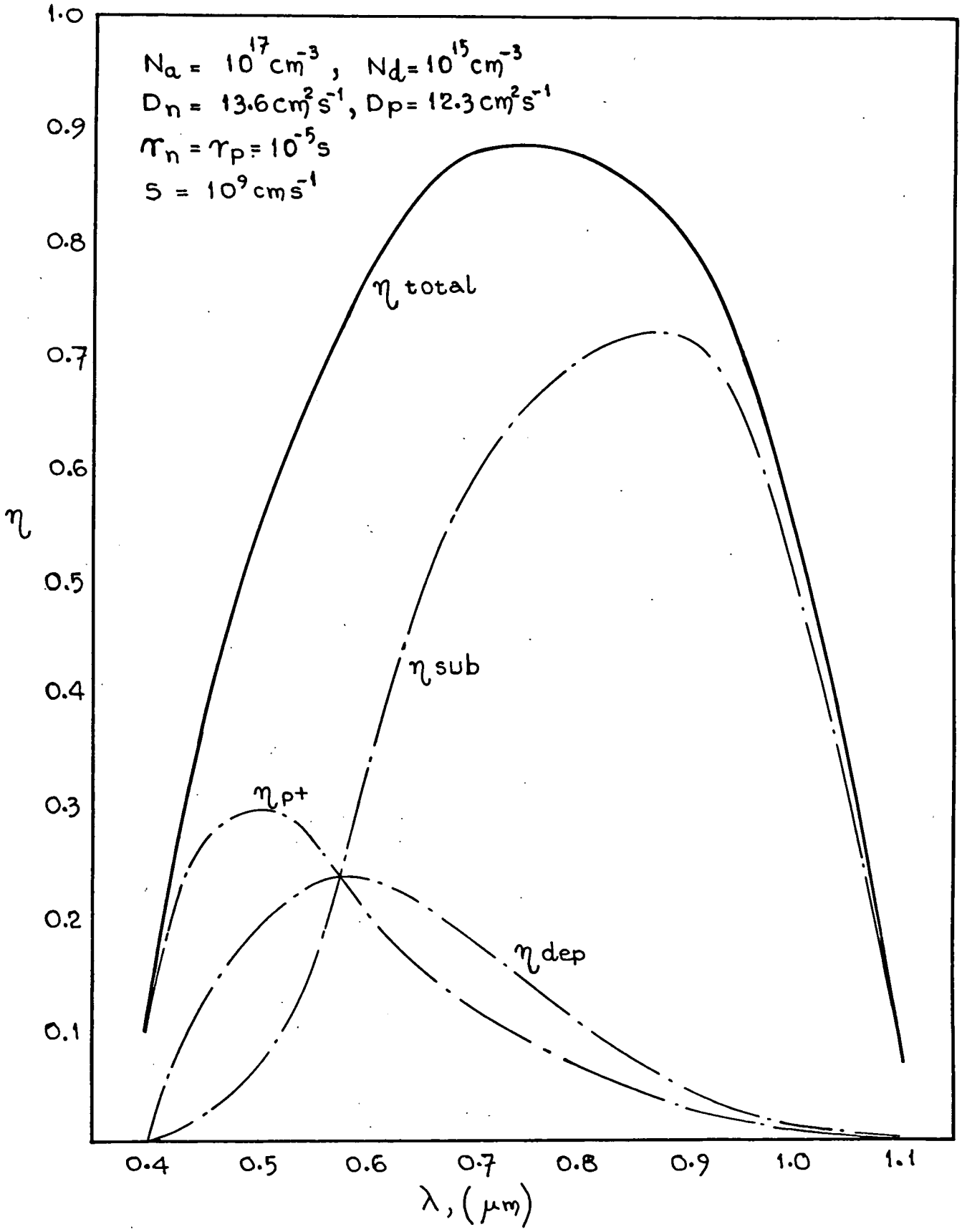


FIG 2.4. CALCULATED PARTIAL QUANTUM EFFICIENCIES FOR A Si PHOTODIODE WITH $x_{jo} = 1.5 \mu m$, $L = 200 \mu m$, $V = -10V$

How significant this increase will be to the overall response depends upon the parameters of the particular device. For example, the red response of the junction of Figure 2.4. is strongly dominated by the substrate contribution and will not be grossly affected.

Of course, some extension of the depletion region into the p^+ diffusion will also occur at higher voltages. Geary has suggested [4] that this will improve the blue response, but such an effect has not yet been reported. Temperature changes have a significant effect on response, especially at the red end of the spectrum.

As temperature is reduced, the mean free path of lower energy photons increases dramatically, and the band gap energy E_g increases. There is a twofold effect at low temperatures. Firstly, low energy (red) photons will be absorbed deeper in the substrate than before, and will have less chance of diffusing to the depletion layer without recombination, lowering the partial quantum efficiency of the substrate at the red end. Furthermore, because of the increased band gap energy, the cut off wave-length is also reduced. The variation in band gap energy with temperature is shown in Figure 2.5 [5]. At room temperature ($300^{\circ}K$) cut off wave-length for silicon is 1.11 μm, and reduces to 1.07 μm at $77^{\circ}K$.

The decrease in red end response at low temperature has been measured by Vogt et al [6] for a Reticon diode array, and the results are shown in Figure 2.6.

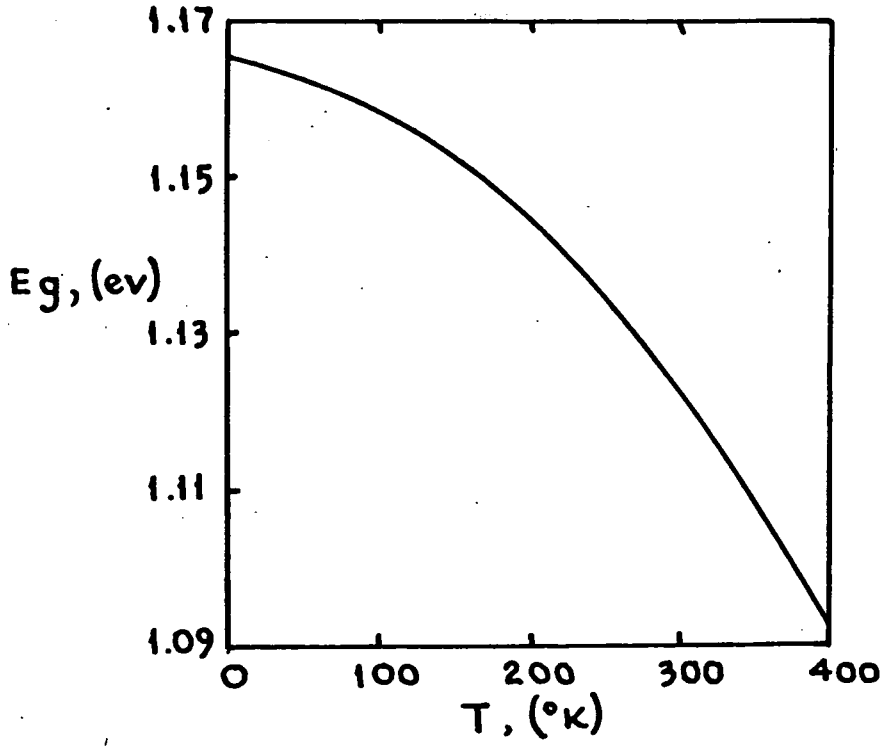


FIG 2.5 VARIATION OF Eg WITH TEMPERATURE (AFTER SMITH)

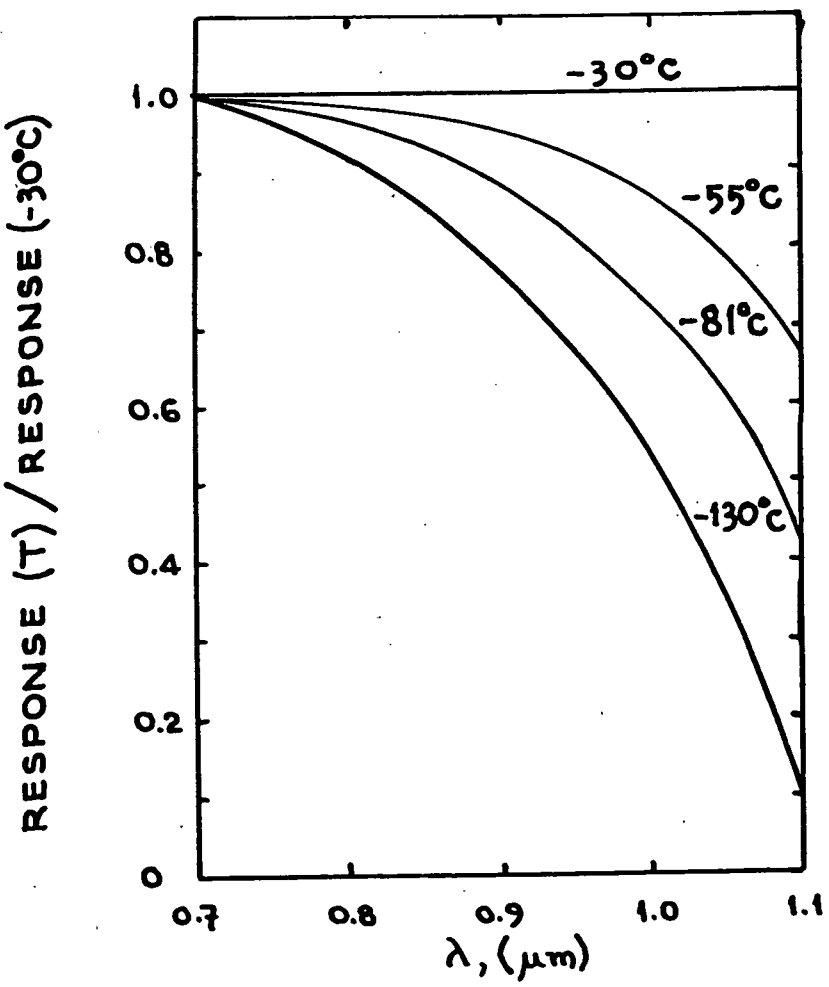


FIG 2.6 DECREASE OF RED RESPONSE WITH COOLING (AFTER Vogt et al)

So far, the calculation of photocurrent has been based on the incident photon rate entering the surface of the silicon. The way in which this is related to the incident flux on the detector is modified by reflection and interference at the surface.

The refractive index of silicon is approximately 3.9 and the reflection co-efficient R at the surface can be calculated from [7]:-

$$R = \left[\frac{n_{Si} - n_{air}}{n_{Si} + n_{air}} \right]^2 \qquad (2.5)$$

This gives a co-efficient of R = 0.35

If the presence of the thin ($\sim 3\mu m$) silicon dioxide surface layer is considered, the situation is improved slightly.

Silicon dioxide has a refractive index of 1.45, which gives reflection co-efficients of 0.034 and 0.21 at the Air-SiO_2 and SiO_2-Si interfaces respectively. Thus only about 80% of incident light is expected to enter the surface of the silicon. This agrees with the peak quantum efficiences of about 0.8 observed in Figure 1.1.

The thickness of the substrate (several hundred microns) used in diode arrays eliminates the problems of interference in the substrate which have been encountered with silicon targets in electron-beam addressed tubes. However, the silicon dioxide surface layer is typically a few microns thick, and it is possible for interference to occur between incident light and light reflected from the SiO_2-Si boundary. Such interference effects are visible as modulations of the quantum efficiency in Figure 1.9.

2.1.2. Thermal Leakage Current

In classical p-n junction theory, it is assumed that thermally generated carriers contribute to the leakage current if they are generated within one diffusion length of the depletion layer boundary. The width of the depletion region,d, is usually small in comparison with the diffusion length and thus carrier generation is negligible inside this region. Thus the leakage current would be largely independent of bias voltage.

The above treatment assumes that all electron-hole pair generation is due to transitions from the valency band to the conduction band. However, in the depletion region, the scarcity of free carriers can lead to a net generation of carriers from recombination centres.

Normally, the emission of carriers from a recombination centre is balanced by corresponding capture processes, but in the reverse biased depletion region the lack of free carriers, and the speed with which generated carriers are swept out, inhibit the recombination process. Generation from such centres is most significant in materials with a large energy gap, such as silicon, for which band-to-band transitions are rare. Narrow gap materials such as germanium however, follow the classical theory closely.

The implication of this is that for silicon diodes, the leakage current is dependent on the width of the depletion layer (and thus on the bias voltage), and also on the number of trace element impurities and lattice defects.

It has been found that three geometric properties of the diode contribute to the leakage current, these being :-

(a) diode area
(b) diode periphery
(c) number of corners

Table 2.1. shows the leakage currents measured by Chamberlain [8] for a 1.4 μm deep p-type diffusion. He found that the peripheral leakage currents can be reduced by covering the junction with an aluminium ring electrically connected to the p region. The optimum diode geometry for minimum leakage current has the fewest corners and least periphery for a given area, that is, circular. This conflicts with packing density and imaging geometry requirements, so rectangular diodes with rounded corners are usually preferred.

Because leakage is predominantly a depletion layer effect, it will have some voltage dependence. The exact behaviour is complex but the empirical formula of Equ. 2.6. below has been found by Chamberlain [8] to hold for bias voltages between 5V and 25V.

$$J_{L(V)} = J_{Lo} \cdot (1 - 0.06 (V_o - V)) \qquad (2.6)$$

where $J_{L(V)}$ = leakage current density at a reverse bias V

V = reverse bias

V_o = voltage to which the diode is initially charged

and J_{Lo} = leakage current density at $V = V_o$

The dependence of the leakage current on temperature is also rather complex. The simple theory predicts the leakage current to be proportional to the square of the thermally generated equilibrium charge density for intrinsic silicon.

	NO ALUMINIUM COVER		ALUMINIUM COVER OVER RIM		
	TYPICAL	MAX	TYPICAL	MAX.	UNITS
PERIPHERY	6.3×10^{-14}	1.25×10^{-13}	6.3×10^{-15}	1.25×10^{-14}	A/μm
AREA	6.2×10^{-16}	9.3×10^{-16}	6.2×10^{-16}	9.3×10^{-16}	$A/\mu m^2$
90° CORNER	1.9×10^{-11}	4.4×10^{-11}	2.0×10^{-12}	4.4×10^{-12}	A/CORNER
270° CORNER	1.3×10^{-11}	3.0×10^{-11}	1.3×10^{-12}	3.0×10^{-12}	A/CORNER

TABLE 2.1 LEAKAGE COMPONENTS FOR A 1.4μm p-type DIFFUSION (CHAMBERLAIN[8])

Now [9]

$$n_i = p_i = 2\left[\frac{kT}{2\pi\hbar^2}\right]^{3/2} (m_e\, m_p)^{3/4} \exp(-E_g/2kT) \qquad (2.7)$$

where n_i = electron density in intrinsic semiconductor

p_i = hole density in intrinsic semiconductor

m_e = effective mass of electron

m_p = effective mass of hole

and thus we predict a leakage current density of the form

$$J_{L(T)} = \text{const. } T^3 \exp(-E_g/kT) \qquad (2.8)$$

Geary [4] suggests that this relationship holds only at high temperatures, and that at room temperature and below this is dominated by surface leakage and by charge generation in the depletion region. He suggests an empirical relationship of the form.

$$J_{L(T)} = J_{L(T_o)}\, 2^{(T-T_o)/\alpha} \qquad (2.9)$$

where $J_{L(T)}$ the leakage current at temperature T

and α is an empirical constant generally between 6^o and 10^o C.

Figure 2.7. shows the leakage currents of a number of actual devices as a function of temperature, as reported by Chamberlain [8], Vogt et al [6], Livingston et al [10], and Campbell [11]. In order to enable a direct comparison between devices of different areas, all currents have been quoted in terms of carriers/s/cm^2. It is interesting to note how these various sets of experimental data fit the two models suggested.

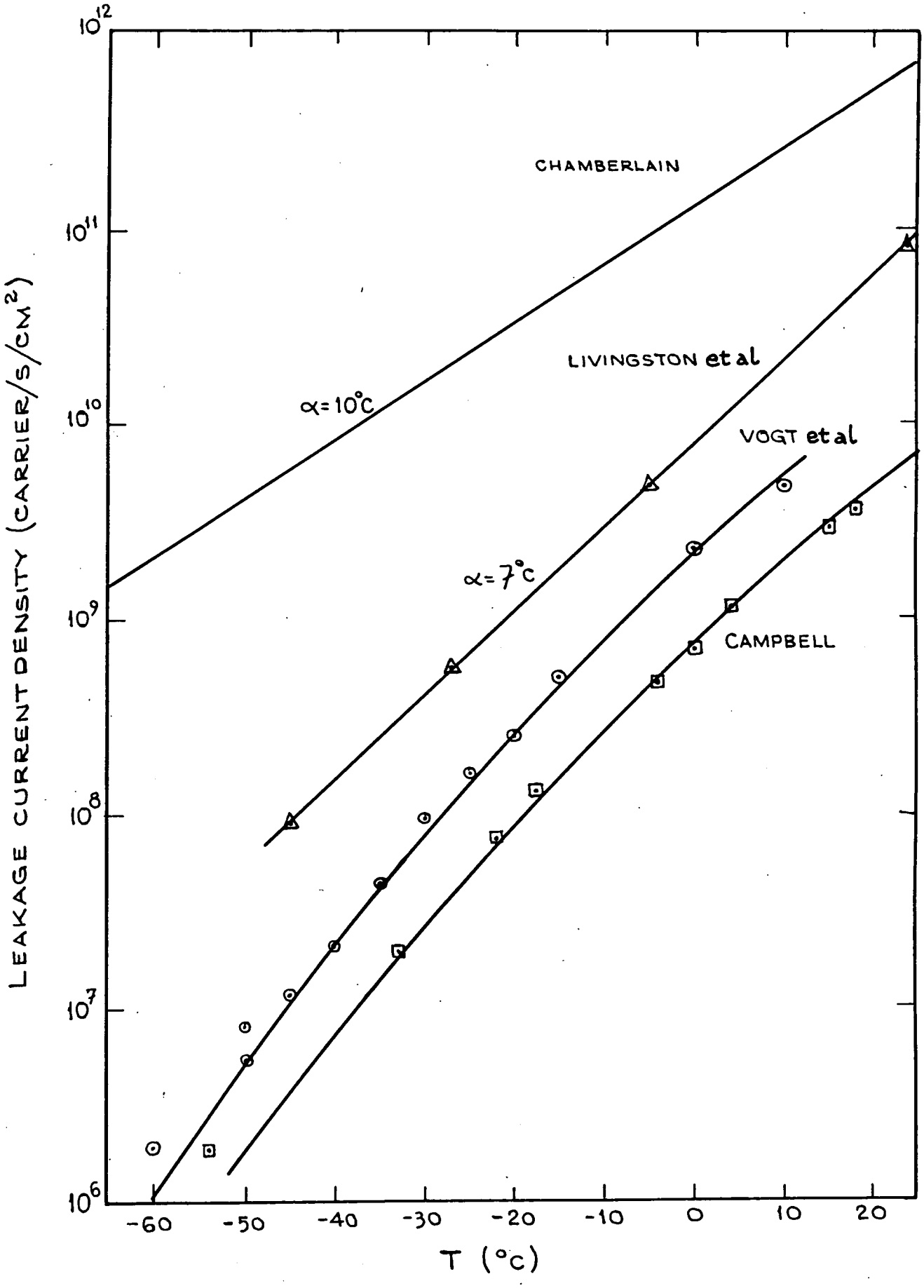


FIG 2.7. LEAKAGE CURRENTS IN VARIOUS SILICON DIODE ARRAYS

Chamberlain quotes his data as fitting a relationship of the type of Equ (2.9.) with a value of $\alpha = 10^{o}$ C. He unfortunately does not publish individual data points, and so it is not possible to see how closely his original data fits this relationship.

Livingston's data is also a good straight line fit, indicating a relationship of the type of Equ (2.9.), but with a value of $\alpha = 7^{o}$C.

However, the data from Vogt et al, and from Campbell, do not convincingly fit to a straight line. The solid lines drawn through these sets of points are curves obeying the "classical" leakage current law of Equ (2.8.).

A possible explanation for these discrepancies is suggested by the fact that it is the devices with lower leakage currents that seem to behave according to the "classical" theory. This may be because in these low leakage devices, surface leakage currents have been reduced by improved process technology, and are no longer dominant.

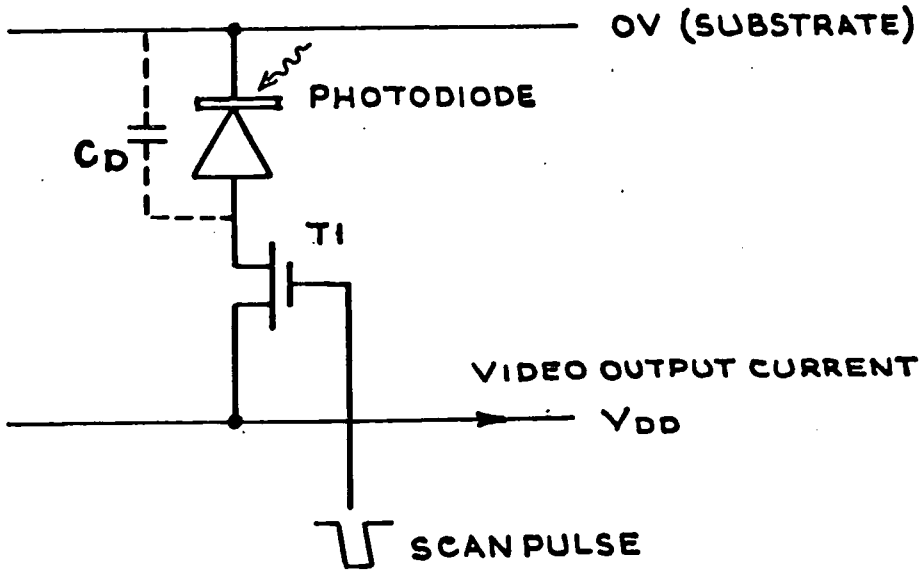
2.2. Signal Sampling Techniques

When operating a reverse biased p-n photodiode in the integrating mode, the diode is initially biased to a voltage V_o, and is then open circuited. The photo-currents and leakage currents as described in Section 2.1 will then decrease the charge stored on the depletion layer capacitance.

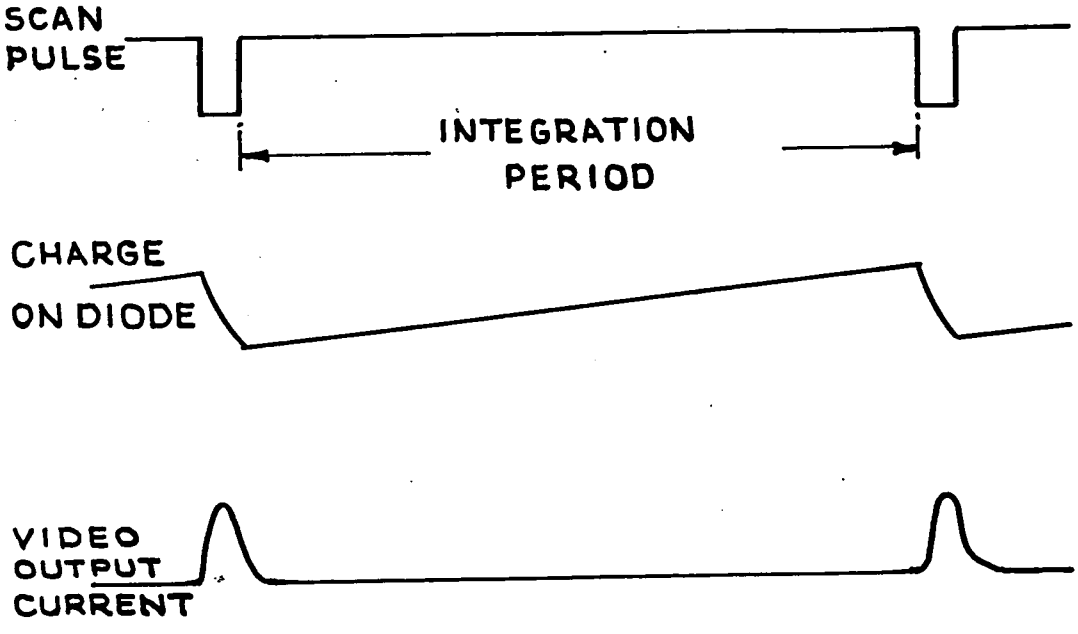
It is then necessary to measure either the charge lost or the charge remaining after a suitable integration period. There are two ways of doing this. The first is to re-bias the diode to its initial potential V_o through a suitable switch, and to integrate the current flowing through the switch during this recharge operation, thus obtaining a measure of the charge lost during the integration interval. This technique is known as recharge or current sampling. The alternative is to measure the open circuit voltage on the diode, usually via a high impedance amplifier. This determines the charge remaining on the junction capacitance, and is called voltage sampling.

2.2.1. Recharge Sampling

This is the simplest mode of operation in terms of element complexity. Various types of switching device have been employed including diodes,[12] but the MOS transistor is now more popular. The circuit, structure and operating cycle of a simple element are shown in Figure 2.8. The reset pulse gates the MOS transistor "on", reverse biasing the diode to V_{DD}, the supply voltage, and at the trailing edge of the reset pulse the diode is open circuited.



(a) CIRCUIT DIAGRAM



(b) OPERATING CYCLE

FIG 2.8 A RECHARGE SAMPLING ARRAY ELEMENT

The time interval until the next reset pulse is called the integration period. During this time the junction is discharged by a combination of leakage currents and photocurrents. At the next reset pulse, current flows through the MOS transistor to recharge the junction to V_{DD}. Thus by integrating the current in the supply line during the reset pulse, the charge lost during the integration period can be measured. Note that the "video" line here is also the supply rail.

The charge "lost" during the integration (the signal charge) is given by.

$$Q_s = \int_0^{t_i} (J_p + J_L)\, A.dt \qquad (2.10)$$

Where Q_s = signal charge.

J_p = photocurrent density

J_L = leakage current density

A = photodiode junction area

t_i = integration time

The signal charge is inherently linear with respect to discharge current. However, the diode bias voltage varies according to the remaining charge. Equation 2.6 shows that the leakage current is therefore dependent on the integrated signal and that its value will change during an exposure. Equations 2.3 (a) - (c) describing the photocurrent contributions from the three regions of the diode also show a dependence on the depths of the depletion layer edges, and thus the quantum efficiency will vary during the exposure.

The saturation level of the recharge sampling element is reached when the diode is completely discharged, and is therefore given by :-

$$Q_s(max) = \int_{V_{DD}}^{0} C_D \, .dV \qquad (2.11)$$

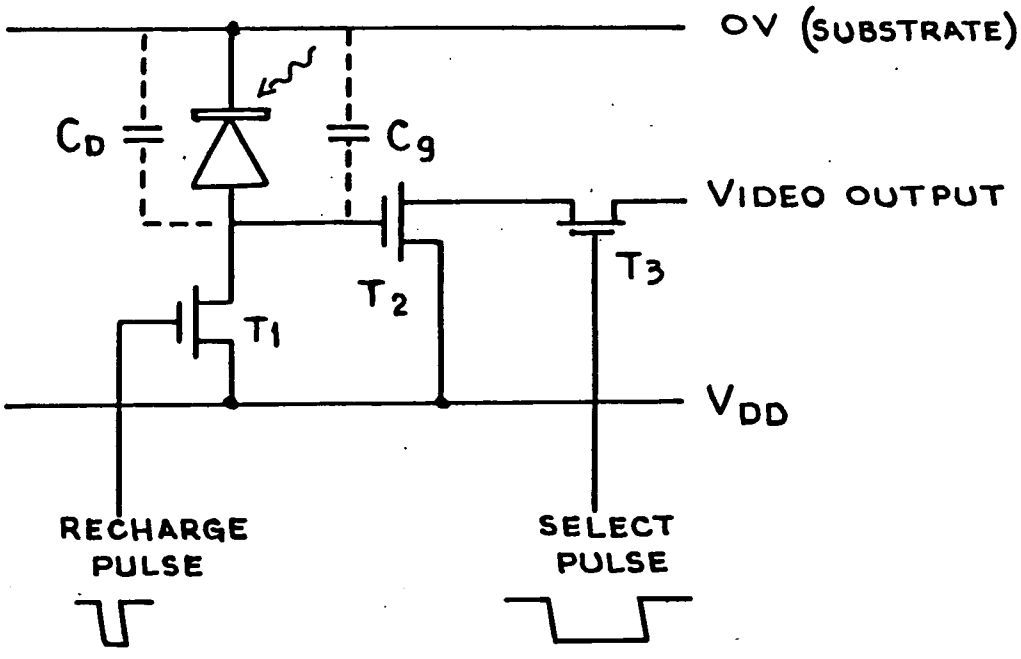
where C_D = diode junction capacitance

Assuming a typical mean junction capacitance of $4\ 10^3$ pF cm $^{-2}$, the stored charge for a diode of area 25 μm x 25 μm with an initial bias of 10V would be 0.25 pC, and thus the saturation would correpond to about $1.6\ .10^6$ electron/hole pairs.

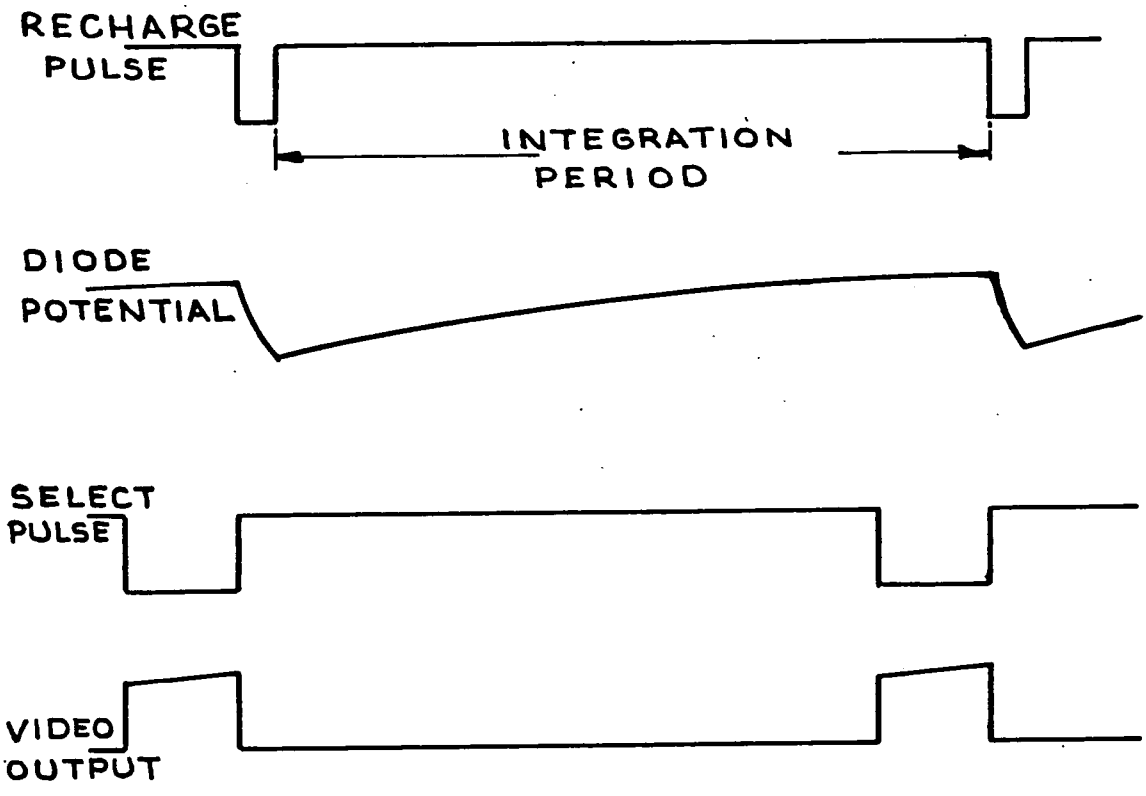
Note from the above and from Equation (2.10) that both the sensitivity and saturation level of a recharge sampled element are proportional to diode area.

2.2.2. Voltage Sampling

The circuit diagram of a simple voltage sampling element is shown in Figure 2.9 (a). The transistor T1 performs the same recharge function as in the recharge sampling array. However, the output signal is derived from the diode bias potential at the gate of the source follower stage T2. T3 is a multiplexing transistor which gates the output of the source follower onto the video line when enabled by a scan pulse. The operating cycle is illustrated in Figure 2.9 (b). One immediate contrast with recharge sampling is evident in that the output from a voltage sampled element is in the form of a dc level, rather than the transient output associated with recharge elements.



(a) CIRCUIT DIAGRAM



(b) OPERATING CYCLE

FIG 2.9 A VOLTAGE SAMPLING ARRAY ELEMENT.

The analogous equation to equation (2.10), describing the output voltage as a function of photocurrents and leakage current, can be derived to various levels of complexity.

By assuming that the diode capacitance is voltage independent, and that the gate capacitance of the source follower T2 is negligible, we can describe the rate of change of voltage across the diode by :-

$$C_D \frac{dV}{dt} = \frac{dQ}{dt}$$

$$= - (J_p + J_L) A \qquad (2.12)$$

Integrating the above we obtain :-

$$C_D \int_{V_o}^{V} dV = -\int_{O}^{t_i} (J_p + J_L) A.dt$$

and hence

$$V_{(t)} = V_{DD} \left[1 - \frac{A}{C_D V_{DD}} \int_{O}^{t} (J_p + J_L) .dt \right] \qquad (2.13)$$

The capacitance of the junction can be expressed as

$$C_D = \frac{\epsilon A}{d}$$

Where d = depletion layer width
ϵ = permittivity of silicon

This removes the area dependance and Equation 2.13 becomes

$$V_{(t)} = V_{DD} \left[1 - \frac{d}{\epsilon V_{DD}} \int_{O}^{t} (J_p + J_L) .dt \right] \qquad (2.14)$$

Non linearity is introduced into this response function because of the voltage dependence of the depletion layer width.

This voltage dependence can be seen from Equations 2.4 (a) and (b). By assuming that the doping density is very much higher in the p^+ region than in the substrate, then the movement of the depletion layer into this region can be neglected and from Equations (2.4) the depletion layer width can now be expressed as :-

$$d = \left[\frac{2\epsilon (V_c + V)}{N_d} \right]^{\frac{1}{2}}$$

This expression is valid only for an abrupt junction. An approximate general expression is [13]

$$d = k\, V^p \qquad (2.15)$$

where k = a constant incorporation some junction parameters
$p = \frac{1}{2}$ for an abrupt junction
$= 1/3$ for a linearly graded junction

This assumes that V is significantly larger than the contact potential V_c (≈ 0.6v).

The diode capacitance now becomes :-

$$C_{(V)} = \frac{A\epsilon V^{-p}}{k}$$

Substituting this into Equation (2.12) and integrating, we obtain :-

$$-\int_0^t (J_p + J_L)\, A.dt = \int_{V_o}^{V} \frac{A\epsilon V^{-p}}{k} .dV$$

$$= \frac{A\epsilon}{k(1-p)} \left[V^{1-p} - V_o^{1-p} \right]$$

Now $k = d_o V_o^{-p}$

where d_o is the depletion layer width at $V = V_o$

and thus

$$V_{(t)} = V_o \left[1 - \frac{(1-p)\, d_o}{\epsilon V_o} \int_0^t (J_p + J_L) \, .dt \right]^{\frac{1}{1-p}} \qquad (2.16)$$

Compare this with Equation 2.14 for a voltage independent capacitance, which can be seen to be a special case of the above with $p = 0$.

It should be noted that additional non-linearities also occur as in the recharge sampling element, due to the dependence on depletion layer width of J_p and J_L, the photocurrents and thermal leakage currents respectively.

Figure 2.10 shows the decay of voltage as a function of time for constant $(J_p + J_L)$ with $p = 0$, $1/3$ and $\frac{1}{2}$.

A more precise treatment would use

$$d = k (V + V_c)^p$$

in place of Equation 2.15, and this would accentuate the deviations at low output voltages.

Two points are of interest when comparing the response characteristic of the voltage sampling element with that of the recharge sampling element. The non linearity displayed in Equation 2.16 can be considered to arise from integration of the signal on a non-linear element (i.e. the diode capacitance) rather than on the external and hopefully linear integrator capacitor of the external amplifier.

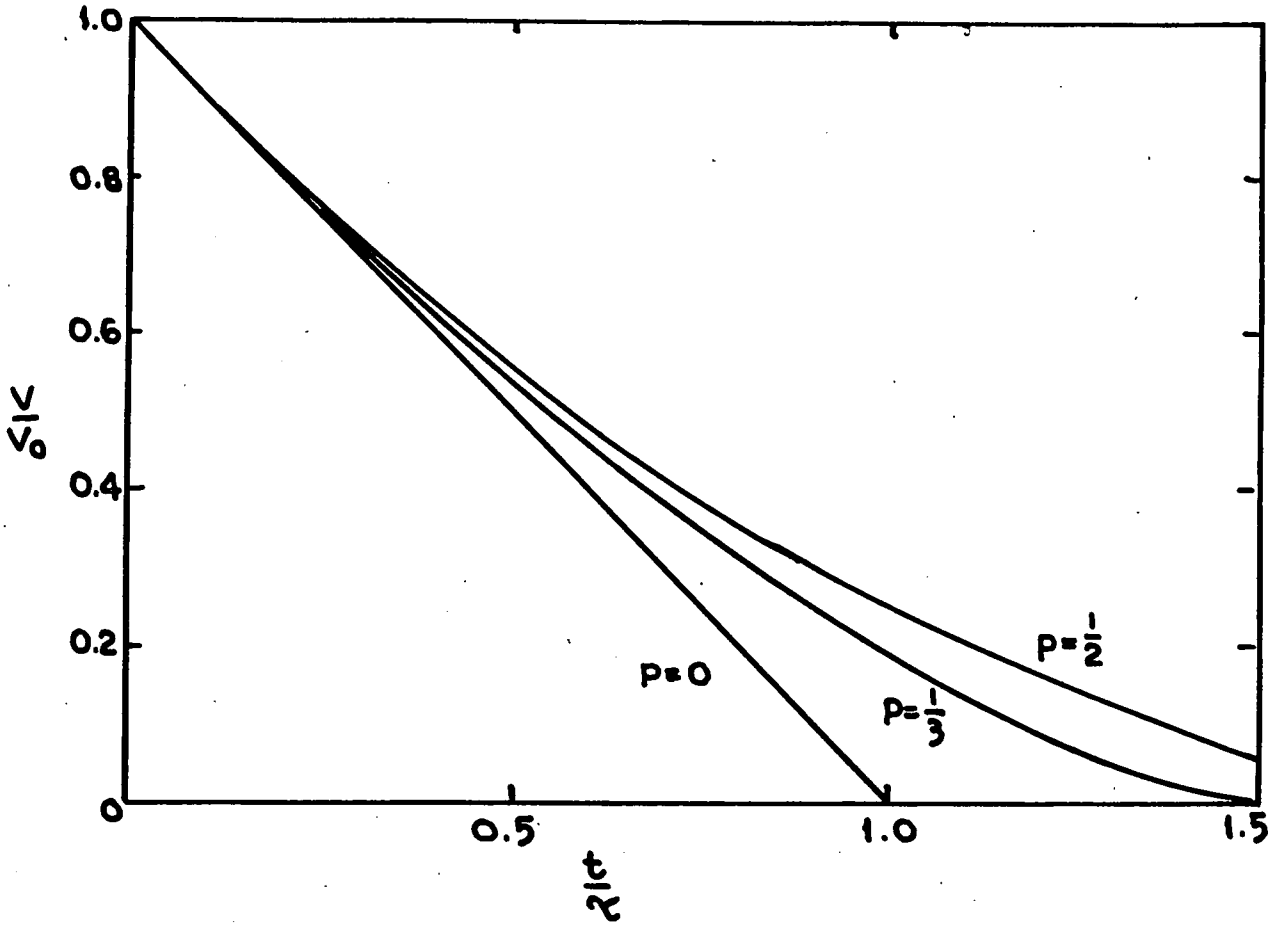


FIG 2.10 THE RELATIVE JUNCTION VOLTAGE AS A FUNCTION OF EXPOSURE TIME $\left(\frac{t}{\tau_c}\right)$ ASSUMING A C-V LAW WITH $p=0, \frac{1}{3}$ & $\frac{1}{2}$ [EQN. 2.14]

Secondly, it can be seen that the area dependence of the responsivity has been eliminated, and therefore no signal "gain" is achieved by the use of larger diodes. Conversely, small element sizes are feasible for use in high resolution arrays without loss of signal.

So far only the potential across the diode has been described. The transfer characteristics of the MOS source follower (T2 in Figure 2.9) is strongly dependent on the type of external load used. Three types of load can be envisaged, namely a resistive load, a virtual earth load and a constant current load. The following analyses follow the techniques of Dickson et al [14]

The three cases are shown in Figure 2.11 (a) - (c). In all the analyses to be given, the multiplexing transistor T3 is replaced for simplicity by a resistor R_3 of value equal to its "on" resistance. The two characterstics of interest are the output voltage as a function of diode voltage, and the risetime of the output voltage in response to a step function of diode potential.

a) Resistive Load

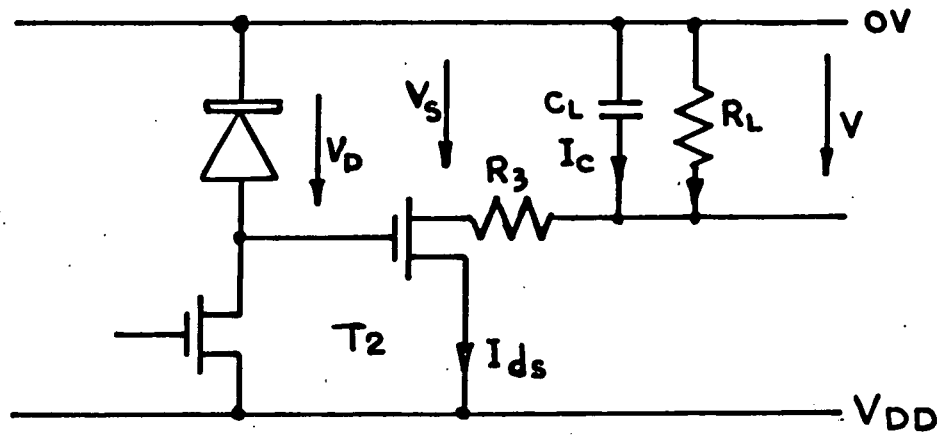
Referring to Figure 2.11 (a) and using the terms as defined there, then the equilibrium output voltage is given by :-

$$V_o = I_{ds} R_L \qquad (2.17)$$

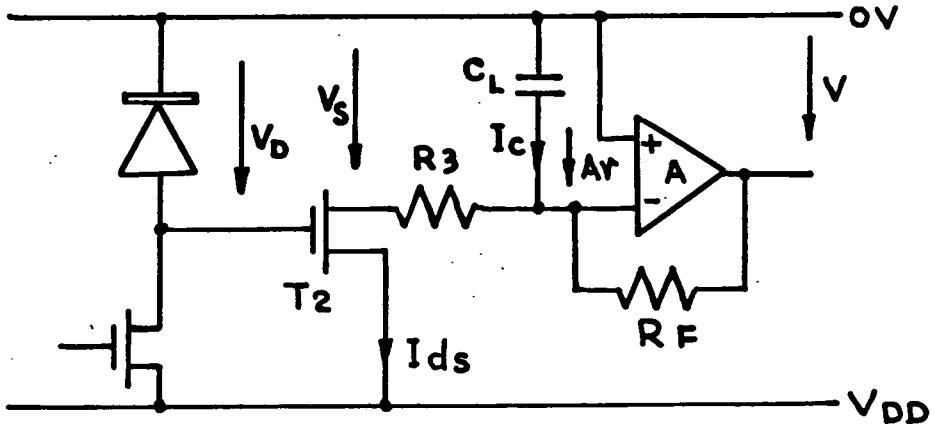
Now for an MOS transistor at saturation [3]

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_T)^2$$

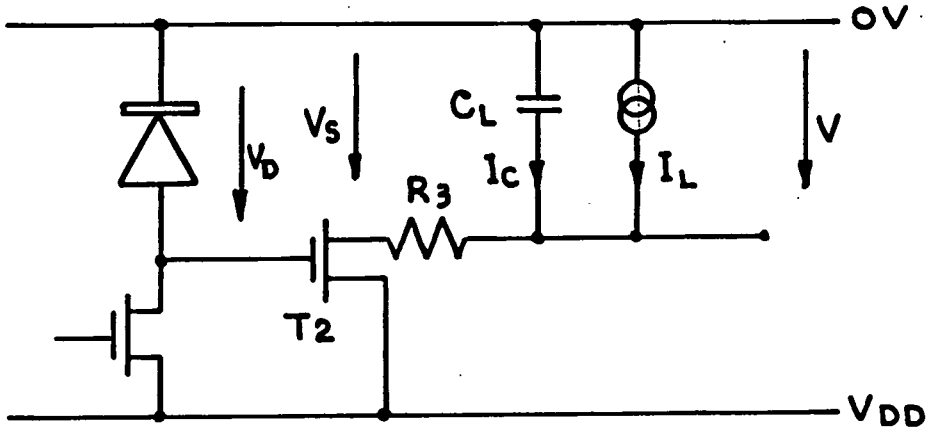
where β = is a parameter of the device defined by the process



(a) RESISTIVE LOAD



(b) VIRTUAL EARTH LOAD



(c) CONSTANT CURRENT LOAD

FIG 2.11 OUTPUT LOADS FOR VOLTAGE SAMPLING ARRAYS

V_{gs} is the gate-source voltage

V_T is the threshold voltage

Applying this to the situation in Figure 2.11 (a)

$$I_{ds} = \frac{\beta_2}{2} (V_D - V_s - V_T)^2$$

$$= \frac{\beta_2}{2} (V_D - V_T - I_{ds} (R_L + R_3))$$

where β_2 is the β associated with T_2. This gives a quadratic equation for I_{ds} of :-

$$(R_L + R_3)^2 I_{ds}^2 - (2(V_D - V_T) (R_L + R_3) + 1/\beta_2) I_{ds} + (V_D - V_T)^2 = 0$$

Solving for I_{ds} and substituting into Equation 2.17 gives the equilibrium output voltage V_o as a function of diode voltage V_D as :-

$$V_o = \frac{R_L}{R_3 + R_L} \left[V_D - V_T + \frac{1 - \sqrt{(1 + 2\beta_2 (R_L + R_3) (V_D - V_T))}}{\beta_2 (R_3 + R_L)} \right] \quad (2.18)$$

The transient response of the circuit can be derived by observing that at equilibrium :-

$$\frac{V_o - V_E}{R_3} = - \frac{V_o}{R_L}$$

where $V_E = V_D - V_T$ and is the effective diode voltage and noting that all voltages are defined negative and thus;

$$R_L V_E = (R_L + R_3) V_o \quad (2.19)$$

In general though, at a time t the output voltage V will be given by :-

$$\frac{V - V_E}{R_3} = - \frac{V}{R_L} + I_c \quad (2.20)$$

where I_c is the instantaneous current in the video line capacitance C_L.

Now

$$I_c = - C_L \frac{dV}{dt}$$

and the general case of Equation (2.19) is

$$(R_L + R_3)\ V - R_L\ V_E = - R_L\ R_3\ C_L \frac{dV}{dt}$$

Integrating and substituting for $R_L\ V_E$ from Equation 2.19 we obtain

$$\log \frac{V_o - V}{V_o} = - \frac{R_L + R_3}{R_L\ R_3\ C_L}\ t$$

and

$$V = V_o \left[1 - \exp \left[- \frac{R_L + R_3}{R_L\ R_3\ C_L}\ t \right] \right] \qquad (2.21)$$

which describes the response to a step change in V_D which would produce an equilibrium voltage V_o.

b) Virtual Earth Load

The expression for the equilibrium output voltage for the virtual earth example of Figure 2.11 (b) can be derived in a similar fashion to that for a resistive load by noting that :

$$V_o = - I_{ds}\ R_F$$

where R_F is the feed-back resistance of the amplifier, and that R_L is now zero.

Thus

$$V_o = -\frac{R_F}{R_3}\left[V_D - V_T + \frac{1 - \sqrt{1 + 2\beta_2 R_3 (V_D - V_T)}}{\beta_2 R_3}\right] \quad (2.22)$$

The derivation of the transient response also closely follows that for the resistive load, using the equation corresponding to equation (2.20) which is :-

$$\frac{\Delta v - V_E}{R_3} = -\frac{(A+1)\Delta v}{R_F} + I_c$$

and the expression for the output voltage V at time t becomes :-

$$V = V_o\left[1 - \exp\left(\frac{-A}{R_F C_L}\, t\right)\right] \quad (2.23)$$

c) Constant Current Load

The expression for the equilibrium output voltage is somewhat more straightforward for the constant current case. The drain current is now equal to I_L, the load current, and therefore

$$I_L = \frac{\beta_2}{2}(V_D - V_T - V_s)^2$$

Now $V_s = V_o + I_L R_3$

and $I_L = \frac{\beta_2}{2}(V_D - V_T - V_o - I_L R_3)$

Hence $V_o = V_D - V_T - I_L R_3 - \sqrt{\frac{2I_L}{\beta_2}}$ (2.24)

The transient response analysis is similar to the two previous derivations, using the expression for the output voltage (cf. Equations 2.20) :-

$$\frac{V - V_E}{R_3} = I_L + I_c$$

The output voltage at time t then becomes :-

$$V = V_o \ (1 - \exp (- t/R_3 \ C_L)) \qquad (2.25)$$

In order to compare the linearity of response of the three types of load, we can write the equilibrium output voltages in a common form.

All the equations (2.18, 2.22, 2.24) are of the form :-

$$V_o = K \ (V_D - V_T - V_{ERR})$$

so for the resistive load, from Equation (2.18)

$$V_{ERR} = \frac{1 - \sqrt{(1 + 2\beta_2 \ (R_L + R_3) \ (V_D - V_T))}}{\beta_2 \ (R_3 + R_L)} ,$$

and similarly for the other loads.

The extent to which the load degrades the output response is shown in Figure 2.12. Typical values [15] have been taken for the relevant parameters and a family of output curves plotted.

The ideal situation is where the load resistance is infinite, equivalent to a constant current load of zero.

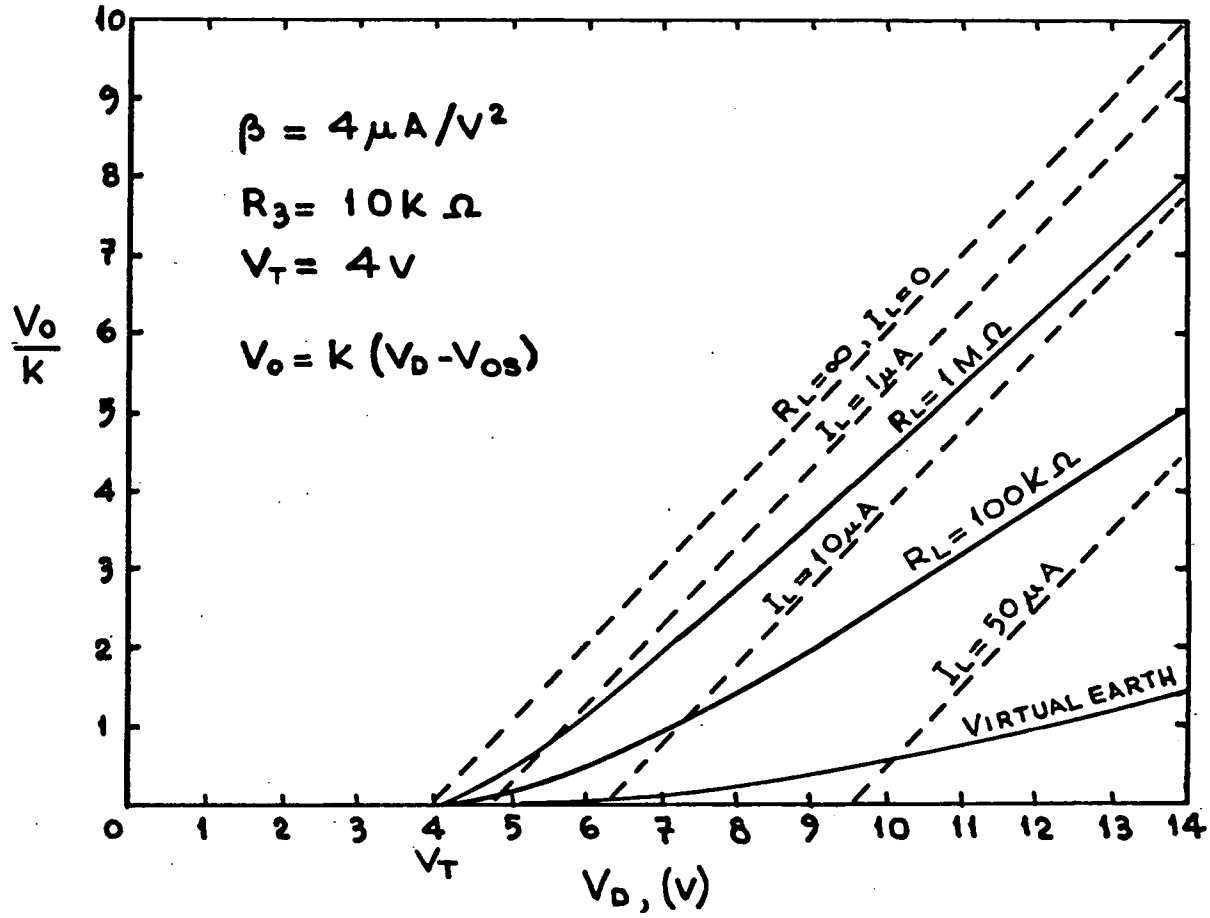


FIG 2.12 OUTPUT CHARACTERISTICS FOR RESISTIVE, VIRTUAL EARTH AND CONSTANT CURRENT LOADS

For the resistive load case, as the load resistance decreases, attenuation and non-linearity increase until the limiting situation of the virtual earth amplifier is reached.

The constant current load exhibits good linearity, but the dynamic range deteriorates because of the imposition of what is effectively an additional threshold voltage.

Expressing the dynamic range quantitively in terms of signal charge, we obtain for the resistive and virtual earth loads.

$$Q_{s\ max} = \int_{V_{DD}}^{V_T} C_D \cdot dV \qquad (2.26)$$

and for the constant current load

$$Q_{s\ max} = \int_{V_{DD}}^{V_T + V_{ERR}} C_D \cdot dV \qquad (2.27)$$

where $V_{ERR} = I_L R_3 + \sqrt{(2I_L/\beta_2)}$

The time response of each output circuit can be expressed in a common form, from Equations (2.21, 2.23, and 2.25)

$$V_E = V_o \ (1 - \exp (-t/\tau))$$

where for the resistive load for example, from Equation (2.21)

$$\tau = \frac{R_L R_3}{R_L + R_3} C_L$$

and similarly for the other loads. These time constants, and their values under a range of typical conditions are shown in Table 2.2.

From this, it can be seen that the virtual earth load has by far the fastest response time.

TYPE OF LOAD	GENERAL EXPRESSION	TYPICAL CONDITIONS	TIME CONSTANT [1]
RESISTIVE	$\tau = \frac{R_L R_3}{R_L + R_3} C_2$	$R_L = 1M\Omega$	$9.9\ C_L$ nS
		$R_L = 100K\Omega$	$9.1\ C_L$ nS
VIRTUAL EARTH	$\tau = \frac{R_F C_L}{A}$	$A = 10^5$, $R_F = 50K\Omega$	$5 \times 10^{-2} C_L$ nS
		$A = 10^5$, $R_F = 10K\Omega$	$10^{-2} C_L$ nS
CONSTANT CURRENT	$\tau = R_3 C_L$	—	$10\ C_L$ nS

$R_3 = 10K\Omega$

1) C_L = VIDEO LINE CAPACITANCE, (pF)

TABLE 2.2 OUTPUT TIME CONSTANTS FOR VARIOUS EXTERNAL LOADS

So far, the discussion has been restricted to the operation of a single element, whether recharge or voltage sampled. In order to produce a useful detector many elements must be incorporated together in some way.

2.3. Scanning Techniques

It is theoretically possible to operate any form of addressed structure such as a memory or an imaging array in either a sequential or a random access mode. Although diode arrays have been constructed with a random access organisation [16], these have not been based on the integrating mode of operation. A problem arises with arrays of the type described in the earlier sections of this chapter in that if a random addressing sequence is employed, the integration periods experienced by each diode can all be different, making signal analysis very complex.

The simplest form of sequential addressing structure is the shift register with parallel outputs, and it is obviously desirable to implement the shift register "on-chip" and with the same processing technology as used for the light sensing elements. This minimises the number of interconnections, thus minimising assembly cost and enhancing yield and reliability.

Given that the shift register is to be manufactured on the same chip, it becomes essential to minimise the thermal dissipation of the register, otherwise the operating temperature of the array will rise and thermal gradients may occur. This leads to an increase, or worse, a non-uniformity, in dark current. Historically, the first on-chip registers were of the static MOS type. However, dynamic registers with lower power dissipations are now available.

2.3.1. Static MOS Shift Registers

Most shift registers are based on the concatenation of inverter stages, with some form of storage element between stages. Each MOS inverter requires a load, and this can be simply a diffused resistor. However, diffused high value resistors are extremely costly in terms of area, and it is preferable to use a suitably biased MOS device as an active load.

A single element of a static shift register designed by Chamberlain for use in a diode array is shown in Figure 2.13.

Note the similarity between this circuit and the traditional bistable. Here T3, T5 and T9 are the load transistors. The feed-back transistor T6 is used to maintain the stored charge on the gate of T2 during Ø2. This register is capable of driving loads in excess of 15 pF and can be operated at arbitrarily low speeds. However, there are 9 devices per stage, the power dissipation is about 3mW per stage and the maximum scanning frequency is limited to about 50 kHz. For higher operating speeds, dynamic registers are required.

2.3.2. Ratio Dynamic MOS Registers

A simpler shift register can be achieved by eliminating the feed-back transistor and relying on temporary charge storage on the transistor gates. The storage time is then no longer infinite and the clock period must be made smaller than this. The simplest form of such a register is shown in Figure 2.14 (a). The loads are still MOS transistors which are always held conducting.

The power dissipation can be reduced by using clocked load devices that are turned "on" only as required. In the circuit of Figure 2.14 (b) power is only dissipated in an inverter during the relevant clock phase, and thus the power dissipation is now proportional to the duty cycle of the clock phase. Typical scan rates achievable with dynamic registers of this type are about 10 MHz, and the power dissipation is about 0.5 mW/stage. One problem which occurs with shift registers of the clocked load type is that the output zero levels are not well defined and low amplitude pulses are present synchronous with one clock phase. Although these are of insufficient amplitude to address an array element, they can contribute to clock breakthrough on the video line.

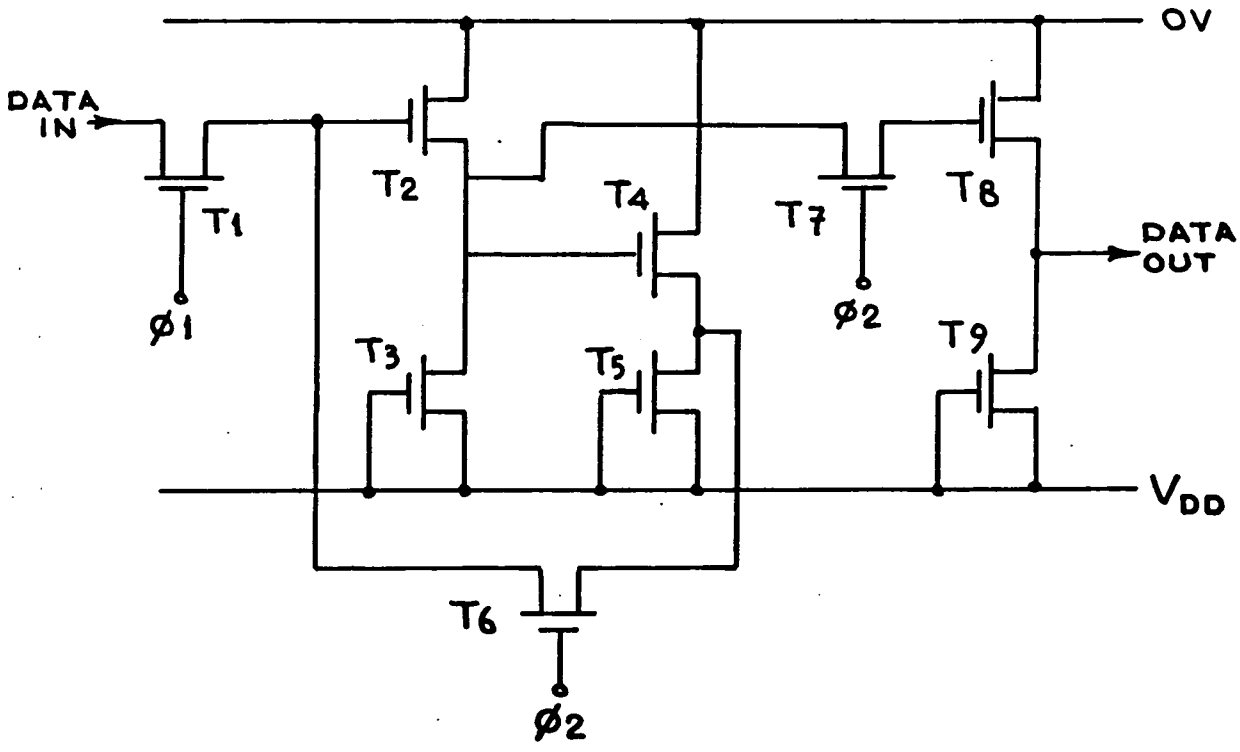
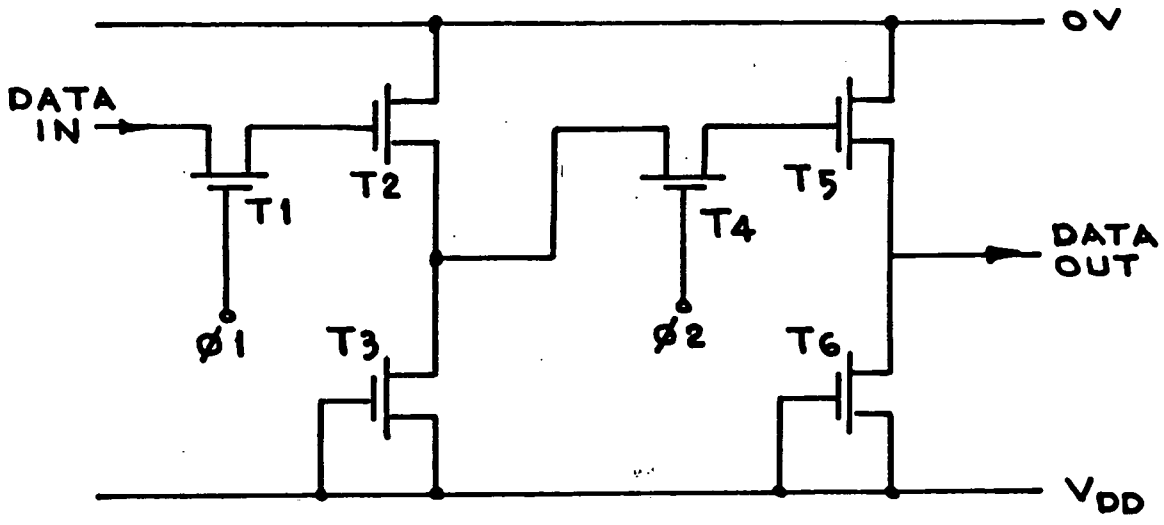
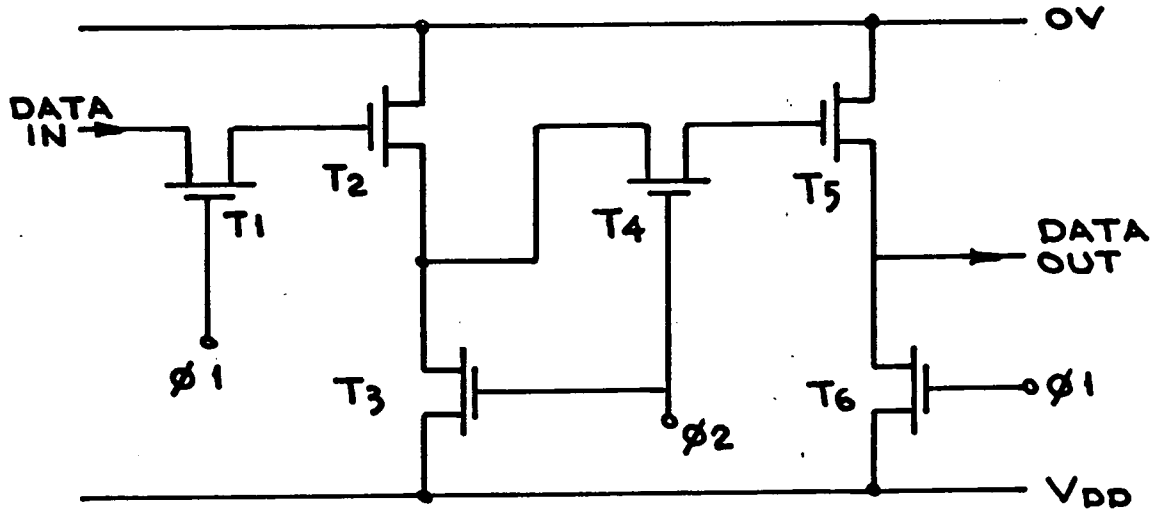


FIG 2.13 STATIC MOS SHIFT REGISTER (SINGLE ELEMENT)



(a) SIMPLE MOS TRANSISTOR LOADS



(b) CLOCKED LOADS

FIG 2.14 SINGLE ELEMENTS OF AN MOS RATIO. DYNAMIC SHIFT REGISTER WITH SIMPLE AND CLOCKED LOADS

Both registers described above use the ratio of the load and input device resistances to define the output logical "1" state. The load transistor is required to have a resistance 10 to 20 times larger than that of the input transistor, and therefore occupies a correspondingly larger area. The maximum operating frequency is also limited by the large time constant associated with the load transistor.

2.3.3. Ratioless Dynamic MOS Registers

The above problems are solved by the use of ratioless inverter circuits in which the output level is defined by the discharge of a capacitor. Such a shift register element is shown in Figure 2.15 [17]. The clock line loading in this circuit is high, since these are used also for ground and power connections. No d.c. paths exist and the power dissipation is thus given by :-

$$P = CV^2f$$

where C = clock line capacitance
V = clock voltage
f = clock frequency

The dissipation at 1 MHz for a typical ratioless register is about 0.1 mW/stage.

2.3.4. Dynamic CMOS Registers

Further reductions in power dissipation can be achieved by using complementary transistor pair (CMOS) circuitry. Dissipations of about 0.01 mW/stage at 1 MHz are achievable [17] with registers of the type shown in Figure 2.16. The CMOS technique, however, requires complex processing with large "p-well" diffusions to accommodate the n-channel devices. This leads inevitably to large element areas and reduced yields. Consequently,

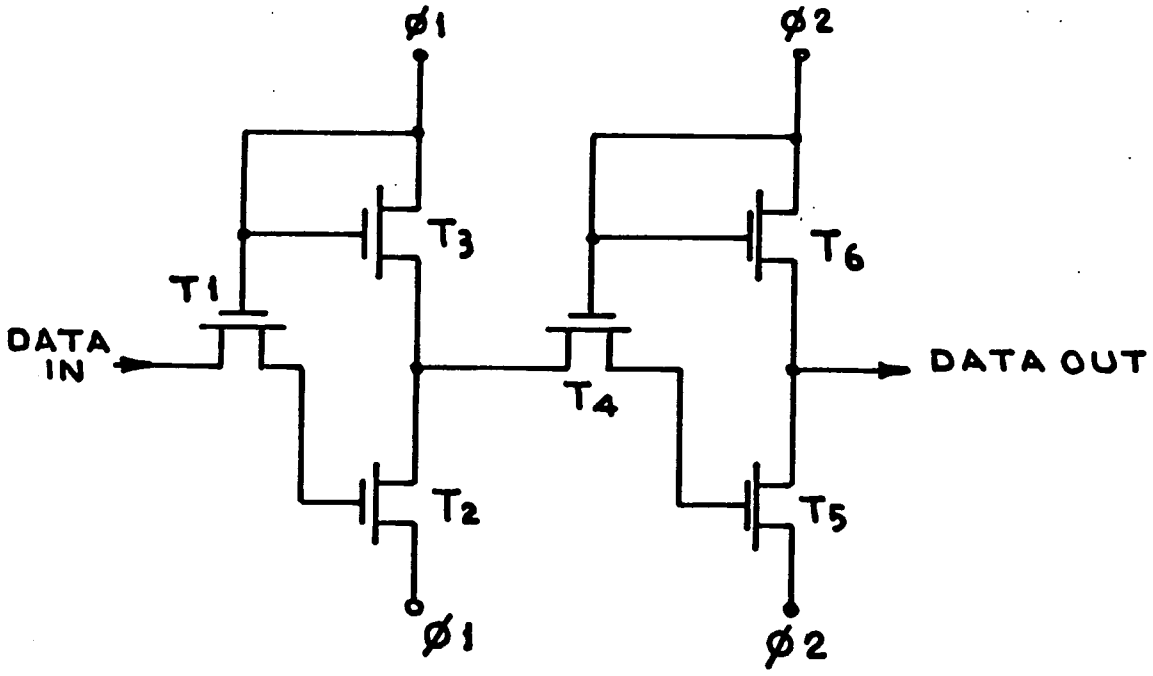


FIG 2.15 SINGLE ELEMENT OF A RATIOLESS DYNAMIC MOS SHIFT REGISTER

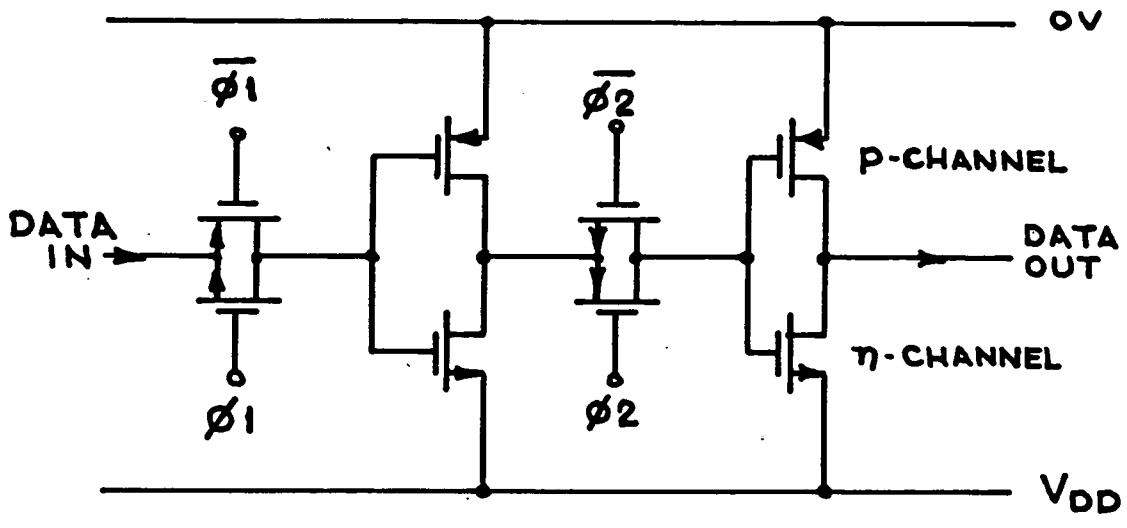


FIG 2.16 SINGLE ELEMENT OF A RATIOLESS DYNAMIC CMOS SHIFT REGISTER

although some applications have been reported [18], the use of CMOS registers in diode arrays has not been widespread.

2.3.5. Bootstrapped MOS Registers

So far, all the registers described have used as the basic element two inverters. It is also possible to implement a shift register with source followers rather than inverters. Usable outputs are then obtained from every "half-stage", resulting in an effective halving of area requirement and power dissipation.

In an MOS follower stage, however, there is a voltage drop between input and output of one threshold voltage, and thus the construction of such registers was not feasible until the development of the "bootstrap" technique [19] for eliminating this drop. The bootstrap element can be either a capacitor or an MOS varactor, and a circuit developed for diode array scanning using the latter is shown in Figure 2.17.

2.3.6. Bucket Brigade Device Registers

A further departure from conventional, inverter based registers is the use of a digital bucket brigade delay line. In tests carried out by Weimer et al [20], a p-channel MOS bucket brigade delay line was operated with double and single clocks, and negative and positive inputs. The two most interesting modes of operation were found to be the double clock with a negative input, which produces a useful scan pulse at each output, and the single clock with a positive input, which gives a scan pulse at every alternate output. These two modes of operation are illustrated in Figure 2.18. The switching transients at the outputs are considerably worse than from more conventional registers, and this seems to be the reason why little interest has been shown in the technique since, despite the considerable reduction in device count.

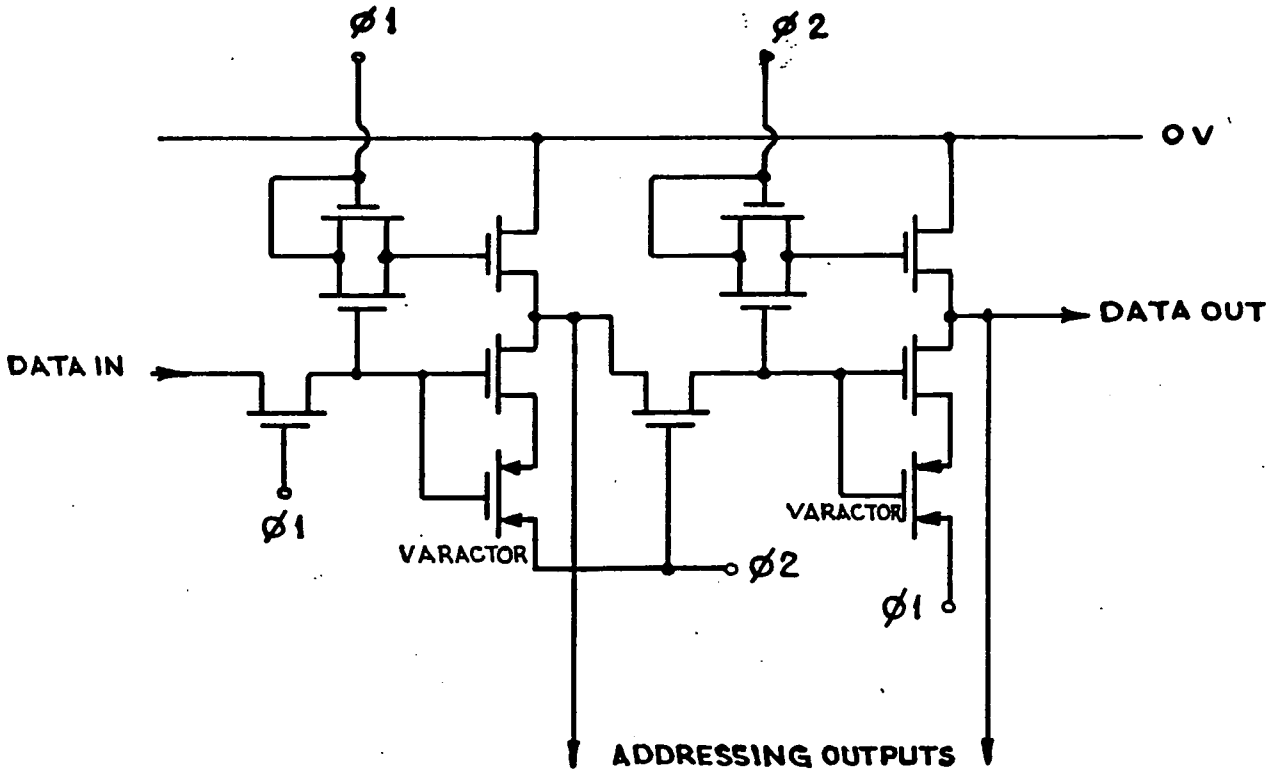
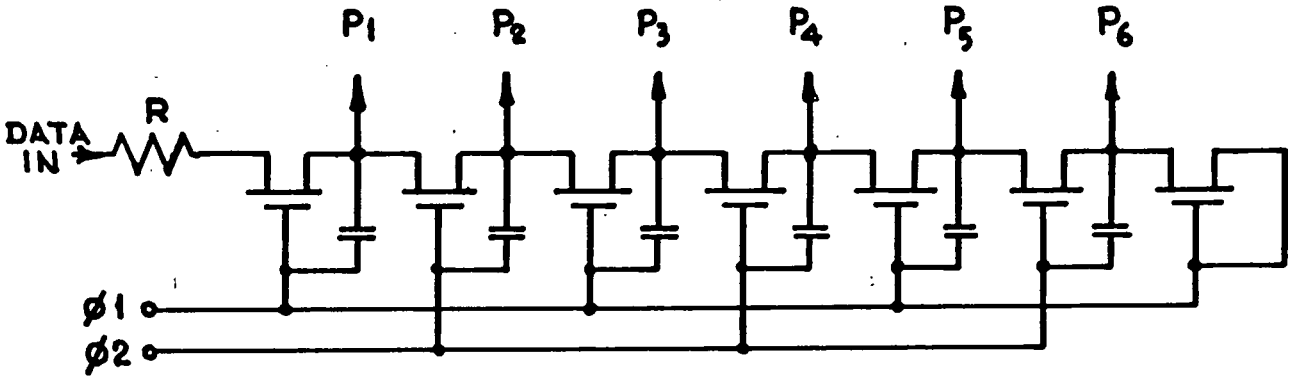
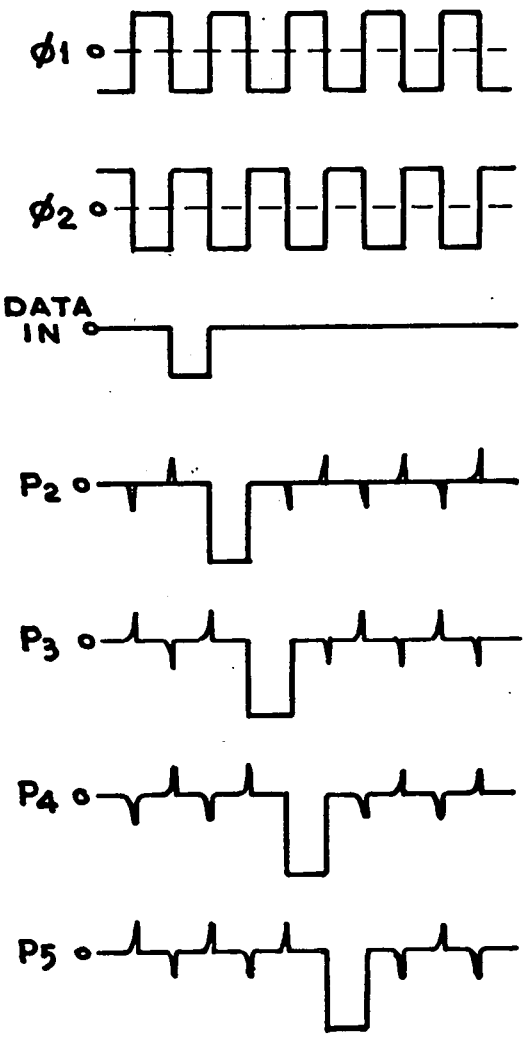


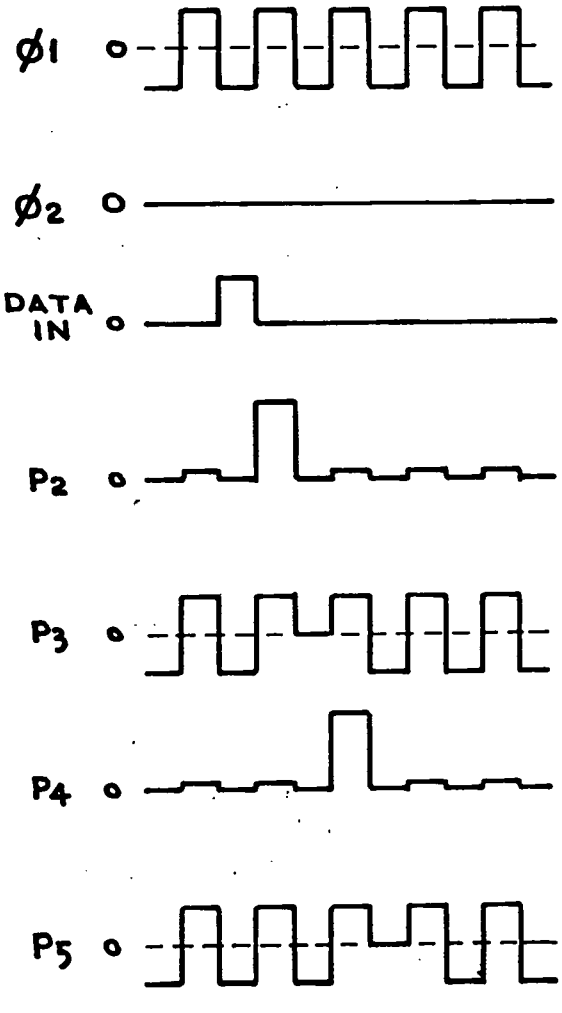
FIG 2.17 MOS SHIFT REGISTER WITH VARACTOR BOOTSTRAPPING



(a) CIRCUIT DIAGRAM



(b) DOUBLE CLOCK OPERATION



(c) SINGLE CLOCK OPERATION

FIG 2.18 BUCKET BRIGADE SCAN GENERATOR

2.3.7. Register Organisation

Figures 2.19 (a) and (b) respectively illustrate the way in which recharge and voltage sampling arrays are scanned by a suitable register. In order to initiate a scan, a start pulse must be loaded into the first element of the shift register. If the shift register input is made available this can be carried out by external logic and this is the most versatile mode of operation. The register can be either cycled continually, in which case the integration time experienced by each element is given by :-

$$t_I = nf$$

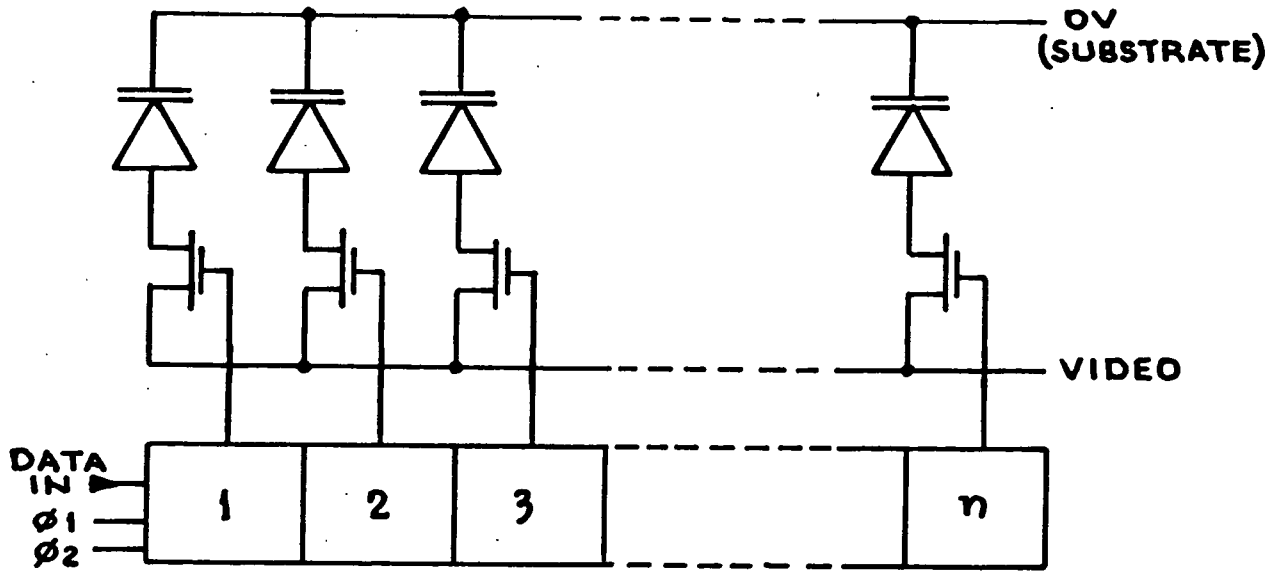
where n = no. of stages in the shift register.
f = scan rate of register in stages/second

Alternatively, the array can be scanned once and then allowed to integrate for a period t_o before a second scan initiate pulse is sent to the register. In this case the integration time becomes :-

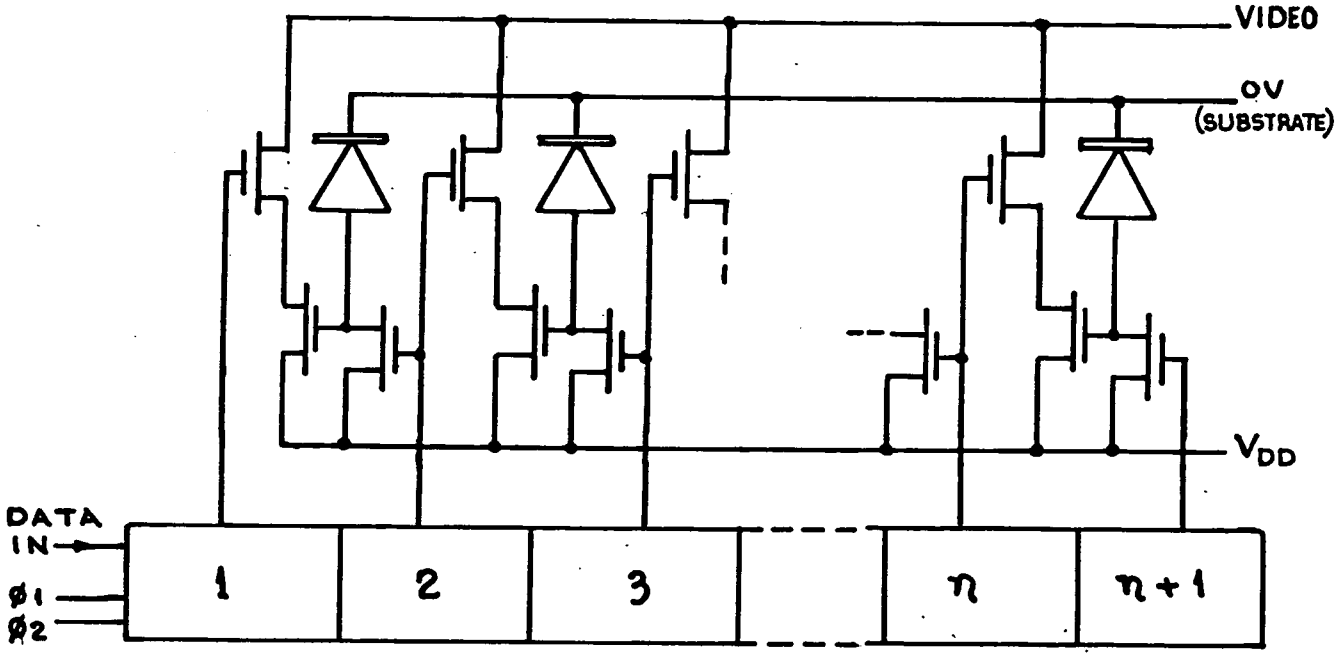
$$t_I = t_o + nf$$

and the integration can be made arbitrarily long without reducing the clock frequency.

In many applications where simple repetitive scanning is sufficient, it is more attractive to implement a self-initiating ring counter on-chip and thus minimise the external logic. Such a circuit is used in the Reticon 64 element circular geometry array, type RO64 [18].



(a) SCANNING OF AN n-ELEMENT RECHARGE SAMPLING ARRAY



(b) SCANNING OF AN n-ELEMENT VOLTAGE SAMPLING ARRAY

FIG 2.19 SCANNING REGISTER ORGANISATION

2.4. Noise Sources

So far the two basic types of diode array element, and the way in which they can be scanned, have been described, and the response characteristics have been studied. Any comparison of performance must also include an evaluation of the noise sources for recharge and voltage sampling arrays. The classification of noise into fixed pattern noise and random noise has been described in Chapter 1. The two types of noise will be described separately for each mode of array sampling.

2.4.1. Fixed Pattern Noise in Recharge Sampling Arrays

Responsivity fixed pattern noise (f.p.n.) in recharge sampling arrays is caused by variations in quantum efficiency and diode area, whereas offset f.p.n. arises from variations in thermal leakage current and in the level of MOS charge pumping in the addressing transistors. Synchronous noise is present on the output waveform because of clock breakthrough onto the video lines. These three contributions to fixed pattern noise will be described separately.

(a) Responsivity F.P.N.

The quantum efficiency of a diode, as seen in Section 2.1, is a function of such parameters as carrier lifetimes, diffusion co-efficients, junction depths and doping concentrations. Variations in these can be expected from one batch of chips to another, but from point to point on a single chip variations should be negligible, and the contribution to the total responsivity f.p.n. from quantum efficiency variation is probably less than 1%.

A much larger contribution comes from variations in diode area. Such variation is a function of the photoengraving tolerances, which are continually being improved, and for a given tolerance, the responsivity variation will be more severe for smaller area diodes. Taking for example a dimensional tolerance of $\pm$ 0.5 μm and a nominal area of 250 μm x 40 μm, the responsivity f.p.n. would be about 1.5% of the signal

(b) Offset F.P.N.

The fixed pattern noise due to variations in offset level is independent of signal, and it is therefore convenient to express the noise sources as an equivalent noise charge (ENC) in either picocoulombs or electrons.

Thermal leakage currents arise not only in the photodiode as described in Section 2.1., but also in the drain diffusions of the addressing transistors.

The leakage current densities will be of the same order in both the photodiode and the drain diffusion, and typical drain areas are about 5.10^{-6} cm^2. Thus for a large diode of 600 μm x 25 μm the contribution from the drain diffusion would be only about 3% of the total leakage, whereas the drain leakage would be dominant for a small diode of 20 μm x 20 μm.

The thermal leakage currents measured for various Reticon devices were shown in Figure 2.7 and for example, the leakage current at room temperature for a 600 μm x 25 μm diode was measured [4] to be about 10^6 - 10^7 electrons/sec. The variation from diode to diode in leakage current is typically of the same order as the magnitude of the current[15] and can thus be estimated to contribute a noise of about 5.10^{10} electrons /sec/cm^2. Note that although signal independent, this source of offset f.p.n. is proportional to the integration time.

An effect known as charge pumping was discovered in MOS transistors by Brugler and Jespers[21] in 1968, and this contributes to offset noise in diode arrays. Briefly, charge pumping is a net flow of current into the substrate from the drain and source diffusions which occurs when the gate voltage is pulsed. When a gate pulse is applied, carriers are drawn into the channel from the drain and source diffusions. When the pulse is removed, not all the carriers return to the diffused regions, but some diffuse into the substrate and recombine there, leading to a net injection or "pumping" of charge into the substrate.

This effect occurs in the addressing transistors of a recharge sampling array, and differences in its magnitude from transistor to transistor contribute to offset f.p.n. The variations are largely determined by the dimensional tolerances of the channel, and assuming a tolerance of $\pm$ 0.5 μm on a channel of 20 μm x 5 μm, such variations will be about 10% r.m.s. of the nominal area. The charge pumped per cycle for a channel of this area is typically 10^{-2} pC [14], so the offset fixed pattern noise due to charge pumping is likely to be about 10^{-3} pC or about 6×10^{3} electrons.

c) Synchronous Noise

Synchronous noise occurs in recharge sampling arrays due to the coupling onto the video line of the address pulse via the gate to drain capacitance of the addressing transistor.

Assuming coincident address pulse edges, the charge removed at the fall of address pulse m would be exactly cancelled by the charge injected at the rise of address pulse m + 1. This assumes identical gate-drain capacitances (C_{dg}) for the transistors of both elements, and it is the variation from device to device of C_{dg} that leads to imperfect cancellation and hence to synchronous fixed pattern noise.

The feedthrough capacitance is typically 0.01 pF, with a r.m.s. variation of 10% [14]. For a 10V address pulse then, the charge injected or removed will be 0.1 pC, and the fixed pattern noise contribution will be about 10^{-2} pC, or 6×10^4 electrons.

Further synchronous noise can be introduced if a shift register of either the clocked load or bootstrapped type is used, where low amplitude feedthrough pulses are present on the non-selected outputs. Typical pulse amplitudes are 2V and these will be coupled to the video line by the transistor gate-drain capacitances. Thus the injected signal will be about n (0.02)pC or n (1.2×10^5) electrons. The contribution of this to synchronous noise is difficult to estimate, since this injected signal will, in a large array, be approximately constant irrespective of the element being addressed, since any variations in C_{dg} will be averaged out by scanning over the (n-1) addressed elements.

Table 2.3. shows typical levels of fixed pattern noise contributions from the above sources, computed for an array with characteristics as above, and with an element size of 250 μm x 40 μm. Shown for comparison is the typical saturation signal.

2.4.2. Fixed Pattern Noise in Voltage Sampling Arrays

As in recharge sampling arrays, quantum efficiency variations are a source of responsivity fixed pattern noise. Responsivity is however no longer dependent on diode area. There are additional sources of responsivity f.p.n. peculiar to voltage sampling arrays, namely variations in the gate capacitance, threshold voltage and β of the source follower transistor T2, and in the "on" resistance of the multiplexing transistor T3.

TYPE	ORIGIN	VALUE [1]	UNITS
RESPONSIVITY	DIODE AREA	5	%
OFFSET	I_L	$(5\times10^6)t_I$	ELECTRONS
	Q_P	6×10^3	ELECTRONS
SYNCHRONOUS	C_{DG}	6×10^4	ELECTRONS
SATURATION SIGNAL		2.5×10^7	ELECTRONS

DIODE AREA = $250\mu m \times 40\mu m$

1) t_I = INTEGRATION TIME (s)

TABLE 2.3 TYPICAL FIXED PATTERN NOISE COMPONENTS AND SATURATION SIGNAL IN A RECHARGE SAMPLING ARRAY AT ROOM TEMPERATURE

Offset variations originate from leakage current variations, and from charge pumping variations in T1, and also from variations in capacitive feedthrough in T1, β and threshold voltage in T2, and in "on" resistance of T3. It will be seen that offset and responsivity variations are to an extent interdependent in voltage sampling elements.

Synchronous noise is not a significant problem in voltage sampling arrays, since the output is a series of d.c. voltage levels, whilst the synchronous noise appears as transients between these levels, coincident with the rise and fall of the clocks.

The above sources of fixed pattern noise will now be examined in more detail.

(a) Responsivity Fixed Pattern Noise

Quantum efficiency variations, as in recharge sampling arrays, are small and typically contribute less than 1% of the total responsivity fixed pattern noise.

The gate capacitance of the source follower transistor shunts the diode capacitance consequently slightly reducing the responsivity. Variations in this gate capacitance are due to dimensional tolerances, and for a gate area of 12 μm x 8 μm and a tolerance of 0.5 μm, capacitance variations of 10% would be expected. The gate capacitance of such a transistor is about 0.04 pF[14], and for a diode area of 250 μm x 40 μm with a junction capacitance of 4 10^3 pF/cm^3, then the variation in the small signal responsivity G is given by :-

$$\frac{\Delta G\ (C_g)}{G} = \frac{\Delta C_g}{C_D + C_g} \qquad (2.28)$$

$$= 0.01$$

This term will be correspondingly larger for smaller area diodes.

The effects of variation in source follower β and threshold voltage, and multiplexing transistor "on" resistance are dependent on the type of output load used. As might be expected from the transfer characteristics described in Section 2.2.2., the virtual earth amplifier suffers from the worst responsivity fixed pattern noise. This noise contribution can be derived starting with Equation 2.22 to describe the equilibrium output voltage :-

$$V_o = - \frac{R_F}{R_3} \left[V_D - V_T + \frac{1 - \sqrt{1 + 2\beta_2 R_3 (V_D - V_T)}}{\beta_2 R_3} \right]$$

and differentiating with respect to V_D to obtain the small signal gain G :-

$$G = - \frac{R_F}{R_3} \left[\frac{\sqrt{1 + m} - 1}{\sqrt{1 + m}} \right] \qquad (2.29)$$

where $m = 2\beta_2 R_3 (V_D - V_T)$

ΔG, the peak-peak fixed pattern noise in G due to β_2 and R_3 variations is given by :-

$$\Delta G (\beta_2, R_3) = \frac{\partial G}{\partial \beta_2} \Delta \beta_2 + \frac{\partial G}{\partial R_3} \Delta R_3 \qquad (2.30)$$

where $\Delta \beta_2$ and ΔR_3 are the peak to peak variations in β_2 and R_3 respectively.

Now $$\frac{\partial G}{\partial \beta_2} = - \frac{R_F}{R_3} \frac{(V_D - V_T) R_3}{(1 + m)^{3/2}}$$

and $$\frac{\partial G}{\partial R_3} = - \frac{R_F}{R_3} \left[\frac{R_3 (V_D - V_T)\beta_2 + (1 + m) (1 - \sqrt{1 + m})}{R_3 (1 + m)^{3/2}} \right]$$

Inserting the above into Equation (2.30) and dividing by Equation (2.29) gives the responsivity f.p.n. :-

(2.31)

$$\frac{\Delta G}{G}\ (\beta_2,\ R_3) = \frac{m}{2(1+m)\ (\sqrt{1+m}-1)} \left[\frac{\Delta R_3}{R_3} + \frac{\Delta \beta_2}{\beta_2}\right] - \frac{\Delta R_3}{R_3}$$

Similarily, considering the effect of threshold voltage variations in T2,

$$\frac{\Delta G}{G}\ (V_T) = \frac{m}{2(1+m)\ (\sqrt{1+m}-1)} \left[\frac{\Delta V_T}{V_D - V_T}\right] \qquad (2.32)$$

A similar analysis applies for the resistive load output circuit, starting with Equation 2.18 for the equilibrium output voltage :-

$$V_o = \frac{R_L}{R_3 + R_L} \left[V_D - V_T + \frac{1 - \sqrt{1+2\beta_2\ (R_3 + R_L)(V_D - V_T)}}{\beta_2 (R_3 + R_L)}\right]$$

which leads to (2.33)

$$\frac{\Delta G}{G}\ (\beta_2,\ R_3)\ \frac{n}{2(1+n)\ (\sqrt{1+n}-1)} \left[\frac{\Delta \beta_2}{\beta_2} + \frac{\Delta R_3}{R_3 + R_L}\right] - \frac{\Delta R_3}{R_3 + R_L}$$

where $n = 2\beta_2\ (R_3 + R_L)\ (V_D - V_T)$.

and $$\frac{\Delta G}{G}\ (V_T) = \frac{n}{2(1+n)\ (\sqrt{1+n}-1)} \left[\frac{\Delta V_T}{V_D - V_T}\right] \qquad (2.34)$$

As would be expected it can be seen that the virtual earth solutions are a special case of the above with $R_L = 0$.

For the constant current load, starting with Equation 2.24.

$$V_o = V_D - V_T - I_L R_3 - \sqrt{\frac{2I_L}{\beta_2}}$$

The gain is given by, $G = \frac{dV_o}{dV_D} = 1$

and therefore

$$\frac{\Delta G}{G} \quad (\beta_2, R_3, V_T) = 0 \qquad (2.35)$$

Thus there is no contribution to the responsivity f.p.n. from these variations in transistor parameters in the case of the constant current load.

(b) Offset Fixed Pattern Noise

Assuming, as in Section 2.4.1., a room temperature leakage current density equivalent to 5.10^{10} electrons/s/cm^2, then for a diode of area 250 μm x 40 μm with a capacitance C_D = 0.4 pf, the decay rate will be about $2Vs^{-1}$ at the diode, with an offset variation, V_{os}, of a similar magnitude.

Therefore

$$\Delta V_{os} \ (I_L) = 2 \ t_I \ .V$$

where t_I = integration time

Charge pumping offset noise now depends on diode area, as the resulting offset voltage is inversely proportional to the sum of the diode and source follower gate capacitances. For a pumped charge of 10^{-2} pC and a variation in this of 10%. the array element described above would have

$$\Delta V_{os} \ (Q_p) = 2mV$$

There exists a coupling capacitance, C_F, between the diode and the gate of the charging transistor T1. Feedthrough of the charge pulse occurs, reducing the potential to which the diode is biased at the start of the integration. Variations in the feedthrough capacity lead to an offset f.p.n. component of :-

$$\Delta V_{os}\,(C_F) = V_{cp}\ \frac{\Delta C_F}{C_D + C_G} \qquad (2.36)$$

where V_{cp} = charge pulse voltage

ΔC_F = variation in feedthrough capacitance

C_F is typically 0.01pF, with a tolerance of 20% and assuming V_{cp} = 10V.

$$\Delta V_{os}\,(C_F) \approx 50mV$$

The contribution from the spread of source follower β's & thresholds, and multiplexing transistor 'on' resistances is again a function of the load used. For the virtual earth load, from Equation 2.22, the offset voltage referred to the diode potential can be written as :-

$$V_{os} = -V_T + \frac{1-\sqrt{1+m}}{\beta_2 R_3} \qquad (2.37)$$

Now $$\Delta V_{os}\,(\beta_2, R_3) = \frac{\partial V_{os}}{\partial \beta_2}\ \Delta\beta_2 + \frac{\partial V_{os}}{\partial R_3}\ \Delta R_3$$

and $$\frac{\partial V_{os}}{\partial \beta_2} = \frac{1}{\beta_2}\left[\frac{\sqrt{1+m}-1}{\beta_2 R_3} - \frac{V_D - V_T}{\sqrt{1+m}}\right]$$

Similarly
$$\frac{\partial V_{os}}{\partial R_3} = \frac{1}{R_3}\left[\frac{\sqrt{1+m}-1}{\beta_2 R_3} - \frac{V_D - V_T}{\sqrt{1+m}}\right]$$

and therefore

$$\Delta V_{os}\,(\beta_2, R_3) = \left[\frac{\Delta\beta_2}{2} + \frac{\Delta R_3}{R_3}\right]\left[\frac{\sqrt{1+m}-1}{\beta_2 R_3} - \frac{V_D - V_T}{\sqrt{1+m}}\right] \qquad (2.38)$$

Also

$$\Delta V_{os}(V_T) = \frac{\partial V_{os}}{\partial V_T} \Delta V_T$$

$$= \left[1 - \frac{1}{\sqrt{1+m}}\right] \Delta V_T \qquad (2.39)$$

For the resistive loads, the corresponding expressions become :-

$$\Delta V_{os}(\beta_2, R_3) = \left[\frac{\Delta\beta_2}{\beta_2} + \frac{\Delta R_3}{R_3+R_L}\right]\left[\frac{\sqrt{1+n}-1}{\beta_2(R_3+R_L)} - \frac{V_D - V_T}{\sqrt{1+n}}\right] \qquad (2.40)$$

and

$$\Delta V_{os}(V_T) = \left[1 - \frac{1}{\sqrt{1+n}}\right] \Delta V_T \qquad (2.41)$$

For the constant current load, the offset voltage, from Equation 2.24, is

$$V_{os} = -V_T - I_L R_3 - \sqrt{\frac{2I_L}{\beta_2}}$$

giving

$$\Delta V_{os}(\beta_2, R_3) = \sqrt{\frac{I_L}{2\beta_2}} \cdot \frac{\Delta\beta_2}{\beta_2} + I_L \Delta R_3 \qquad (2.42)$$

and

$$\Delta V_{os}(V_T) = \Delta V_T \qquad (2.43)$$

Values for the offset f.p.n. contributions described above are given in Table 2.4., calculated for the element as described there. It is interesting to note that the supposedly "fixed" offset noise does in fact have a signal dependence (Equations (2.38 and 2.40) except when a constant current load is used.

The situation becomes further complicated because of these offset variations. Due to the non-linearities inherent in the responsivity of a voltage sampling element, the offset variations themselves contribute some responsivity fixed pattern noise. An example of this problem is the variation of diode capacitance with diode potential. Variations in diode potential, usually classed as a source of offset noise, will also affect diode capacitance,which contributes to variations in responsivity. The situation is extremely complex and there is probably little to be gained from a detailed quantitative analysis.

2.4.3. Random Noise in Recharge Sampling Arrays

In Chapter One it was noted that for astronomical work, or indeed for any measurement system in which extensive post-readout processing was permissible, the fixed pattern noise could be reduced or even eliminated, and that the random noise was the limiting factor which determined the "sensitivity" of a detector array. The origins and characteristics of this random noise will now be described, firstly for recharge sampling arrays.

Leakage current is caused by events (i.e. thermal generation of electron hole pairs) which occur at random times. Because of this random timing, the leakage current will have an average value, but there will be a fluctuation in the instantaneous current. This fluctuation is known as shot noise. The shot noise is defined as the standard deviation of the instantaneous current.

		RESPONSIVITY $\frac{\Delta G}{G}$			OFFSET ΔV_{os}					
LOAD	CONDITIONS	(C_G)	(β_2, R_3)	(V_T)	$(I_L)^{1)}$	(Q_p)	(C_T)	(β_2, R_3)	(V_T)	SATURATION RANGE
RESISTIVE	$R_L = 1M\Omega$	1	1	0.1	$2t_I$	2	50	0.47	0.11	6
	$R_L = 100K\Omega$		4	0.5				1.28	0.14	
VIRTUAL EARTH			9	1				4.17	0.18	
CONST. CURRENT	$I_L = 1\mu A$		0	0				0.07	0.1	5.3
	$I_L = 10\mu A$							0.24		3.75
	$I_L = 50\mu A$							0.6		0.5
		%	%	%	V	mV	mV	V	V	V

DIODE AREA = $250\mu m \times 40\mu m$. $C_D = 0.4pF$ $C_G = 0.04pF$

$\beta_2 = (4 \pm 0.8)\mu A/V^2$, $R_3 = (10 \pm 2)\mu A/V^2$, $V_T = (4 \pm 0.1)V$

1) t_I = INTEGRATION TIME (S)

TABLE 2.4. TYPICAL FIXED PATTERN NOISE COMPONENTS AND SATURATION SIGNALS IN A VOLTAGE SAMPLING ARRAY AT ROOM TEMPERATURE

Assuming a Poisson distribution for the instantaneous leakage current, then the standard deviation is simply the square root of the time averaged current. Since we are interested in comparing noise levels with signal levels in terms of a number of detected photons, it is convenient to express the r.m.s. noise terms in units of electronic charge or "equivalent noise charge" (ENC).

The total leakage charge, Q_L, expressed in electrons is :-

$$Q_L = \frac{I_L \, t_I}{q}$$

where I_L = combined leakage current of photodiode and drain diffusion (See Section 2.4.1.)

q = the electronic charge

The r.m.s. noise term due to shot noise on the leakage current is given by

$$\text{ENC (leakage)} = \left[\frac{I_L \, t_I}{q} \right]^{\frac{1}{2}} \qquad (2.44)$$

Shot noise will also be present on the charge injected via the charge pumping effect, and again will be simply the square root of the injected charge.

Thus

$$\text{ENC (charge pumping)} = \left[\frac{Q_p}{q} \right]^{\frac{1}{2}} \qquad (2.45)$$

where Q_p = mean charge pumped per cycle

During the recharge operation, there will be an uncertainty in the level to which the diode capacitance is charged. This arises because of Johnson (thermal) noise in the "on" resistance of the addressing transistor.

Thermal noise in resistors is a random fluctuation in voltage across the terminals caused by the random motion of electrons within the resistor, each having an average kinetic energy of $\frac{3}{2}$ kT.

It can be shown [18], that this noise term is :-

$$\text{ENC (reset)} = \left[\frac{kTC_D \, (1-e^{-2t/RC_D})}{q^2} \right]^{\frac{1}{2}}$$

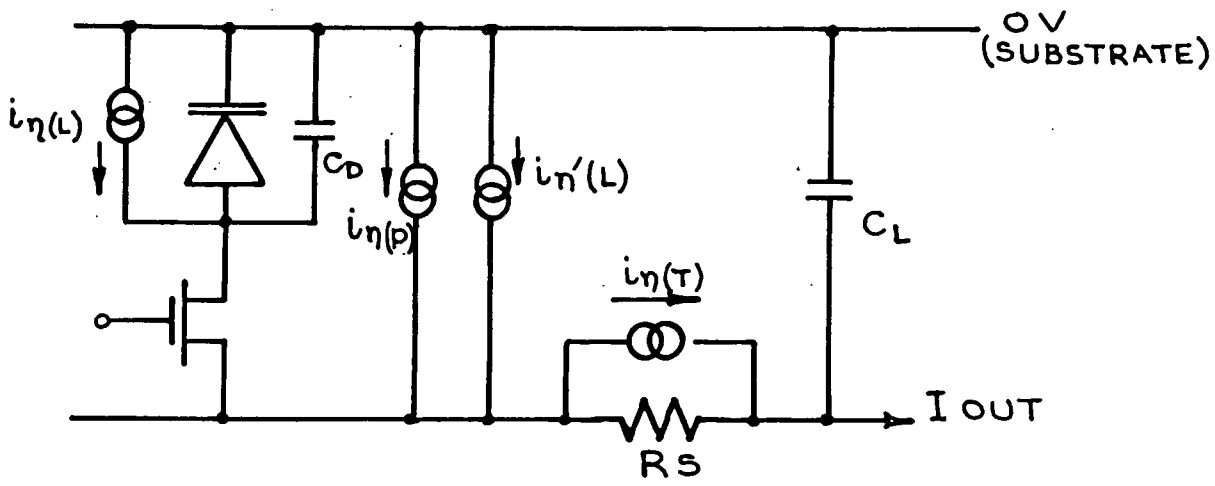
where

t = the length of the recharge pulse
R = the series "on" resistance of the addressing transistor

Typically, R = 10K and for a diode capacitance of 0.4 pF, the time constant $RC_D \approx 4nS$. The recharge pulse will usually be several microseconds long, and thus the above reduces to :-

$$\text{ENC (reset)} = \left[\frac{kTC_D}{q^2} \right]^{\frac{1}{2}} \qquad (2.46)$$

The above noise sources are shown in the noise model of Figure 2.20. Here, the noise components are represented as current sources. The leakage current shot noise has two components, i_L and i_L' representing the leakage currents in the photodiode and the addressing transistor drain diffusion respectively. Charge pumping shot noise is shown as a noise current i_p from the substrate, while reset noise is represented by a thermal noise current i_{nT} in the addressing transistor resistance. Table 2.5. lists the magnitudes of the various noise components for an array with the parameters as described there.



$i_{\eta(L)} = i_{\eta'(L)}$ = THERMAL LEAKAGE SHOT NOISE IN PHOTODIODE AND VIDEO LINE

$i_{\eta(p)}$ = CHARGE PUMPING SHOT NOISE

$i_{\eta(T)}$ = THERMAL NOISE IN ADDRESSING TRANSISTOR

FIG 2.20 RANDOM NOISE MODEL FOR A RECHARGE SAMPLING ELEMENT

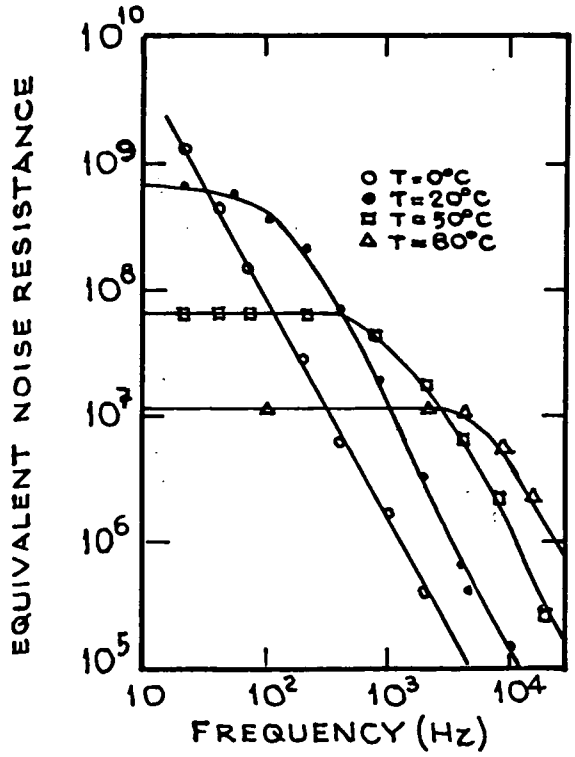


FIG 2.21 TEMPERATURE DEPENDENCE OF THE G-R NOISE SPECTRUM (AFTER YAU & SAH)

SOURCE	TERM	VALUE	UNITS
LEAKAGE CURRENT SHOT NOISE	ENC (I_L)	$2200\sqrt{t_i}$ [1]	electrons
CHARGE PUMPING SHOT NOISE	ENC (Q_P)	250	electrons
RESET NOISE	ENC (reset)	250	electrons

1) t_i = INTEGRATION PERIOD (s)

C_D = 0·4 pF I_L = 0·8 pA DIODE AREA = 250 μm x 40 μm

TABLE. 2.5. TYPICAL RANDOM NOISE COMPONENTS IN A RECHARGE SAMPLING ARRAY AT ROOM TEMPERATURE

2.4.4. Random Noise in Voltage Sampling Arrays

The three noise components described above in connection with recharge sampling arrays are also present in voltage sampling arrays. However, whereas it is convenient to express noise in terms of charges for a recharge sampling array where the output signal is in the form of a charge, it is convenient for voltage sampling arrays to describe the noise as an r.m.s. noise voltage.

Thus the shot noise on the leakage current becomes :-

$$V_n\ (I_L) = \frac{1}{C_D+C_G}\ (q\ I_L\ t_I)^{\frac{1}{2}} \qquad (2.47)$$

Similarly, the charge pumping shot noise becomes :-

$$V_n\ (Q_p) = \left[\frac{qQ_p}{(C_D+C_G)^2}\right]^{\frac{1}{2}} \qquad (2.48)$$

The reset noise on the diode capacitance is now due to the Johnson noise arising in the series resistance of T1, the recharge transistor. This becomes :-

$$V_n\ (\text{reset}) = \left[\frac{kT}{C_D+C_G}\right]^{\frac{1}{2}} \qquad (2.49)$$

There is now also Johnson noise in the combined series resistances of the source follower and multiplexing transistors T2 and T3 (and of the video line itself). This can be expressed as :-

$$V_n\ (\text{series}) = \sqrt{4kT\ R_s\ B} \qquad (2.50)$$

where

R_S = total series output resistance

B = bandwidth of observation

In practice, the bandwidth is often determined not by external filtering but by the low pass filter composed by the series output resistance R_S and the video line capacitance C_L, and therefore :-

$$B = (2\pi R_S C_L)^{-1}$$

and thus

$$V_n \text{ (series)} = \left[\frac{0.64\ kT}{C_L}\right]^{\frac{1}{2}} \qquad (2.51)$$

Generation - recombination noise occurs in the source follower transistor T2, and appears as a modulation of the drain current. Generation -recombination (g-r) noise arises from the exchange of carriers between defect centres in the depletion region, and the channel[22]. This exchange results in a fluctuation of the carrier density in the channel, and consequently of the drain current. This noise component is a low frequency phenomenon with a noise spectrum that is generally flat up to a cut off of about 100Hz. The magnitude of the generation-recombination noise depends on the impurity concentration, since the defect centres are usually impurity ions. It is also temperature dependent, and the effect of temperature on the noise spectrum as measured by Yau and Sah[23] is shown in Figure 2.21.

Plessey have found[14], that the magnitude of the g-r noise varies as the rate of change of gate voltage, and have determined the empirical relationship

$$V_n^{\circ}\ (g\text{-}r) = \left[0.4\ 10^{-6} \quad \frac{dV_G}{dt} \right]^{\frac{1}{2}} \qquad (2.52)$$

In this case, $\frac{dV_G}{dt}$ represents the discharge of the diode capacitance.

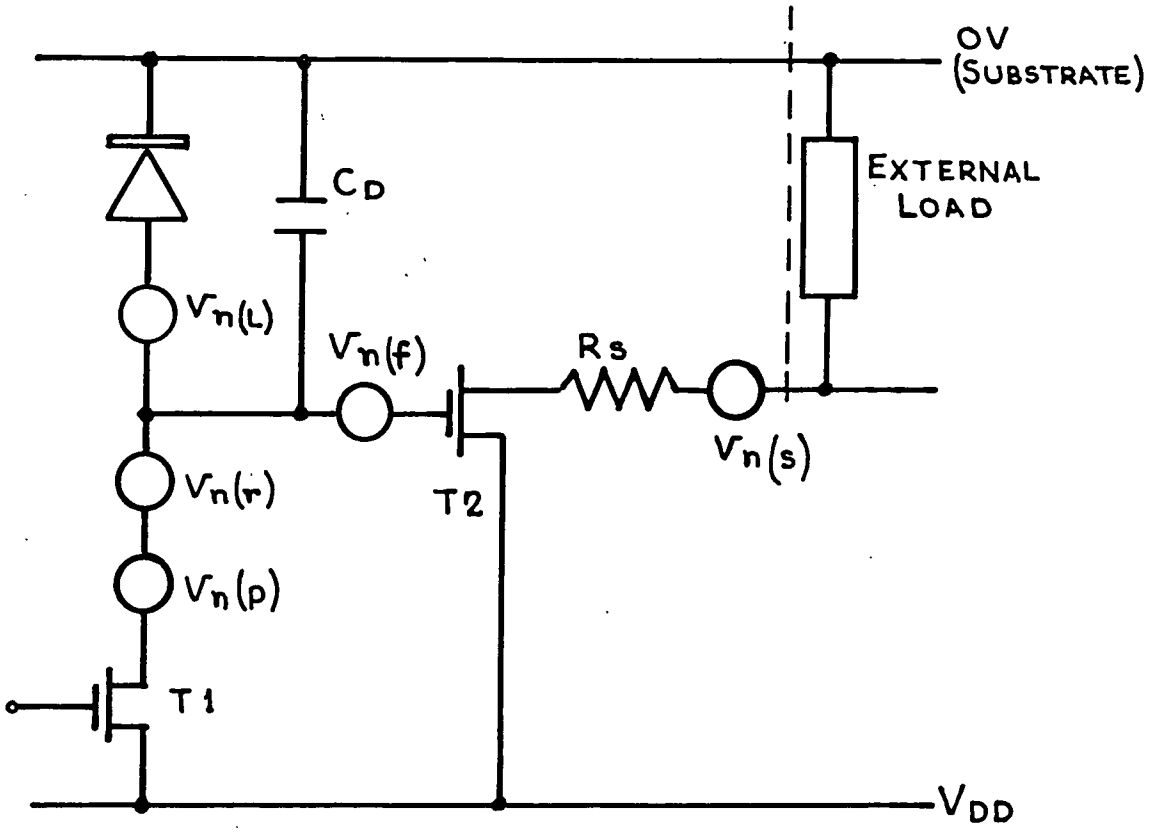
A further source of noise in MOS transistors is known as 1/f noise because of its reciprocal frequency dependence. It is also known as interface noise. The mechanisms behind this noise are not fully understood, and a variety of models to account for it have been suggested[22]. The significance of this type of noise in diode arrays has been described elsewhere[24] and the equation below has been derived which gives the likely range of the noise voltage.

$$V_n\ (1/f) = \left[(10^{-11} \rightarrow 10^{-7})\ \log_e \left[\frac{fmax}{fmin} \right] \right]^{\frac{1}{2}} \qquad (2.53)$$

where

fmax, fmin = the upper and lower frequency limits of observation respectively.

The noise model of the voltage sampling element, incorporating the above noise sources, is shown in Figure 2.22. It can be seen that all noise sources except the Johnson noise in the series output resistance are referred to the diode voltage. This latter source appears in series with the output resistance and its contribution depends on the characteristics of the output stage. Table 2.6 lists the magnitudes of these components for a typical voltage sampling array with the parameters shown there.



$V_{n(L)}$ = LEAKAGE CURRENT SHOT NOISE

$V_{n(r)}$ = RESET NOISE

$V_{n(p)}$ = CHARGE PUMPING SHOT NOISE

$V_{n(f)}$ = FLICKER NOISE

$V_{n(s)}$ = JOHNSON NOISE IN SERIES RESISTANCE R_S

FIG 2.22 RANDOM NOISE MODEL FOR A VOLTAGE SAMPLING ELEMENT

SOURCE	TERM	VALUE	UNITS
LEAKAGE CURRENT SHOT NOISE	$V_n(I_L)$	$820\sqrt{t_i}$ [1]	μV [4]
CHARGE PUMPING SHOT NOISE	$V_n(Q_P)$	91	μV
RESET NOISE	$V_n(\text{reset})$	97	μV
SERIES RESISTANCE NOISE	$V_n(\text{series})$	$\frac{51}{\sqrt{C_L}}$ [2]	μV
GENERATION - RECOMBINATION NOISE	$V_n(g\text{-}r)$	860	μV
1/f NOISE	$V_n(1/f)$	$.48\sqrt{B_w}$ [3]	μV

1) t_i = INTEGRATION PERIOD (s)

2) C_L = VIDEO LINE CAPACITANCE (pF)

3) B_w = BANDWIDTH OF OBSERVATION (DECADES)

4) FOR COMPARISON ONE ELECTRON CHARGE DEVELOPS ~ 0·36μV

TABLE 2.6. TYPICAL RANDOM NOISE COMPONENTS IN A VOLTAGE SAMPLING ARRAY AT ROOM TEMPERATURE

2.5. The Summary

Signal generation processes are essentially the same for both voltage sampling and recharge sampling arrays. The overall characteristics of the two types of array differ considerably, however, largely due to the extra non-linearities inherent in the voltage sampling array. Given these non-linearities, and the extra chip complexity of the voltage sampling array, at first sight the recharge sampling array is more attractive. There are some advantages to the voltage sampling array. One of these is that the output is in a much more convenient form. The other advantages lie in the opportunities for on-chip amplification and correlated double sampling. The next chapter describes a diode array with these facilities.

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CHAPTER THREE

The Plessey/RGO Diode Array and the Principles of its Operation

In this chapter, the design and development of a new type of linear MOS photodiode array will be described. This array is closely related to the voltage sampling arrays described in Chapter 2, but possesses a number of advantages over these.

3.1. The History of the Plessey/RGO Array Project

With the introduction of commercially available linear photodiode arrays in the early "Seventies", the astronomical community began to investigate the applications of such devices to optical astronomy. The most readily available devices were those produced by the Reticon Corporation[1)] in the U.S.A., and these have been used by many workers both as a direct optical imager and in intensified form. The known users to date (March 1979) are listed in Table 3.1.[2-12)]

Dr D.McMullan and others at the Royal Greenwich Observatory were interested in using a diode array for readout of electronographic tubes, and were concerned that the signal level from a single photoelectron event would be insufficient to overcome the readout noise. The use of higher pre-array gain was not attractive because this would entail substantial re-design of the electronographic tube. There were also doubts about the lifetime of an array under bombardment with higher energy electrons. The alternative was to introduce amplification into each element of the array, between the diode and the readout multiplexing transistor.

Investigator (s)	Observatory/Institute	Instruments	Array	Intens. or Direct	Ref
Campbell	David Dunlap Obs., Ontario, Canada.	Cassegrain Spectrograph	RL 256A/17 RL 256C/17	D	2
Dravins	Lund Observatory, Sweden	Solar Spectrograph and Plate Photometer	RL 128EC	D	3
Geary	Steward Observatory, Arizona, U.S.A.	Cassegrain Spectrograph	RL 128L	D	4
Livingston, Harvey, Slaughter and Trumbo	Kitt Peak National Observatory, Arizona U.S.A.	Solar Magnetograph	RL 512B/24	D	5
Mende, Chaffee and Shelley	Lockheed Palo Alto Research Laboratories, California, U.S.A.	----------	RL 512/17	I	6, 7
Smithson	Lockheed Solar Obs., California, U.S.A.	Solar Magnetograph	RL 512L	D	8
Vogt, Tull, Nather and Kelton	McDonald Observatory, Texas, U.S.A.	Coude Spectrograph	RL 256A/17) RL 1024B/24) RL 1024B/24	D I	9,10,11
Walker, et al.	U.B.C., Vancouver Canada	----------	RL 256A/17	D	12

ASTRONOMICAL USERS OF RETICON ARRAYS

TABLE 3.1.

This dictated the use of voltage sampling elements. A single element "array" was developed for the RGO by Plessey at the Allen Clark Research Centre, and this was mounted for evaluation into a Kron Electronic Camera tube. Tests on this device showed that single electron counting was feasible[13], and the development of a linear array using such elements was commenced.

Some of the early linear arrays were installed in electronographic tubes with a certain amount of success, but after a while it was decided to carry out investigations into the use of the arrays for direct optical imaging.

At the time that such tests were being started, the Nuclear Instrumentation Group at Durham University, under Dr. J.M. Breare, were exploring the possibility of moving from their previous field of detectors for high-energy physics into the development of detectors for astronomical imaging. It was agreed that the Durham Group should co-operate with Dr. McMullan on the further development of these arrays, and in the February of 1977, the author visited the R.G.O. for preliminary evaluation of the project, and returned to Durham with four of the prototype arrays. Since that time, the development work has been carried out within the Nuclear Instrumentation Group at Durham. The remainder of this chapter describes the design characteristics of the arrays themselves.

The array possesses a number of novel features. These can be subdivided into 3 regions, namely on-chip amplification, multiplexing and scanning techniques, and array organisation.

3.2. The Amplified Array Element

The circuit diagram representing the single element "array" manufactured for initial tests is shown in Figure 3.1. along with its idealised operating cycle. The multiplexing transistor that would be required in a multi-element array is not shown. Thus T2 here corresponds to T1, the charging "switch" of the conventional voltage sampled element (Figure 2.9), and T3 is the source follower "buffer" stage. The amplification takes place in T1. It was seen in Section 2.4.2. that for a diode element of 250 μm x 50 μm, a typical value for the diode capacitance C_D is 0.4 pF, whereas the gate capacitance of the source follower is around 0.04pF. The action of T1 is such that the diode potential V_D is maintained at a constant voltage $V_{ref} - V_T$ where V_T is the threshold voltage of the amplifying transistor T1, and V_{ref} is the gate potential applied to T1. First consider the effect on the responsivity and linearity.

3.2.1. Responsivity and Linearity

Any diode current, from either thermal leakage, photocurrent or from absorbed photoelectrons, discharges not the diode capacitance itself, but the gate capacitance of the source follower, which being smaller, consequently develops a greater voltage change. Thus the equation for the diode voltage, which was previously (Equation 2.13).

$$V_{(t)} = V_{DD}\left[1 - \frac{A}{(C_D+C_G)\,V_{DD}}\int_o^t (J_p + J_L)\ .dt\right]$$

now becomes, for the gate voltage V_G,

$$V_{G(t)} = V_{DD}\left[1 - \frac{A}{C_G}\int_o^t (J_p + J_L)\ .dt\right] \qquad (3.1)$$

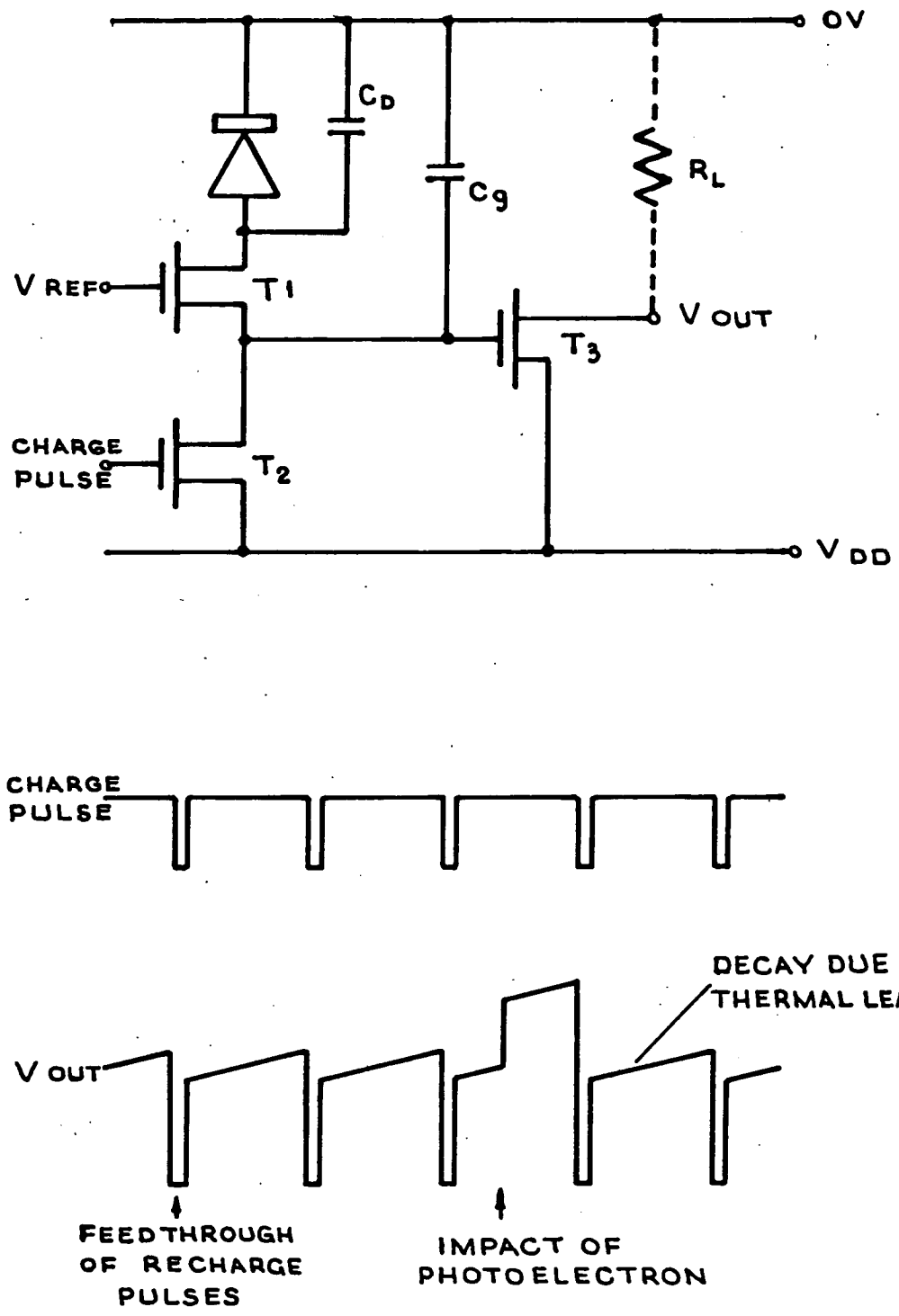


FIG 3.1 EXPERIMENTAL SINGLE DIODE ELEMENT & IDEALISED OUTPUT WAVEFORM

Several points arise from this. Firstly, there is an effective voltage gain of $\frac{C_D+C_G}{C_G}$, which from the example above is typically 10.

Secondly any benefits of larger diode area are no longer negated by the associated increase in diode capacitance.

Some of the inherent non-linearities of conventional sampling arrays are removed.

In the conventional array, variations in diode capacitance with diode voltage introduced non-linearities. In this element, the signal voltage is developed acoss C_G, the gate-capacitance. This is a MIS (metal-insulator-silicon) capacitance rather than a depletion layer capacitance and as such is not voltage dependent.

Another problem in the conventional array is the variation in depletion layer width with diode voltage, which makes both the leakage current and the quantum efficiency functions of the integrated signal. In the amplified element, the diode bias is constant. Furthermore, the diode bias may be kept small, in order to reduce the leakage current (refer to Equation 2.6).

The above advantages are not obtained without drawbacks, however. The chip complexity is increased, not only by the additional device per element, but also by the addition of a extra supply rail (V_{ref}). This will inevitably reduce yields. We must also consider the noise characteristics of the new element.

3.2.2. Noise Characteristics

Responsivity fixed pattern noise is increased when compared with the conventional voltage sampling array. In the conventional array, responsivity is independent of diode area. From Equation 3.1. this can be seen to no longer be true, and variations in diode area will now contribute to responsivity variation. In the conventional array, variations in responsivity due to variations in C_G, the gate capacitance of the source follower, were "damped" by the presence of the larger diode capacitance in parallel. From Equation 2.28,

$$\frac{\Delta G}{G}\ (C_G) = \frac{\Delta C_G}{C_D+C_G}$$

and this now becomes for the amplified element,

$$\frac{\Delta G}{G}\ (C_G) = \frac{\Delta C_G}{C_G} \qquad (3.2)$$

Thus this component of responsivity f.p.n. is increased by the "gain" factor.

Random noise is also affected. Referring noise sources now to the gate voltage of the source follower, then the thermal leakage shot noise and the charge pumping shot noise now becomes (cf. Equations 2.47 and 2.48).

$$V_{n\ (I_L)} = \frac{1}{C_G}\ \sqrt{qI_L t_i} \qquad (3.3)$$

and

$$V_{n(Q_p)} = \frac{1}{C_G}\ \sqrt{q\ Q_p} \qquad (3.4)$$

Thus these noise components have simply been increased by the "gain" factor, so there is no change in signal-to-noise ratio.

For the reset noise, however, Equation 2.49 now becomes :-

$$V_{n\ (reset)} = \sqrt{\frac{kT}{C_G}} \qquad (3.5)$$

an increase equivalent to only the root of the "gain" factor.

There is now an additional MOS transistor in the signal chain (the "amplifying" transistor, T_1) in which generation-recombination and 1/f noise arise. These components will be similar to those arising in the source follower transistor [14], and referring back to Table 2.6, it is apparent that this more than offsets the reduced reset noise.

In general then, both fixed pattern noise and random noise are worse in the amplified element than in the conventional counterpart. The time response of the circuit is also worsened. It will be shown (p.89) that double sampling can be used to reduce the random and fixed pattern noise.

3.2.3. Response Time

The time response of the element is best illustrated by considering a step injection of carriers into the diode, such as would be caused by sudden exposure to light, or by the absorption of a photo-electron.

In general, the current through T1, that is the current through the diode, can be described by the usual ideal MOS equation, as :-

$$I_{ds} = \frac{\beta}{2} \left[V_{ref} - V_D - V_T \right]^2$$

$$= \frac{\beta}{2} V_E^2$$

where V_E is the effective gate voltage.

With only leakage current flowing in the diode, then the effective gate voltage has a steady value $V_{E(o)}$ given by :-

$$V_{E(o)} = \sqrt{\frac{2I_L}{\beta}}$$

A step injection of carriers into the diode will result in a loss of charge ΔQ from the charge stored on the diode capacitance. This charge will be replenished by an increase in the current through T1.

If at a time t, a certain fraction α of this charge has been replaced, then the instantaneous effective gate voltage will be :-

$$V_{E(t)} = V_{E(o)} + (1-\alpha) \frac{\Delta Q}{C_D}$$

and the current through T1 is now :-

$$I_{(t)} = I_L + \frac{d}{dt} (\alpha \Delta Q)$$

$$= \frac{\beta}{2} \left[V_{E(o)} + (1-\alpha) \frac{\Delta Q}{C_D} \right]^2$$

Integrating the above to obtain α, the fraction of charge transfered at a time t, gives [15]

$$\alpha = \frac{((\exp t/B) - 1)(1 + \frac{B}{A})}{(1 + \frac{B}{A})(\exp t/B) - \frac{B}{A}} \qquad (3.6)$$

where

$$A = \frac{2C_D^2}{\Delta Q} \quad \text{and} \quad B = \frac{C_D}{\sqrt{2I_L\beta}}$$

when $I_L = 0$, this simplifies to

$$= \frac{(t/B)\,(1 + \frac{B}{A})}{(1 + \frac{B}{A})(1 + \frac{t}{B}) - \frac{B}{A}}$$

$$= \frac{1}{1 + (A/t)} \qquad (3.7)$$

The absorption of a photoelectron of energy 20 keV would be expected to generate a step signal of about 6000 carriers (assuming 3.5 eV/electron hole pair). Figure 3.2. shows the fraction of such a charge transferred after time t for a diode capacitance of 0.4 pF, $\beta = 4\ \mu A/V^2$ and leakage currents of $5\ 10^6$, $5\ 10^4$ and 0 carriers/second. This figure indicates time constants of the order of hundreds of microseconds. For smaller injections of charge, the transfer is slower. This points to a possibility of lag problems for small signals in cooled arrays. In fact at low temperatures additional slow time constants come into effect. These will be mentioned later.

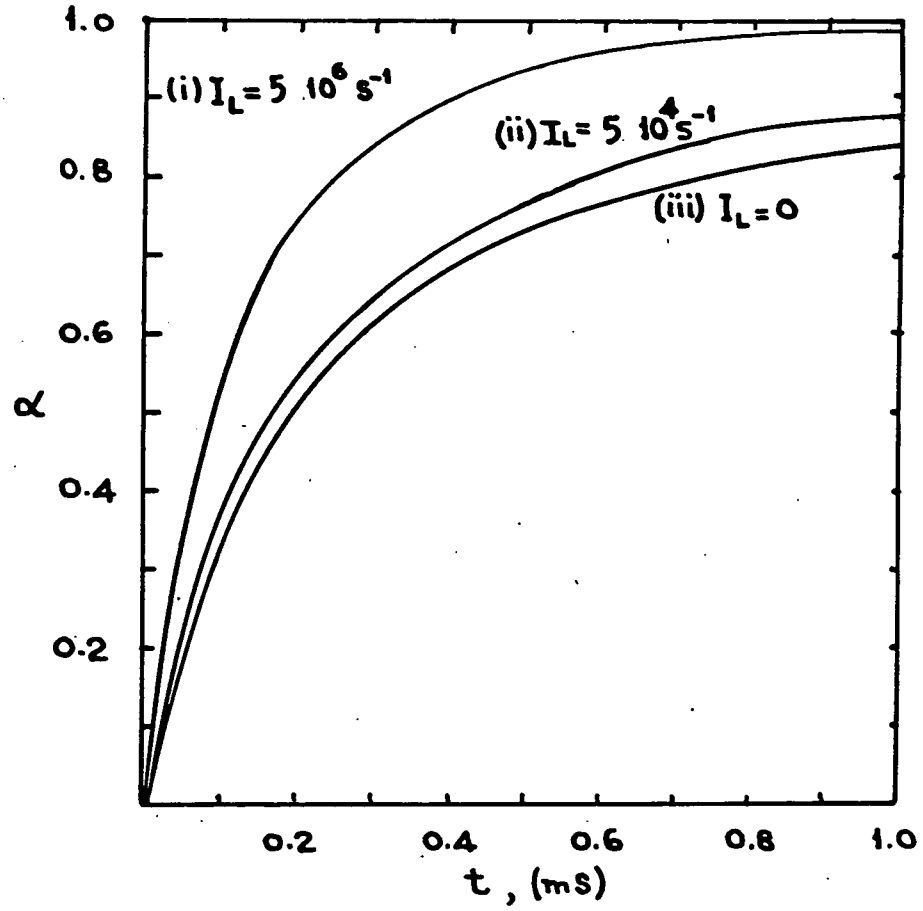


FIG 3.2 α AS A FUNCTION OF TIME FOR LEAKAGE CURRENTS OF i) 5×10^6 carriers/sec.
ii) 5×10^4 carriers/sec.
iii) 0

3.3. Multiplexing and Scanning Techniques

The multiplexing of the Plessey array is rather unique, in that diodes are addressed as pairs. This will be explained in detail in a later section, as to include it now would obscure discussion of some of the other techniques to be described.

In a conventional voltage sampling array, the recharge pulse for an element, m, is taken from the (m+1) th bit of the scanning register, as shown in Figure 2.19. In other words, recharge and readout are inseparable, with each element being recharged immediately after it has been readout.

In the Plessey array, the recharge can be controlled independently of the readout. This considerably increases the versatility of the array and gives rise to two useful techniques, namely double sampling and non-destructive readout.

3.3.1. Double Sampling

The concept of double sampling is illustrated in Figure 3.3. A recharge pulse and an address pulse are applied to the element during the same phase of the shift register cycle. The recharge pulse is shorter than the address pulse and occurs within it, as shown.

During the first part of the output waveform, from time t_o to t_1, the output voltage is approximately proportional to the integrated light flux since the last recharge. At time t_1, the gate capacitance C_G is recharged to V_{DD}, and for time t_2 to t_3, the output voltage represents the recharged, or no light state. There exists some slope on these output levels due to the effects of illumination and thermal leakage currents during the address pulse. The output signal has now been sampled both immediately before and after the recharge pulse. By subtracting the two signals in the external processing electronics, all fixed pattern offset noise can be removed from the output signal.

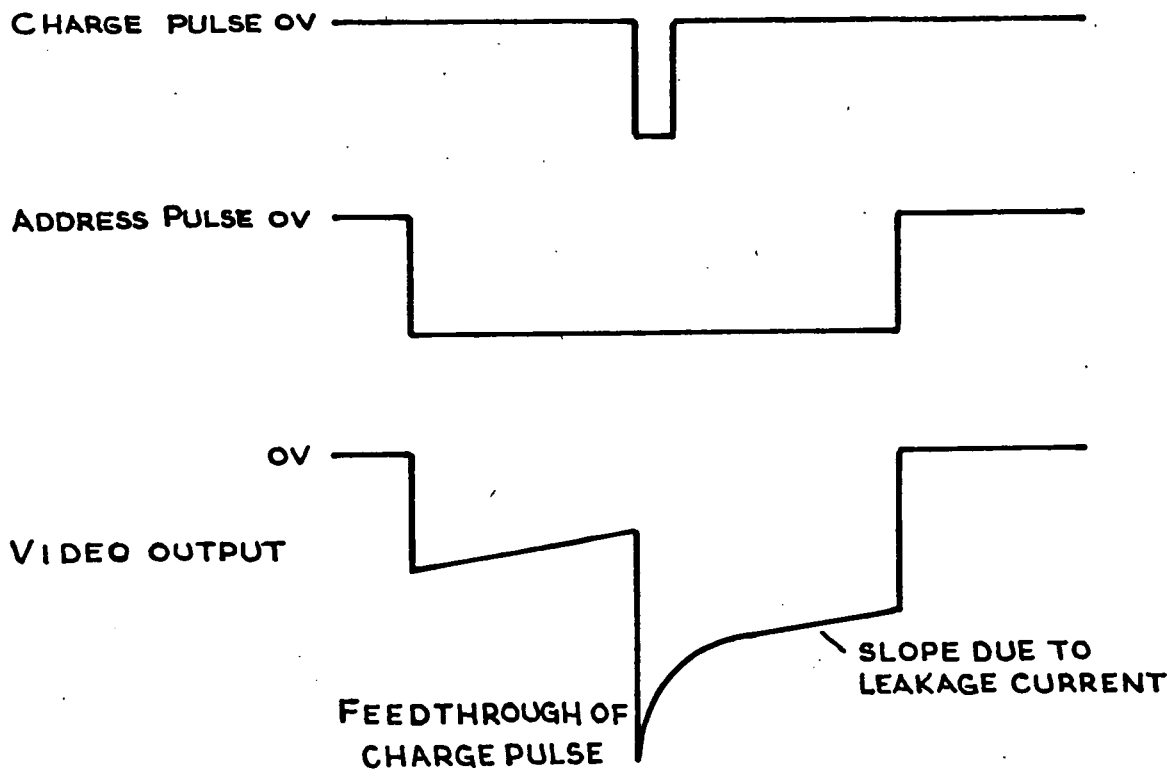


FIG 3.3 DOUBLE SAMPLING

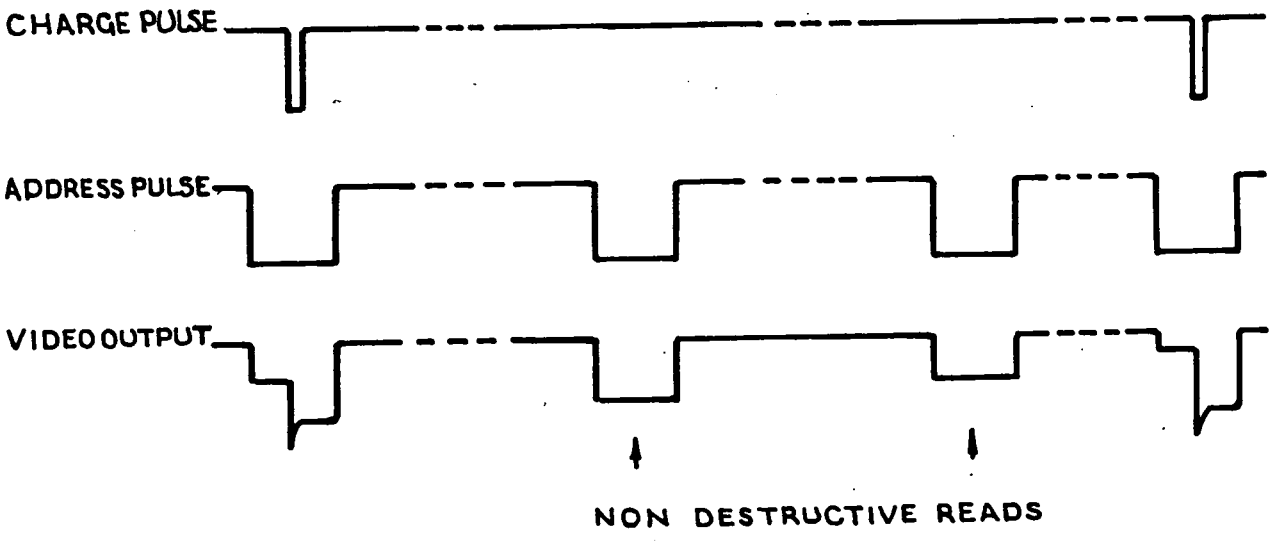


FIG 3.4 NON DESTRUCTIVE READOUT

A further and potentially more valuable benefit is derived from double sampling, namely the reduction of low frequency components of random noise. Components of noise with a period of greater than the width of the charge pulse (or more strictly in any practical system, greater than the sampling interval) will be highly correlated between the two samples and will thereby be reduced by the subtraction of the two samples.

Double sampling will not reduce the shot noise components of the leakage current, nor the Johnson noise on the series output resistance, as these have an essentially "white" spectrum.

Charge pumping shot noise and reset noise are functions of the recharging mechanism itself, and are quantised at the falling edge of the recharge pulse, resulting in random offsets which are time invariant until the next recharge pulse. Thus neither of these can be reduced by double sampling.

3.3.2. Non Destructive Readout

Independent access to the recharge pulse leads to the possibility of non-destructive readout of the array. Provided that the frame time, that is the time taken to scan the array once, and which hitherto has necessarily been equal to the integration time, is small compared to the time taken for the array to saturate, then the recharge pulse can be omitted for one or more such frames. Such a sequence for a single element is shown in Figure 3.4.

In this way, the decay of voltage on C_G can be monitored without recharging, and the integration time can be adjusted to provide maximum signal without saturation, and therefore a high signal-to-noise ratio.

Furthermore, it was shown in Chapter One and Appendix A, that by averaging a number of successive non-destructive readouts, that the effective random noise can be reduced, thereby improving Detective Quantum Efficiency.

3.3.3. Multiplexing Circuitry

The circuitry by which double sampling and non-destructive readout are facilitated is shown in Figure 3.5. As in the conventional array, the select pulse from the scanning register switches a multiplexing transistor (in this case T5), connecting the output of the source follower T3 onto the video line. The same select pulse also switches transistor T4, which connects the charge pulse line through to the gate of T2, the re-charge transistor. At the appropriate time, a pulse is applied to the charge pulse line recharging the selected element.

Non destructive readout is achieved simply by not applying the pulses to the charge pulse line.

3.3.4. The Scanning Register

The scanning register used in the Plessey array is of the "bootstrapped" MOS variety as described in Chapter 2.3.5. The circuitry of this register is shown in Figure 3.6., and is a design developed by Plessey [14]. The "bootstrapping" is achieved using a capacitor rather than with a varactor as in the circuit of Figure 2.17.

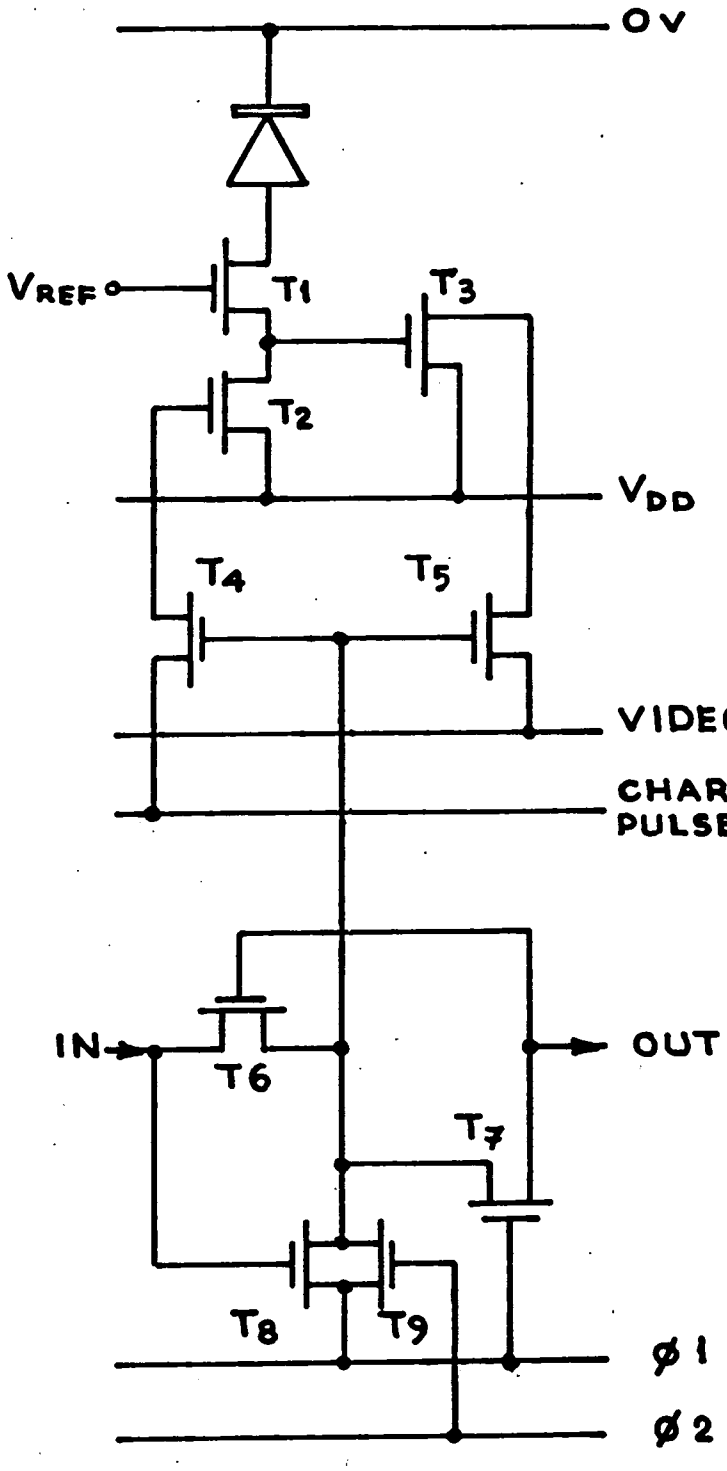


FIG 3.5 SINGLE ELEMENT WITH MULTIPLEXING AND ADDRESS REGISTER CIRCUITRY

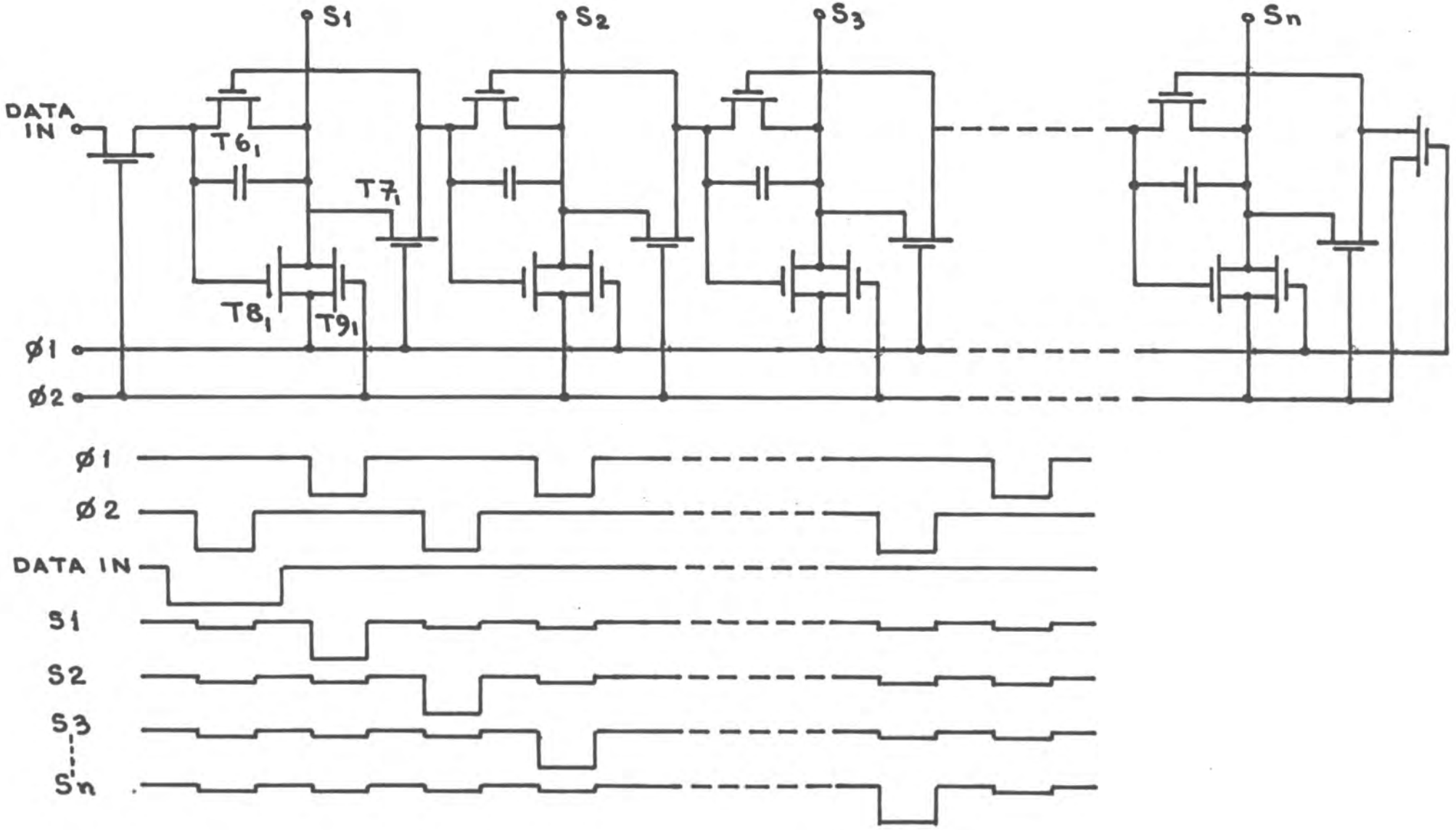


FIG 3.6. BOOTSTRAPPED SCANNING REGISTER.

Consider S_2, the output from the second stage, assuming there has been as output from the previous stage (S_1) during $\emptyset$ 1. This will have charged up capacitors C_2 to V', which will hold $T8_2$ on. Without bootstrapping, during $\emptyset 2$, S_2 would charge up to $V' - V_T$ through $T8_2$. The bootstrap capacitor feeds through a sufficient fraction of the voltage swing to overcome the threshold, and S_2 is charged up to the full clock voltage $V_\emptyset$. Meanwhile, $T7_2$ will have charged up C_3, the capacitor of the next stage, to $V_\emptyset - V_T$. At the end of $\emptyset 2$, S_2 is discharged through $T8_2$, which conducts until C_2 is discharged by $T6_2$. $T9_2$ prevents build up of excessive potential on S_2 due to charge pumping in $T7_2$.

There are a number of reasons why this circuit is particularly suited to diode array applications. Power dissipation is limited to $P = CV^2f$ (that is, there is no. d.c. dissipation). The only power lines required are the clock lines themselves, hence reducing layout complexity. High scanning rates (up to 10MHz) are achievable. Also, the scanning pulses supplied to the array elements have the same width and amplitude as the clock phases, allowing considerable external control over the operation of the register.

3.4. Organisation and Layout of the Plessey Array

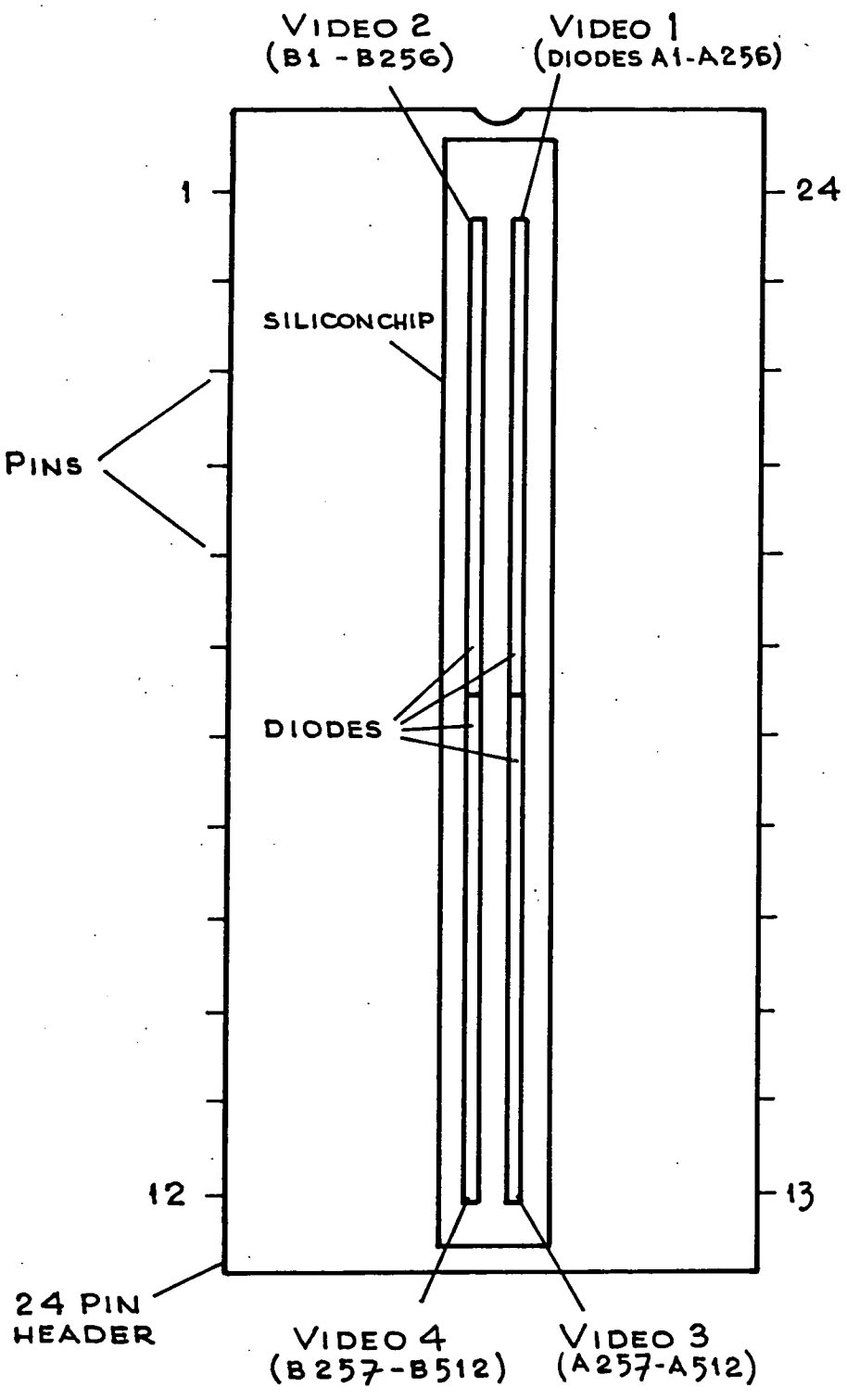
Figure 3.7 shows an overall view of the Plessey array as used for optical imaging. This can be compared with the photograph of the device in Figure 3.8. The devices are arranged electrically as four arrays of 256 diodes each, mechanically laid out as 2 parallel lines of 512 diodes each. This arrangement is designed to facilitate the recording of a stellar spectrum on one line, and a "sky background" spectrum on the second line. The silicon "chip" on which the devices are fabricated is mounted onto a 24 pin DIL header, and the array is covered with a thin quartz window.

3.4.1. Geometrical Layout and Electrical Interconnection

In order to achieve the desired 45 μm pitch, each "line" of 256 diodes is laid out as two interlaced arrays of 128 diodes each, with the circuitry associated with each array mounted on opposite sides of the line of diodes. This can be seen from the photograph of Figure 3.9, and Figure 3.10, a simplified layout diagram.

This shows the "left hand" end of the array, that is line 1 (diodes A1 to A256) and line 2 (diodes B1 to B256). The diodes are laid out on a 45 μm pitch. By laying out the associated circuitry on alternate sides of the array as shown, a space of 90 μm is available for the register element and switching transistors.

The "chip" is entirely symmetrical around the centre line shown on Figure 3.10. The left and right hand sides are totally isolated electrically. Each line of 256 diodes has its own video output line. The circuits on the left hand side of the array, that is the upper and lower sections of A(1-256) and B(1-256), all share the same V_{ref}, V_{DD} $\emptyset 1$, $\emptyset 2$ and Load Shift Register (LSR) lines. These have been omitted from the diagram for clarity. It is the video and charge pulse lines which are of interest.



PIN Nº	FUNCTION
1	VIDEO 1
2	VIDEO 2
3	
4	
5	V REF
6	VDD
7	VDD
8	V REF
9	
10	VIDEO 4
11	VIDEO 3
12	SUB STR
13	SUB STR
14	L.S.R
15	
16	CP1
17	CP2
18	Ø2
19	Ø1
20	Ø1
21	Ø2
22	CP2
23	CP1
24	LSR

FIG 3.7 LAYOUT AND PIN CONNECTIONS OF PLESSEY / RGO ARRAY ON 24 PIN HEADER

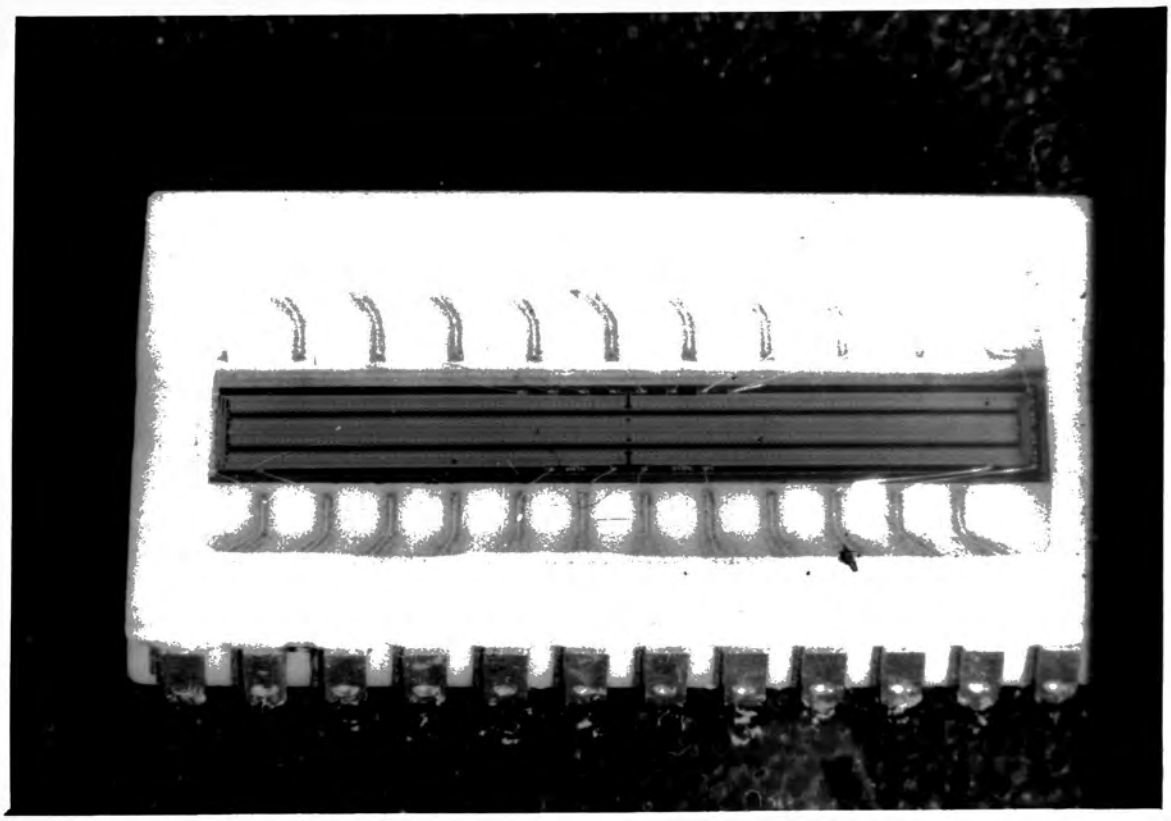


FIG.3.8

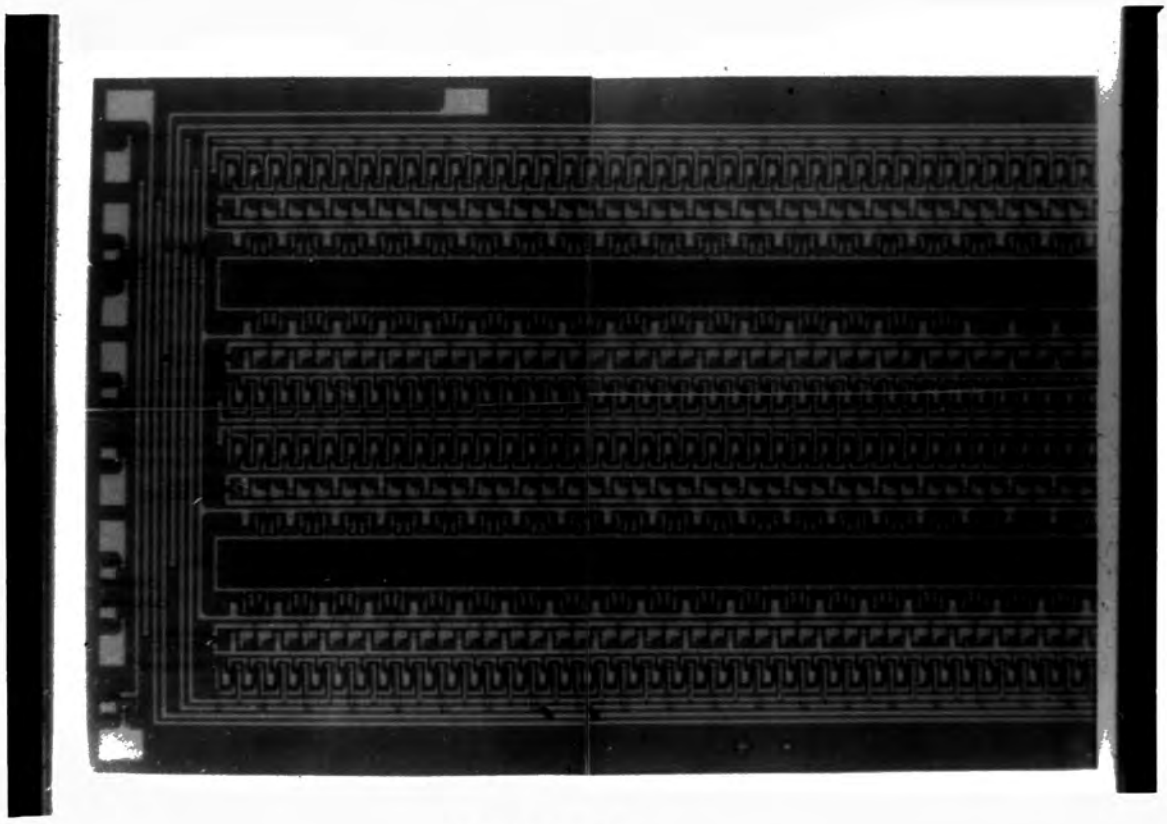


FIG.3.9

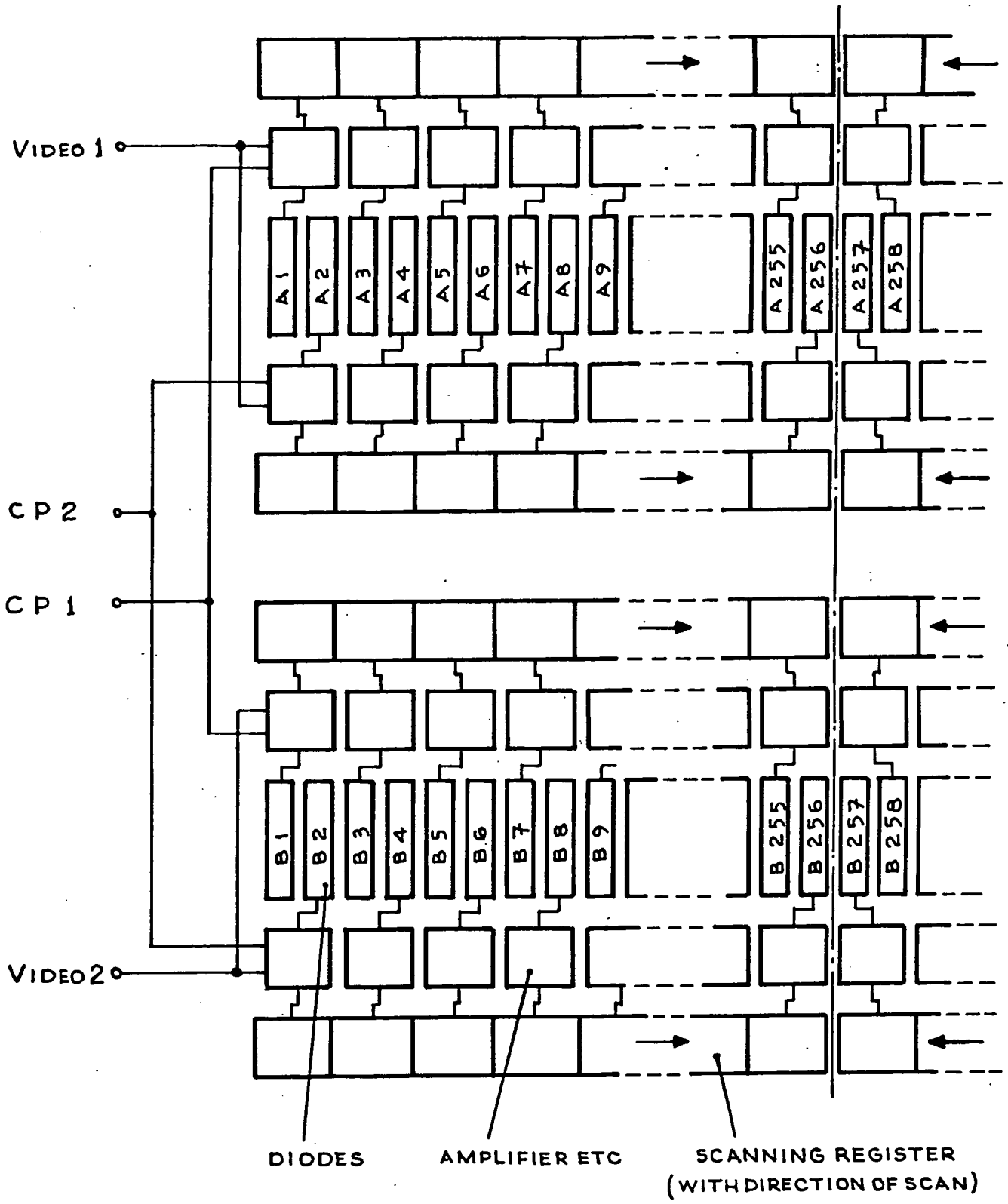


FIG 3.10. INTERLACING OF ELEMENTS
(VIDEO LINES 1 & 2)

Note that each "side" of an array is served by a different charge pulse line. Odd numbered elements are connected to line CP1, and even numbered elements to line CP2.

Now consider the scanning of Line 2, that is diodes B1 to B256. Scanning is initiated by a Load Shift Register (LSR) pulse. Both the upper and lower registers then clock at the same rate and simultaneously. Thus during the first Ø1 clock phase, diodes B1 and B2 are addressed together. Their video lines are common, however. The way in which the information content of the two diodes is seperated is discussed in the next section. However, before leaving the subject of chip layout, it is interesting to compare the schematic of Figure 3.10 with the x-ray photograph of Figure 3.11. This shows a small portion at the bottom left corner of the chip. The various lines and areas of interest are marked on this photograph. Note the device between the bonding pad for V_{ref} and the line itself. This is a gate protection diode to prevent damage to any gates brought out to external pins from floating potentials or static charges.

3.4.2. Diode Pairing

Because of the interlacing described above, the video outputs of adjacent elements such as B1 and B2 are presented onto a common video line simultaneously. Individual signals can be recovered by appropriate timing of the charge pulses CP1 and CP2. This is illustrated in Figure 3.12. The following discussion assumes that the video line acts as a true voltage summing junction. The validity of this assumption will be examined later.

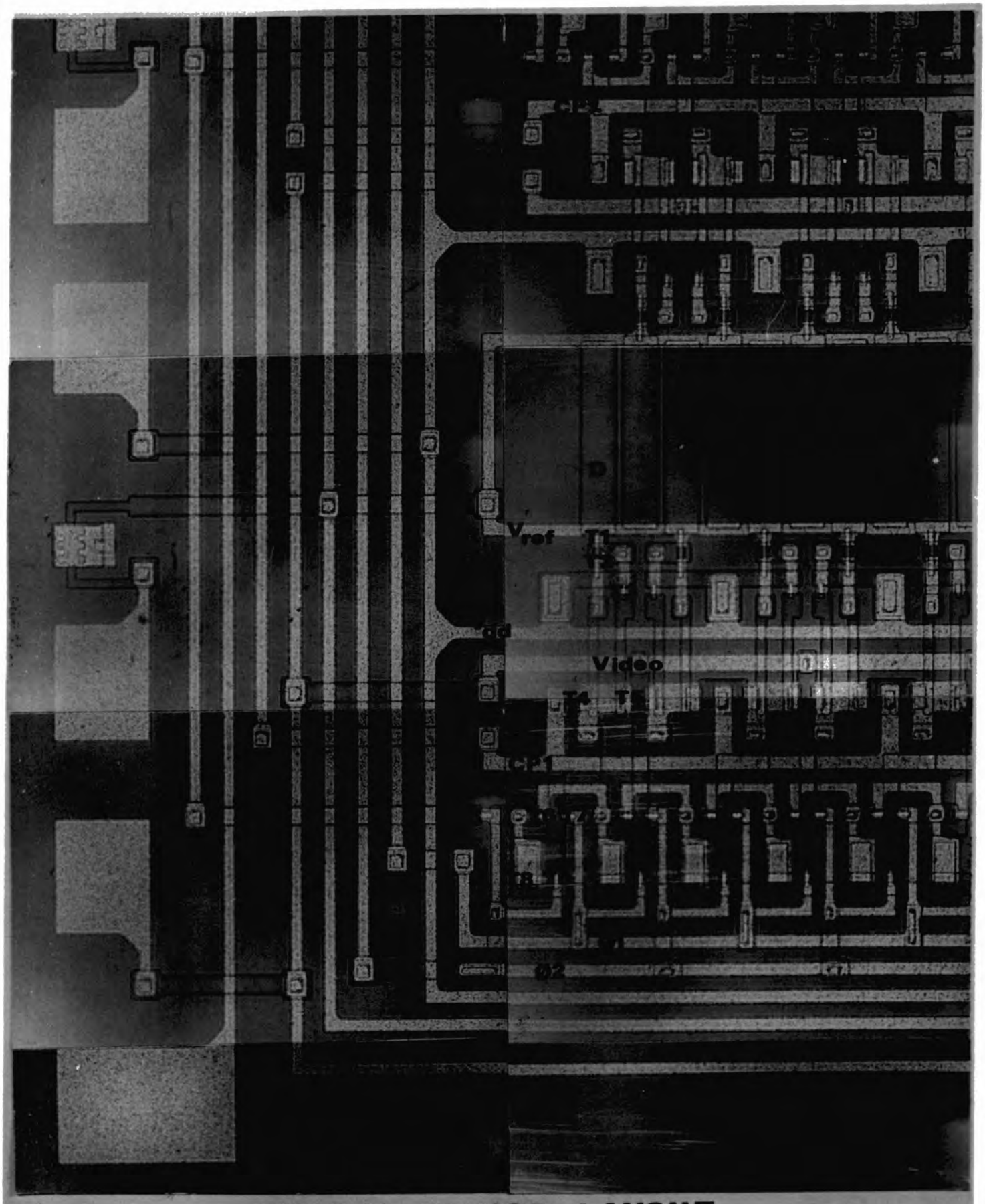


FIG.3.11. DEVICE LAYOUT

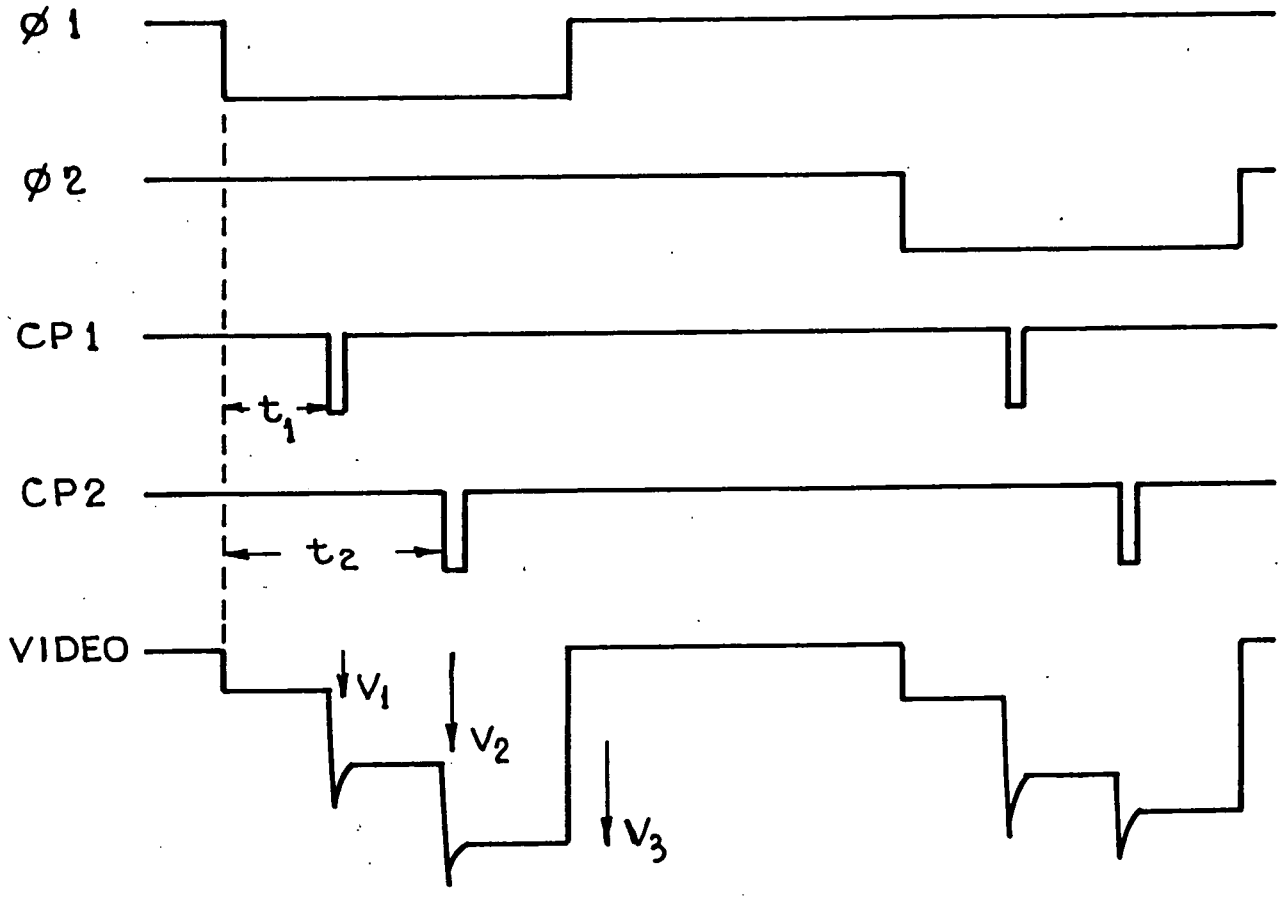


FIG 3.12 THE USE OF TWO CHARGE PULSE LINES TO ACHIEVE INTERLACING

At the beginning of the relevant clock phase (Ø1 for diode elements B1 and B2), the output voltages from the two elements are added together and therefore the voltage on the video line is :-

$$V_1 = V_{XA} + V_{XB}$$

where V_1 is the voltage on the video line until time t_1.

V_{XA} is the voltage at the output of element A (in this case B1) following an exposure.

V_{XB} is the voltage at the output of element B (in this case B2) following exposure.

At a time t_1 inside the clock phase Ø1, a charge pulse on line CP1 recharges the element A to its recharged potential V_{RA}.

The voltage on the video line is now

$$V_2 = V_{RA} + V_{XB}$$

At a later time t_2, still within the clock phase Ø1, a charge pulse on line CP2 recharges element B up to its recharge output potential V_{RB}, and thus now the voltage on the video line is :-

$$V_3 = V_{RA} + V_{RB}$$

The individual signals can be recovered by subtracting levels from each other. For example, the signal level on element A is :-

$$V_{SA} = V_{XA} - V_{RA}$$

$$= V_1 - V_2 \qquad (3.8\ (a))$$

and for element B

$$V_{SB} = V_{XB} - V_{RB}$$

$$= V_2 - V_3 \qquad (3.8\ (b))$$

As mentioned previously, this treatment assumes that the video line acts as a true voltage summing junction. Now consider how valid this assumption is for some practical output circuits.

The general case is represented by Figure 3.13 (a). This shows the output circuits of the two elements as source followers with a gate voltage V_G, connected to the external load through resistors R_m, representing the "on" resistance of the video multiplexing transistors. We wish to derive the output voltage V_o in terms of the two gate voltages V_{GA} and V_{GB}. In order to simplify the derivations, we replace the gate voltages V_{GA}, V_{GB} with effective gate voltages V_A and V_B, where

$$V_A = V_{GA} - V_{TA}$$

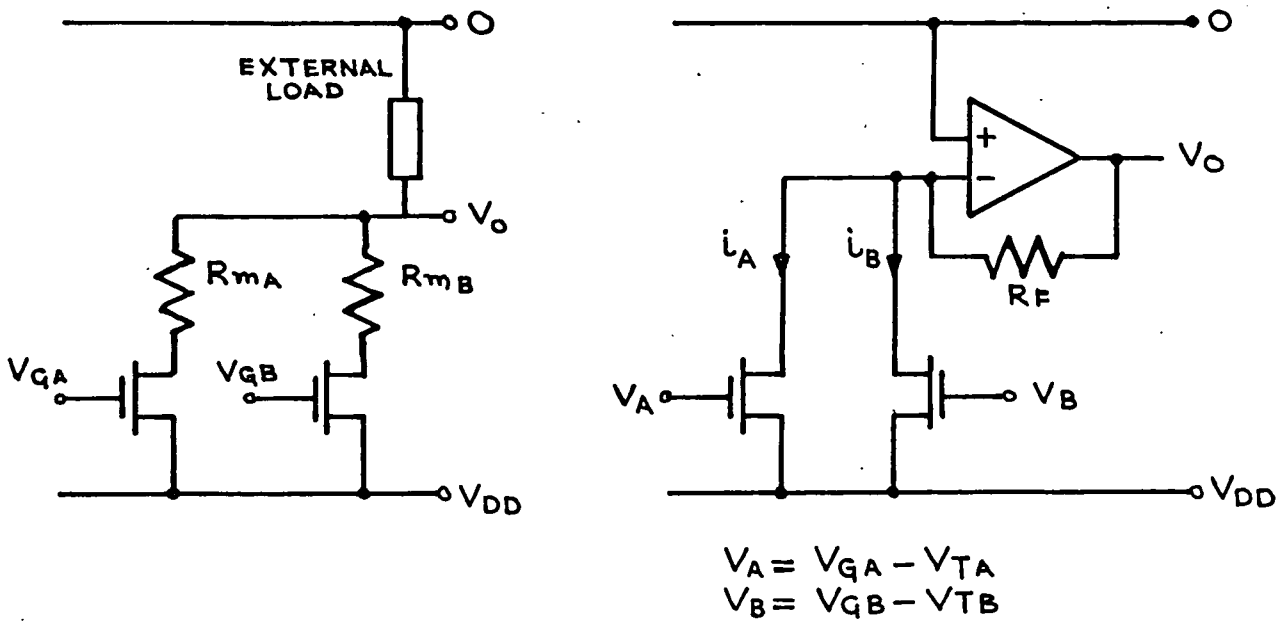
and $$V_B = V_{GB} - V_{TB}$$

where V_{TA} and V_{TB} are the threshold voltages of the two source followers. We will also assume that the two elements have identical characteristics thus.

$$\beta_A = \beta_B$$

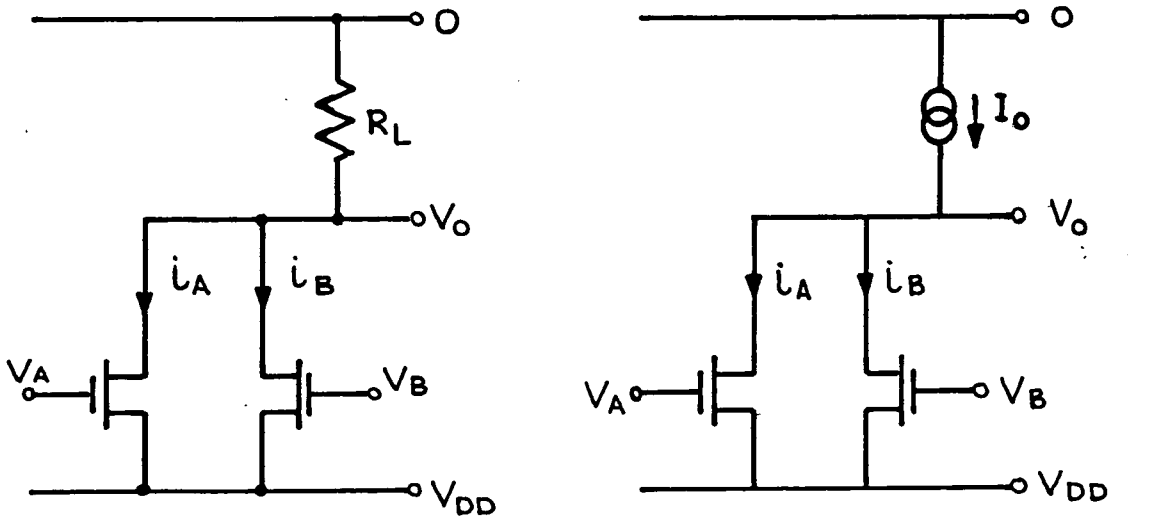
$$V_{TA} = V_{TB}$$

and $$R_{mA} = R_{mB} = 0$$



(a) GENERAL CASE

(b) SIMPLIFIED VIRTUAL EARTH LOAD



(C) RESISTIVE LOAD

(d) CURRENT SOURCE LOAD

FIG 3.13 SUMMING JUNCTIONS WITH VARIOUS LOADS

These are obviously never true in practice. However, the results of the derivations will serve to illustrate the relative merits and demerits of the three possible types of external load, namely the virtual earth, the resistive load and the constant current load.

First, the virtual earth load as illustrated in Figure 3.13 (b).

Recalling the ideal MOS Equations

$$i_A = \frac{\beta}{2} V_A^2 \quad \text{and} \quad i_B = \frac{\beta}{2} V_B^2$$

now,

$$V_o = -(i_A + i_B) R_F$$

$$= \frac{\beta R_F}{2} (V_A^2 + V_B^2) \qquad (3.9)$$

This result shows two points of interest. The first is the square law relationship. This in fact arises from the over simplification of making R_m zero. The true relationship is closer to that derived in Chapter 2 (Equation 2.22). However, what is apparent is that the output voltage is in fact a true sum of the voltages that would be obtained from each element separately. A more precise treatment, including the non-zero value of R_m has been derived by A.W. Campbell [16].

The resistive load case is illustrated in Figure 3.13 (c). Here

$$i_A = \frac{\beta}{2} (V_A - V_o)^2 \text{ and } i_B = \frac{\beta}{2} (V_B - V_o)^2$$

and $$V_o = (i_A + i_B) R_L$$

This gives the quadratic equation

$$2V_o^2 - 2 (V_A + V_B + \frac{1}{\beta R_L}) V_o + V_A^2 + V_B^2 = 0$$

Solving for V_o, we have (3.10)

$$V_o = \frac{1}{2} \left[V_A + V_B + \frac{1}{\beta R_L} - \sqrt{\frac{2(V_A+V_B)}{\beta R_L} + \frac{1}{\beta^2 R_L^2} - (V_A - V_B)^2} \right]$$

For the constant current load as in Figure 3.13 (d),

$$i_A = \frac{\beta}{2} (V_A - V_o)^2, \quad i_B = \frac{\beta}{2} (V_A - V_o)^2$$

and $$I_o = i_A + i_B$$

giving the quadratic equation

$$2V_o^2 - 2(V_A + V_B) V_o + V_A^2 + V_B^2 - \frac{2I_o}{\beta} = 0$$

Solving for V_o,

$$V_o = \frac{1}{2} \left[V_A + V_B - \sqrt{\frac{4I_o}{\beta} - (V_A - V_B)^2} \right] \qquad (3.11)$$

Note that as would be expected, the limiting case of the resistive load as $R_L \to \infty$ leads to the same result as the constant current load as $I_o \to 0$.

Referring to Equations 3.10 and 3.11 above, note the presence of the $(V_A - V_B)^2$ term. This severely limits the summing ability and dynamic range of the resistive and constant current loads. The physical constraints on the circuit do not permit the output voltage V_o to be opposite in sign to V_{DD} or to be complex.

The constraints imposed by the above are, for the resistive load.

$$\frac{2(V_A + V_B)}{\beta R_L} + \frac{1}{\beta^2 R_L^2} \geqslant (V_A - V_B)^2 \qquad (3.12)$$

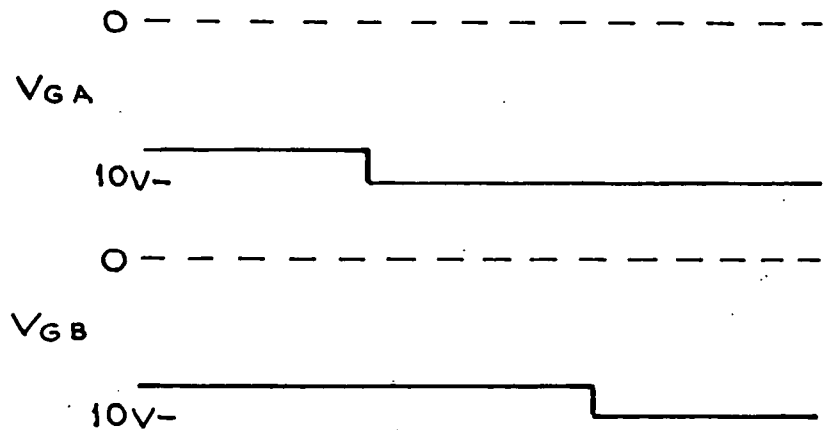
and for the constant current load

$$\frac{4I_o}{\beta} + 2V_A V_B \geqslant V_A^2 + V_B^2 \geqslant \frac{2I_o}{\beta} \qquad (3.13)$$

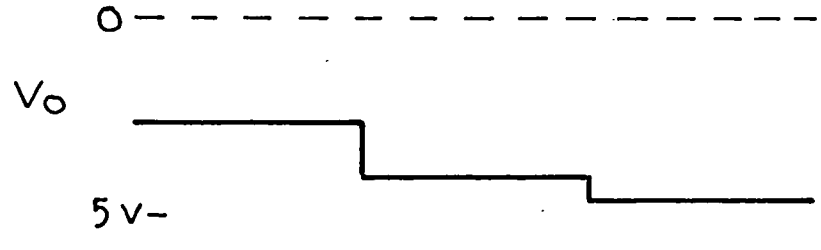
An illustration of the summing abilities of these various loads can be seen in Figure 3.14

The situation represented here is shown in (a). V_{DD} is 10V, V_T is 4V. The two elements A and B have been discharged by equal amounts to $V_{GA} = V_{GB} = 8V$, or an effective gate voltage $V_A = V_B = 4V$. The first recharge pulse restores the gate voltage of element A to V_{DD} ($V_A = 6V$, $V_B = 4V$). The second recharge pulse restores the gate voltage of element B to V_{DD} ($V_A = 6V$, $V_B = 6V$).

For the cases shown it can be seen that the constant current load (Figure 3.14(b)) and the resistive load (Figure 3.14(c)) both underestimate the second voltage change. As expected, the virtual earth load behaves as a perfect summing junction.

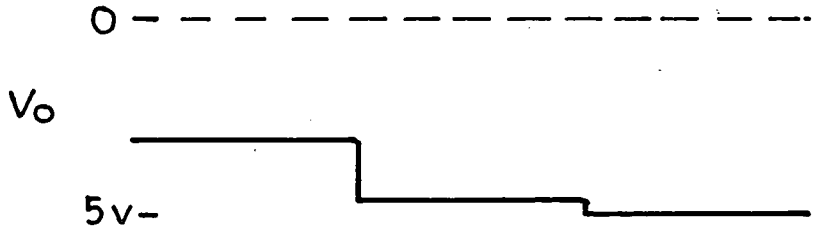


(a) GATE VOLTAGES



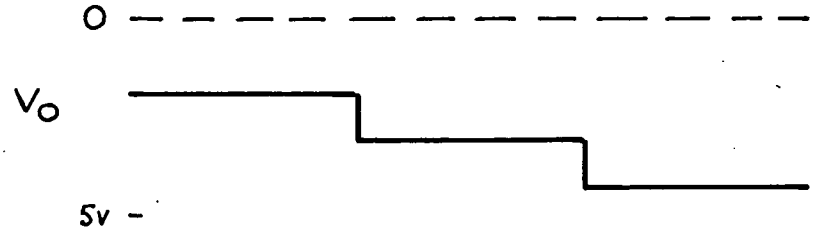
$I_O = 8\mu A$
$\beta = 4\mu A/V^2$
$V_T = 4V$

(b) OUTPUT FROM CONSTANT CURRENT LOAD



$R_L = 1M\Omega$

(c) OUTPUT FROM RESISTIVE LOAD



$R_F = 30k\Omega$

(d) OUTPUT FROM VIRTUAL EARTH LOAD

FIG 3.14 SUMMING ABILITY OF DIFFERENT LOADS, SHOWING THE OUTPUT WAVEFORMS EXPECTED AFTER IDENTICAL DISHARGE OF BOTH DIODES.

It appears then that the nature of the diode-pairing in the Plessey array will force the choice of a virtual earth output circuit in order to permit correct extraction of data from both diodes.

A further point arises from the diode pairing. If the array is used in the non-destructive read mode as described in Section 3.3.2., then the diode signals are available only as pairs because of the absence of charge pulses. Thus although NDRO is still feasible, the spatial resolution is now worse by a factor 2.

3.5. Manufacturing Process Parameters

The Plessey arrays, also known as the H509 array within Plessey, were manufactured on 2 inch slices, with each slice containing about 12 complete 4 x 256 arrays.

The process used in manufacture was Plessey's MNOS-1B process[17], some of the parameters of which are listed in Table 3.2.

The physical sizes of the devices used in the array are listed in Table 3.3., using the terminology of Figure 3.5 for identification of devices.

From these parameters, the diode capacitance C_D can be calculated as approximately 0.9 pF at 0V. Plessey quote a typical value of 1 → 2 pF, with a value of C_G, the gate capacitance of the source follower as typically one-tenth of this [18].

PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{TO}	1·2		2·5	V
Temp Coeff V_{TO}		- 0·2		%/°C
$ß_0$	4		8	$\mu A/V^2$
Temp Coeff $ß_0$		- 0·33		%/°C
GATE CAPACITANCE			3×10^{-4}	$pF/\mu m^2$
FIELD CAPACITANCE			4×10^{-5}	$pF/\mu m^2$
DIFFUSION PERIPHERY CAPACITANCE			5×10^{-4}	$pF/\mu m$
DIFFUSION AREA CAPACITANCE			1×10^{-4}	$pF/\mu m^2$

TABLE 3.2. MNOS 1B PROCESS PARAMETERS

DEVICE	LENGTH	WIDTH	UNITS
D	222	40	µm
T1	12	8	µm
T2	12	8	µm
T3	8	8	µm
T4	12	24	µm
T5	8	24	µm
T6	12	8	µm
T7	12	8	µm
T8	12	24	µm
T9	12	8	µm

TRANSISTOR DIMENSIONS REFER TO CHANNEL

TABLE 3.3. DRAWN DEVICE SIZES

3.5. Summary

The Plessey array demonstrates a number of novel features, including on-chip amplification at each element, double sampling and non-destructive readout. The two latter techniques are extremely promising when considering the suitability of the array for optical imaging.

The array was designed for the detection of photoelectron events, and was intended to be used in a simple counting mode to discriminate between "event"/"no-event". It was feared that the signal produced by a single photoelectron would be insufficient to permit gating directly by the shift register. For this reason, the amplifier was added to the basic element.

The amplifier is of mixed benefit when used for optical imaging. There is some increase in noise. The diode bias voltage is held constant throughout exposure, eliminating some of the non-linearities inherent in conventional arrays. The charge transfer rate through the amplifier transistor is slow at low signal levels and could possibly lead to lag problems.

The pairing of diodes also has drawbacks when aiming for good linearity. A virtual earth amplifier at the output is essential to achieve correct summing. In Chapter Two, it was seen that the virtual earth output circuit contributes to non-linearity and an increase in fixed pattern noise. None of these problems of course would affect the operation of the array for its designed purpose of photoelectron counting.

It is interesting to note that single photoelectron counting has since been demonstrated with unamplified recharge sampling arrays [10, 11].

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CHAPTER FOUR

The Control and Data Acquisition System

Prior to undertaking any experimental work on the Plessey arrays, it was necessary to develop some control and readout system for operating the devices. Some of the electronics required was already in existence at the time the Durham group became involved in the project. This had been developed for the "intensified" array work at the R.G.O., and much of this was used in early experiments at Durham. It was obvious, however, that a new control and acquisition system would have to be developed in order to apply the array to optical imaging work. Design and development was started on this system at the commencement of the project, simultaneously with experimental work on the array itself. Consequently much of the early laboratory testing of the devices was done with somewhat crude control equipment and almost exclusively with oscilloscope observation of the array outputs. The computerised control system described here was completed only a few days prior to operation of the array at the 30 inch telescope of the R.G.O. during August 1978. For completeness, brief mention will be made at the end of this Chapter of the system configurations used prior to the implementation of the full control and acquisition package.

4.1. System Requirements and Specifications

Diode arrays, and other solid state imaging devices are frequently operated purely under hardware control, with analog signal processing and an analog final output. Such systems are often entirely adequate in applications such as thickness gauging and television type imaging. In our applications, the requirements of the experiement dictate the use of a rather more complex system. Also, the requirements are very different according to whether the array is to be used in the intensified electron-counting mode, or in the direct photon-integration mode.

4.1.1. Operation in the Electron Counting Mode

In the electron counting mode envisaged at the R.G.O., each photo electron would liberate about 6000 electron-hole pairs, and an array element would be fully discharged by about 800 such photo-electrons. In order to achieve a larger dynamic range, the "integration" was to be performed external to the array, in a manner similar to the Digicon described in Chapter One. The system as originally devised at the R.G.O.[1] is shown schematically in Figure 4.1.

The array is scanned repetitively with a frame time (the time taken for one complete scan) of slightly over 1ms. The array output is processed by an analog double sampling processor, which extracts from the waveform the difference between signal levels before and after a recharge pulse. Thus the processed output waveform now consists of a train of 256 pulses whose amplitude is representative of the signal on each array element. This waveform is now level-discriminated, with the threshold set such that leakage currents and other noise signals produce a logical "zero" output, whereas for the larger signals due to photoelectrons, the output is a logical "one". The signals are then stored and integrated in a recirculating memory. This consists of a 16 bit by 256 word long shift register memory, which is clocked synchronously with the array. If a logical "one" is present in the array output, then the word in the corresponding register address is incremented by one. The data in this memory is periodically transferred to the memory of the data processing computer.

This system handles one video output waveform from the array. Four such systems are used if all the lines on the array are to be utilised.

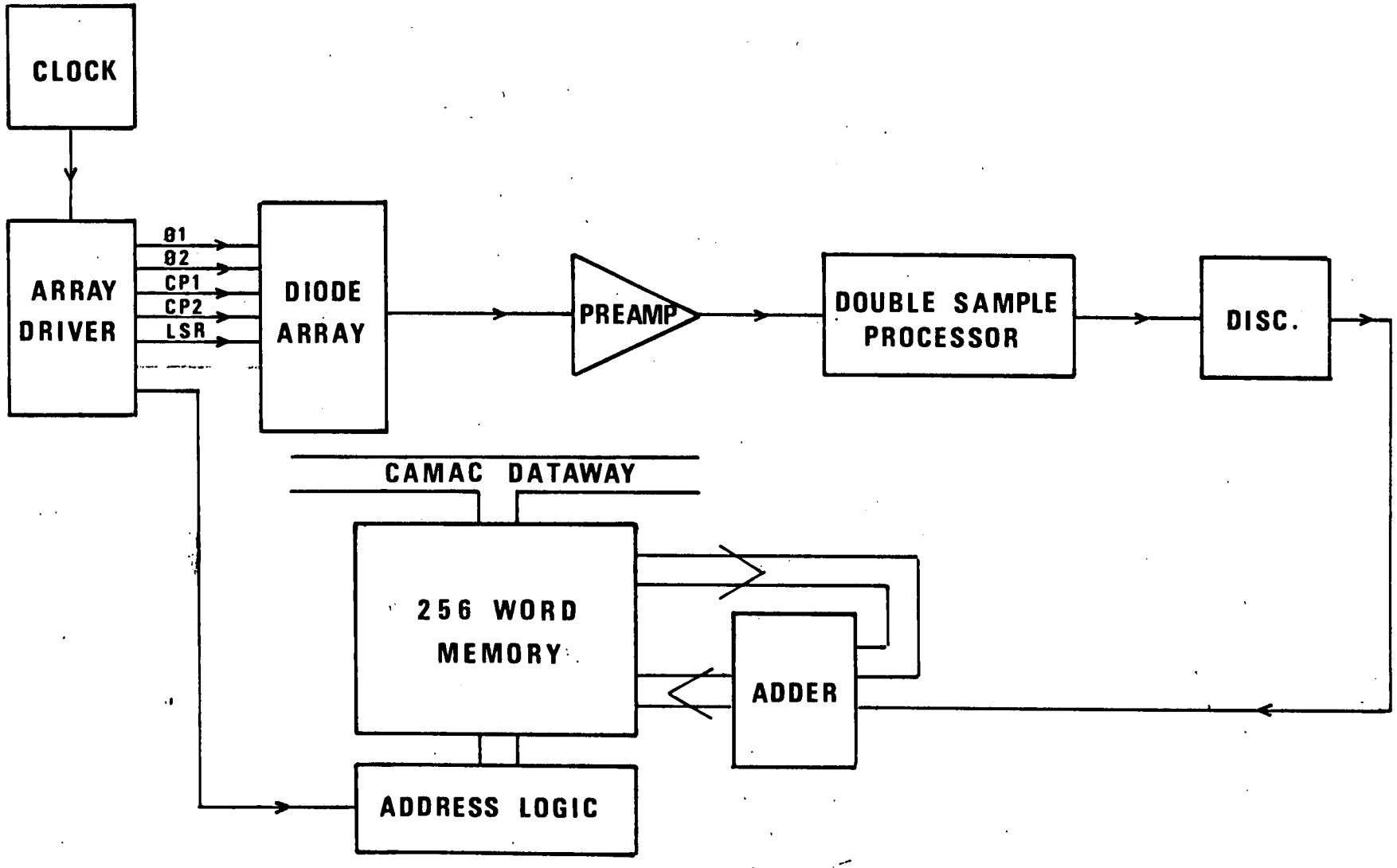


FIG.4.1. ELECTRON COUNTING SYSTEM - READOUT SCHEME

4.1.2. Operation in the Photon Integration Mode

The operating sequence for the array is somewhat more complex when running the array in the photon integration mode. Primarily, it must be possible to achieve long, and variable integration times.

It is possible to adjust the integration time over a limited range simply by reducing the clocking rate and thereby increasing the frame time. This is impractical for very long integration times where the operation of the dynamic on-chip shift register would be impaired by leakage. A neater solution is to run the shift register at the same rate for all integration periods, but to control the recharge function. Thus the sequence of operation becomes firstly a frame during which the recharge function is enabled, followed by a number of frames of integration, when the recharge function is disabled, and then a final frame during which recharge is enabled and the output waveform is sampled.

4.1.3. The Design of the Control System

A control system of the type required can be implemented in one of two ways. All control can be achieved by suitably designed hardware, or the control function can be undertaken by computer software. Since some form of computer is necessary to store, process and display the data derived from the array, it was decided to adopt the second course, and in the system to be described the computer has full control of the integration cycle of the array, functioning under interrupt control.

The block diagram of the control and acquisition system developed at Durham is shown in Figure 4.2.

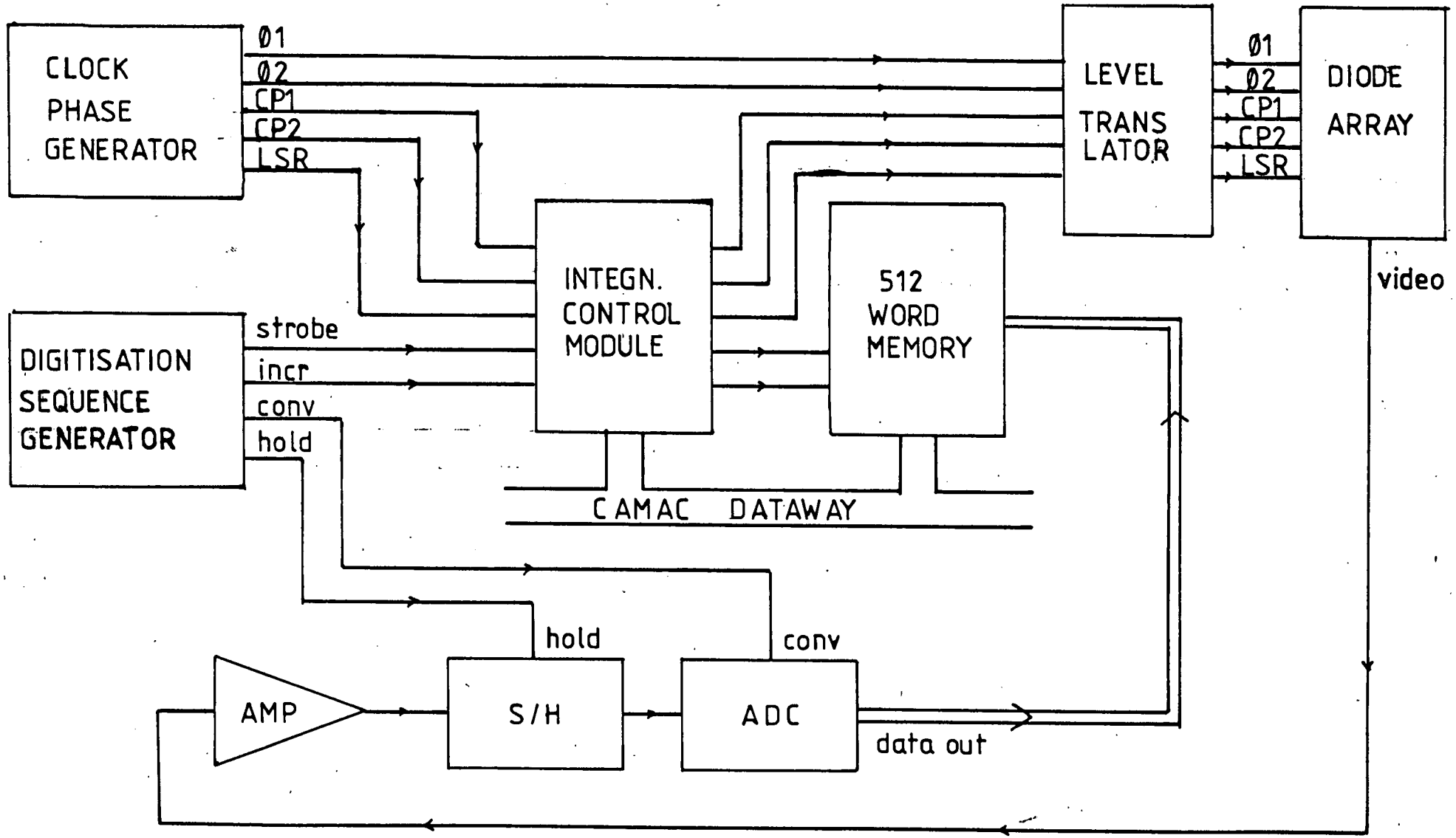


FIG.4.2. CONTROL AND DATA ACQUISITION SYSTEM

The operation of the system will be described in detail module-by-module later, but a few points of interest will be mentioned here.

The five signals required by the array itself are generated by the CLOCK PHASE GENERATOR (CPG), these being the two clock phases $\phi 1$ and $\phi 2$, the charge pulses CP1 and CP2 and the load shift register pulse (LSR). The signals required by the data acquisition circuitry are generated by the DIGITISATION SEQUENCE GENERATOR (DSG) and control the operation of the Sample and Hold, Analog to Digital Converter and Buffer Memory.

The "heart" of the system is the INTEGRATION CONTROL MODULE (ICM). This is interfaced to the computer via CAMAC[2], a modular interface system. The ICM gates the charge pulses and LSR pulse to the array, and also the control signals to the buffer memory. The ICM generates an interrupt to the computer at the beginning of each frame. An interrupt routine in the operating program then commands the ICM to enable or disable the appropriate signals to generate the desired type of frame. Thus any type of integration cycle can be "assembled" by the computer program, which gives the user maximum control over the operation of the system.

4.1.4. Interfacing and Module Standards

At the outset of the project, it was decided that all the instrumentation would be constructed around the CAMAC standard. This is an international standard for computer control and acquisition systems, originally developed to serve the needs of the High Energy Physics community. Several advantages are offered by CAMAC, including independence of the type and model of computer used, and the availability and interchangeability of a large number of standard modules. Two further factors influencing this decision were :-

1. Experience within the Nuclear Instrumentation Group of CAMAC from previous work in High Energy Physics Instrumentation.

and 2. The growth of popularity of CAMAC within the astronomical community.

Consequently, CAMAC has been adopted wherever transfer of data to or from the computer has been necessary. This includes all peripheral interfacing which would normally be done with computer-specific interface boards. In order to economise on crate space and power requirements, all modules not requiring connection to the CAMAC dataway have been implemented in NIM format. All logic levels throughout the system are TTL, and circuitry is constructed wherever possible using 74LS family IC's. The drive signals required by the array are converted from TTL to the required levels by appropriate level translators.

4.2. Descriptions of the Modules of the Control System

In the following section, the modules designed and built for this project are described briefly in terms of their functions. Where the design is of particular interest, further details of the circuitry are given as appendices. The modules can be classed as belonging to the control chain or to the signal processing chain. The control chain will be described first.

4.2.1. Clock Phase Generator

The function of the Clock Phase Generator (CPG) is to provide, at TTL level, the two clock phases Ø1 and Ø2 and the charge pulses CP1 and CP2. In addition it generates a Load Shift Register(LSR) command which overlaps the last Ø2 phase of the previous frame, thus initiating another scan. The timing relationship of these pulses is shown in Figure 4.3. which illustrates the end of one frame and the start of the next. There is an overall similarity between this module and that designed by the RGO /Plessey to be used in the electron counting system. This used fully complementary clock phases Ø1 and Ø2, but these were found to cause some instability on the output video waveform which disappeared when using clock phases with a shorter duty cycle. The ability to control the size and shape of the scan pulses by tailoring the clock waveforms was described in Chapter 3.

The length of the charge pulses is determined by a 74121 monostable, and this is adjustable from the front panel from less than 1 μs up to about 200 μs, there is a front panel switch to disable the recharge pulses.

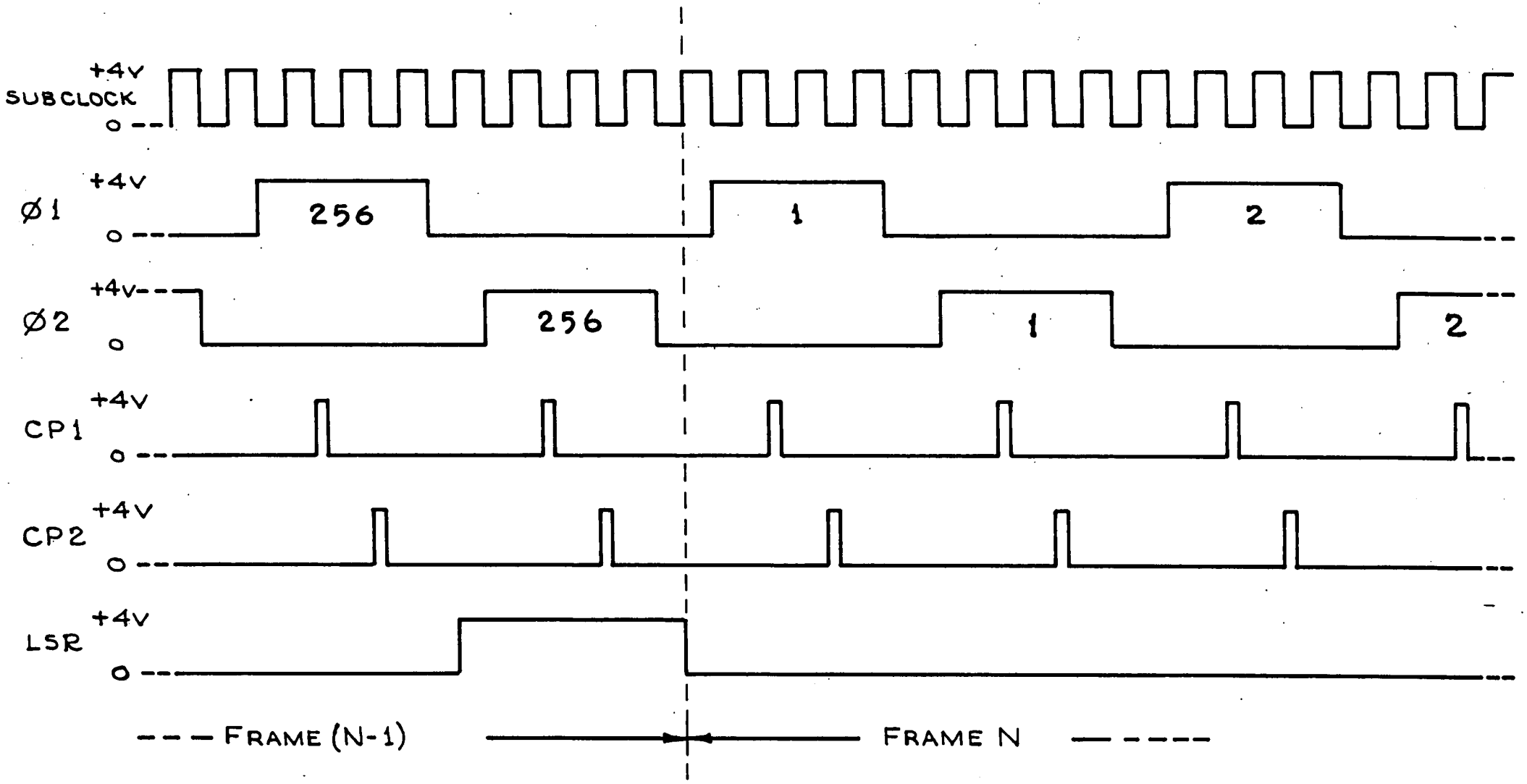


FIG 4.3 PART OF TIMING CYCLE OF THE CLOCK PHASE GENERATOR.

The Clock Phase Generator requires an input clock at 8 times the desired frequency of Ø1 and Ø2. This is provided from the Digitisation Sequence Generator.

The Clock Phase Generator, with an appropriate input clock and suitable level translators, can be used alone to provide the signals required to operate the array in a repetitive scan fashion with an integration time of one frame time.

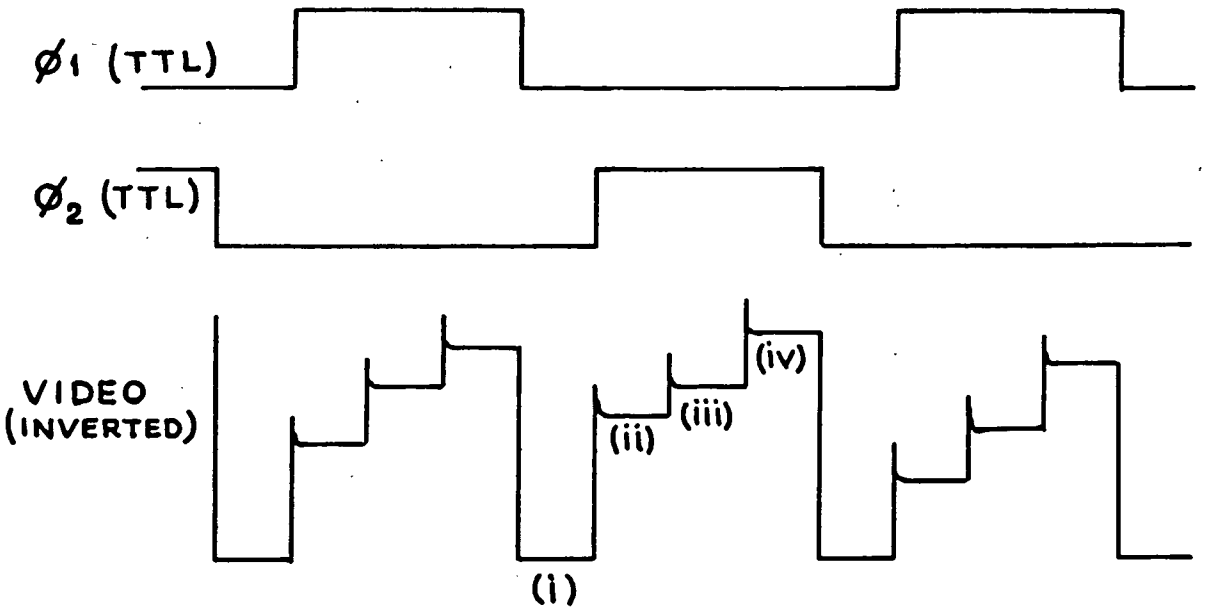
This module is constructed as a single width NIM module.

4.2.2. Digitisation Sequence Generator

In designing the Digitisation Sequence Generator (DSG) it was intended to produce a digitisation system that could handle a variety of video waveforms and control different types of Sample Hold and Analog to Digital Convertors. The digitising system is therefore applicable to other types of array which may be used in the future.

A typical video waveform from the Plessey array is shown in Figure 4.4. There are four information levels in this waveform for each diode pair. These are :-

i) the baseline level
ii) the sum of the two diode signals
iii) the signal on the second diode only
iv) the reset level



(i) BASELINE

(ii) SUM OF DIODE SIGNALS

(iii) SIGNAL ON SECOND DIODE ONLY

(iv) RESET LEVEL

FIG 4.4. DIGITISATION POINTS ON VIDEO WAVEFORM

Of these, i), the baseline level, contains no information relevant to that diode pair, but by digitising this we can monitor drift and noise in the signal chain.

Sampling and digitisation is therefore required at 8 points per Ø1 or Ø2 cycle, or once per cycle of the clock input to the Clock Phase Generator. Each digitisation will require a sequence of four control signals. First of these is a Hold command to the Sample and Hold circuit, followed by a Convert command to the Analog to Digital Convertor to start the conversion. After the end of the conversion, when the data at the ADC output has settled, the data must be transferred into a Buffer Memory. This is achieved by the Strobe command. The memory address counter is then incremented by the Increment command so that the next digitised level will be stored in the next highest memory address. A typical sequence is shown in Figure 4.5., along with some of the timing constraints.

The four control pulses (Hold, Convert, Strobe and Increment) can be programmed by front panel switches to start and finish at any time within a 16 bit cycle. That is, the rising and falling edges of each control pulse can be set to coincide with any falling edge of the Master Clock shown in Figure 4.5., a clock which has 16 cycles during each digitisation cycle. The circuit of the Digitisation Sequence Generator is described in Appendix B.

The Sub-Clock shown in Figure 4.5. is output to the Clock Phase Generator Module to derive the rest of the system timing.

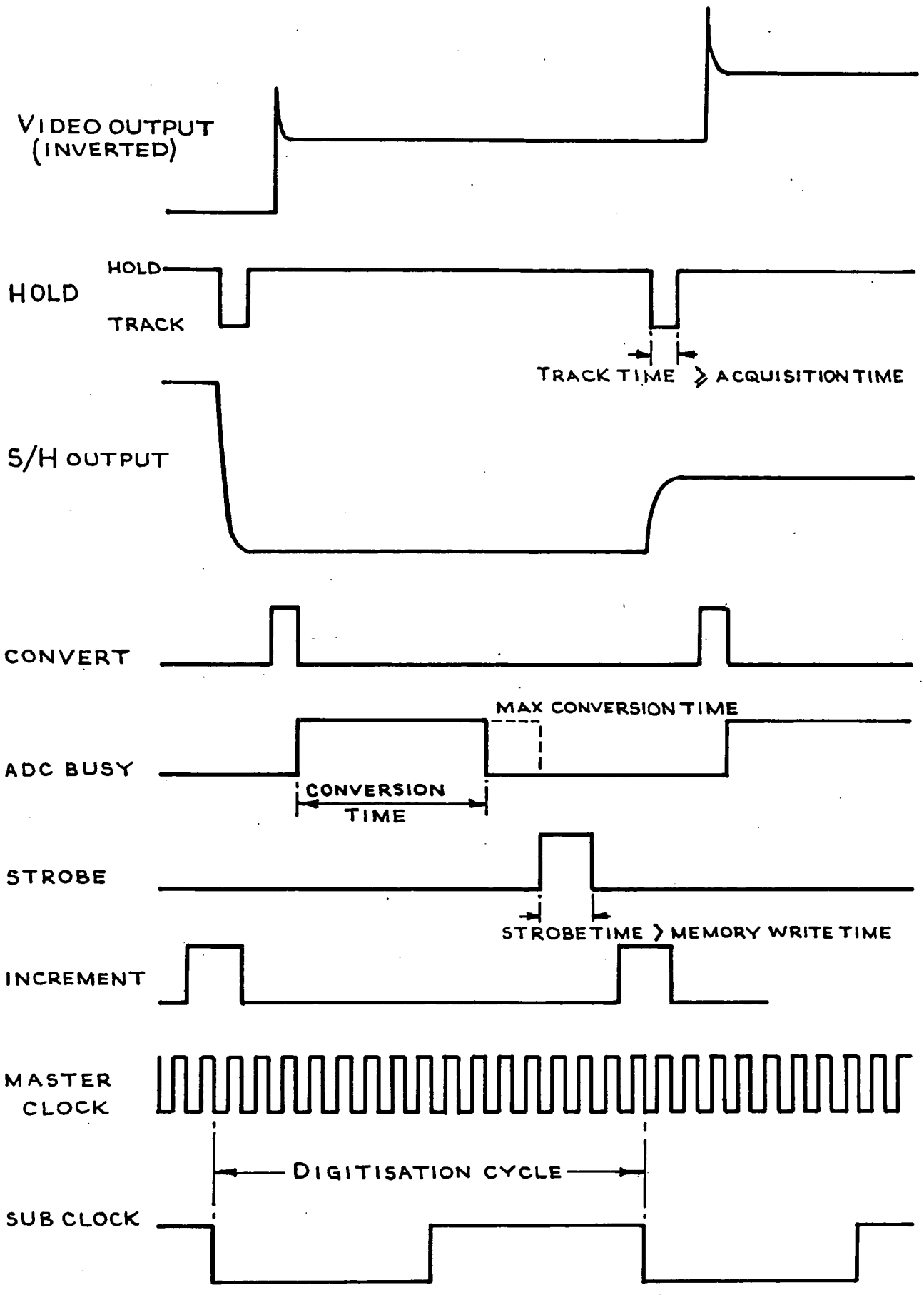


FIG 4.5 DIGITISATION SEQUENCE

The Master Clock input to the Digitisation Sequence Generator is supplied externally from a Hewlett-Packard HP 8004A pulse generator, although it is planned to replace this with a crystal controlled clock. The timing is such that the scan rate of the array in elements per second is f/32 where f is the Master Clock frequency.

The Digitisation Sequence Generator is built as a 4 wide NIM module, this width being dictated by the front panel switches. The circuitry is on two boards.

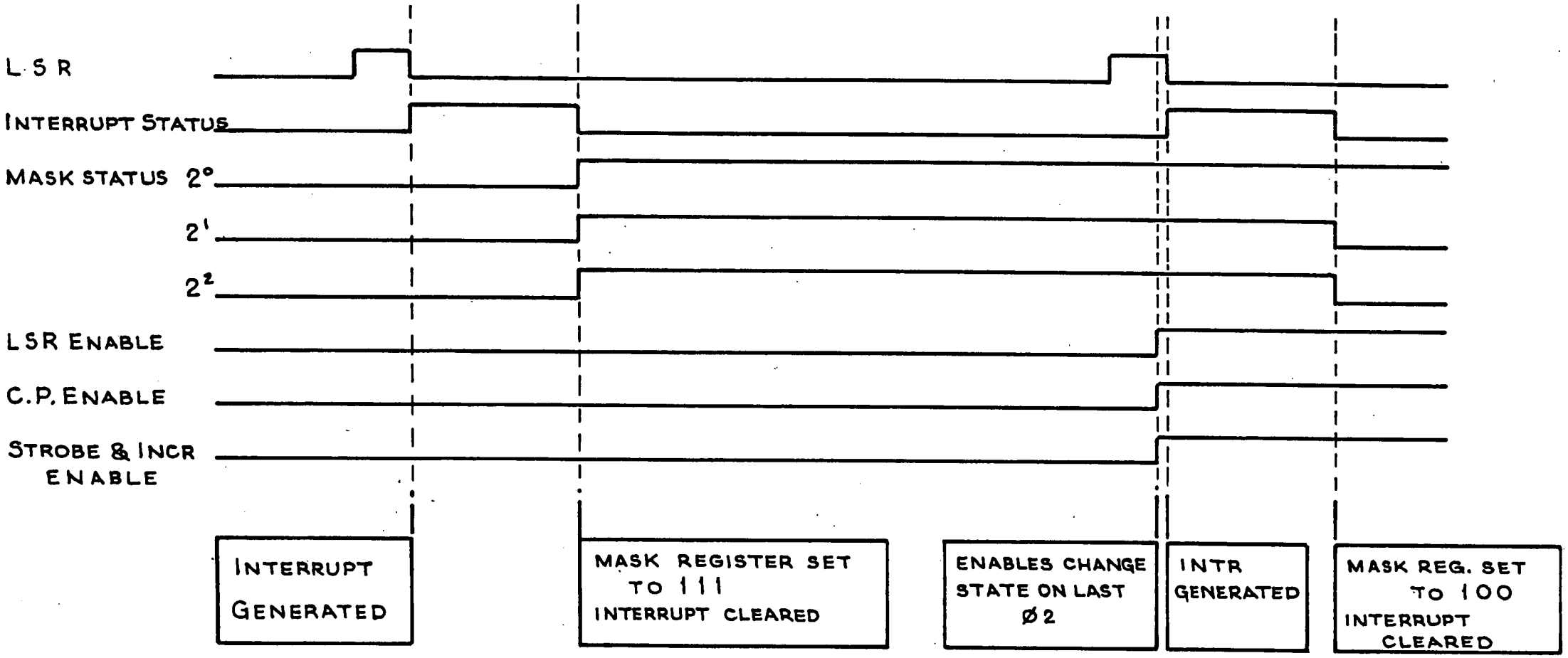
4.2.3. Integration Control Module

The Integration Control Module, (ICM), as explained in Section 4.1.3. operates under control from the computer via the CAMAC dataway. The principle of operation is as follows, referring to Figure 4.6.

On the falling edge of a LSR command, indicating the start of a new frame, the module sets a LAM (Look-at-Me) on the CAMAC dataway, which issues an interrupt to the computer. This interrupt requests a control word which is then transmitted to the module via the dataway and is loaded into a mask register within the I.C.M., clearing the interrupt. Bit 2^0 of this register masks (that is, disables) the LSR commands. Bit 2^1 masks the CP1 and CP2 pulses, and Bit 2^2 masks the Strobe and Increment commands.

The mask is not enabled until the last Ø2 clock phase of that frame. Thus the mask required during a frame N is set up during the preceeding frame, N-1. This was done so that the interrupt handling routine has one whole frame time in which to decide upon and load the appropriate status mask.

The most useful mask words are listed in Table 4.1., along with the actions associated with them. Integration can be achieved with a mask of 0 or 1 depending on whether the load shift register command is required. A zero



MASK BITS	
BIT SET	FUNCTIONS ENABLED
2^0	L S R
2^1	C P1 & C P2
2^2	INCR & STROBE

FIG 4.6 TYPICAL TIMING CYCLE OF INTEGRATION CONTROL MODULE.

will disable the LSR command, and so the array elements will not be scanned and there will be no video waveform. A mask word of 1 will enable the LSR command, and the array will be scanned but not recharged. A video output waveform will be present, and will be digitised by the ADC, but because the Strobe and Increment commands are disabled, nothing will be loaded into the Buffer Memory. A mask word of 3 causes a recharge operation, but again with no data being loaded into memory. A 5 causes a non-destructive read, by enabling the LSR command in order to scan the array, loading the digitised video into the Buffer Memory, but supressing the recharge pulses CP1 and CP2. A mask word of 7 enables all three groups of commands and causes a conventional destructive readout.

Thus an integration period of two frames could be achieved by a recharge frame (3), an integration frame (1) and a readout frame (7). Such a scheme, and the timing cycle associated with it is illustrated in Figure 4.7. Note that the integration period is always one frame longer than the combined number of integration and NDRO frames because of the 1 frame integration that is achieved anyway by continuous readout.

So far, the operation of the Integration Control Module has been described only in terms of control by the computer program. During a long integration on a light source of unknown intensity, there must be provision for the user to monitor the progress of the integration by requesting a Non-Destructive Read Out. When the desired exposure has been made, the user must also be able to terminate the integration. To permit this user control, two front panel buttons are provided.

MASK WORD (OCTAL)	COMMAND STATUS			ACTION
	INCR.&STROBE	CP1 & CP2	L S R	
0	DIS	DIS	DIS	INTEGRATE
1	DIS	DIS	ENB	INTEGRATE
3	DIS	ENB	ENB	RECHARGE
5	ENB	DIS	ENB	NDRO
7	ENB	ENB	ENB	READOUT

TABLE 4.1 USEFUL MASK WORDS

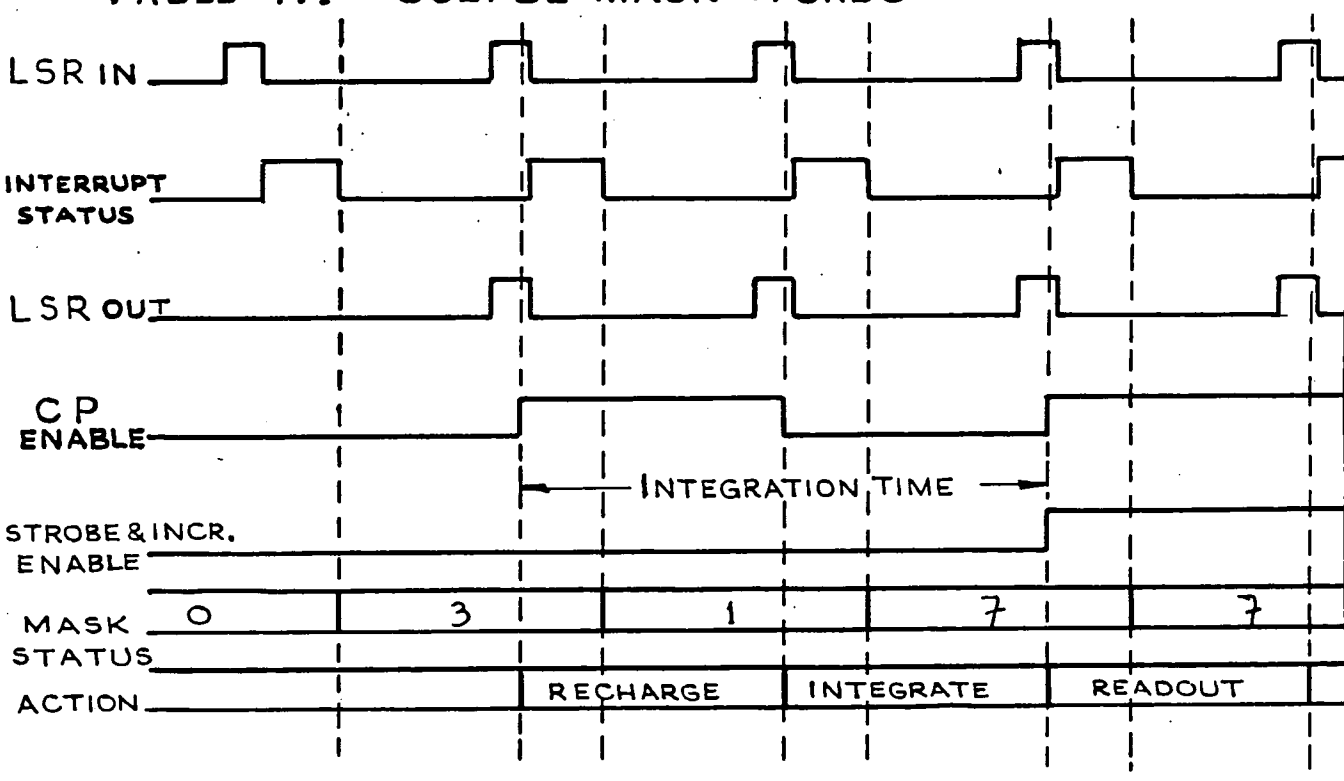


FIG 4.7 POSSIBLE SCHEME FOR A TWO FRAME INTEGRATION

These set up interrupt status flags, but do not generate an interrupt themselves. This is in order to avoid any possibility of overlap of interrupts which could lead to one being "lost". On receiving the interrupt generated by the falling edge of the next LSR pulse, the computer tests these status flags. If set, the program leaves the selected sequence and takes the appropriate action. Obviously these two front panel buttons can be used for any functions desired, their actual effect being determined by the interrupt handling routine.

The Integration Control Module is constructed as a triple width CAMAC unit. Further details of the circuitry are given in Appendix C.

4.2.4. Level Translator Module

The final component in the control signal chain is the Level Translator Module, which converts the Ø1, Ø2, CP1, CP2 and LSR TTL signals into the levels required by the array. The timing of the signals is not changed. The output levels are typically logical "0" = 0V, logical "1" = -14V, but are adjustable. The chief requirements are very stable output voltages, fast rise and fall times and clean pulse shapes. The circuitry of this module is to be described in another work by A.W. Campbell[3].

The Level Translator is built as a single width NIM module. The power rails are supplied from a separate 24V power supply in order to avoid any possibility of noise on the output waveforms due to other modules in the same NIM crate.

4.2.5. The Video Preamplifier

The "signal path" of the system consists of a Video Preamplifier, a Sample and Hold Module, an Analog to Digital Convertor Module, and the Buffer Memory.

The Video Preamplifier is based around a Burr Brown 3550, a high slew rate operational amplifier, used in an inverting, virtual earth configuration. The use of a virtual earth load is dictated by the summing limitations discussed in Chapter 3.

The feedback resistor used in the preamp is 68kΩ. The output swing per carrier generated in the photodiode can now be estimated. From Chapter 2, we have the small signal gain referred to the source follower gate voltage of :-

$$\frac{dV_o}{dV_G} = - \frac{R_F}{R_{on}} \left[1 - \frac{1}{\sqrt{1 + m}} \right]$$

where $m = 2 \beta (V_G - V_T) R_{on}$

Assuming the following parameters

$\beta = 6 \mu A/V^2$
$V_T = 2V$
$R_{on} = 4k\Omega$
$V_G = 5V$

Then this becomes

$$\frac{dV_o}{dV_G} = - 1.11$$

The voltage change at the gate of the source follower for a single carrier discharging the photodiode depends on the gate capacitance.

Assuming a value of C_G = 0.1pF, then

$$dV_G = \frac{dQ}{C_G}$$

and $\frac{dV_o}{dQ}$ is 1.7 μV/carrier

The Video Preamplifier is mounted in a small diecast box and is normally mounted close to the array. The design of the preamplifier is discussed by A.W. Campbell [3].

4.2.6. Sample and Hold Module

Two versions of the digitising system have been constructed. The first was a low cost 8 bit resolution system used for initial work and to prove the system. For the work at the 30 inch telescope at the R.G.O. a 12 bit system was constructed. Consequently there are two types of Sample and Hold Module. The first 8 bit system uses a Hybrid Systems S/H 703 monolithic sample and hold circuit, whereas the 12 bit system employs the more accurate S/H 730 Hybrid circuit. Otherwise the two modules are similar. The S/H circuit is configured as inverting with a unity gain. This is followed by a non-inverting operational amplifier stage with adjustable offset and gain, which are used to match the video signal range to the ADC input requirements. Both modules are packaged as single width NIM units, and are described in greater detail by A.W. Campbell [3].

4.2.7. Analog to Digital Convertor Module

The 8 bit digitiser module is constructed around a Hybrid Systems ADC 540-8, with a conversion time of 5 μs, The 12 bit version was originally designed around another Hybrid Systems unit, the ADC-593-12 with a 4 μs conversion time. Due to delivery problems however, the slower Burr Brown ADC 80-12 had to be substituted,with a conversion time of 25 μs.

The effect of this on the usable frame time is as follows. Four digitisations are necessary per diode pair, that is 512 digitisations per frame. This implies a minimum frame time of 12.8 ms using a 25 μs digitiser, without allowing for the extra time overheads of S/H settling time and memory write time, which are short by comparison.

Both modules have parallel output with straight binary coding, and have an input range of 0 to + 10V. The 12 bit version also has a jumper selectable option for bipolar input with either 2's complement or offset binary output codes.

There are front panel inputs for Convert, Strobe and Increment commands. These latter two are not used functionally within the module but are passed to the output connector (25 way D-type) to the memory module.

Two LED's are provided on the front panel for monitoring. A green display is driven from the Busy signal of the convertor, and a red display indicates the status of the Strobe command.

The circuit of the 12 bit ADC Module is shown in Figure 4.8. The monostable on the Convert command is necessary because the ADC 80 AG-12 requires a convert pulse of less than 2 μs.

Both modules are packaged as single width NIM units.

4.2.8. The Buffer Memory Module

The Memory is the last module in the signal chain. Whilst it would have been possible to load data from the ADC directly into the computer for storage in main memory, under interrupt control, it was decided that external buffer storage was preferable. This choice was made principally to simplify interrupt handling.

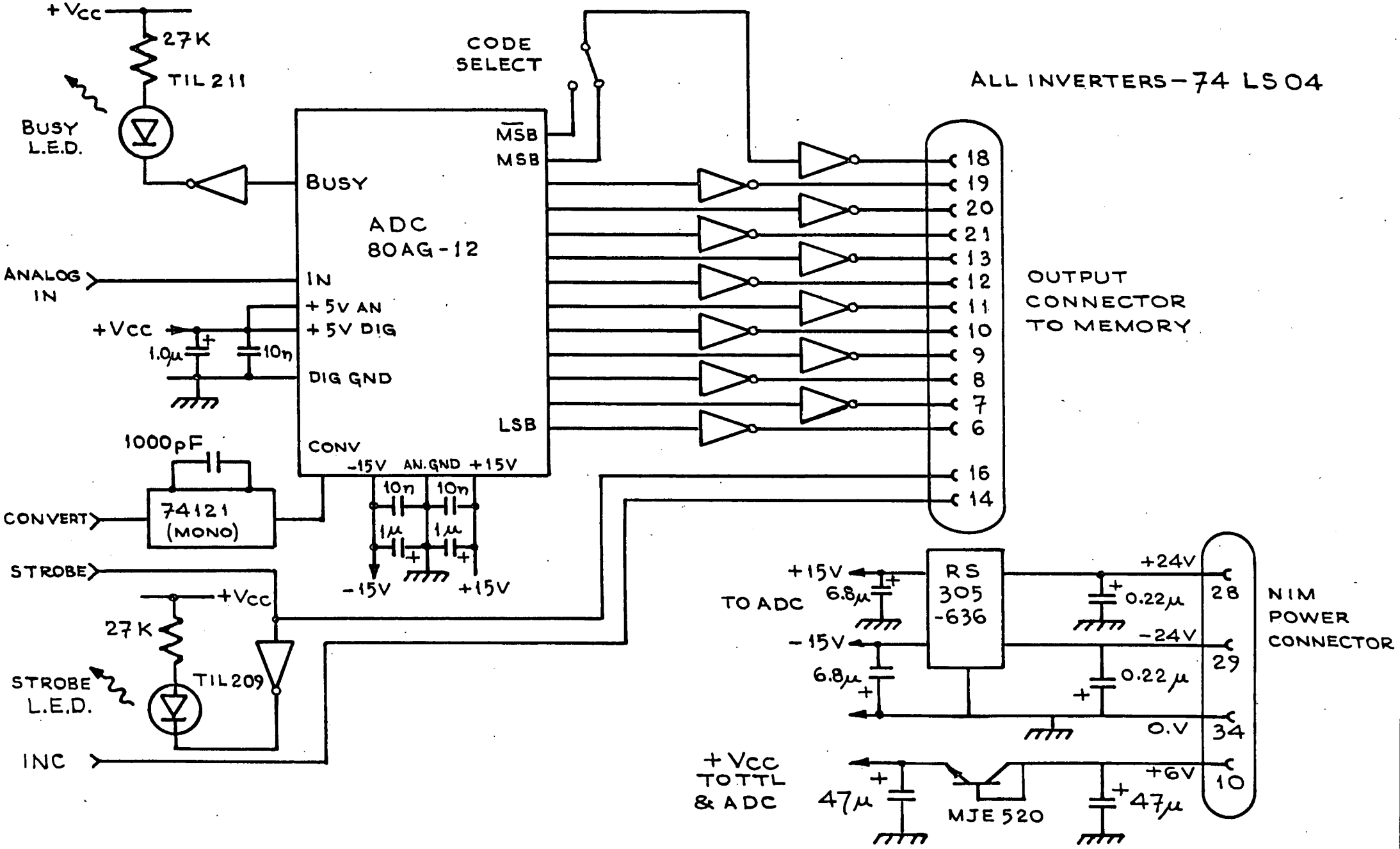


FIG 4.8 CIRCUIT DIAGRAM OF 12 BIT DIGITISER

Two Memories have been constructed, organised as 512 words of either 12 or 8 bit word length, based around 256 x 4 static RAM chips. The 8 bit memory is now obselete as clearly the 12 bit memory can be used in its place by ignoring the most significant 4 bits. There are some small differences between the 8 bit and 12 bit versions, chiefly in the CAMAC function decoding. The design of the memory will be described in detail by A.W. Campbell[3], but its operation from the users point of view will be described here.

The DATA IN/DATA OUT modes are selected by a CAMAC F25 command (EXECUTE). The memory is addressed by a 9 bit counter, and the counter is set to zero by either the DATA IN or DATA OUT commands or by a CAMAC initialise (Z) command. In the DATA IN mode, the address counter is incremented by the increment signal from the ADC module, whereas in the DATA OUT mode it is incremented during a CAMAC READ cycle (FO command).

In order to transfer data in or out of the memory chips, their chip enable (CE) lines must be set high. This can be achieved either by the Strobe signal from the ADC, or by a CAMAC F26 (ENABLE) command. The chips are disabled by Strobe, by a CAMAC F24 (DISABLE) command, or by a CAMAC INITIALISE (Z) command. These functions are summarised in Table 4.2.

ACTION	CAMAC COMMANDS	FRONT PANEL COMMANDS
CHIP ENABLE	F26.A0.S2	STROBE
CHIP DISABLE	F24.A0.S2 + Z.S2	$\overline{\text{STROBE}}$
SET DATA IN	F25.A0.S1	
SET DATA OUT	F25.A1.S1	
ZERO ADDRESS COUNTER	F25.(A_0+A_1).S1+Z.S2	
INCREMENT ADDRESS COUNTER	F0. A0. S2	INCR
READ DATA	F0. A0	

TABLE 4.2 12 BIT BUFFER MEMORY FUNCTIONS AND COMMANDS

4.3. Peripherals and Interfacing

At the outset of the project it was decided that all peripherals should be interfaced via the CAMAC system, in order that the experimental package should be as independent as possible of the host computer in use. This would facilitate its easy integration with existing computer systems at other laboratories and observatories.

The requirements of the experiment call for a communication terminal for program development and control, a permanent mass storage system for programs and data, and some form of graphical display for the observation of spectra, preferably with some hard copy facility.

Initially an ASR 33 teletype was used as the sole peripheral, and was convenient for three reasons :-

a) It was available within the N.I. Group already.

b) It combines a keyboard, hard copy printer, and paper tape reader, punch and copier all within the same unit,

and c) Some type of console device is required by the computer (this will be explained later).

The ASR 33 is severely limited in speed, and was eventually augmented by a Visual Display Unit, a fast Paper Tape Reader, fast Paper Tape Punch and a Storage Graphics Display.

4.3.1. Visual Display Unit

The VDU chosen was the Lynwood DAD-1, largely for its reputation of robustness and reliability at a reasonable price. The unit is directly teletype compatible, but also has some extra facilities such as cursor addressing, blink mode, protected field and printer control. It is interfaced to CAMAC via a Nuclear Enterprises 7061 TTY interface. The 7061 is a somewhat ageing unit now considered obsolete by Nuclear Enterprises. Their replacement, the NE 9047 has been obtained, but at the time of writing has not been satisfactorily incorporated into the system, requiring some software changes.

4.3.2. Paper Tape Reader

The paper tape reader used is the Lynwood ATR 2, a very fast unit with optical character reading and optical sprocket hole detection (rather than the slower but more common toothed sprocket wheel driven by a stepping motor). The CAMAC interface is a GEC TR0801 unit, developed from a DNPL (Daresbury Laboratory) design.

Some problems have been encountered with persistent misreading of certain characters, but these have been traced to crosstalk in the connecting cable and have been eliminated by careful screening.

4.3.3. Paper Tape Punch

The paper tape punch is a Facit 4070, capable of punching at 75 characters per second, and is interfaced via a GEC TP0801 module. As previous experience had led us to expect, this has proved extremely reliable and robust. Three modes of operation are available from the interface. The first produces a length of leader (sprocket hole only) tape, whilst the other two enable the punching of an 8 bit word as a single character or a 16 bit word as two successive characters. These facilities considerably simplify programming.

4.3.4. Storage Graphics Display

For economy, a small storage display was chosen. This is the Tektronix 603 Storage Monitor, with a 4 inch by 5 inch screen, and a resolution of 80 x 100 line pairs. Two CAMAC interface modules are used with this display. The first is the Nuclear Enterprises 9028 Storage Display Mode Generator. As its name suggests, this module supplies, under CAMAC control, the control signals necessary to select the mode of operation of the display. The modes available are store, non-store and erase.

The X and Y deflection signals, and Z modulation (intensity) for the display are generated by a Nuclear Enterprises 7011 Display Driver. This provides facilities for plotting lines in X or Y, and for plotting of points either by X,Y addressing or by automatic increment of X (i.e. spectrum plotting). 3 levels of spot brightness can be programmed.

4.3.5. CAMAC Test and Display Modules

Three CAMAC modules are used for development work and system monitoring.

The Nuclear Enterprises NE 9554 Dataway Display can be used to monitor the status of all the CAMAC lines via LED's on the front panel, or can be used as a binary display register and written to in the same manner as a conventional CAMAC module. The first function is primarily useful in hardware testing, whereas the second finds use in some programs for displaying the status of variables or flags.

The DNPL EC326 System Checkout module enables all the address, data and control lines in a CAMAC crate between its station and the Crate Controller to be tested under program control. This is useful in locating bus problems. Front panel indication of the status of all power lines is provided.

The GEC TC 2403 Dynamic Test Controller, when used, occupies the control station of the crate. It provides the facility for generating two CAMAC commands which can be stepped through manually or free run. Its main use is during the design and testing of modules.

4.4. The Computer System

The computer system itself has three components, the computer hardware, the crate controller linking the computer to the CAMAC system, and the programming language/operating system.

Several approaches were considered towards the problem of obtaining a computer.

Conventional minicomputers of the PDP 11 , Nova, or HP 21 series were, at the time, the traditional machines used for experiments of this size. The cost of purchasing such a machine was prohibitive however.

An IBM 1130 was in use in the Durham Physics department, but this was shared already by two groups, and fortunately this could be rejected on the grounds of there being no commercially available CAMAC interface for this machine.

The purchase of a second hand machine was considered, but at the time PDP-8's were the only readily available second hand machines, and these were already somewhat obselete.

Microprocessors were beginning to become available, but this market was very new, with little in the way of commercially available software or hardware support. The packaged microcomputers now available such as PET, Apple and TRS 80 were yet to be released.

Recently announced was a new minicomputer from Digital Equipment Corporation based on the PDP 11 range, but using a microprocessor as the CPU. This was available in board form as the LSI 11 microcomputer or packaged as a complete small computer as the PDP 11/03. A commercial CAMAC controller was available for this machine, and others were known to be under development. Also, a CAMAC oriented programming language was avilable for PDP-11 machines which would soon be available for implementation on the LSI 11. The following sections describe this computer, the crate controller and the programming language.

4.4.1. The PDP 11/03 Computer

The configuration chosen is the 11/03 KB, consisting of a KD 11-H CPU board, and a MSV - 11CD 16k word dynamic RAM memory board. Two interface boards are fitted. First is the DLV 11 serial interface used to interface to the ASR 33 teletype, and secondly the interface card to the Crate Controller. This configuration is shown in Figure 4.9 and leaves a full width slot available for the addition of extra memory to expand up to 32k words, for the addition of extra peripherals such as floppy disks, or for a bus extension box for a larger system.

One feature of the LSI 11 system is that there is no provision for the traditional programmer's panel, used for manual entry and verification of machine code programs. These functions are carried out via the "console device", in our case the ASR 33 teletype, through a command code called ODT. The teletype is also used for entering short loader programs through its tape reader.

4.4.2. The CAMAC Crate Controller

The Crate Controller is of somewhat unusual design, and some discussion of the various Crate Controller concepts in CAMAC is worthwhile prior to a description of the unit.

The original concept of the Crate Controller was the Crate Controller A-1. This is a standard controller and is driven from a branch highway, the structure of which is defined in EUR 4600[4]. A branch driver, external to the crate, is used to connect the branch highway to the computer bus. A multiple crate configuration based on such a system is shown in Figure 4.10. This system is ideal for large multicrate and multibranch systems, but as CAMAC became considered for small experimental systems, the cost of a branch driver became unacceptable when only a single crate was to be used.

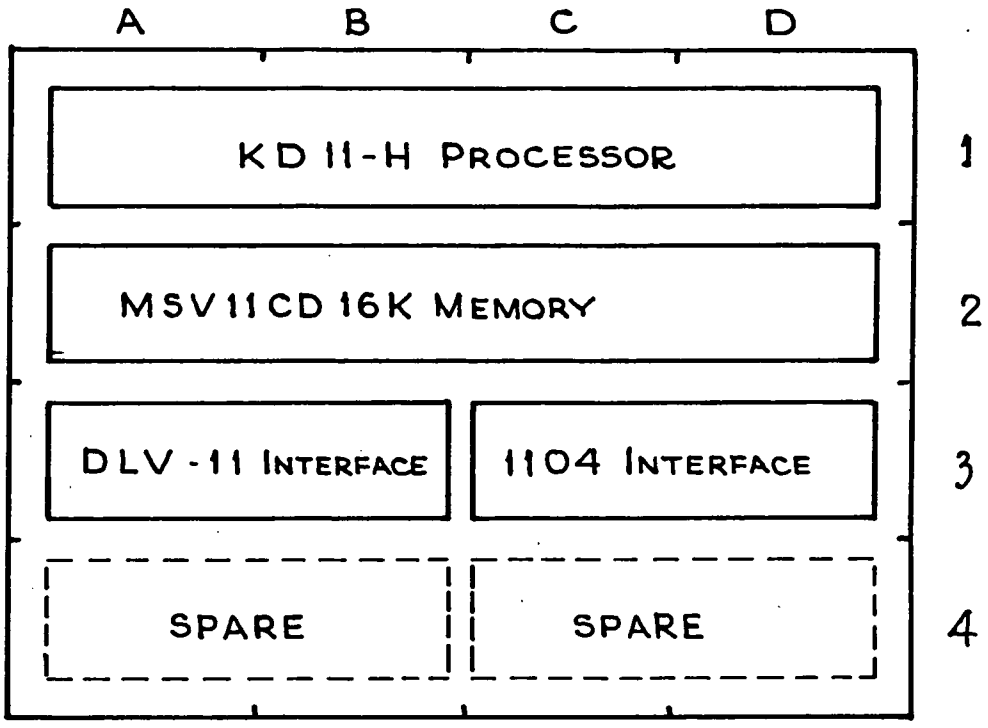


FIG 4.9 CONFIGURATION OF LSI-11 COMPUTER IN 4 x 4 BACKPLANE

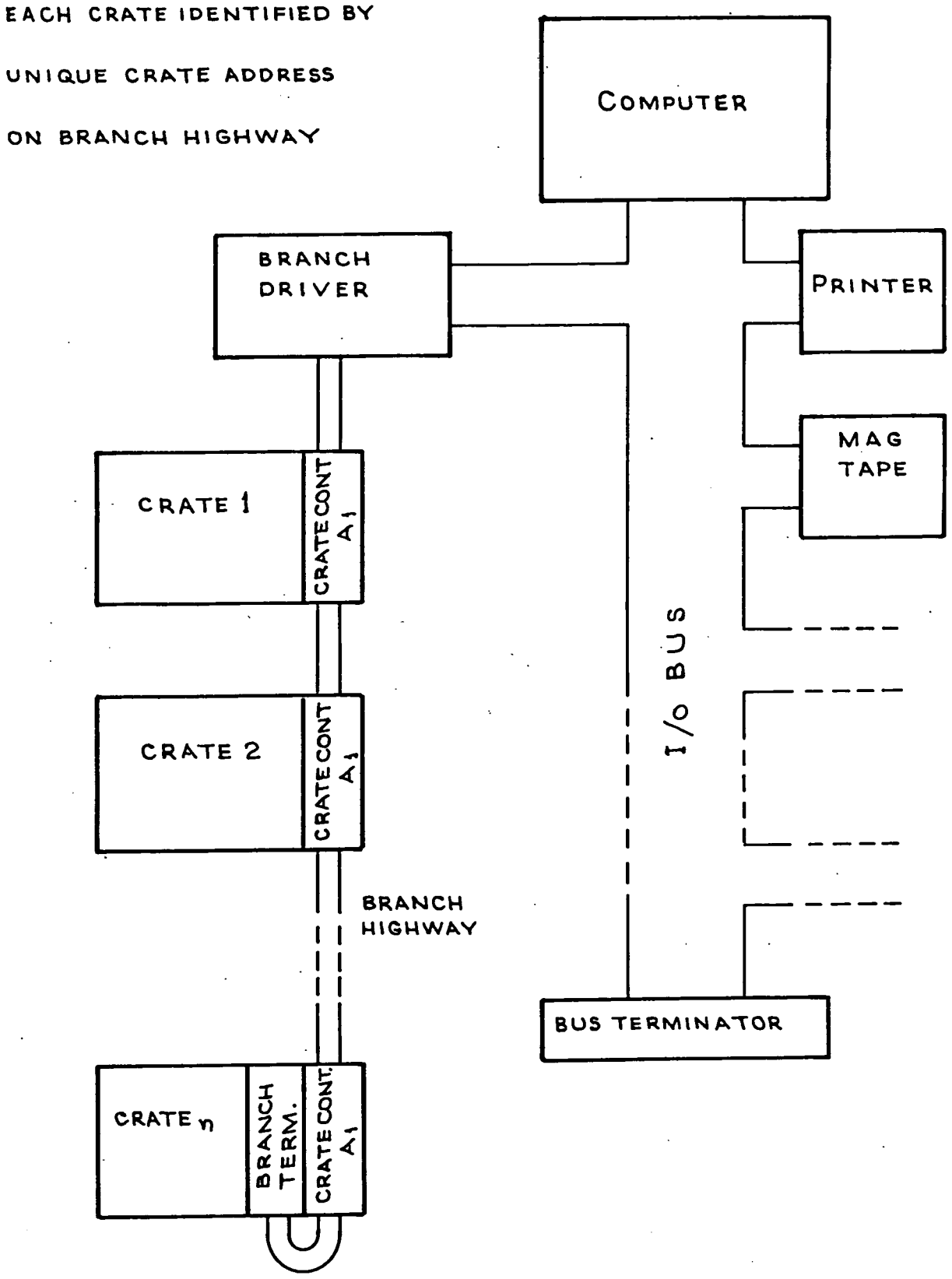


FIG 4.10 MULTICRATE CAMAC SYSTEM USING CRATE CONTROLLER 'A'

The next approach then, was the Dedicated Crate Controller. The Controller is specific to a particular computer and connects directly to the computer I/O bus. There is no Branch Highway, and multicrate systems are configured by using a dedicated controller for each crate, driven off the computer I/O bus. Whilst cheap for single crate systems, expansion to a multicrate system is expensive. A typical multicrate Dedicated Controller system is shown in Figure 4.11.

A third alternative is the System Crate Philosophy, developed by GEC - Elliott[5]. In the two previous systems, control of each crate has been by some sort of controller occupying the rightmost (control) station of that crate. This controller has been connected to the computer I/O bus directly or via the branch highway. In the System Crate Philosophy, there is a master System Crate, at the rightmost station of which resides an Executive Controller. This controller has no connection to any bus other than the CAMAC crate dataway. All other stations of that crate may be occupied by either a normal user module, a Command Source, or a Branch Coupler. A Command Source can be a manual controller, or a computer interfaced controller. Up to ten such Command sources can be resident in the System Crate. These can "talk" to the Executive Controller via the dataway, and the Executive Controller then issues the appropriate commands in the same way as a conventional crate controller. In order to expand to a multicrate system, a Branch Coupler module is inserted in the System Crate. This generates a branch highway as per EUR 4600 which can be used to drive up to seven crates, each equipped with a Crate Controller A-1. Up to seven Branch Couplers can be accommodated in the System Crate, giving a total capability of 49 crates. The advantages of the System Crate concept are several. Multiprocessor control of a single experiment is readily realisable, as is the sharing of common CAMAC peripherals by several experiments, each controlled by their own computer. A typical System Crate configuration is shown in Figure 4.12.

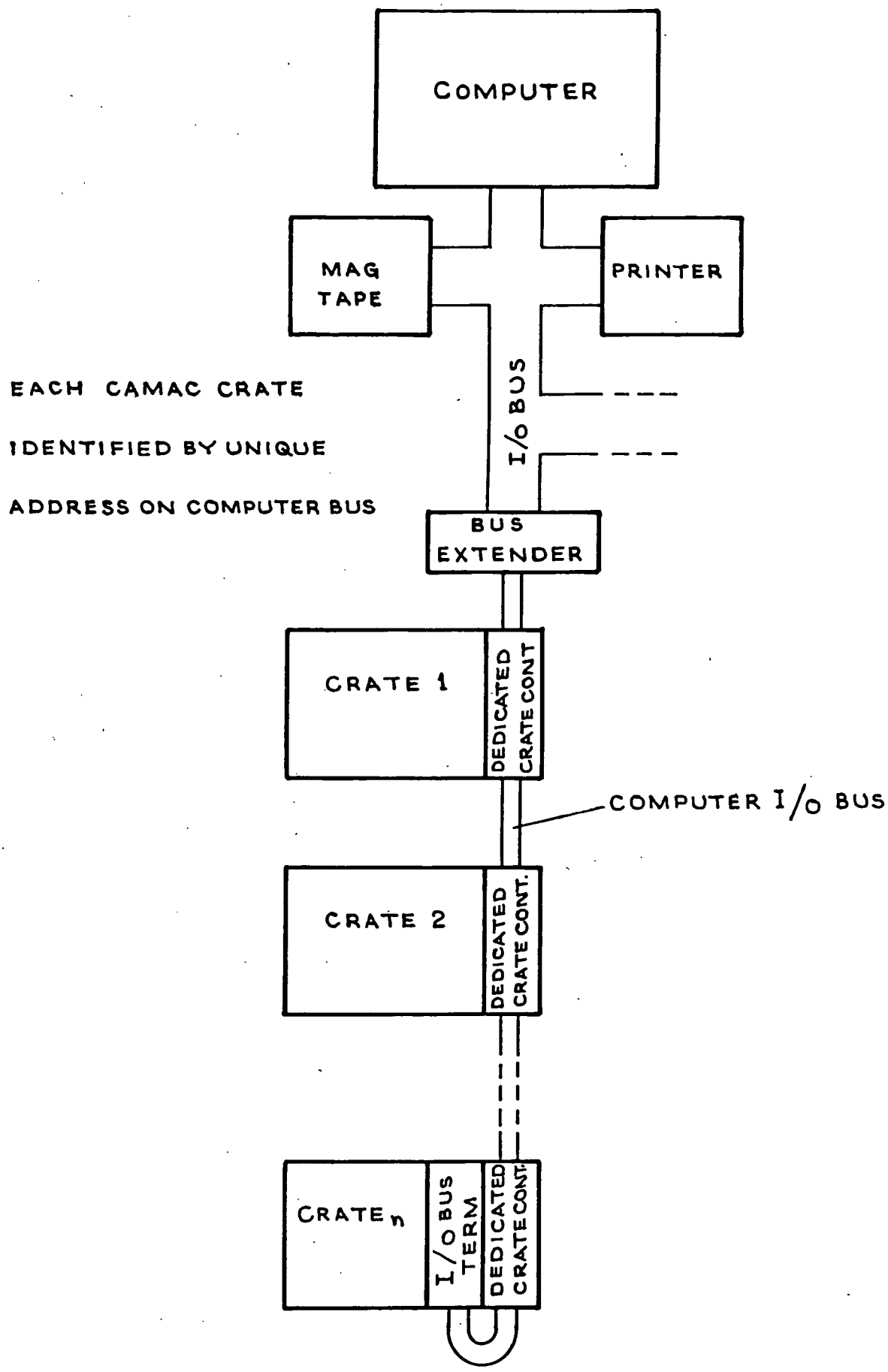
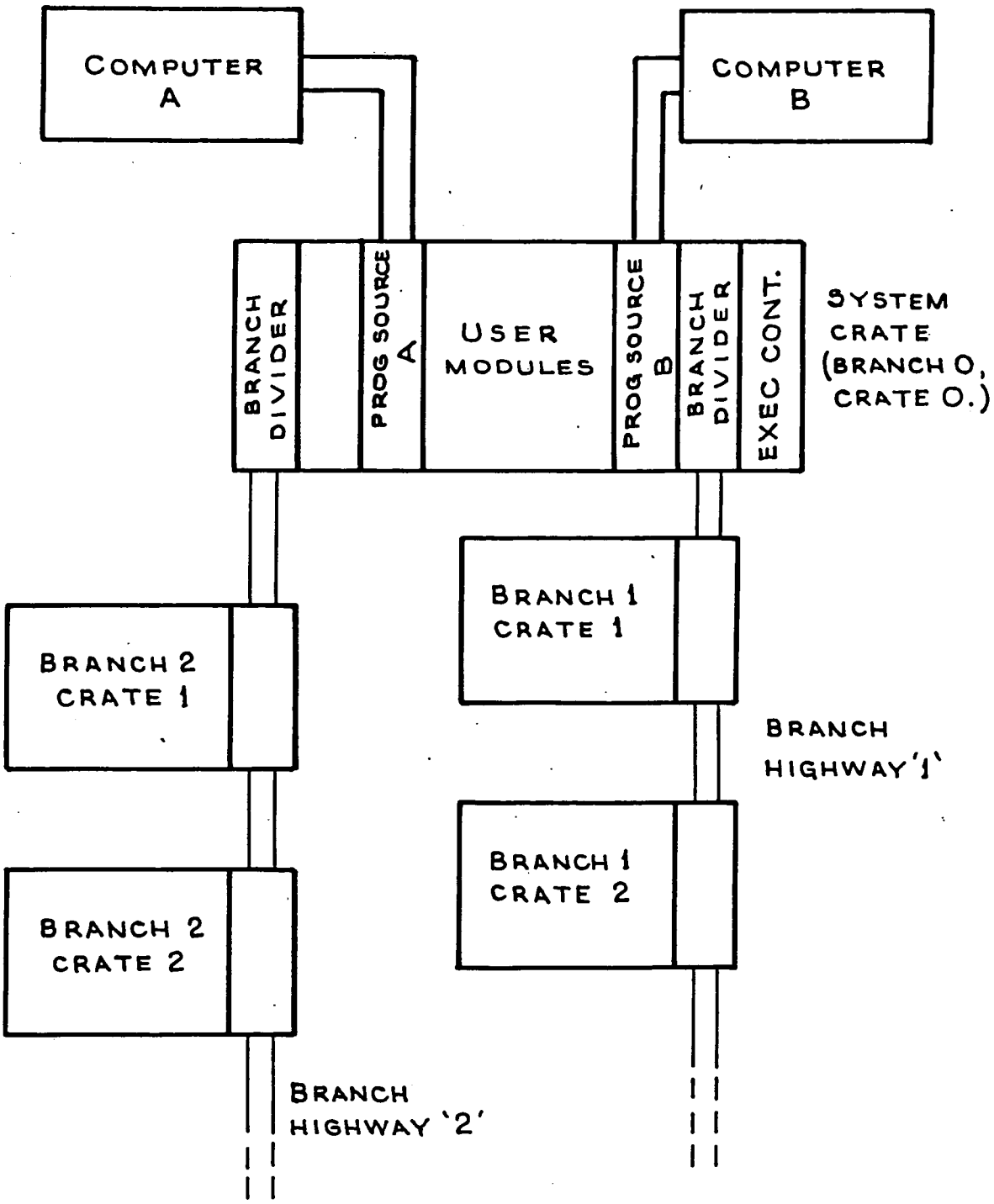


FIG 4.11 MULTCRATE SYSTEM USING DEDICATED CRATE CONTROLLERS



EACH CAMAC CRATE IDENTIFIED BY BRANCH, CRATE ADDRESS

EG B=1, C=2.

N.B. SYSTEM CRATE DRAWN LARGER THAN OTHER CRATES FOR CLARITY

FIG 4.12 SYSTEM CRATE CONFIGURATION

The Crate Controller used for the Durham system is unusual, in that it consists of a System Crate Executive Controller, with a Command Source also built into the same double width module. It offers therefore full System Crate capability while outwardly appearing in a single crate system to be a simple Dedicated Crate Controller. This controller, the Hytec 1100, interfaces to the LSI 11 backplane through the 1104 interface card. This card also provides the functions of the DEC REV 11 card, that is DMA memory refresh and space for bootstrap and diagnostic ROM's.

4.4.3. The CATY Programming Language

The programming language chosen for initial development work is ACSL's CATY 2[6]. This was developed in conjunction with Daresbury Laboratory for the testing of CAMAC modules, but is sufficiently flexible to allow the writing of quite complex control and acquisition programs. CATY 2 is both a language and a resident operating system, with facilities for creating, editing, reading and dumping source program files.

The statement set of CATY 2 is a subset of BASIC, with a number of restrictions, and with the addition of CAMAC I/O, control and interrupt handling statements.

An example of the CAMAC handling ability of CATY 2 is shown in Figure 4.13. This lists four versions of a section of program to read a single character from a paper tape reader: The reader is in station 2 of a single crate system. In example 1, the program issues a CAMAC F27 (test if ready) command to the reader, whose location is branch 0, crate 0, station 2, sub-address 0. If the response is "ready", the module sets the "Q" line on the dataway, and the program responds by issuing a CAMAC F2 (read and clear) command to the reader, and placing the returned data into variable I. Example 2 shows the same routine, but with easily understood mnemonics replacing the CAMAC command numbers (e.g. TST for F27). Example 3 goes a step further by defining a mnemonic for the

```
0001 REM    CATY COMMANDS TO READ A SINGLE CHARACTER FROM A TAPE READER

1000 .
1010 .
1020 .
1150 F27 0,0,2,0
1160 IF NOTQ GO TO 1150
1170 F2  0,0,2,0,I
1180 .
1190 .
1200 .


0002 REM    AS 1 ABOVE,BUT WITH FUNCTION CODES REPLACED BY MNEMONICS

1000 .
1010 .
1020 .
1150 TST 0,0,2,0
1160 IF NOTQ GO TO 1150
1170 RC1 0,0,2,0,I
1180 .
1190 .
1200 .


0003 REM    AS 2 ABOVE,BUT WITH READER ADDRESS DEFINED AT LINE 1000

1000 RDR=0,0,2
1010 .
1020 .
1150 TST RDR,0
1160 IF NOTQ GO TO 1150
1170 RC1 RDR,0,I
1180 .
1190 .
1200 .


0004 REM    AS 3 ABOVE,BUT ILLUSTRATING THE USE OF THE GOSUB STATEMENT

1000 RDR=0,0,2
1010 .
1020 .
1150 GOSUB 2000
1160 .
1170 .
2000 REM SINGLE CHAR. READ
2010 TST RDR,0
2020 IF NOTQ GO TO 2010
2030 RC1 RDR,0,I
2040 RETURN
2050 .
2060 .
```

FIG.4.13 EXAMPLE OF A CATY ROUTINE

reader address. TST RDR,O is much more readily understood by a user unfamiliar with CAMAC than is F27 0,0,2,0. Example 4 shows how this routine can be written as a short subroutine to be called by the main program.

There is an important difference between CATY and BASIC. BASIC is an interpretive language. That is, at execution time, each statement in the source code is translated into machine code and executed before passing on to the next statement. It is therefore slow in execution and not ideally suited to real time systems. CATY source code is compiled prior to execution, producing a more efficient object code with a reduced execution time. To the user, there is no added complication, since the CATY source program is compiled and executed by a single instruction. The utilisation of memory is rather inefficient, since at run time, the operating system, the source code, the compiler and the compiled code are all resident in memory.

A suite of CATY programs was developed for the observational work at the R.G.O. 30" telescope. This suite includes the online program, various routines to read, reduce and display data gathered by the online program, and code conversion programs to produce output paper tapes suitable for reading by mainframe computer system. These programs will be described in more detail in Chapter 6, which deals with that observational work.

4.5. Stand Alone Hardware Configurations

As mentioned at the beginning of this chapter, a large amount of the work on the array was done before the computer controlled system had been completed. For this work, a "stand alone" system had to be put together. It would be misleading to suggest that one single such system was used, since obviously different modules and components of the system were available at different times during the work. One system will be described which is representative of the approach used.

The configuration is shown in Figure 4.14. The Clock Phase Generator, Level Translator and Video Preamplifier are exactly as used in the computer controlled system. The waveform is observed by an oscilloscope with triggering derived from the LSR pulses. A delayed time base facility is used for observing whichever diodes are desired. Overall timing is again derived from an HP 8004A pulse generator. The integration control is achieved by the two additional modules, the Programmable Divider, and the Stand Alone Controller. The functions of these two modules is as follows. The Programmable Divider is used to gate the LSR pulses. Two front panel thumbwheels, designated m and n, set up a counting cycle of $m \times 10^n$, which is used to divide the incoming LSR pulses. Thus Figure 4.15 shows the effect on the pulse timing of a count cycle of 3 ($m = 3$, $n = 0$).

This module alone permits repeated exposures with identical integration times.

Further control is achieved by using the Stand Alone Controller. This enables the user to scan the array onee per frame time until the front panel "START" button is pressed. At the next frame, the integration period set by the Programmable Divider begins. This selected period is repeated until such time as the "HALT" button is pressed, whereupon scanning resumes once per frame time. The usefulness of this type of operation will be shown in the following chapter.

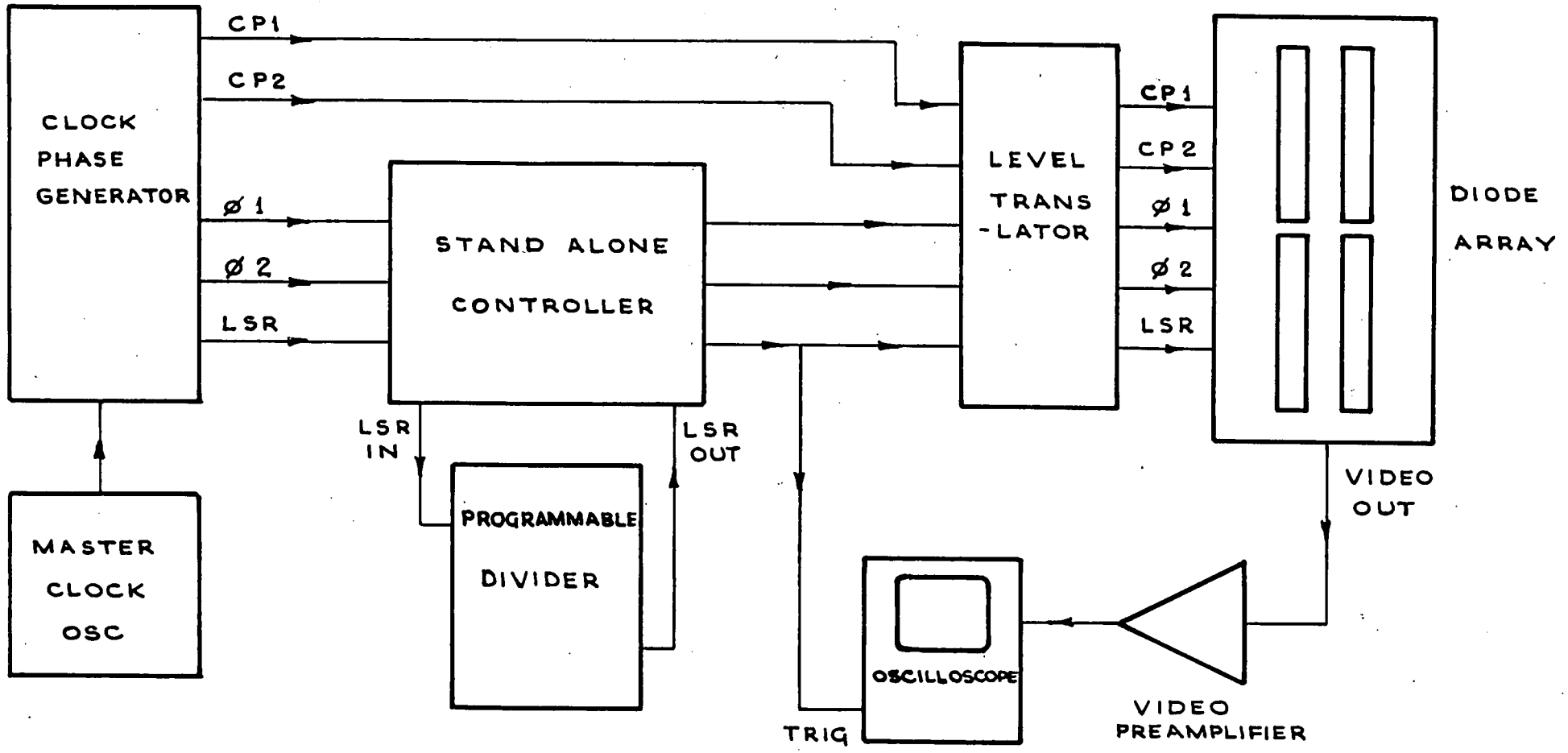


FIG 4.14 STAND ALONE CONTROL CONFIGURATION

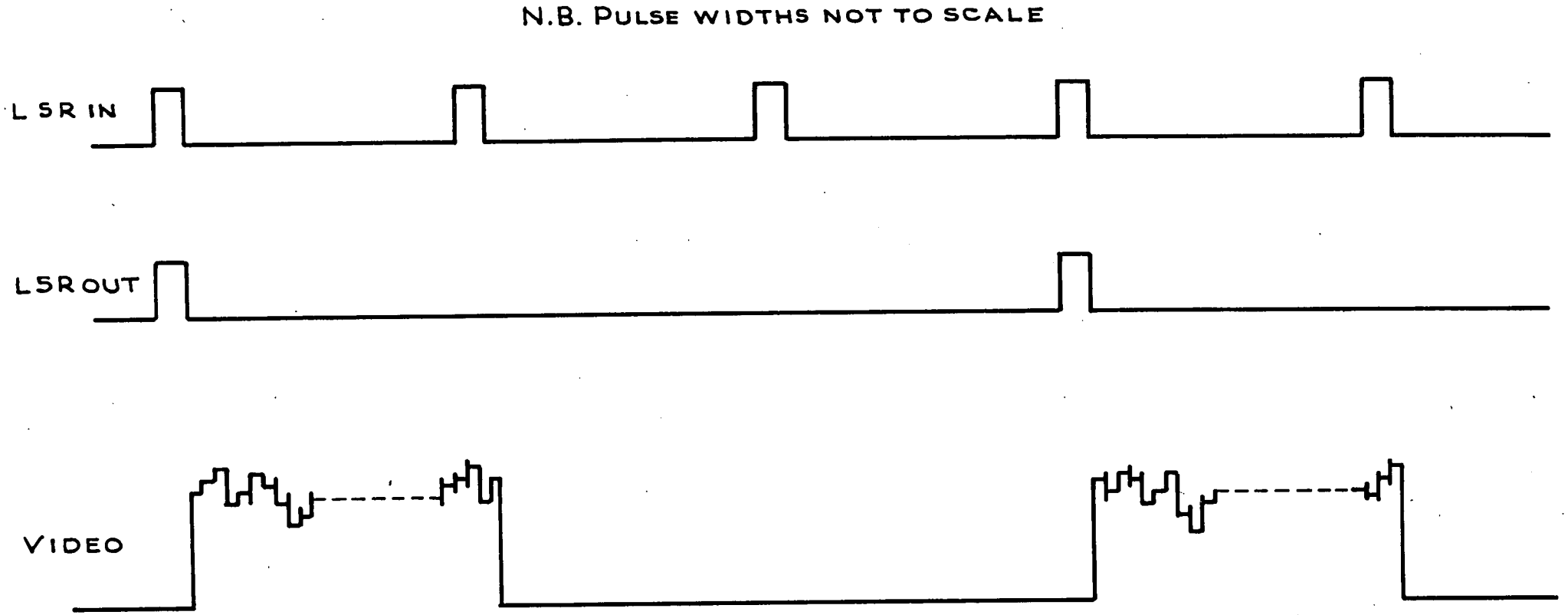


FIG 4.15 TIMING OF A 3 FRAME INTEGRATION PERIOD USING THE PROGRAMMABLE DIVIDER

4.6. Summary

A complete computerised control and data acquisition system has been designed and constructed for the Plessey diode array, based on the requirements of the optical imaging project. The system is modular and based on the CAMAC concept. Control is by a small PDP 11/03 microcomputer running the CATY 2 programming language. Provisions have been made for operating a part of this system under manual control, primarily to enable experimental work on the arrays to continue before the system development was complete.

REFERENCES

1) G.B. Wellgate, Royal Greenwich Observatory, unpublished notes.

2) "Introduction to CAMAC", CERN - NP CAMAC Note 25-00, 1971.

3) A.W. Campbell, Ph.D. Thesis, University of Durham, in preparation.

4) EUR 4600, published by European Standards Organisation on Nuclear Electronics (ESONE), 1971.

5) "Configuring CAMAC System Controllers", GEC - Elliott Publication A.2951.1, 1977.

6) "The CATY Reference Manual", F.R. Golding, Applied Computer Systems Limited, U.K.

CHAPTER FIVE

Laboratory Measurements on the Characteristics of the Plessey Diode Arrays

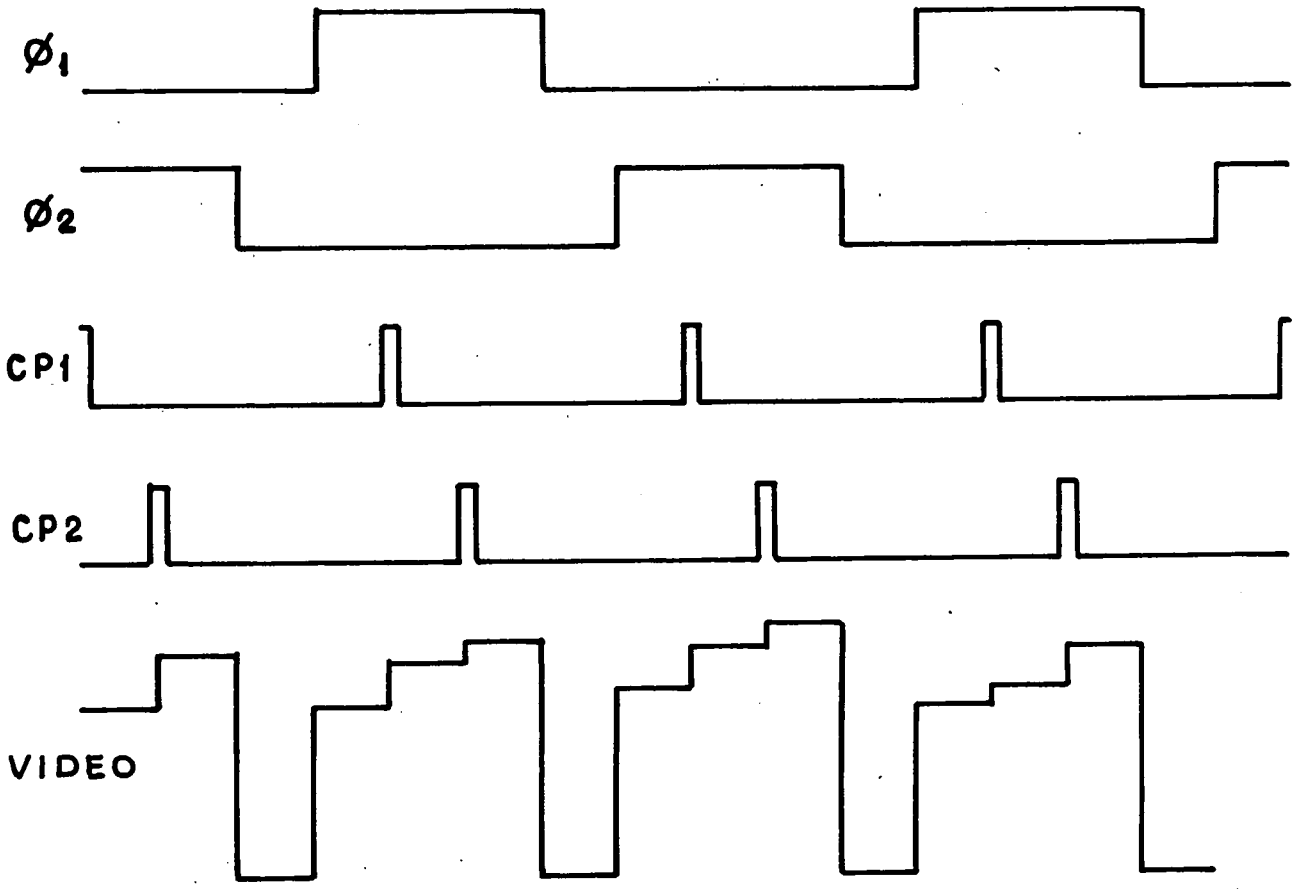
In this chapter, a programme of tests carried out on the arrays is described. Most of the tests were carried out at Durham prior to the operation of an array at the 30 inch telescope at the R.G.O., (the exceptions being tests on spectral response and the response to a pulse input of light). Tests include observations of responsivity, leakage current, random noise, linearity and lag.

5.1. Equipment used for Laboratory Tests

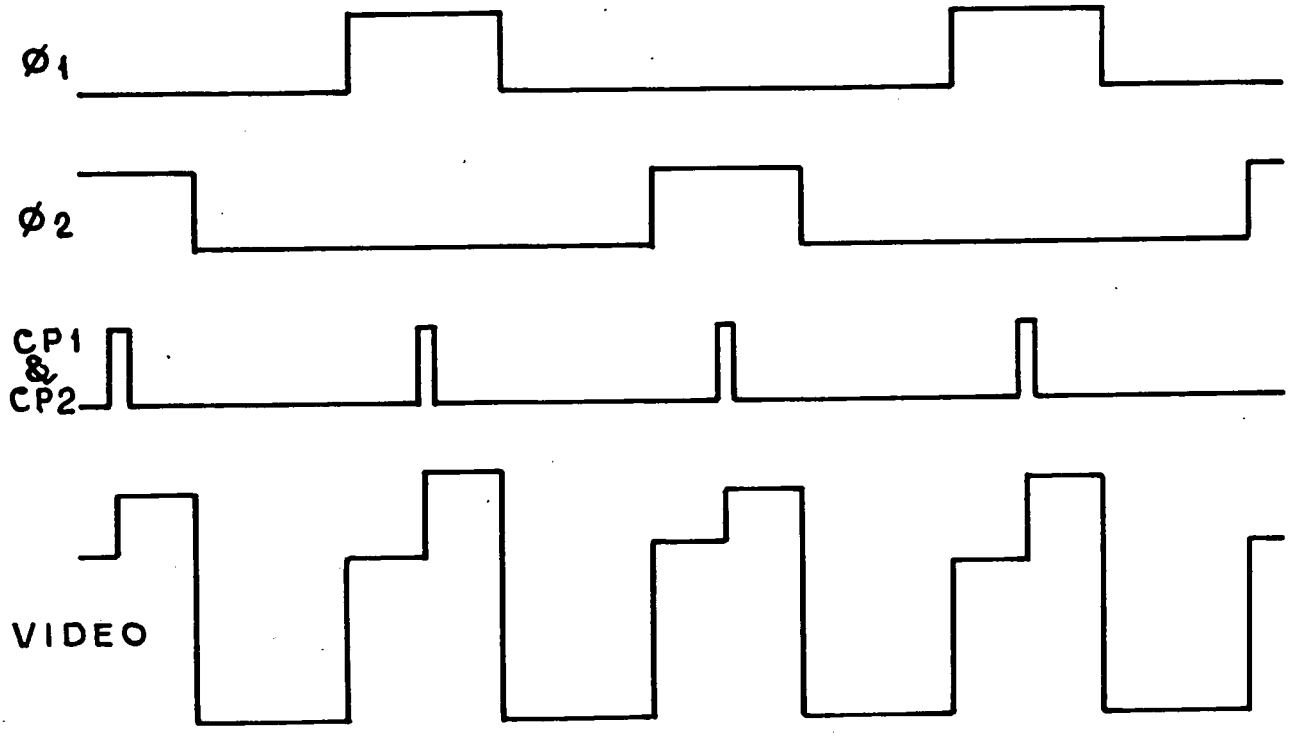
As was described in Chapter Four, for most of these tests a simplified hardware - only control system was used. Also of interest are a simplified charge pulse scheme used for some early work, and the cryogenic system used to cool the array. These will be described briefly in the following sections. Other equipment used for specific tests will be described along with these tests.

5.1.1. Charge Pulse Timing

Figure 5.1 (a) shows the conventional charge pulse timing and its relationship to the video waveform, as has been described in Chapters Three and Four. To recap, the first level of the video waveform is the sum of the integrated signal on both diodes of a pair. After CP1, the first diode has been recharged and the second video level now represents the signal on only the second diode. Following CP2, the second diode has also been recharged and the third level of the video represents the fully charged state of both diodes.



(a) TWO CHARGE PULSE SCHEME



(b) SINGLE CHARGE PULSE SCHEME

FIG 5.1 CHARGE PULSES AND DIODE PAIRING.

A simpler timing scheme is shown in Figure 5.1 (b). Note that the mark/space ratio of the two clocks Ø1 and Ø2 has been reduced. This is not particularly important and has been done to simplify the sequencing logic. CP1 and CP2, the two charge pulses, are now coincident. This results in a simpler video waveform, where the first level corresponds to the sum of the signals on both diodes in a pair, and the second level results from charging both. This leads to some degree of simplification when carrying out measurements with only an oscilloscope available.

5.1.2. Cryogenics

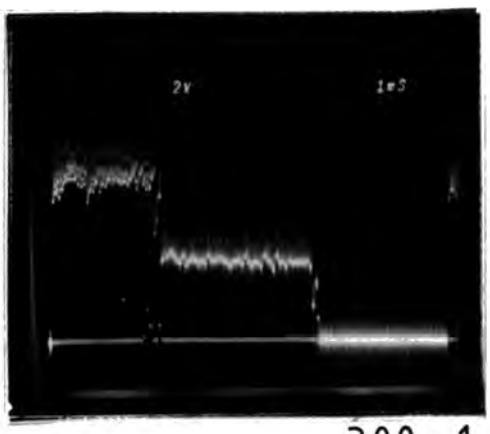
The cryostat used throughout this work is a simple "cold finger" system. It is described in detail by A.Humrich[1)], and will only be mentioned briefly here. Cooling is by means of a brass finger, the bottom end of which is immersed (usually) in liquid nitrogen. The array is mounted on a brass block at the upper end of the finger. A heating resistor and a copper-constantan thermocouple are mounted adjacent to the array. The cryostat is evacuated by a simple rotary pump in order to reduce heat influx from the walls of the enclosure. Temperatures of down to about -120^{o} C have been measured at the thermocouple.

5.2. Preliminary Evaluation of the Available Devices

Four packaged arrays were made available for tests at Durham. Each array has four video lines, but it was necessary to determine how many of these were functional. The arrays were tested one line at a time. The arrays were operated in the dark at room temperature, free running (one scan every frame time) with a two charge pulse system and a frame time of 10 ms. Figure 5.2. shows the outputs obtained from the video preamplifier for the video lines found to be operational, and Figure 5.3. summarises the availability of working lines on each of the arrays (designated as arrays no. 300 to 303 by Plessey).

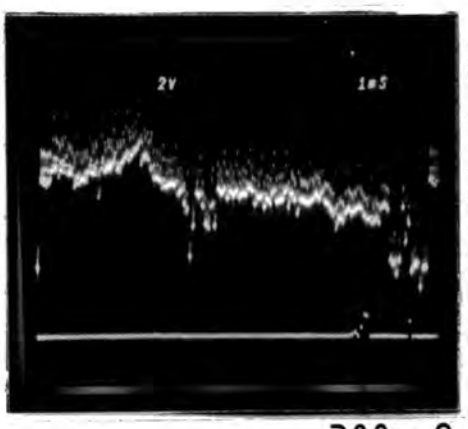
Considerable variations are obvious in the level of fixed pattern offset noise between the arrays, from the reasonable (Figure 5.2. (a), Array 302, Video 3) to the appalling (Figure (b), Array 300, Video 2).

Video line 1 of device 300 exhibits a very interesting fault. The first 66 (approx) diodes appear to function satisfactorily. Diodes 67 to 165 do not receive CP2, presumably because the CP2 line is broken by a defect at diode 66. Thus the second diode of each pair is permanently fully discharged. From diode 165 onwards, the CP1 line is also broken. For early experimental work, the first section of diodes of this video line was used, so that in the event of any inadvertent damage, a scarce, fully working video line would not be lost. Video line 3 of array 302 was chosen as the line to use for observational work. Note that regretably there is no array which has a line of 512 working elements.



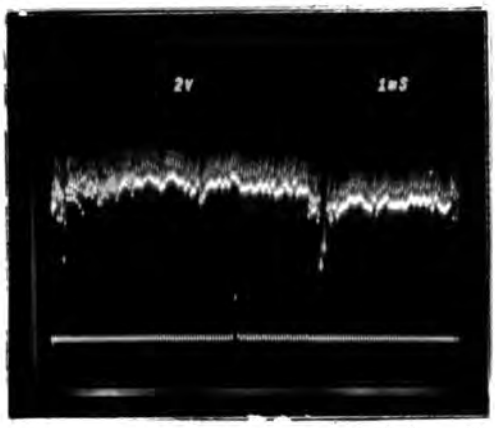
300 - 1

(a)



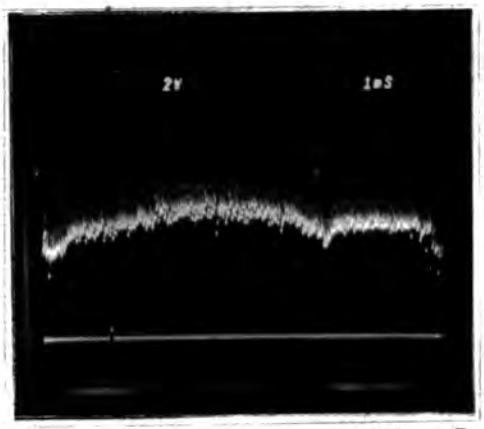
300 - 2

(b)



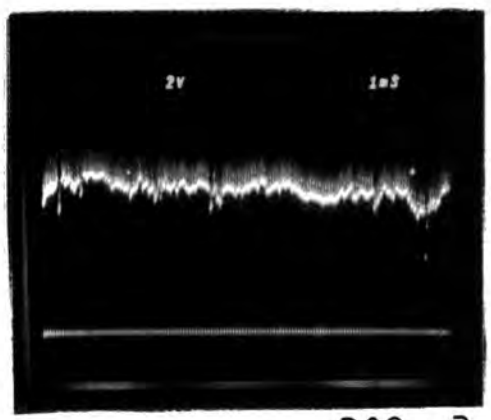
300 - 3

(c)



301 - 3

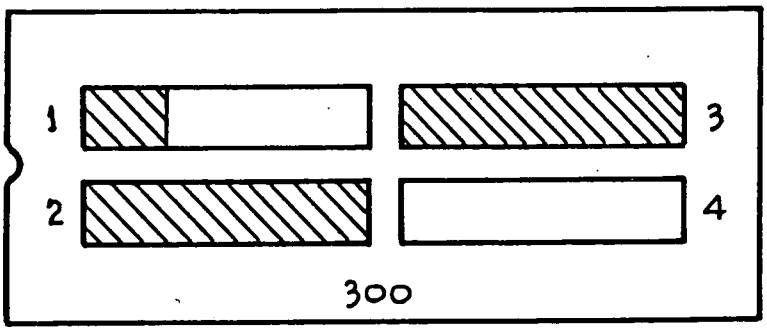
(d)

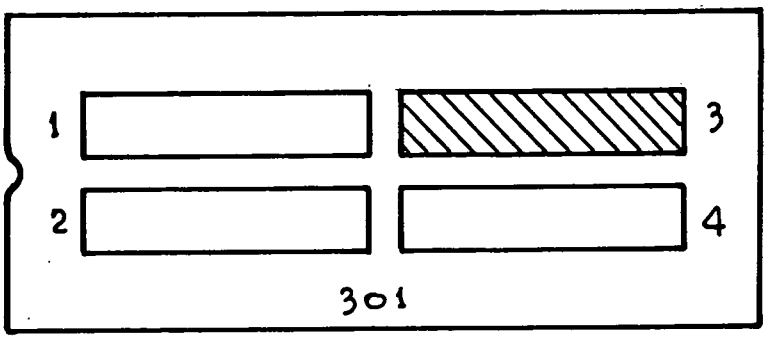


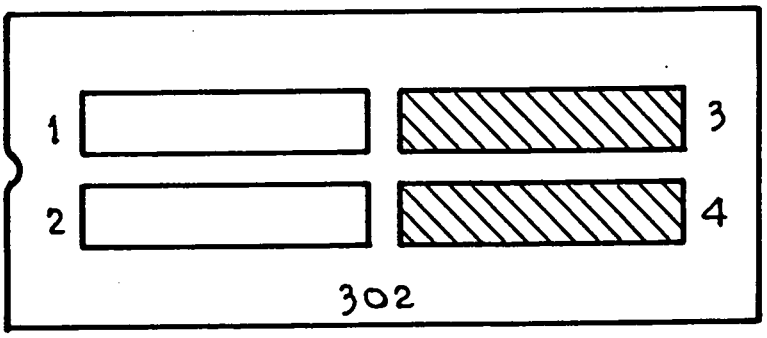
302 - 3

(e)

FIG. 5.2. FUNCTIONAL VIDEO LINES







(d) ARRAY 303 - NO GOOD LINES

FIG 5.3 USEABLE VIDEO LINES (SHADED AREAS)

Also note that the fixed pattern offset noise is not entirely random. That is, there is some definite local correlation of offset. This is perhaps best illustrated by Figure 5.2. (d), showing Video line 3 of array 301. It will be recalled from Chapter 2 that the chief sources of fixed pattern offset noise are variations in the β and threshold voltage of the source follower, and in the "on" resistance of the multiplexing transistor. These are process dependent, and in the case of the "on" resistance, geometry dependent. The process parameters may well change slowly over the length of the array, but are unlikely to vary much from element to element. This probably gives rise to the distinct shape of the offset variations.

5.3. A Measurement of Photoresponse

It was calculated in Chapter Four that an output change of approximately 1.7 μV is expected for each carrier contributing to the leakage current (of either thermal or photon origin), this using a virtual earth output amplifier with a feedback resistance of 68 kΩ. A simple experiment was carried out to see if this was the case, although the accuracy of the experiment was really only sufficient to prove that the responsivity was or was not roughly as it should be.

A Centronic OS1-5K phototransistor was used as a reference detector. This was calibrated by the manufacturer at three wavelengths, and is also supplied with a "typical device" responsivity curve. A crude "optical bench" was constructed out of brass tube with a light source at one end, and either of the two detectors (the array or the phototransistor) could be placed at the other end. The light source was a domestic torch bulb running from a variable power supply, and a narrow band filter of wavelength 5434Å (Barr and Stroud 09D26). This set up produced an output of 4mV from the phototransistor, and from the manufacturers data, this was calculated as an incident light flux of :-

$$3.48\ 10^{-4}\ W.m^{-2}$$

For photons of this wavelength, this corresponds to an incident photon rate of :-

$$9.51\ \ 10^{14}\ \text{photons}\ s^{-1}\ m^{-2}$$

By using the array in place of the phototransistor, an output of 3.4V was observed (from a diode pair) for a 30 frame integration at a frame period of 11.2mS. At the time of the measurement the feedback resistance in the Video Preamplifier was 47kΩ. Using these figures yields a voltage decay rate of :-

5.05 V s^{-1} for a single diode

corresponding to a responsivity of :-

0.67 μV/incident photon

Two factors must be applied to compare this with the 1.7 μV/carrier predicted in Chapter Four. The feedback resistor is here 47kΩ rather than 68kΩ. Correcting for this brings the responsivity to :-

0.96 μV/incident photon (for R_F = 68kΩ)

This is in terms of incident photons and takes no account of the quantum efficiency of the array. Published data for other arrays suggests a quantum efficiency of around 60% at this wavelength. This would give a responsivity of :-

1.6 μV/detected photon

Thus the predicted (1.7 μV/carrier) and measured (1.6 μV/detected photon) values for responsivity agree remarkably closely, especially since in both cases a fair amount of (hopefully) educated guesswork is involved.

5.4. Thermal Leakage Current Measurements

The use of these arrays for astronomical imaging work depends very much on whether the thermal leakage current can be reduced to an significant level by cooling in order to achieve long integration periods. For this reason, some studies were carried out into the behaviour of the thermal leakage current. Two characteristics are of interest. First is the way in which the video levels decay with time, and second is the way in which the leakage current behaves as a function of temperature.

5.4.1. Thermal Leakage Signal as a function of Integration Time

If we wish to study the signal produced by the thermal leakage current as a function of integration time, there are two possible approaches.

The first method is to scan the array with a given integration period, measure the signal levels, and repeat the measurement with different integration periods until sufficient data has been obtained. This is a suitable approach when the integration periods involved are short. Figure 5.4. shows the results obtained for a pair of diodes in array 300, at room temperature (23^{o} C). The frame period was 11.2mS, and the points obtained represent integrations of 1 frame 2 frames, 3 frames etc. The upper line represents V_{RESET}, the voltage to which the diode pair is recharged by the charge pulse. V_{SIGNAL} is the level on the diode pair prior to recharge, and as expected, decays with time.

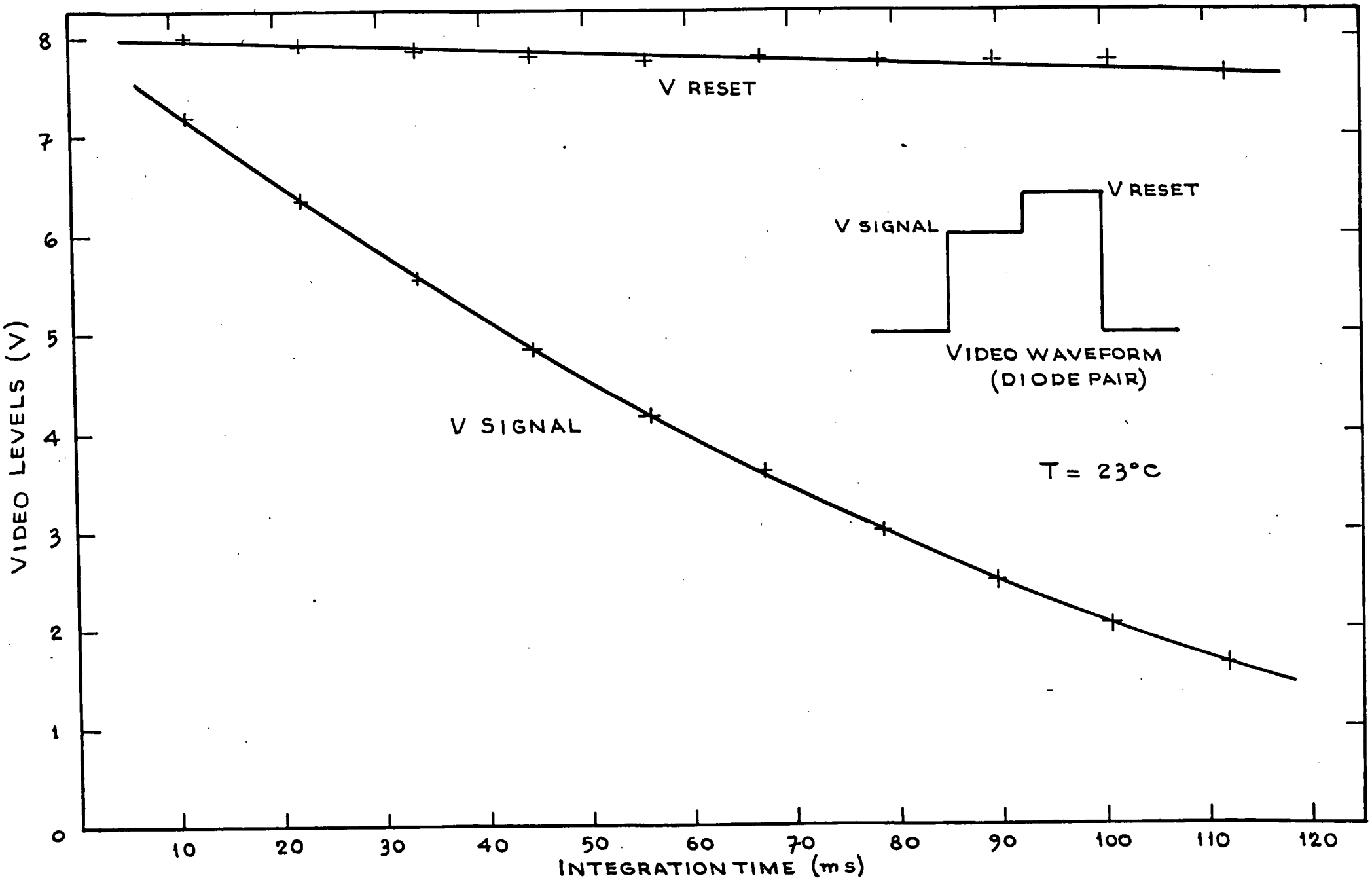


FIG 5.4 OBSERVED DECAY OF VIDEO WAVEFORM DUE TO THERMAL LEAKAGE

The decay is approximately linear at first, until the array output appears to saturate at a total voltage swing of around 7V (3.5V per diode).

The decay rate at room temperature due to thermal leakage, from the above measurements, is 33 V s^{-1} per diode.

These figures can be translated into terms of carriers from the results of the previous section. The feedback resistance is 47kΩ for these measurements, so we have a responsivity of about 1.14 μV/carrier, and thus the dynamic output range becomes about :-

3.1×10^6 carriers

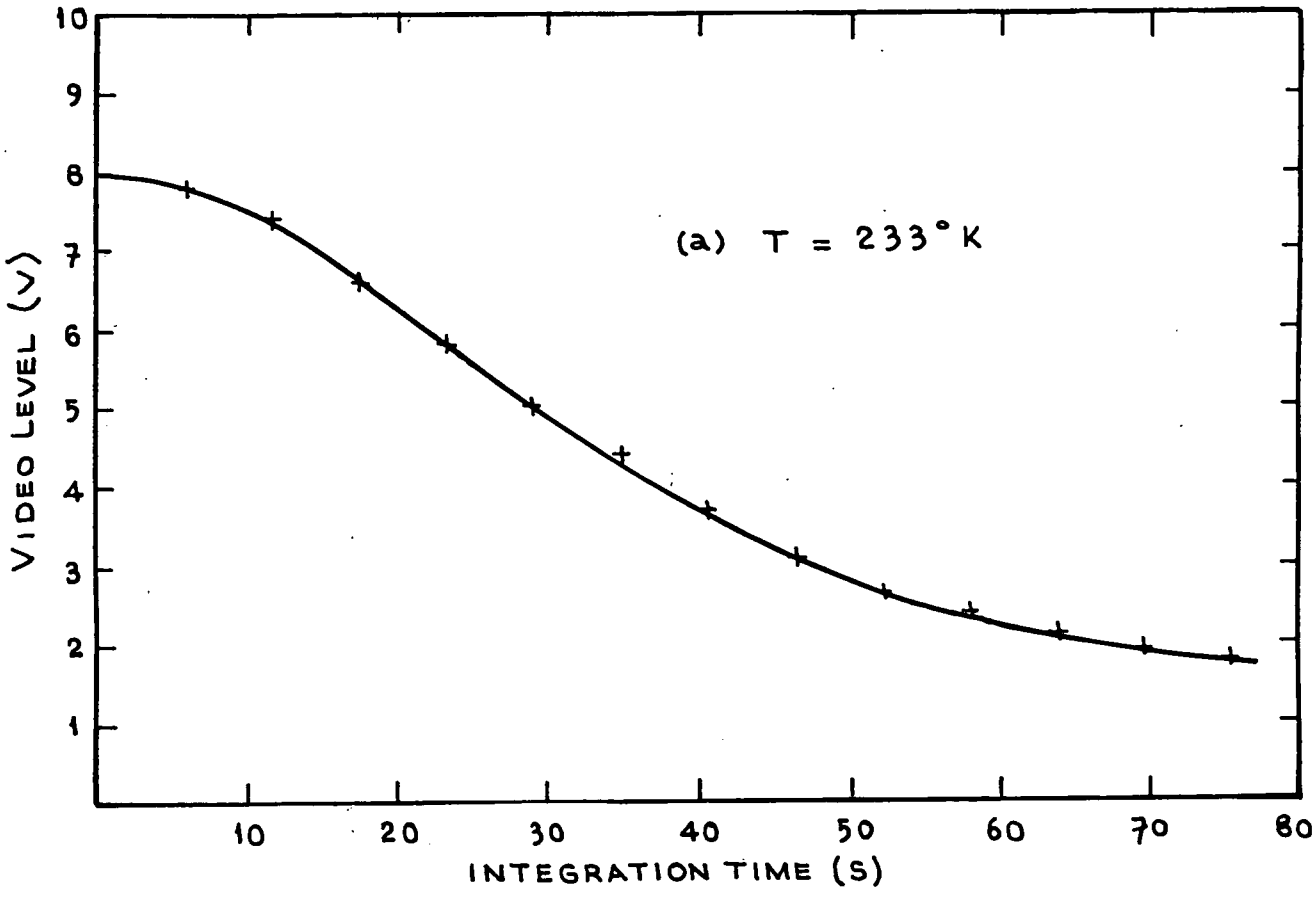
and the thermal leakage at room temperature becomes about :-

29×10^6 carriers s^{-1}

This method of observing the leakage current becomes lengthy and difficult for long integration times (at low temperatures). The second method that has been used, for longer integration times, is to scan the array at a constant frame time, but to disable the charge pulses simply by switching them off. The video level corresponding to a diode pair now has no reset level of course, but the signal level on the diode pair can be observed.

The results of two such observations at different temperatures are shown in Figure 5.5. The upper graph (a) was obtained at a temperature (measured at the thermocouple) of 233^{o}K, and the lower graph (b) at a temperature of 206^{o}K.

The shapes of the two carriers are similar, an initial period of slow decay, followed by a linear decay until the signal begins to reach saturation. This is a commonly observed shape when carrying out this type of observation.



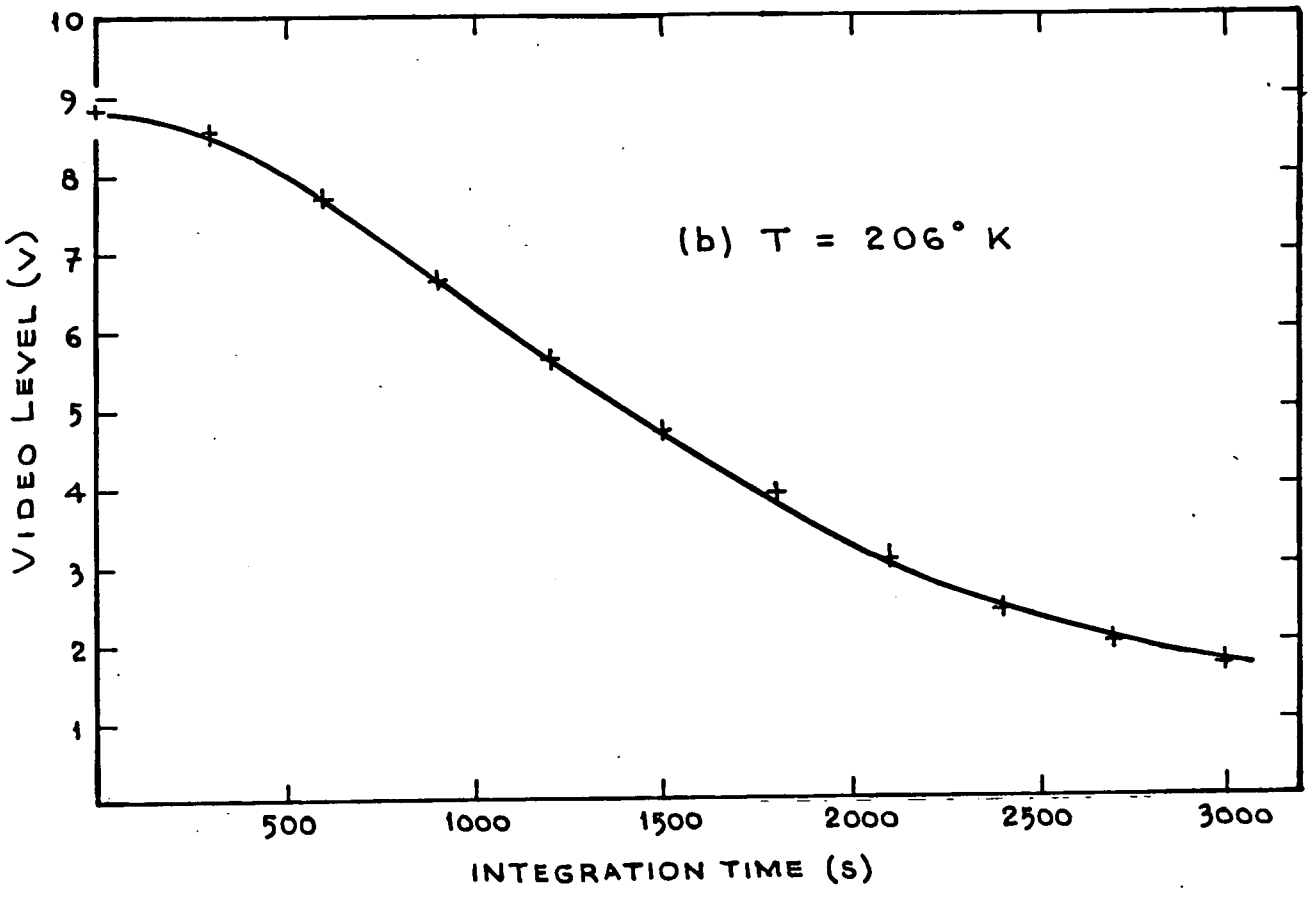


FIG 5.5 LEAKAGE CHARACTERISTICS AT LOW TEMPERATURES

The presence of this plateau at early times appears to indicate a threshold affect. It seems that the leakage current does not begin to affect the output signal until the integrated dark signal has exceeded a certain value. The investigation of this plateau region proved extremely difficult, as accurate repetition of the effect was not possible, probably due to lack of repeatability of the thermal conditions with the rather crude temperature control system.

5.4.2. Leakage Current as a function of Temperature

The thermal leakage current has been measured over a wide range of temperatures using the methods described above. The leakage rate has been taken as the gradient of the linear part of the decay, measured in V s^{-1} per diode. This has then been converted to units of carriers/sec/cm^2 to enable comparison with published results for other arrays. Figure 5.6. shows the leakage current calculated in this way and plotted as a function of temperature.

The points marked as solid circles were obtained using the heater in the cryostat to generate the desired temperature. As mentioned, this is not a very satisfactory arrangement and probably accounts for the spread in the data. The three data points plotted as crosses, however, were obtained without the use of the heater, and are better defined and more repeatable.

The high temperature point is room temperature ($297^{o}K$) obtained with the cold finger of the cryostat in free air.

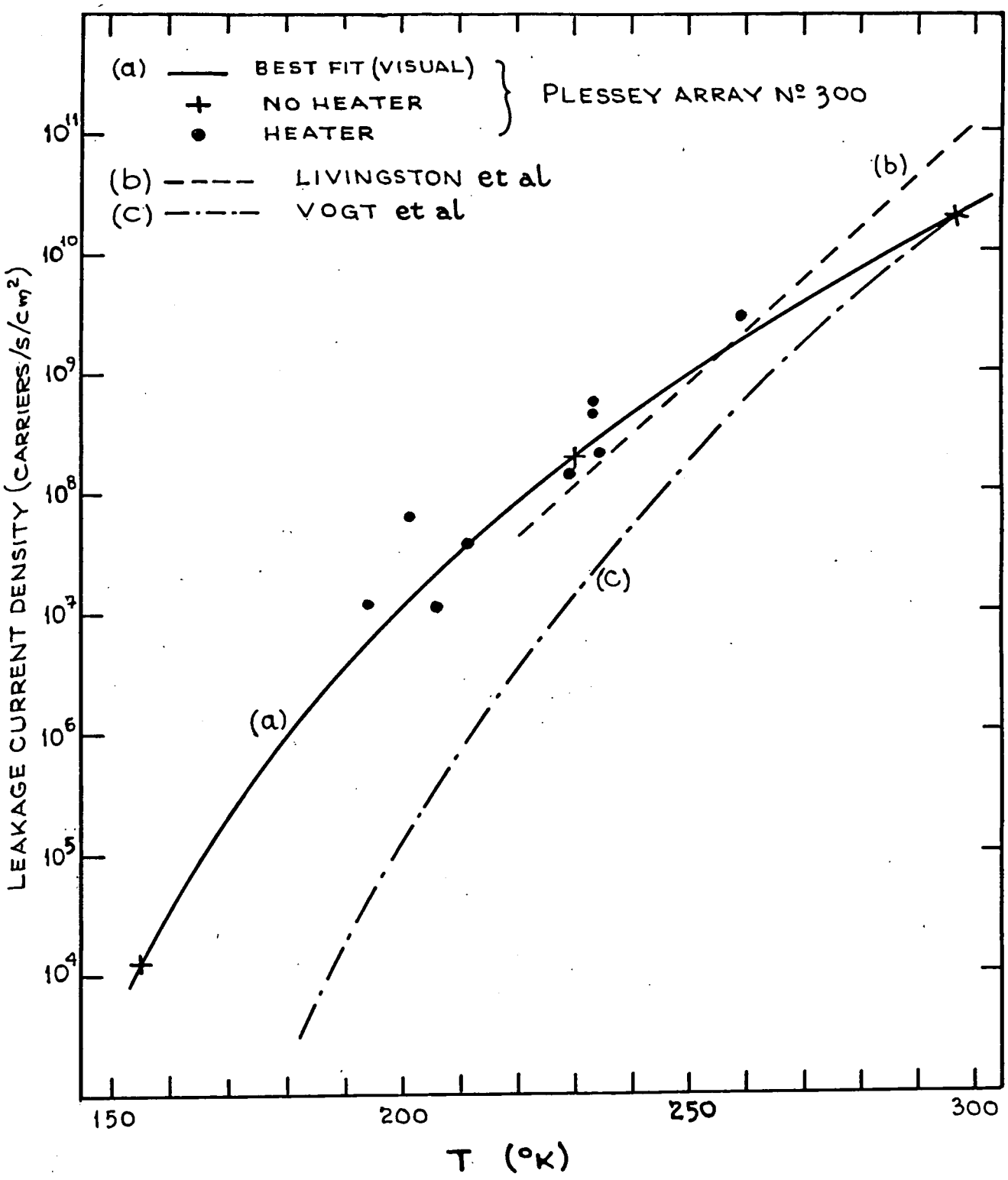


FIG 5.6. OBSERVED LEAKAGE CURRENT DENSITY, AS A FUNCTION OF TEMPERATURE

The low temperature point (155^{o}K) was achieved by immersing the cold finger in liquid nitrogen and without using the heating resistor. The intermediate point (230^{o}K) was obtained by immersing the cold finger in a freezing mixture of dry ice and acetone, again with no heater.

The solid line drawn on the graph is a visual "best fit" to the data. Two other lines are shown for comparison. Line (b) is a fit to the data obtained by Livingston et al[2] according to the empirical relationship by Geary[3].

$$I_L = I_o \; 2^{(T-T_o)/\alpha}$$

and is taken from Figure 2.7. Also from Figure 2.7. is the curve plotted as line (c) in Figure 5.6. This is a fit to the data of Vogt et al[4] according to the relationship

$$I_L = \text{const. } T^{3/2} \exp(-7015/T)$$

derived by Campbell[5].

The data for this array clearly does not fit the empirical relationship of Geary, as this would plot as a straight line on Figure 5.6. It is also seen to deviate from the behaviour predicted by Campbell. It does however have a similar order of magnitude in the room temperature region to the leakage currents observed by these workers. G.R. Hopkinson[6] has shown this experimental data to fit well to the relationship,

$$I_L = \text{const. } 10^{-2000/T}$$

In the region around room temperature, the leakage current approximately halves for every 8^{o} drop in temperature.

The decay rate due to thermal leakage at the coldest point measured was 1.08 $\mu V\ s^{-1}$ per diode. From Section 5.4.1., this would saturate the array in about 3.24×10^6 seconds, or 900 hours! Thus by cooling the cryostat with liquid nitrogen, we can easily reduce the leakage current to the point where it is negligible.

5.5. Spectral Response

The measurement of spectral response was not possible at Durham due to the (at that time) very limited optical test facilities available. Following the completion of the observational tests at the R.G.O., a monochromator belonging to Dr Mc. Mullan's group was made available to us for a short period. Transporting the entire system from the dome of the 30" telescope for the tests was impractical, and therefore the measurements were carried out with the minimum of supporting electronics. The Clock Phase Generator was used operating in a stand alone fashion, so the integration period was equal to a single frame period. The frame period was adjusted to give a "sensitivity" suited to the available light levels, by varying the input clock frequency. Signals were monitored by an oscilloscope at the output of the Video Preamplifier. The usable range of the monochromator was 400 - 1000 nm. The measurement was done twice, once with the array at room temperature ($20^{o}C$) and again with the cryostat cooled by liquid nitrogen to about $-120^{o}C$. The relative spectral responses obtained are plotted in Figure 5.7. This demonstrates the increase in sensitivity at the red end of the spectrum at the higher temperature. This was described in Chapter 2, and is due to the increase in the silicon band-gap energy with temperature.

No interference effects are visible in this data. However, the light was not well collimated and the measured points are at intervals of 50nm. It is possible that such effects will be observed under more carefully controlled experimental conditions.

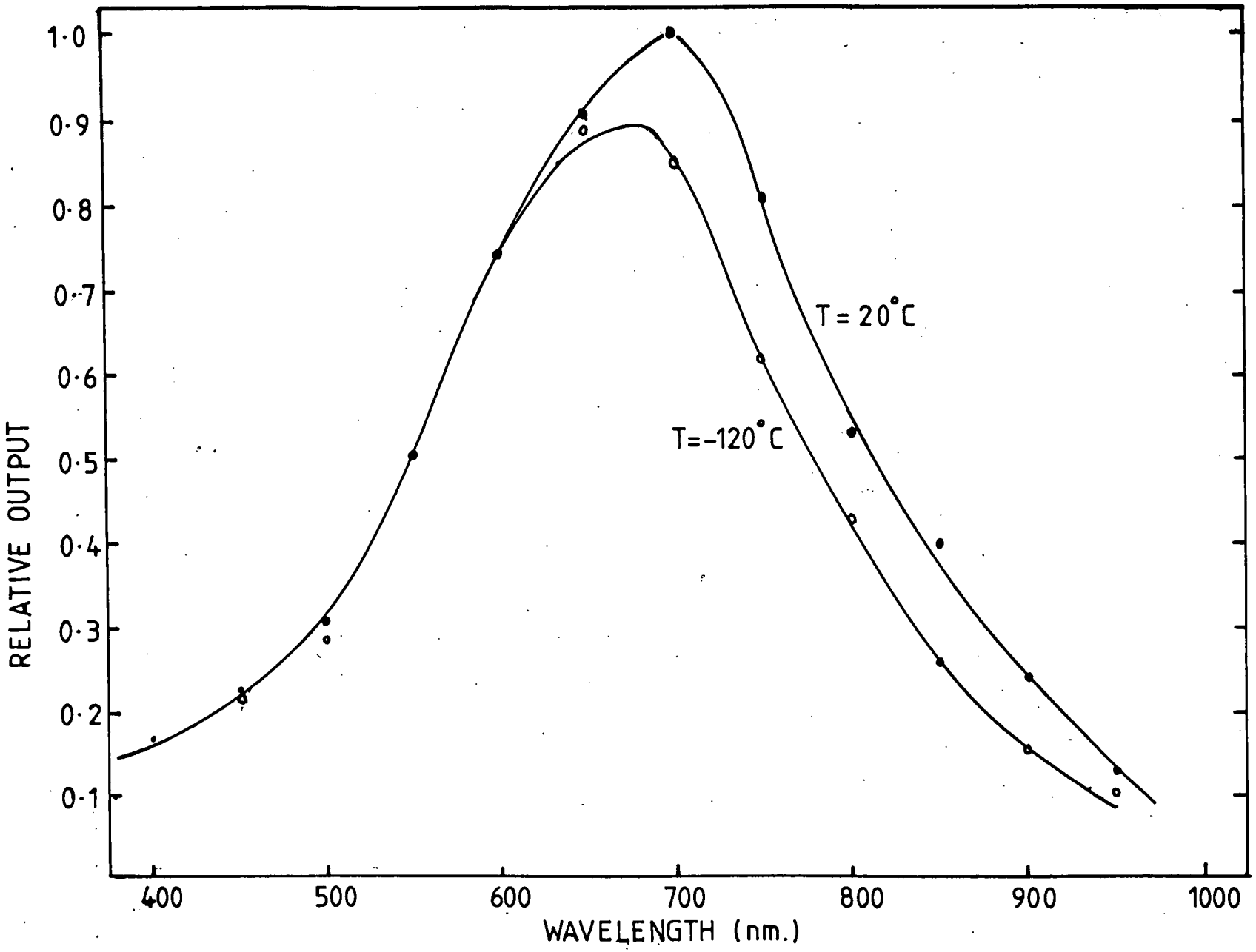


FIG.5.7. SPECTRAL RESPONSE

5.6. Random Noise Measurements

The preliminary investigations into the random noise characteristics of the array have been described in detail in an Internal Report [7]. A brief mention will be made here of some of the findings.

Due to the wide variations in offsets from diode to diode, it is possible to select a diode and amplify its video level such that with a suitable D.C. offset on the oscilloscope, that video level is the only trace visible on the oscilloscope screen. For example, at a vertical gain of 5mV/DIV (50mV full scale), if the mean video level for the desired diode is displayed at the centre of the screen, an uncluttered trace can be obtained as long as no other video level in the frame is within 25mV. Then by running with a time base that is very slow compared to the frame time, a "history" of a particular video level can be built up over a large number of frames.

By "pairing" the charge pulses, and running the array in the dark and cooled by liquid nitrogen, there is a difference of a few millivolts between the signal level and the reset level of a pair of diodes. This difference is in fact of the opposite sense to that expected, but this will be discussed in Chapter 6, and is not important here.

This difference of a few millivolts works to our benefit, as it is possible to display simultaneously the signal level and the reset level of a pair of diodes. Figure 5.8 shows such a "history" of the two levels with the array operated at a frame time of 11.3 mS. The levels appear as wide bands rather than lines because of the ringing and switching transients that are superimposed on the video. From this trace, it can be seen that there is indeed a correlation between the variations on the two levels, with a correlation time of the order of tens of milliseconds.

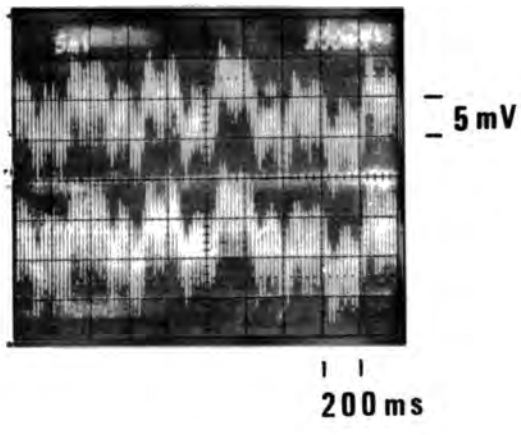


FIG.5.8. RANDOM NOISE

The r.m.s. noise on the signal level is measured in this way to be 2.2mV. This corresponds to a noise of about 2000 carriers r.m.s. This is for a pair of diodes, and the noise on a single diode should be $2000/\sqrt{2}$, $\approx$ 1400 carriers r.m.s.

An estimate of the effectiveness of double sampling can be obtained by calculating the r.m.s. variation in the differences between the signal and the reset levels. In this case the r.m.s. noise is reduced to about 0.5 mV or about 440 carriers for the diode paired operation. This yields an estimate of about 310 carriers r.m.s. for a single diode, double sampled.

These figures must be treated with some caution, especially in the way in which the results from a diode pair are extrapolated to the single diode case. They do however serve to demonstrate the use of double sampling in reducing correlated noise.

For comparison, random noise figures observed by other workers for Reticon devices are shown below[8] :-

Geary	4700	detected photons
Campbell	3800	detected photons
Livingston et al	950	detected photons
Vogt et al	750	detected photons
Walker et al	1100-3600	detected photons
Smithson	7000	detected photons
Dravins	2000	detected photons

Many of these quoted noise figures include noise generated in the external electronics and do not always represent true potential device performance.

5.7. Linearity and Lag

The linearity of a detector is of prime importance in high accuracy spectrographic work. Techniques do exist to remove non-linearities, and these are applied to data obtained from photographic plates. However, the strength of the diode array such as the Reticon has been in its unquestioned linearity, and no measurable deviation from linearity has been reported for a recharge sampling array. Similarly, diode arrays have always been put forward as devices that are free from image retention or lag.

In the case of an integrating detector, there are two rather different aspects of linearity to be investigated. The first is the behaviour of the output signal when the light intensity is constant, and the integration period is varied. Secondly is the case where the integration period remains constant and the light intensity is varied.

The initial laboratory measurements on linearity have been described in an Internal Report[6] and will not be repeated here in detail. Some important aspects will be described which have a bearing on later sections of this work.

A problem became apparent when investigating the output signal as a function of integration time for a steady light intensity. The array was being operated with the Stand Alone Controller and the Programmable Divider described in Chapter Four. The frame time was approximately 11mS, and with the weak illumination used, the single frame integration period produces only a very small, insignificant output. Then, after the "START" button is pressed, the selected integration period was repeated indefinitely. The problem noted was that the readout following the first integration was not identical to the readout after the second and so on. This occurred

for light levels that cause a discharge of about 100mV s^{-1} per diode pair, but was not noticeable at higher light levels. The typical behaviour of the video levels of a diode pair is shown in Figure 5.9. Readout 0 is the state of the video waveform before beginning the integration, after the array has been recharged repeatedly.

Readout 1 is the video waveform at the end of the first integration period. The array, having been recharged once during this readout frame is allowed to integrate for another, identical period.

Readout 2 is the video from the readout at the end of this second integration period, and similarly Readout 3 is the video from the readout at the end of the third integration period. Subsequent readouts are similar to Readout 3, that is, the video levels seem to have stabilised. Several points arise from this :-

(a) The recharge levels are not constant.

(b) If the signal is derived by double sampling, that is subtracting the signal level from the recharge level, then the first measurement of the integrated signal (V_B in Figure 5.9.) is an underestimate of the final, equilibrium integrated signal as measured by double sampling in Readouts 3 and later,(V_C). This (V_C) appears to be a good estimate of the integrated signal, as it is usually equal to V_A, the amount by which the "signal" video dropped between Readout 0 and Readout 1. This (V_A) is the signal that would be measured by a non-destructive readout.

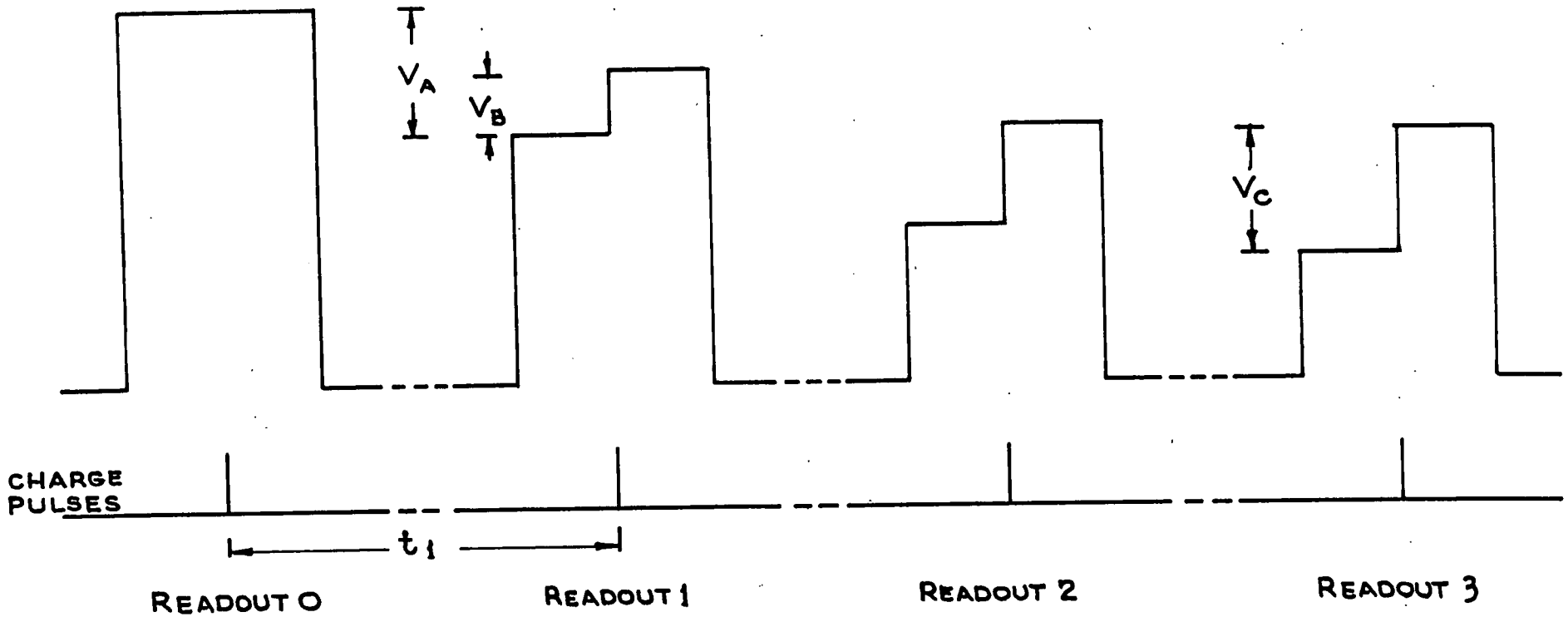


FIG 5.9 TYPICAL OBSERVED VIDEO WAVEFORMS FOR SUCCESSIVE INTEGRATIONS

(c) This behaviour cannot be explained by "lag" in the traditional sense. There has been no step change in the illumination level.

The effect of this underestimation of signal on the linearity of the detector can be seen in Figure 5.10., which shows the initial (V_B) and final (V_C) estimates of the integrated signal plotted as a function of integration time. The plot of the final estimates displays the good linearity hoped for.

The implications of this are disturbing. It appears that the correct value is only obtained after a number of identical integration frames. For long integration times this is an impractical way of arriving at the correct value. Alternatively, the first "signal" video level can be compared with the preceeding "recharge" video level. This destroys the advantages of double sampling, and can only be used when recharging with "paired" charge pulses (i.e. poorer spatial resolution).

The situation becomes even worse at lower light levels. More readouts are required before a stable situation is reached, and also the "non-destructive" signal estimate (V_A) is no longer equal to the equilibrium value (V_C).

Other problems of this type have been described in detail in the Internal Report[6)], and are still under investigation at the time of writing. The sources of the problem appear to be slow charge transfer through the amplifying transistor, and incomplete recharge.

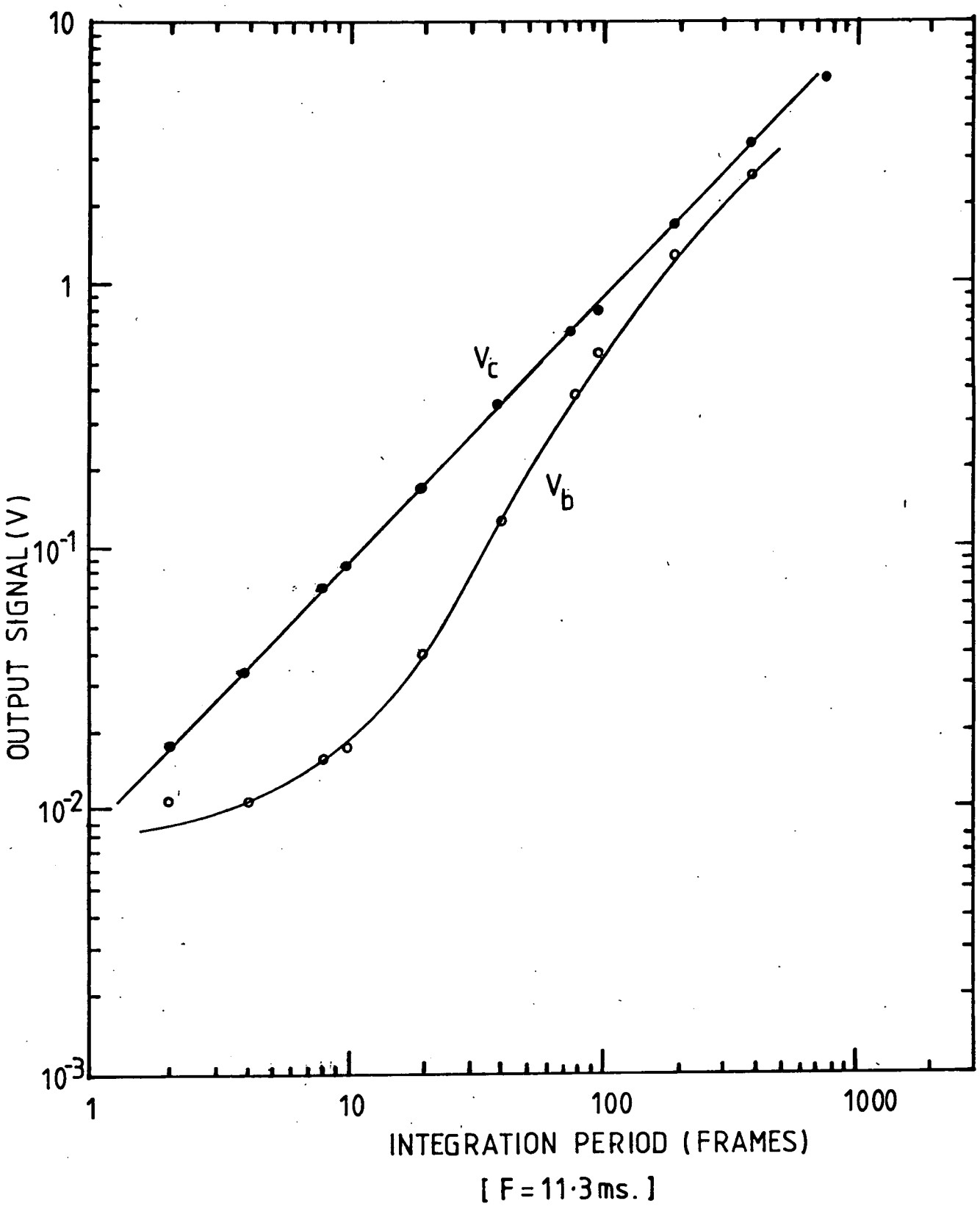


FIG.5.10. LINEARITY MEASUREMENTS

Linearity of the array when operated with a constant integration time and variable light input has also been shown in the Internal Report, although this linearity is conditional on the readout chosen for plotting as for the measurements above.

5.8. Impulse Response

In the hope of clarifying some of the problems of threshold, lag and non-linearity encountered in previous measurements, an attempt was made to observe the detection and integration process on a single element as it was exposed to a pulse of light. Previous tests had all been done under steady state illumination conditions. Unfortunately, the design of the array does not allow direct access to a single element, because the shift registers are dynamic and cannot be halted to display the selected element. The following scheme was devised to simulate such a situation.

The readout sequence and pulse timing is shown in Figure 5.11. The integration Control Module is used under program control to define this sequence.

The frame time is 4 seconds (the array is cooled with liquid nitrogen). The charge pulse lines are held high for five frame times to ensure complete recharging. The charge pulses are then enabled for the next frame. Simultaneously, a spare output from the Integration Control Module is used to trigger a LED (light emitting diode) via two adjustable monostables (pulse delay and pulse width). This LED pulse is adjusted by the pulse delay monostable to "fire" during the first signal level of the video waveform of the element under investigation. In Figure 5.11 this is shown as the second video waveform (i.e. diode pair 3, 4).

The long frame time was chosen to enable LED pulses in the region of 1ms wide to be used. The LED illuminates the array and produces a characterstic slope on the waveform due to the integrating nature of the array.

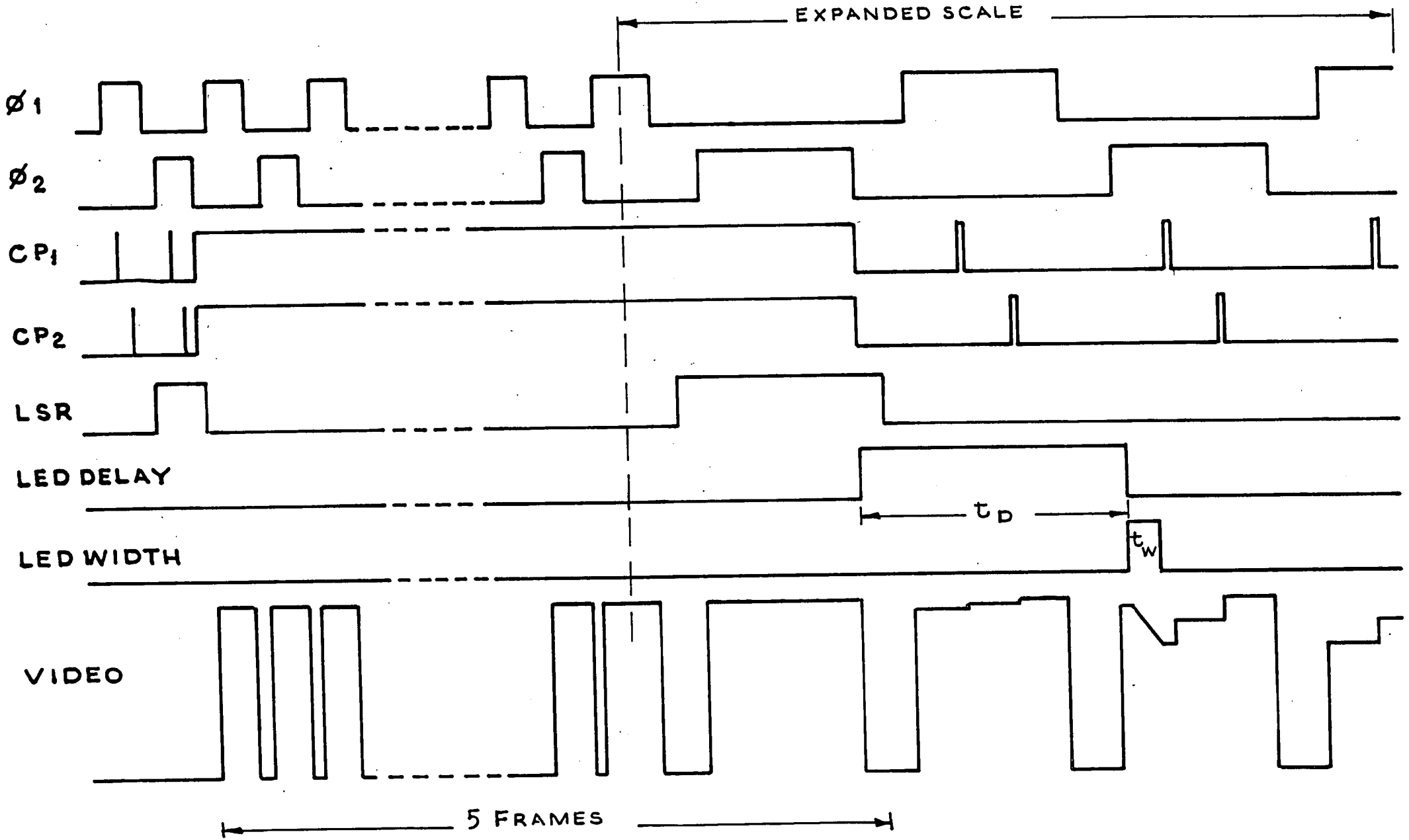


FIG 5.11 PULSE TIMING SCHEME FOR OBSERVATION OF IMPULSE RESPONSE

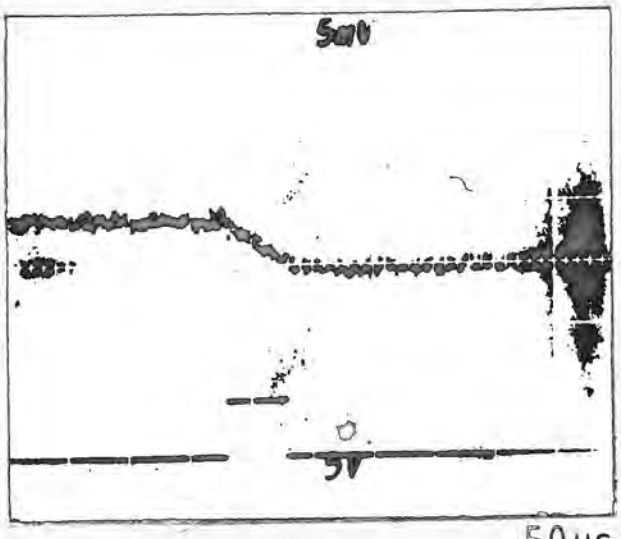
The video waveform is displayed on a storage oscilloscope, triggered via a delayed timebase by the Integration Control Module. Figure 5.12 shows a set of six traces obtained with LED pulse widths of 50 μs to 5 ms, and a constant LED voltage. The upper trace in each photograph is the video level, and the lower trace is the timing of the LED pulse (the height of the lower waveform is not representative of the magnitude of the LED voltage however).

These photographs all show a linear decay of signal during the flash, and show the element as a perfect integrator. The decay rate in all these is approximately 78 Vs^{-1}.

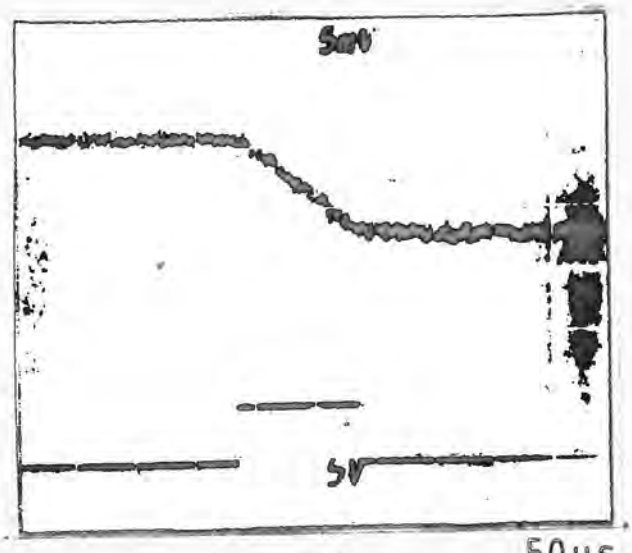
The second series of photographs, shown in Figure 5.13., was obtained with a larger voltage on the LED and consequently a higher light intensity. The decay rate is approximately 480 Vs^{-1}. The decays displayed in this sequence are obviously non-linear, and as the exposure time is increased, the voltage change under-estimates the actual integrated light intensity.

The magnitudes of the signals involved in this sequence are very similar to those shown in Figure 5.12. (d, e and f), so this does not appear to be a saturation effect, but rather an inability to transfer at a high rate of discharge.

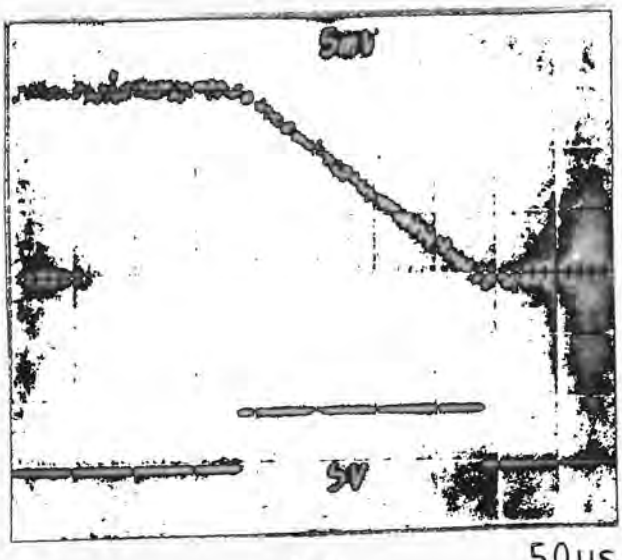
Also, the exposure times involved in this sequence are similar to those in Figure 5.12 (a, b and c), so it does not appear to be a simple problem of a time constant in the output circuit.



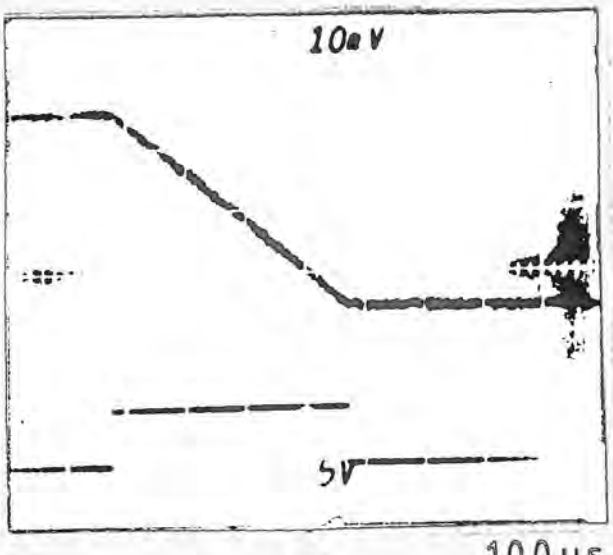
(a)



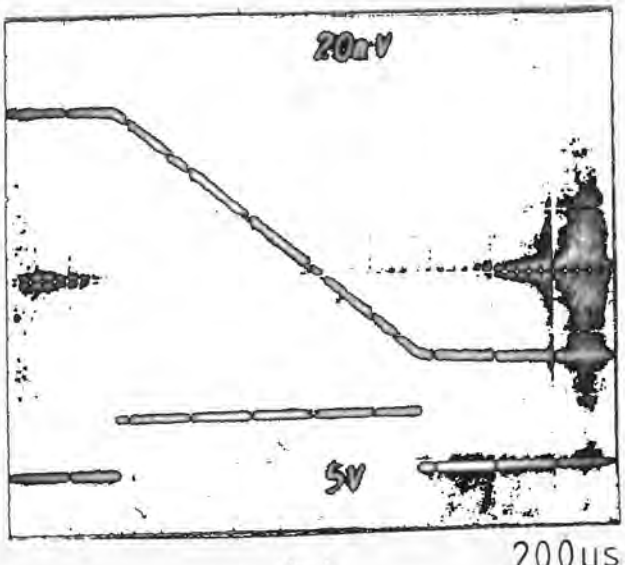
(b)



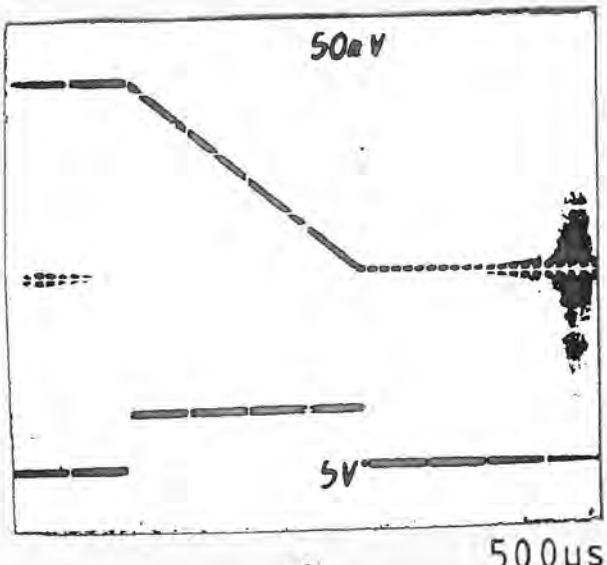
(c)



(d)

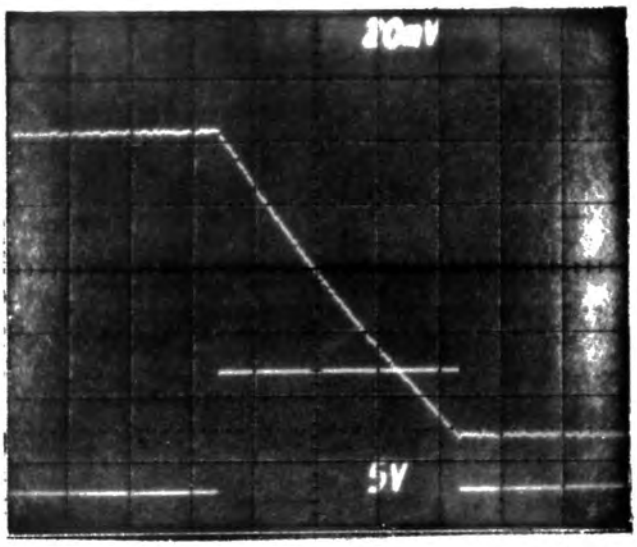


(e)

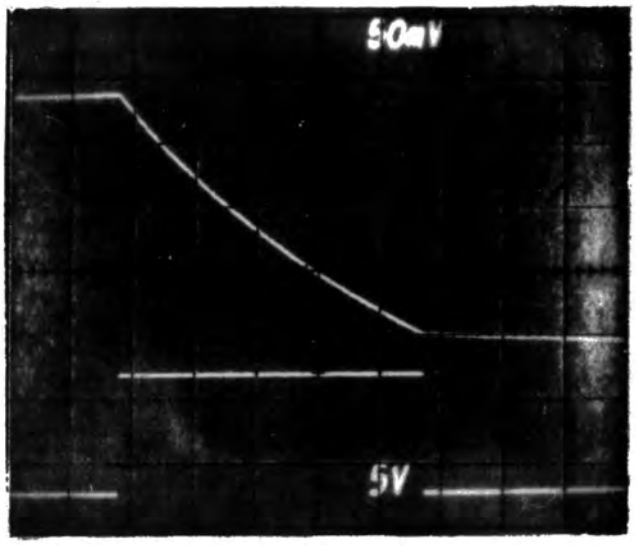


(f)

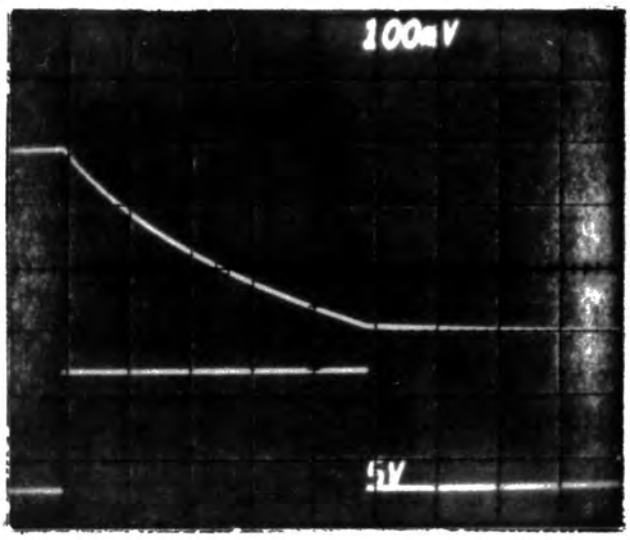
FIG. 5.12 IMPULSE RESPONSE - 1



(a) 50μs



(b) 100μs



(c) 200μs

FIG. 5.13. IMPULSE RESPONSE - 2

A further point of interest is the behaviour after the end of the LED flash in the photographs of Figure 5.13. The video level seems to continue to discharge after the end of the LED flash.

The rather limited evidence so far seems to suggest that at high light levels, signal transfer from the diode to the storage capacitance is slower than the signal generation in the diode, and consequently, even after the end of the light impulse, some signal is still being transferred.

Unfortunately, the use of a storage scope in this application is far from ideal, and the sequences of photographs shown in Figure 5.12. and 5.13. took a good many days to obtain. A fast transient recorder is more suitable for this type of investigation, and such an instrument has since been obtained by the group. Furthermore it would be instructive to have a fast (non-integrating) photodetector mounted alongside the array in order to observe the actual shape of the LED output pulse.

This type of experiment could, if properly instrumented, be very valuable in investigating the properties of the array element, as it gives us a insight into the integration process taking place. It also demonstrates the versatility of the computer control system for conducting experiments that would otherwise not be possible.

5.9. Summary

Some initial measurements on the characteristics of the Plessey arrays have been carried out. The photoresponse of the array has been shown to agree with the figure predicted from the device parameters. Similarly, the spectral response behaves as expected and demonstrates the reduction in red-end sensitivity at low temperature that was predicted in Chapter 2. Thermal leakage current can be reduced to insignificant levels by cooling the array, and the behaviour of the leakage current with temperature agrees roughly with the observations of other workers using Reticon devices. Tighter control of array temperature is needed before repeatable measurements on thermal leakage characteristics can be made, but some sort of threshold effect is apparent.

The random noise has been measured crudely as about 1400 carriers, for a non-destructive readout, reducing to about 310 carriers for a double sampled read. These figures compare favorably with those obtained by other workers using Reticon devices.

When attempting to measure linearity, a number of problems have arisen. These seem to be related to slow charge transfer from the diode to the integrating capacitance and to incomplete recharge by the charge pulses. Attempts have been made to identify these problems by investigating the impulse response of an array element. Initial results are encouraging, and further investigations into the sources of non-linearity and lag are continuing.

Some further points regarding the above characteristics arose during the observational trials at the R.G.O. 30 inch telescope. These will be discussed in the following Chapter.

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6) G.R. Hopkinson, A.W. Campbell, A.R. Hedge and A. Humrich, Durham University Internal Report NI - 78 - 5, 1978.

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CHAPTER SIX

Operation of a Plessey Array at the 30 inch Telescope of the R.G.O.

By the end of July 1978, the control and acquisition system described in Chapter 4 was sufficiently near completion to begin tests of the array on a telescope spectrograph. While the author and A.W. Campbell[1] had been developing the electronics systems, A. Humrich[2] had been designing the mechanical and cryogenic systems required to mount the array. The experiment was transported to and set up at the 30 inch telescope at the R.G.O. during the last days of July, and was operated there throughout August.

This Chapter describes the experimental set up, the operational software developed for the acquisition and display of stellar spectra, some of the problems encountered during operation, and presents some of the initial results which are of interest from the systems and device aspect. A detailed description of the observing programme, the analysis techniques used and the astronomical results obtained will be presented by A. Humrich[2].

6.1. The Instrument

There are three distinct parts to the observing instrument, these being the telescope, the spectrograph and the diode array mounting. These will be discussed briefly in turn. Detailed descriptions will be given by A. Humrich[2].

6.1.1. The Telescope

The 30 inch telescope began its operational life as part of the Thompson equatorial telescope group installed prior to the turn of the century at the Greenwich site. The Thompson group also contained the 26 inch refractor.

When moved to the Herstmonceaux site after the war, these two telescopes were separated and the 30 inch reflector was installed on a new mount in "A" dome, its current location.

After some initial work on photoelectric photometry, a coudé focus spectrograph was proposed. Such a permanent spectrograph would be much more stable than a demountable Cassegrain focus instrument, and would provide an easily accessible test-bed for new instruments such as image tube systems.

The conventional approach to the provision of a coudé focus is shown in Figure 6.1. The light is reflected down the polar axis of the mount via a plane mirror on the declination axis. Such a configuration was not possible on the 30 inch telescope due to mechanical constraints and instead the light is reflected up the polar axis, and then down onto the spectrograph slit. The layout of the 30 inch telescope and the coudé focus is shown in Figure 6.2.

6.1.2. The Coudé Spectrograph

A coudé spectrograph is a very useful tool for high dispersion spectroscopy. The physical size of a high dispersion instrument prohibits its use at most Cassegrain focus positions. Similarly, the mounting of a detector at a Cassegrain focus imposes weight, access and mechanical constraints on the mounting system.

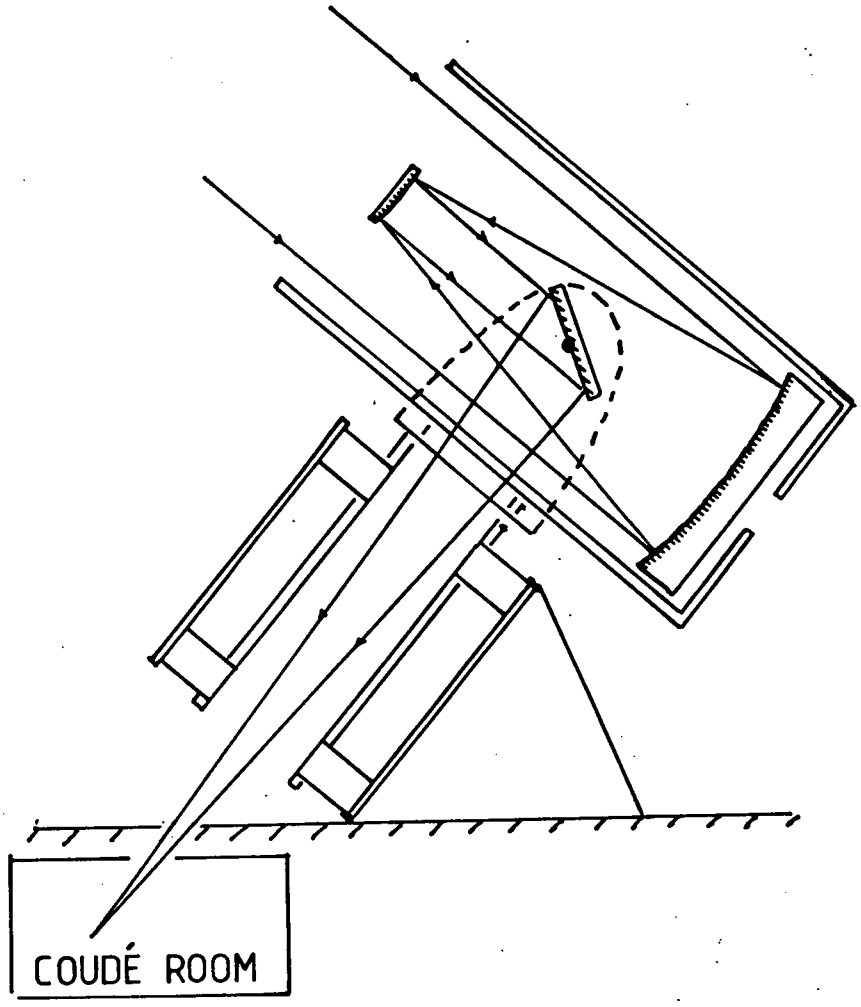


FIG.6.1. CONVENTIONAL COUDÉ FOCUS ARRANGEMENT

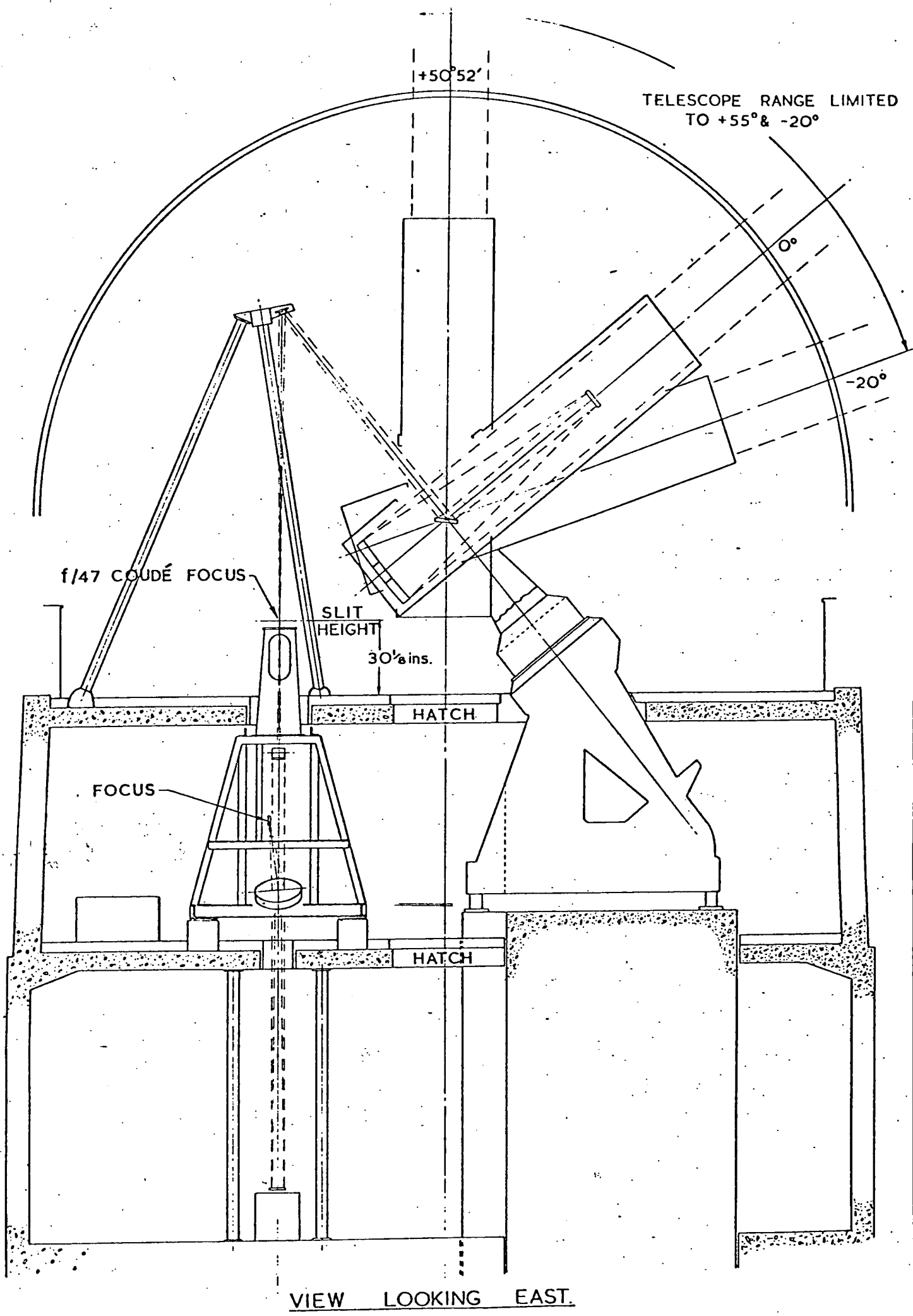


FIG.6.2. THE RGO 30inch TELESCOPE

The coudé spectrograph at the 30 inch reflector is arranged with the dispersion in a vertical axis at the final focus. The grating is ruled at 830 lines/mm to give first and second order dispersions of 10 and 5 Å/mm respectively. This translates for the Plessey array to, for first order, a resolution of 0.45 Å/diode and a range of 115 Å, and for second order a resolution of 0.225 Å/diode and a range of 58 Å..

Two rails are available, set in concrete, for the mounting of detectors.

6.1.3. Diode Array Mounting and Cooling

The mechanical mount for the diode array permits movement of the array horizontally and vertically, and also allows for rotation of the array. These three adjustments are by micrometer. The entire mounting trolley can slide backwards and forwards on the rails in the spectrograph.

The array mount incorporates a cold finger cryostat and a liquid nitrogen dewar. The cryogenic system has been described in an Internal Report by A. Humrich[3)].

6.2. Observational Software

With the control hardware developed and constructed, and the mechanical mount for the array complete, it remained to develop a suitable integration scheme and a suite of programs to implement and support it. In the following sections, a complete exposure, starting with initialisation by the user and ending with return of control to the user will be referred to as a run.

6.2.1. Integration Scheme

In order to ensure that prior to an integration, recharging is as complete as possible, the starting sequence of a run is a number of frames (typically 25) during which the recharge pulses are enabled. Referring to Chapter 4, Table 4.1., this requires a Mask word of 3. The last of these frames is digitised and stored (Mask 7), and this readout will be used later to subtract fixed pattern noise from a non-destructive readout. For this reason, this readout is named FPN1.

The integration period now begins. It will be seen from Table 4.1. that two conditions are available to achieve integration. As long as the charge pulses and memory load pulses are both disabled, the LSR pulse can be either enabled (Mask 1) or disabled (Mask 0). The LSR pulse decides whether or not a bit is to be loaded into the shift register. It has been suggested by other workers[4] using Reticon arrays that the temperature of an array can change significantly between when it is clocked and when it is not, due to the power dissipation in the register. In theory, the power dissipation in the shift register of the Plessey array is due solely to the capacitance of the clock lines and is independent of the state of the "data" in the register. Even so, it was felt that it would be advisable to avoid any changes in the register clocking during an exposure, so the LSR pulse is kept enabled throughout integration frames.

The integration period is selected by the user at the start of a run. At any time during the integration period the user can request a non-destructive read or a run termination by means of the front panel buttons on the Integration Control Module.

When a request for a non-destructive read is identified, the memory load pulses are enabled for one frame (Mask 5), and the digitised video loaded into memory. The memory contents are then transferred to the computer. The raw data from the non-destructive read is rather meaningless to the operator because of the fixed pattern offset noise superimposed on it. The reset values from FPN1 are subtracted from this data, resulting in a 256 point spectrum in which only 128 points are independent. This is because of the diode pairing in the NDRO data. Following this subtraction, the raw data and the "subtracted" spectrum are displayed to the user simultaneously on a split screen. When the display has been written the NDRO request button is re-enabled. A second NDRO overwrites the computer memory space reserved for the first. Thus the computer memory allocated to NDRO always refers to the most recent non-destructive read.

At the end of the requested integration period, or when the user requests a run termination, a double sample read frame (DSRO) is effected by enabling the charge pulse and memory load commands (Mask 7).

The DSRO is then transferred, "subtracted" (using its own reset levels) and displayed as for the NDRO. Meanwhile, for the next 50 frames following the DSRO, the charge pulses remain enabled. Then a second DSRO frame is taken, and this is known as FPN2. This is used to monitor drifts in amplifier gain and offset, since in the absence of these it will be identical to FPN1.

During the run, the user's VDU screen displays the current frame number and the frame number of the last non-destructive readout. Audible signals are generated by the VDU to signal the start and end of the integration. At the end of the run, control is returned to the user's VDU.

6.2.2. Display, Inspection and Dumping of Spectra

At the end of the run, the user has the facility to view on the storage display any of the four recorded "spectra" (FPN1, NDRO, DSRO, and FPN2), to display " subtracted" spectra, to obtain VDU or hard copy listings of raw or subtracted data, or to obtain a dump of the data on punched paper tape. At any time, the user can escape from these inspection routines to begin a new run. The dumped data can be obtained in long or short format. In both formats, a 20 word run header is punched following an "all-ones" start of dump character (2^{16}-1). The run header contains data relating to the run, such as run number, integration time etc. The long format dump follows the header with the 2048 data words describing the raw data (512 each for FPN1, NDRO, DSRO and FPN2). Each word requires 2 (8 bit) punched characters and the dump is thus 4138 characters long - some 35 feet of paper tape in all. The short format dump follows the 20 word header with only 256 words describing the "subtracted" double sample readout.

The CATY program written to perform the above on-line functions is listed and briefly described in Appendix D. Figure 6.3. is a simplified flow diagram of this program.

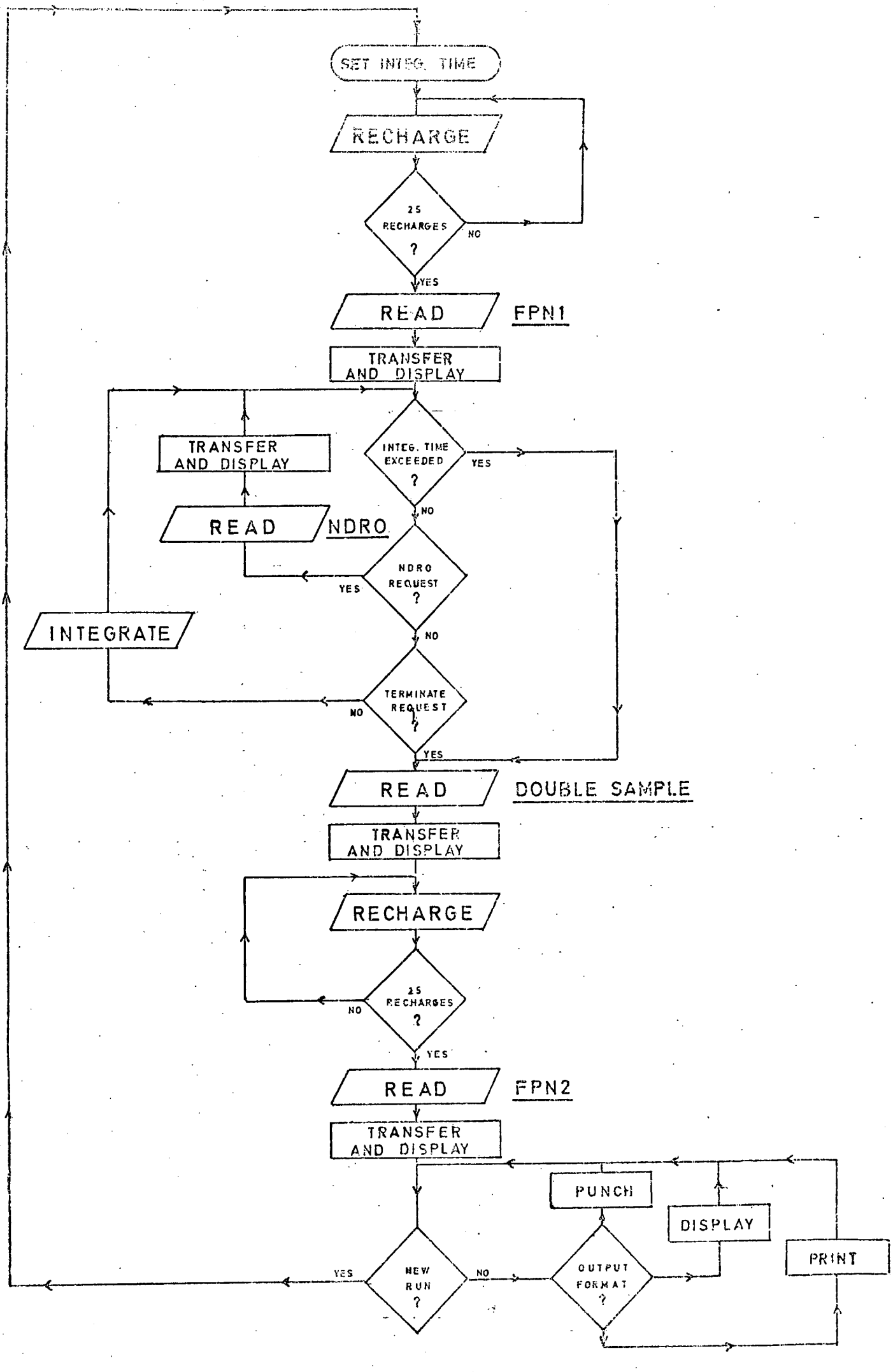


FIG.6.3. CONTROL PROGRAM

6.2.3. Additional User Programs

Further programs have been developed in CATY for execution on the PDP 11/03 to assist the user. The most interesting of these is the spectrum division program, which divides the subtracted DSRO spectrum by a subtracted DSRO spectrum from a tungsten calibration exposure.

As has been described, the raw DSRO data has had removed from it the fixed pattern offset noise by subtraction of the second video level from the first, and the reset level from the second video level, for each diode pair. The fixed pattern responsivity noise is however still present in this "subtracted" spectrum.

This can only be removed by a knowledge of the individual diode responsivities at the particular wavelength imaged by each diode. The most practical method is to image the spectrum of a black body radiator onto the array, and to divide the "subtracted" stellar spectrum by the the "subtracted" black body spectrum. In this way diode-to-diode variations in responsivity are removed, as are some types of imperfection in the spectrograph. The "folding in" of the black body spectrum must be taken into account when analysing the resultant spectrum. A reasonable approximation to a black body source is a domestic tungsten light bulb, and such a bulb is installed in the spectrograph for this purpose.

In use, after the stellar exposure has been made, and a short dump obtained of the subtracted spectrum, a short exposure is made on the tungsten spectrum and a short dump produced. The off-line Division program is then used to divide the two dumped spectra and display the result. A scale factor can be applied to the division to produce the resultant spectrum in useful units.

Operationally it would be of more value to the user if such a tungsten division routine could be incorporated into the online data acquisition program. At the time, insufficient memory was available in the PDP 11 to implement such a program. In fact, the on-line program as listed in Appendix D will not execute in 16K words, and many of the remark (REM) statements included there to make the listing more readable have to be deleted.

Other programs available include the Long Dump Analysis which is essentially the latter part of the acquisition program with the addition of the necessary read routines to input the data tape. Also available are routines to convert the binary output tape into ASCII coded formats acceptable to other computer installations.

6.2.4. Data Analysis

The mathematical abilities of the CATY language are severely limited and for this reason only very crude data reductionss are attempted on the PDP-11. More sophisticated analysis is left to machines capable of running FORTRAN. At the time of writing, the hardware configuration of the PDP 11/03, as described in Chapter Four, will not support FORTRAN, although a compiler is available.

FORTRAN routines have been written to input data tapes into the NUMAC (Northumbrian Universities Multiple Access Computer) facility at Durham. Routines have also been written to input the data tapes into the ICL 1905 computer at the RGO although these had not been fully proved before the end of the observing run at the Observatory.

The analysis techniques used to further "clean-up" the spectra are to be described in detail by A. Humrich[2)].

6.3. Performance of the Plessey Array under Observational Conditions

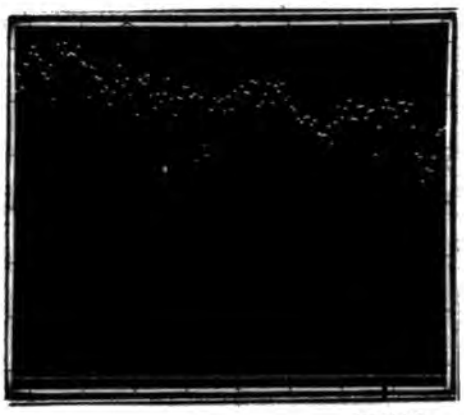
Some problems were encountered when operating the array during the observing programme, some of which had not been encountered previously. These will be described here, but first some specimen data is described, illustrating the operation of the array.

During all observational work, the array was operated with no heater supply, and with liquid nitrogen cooling, so array temperatures were around -120^{o}C. The frame time used was 100mS.

6.3.1. Specimen Data from Observations of Vega

The sequence of readouts and displays obtained during a run was described in Section 6.2. The photographs in Figure 6.4. are from an exposure on Vega in the region of the oxygen lines at 7770Å, Run 196. Figure 6.4. (a) shows the raw data from the FPN1 readout at the start of the integration sequence. The vertical axis is 4096 ADC units (10V) full scale, with the fully charged state towards the top of the screen. The baseline levels can be seen at the bottom of the trace. The presence of considerable offset fixed pattern noise can be seen.

Figure 6.4. (b) shows the raw data from a NDRO frame after an integration of 1811 frames (3 min. 1 sec). Little information can be seen in the data when presented in this way. The general accumulation of signal is evident from the decrease in the video levels, but any features are masked by the offset fixed pattern noise.

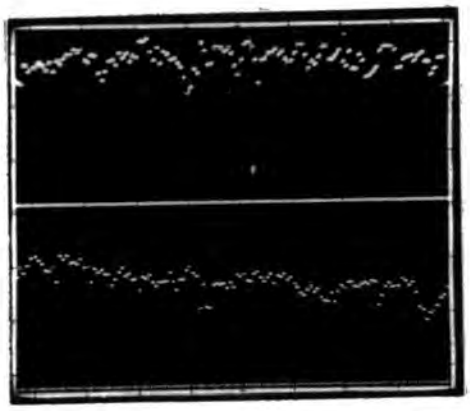


FPN1

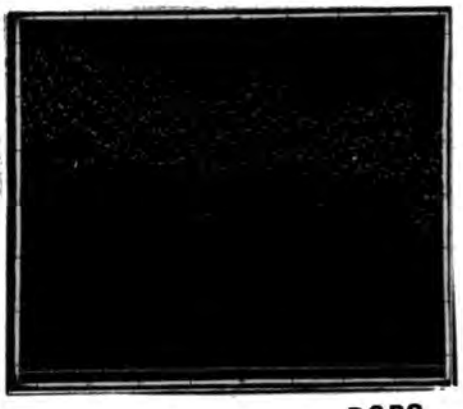
(a)

NDRO

(b)

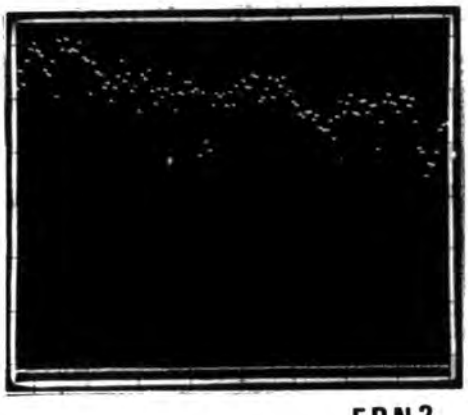


(c)



DSRO

(d)



FPN2

(e)

FIG. 6.4. READOUT SEQUENCE

Figure 6.4. (c) shows the display presented to the user after the NDRO readout. The lower trace is simply a repeat of the raw NDRO data of Figure 6.4. (b). The upper trace shows this data after the subtraction of the FPN1 reset levels. The full scale here is 1024 ADC units (2.5V). The presence of spectral features is evident. In general, the exposure is terminated when the signal level in this upper trace reaches close to full scale in order to ensure the array does not go into the saturation region.

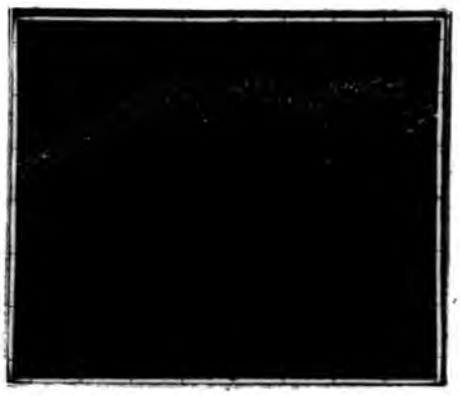
Figure 6.4. (d) displays the raw data from the double sample readout (DSRO) which was requested following the inspection of the NDRO data. The integration period is 1843 frames (3 min 4 sec). The four video levels per diode pair (see Figure 4.4.) are readily visible. Again it is difficult to visually extract any useful information.

Figure 6.4. (e) shows the raw data from FPN2, and this is approximately the same as FPN1.

The data from the DSRO frame has its offset variations removed by subtraction of appropriate levels within this data as described in Chapter 3. The resulting spectrum is illustrated in Figure 6.5. (a), with a full scale of 512 ADC units (1.25V). This data is still very "noisy", although some features can be clearly distinguished, such as the large absorption feature at about 1/3 of the way along the array.

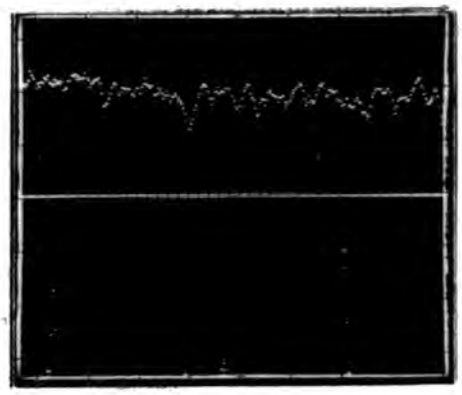
Section 6.2.3. described the removal of responsivity variations by division of the subtracted stellar spectrum with a subtracted tungsten spectrum. Figure 6.5. (b) shows a subtracted spectrum obtained with a 30 frame exposure on the tungsten source, (Run 201). Full scale is again 512 A.D.C. units.

(a)



(b)

(c)



(d)

FIG. 6.5. SPECTRUM REDUCTION and CALIBRATION

Figure 6.5. (c) shows the results of this division. Full scale here is a ratio of 2.048. The data has been considerably improved, especially at the right hand (red) end. The poor quality of the smoothed data at the left end is due to the misalignement of the tungsten spectrum on the array, evident also in Figure 6.5. (b).

The wavelength scale on this spectrum is approximately 0.45Å/diode, or 115Å full scale, with the blue end on the left.

In order to be able to accurately identify the features, a wavelength calibration is required. This can be achieved by an exposure with a neon discharge lamp illuminating the spectrograph slit. Figure 6.5. (d) shows a display of the stellar spectrum of Figure 6.5. (c) in the upper trace, and a neon spectrum on the lower trace. A detailed description of the use of neon spectra for the identification of stellar spectral features is to be given by A. Humrich[2].

Some idea of the "collecting rate" of the system as a whole can be deduced from above data. The spectrum of Figure 6.5. (a) was obtained with an integration time of 3 min 4 sec, and the mean signal level in the continuum is about 330 ADC units or 0.8V. The magnitude of Vega is 0.03 Thus for Vega (m = 0.03) the collecting rate is approximately 1.79 ADC units/sec. In general, for a star of magnitude m, the collecting rate is given by :-

$$1.79\ (2.512^{-(m - 0.03)})$$

$$= \quad 1.83\ (2.512^{-m})\ \text{ADC units/sec}$$

$$\text{or} \quad 4.46\ (2.512^{-m})\ \text{mV/sec}$$

6.3.2. Fixed Pattern Noise

The data described above can be used for performing a statistical analysis of fixed pattern noise, an exercise that would be extremely lengthy and laborious without the computerised acquisition system.

a) Fixed Pattern Offset Noise

An analysis has been made of the distribution of reset levels in the FPN1 data of Run 196 (Figure 6.4. (a)). Figure 6.6. shows this distribution of reset levels.

The range of reset levels encountered is 1594 ADC units, compared with the full output swing of the array (from the highest reset level to the baseline) of 3775 ADC units.

The magnitude of the offset fixed pattern noise places considerable limitations on the digitisation step size. For example, in the exposure of Run 196 described above, the average signal level in the continuum was 330 ADC units. Thus the "resolution" of signal level is only 1 in 330 despite the use of a 12 bit ADC. This arises because we choose here to digitise the baseline level also. Consider the situation if we were not to digitise the baseline. The signal could be amplified further before input to the ADC, but only to point where the range of offsets matches the input range of the ADC. The average signal would then be around 850 ADC units. Thus the resolution of the digitising system is being greatly degraded by the need to accommodate the range of offsets present in the video waveform.

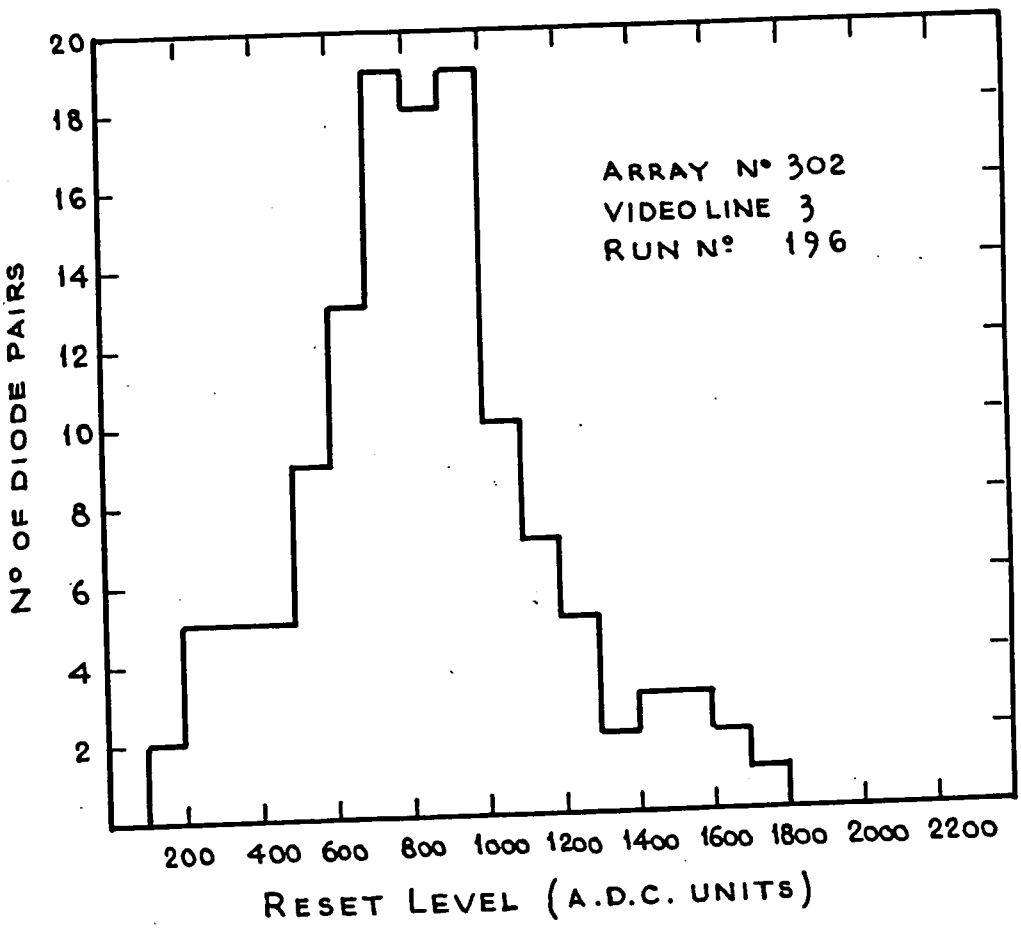


FIG 6.6. FIXED PATTERN OFFSET DISTRIBUTION

Various schemes have been suggested for removing some of the fixed pattern offset prior to digitisation. All such systems involve the use of a differential amplifier, with one input signal representing the offset. This offset can be obtained in real time by delaying the video and feeding back the appropriate levels, or can be synthesised from previously stored digital data via a D to A convertor. Figure 6.7. presents a sketch of a system of the latter type. The merits and limitations of various schemes are currently being investigated.

b) Fixed Pattern Responsivity Noise

In order to measure variations in responsivity, ideally a perfectly uniform illumination over the length of the array is required. Such an exposure proved very difficult to obtain, and instead the tungsten exposure from Run 201 (Figure 6.5. (b)) has been used. Before the responsivity distribution can be measured, the variation in illumination along the array must be "removed". In order to do this, it was assumed that the illumination would be a smooth function, and a third order polynominal fit was made to the data. This function was then assumed as unity responsivity, and the deviations from this were computed. The distribution obtained is shown in Figure 6.8. The standard deviation of the responsivity is calculated as $\sigma = 4.9\%$.

This will inevitably include some deviation caused by the error in assuming the illumination function to fit the third order polynominal, but serves as a useful preliminary indication of the level of responsivity noise.

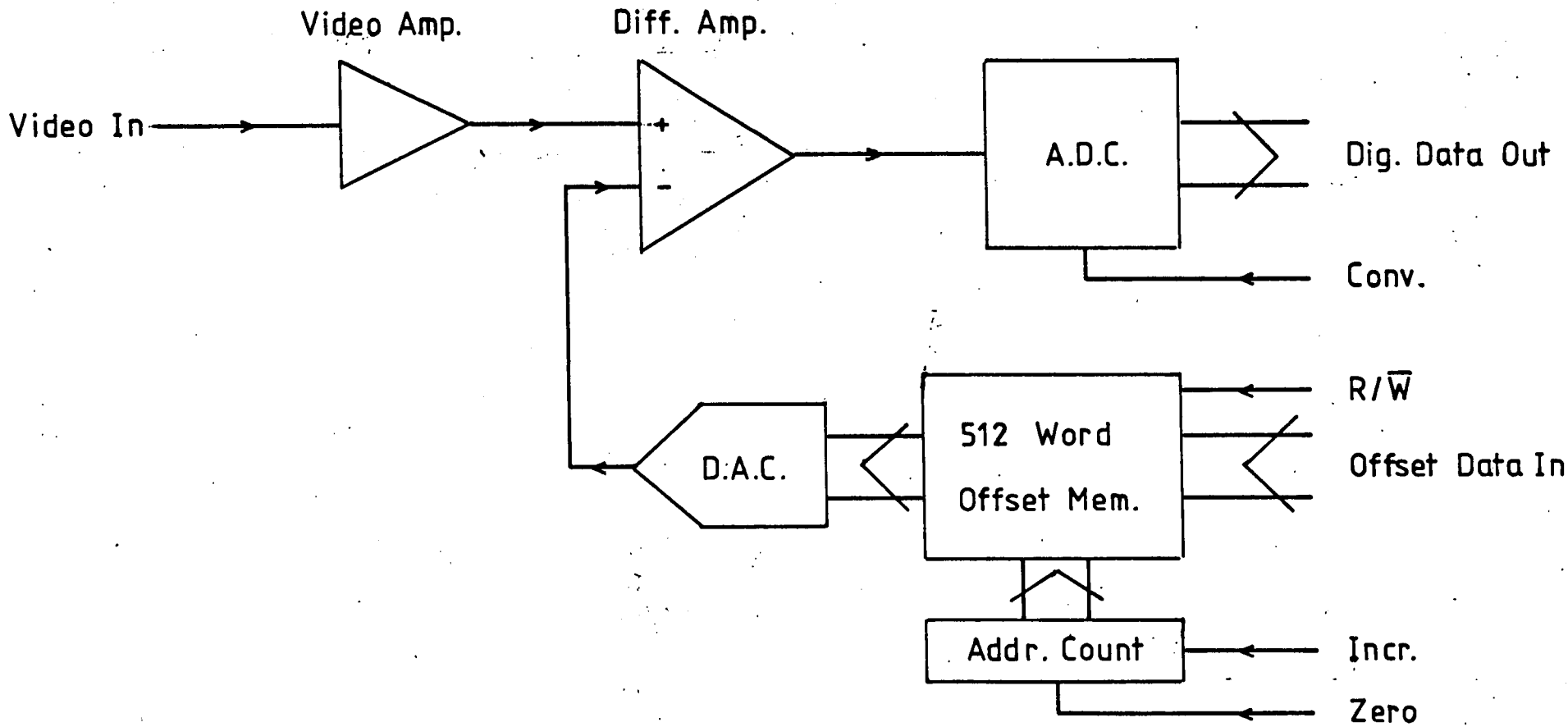


FIG.6.7. OUTLINE OF AN OFFSET FEEDBACK SYSTEM.

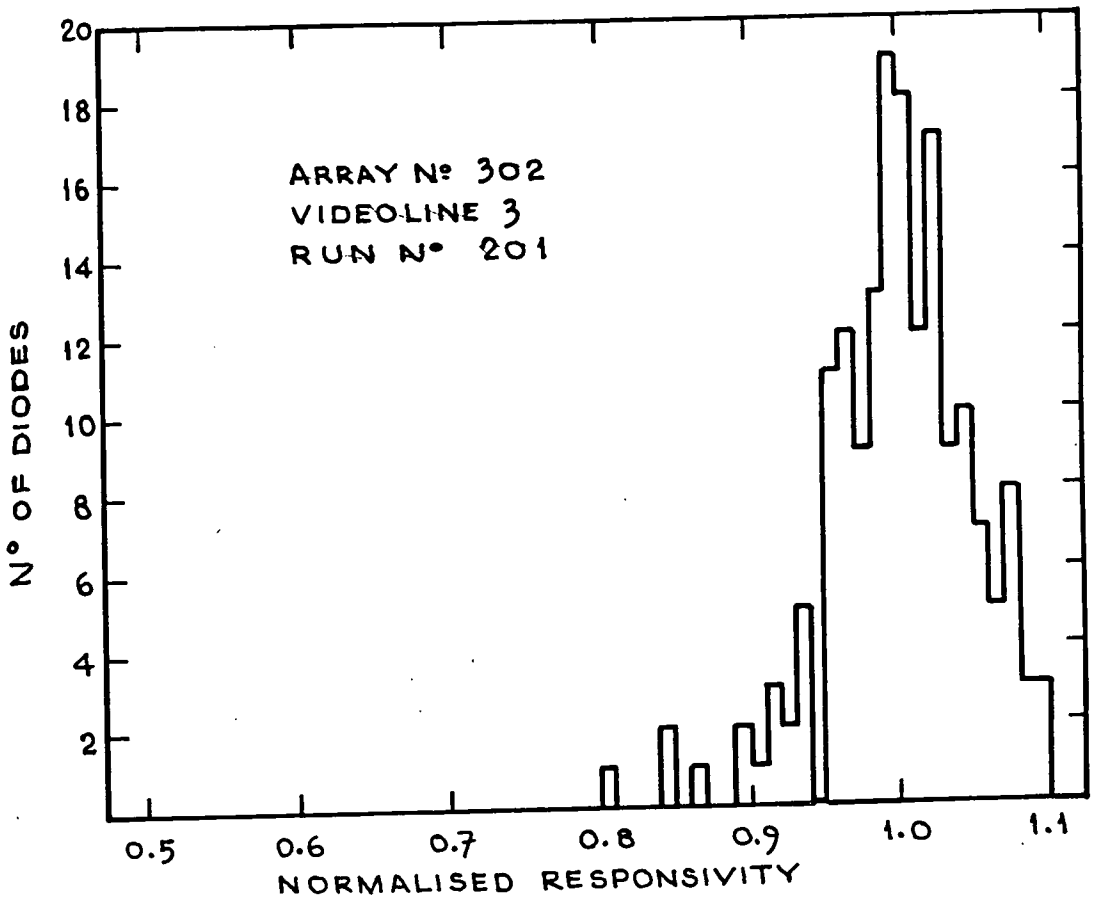


FIG 6.8. FIXED PATTERN RESPONSIVITY VARIATION

6.3.3. Random Noise

The digitisation step size throughout the work at the RGO was approximately 2.5mV. From the estimated 1.6μV/carrier of Chapter 5, this step represents a "quantisation noise" of some 1500 carriers, which we would expect to mask the random noise. Thus we expected the following experiment to show us that the only observable noise was due to the quantisation step size.

In order to measure the random noise, the plan was to make a large number of identical exposures in succession, in the dark. The random noise could then be computed from the distribution of a particular level from exposure to exposure, and the double sampled noise computed from the distribution of the difference between an appropriate pair of levels.

Attempts to measure the distribution of a given level over several exposures were largely unsuccessful. As expected, the difference between levels (double sample noise) from exposure to exposure did not show more than 1 ADC unit variation either side of the mean. The levels themselves however, in the exposures for which we took the data, exhibited a slow rise from exposure to exposure with time. Some typical data exhibiting this effect is shown in Figure 6.9.

This effect will be described in the next section, which includes other seemingly related problems.

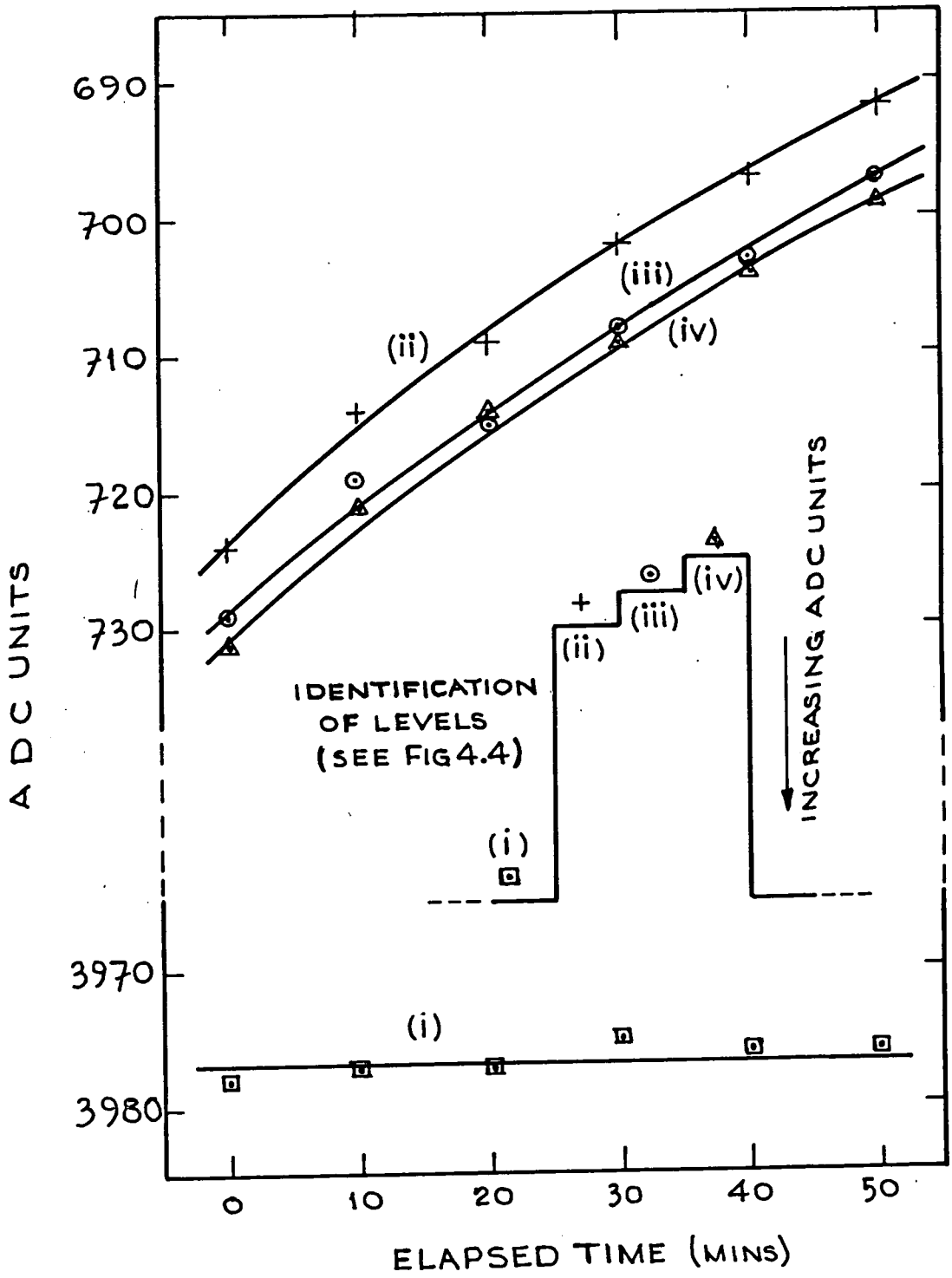


FIG 6.9. INCREASE OF VIDEO LEVELS WITH TIME IN THE DARK.

6.3.4. Lag Problems

It was noted in Chapter 5 that there were apparent problems with image lag, probably due to a combination of incomplete recharge and inefficient transfer. The behaviour as shown in Figure 6.9. seems to be further evidence of similar problems. The data of Figure 6.9. was gathered over a timespan of roughly one hour. Prior to the exposures, the spectrograph had been opened in order to fill the liquid nitrogen dewar, and so the array had been exposed to light.

Some interesting points arise :

(a) The baseline levels are stable, and so gain or offset drifts in the external electronics can be ruled out.

(b) The first video level of a diode pair is higher (more charged) than the second, and the second is higher than the third (reset) level. This is in fact a commonly observed phenomenon at low temperatures and very low light levels. A possible explanation for this is charge pumping.

(c) The differences between levels do not change with time, although the levels themselves increase, as if there is some slow change in some internal parameter leading to a drift in output level following exposure to light.

The feasibility of charge pumping as a candidate for the effect as described in (b) above can be tested by inserting some typical values. As the gate of the recharge transistor is pulsed, charge will be injected into the substrate, tending to reduce the charge on the gate capacitance of the source follower transistor. Assuming, as in Chapter 2, a pumped charge of 10^{-2} pC, and a gate capacitance of say 0.1 pC, this would lead to a step in the region of 100mV, compared to the 25mV or so observed. Thus charge pumping could produce

an effect of the correct order of magnitude. If it is responsible however, it remains to be seen why, as can be clearly seen from Figure 6.9., the second step (as the second diode is recharged) is smaller than the first step (as the first diode is recharged). This is perhaps peculiar to this particular video line (Array Number 302, Video Line 3), but this has yet to be investigated.

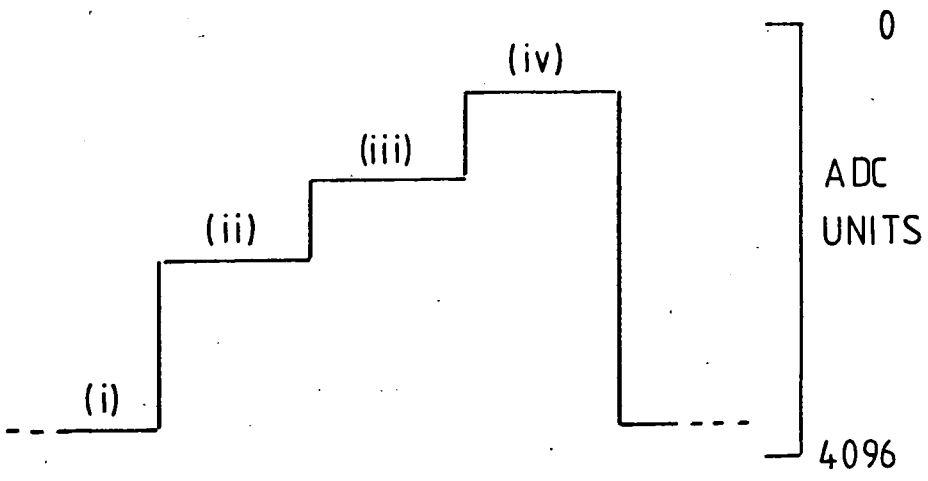
A further problem became apparent when investigating the behaviour of the array during the exposure on Vega described earlier (Run 196). Figure 6.10 shows a printout for Run 196 which lists the video levels for the first five diode pairs for FPN1 (Block 0), DSRO (Block 2) and FPN2 (Block 3). The first video level is the baseline, the second the signal on both diodes of a pair, the third the signal on the second diode only and the fourth the recharge level.

The situation is shown graphically in Figure 6.11., for the first diode pair.

In the DSRO readout, the recharge level has dropped significantly, by about 150 ADC units, compared to a "signal" level of about 300 ADC units. The FPN2 readout is made 50 recharge frames later. The recharge level is now higher, but still some 30 ADC units lower than it was in FPN1. This, combined with the behaviour noticed in Chapter 5 (Figure 5.9.) casts considerable doubt over the validity of the double sampling process.

6.3.5. Reciprocity Failure

Suspicions were aroused about a possible non-reciprocity effect when it was noticed that during observational runs on faint objects, no strong features had been detected. The following observations were made in an attempt to demonstrate such a reciprocity failure.



RUN NUMBER 196

INTEGRATION PERIOD 100000
NO. OF INTEGRATIONS 1
FPN1 AT FRAME 20
INTEGRATION BEGAN AT FRAME 35
LAST NON DESTRUCTIVE READ AT 1846
LAST INTEGRATION FINISHED AT FRAME 1878
FPN2 AT FRAME 1928

INTEGRATION PERIOD (ACTUAL) 1843

BLOCK NUMBER= 0 FPN1

		(i)	(ii)	(iii)	(iv)
1 ,	2 :	3945	725	732	734
3 ,	4 :	3946	529	535	538
5 ,	6 :	3945	677	684	687
7 ,	8 :	3946	415	419	421
9 ,	10 :	3946	280	286	287

BLOCK NUMBER= 2 DSRO

1 ,	2 :	3947	1452	1153	888
3 ,	4 :	3946	1236	976	691
5 ,	6 :	3947	1371	1131	844
7 ,	8 :	3947	1212	903	579
9 ,	10 :	3946	1043	741	459

BLOCK NUMBER= 3 FPN2

1 ,	2 :	3944	762	768	769
3 ,	4 :	3944	566	572	574
5 ,	6 :	3943	719	725	728
7 ,	8 :	3944	454	458	460
9 ,	10 :	3946	321	327	329

FIG.6.10. RECHARGE FAILURE IN RUN 196 - PRINTOUT

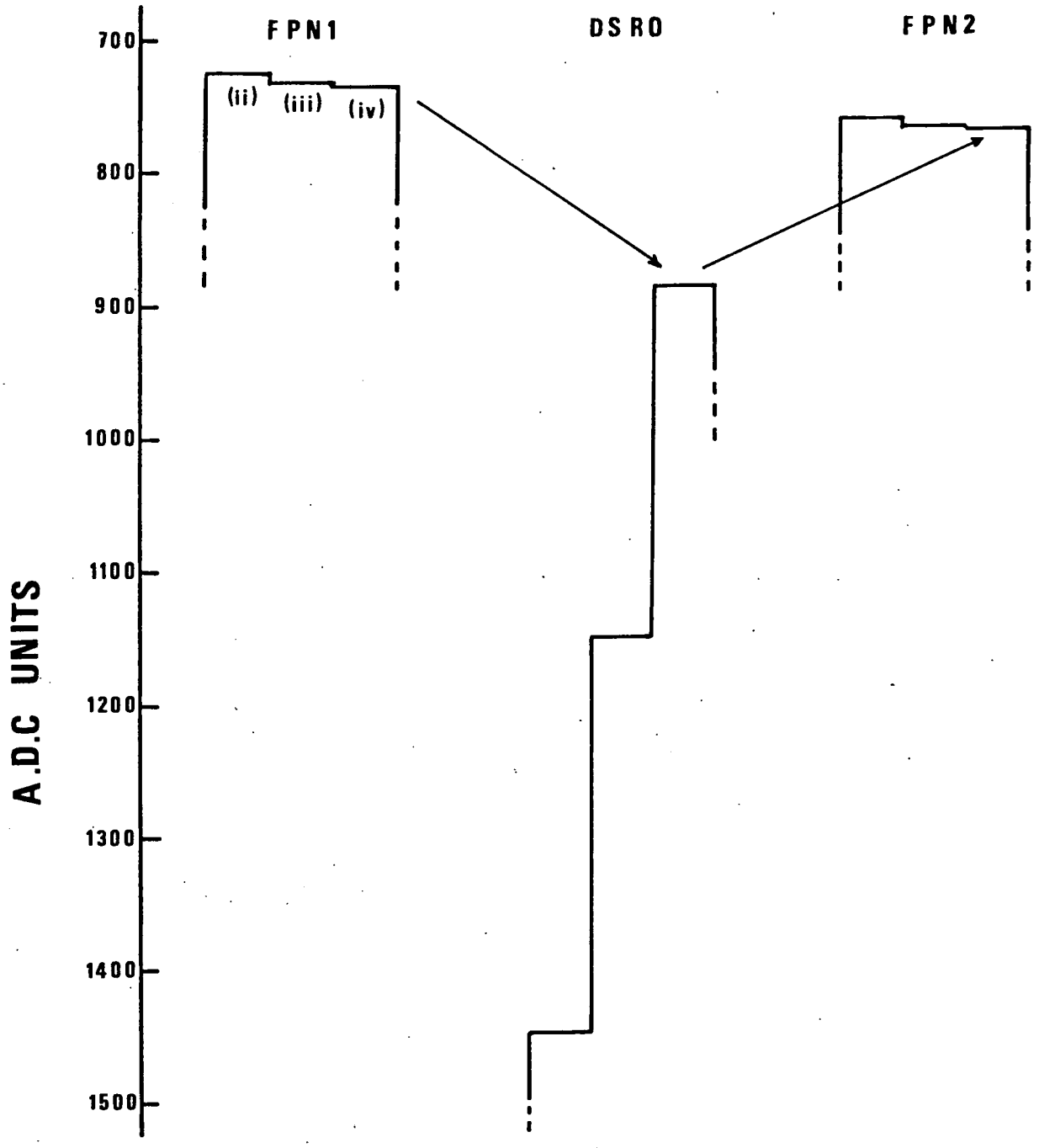


FIG.6.11 RECHARGE FAILURE

Exposures were made on the H_α line in Vega, as this is a very wide and strong feature. An exposure was made on this line for 2.5 minutes (Run 312). This was followed by a second exposure (Run 314), this time with a 10.5% neutral density filter inserted between the telescope and the spectrograph slit, but with an exposure time of 25 minutes. Thus these two exposures should have been similar in terms of integrated light. The continuum level of Run 312 (no filter) proved slightly lower than that of Run 314, possibly due to guiding problems or incorrect calibration of the filter. The two continua were normalised by simply scaling the data of Run 312 by a constant factor (1.24). The two spectra, so matched, and divided by the tungsten spectrum of Run 201 (Figure 6.5. (b)) are shown in Figure 6.12. (in the region of the H_α line only).

The feature is shallower in the spectrum from the weaker signal than in the spectrum from the stronger signal.

This supports the suspicions that led to the experiment. It is not clear from these observations whether the effect is due to a genuine reduction in responsivity at low light levels, or to a threshold effect, or to a combination of both. There is evidence for both in previous data (Chapter 5.4). A threshold has been observed during observations of thermal leakage, but this has yet to be satisfactorily investigated. Support for the responsivity being a function of signal level also comes from thermal leakage current measurements. Consider the leakage current density curve of Figure 5.6. This shows a downward trend at low temperatures. This could be explained by a reduced responsivity at low temperatures (small signal levels).

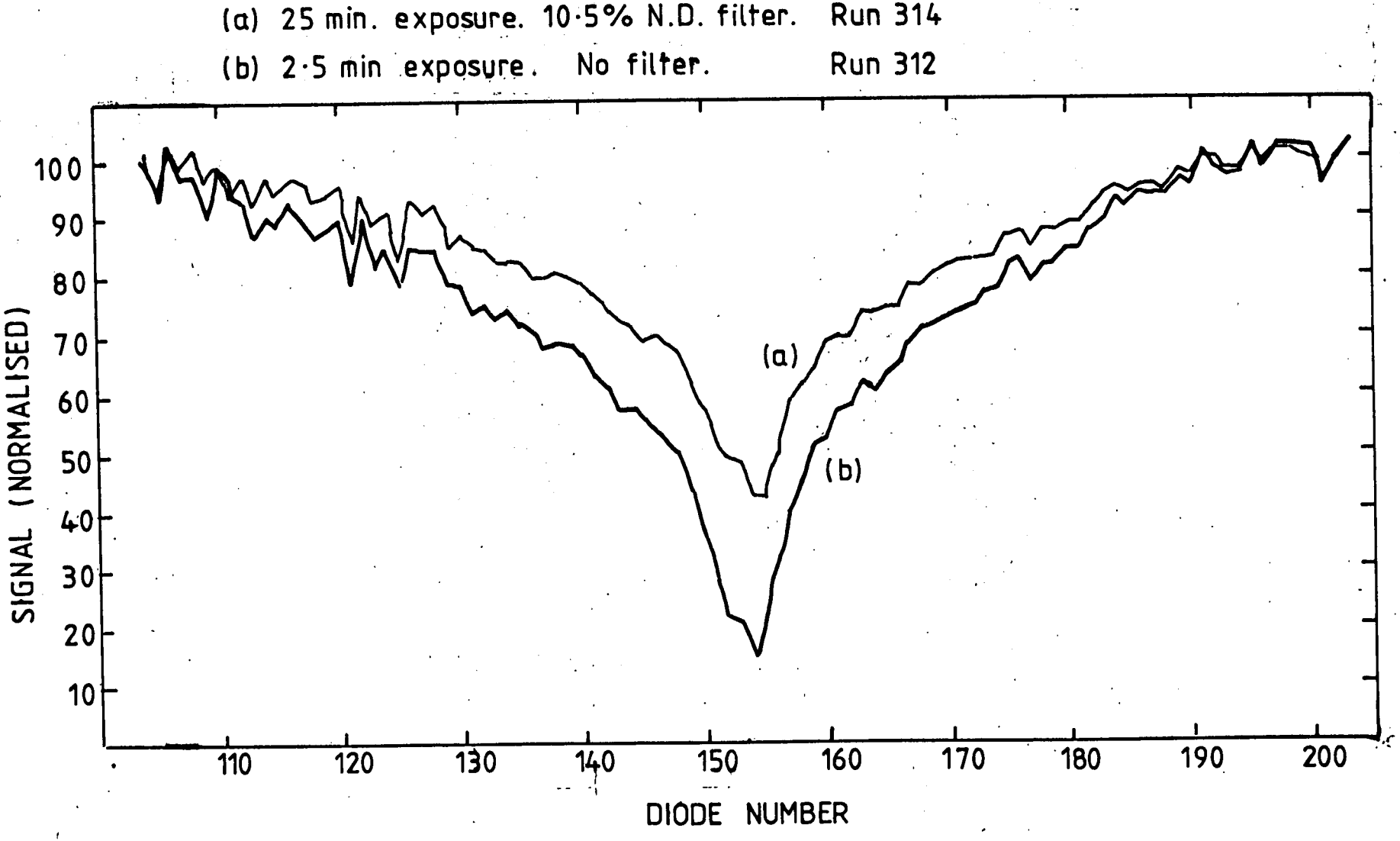


FIG.6.12. OBSERVED RECIPROCITY FAILURE

More work is necessary to isolate the factors contributing to this reciprocity failure. Suggestions have been made that the effect is caused by the "inversion" of levels at low light levels as seen in Section 6.3.4. This would contribute about 5 to 8 ADC units, as opposed to the threshold of 30 or so ADC units required to explain this example of non-reciprocity.

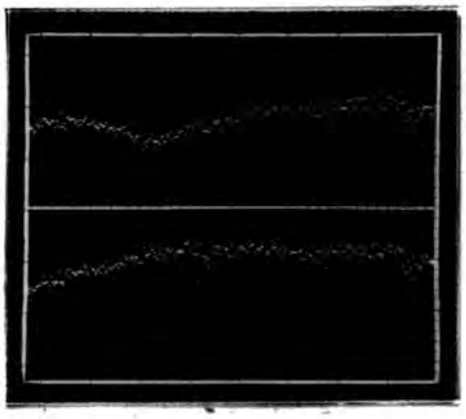
6.3.6. Odd-Even Effect

On many exposures, a difference in responsivity between odd and even numbered diodes has been observed. An illustration of this effect can be seen in Figure 6.13. The photograph of Figure 6.13 (a) shows, on the upper half of the screen, a "subtracted" spectrum of Vega showing a strong absorption feature (Run 175). On the lower half of the screen is a tungsten exposure (Run 174), taken immediately prior to the exposure. The result of dividing the upper spectrum by the lower spectrum is shown in Figure 6.13 (b).

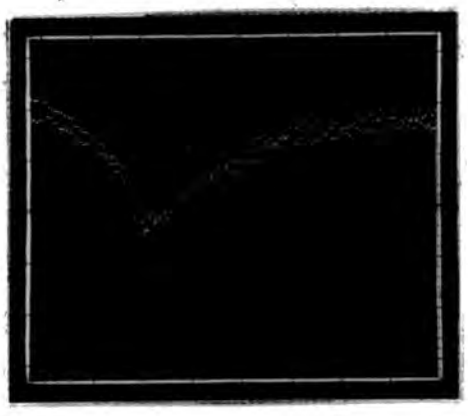
The differences in responsivity between the odd and even diodes is clearly visible, especially at the left hand end of the spectrum. Note however, that if this effect had the same magnitude in both the stellar and the tungsten spectra, then it would be removed by the division.

Observation of the phenomenon has led us to believe that it is dependent upon the alignment of the slit image onto the diode array. Where the image spills over the edge of the diode area, excess signal appears to be generated.

In this array, because it was not designed for optical imaging, the circuitry on either side of the active diode area is not masked from light. Odd and even numbered diodes have their readout electronics situated on opposite sides of the line of diodes. Therefore, if there is some mechanism whereby signal can be generated in the supposedly insensitive electronics, a misaligned slit image will cause this odd-even effect.



(a)



(b)

FIG. 6.13. ODD - EVEN EFFECT

Figure 6.14 (a) shows the conventional circuit diagram for the elements. However, each reverse biased diffusion will of course act as a photodiode. Figure 6.14. (b) shows this circuit redrawn to include these additional sources of photocurrent. Each has a somewhat different effect.

D1 is the large area photodiode. D2 is the drain diffusion of T1, and is in parallel with D1. The area of the drain diffusion is not known, but is probably about 10 μm x 10 μm, that is just over 1% of the area of D1. Thus its contribution to the responsivity will be very small.

Diodes D3 and D5 are formed by the drain diffusion of T2 and the source diffusion of T1 respectively. These are of similar area to D2. These photocurrents will discharge directly the gate capacitance C_G of T3, the source follower transistor.

The photocurrents of D1, D2, D3 and D5 are thus all integrated on the source follower gate capacitance. The drain of T3 acts as a photodiode (D4) but this photocurrent is not integrated and its effect will therefore be small except at very high light levels.

The source diffusions of T2 and T3 also act as photodiodes, but their effect is only to create a leakage current from the V_{DD} line to the substrate and this will not affect responsivity. Sources of photocurrent exist within the shift register, but their effect is difficult to predict and will hopefully not degrade the array characteristics.

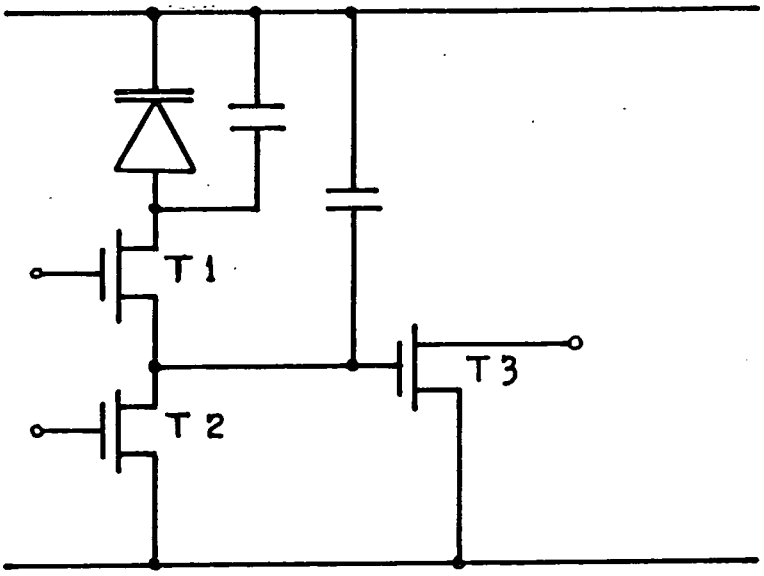


FIG 6.14. (a) BASIC CIRCUIT OF ELEMENT

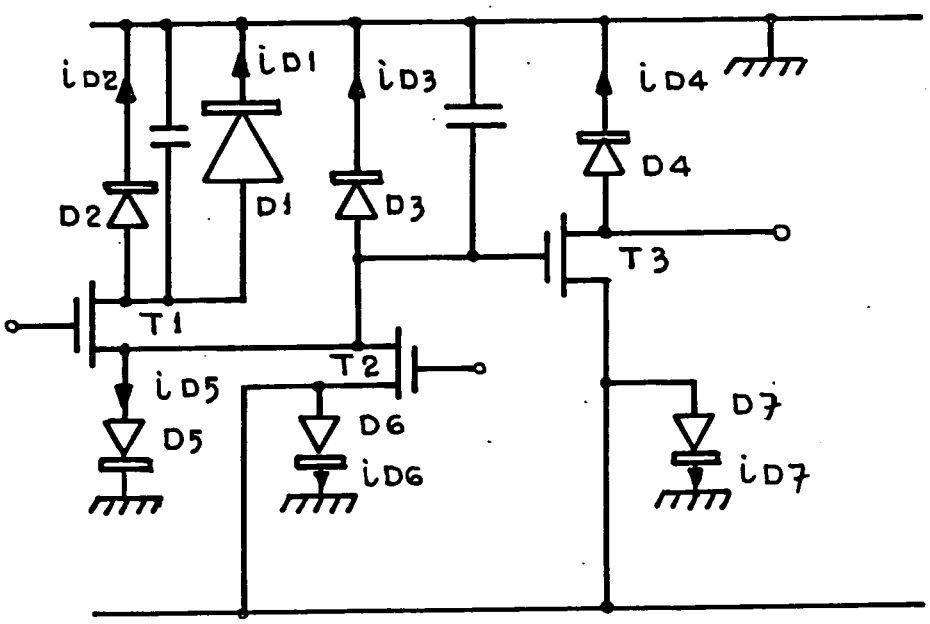


FIG 6.14. (b) SOURCES OF PHOTOCURRENT

It was noted earlier that this odd-even effect, or "splitting", had different characteristics in the tungsten and stellar exposures. This has been attributed to the alignment of the spectrograph. The slit image from the tungsten lamp is not accurately coincident with the slit image from a star. Further problems arise because the position of the slit image moves as the grating incidence is changed.

These difficulties make it essential that array alignment is checked, and if necessary, corrected, periodically. Problems arise on long integrations on stellar objects. The position of the slit image on the array is dependent on the position of the stellar image on the entrace slit. As the hour angle of the telescope changes during guiding, the position at which the autoguider places the image moves. Also, it has been found that the array position moves slightly as the level of the liquid nitrogen in the dewar drops. Thus even with careful alignment, some "splitting" is usually found on long exposures.

6.4. Summary

The array has been operated with a certain degree of success at the 30 inch telescope at the RGO. The operation of the computer controlled electronic system has been proved, and a suite of programs has been developed in CATY covering on-line operation, data inspection and limited data reduction. The techniques of non-destructive readout, subtraction of fixed pattern noise and responsivity correction by division of spectra have all been developed and proved.

The minimum digitisation step is too large to enable noise limited performance, but excessive fixed pattern offset noise prevents significant reduction of this step size. Possible "feedback" systems for reducing the offset noise prior to digitisation are being evaluated.

Some "odd-even" variation in diode signal has been observed, and this has been traced to light spillage onto unmasked, photosensitive areas of the on-chip electronics.

Considerable problems have been encountered with variation of recharge levels and with image retention. Reciprocity failure has also been demonstrated, in that the array is less responsive to faint light than to strong, and consequently strong spectral features have not been found in exposures on weak objects. These problems confirm many of the findings of Chapter 5, which described the initial laboratory testing.

The implications of these problems for the project as a whole are discussed in the following Chapter.

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1) A.W. Campbell, Ph.D. Thesis, University of Durham, in preparation.

2) A. Humrich, Ph.D. Thesis, University of Durham, in preparation.

3) A Humrich, University of Durham Internal Report, NI - 79 - 1, 1979.

4) S.S. Vogt, R.G. Tull and P. Kelton, Applied Optics, 17, p. 574, 1978.

CHAPTER SEVEN

A Review of the Plessey Array Project, and some Comments on Future Development

This Chapter sets out to review the important features of the work so far carried out by the Durham group in the period from their first involvement with the project in February 1977, until the end of the first observing period at the R.G.O. in August 1980.

The concepts underlying the design of the array will be reviewed briefly prior to a discussion of the results so far.

7.1. The Design of the Plessey Array

The interest in diode arrays for astronomical imaging has been demonstrated by the number of groups using Reticon arrays. These have all been recharge sampling arrays. The benefits offered by such detectors have been the high quantum efficiency characteristic of silicon detectors, the absence of image retention or lag, and the linearity of response, coupled with simplicity of use.

The Plessey array was developed in conjunction with the RGO not for use in direct optical imaging applications, but for installation as a photoelectron detector in an electronographic tube. Various novel techniques were included in its design.

It was thought that the signal produced by a single photoelectron would be insufficient to overcome readout noise, and so the "on-chip" amplifier transistor was included. This has the effect of integrating the photocurrent (and the leakage current) not on the photodiode capacitance, but on the smaller gate capacitance of the source follower, thereby producing a greater voltage swing. The source follower output is then gated onto the video line by a multiplexing transistor. The source follower gate capacitance can be recharged after readout by a charging transistor. Thus the array has considerable similarities in principle to a conventional voltage sampling array and of course also inherits its problems of an output characteristic that is critically dependent upon the type of output load in use.

There is a further special feature of the Plessey array. There is separate access to the recharge line, and this leads to the possibility of double sampling, which can be used to remove offset fixed pattern noise and reduces low frequency random noise. Furthermore, by not enabling the recharge line during a readout, a non-destructive read can be performed. Averaging a number of successive non-destructive readouts can be used as a means of reducing random noise.

The expected advantages of the Plessey array therefore are chiefly an improved signal-to-noise ratio due to the amplifying transistor and to the double sampling and non-destructive read techniques. Some problems are predicted to arise from these techniques, however.

7.2. Predicted Problems arising from the Design of the Plessey Array

Conventional voltage sampling arrays have been shown to have non-ideal output characteristics when driven into real loads. The worst case load has been shown to be the virtual earth circuit.

The situation for the Plessey array becomes even worse. Because of layout constraints, outputs from adjacent diode elements are gated onto the video line simultaneously. Extraction of the separate diode data is achieved by the use of two charge pulse lines. Linear operation relies upon a correct summing action on the video line when connected to the output load. Such a summing action occurs only in the case of the virtual earth load.

Further problems arise when the charge transfer mechanism through the amplifying transistor is considered. Signal transfer has been predicted to be slow at low signal levels.

Such then are the anticipated problems based on simple linear circuit analysis. Further problems have been encountered in practice.

7.3. Observed Problems with the Operation of the Plessey Arrays

During laboratory tests, it was discovered that the double sample read operation fails to give a representative measure of the integrated light signal. This appears to be due to incomplete recharging by the charge pulses. The non-destructive read seems a better estimate, but by using this the spatial resolution is degraded by a factor of two, and any advantages of double sampling to reduce random noise are lost.

The response time of the output to changes in light intensity was found to be slow. Furthermore, there seems to be evidence that the integrating action of the detector fails at high light levels.

During operation at the R.G.O., the same problem of the double sample readout underestimating the integrated signal was noted. Image retention over a considerable period has been observed, and reciprocity failure has been demonstrated.

Two other problems have been encountered, but these promise to be relatively easy to overcome. The first is the excessive fixed pattern offset noise which limits the digitisation precision. This should be reduceable by pre - ADC signal processing. The second is the odd-even effect which is due to stray illumination of the on-chip readout electronics. This should be eliminated by masking.

On the merit side, tests have shown a random noise figure lower than that observed in Reticon devices. The spectral response characteristics are also very promising.

So far, the causes of the problems observed have not been satisfactorily identified, and this must form a major part of future work plans.

7.4. A Suggested Outline for Short-Term Future Work

7.4.1. Laboratory Measurements

The laboratory measurements described in Chapter Five were restricted by a lack of suitable equipment. In particular, the integration control and data acquisition system was still under development. Temperature control of the array was poor and no optical test facilities existed. Furthermore, many measurements would have benefited from the use of a transient recorder.

A major problem has been to isolate one aspect of array operation from another. Some steps were made towards this in the impulse response experiments (Chapter 5.8.). This experiment was only possible with advent of the computer based control system. The use of the control system, in conjunction with the transient recorder, has been shown in recent measurements on random noise characteristics[1)], measurements which would not have been possible without this equipment.

With the equipment now available, along with a good optical imaging system, it should be possible to carry out detailed investigation into the effects so far discovered.

There appear to be three main functions of the element that are worthy of investigation.

The transfer of signal from the diode and its integration on the source follower gate capacitance needs to be investigated. The method of using short light impulses seems promising, as this enables the process to be monitored in isolation from the recharge function.

The recharging function also requires further investigation. Again, a system using short light impulses enables a single recharge operation from any desired signal level to be monitored.

There is an apparent reciprocity failure and possibly a threshold effect. A study of these requires a light source capable of imaging accurately related and very small light intensities onto the array in order to observe its behaviour with small diode currents.

Even using such techniques it may prove impossible to isolate one mechanism from another. It would be very useful, for such work, to have available a single element device such as the device used by the RGO for initial tests in the Kron camera.

7.4.2. Improvements to the Control and Acquisition System

The system as described in Chapter Four is well suited to experimental work of the type proposed above. For the full potential of the array to be realised for astronomical work, some additions to the system are required. The first of these in terms of priority is the pre-ADC offset reduction system.

The usefulness of the computer is limited by its shortage of addressable memory, and the absence of a rapid access mass storage device. An extension to 32K words of main memory and the addition of a twin floppy disk unit is worthwhile, and this has been done already. This permits the use of the powerful RT-11 operating system and the use of high-level languages such as FORTRAN IV for data analysis. As mentioned previously, CATY is ideal for the type of on-line control being done at present. More powerful languages are worth considering for future use, but the programming overheads associated must be carefully evaluated.

Two useful surveys of the CAMAC oriented languages on the market have been published [2,3].

It is not possible with the present system to exploit the possibilities of averaging successive non-destructive read outs. To do so requires either an extremely large buffer store, or some sort of recycling memory into which successive frames can be added. These two alternatives are sketched as Figures 7.1. and 7.2.

The above, then, is a recommendation for the immediate, short term work, and consists of some extensions to the control and acquisition system and a detailed investigation into the device characteristics.

A long term development programme is much more difficult to suggest. The following section puts forward the author's personal views and recommendations, and these do not necessarily represent the opinions of any other members of the group, past or present.

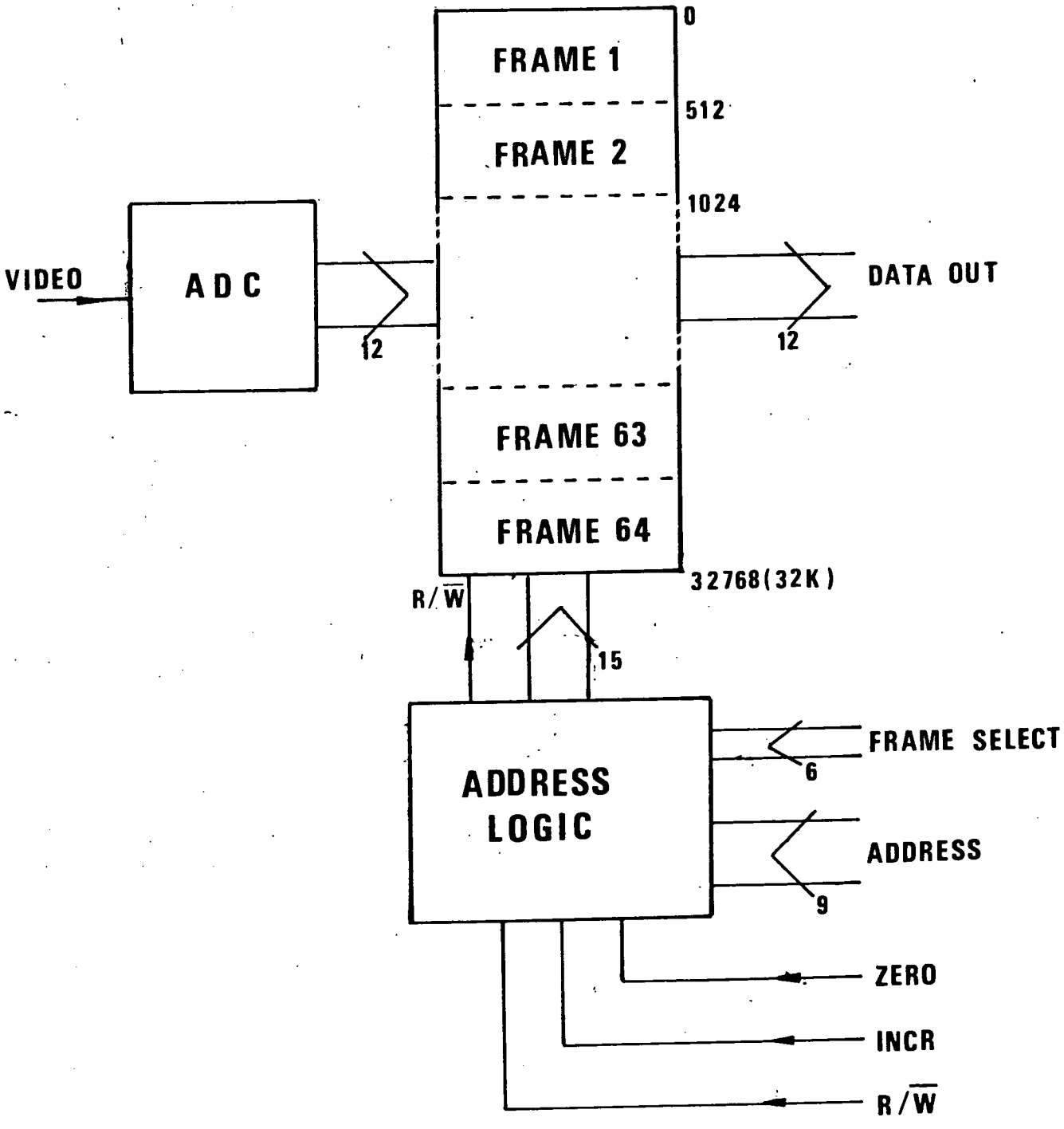


FIG.7.1. NDRO SCHEME USING VERY LARGE BUFFER MEMORY

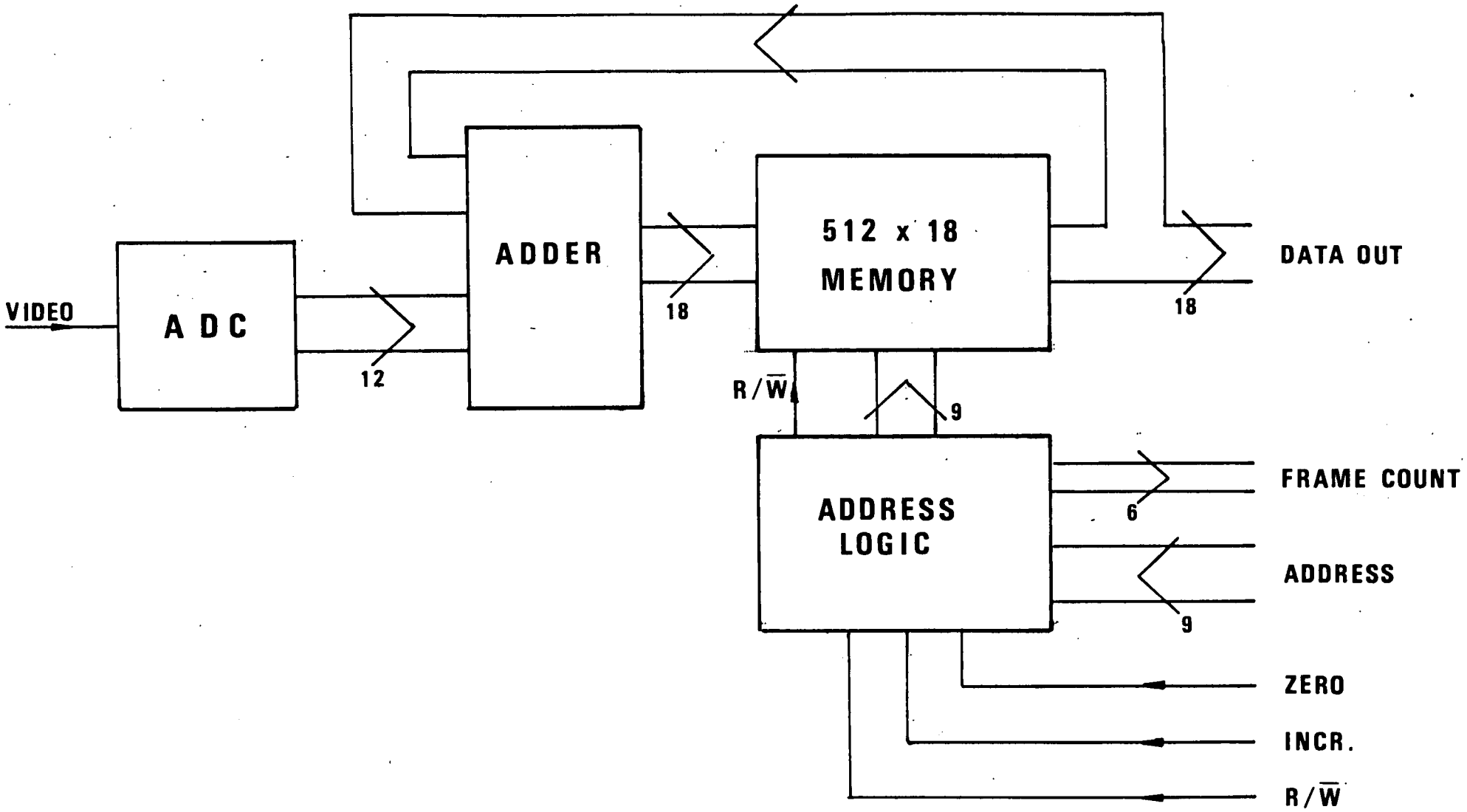


FIG.7.2. NDRO SCHEME USING RECIRCULATING/ADDING MEMORY

7.5. Suggested Long-Term Development Plans

The following suggestions are based on the premise that the goal of this project is to produce a detector system capable of generating good astronomical observations. Implicit in this is that it should have a performance better or at least equal to other systems currently in use. The discussion really hinges on the type of device to use, as no major re-think is required concerning the structure of the electronic/computing system. The options available for the type of device to be used include the existing Plessey array, a custom designed device, or a commercially available diode array, CCD or CID.

7.5.1. The Plessey Array

The most immediately attractive policy is to continue observational work with the Plessey Array.

The observational period at the R.G.O. was extremely valuable in revealing problems associated with the devices. Much work on identifying the sources of these problems remains to be done before further observing work can be attempted. Even then it is difficult to see how a good detector system can be built around a device known to have these problems of image retention, non-reciprocity, incorrect estimation of signal, and non-linearity.

The one outstanding feature of the array is non-destructive readout, but even this is achievable only with a reduced spatial resolution.

7.5.2. A Custom Designed Array

This is in some ways the logical extension of the project, in that a custom designed array has been built, tested and its deficiences identified, and so the experience gained could be put into an improved design. It is possible to put forward tentative suggestions for a voltage sampling array which might possess some of the advantages of the Plessey array but without some of the problems. For example, the circuit of Figure 7.3. would still provide for non-destructive readout and double sampling. The transfer transistor has been removed and the signal is now integrated on the diode capacitance. The elements are no longer paired and thus non-destructive readout is now possible without loss of spatial resolution, and the summing problem is removed. The inherent non-linearities of voltage sampling arrays are still present.

Before such a project could be started, an in-depth knowledge of the mechanisms within the Plessey array would be required. Close collaboration with a semi-conductor manufacturer would be essential and considerable funding would be required. It is difficult to see from where sufficient interest could be generated in order to sponsor such a project. It is also not clear that the device would out-perform existing commercially available arrays.

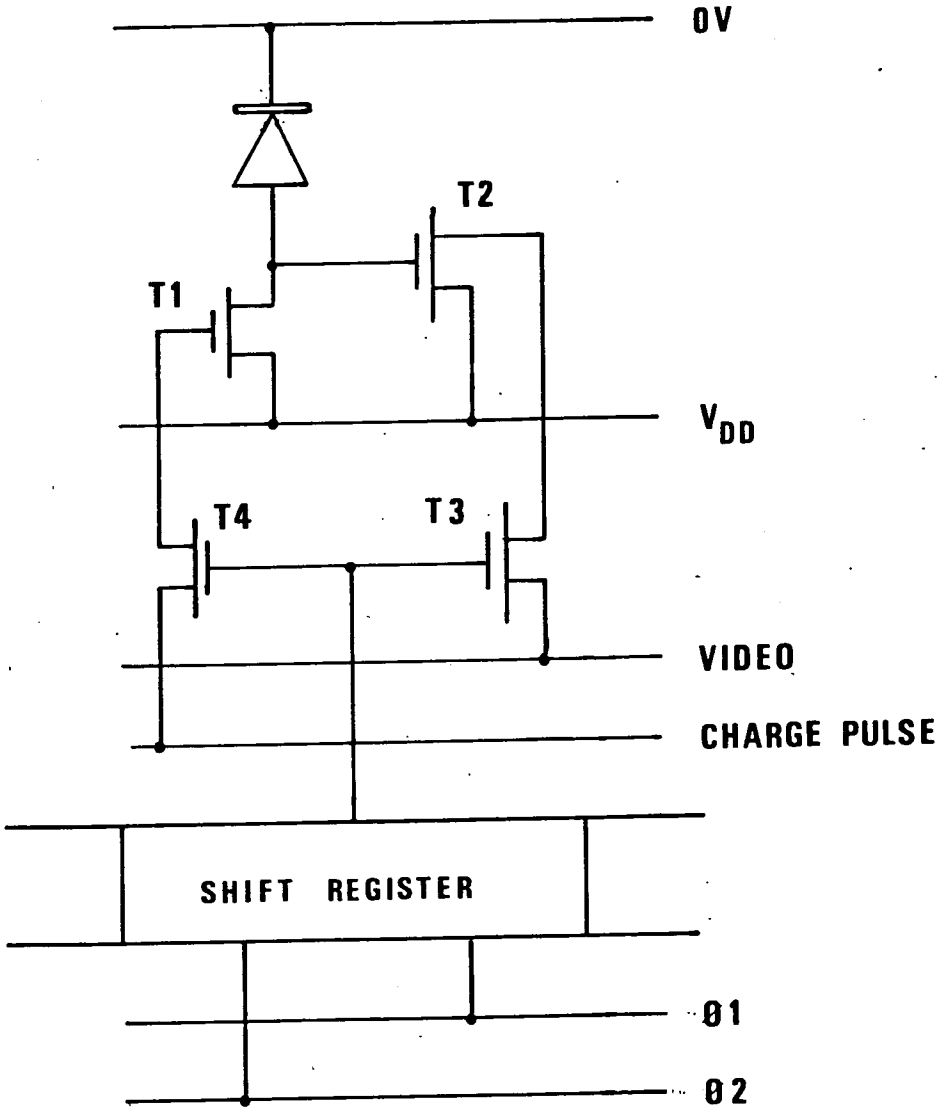


FIG.7.3. SUGGESTED ARRAY

7.5.3. Reticons and CCD's

Other groups have had success with Reticon arrays, and these appear to suffer from none of the problems we have encountered. These arrays, being recharge sampled, do not offer the possibility of non-destructive readout. Similarly work has been done with CCD's and these seem to offer a lower noise level than recharge sampling diode arrays. Both types of device are readily available. Of particular interest is the Reticon CCPD, a diode array with a CCD readout register.

Using such devices would enable a working system, usable for astronomy, to be constructed within a relatively short time. It has been done before, and holds little technical interest as a research project, but may be of value as a "bread and butter" project to maintain credibility and generate enthusiasm within the astronomical community. If the aims of the group were simply to "do some astronomy", it would probably be the best option to follow.

7.5.4. The CID Array

Of much greater technical interest is the potential of the CID device. CID's are capable of performing a non-destructive read operation. A CID array has been purchased by the group, but so far little work has been done on this. The device size is 342 elements by 42 elements, and this will lead to some signal processing problems. The storage required for a single frame is slightly less than 16K words. In order to benefit from averaging repetitive non-destructive readouts, a large recirculating and adding memory is required. For example, to sum 64 frames of 12 bit resolution would require a 16K x 18 bit buffer memory.

The investigation of the CID is worth considerable effort, and it seems to be here that the future of the group lies, rather than in continuing astronomical observations of dubious quality with the Plessey array.

7.5.5. Intensified Imaging with the Plessey Array

The Plessey array was developed for use in the photoelectron counting mode. All the problems that have so far hampered its use as an optical imager would be unimportant if the array was used in this mode. Some consideration should be given to this, and the interest within groups using devices such as the electronographic tube should be assessed.

7.6. Conclusion

At the outset of the project, the Nuclear Instrumentation Group had no experience of optical imaging systems. In the 18 month period between the first visit of the author to the R.G.O. to acquaint himself with the arrays, and the end of the first observational trials at the R.G.O., considerable progress has been made. A powerful computer controlled acquisition system has been developed from scratch, and a number of properties of the arrays have been evaluated. The group as a whole has built up a considerable expertise in imaging systems work, both in terms of knowledge and experimental facilities. The Plessey array has exhibited a number of shortcomings when used for optical imaging, and these cast some doubt about its ultimate usefulness as a detector for astronomy. The characteristics of the device are worth further investigation, but consideration must be given to other types of solid state imaging array. The CID seems to be the most promising, but a Reticon device would probably lead to an operational observing instrument in a shorter time.

REFERENCES

1) G.R. Hopkinson and A.W. Campbell,
Durham University Internal Report, NI - 80 - 1, 1980.

2) P.N. Clout, Daresbury Laboratory Preprint,
DL/P 263, 1976.

3) C.L. Stephens, Proc. ESO/SRC Conference on
Applications of CAMAC to Astronomy, p.76, 1978.

APPENDIX A

Definitions and Derivations of DQE for an Integrating Detector

The usual measure of quantum efficiency quoted for a detector is its Responsive Quantum Efficiency (RQE). The RQE is defined simply as :-

$$RQE = \frac{\text{no. of detected photons}}{\text{no. of incident photons}} \qquad (A.1.)$$

A more useful measure of the performance of an integrating detector is its Detective Quantum Efficiency (DQE). This is defined as :-

$$DQE = \frac{(S/N)^2 \text{ out}}{(S/N)^2 \text{ in}} \qquad (A.2.)$$

where (S/N) out = signal to noise ratio of the output signal

and (S/N) in = signal to noise ratio of the input signal

Consider this in relation to a diode array. We must first calculate the signal to noise ratio of the output. In order to do this, we assume that two readouts are made, one after an integration on the light source, and the second after a dark exposure. These are then subtracted to remove offset noise. The array is cooled, so leakage current and the shot noise on the leakage current are taken as zero.

The signal will be given by :-

$$S_{out} = RQE\ N_p\ \Delta T_1$$

where RQE = Responsive Quantum Efficiency of the detector

N_p = Incident Photon Rate

ΔT_1 = Exposure time of first (signal) integration

The noise on the output has 3 components.

(a) the shot noise on the input signal.

(b) the readout noise on the first integration.

(c) the readout noise on the second integration.

Thus $N^2_{out} = RQE\ N_p\ \Delta T_1 + 2\sigma^2$; where σ is the readout noise

and we have

$$(S/N)_{out} = \frac{RQE\ N_p \Delta T_1}{\sqrt{RQE\ N_p \Delta T_1 + 2\sigma^2}} \qquad (A.3.)$$

The signal at the input is given by :-

$$S_{in} = N_p \Delta T_1$$

and the noise on this is the shot noise, given by :-

$$N_{in} = \sqrt{N_p \Delta T_1}$$

and so

$$(S/N)_{in} = \sqrt{N_p\ \Delta T_1} \qquad (A.4.)$$

This gives the DQE, from Equation A.2. as :-

$$DQE = \frac{RQE}{1 + \left[\frac{2\sigma^2}{RQE\ \ N_p \Delta T_1}\right]} \qquad (A.5.)$$

The advantages of non-destructive readout can be seen by predicting the DQE obtained by averaging a number of such readouts. The approach is similar, but the readout noise is reduced because N samples are taken.

This gives a new readout noise of :-

$$\mathcal{E} = \frac{\sigma}{\sqrt{N}}$$

$\mathcal{E}_1$ is the noise resulting from N_1 measurements of the signal, and

$\mathcal{E}_2$ is the noise resulting from N_2 measurements of the dark integration.

The DQE becomes :-

$$DQE = \frac{RQE}{1 + \left[\frac{\mathcal{E}_1^2 + \mathcal{E}_2^2}{RQE\ N_p \Delta T_1}\right]}$$

Now, if $N_1 = N_2$, then $\mathcal{E}_1 = \mathcal{E}_2$ and this becomes :-

$$DQE = \frac{RQE}{1 + \left[\frac{2\sigma^2}{N\ RQE\ N_p \Delta T_1}\right]} \qquad (A.6.)$$

APPENDIX B

The Digitisation Sequence Generator

The circuit diagram of this module is shown in Figure B.1. Only one of the four programmable channels is shown in full, the others being identical.

The 16 cycle count sequence is generated by the 4 bit counter IC1 and the 4 to 16 line demulitplexer IC2. Start and Stop pulses are synthesised by programming 16 to 4 line multiplexers(IC3A and IC8A), the outputs of which feed a D-type flip flop (IC7A) which generates the output pulse of the desired length and timing.

Four programmable outputs are generated in this way. A fifth, preset output is generated by the flip-flop IC12. This output has a duty cycle of 50% and is used as the Sub-Clock to the Clock Phase Generator.

Programming of the Stop and Start Multiplexers is by a single pair of hexadecimal thumb wheel switches common to all four output channels. Programming of each channel is achieved by setting the desired start and stop times on the thumb wheels and depressing the "SET" switch for that particular channel. The next channel can then be programmed in the same manner. Similarly the settings of each channel can be observed on a pair of hexadecimal LED displays by depressing the "VIEW" switch of the desired channel.

Figure B.2. shows a typical timing sequence and the thumb wheel settings required to program it.

Power for the module is taken from the NIM + 6V rail via series transistors to reduce the TTL supply to 5.4V.

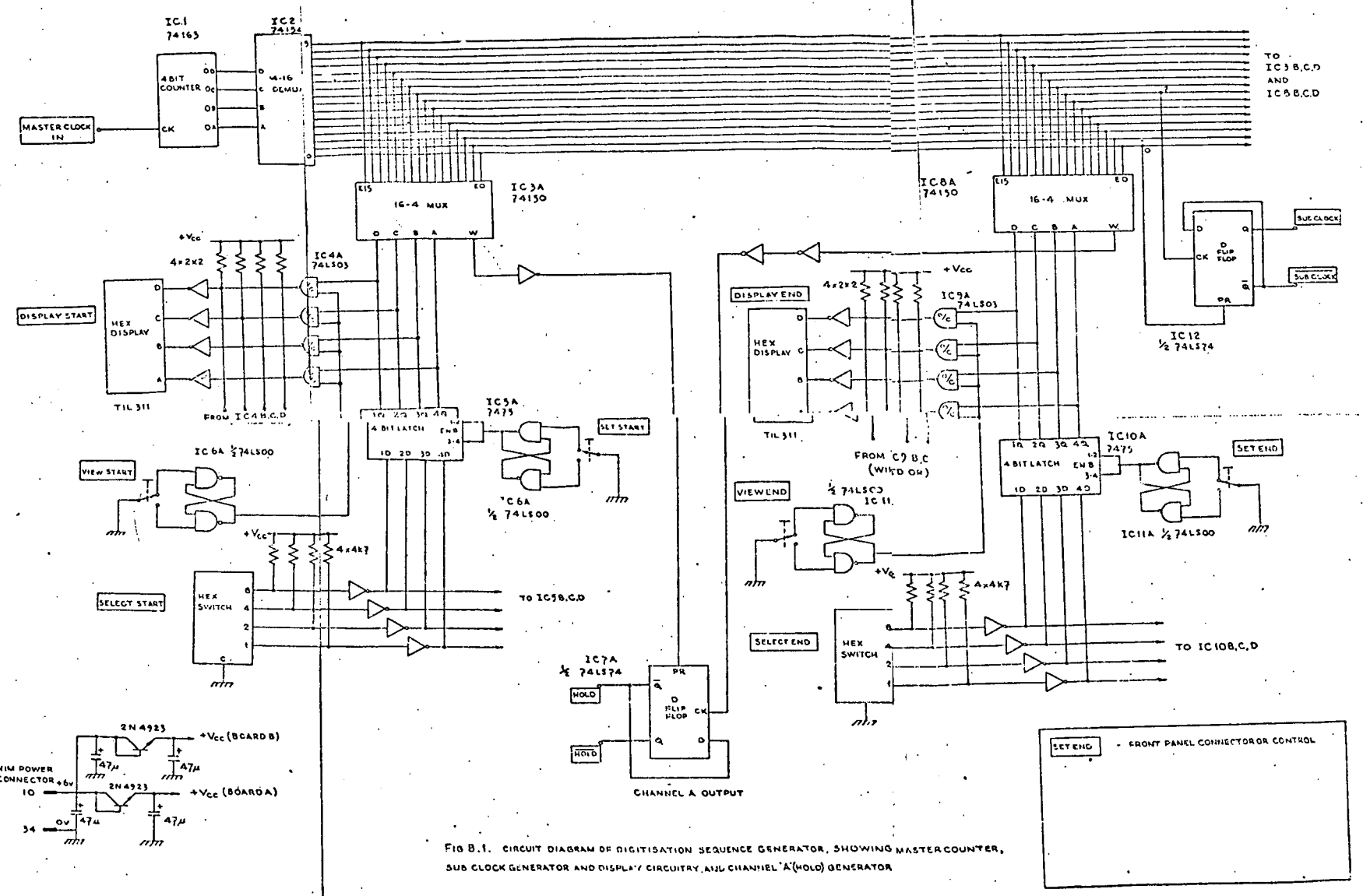


FIG 8.1. CIRCUIT DIAGRAM OF DIGITISATION SEQUENCE GENERATOR, SHOWING MASTER COUNTER, SUB CLOCK GENERATOR AND DISPLAY CIRCUITRY, AND CHANNEL 'A' (HOLD) GENERATOR

SCALE

DRG No

M. R. Smith (Technical Developments) Ltd.

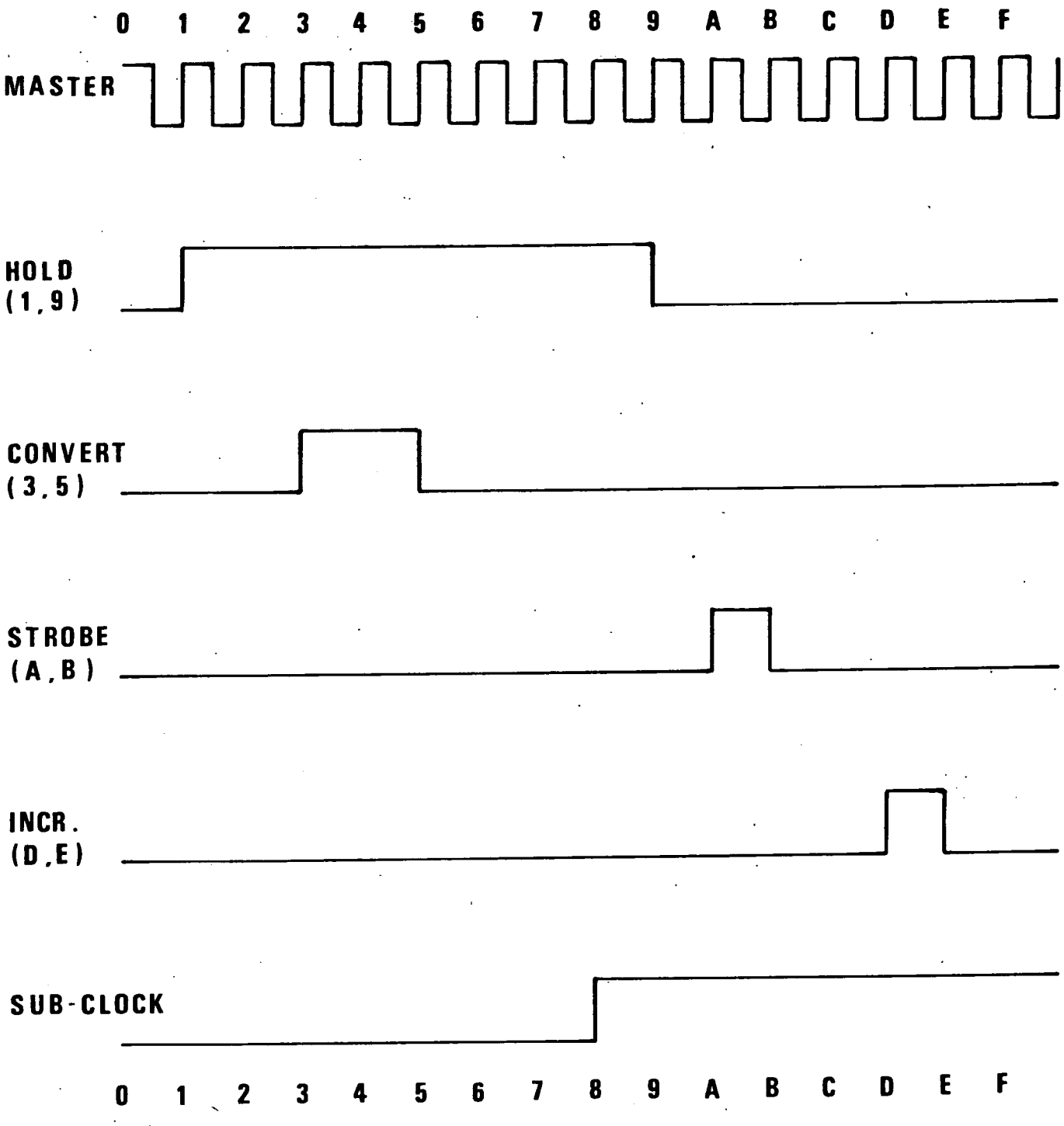


FIG.B.2. TYPICAL TIMING SEQUENCE

APPENDIX C

The Integration Control Module

The circuit of this module is drawn in Figures C.1A. and C.1B. Figure C.1.A. shows the functional section of the module, and Figure C.1B. shows the CAMAC decoder and power supplies.

The MASK register is written to from the W1 to W3 lines on the dataway. W1 gates the Strobe and Increment commands, W2 the Charge Pulses and W3 the LSR pulse.

There are 3 LAM sources, L1 set by the LSR pulse each frame, and L2 and L3 by front panel push-buttons but generated coincident with L1 to simplify LAM handling.

These are monitored by the LAM status register. The design rules of EUR 4100 specify that each LAM source shall be independently maskable and testable. Outputs enabled by the LAM Mask register are "OR'ed" to produce the L request. Similarly, the results of the TEST functions are "OR'ed" to produce the Q response.

Only even-numbered F commands are used, thus simplifying decoder logic. Full CAMAC decode is implemented, and the commands are summarised in the table in Figure C.1B. For the LAM handling commands, sub-address 0 forces a common action to all three LAM sources, whereas each source can be handled independently by using the appropriate sub-address.

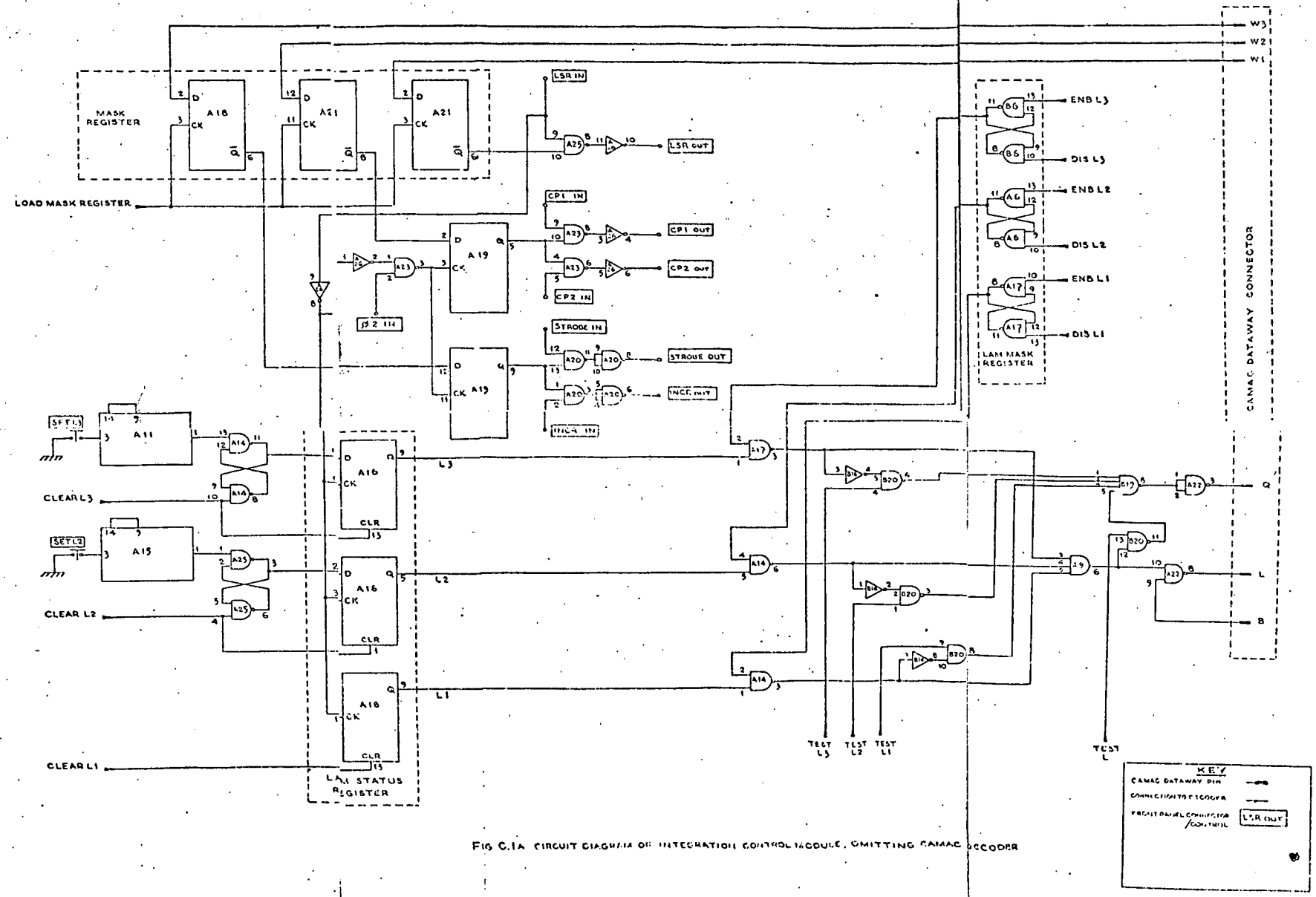
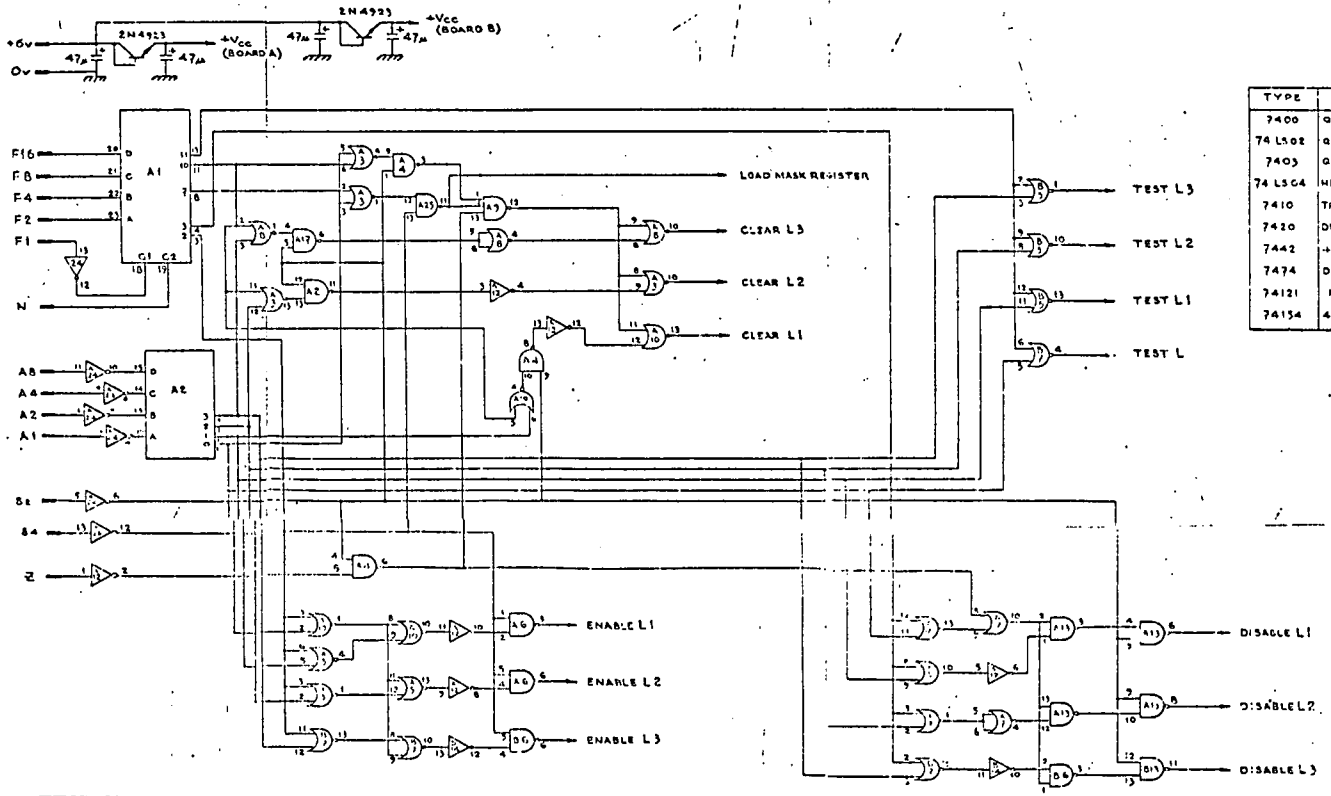


FIG C.1A CIRCUIT DIAGRAM OF INTEGRATION CONTROL MODULE, OMITTING CAMAC DECODER



TYPE	FUNCTION	I C's
7400	QUAD 2 IN N.AND	A 4,6,11,14,17,20,22,23 B 6,13,20
74 LS02	QUAD 2 IN N.R	A 3, A5, A7, A8, A10 B5, B7.
7403	QUAD 2 IN N/OD (*)	A 22
74 LS04	HEX INVERTR	A12, A24, A26 B 14
7410	TRIPLE 3 IN NAND	A 9.
7420	DUAL 4 IN N.AND	B 19
7442	4-10 DECODER	A 2
7474	DUAL D FLIP-FLOP	A 16, A18, A19, A21
74121	MONOSTABLE	A 11 , A15
74154	4-16 DECODR	A 1

FUNCTION	CAMAC COMMAND (S)	FUNCTION	CAMAC COMMANDS
LOAD MASK REG	F 16 . A0 . S1	TEST L	F 8 . A 0
CLEAR L 1 CLEAR L 2 CLEAR L 3	F16 . A0 . S1 + F10 . A0 . S2 + { F10 . A1 . S2 / F10 . A2 . S2 / F10 . A3 . S2 } + 2 . S2	TEST L1 TEST L2 TEST L3	F 8 . A 1 F 8 . A 2 F 8 . A 3
ENABLE L1 ENABLE L2 ENABLE L3	F 26 . A0 . S1 + { F26 A1 . S1 / F26 . A2 . S1 / F26 . A3 . S1 }	DISABLE L1 DISABLE L2 DISABLE L3	F24 . A0 . S2 + { F24 . A1 . S2 / F24 . A2 . S2 / F24 . A3 . S2 } + 2 . S2

FIG C.1B. CAMAC FUNCTION DECODER, POWER SUPPLY AND FUNCTION & I C. TABLES (READ IN CONJUNCTION WITH FIG C.1A)

APPENDIX D

The On-Line Control Program

The on-line control program is listed in Figure D.1. (a) - (m). This is the version for the 12 bit data acquisition system.

Lines 100 to 1060 define module addresses and storage areas. Because of the limitation on the naming of simple variables, a number of variables are gathered together in arrays W, A and U for economy.

Lines 1080 to 1175 prompt the user and initialise various counters and flags.

The main loop of the program is contained within lines 1185 to 1240. The current frame number is displayed on the user's VDU by lines 1222 to 1226.

On receipt of an interrupt, the program jumps out of the main loop into the interrupt handling routine (lines 1250 to 2140). Decisions within the routine are made according to the state of the frame counter, X, the "readout in progress" flag, L, and the L2 and L3 LAM requests.

Lines 2490 to 3650 are the memory transfer and display routines for the four readout frames.

At the end of the run, execution passes to line 4000. Interrupts are disabled and control is returned to the user. A run summary is printed and a menu of options for display, printout and dumping of data is presented.

Lines 4580 to 4780 contain the print routines, and lines 5000 to 5340 the graphics display routines. Lines 5360 to 5950 are subroutines called by the display routine.

Subtraction of spectra is handled by the Number Crunching subroutine of lines 6000 to 6210.

Lines 7000 to 7610 form the punch routine. The punching of some variables in the run header presents some problems. CATY words have a 24 bit precision, but only words of 8 bit or 16 bit length can be punched. A 16 bit word can store an integer up to 65535, but some integration periods (in frames) are larger than this. 24 bit words are split into two 16 bit words by lines 7120 to 7130, using the logical "AND" and "bit shift" facilities of CATY.

Lines 7620 to 8800 contain some short CAMAC subroutines called from other parts of the program. Lines 8600 to 8630 are a null subroutine, but a short routine to scale data is included here when using the 8 bit acquisition system. This is the only change required.

On occasion, it is useful to be able to "free run" the array (e.g. to set up amplifier gains), and a "free run" routine is included in line 9000 to 9160.

This is called from the interrupt routine when the flag, O, is set. A variable P is read from the DATA list in line 9130. This variable is the required mask word. If a value other than a valid mask work is returned, the RESTORE statement returns the DATA pointer to the beginning of the list. The free run routine is halted by the setting of the L2 LAM.

```
0100 REM *** 12 BIT DATA ACQUISITION PROGRAM.      TONY.1/8/76 ***
0101
0110 VDU=0,0,1     ;                    MODULE DEFINITION
0120 PTR=0,0,2
0130 PUNCH=0,0,3
0140 MEMR=0,0,8
0150 CNTL=0,0,7
0160 DRIVER=0,0,12
0170 MODE=0,0,13
0180 CHECK=0,0,15
0190 DSPL=0,0,20
0220
1010 REM              STORAGE ALLOCATION
1020 DIMEN Z(2048)
1030 DIMEN T(256)       ; STORAGE FOR REDUCED SPECTRUM
1040 DIMEN W(2)         ; STORAGE USED IN REDUCTION ROUTINE
1050 DIMEN A(4)         ; STORAGE USED IN PRINTOUT ROUTINE
1055 DIMEN U(4)        ; FRAME COUNTERS
1060 DIMEN M(20)      ; HEADER BLOCK FOR PAPER TAPE O/P
1070
1080 LET O=0                    ; CLEAR SCREEN AND PROMPT USER
1090 LET Y=1
1092 GOSUB 8750
1096 FOR Q= 1 TO 10000
1098 NEXT Q
1120
1125 LET D=20
1130 PRINT "LENGTH OF INTEGRATION PERIOD?"
1132 INPUT E
1135 LET G=1
1140 LET I=50
1145 PRINT "                RETURN TO START RUN "
1147 WAIT
1148 REM                      PROGRAM RUNNING
1150 PRINT " "
1152 LET M(4)=E
1153 LET M(5)=G
1155 LET M(10)=0
1156 FOR Q= 1 TO 2048 ;          ; CLEAR Z
1157 LET Z(Q)=0
1158 NEXT Q
1160 LET X=0    ; FRAME COUNTER                    INITIALISE COUNTERS & FLAG
1165 LET K=0      ; INTEGRATION COUNTER
1170 LET L=0    ; FLAG
1171 LET J=0
1175
```

FIG.D.1. LISTING OF ONLINE PROGRAM

(a)

```
1175
1176 REM --------- INTERRUPT DETECTION AND IDENTIFICATION ----------
1177
1180 ENB CNTL,0  ; ENABLE INTERRUPTS FROM CNTL MODULE
1185
1190 IF L=1 GOTO 2500 ; FPN1 READOUT IN PROGRESS
1200 IF L=2 GOTO 3000 ; DOUBLE SAMPLE READOUT IN PROGRESS
1210 IF L=3 GO TO3500 ; FPN2 IN PROGRESS
1215 IF L=4 GO TO 2750 ; NDRO IN PROGRESS
1217 IF L=5 GO TO 3700 ; FINAL NDRO SEQUENCE
1220 LET V=X-M(8)
1222 PRINT "        ",V
1224 LET Y='16
1226 GOSUB 8750
1228
1230 FOR Q= 1 TO 5000
1232 NEXT Q
1240 GO TO 1185
1245
1250 INTR 7        ; INTR FROM CONTROL MODULE
1251
1260 LET X=X+1
1270 WT1 DSPL,0,X ; CYCLE COUNTER
1280 IF 0=1 GO TO 9050    ;0#0 - FREE RUNNING
1285 IF 0=2 GO TO 9160
1290
1300 IF L=1 GOTO 1500  ; RECHARGE WHILE FPN1 IN PROGRESS
1310 IF L=2 GOTO 1500  ; RECHARGE WHILE D.SAMPLE IN PROGRESS
1320 IF L=3 GO TO 1500
1325 IF L=4 GO TO 1600
1326 TLM CNTL,2         ; TEST FOR STOP SIGNAL
1327 IF CAM2 GO TO 1950
1330 IF X<D GO TO 1500
1340 IF X=D GOTO 1800  ; FPN1 READ CYCLE
1360 IF X=F GO TO 1900  ; DOUBLE SAMPLE READ CYCLE
1390 TLM CNTL,3         ; TEST FOR NDRO REQUEST
1400 IF CAM2 GO TO 2100
1420 IF X<F GO TO 1600  ; LSR ONLY
1430 IF X=N GOTO 2000 ;FPN2 READ CYCLE
1440
```

(b)

```
1440
1480 REM  ---------------  ACTION AFTER INTERRUPT  -------------------
1490
1500 WTI CNTL,0,3            ; RECHARGE
1510 IF X#2 GO TO 1530
1520 GOSUB 8550             ; SET MEMORY FOR DATA IN
1530 EXIT
1540
1600 WTI CNTL,0,1            ; LSR PULSES ONLY
1610 EXIT
1620
1700 WTI CNTL,0,0            ; DISABLE
1710 EXIT
1720
1750 WTI CNTL,0,7            ; READ ( FREE RUNNING)
1760 EXIT
1770
1800 WTI CNTL,0,7            ; FPN1 READ CYCLE
1810 LET U(1)=X+1
1820 LET L=1
1830 EXIT
1840
1900 WTI CNTL,0,7            ; DOUBLE SAMPLE READ CYCLE
1910 LET U(3)=X+1
1915 LET N=X+I
1920 LET L=2
1930 EXIT
1940
1950 WTI CNTL,0,7          ; DOUBLE SAMPLE READ AFTER STOP SIGNAL
1955 LET U(3)=X+1
1960 LET N=X+I
1965 LET K=G
1967 LET L=2
1968 LET F=X-1
1970 EXIT
1980
2000 WTI CNTL,0,7            ; FPN2 READ CYCLE
2010 LET U(4)=X+1
2020 LET L=3
2030 EXIT
2040
2100 WTI CNTL,0,5          ; NDRO READ CYCLE
2110 DIS CNTL,3
2120 LET L=4
2130 LET U(2)=X+1
2140 EXIT
2150
```

(c)

```
2150
2490 REM ..........................................................
2500 REM                          MEMORY TRANSFER & DISPLAY OF FPNI
2510 IF X<=U(1) GO TO 2500;
2520
2530 GOSUB 8500                  ; ENABLE MEMORY FOR DATA OUT
2540
2550 FOR Q= 1 TO 512
2560 RDI MEMR,0,Z(Q)
2570 GOSUB 8600                  ; SCALE LEVELS
2580 NEXT Q
2590
2595 LET M(6)=U(1)-1
2600 LET R=0                     ; BLOCK IDENTIFIER
2610 LET B=0
2620 GOSUB 5000                  ; DISPLAY
2630 GOSUB 8550                  ; SET MEMORY FOR DATA IN
2660 LET L=0
2670 LET Y='7
2672 GOSUB 8750
2680
2685 LET M(8)=X
2687 LET F=X+E          ; SET UP END OF INTEGRATION
2690 GOTO 1185                ; RETURN TO MAIN PROGRAM
2700
2710 REM ..........................................................
2750 REM                          MEMORY TRANSFER OF NON DESTRUCTIVE READ
2760 IF X<=U(2) GO TO 2750
2765
2770 GOSUB 8500                  ;SET MEMORY TO DATA OUT
2775
2780 FOR Q= 513 TO 1024          ; TRANSFER TO COMPUTER MEMORY
2785 RDI MEMR,0,Z(Q)
2790 GOSUB 8600                    ; SCALE LEVELS
2795 NEXT Q
2796 LET M(10)=U(2)-1
2797 LET V=M(10)- M(8)
2798 FOR Q= 1 TO 3
2799 LET Y='13
2800 GOSUB 8750
2801 NEXT Q
2803 PRINT " NDRO AT",V
2804 FOR Q= 1 TO 4
2805 LET Y='16
2806 GOSUB 8750
2807 NEXT Q
2810 LET B=2                       ; SPLIT SPECTRUM DISPLAY
2812 LET R=1          ; BLOCK IDENTIFIER
2815 GOSUB 5000
2820 GOSUB 8550                    ; SET MEMORY FOR DATA IN
2821 ENB CNTL,3                   ; RE-ENABLE INTERRUPTS
2822 LET L=0
2825 IF X<F GO TO 1185
2830 PRINT "RATS!!!"             ; MISSED PROGRAMMED END OF INT.
2835 LET F=X+1
2840 GO TO 1185
2850
```

(d)

```
2850
2890 REM ..........................................................
3000 REM                              DOUBLE SAMPLE TRANSFER AND DISPLAY
3010 LET K=K+1
3012 IF K>=G GOTO 3020
3014 LET L=0
3016 LET F=X+E
3018 GO TO 1185
3020
3025 IF X<=U(3) GO TO 3020
3030 GOSUB 8500              ; ENABLE MEMORY FOR DATA OUT
3040
3050 FOR Q=1025 TO 1536
3060 RDI MEMR,0,Z(Q)
3070 GOSUB 8600              ; SCALE LEVELS
3080 NEXT Q
3090
3095 LET M(12)= U(3)-1
3100 LET R=2    ; BLOCK IDENTIFIER
3110 LET B=2
3120 GOSUB 5000              ; DISPLAY
3130 GOSUB 8550              ; SET MEMORY FOR DATA IN
3135 LET L=0
3140 IF X<N GO TO 3160
3150 LET N=X+1
3160
3220 GOTO 1185
3230
3490 REM ..........................................................
3500 REM                              FPN2 TRANSFER AND DISPLAY
3510 IF X<=U(4) GO TO 3500
3520
3530 GOSUB 8500              ; SET MEMORY FOR DATA OUT
3540
3550 FOR Q= 1537 TO 2048
3560 RDI MEMR,0,Z(Q)
3570 GOSUB 8600              ; SCALE LEVELS
3580 NEXT Q
3590
3595 LET M(14)=U(4)-1
3600 LET R=3
3610 LET B=0                 ; DISPLAY SELECTOR - RAW SPECTRUM
3620 GOSUB 5000
3650
```

(e)

```
3650
3690 REM ..........................................................
4000 REM                                  END OF RUN
4002
4010 DIS CNTL,0              ; DISABLE INTERRUPTS
4015 LET V=M(12)-M(8)
4020 PRINT "RETURN TO PRINT RUN DATA"
4021 WAIT
4022 PRINT ""
4023 PRINT ""
4025 PRINT ""
4026 PRINTH " INTEGRATION PERIOD                          ",M(4)
4027 PRINTH " NO. OF INTEGRATIONS                         ",M(5)
4030 PRINTH " FPN1 AT FRAME                               ",M(6)
4040 PRINTH " INTEGRATION BEGAN AT FRAME                  ",M(8)
4050 PRINTH " LAST NON DESTRUCTIVE READ AT                ",M(10)
4070 PRINTH " LAST INTEGRATION FINISHED AT FRAME          ",M(12)
4080 PRINTH " FPN2 AT FRAME                               ",M(14)
4090 PRINTH " "
4095 PRINTH " INTEGRATION PERIOD ( ACTUAL )               ",V
4100 PRINTH " "
4110 REM      SELECT DISPLAYS,DUMPS OR NEW RUN
4120 PRINT " DISPLAYS. FPN1=0,NDRO=1,DOUBLE SAMPLE=2,FPN2=3"
4130 PRINT " HARD COPY=4,LONG DUMP=5,SHORT DUMP=6,NEW RUN=7"
4140 INPUT R
4150 IF R<=3 GOTO 4180
4160 IF R=4 GOTO 4500
4162 IF R=5 GO TO 7000
4164 IF R=6 GO TO 7000
4166 IF R=7 GO TO 1080
4170 GO TO 4140
4175
4180 LET B=2
4185 LET J=0
4190 GOSUB 5000      ;    DISPLAY ROUTINE
4200 GO TO 4140
4500 REM        SELECT PRINTOUTS,DUMPS,OR NEW RUN
4510 PRINT "PRINTOUTS. FPN1=0,NDRO=1,D.SAMPLE=2,FPN2=3,REDUCED D.S=4"
4520 PRINT "DUMP RUN=5, DUMP REDUCED SPECTRUM ONLY=6, NEW RUN=7"
4530 INPUT R
4540 IF R<=4 GO TO 4600
4550 IF R=5 GO TO 7000
4560 IF R=6 GOTO 7000
4565 IF R=7 GO TO 1080
4570 GO TO 4530
4580
```

```
4580
4590 REM    ------------ PRINT DATA -----------
4600 LET S=R *512
4605 LET J=0
4610 PRINT "NO. OF POINTS?"
4620 INPUT G
4630 LET B=0
4640 PRINTH ""
4645 PRINTH ""
4650 PRINTH ""
4655 PRINTH "     BLOCK NUMBER=",R
4660 PRINTH ""
4661 IF R#4 GO TO 4665
4662 LET J=1
4663 GOSUB 6000
4664 LET S=0
4665 IF B<G GO TO4675
4667
4670 GO TO 4530
4675
4680 FOR Q=1 TO 4
4690 LET C= B+Q
4700 LET C=C+S
4705 IF J#1 GOTO 4710
4706 LET A(Q)=T(C)
4707 GO TO 4720
4710 LET A(Q)=Z(C)
4720 NEXT Q
4730
4740 LET C= B+1
4750 PRINTH C,":",A(1),A(2),"       ",A(3),A(4)
4760 LET B= B+4
4765
4770 GO TO 4665
4780
```

(g)

```
4780
5000 REM    ----------------------------  DISPLAY ROUTINES  ------------
5010
5020 WT1 MODE,0,1          ; ERASE DISPLAY
5030 TST MODE,0
5040 IF NOTQ GO TO 5030
5050 CL1 MODE,0
5060
5070 REM                     PLOT AXES
5080 F17 DRIVER,0,'2002    ; X-LINE MODE
5090 GOSUB 5800              ; Y=0
5100 GOSUB 5850              ; Y=1023
5110 IF B#2 GOT05130       ; SPLIT SPECTRA
5120 GOSUB 5900              ; Y=512
5130
5140 F17 DRIVER,0,'2003    ; Y-LINE MODE
5150 GOSUB 5800            ; X=0
5160 GOSUB 5850            ;X=1023
5170
5180 IF B=2 GOTO 5240
5190 F17 DRIVER,0,'210     ; FULL PAGE, X SCALE=512
5200 F9 DRIVER,1
5210 GOSUB 5600            ; 512 POINT SPECTRUM
5220 RETURN
5230
5240 REM                     SPLIT SPECTRUM
5250 GOSUB 6000            ; COMPUTE REDUCED SPECTRUM
5260
5270 F17 DRIVER,0,'10310 ; LOWER HALF PAGE, 512 POINTS
5280 F9 DRIVER,1
5290 GOSUB 5600            ; 512 POINT SPECTRUM
5300
5310 F17 DRIVER,0,'14120 ; UPPER HALF PAGE, 256 POINTS
5320 F9 DRIVER,1
5330 GOSUB 5700            ; 256 POINT SPECTRUM
5340 RETURN
5350
```

(h)

```
5360
5590 REM    ---------------------- DISPLAY SUBROUTINES ----------------
5595
5600 REM                                        512 POINT SPECTRUM
5610 LET S=R*512
5620 FOR Q=1 TO 512
5630 LET H=Q+S
5635 LET Y=4096-Z(H)
5640 F16 DRIVER,0,Y
5650 TLM DRIVER,0
5660 IF NOTQ GOTO 5650
5670 NEXT Q
5680 RETURN
5690
5700 REM                                        256 POINT SPECTRUM
5710 FOR Q=1 TO 256
5714 LET Y=T(Q)
5716 IF Y<1024 GO TO 5720
5718 LET Y=0
5720 F16 DRIVER,0,T(Q)
5730 TLM DRIVER,0
5740 IF NOTQ GOTO 5730
5750 NEXT Q
5760 RETURN
5770
5800 REM                                        LINE PLOT Y=0
5810 F16 DRIVER,0,0
5820 TLM DRIVER,0
5830 IF NOTQ GO TO5820
5840 RETURN
5845
5850 REM                                        LINE PLOT Y=1023
5860 F16 DRIVER,0,1023
5870 TLM DRIVER,0
5880 IF NOTQ GOTO 5870
5890 RETURN
5895
5900 REM                                        LINE PLOT Y=512
5910 F16 DRIVER,0,528
5920 TLM DRIVER,0
5930 IF NOTQ GO TO 5920
5940 RETURN
5950
```

```
5950
6000 REM   ----------------------------        NUMBER CRUNCHING ----------
6010 IF J#1 GOTO 6020
6012 LET R=2
6020 LET S=R*512
6030 FOR Q=1 TO 128
6040 LET H=Q-1
6050 LET H=H*4
6060 LET H=H+S
6070 LET H=H+3
6080 LET W(1)=Z(H)
6090 LET H=H+1
6100 LET W(2)=Z(H)
6120 LET H=H+1
6122 IF R#1 GOTO 6130
6124 LET H=H-S          ; FOR NDRO TAKE RESET LEVELS FROM FPN1
6130 LET P=Q*2
6140 IF Q#128 GOTO 6170
6150 LET T(P)=0
6160 GOTO 6180
6170 LET T(P)=W(2)-Z(H)
6172 IF Z(H)<W(2) GO TO 6180
6174 LET T(P)=0
6180 LET P=P-1
6182 IF R#1 GO TO 6190
6184 LET W(2)=Z(H)
6190 LET T(P)=W(1)-W(2)
6192 IF W(2)<W(1) GO TO 6200
6194 LET T(P)=0
6200 NEXT Q
6210 RETURN
6280
```

```
6290
7000 REM     ----------------------          PUNCH ROUTINE  ----------------
7001                                                    HEADER DEFINITION
7002 REM
7005
7010 REM     OUTPUT HEADER          FIRST CHAR= '177777
7012 REM                            M(1)=NO. OF WORDS IN DUMP
7014 REM                            M(2)=RUN NUMBER
7016 REM                            M(3)=INT.PERIOD (HI WORD)
7018 REM                            M(4)=INT.PERIOD (LO WORD)
7020 REM                            M(5)=NO. OF INTEG
7022 REM                            M(6)=FRAME NO. OF FPN1
7024 REM                            M(7)=INT BEGINS(HI)
7026 REM                            M(8)=INT BEGINS(LO)
7028 REM                            M(9)=LAST NDRO(HI)
7030 REM                            M(10)=LAST NDRO(LO)
7032 REM                            M(11)=DOUBLE SAMPLE(HI)
7034 REM                            M(12)=DOUBLE SAMPLE(LO)
7036 REM                            M(13)=FPN2(HI)
7038 REM                            M(14)=FPN2(LO)
7040 REM                            M(15)-M(20)   SPARE
7111
7112 LET J=0
7113
7114 IF R=6 GO TO 7118
7116 LET M(1)=2068      ; LONG DUMP
7117 GO TO 7120
7118 LET M(1)=276   ; SHORT DUMP
7119
7120 LET M(3)=M(4) & '77600000   ; SEPERATE 24 BIT VARIABLES INTO 2*16 B
7121 LET M(3)= M(3) DOWN 16
7122 LET M(7) = M(8) & '77600000
7123 LET M(7)= M(7) DOWN 16
7124 LET M(9) = M(10) & '77600000
7125 LET M(9) = M(9) DOWN 16
7126 LET M(11) = M(12) & '77600000
7127 LET M(11) = M(11) DOWN 16
7128 LET M(13) = M(14) & '77600000
7129 LET M(13) = M(13) DOWN 16
7130
7132 FOR Q= 15 TO 20
7134 LET M(Q)=0
7136 NEXT Q
7140
7160 PRINT "RUN NUMBER?"
7170 INPUT M(2)
7180
```

```
7180
7185 REM                                                    PUNCH TAPE
7186
7190 TST PUNCH,3        ; TEST FOR LOW TAPE
7200 IF NOTQ GOTO 7230
7210 PRINT " TAPE LOW "
7220 GO TO 4120
7230
7240 GOSUB 7800
7250 F26 PUNCH,1         ; PUNCH LEADER TAPE
7260 GOSUB 7800
7262
7264 F24 PUNCH,2        ; 16 BIT MODE
7266
7268 F16 PUNCH,0,'177777     ; PUNCH START CHARACTER
7270
7280
7290 FOR Q=1 TO 20
7300 GOSUB 7800
7310 F16 PUNCH,0,M(Q)
7320 NEXT Q
7330
7340 IF R=6 GO TO 7500
7350
7360 FOR Q= 1 TO 2048   ; PUNCH DATA
7370 GOSUB 7800
7380 F16 PUNCH,0,Z(Q)
7390 NEXT Q
7400 GO TO 7570
7410
7500 LET R=2
7510 GOSUB 6000          ; COMPUTE REDUCED SPECTRUM
7520 FOR Q =1 TO 256
7530 GOSUB 7800
7540 F16 PUNCH,0,T(Q)
7550 NEXT Q
7560
7570 GOSUB 7800
7580 F26 PUNCH,1   ; PUNCH TRAILER
7590 GOSUB 7800
7600 GO TO 4120
7610
```

```
7610
7620 REM    ----------------  SUBROUTINES ----------------------------
7630
7800 REM                          TEST PUNCH READY
7810 TST PUNCH,0
7820 IF NOTQ GO TO 7810
7830 RETURN
7840
8500 REM                                   SET MEMORY FOR DATA OUT
8505 DIS MEMR,0
8510 XEQ MEMR,1
8515 ENB MEMR,0
8520 RETURN
8540
8550 REM                                   SET MEMORY FOR DATA IN
8555 DIS MEMR,0
8565 XEQ MEMR,0
8575 RETURN
8595
8600 REM                                    SCALE DATA( 8 BIT PROGRAM ONLY)
8630 RETURN
8640
8750 REM              VDU ROUTINE
8760 TST VDU,2
8770 IF NOTQ GO TO 8760
8780 WT1 VDU,0,Y
8790 RETURN
8800
9000 REM    -------------------   FREE RUNNING   ----------------------
9010
9020 ENB CNTL,0
9030 REM                              CYCLE
9040 GOTO 9030
9050 TLM CNTL,2
9052 IF NOTQ GO TO 9060
9054 LET 0=2
9060 READ P
9070 IF P=0 GOTO 1700
9080 IF P=1 GOTO 1600
9090 IF P=3 GOTO 1500
9100 IF P=7 GOTO 1750
9110 RESTORE
9120 EXIT
9130 DATA 7,8
9140
9160 STOP
```

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