A thin film triode type carbon nanotube field emission cathode

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Abstract: The field electron emission of carbon nanotubes has been heavily studied over the past two decades for various applications, such as in display technologies, microwave amplifiers, and spacecraft propulsion. However, a commercializable lightweight and internally gated electron source has yet to be realized. This work presents the fabrication and testing of a novel internally gated carbon nanotube field electron emitter. Several specific methods are used to prevent electrical shorting of the gate layer, a common failure for internally gated devices. A unique design is explored where the etch pits extend into the Si substrate and isotropic etching is used to create a lateral buffer zone between the gate and carbon nanotubes. Carbon nanotubes are self-aligned to and within 10 microns from the gate, which creates large electric fields at low potential inputs. Initial tests confirm high field emission performance with an anode current density (based on total area of the device) of 293 μA cm^{-2} and a gate current density of 1.68 mA cm^{-2} at 250 V.

Keywords: carbon nanotube, field emission, electron emission, Spindt, triode

1. Introduction

The current technological age is embodied by a constant push for increased performance and efficiency of devices. This push is particularly observable for technologies that involve electron sources, such as spacecraft propulsion, electronic displays, and x-ray sources [1]. Efficiency of these systems can be increased by reducing weight and power consumption, but is often limited by a bulky and energy hungry electron source. This work explores the development of a low power, thin film electron source in a design that takes advantage of the unique material properties of carbon nanotubes (CNT).

Most electron sources utilize thermionic emission, which involves heating a metal filament to several thousand degrees Celsius in order to produce electrons

[1]. Thermionic emission sources possess inherent inefficiencies because they are relatively bulky and must be heated to very high temperatures, thus consuming more energy [2]. One alternative to thermionic emission is field electron emission (FE), which involves the application of electric fields at room temperatures to induce electron emission via tunnelling. Normally, large electric fields (100's of V μm^{-1}) are needed for FE [3], but this field is highly dependent on the electron source geometry, where sharp tips can reduce the macroscopic electric field needed. Since no heating is necessary, these sources can be much more efficient and reliable if emission can be achieved at a sufficiently low potential, providing marked improvement over current technologies [1, 2, 4].

Recently, the unique properties of conductive, high aspect ratio nanomaterials have been utilized to improve FE performance. One nanomaterial of interest is the CNT which has ideal properties for FE, including very high electrical conductivity, high temperature stability, chemical inertness, and a nanoscale geometry [5-7]. The first demonstration of the remarkable FE properties of CNTs was reported in 1994 [8], and thousands of papers have been published ever since [9]. Single CNT emitters are able to emit over a very large current range, roughly following Fowler-Nordheim behaviour and have a large maximum current of 0.2mA for a single CNT [10-12]. Some work has explored an internally gated CNT field emitter using a Spindt cathode-based design by separating a conductive substrate and gate with a dielectric layer [6, 13-15]. Even though this triode design has a lower emitter density, it is offset by higher field enhancement and less screening of the electrostatically isolated emission sites. In an ideal case, electron beam lithography can be used to create pits that have single or few CNTs within each pit [1, 13, 14, 16]. Even though CNT FE in this design is well studied, electrical shorting of the gate and non-scalable techniques have prevented the production of a commercializable internally gated CNT electron source.

This work develops an internally gated CNT field emitter using a Spindt cathode-based design specifically made to prevent shorting of the gate. A unique modification is explored where the etch pits extend into the Si substrate, which allows fabrication of a larger CNT-to-gate separation to prevent shorting while still allowing growth of longer CNTs, which are more uniform and reproducible than short (< 1μm) CNTs. In addition, isotropic etching is used to create a lateral

buffer zone between the gate and CNTs. The CNTs are self-aligned to and within 10 microns from the gate, creating large electric fields at the CNT tips at relatively low potentials (~100 V). This field emitter design can have a very low operating voltage in a compact package that enables portable electron source devices [1, 17].

2. Experimental

Arsenic doped silicon wafers with a resistivity of 0.001-0.005 Ω cm serve as the substrate and cathode contact. Thermally grown SiO_2 synthesized at 1,100°C for ~24 hours is used as the insulator and doped polycrystalline silicon (p-Si) is used as the gate. The 500 nm p-Si is deposited by low pressure chemical vapour deposition (LPCVD) at 588°C and 250 mTorr with a silane flow of 100 sccm for 90 minutes. The p-Si is doped with Techneglas (Perrysburg, OH) PhosPlus TP-470 solid source dopant by heating to 1,050°C for 1 hour followed by a drive-in anneal at 1,100°C for 30 minutes. These particular materials are chosen to maximize film quality while maintaining ease of fabrication. Thermal oxide deposits the best quality SiO_2 in terms of density, uniformity, purity, and dielectric breakdown. It has a theoretical dielectric breakdown of about 1,000 V μm^{-1}, which can be ten times higher than CVD SiO_2 [18]. High dielectric breakdown prevents degradation of the device during operation. The p-Si is used for its robustness and high temperature stability with SiO_2, preventing degradation during high temperature fabrication and operation.

A schematic of the fabrication process is shown in figure 1. The backside p-Si is removed after deposition by a short SF_6 plasma etch and the backside oxide is removed during wet etching of the front oxide. Standard ultraviolet lithography is used to pattern the substrate instead of higher resolution methods, such as electron beam lithography, in order to maintain scalable fabrication methods (figure 1(c)). AZ Electronic Materials (Stockley Park, UK) 3312 photoresist is spin coated at 3,000 RPM and baked at 95°C for 10 minutes. Photoresist exposure is at 365 nm and is developed in 300 MIF developer solution followed by a hard bake at 110°C for 10-20 minutes. Arrays of 4 μm diameter features across a 6x6 mm square are patterned on each die with a pitch ranging from 25-400 μm in a hexagonal pattern. Depending on pitch, a die will have 217-56,000 features.

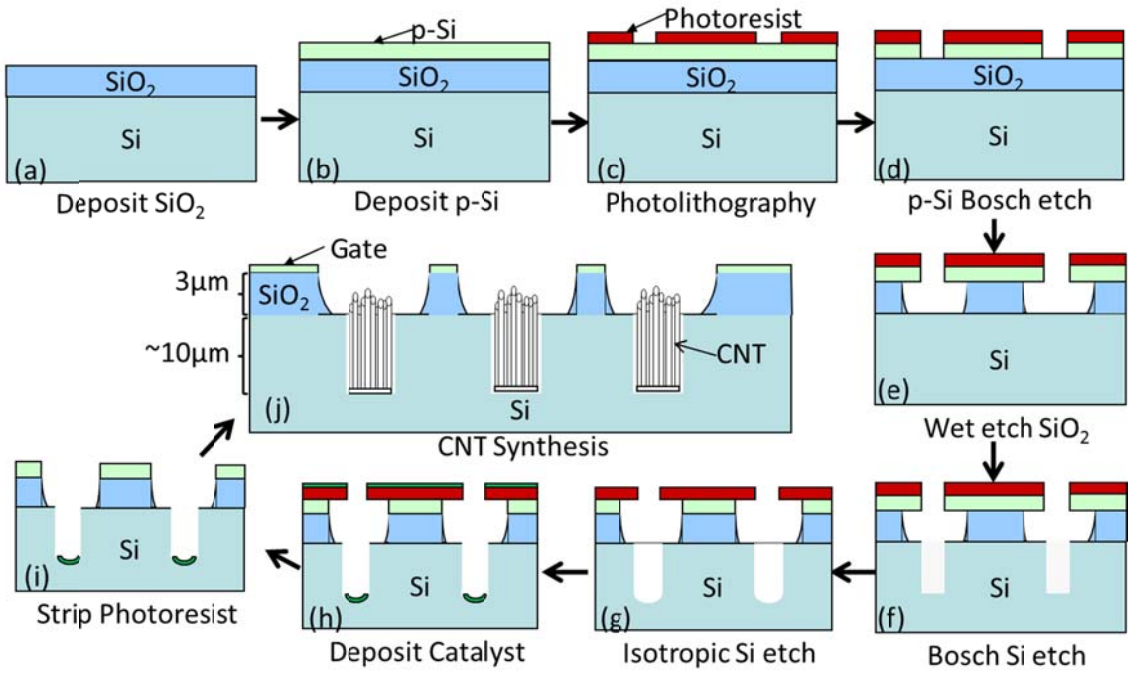

Fig. 1 Fabrication process flow for the internally gated CNT FE design

A Bosch etch process in an SPTS (Newport, UK) Deep Reactive Ion Etch (RIE) tool anisotropically etches the p-Si gate (figure 1(d)). The etch step is 5 seconds with SF_6 at 130 sccm and O_2 at 13 sccm, a pressure of 10 mTorr, and a coil power of 600 W with a platen power of 30 W. The passivation step is 4 seconds with C_4F_8 at 50 sccm. Approximately 8 cycles are needed. Standard isotropic plasma etching of p-Si does not achieve uniform etching due to the disparate etch rates of the crystal grains, which results in jagged sidewalls and loss of feature definition. The Bosch process is mainly used for its sidewall passivation, which results in smoother etch sidewalls. The etch has short cycle times to minimize sidewall roughness and achieve an anisotropic etch.

The SiO_2 is isotropically etched for 35 min in a buffered oxide etch (BOE) solution (6:1) using a magnetic stir bar (figure 1(e)). The SiO_2 is intentionally over etched so that the exposed Si substrate in each pit is larger than the photoresist aperture. A second Bosch etch is used to deepen the etch pits by etching into the Si substrate using a 7 second etch and 11 second passivation step for 30 cycles (figure 1(f)). This step is ideal as it increases the pit depth by 10 µm or more without significant removal of photoresist or increasing the insulation layer thickness. In addition, the Si walls in the pit enhance vertical alignment of

the CNTs due to steric hindrance. Interestingly, the Si pit diameter is determined by the size of the photoresist aperture and not by the amount of Si surface exposed, as shown by the unetched Si surface in figure 2(a).

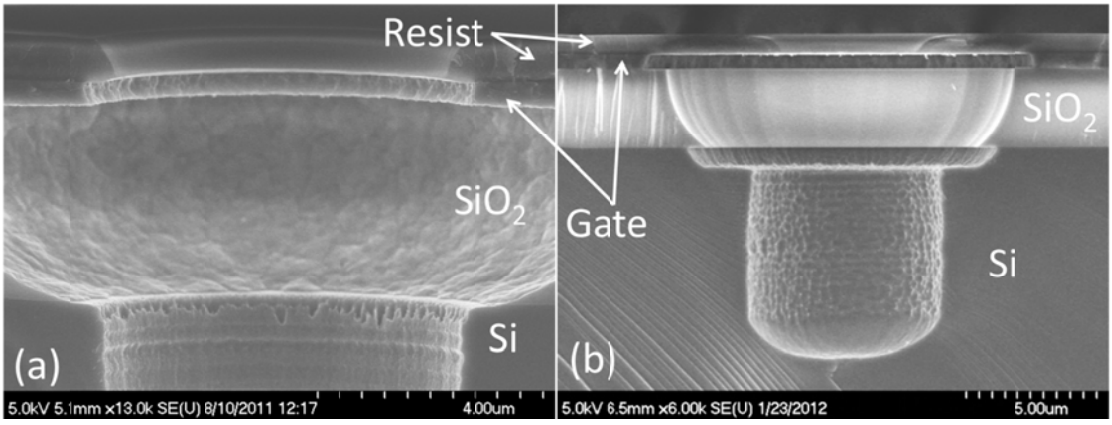

Fig 2 SEM cross section of etch geometry a) after Si Bosch etch, showing the slight over etch of SiO_2, the undercut p-Si, and a Si aperture that is larger than the photoresist aperture. b) After the lateral Si etch, showing the Si pit and lateral etch of the p-Si causing an overhang of the photoresist over the Si pit.

The isotropic oxide etch causes an undercut of the gate layer by several microns. An RIE process is used to simultaneously remove this undercut p-Si and increase the diameter of the Si pit (figure 1(g)). An Advanced Vacuum (Lomma, Sweden) Vision RIE is used at 70 W and 100 mTorr with 25 sccm of SF_6 and 5 sccm of O_2 for ~4 minutes. Etching the p-Si ensures that catalyst cannot deposit on the gate and results in a ~3 μm lateral buffer zone between the CNT growth and the gate sidewall, thus preventing an electrical short between the two (figure 3(c)). The Si pit is widened to prevent any catalyst deposition on the Si sidewalls and is consequently deepened to achieve a total pit depth of 15-20 μm. Typically the p-Si is etched about 100-200 nm past the p-Si/SiO_2 interface, where the close proximity of the layers hinders diffusion of reactive species and prevents further etching. It is this etch stop mechanism that minimizes the jagged etch profile that can occur from etching the p-Si. The final etch geometry is shown in figure 2(b).

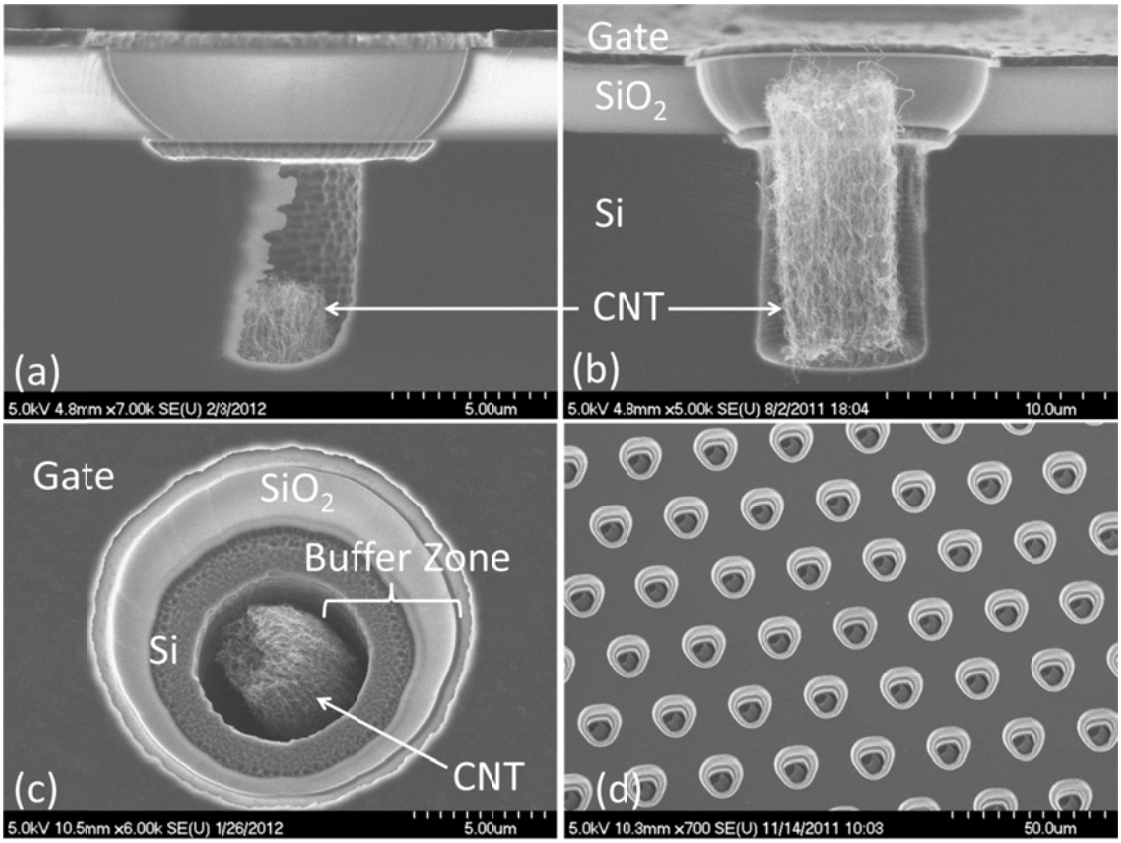

Fig 3 SEM of LPCVD CNT synthesis. Cross section image for (a) 20 sec and (b) 60 sec of CNT growth. 15° angle view of (c) a single pit showing CNT bundle and buffer zone between CNT and gate, and (d) relative uniformity of CNT growth across many pits

The fabrication process allows a line-of-sight path for deposition of the 3nm Fe catalyst layer directly on the base of the pit (figure 1(h)). Electron beam evaporation with an Angstrom Engineering (Kitchener, Canada) EvoVac system deposits catalyst at $< 1 \times 10^{-6}$ torr. The photoresist is removed by Baker (Phillipsburg, NJ) PRS 2000 photoresist stripper, leaving catalyst only in the Si pits (figure 1(i)).

An Aixtron (Herzogenrath, Germany) Black Magic plasma enhanced CVD (PECVD) tool is used for all CNT synthesis. PECVD CNT growth in this particular triode design is preferred due to the precise height control. This control is achieved by the driving force for CNT growth, a plasma, which can be instantly terminated by removing the electric field. PECVD can produce CNTs that are very well aligned at densities much lower than thermal CVD, whose alignment mechanism depends on dense growth [19]. This lower density will reduce the total field screening of a group of CNTs [20]. Therefore, the PECVD method was

initially pursued. However, PECVD caused arcing and shorting of the gate during the growth process due to the high potential (up to 700 V) of the plasma. Since the gate is electrically isolated from the substrate, it floats at the plasma potential, which causes arcing and damage across the sample electrode spacing. Shorting is not due to CNT growth since it occurred even if no carbon source was used.

To avoid arcing in the pits, LPCVD synthesis without plasma is used. It is much more difficult to uniformly synthesize short CNTs using LPCVD because the growth rate is normally much faster and there is no immediate removal of growth species. An LPCVD system with precisely controlled process parameters and recipe steps is used to produce uniform and consistent CNT growth. The LPCVD synthesis uses C_2H_2 and NH_3 or H_2 at 700°C and 10 mbar for 0.5-5 minutes. Annealing at 650°C for 15 minutes in NH_3 or H_2 ensures catalyst particle formation is uniform across the sample. A change in growth of as little as 15 seconds can create a large change in CNT length, showing precision is required. Figure 3 shows that the CNT growth can be precisely controlled, remains aligned past the Si pit, and is uniform across many pits. Raman spectroscopy shows marginal CNT quality with a D/G ratio of ~1.

FE testing is conducted in a vacuum chamber at $<1x10^{-6}$ torr in a triode design with the gate grounded, a negative bias on the cathode, and a +30 V bias on an anode 1.4 cm from the gate. Gate, cathode, and anode current are independently measured.

3. Results & Discussion

3.1. Electrical Shorting

Due to the nature of the integrated gate design, several methods are used to maintain the electrical isolation of the gate. First, it was found that the top gate layer can easily short to the substrate during wafer dicing, causing the gate to be electrically useless. A second lithography mask is used to expose the gate material around each die where dicing occurs. This allows the gate material in the dicing areas to be etched away before dicing, which prevents shorting of the gate.

Second, the catalyst is deposited such that the catalyst or subsequent CNT growth would not electrically short the gate. The catalyst is deposited by electron beam evaporation, which is a line-of-sight deposition process. Careful attention is

given to the angle of deposition because the angle correlates to a flux of material on the pit sidewalls. The angle is minimized by centering the sample over the source material and maximizing the distance between the source and substrate. In the tool used for this work, a 5 cm diameter sample has a variation of ±1.9°, which corresponds to a maximum 4% flux of material onto the sidewall. The pit geometry is carefully tuned such that the photoresist aperture is smaller than the gate, oxide, and Si pit apertures (figure 2). This resulting overhang ensures that the small angle of deposition is shadowed so that deposition only occurs in the bottom of the pit. For example, in the extreme case that a pit is 20 μm deep with a deposition angle of 1.9°, a 0.7 μm photoresist overhang is required to completely shadow the catalyst to the bottom of the pit. This overhang is achieved in the design described.

Finally, the pit geometry allows prevention of a short between the CNT and gate. The etch pits extend into the Si substrate, thus creating a larger electrode separation than would be possible by just using an oxide layer. This deeper pit allows for fabrication of a larger CNT-to-gate separation to prevent shorting while still allowing growth of longer, more reproducible CNTs. The lateral p-Si etch increases the diameter of the gate aperture without increasing the catalyst spot size. This etch essentially creates a buffer zone between the CNT growth and the gate sidewall, thus preventing a short between a CNT and the gate. This etch geometry is highly beneficial because the many thousands of features per sample increase the chances of having an abnormally long CNT that can short the entire sample by contacting the gate.

3.2. Field Emission

An initial FE test, shown in figure 4**,** demonstrates anode turn on (defined as 10 μA cm^{-2}) at 140 V and an electric field of 16 V μm^{-1}. In order to prevent electrical shorting, this sample has far from ideal CNT growth that is ~2 μm long. The electric field is approximated by estimating the spacing between the CNT and gate to be 9 μm. The sample produced a maximum anode current density of 293 μA cm^{-2} at 250 V with an active area of 0.347 cm^2. The maximum current density at the gate is much higher with 1.68 mA cm^{-2} at 250 V.

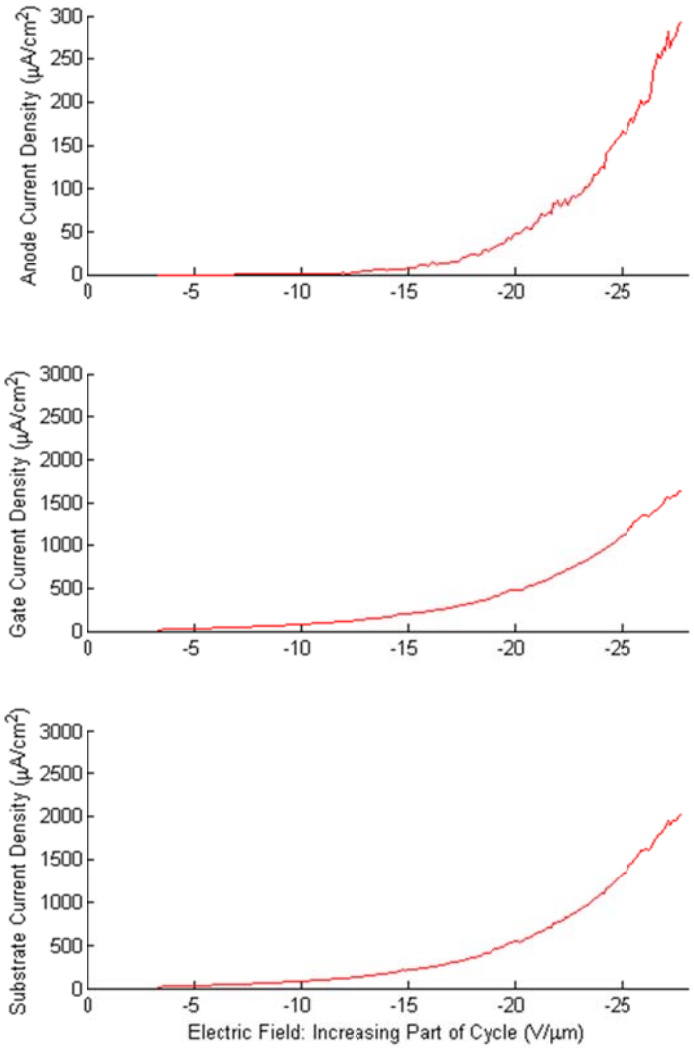

Fig 4 Initial field emission data for 0-250 V from a sample with short CNT growth and a 100 μm feature pitch. Anode, gate, and cathode current density are shown. Maximum anode current density is 293 μA cm^{-2} at 249 V, based off of total device area.

Analysis shows that on average 89% of the current goes to the gate, 8% to the anode, and 3% is lost (electrons not collected at the anode or gate). Thus, a majority of the electrons that make it past the gate are captured by the anode in the current configuration. Unfortunately, most of the electrons are captured by the gate. Since FE is occurring, it is assumed a majority of the gate current is from field emitted electrons with a small contribution of leakage current. The high proportion of gate current is attributed to the very short CNT growth, which gives a longer distance for the electrons to disperse into the gate. Typically, Spindt based cathodes that are fabricated with the emitter parallel to the gate have a much higher proportion of electrons captured by the anode [21]. If a higher proportion

of anode current can be achieved, then an effective CNT triode electron source may be realized, especially considering the pitch could be much smaller than the 100 μm feature pitch of the sample.

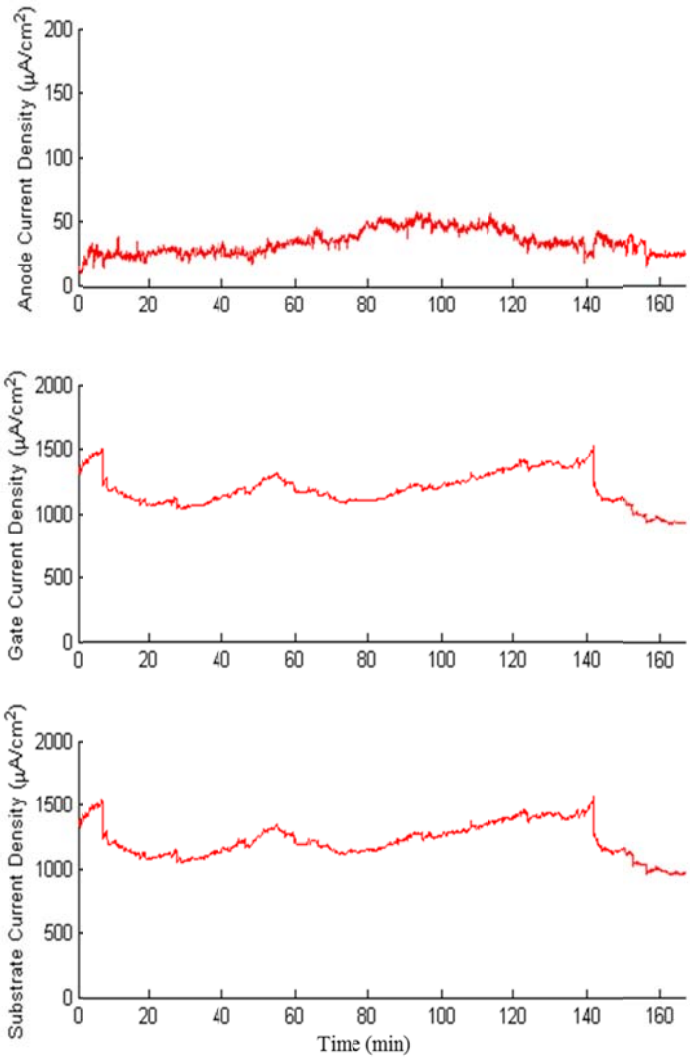

Fig 5 Constant voltage emission data for 75 μm pitch features with a constant potential of 220 V over 167 minutes shows unstable yet constant field emission over time.

Current density is reported in terms of actual area of the array and not the total area of CNT growth to give a realistic estimation of the density. However, this does not allow for comparison of the turn on field to other planar CNT electron sources. For the sake of comparison, current density calculated using just the CNT growth area gives a turn on at ~5 V μm^{-1} with a maximum current density of 360 mA cm^{-2}. This turn on field is slightly high compared to the 1-4 V

μm^{-1} that is observed in the literature for other CNT FE devices [22-24]. This could be due to the very short CNT growth and electrostatic screening of the electric field by the walls of the Si pit.

An example of constant voltage testing is shown in figure 5. A constant emission of < 50 $\mu A\ cm^{-2}$ at the anode and 1-1.5 $mA\ cm^{-2}$ at the cathode over 167 minutes is achieved. Significant instability is observed which makes it difficult to discern any gradual degradation. However, no sudden degradation is observed at the anode. This data shows that the emission can be sustained over extended periods.

Other CNT field emitters have a turn on potential that is normally much higher, ranging from ~150-2000V, due in part to larger electrode separations (such as in diode configurations) [22, 24-26]. The initial FE tests exhibit the capabilities of this triode design, demonstrating that a low voltage (140V) compared to other devices is needed for turn on. If electrical isolation can be maintained with longer CNT growth, a much lower turn on field and larger anode current should be achieved.

4. Conclusion

This work presents the fabrication process for an internally gated CNT field emitter using a Spindt cathode-based design. The fabrication process is thoroughly discussed, where several specific methods are used to prevent electrical shorting of the gate layer, a common failure for internally gated devices. A unique modification is explored where the etch pits extend into the Si substrate to allow fabrication of a larger CNT-to-gate separation to prevent shorting while still allowing growth of longer CNTs, which are more uniform and reproducible than short (< 1μm) CNTs. In addition, isotropic etching of the p-Si creates a buffer zone between the gate and CNT without increasing the CNT area, which helps prevent electrical shorting. CNTs that are self-aligned to and within 10 microns from the gate are synthesized, which enables large electric fields at the CNT tips at relatively low potentials (~100V). FE performance is confirmed with a current density of 293 $\mu A\ cm^{-2}$ at the anode and 1.68 $mA\ cm^{-2}$ at the gate, where current density is calculated from total area of the device. These results show that the design can achieve a very low operating voltage (250V) in a compact package that enables portable electron source devices.

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