E-MODE III-N HIGH-VOLTAGE TRANSISTOR DEVELOPMENT

1st-Year Final Project Report (Feb 2010 – March 2011)

Presented to Intersil Corp., Milpitas CA

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SUMMARY

During the first-year development (February 2010 – March 2011), we performed multiple subtasks to evaluate the feasibility of GaN HFETs for power electronics. For material characterizations, we conducted comparative study of high-voltage D-mode GaN HEMT epitaxial wafers grown on silicon substrates using various metrology tools and electric characterization methods such as th eatomic force microscope (AFM), X-ray diffraction, current-voltage (I-V) and capacitance-voltage (C-V) measurements. Seven wafers have been evaluated including INTS100512h1(h2), INTS100512h3, INTS100728h1(h2), and SN174001 coupons.

For D-mode GaN HEMT fabrication, we successfully demonstrated the state-of-the-art switching performance for GaN HEMTs on Si with a low specific on-resistance and ultra-high breakdown voltage characteristics. Fabricated 10-mm-wide GaN HEMTs (INTS100512h3) achieved the drain-to-source breakdown voltage (BV_{ds}) > 2,000 V with a specific on-resistance ($R_{ds(ON)}A$) of 5.4 mΩ-cm^2. These values are among one of the best results for GaN HEMTs on Si substrates reported to date. During the course of the study we also validated that GaN HEMTs with thin GaN cap layer are effective for achieving higher voltage breakdown characteristics.

In the E-mode device development, blanket *p*-type GaN and p-type AlGaN were fabricated and measured. The blanket *p*-GaN HEMTs exhibits *E*-mode operation (V_{th}= 0.2 V) and achieved $I_{d,max}$ = 140 mA/mm and $R_{ds(on)}$ = 24 Ω-mm at V_{gs} = 5V. Blanket *p*-AlGaN HEMTs were also fabricated. The devices demonstrated V_{th} = 0.2 V, $I_{d,max}$ = 100 mA/mm, and $R_{ds(on)}$ = 36 Ω-mm at V_{gs} = 2V. However, these devices do not provide sufficient current drive and exhibited significant gate leakage current, which should be further investigated.

The *p*-gate regrowth development are actively studied as well. As part of our efforts to build up the knowledge base of this novel approach, we observed several issues in this particular regrowth step, including possible residual silicon dioxide masking and rough regrowth surface on etched GaN surface, which may lead to inconsistency in the device

fabrication. These issues were actively studied in Year 1 and development efforts are continued in Year 2 from both material growth and fabrication processing development perspective. With a series of study on different surface preparation methods and plasma-induced surface condition changes, we were able to grow a 1-μm thick p-AlGaN layer with uniform surface morphology and window coverage. We are investigating the optimal regrowth conditions of a thinner p-(Al)GaN layer in Year 2 for possible p-GaN regrowth gate structure for E-mode device implementation.

We also focused on the recessed-gate approach for high-performance E-mode device implementation. A series of PEC recessing etching experiments showed that this approach is controllable and feasible. To extend the dynamic range and to reduce the on-state resistance in recessed-gate E-mode transistors, we also initiated the development of a metal-insulator-semiconductor (MIS) gate structure for GaN-based FETs. ALD-Al_2O_3 was chosen for the gate dielectric for the preliminary study and post-growth annealing conditions were investigated to further remove the hysteresis behavior in the C-V measurement.

Gate-recessed MIS-HEMTs with different etching time and gate dielectric layer bthicknesses were performed. The devices showed that a maximum drain current of 210 mA/mm can be achieved at V_{gs} = 7V with V_{th} = +0.1 V and a standard deviation of the threshold voltage = 65 mV. A study of GaN MIS-HEMTs on Si with a combination of different gate recessing depths and ALD-Al_2O_3 thicknesses was also performed. The preliminary results show that devices with thicker gate dielectric will shift the threshold voltage toward positive direction and extend the gate breakdown voltage. Further study will be required to extend the gate voltage swing and higher breakdown voltage in Year 2.

In parallel, a collaborative work with Intersil/Palm Bay facility to co-develop SiNx LPCVD passivation for GaN/AlGaN HEMTs was initiated in December 2010. The device performance with SiNx LPCVD passivation was evaluated and shows promising results with effective surface passivation to reduce the current collapse phenomenon in GaN HEMTs. These results from the first year development forms good knowledge base and viable paths to the E-mode GaN HEMT development for the 2nd year project.

PROJECT TIMELINE, MILESTONES, DELIVERABLES

A summary of research progress and status against proposed milestones and deliverables up to March 2011 is listed below.

WIP: Work in progress; initial results obtained, efforts extended to 4th quarter.

Achieved: Goal achieved;

NA: Work not fully engaged at the time of the report.

Milestone #1 (M1, 3rd MARO)

(a) Demonstrate first p-GaN SALEO HEMT growth completed. (**Achieved**)

(b) Demonstrate first-pass E-mode AlGaN/GaN HEMTs with $V_p \geq$ 0V, BV_{ds}> 800 V, $R_{sp(ON)}$< 10 mΩ•cm2 for two-fingered standard power transistor unit cells on sapphire substrates using recessed-gate approach. (**Achieved**)

(c) Complete first-pass E-mode AlGaN/GaN and InAlN/GaN HEMT designs. (**Achieved**)

Milestone #2 (M2, 6th MARO)

a) Demonstrate first P-type gate HEMTs (SALEO Gate, SEG Gate and or blanket P-GaN or P-AlGaN Gate epi layer as back-up options) through device fabrication and evaluation, with pinch-off voltage >-0.5V and I_{dsat}>0.3A/mm (**Achieved**)

b) Demonstrate enhancement-mode AlGaN/GaN HEMTs with Vth>0V, BV_{dss}>800 V, $R_{ds(on)}$ <2 ohm on sapphire substrates using recessed-gate approach (**Achieved,** less $R_{ds(on)}$ <2 ohm spec. -- WIP**)**

c) Complete 2D TCAD simulation set-up for P-type gate SALEO HEMTs analysis (**Achieved)**

d) Fabrication and evaluation of InAlN/GaN e-mode HEMTs (**NA**)

e) Complete first-pass comparative study of depletion-mode 10-Amp AlGaN/GaN HEMTs on Sapphire, Silicon and SiC substrates, with target performance as follows: BV_{ds} >1 kV, R_{dson} <0.5 ohms, Pinch-off voltage (Vpo) in the 3 to 5V range, Drain leakage (I_{dss}) of <10uA/mm at V_{gs} = -12V and Vds=800V (**Achieved,** less 10-Amp spec.)

Milestone #3 (M3, 9th MARO)

(a) Complete comparative analysis and fabrication compatibility study for AlGaN/GaN HFETs on both GaN or sapphire and GaN on Si platform with targeted performance for BV_{ds}> 1 kV, $R_{ds(ON)}$ < 0.3 Ω, $I_{leakage}$ < 1 μA/mm @ V_{gs} = -10V, and V_{ds} = 800 V. **(Achieved)**

(b) Down-select E-mode HFETs implementation approach for $V_p \geq$ 0V, BV_{ds}> 1 kV, R_{ON} < 0.3 Ω device demonstration on sapphire substrates. **(WIP)**

(c) Demonstrate AlGaN/GaN p-GaN SALEO HFETs with $V_p \geq$ 0V, BV_{ds}> 1 kV, $R_{ds(ON)}$ <10 mΩ•cm2 on 2" GaN on sapphire substrates. **(WIP)**

Milestone #4 (M3, 12th MARO)

(a) Demonstrate paths for high-quality uniform P-type gate (AlGaN or GaN) SALEO technology in MOCVD reactor for high-performance enhancement-mode FETs. **(WIP)**

(b) Demonstrate enhancement-mode III-N HEMT device technology with $V_{th} \geq$ 1V, BV_{ds}> 1 kV, $R_{ds(ON)}$ < 0.3Ω on 2" sapphire wafers using the approach or approaches determined in M3b) above. **(WIP)**

(c) Demonstrate enhancement-mode III-N HEMT simulation codes using ISE-TCAD (Sentaurus) platform. **(Achieved)**

I SUMMARY OF FIRST YEAR PROGRAM ACHIEVEMENT

The first year program is referred to as the "GaN Device Feasibility Evaluation Project." The Georgia Tech team built up the technical knowledge base for novel E-mode GaN HEMT on silicon with close collaboration with the Intersil engineering team. Using baseline device fabrication technology established at Georgia Tech, we also evaluate commercial wafers from epi-vendors and demonstrated the state-of-the-art D-mode GaN HEMTs on silicon platform. In particular, we achieved the following tasks:

1. Comparative study of GaN HEMT on silicon wafers from various external epi-vendors
2. Demonstration of the feasibility of GaN HEMTs and achieving the state-of-the-art D-mode III-N HEMT with $R_{ds(ON)} < 5$ mΩ-cm^2 for devices with $BV_{ds} > 1.1$ kV and $R_{ds(ON)} < 6$ mΩ-cm^2 for devices with $BV_{ds} > 1.8$ kV
3. Establishment of III-N HEMT TCAD simulation deck and new HEMT structure designs with AlGaN-based and InAlN-based HEMTs
4. Initial study on p-(Al)GaN regrowth SAG technique development
5. Developing high-voltage E-mode III-N HEMT using various gate-formation approaches such as blanket p-gate, recessed-gate MESFET, and recessed-gate MISFET processing to provide paths for E-mode HV HEMT implementation schemes down selection.
6. Initiating better III-N HEMT passivation technique with collaboration with Intersil's Palm Bay facility
7. Developing new InAlN-based HEMT structures for E-mode implementation and generating new IP for InAlN-based HEMTs.

One patent disclosure on two-layer InAlN-based HEMT structure design was filed and one conference paper was accepted to the 2011 CSMANTECH conference, one of the premium manufacturing conferences in the compound semiconductor industry. A summary of these development progress and achievements are described in the following subsections:

I.1 Comparative study of GaN HEMT on silicon

I.1.1 Material characterization of GaN HEMTs on silicon

In the past year, we have conducted a comparative study of high-voltage D-mode GaN HEMTs grown on silicon substrates. Material characterizations of the GaN HEMT on Si were carried out and the D-mode devices of various layer structures were fabricated. For the material characterizations, we have performed atomic force microscope (AFM), X-ray diffraction, and capacitance-voltage (C-V) profile on the GaN HEMTs on Si (seven wafers have been evaluated including INTS100512h1(h2), INTS100512h3, INTS100728h1(h2), and SN174001 coupons). The Mercury Probe was used for the C-V measurement on as-grown wafers. For each measurement, at least three points were taken on each wafer. A summary of these epi-layer characterizations are listed in Table 1.

Table 1. Material comparison chart for GaN HEMTs grown on Si

	Vendor 2			Vendor 5		
Wafer ID	**INTS100512h1**	**INTS100512h2**	**INTS100512h3**	**INTS100728h1**	**INTS100728h2**	**SN174001**
AFM	Non typical surface morphology	Non typical surface morphology	Normal surface morphology			
X-ray diffraction	Al %: 25% 3-points scan shows good uniformity	AlGaN peak overshadowed by 3rd peak	AlGaN peak overshadowed by 3rd peak			Al %: 23%
C-V profile	V_p : -5.7 V t(AlGaN)~ 40 nm Note: w/ buffer charge	V_p : -5.6 V t(AlGaN)~ 40 nm Note: w/ buffer charge	V_p : -4.0 V t(AlGaN)~ 40 nm Note: w/ buffer charge	V_p : -5.8 V t(AlGaN)~ 40 nm Note: model of uniformity	V_p : -5.6 V t(AlGaN)~ 40 nm	V_p : -3.2 V t(AlGaN)~ 20 nm

I.2 High-performance D-mode AlGaN/GaN HEMT on Silicon substrate

I.2.1 Wafer Processed: INTS100512h2, INTS100512h3, INTS100728h1, SN174001

I.2.2 Device Fabrication: Four wafers were processed for D-mode HEMTs in the preliminary study for the first year. The processing started with mesa isolation utilizing inductively coupled plasma (ICP). The contact resistance of Ti/Al-based ohmic contact is ~1.5 Ω-mm after annealing and 200-nm Ni was then evaporated as gate electrode. The devices were passivated with BCB-based polymer, followed by contact window opening and final overlay metal. A microscope photograph image of the fabricated AlGaN/GaN HEMTs power transistor was shown in Figure 1.

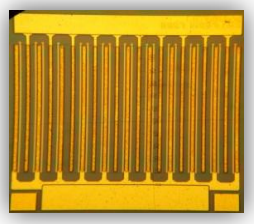


Figure 1. A microscope image of the fabricated multi-finger AlGaN/GaN HEMTs .

I.2.3 Measurement Setup:

The current-voltage (*I-V*) characteristics of AlGaN/GaN D-mode HEMTs on Silicon substrate were measured using Agilent 1505A curve tracer. For high-voltage measurement, we setup a simple measurement system using two 6-1/2 digital multi-meter for current sensing, one low-voltage power supply (up to 40 V), and one high-voltage power supply (up to 5 kV) for high-voltage characterization, as shown in Figure (2). The minimal detectable current is 10 nA for the digital multimeters used in this measurement. The drain leakage current is assessed as the sum of the gate leakage current and the source leakage current.

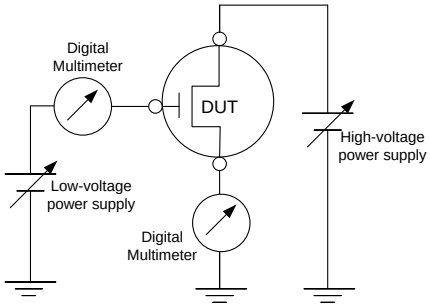
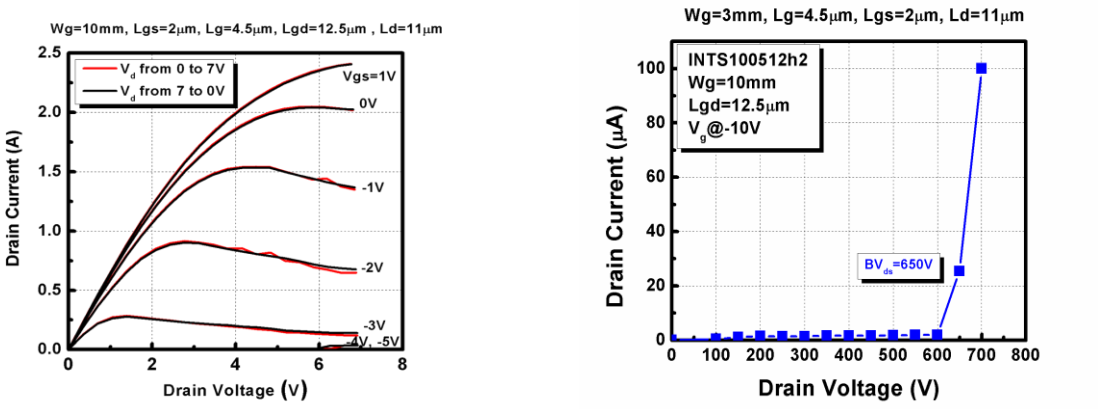


Figure 2. A schematic system setup for a preliminary high-voltage GaN transistor measurement.

I.2.4 Device Characteristics:

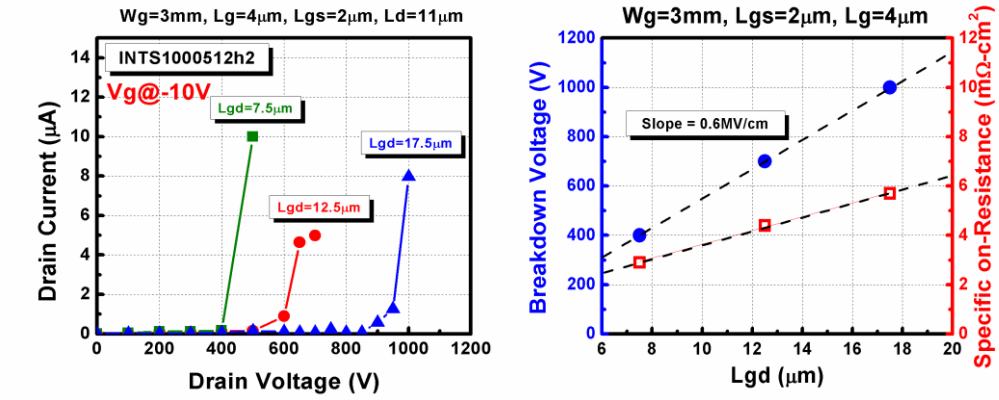
a) INTS100512h2: The DC characteristics for AlGaN/GaN HEMTs (Wafer ID: INTS100512h2) are shown in Figure 3 (a). The device has a dimension of gate width (W_G)= 10 mm and gate-to-drain distance (L_{GD}) = 12.5 µm. The maximum drain current of > 2 A is measured at V_{gs} = 1 V. The threshold voltage and I_{dss} are -4.7 V and 200 mA/mm, respectively. The threshold voltage is defined at the gate voltage where I_d = 1 mA/mm. The $R_{ds(ON)}A$ is estimated to be 4.1 mΩ-cm^2 at V_{gs} = 0 V, where A is defined as the total mesa etched area. The gate-to-drain breakdown voltage is measured in a fluorinert environment to prevent the arcing. As shown in Figure 3 (b), the device shows BV_{ds} = 650 V.



(a) **(b)**

Figure 3. (a) The on-state and (b) off-state characteristics for an AlGaN/GaN HEMTs (INTS100512h2) with W_G=10mm and L_{GD}=12.5µm.

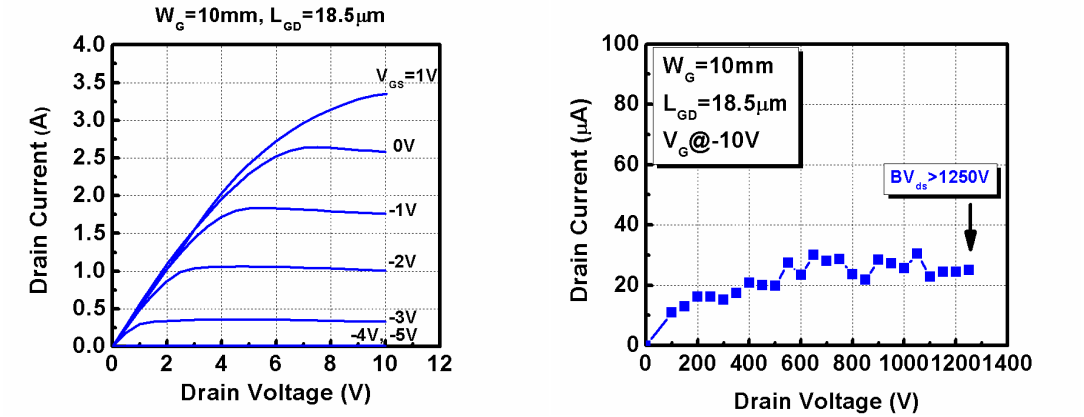
The lateral device scaling was also studied for devices with W_G = 3 mm. As shown in Figure 4 (b), the breakdown voltage scales linearly with the increase in the L_{GD}. As L_{GD} increases from 7.5µm to 17.5µm, BV_{ds} increases from 400 V to 1000 V. The corresponding breakdown electric field of these devices is ~0.6 MV/cm. The $R_{ds(ON)}A$ also scales linearly with L_{GD}, from 2.9 mΩ-cm^2 to 5.7 mΩ-cm^2, as shown in Figure 4 (b).



(a) **(b)**

Figure 4. (a) The off-state performance for AlGaN/GaN HEMTs (INTS100512h2) with W_G =3mm, L_{GD}=7.5, 12.5, and 17.5 µm, respectively. The gate-to-source voltage is -10 V. (b) A plot showing the scaling effect of the breakdown voltage (blue circle) and Specific on-resistance (red square) for fabricated AlGaN/GaN HEMTs on silicon. The measured devices have W_G= 3 mm.

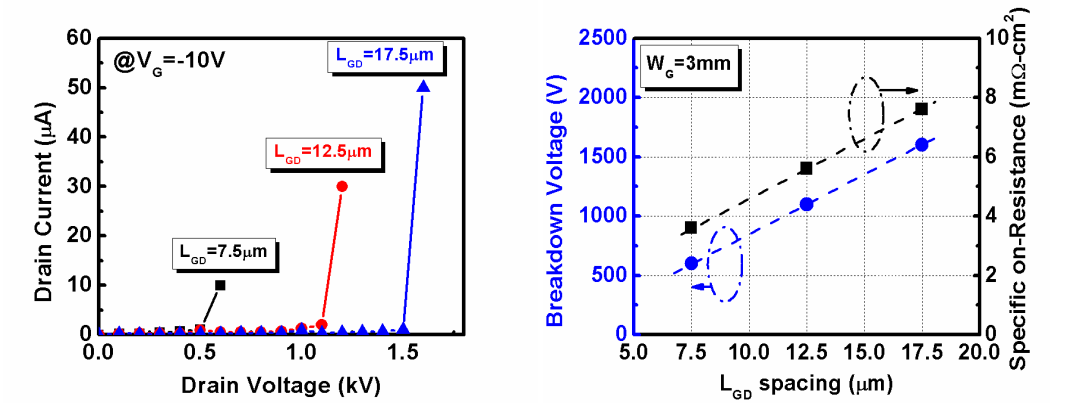
INTS100728h1: The DC characteristics for AlGaN/GaN HEMTs (W_G = 10 mm, L_{GD}= 18.5 µm) are shown in Figure 5 (a). At V_{gs} = 1 V, the maximum current of > 3 A is achieved. The threshold voltage and I_{dss} are -4.6 V and 265 mA/mm, respectively. The $R_{ds(ON)}A$ is estimated to be 6.2 mΩ-cm^2 at V_{gs} = 0 V. The gate-to-drain breakdown voltage is also measured. As shown in Figure 5 (b), the device shows BV_{ds} of greater than 1.25 kV.



(a) **(b)**

Figure 5. (a) The on-state and (b) off-state characteristics for an AlGaN/GaN HEMTs (INTS100728h1) with W_G=10mm and L_{GD}=18.5µm.

The lateral device scaling is also investigated for 3-mm-wide devices. As shown in Figure 6 (b), the breakdown voltage scales linearly with the increase in the L_{GD}. As L_{GD} increases from 7.5µm to 17.5µm, BV_{ds} increases from 600 V to 1600 V. The corresponding breakdown electric field of these devices is ~1.0 MV/cm. The $R_{ds(ON)}A$ scales linearly with L_{GD}, from 3.6 mΩ-cm^2 to 7.2 mΩ-cm^2, as shown in Figure 6 (b).

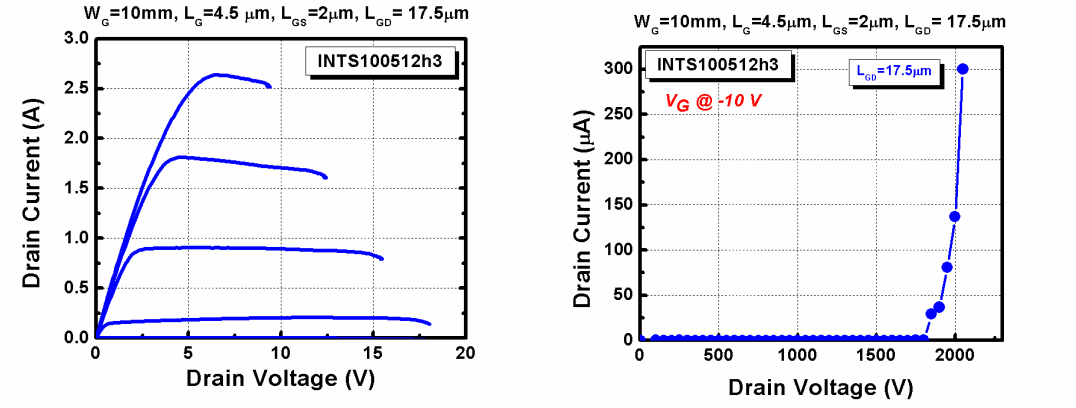


(a) **(b)**

Figure 6. (a) The off-state performance for AlGaN/GaN HEMTs (INTS100728h1) with W_G =3mm, L_{GD}=7.5, 12.5, and 17.5 µm, respectively. The gate-to-source voltage is -10 V. (b) A plot showing the scaling effect of the breakdown voltage (blue circle) and Specific on-resistance (black square) for fabricated AlGaN/GaN HEMTs on silicon. The measured devices have W_G= 3 mm.

INTS100512h3: The AlGaN/GaN HEMTs consists of an additional thin GaN cap layer grown on standard FET structure. DC characteristics for the device with W_G = 10 mm, L_{GD}

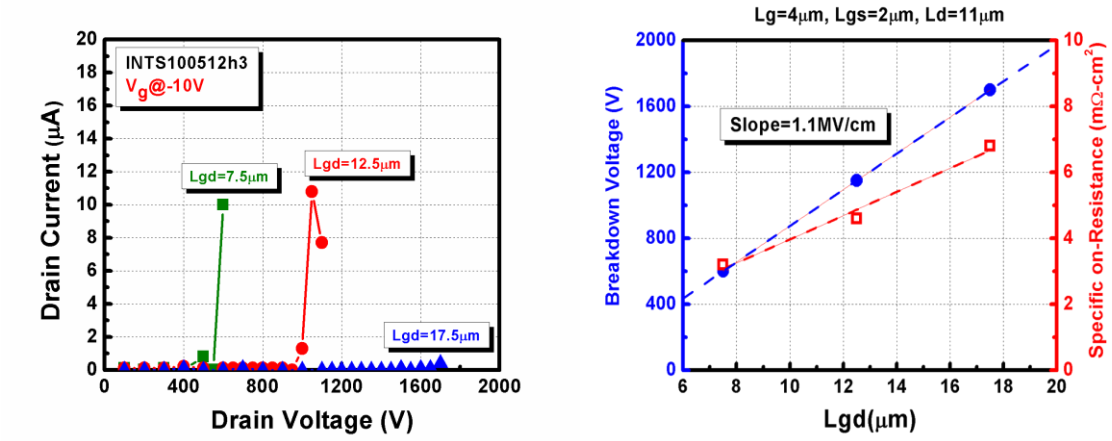
= 17.5 µm are shown in Figure 7 (a). The maximum current of ~ 2 A is measured at V_{gs} = 1 V. The threshold voltage and I_{dss} are -3.2 V and 175 mA/mm, respectively. The $R_{ds(ON)}A$ is estimated to be 5.4 mΩ-cm^2 at V_{gs} = 0 V. As shown in Figure 7 (b), the device shows BV_{ds} > 1.8 kV.



(a) **(b)**

Figure 7. (a) The on-state and (b) off-state characteristics for an AlGaN/GaN HEMT (INTS100512h3) with W_G=10mm and L_{GD}=17.5µm.

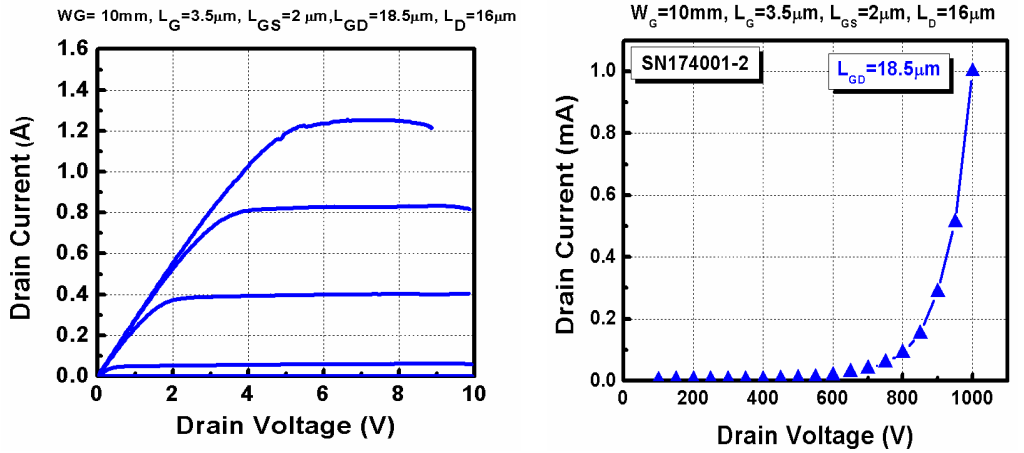
The lateral device scaling was investigated for devices with W_G = 3 mm. As shown in Figure 8 (a), BV_{ds} scales linearly with the increase in L_{GD}. As L_{GD} increases from 7.5µm to 17.5µm, BV_{ds} increases from 600 V to 1750 V. The corresponding breakdown electric field of these devices is ~1.1 MV/cm. The $R_{ds(ON)}A$ scales linearly with L_{GD}, from 3.2 mΩ-cm^2 to 6.8 mΩ-cm^2, as shown in Figure 8.



(a) **(b)**

Figure 8 (a) The off-state performance for AlGaN/GaN HEMTs with W_G =3mm, L_{GD}=7.5, 12.5, and 17.5 µm, respectively. The gate-to-source voltage is -10 V. (b) A plot showing the scaling effect of the breakdown voltage (blue circle) and Specific on-resistance (red square) for fabricated AlGaN/GaN HEMTs on silicon. The measured devices have W_G= 3 mm.

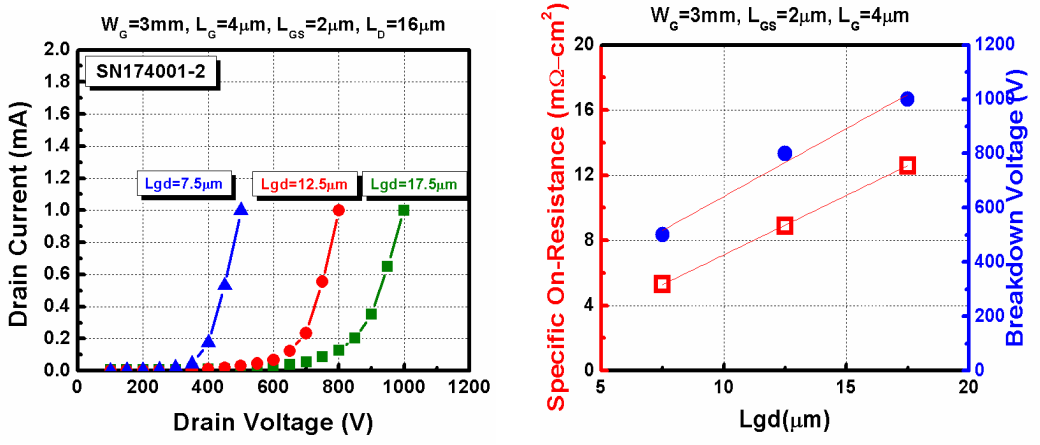
SN174001: The SN174001 device structure consists of a 4-nm-GaN cap layer grown on standard FET structure. The DC characteristics for a device with W_G = 10 mm and L_{GD} = 18.5 µm are shown in Figure 9 (a). The maximum current of ~ 1.2 A is measured at V_{gs} = 1 V. The V_{th} and I_{dss} are -2.5 V and 80 mA/mm, respectively. The $R_{ds(ON)}A$ is 15 mΩ-cm^2 at V_{gs} = 0 V. The gate-to-drain breakdown voltage is shown in Figure 9 (b). The device exhibits soft BV_{ds} at 1 kV.



(a) (b)

Figure 9. (a) The on-state and (b) off-state characteristics for an AlGaN/GaN HEMT (SN174001) with W_G=10mm and L_{GD}=18.5µm.

The lateral device scaling is also investigated for devices with W_G = 3 mm. As shown in Figure 10 (a), the breakdown voltage also scales linearly with the increase in the L_{GD}. As L_{GD} increases from 7.5µm to 17.5µm, BV_{ds} increases from 500 V to 1000 V. The corresponding breakdown electric field of these devices is ~0.5 MV/cm. The $R_{ds(ON)}A$ also scales linearly with L_{GD}, from 5.3 mΩ-cm^2 to 12.6 mΩ-cm^2, as shown in Figure 10 (b).



(a) (b)

Figure 10 (a) The off-state performance for AlGaN/GaN HEMTs (SN174001) with W_G =3mm, L_{GD}=7.5, 12.5, and 17.5 µm, respectively. The gate-to-source voltage is -10 V. (b) A plot showing the scaling effect of the breakdown voltage (blue circle) and Specific on-resistance (red square) for fabricated AlGaN/GaN HEMTs on silicon.

A performance comparison chart for the fabricated D-mode GaN HEMTs on Si is summarized in Table 2. The devices evaluated here have the same design parameters: W_G= 3 mm, L_{GS}= 2 µm, L_G= 4 µm, L_{GD}= 17.5 µm.

Table 2. Comparative performance chart for the fabricated D-mode HEMTs on Si

Wafer ID	*INTS100512h2*	*INTS100512h3*	*INTS100728h1*	*SN174001*
Layer structure	AlGaN: 30 nm (Al: 25%) GaN: 4.0 µm	GaN cap: 1 nm AlGaN: 30 nm (Al: 25%) GaN: 4.8 µm	AlGaN: 30 nm (Al: 25%) GaN: 4.8 µm	GaN cap: 4 nm AlGaN: 30 nm (Al: 25%) GaN: 4.8 µm
AFM result	Non typical surface morphology	Normal surface morphology		
X-ray diffraction	AlGaN peak overshadowed by 3rd peak	AlGaN peak overshadowed by 3rd peak		Al %: 23%
C-V profile	V_p: -5.6 V t(AlGaN)~ 40 nm Note: w/ buffer charge	V_p: -4.0 V t(AlGaN)~ 40 nm Note: w/ buffer charge	V_p: -5.8 V t(AlGaN)~ 40 nm Note: uniformity issue	V_p: -3.2 V t(AlGaN)~ 20 nm
Rs (Ω/sq)	394	527	461	700
ρ_c (Ω-mm)	1.5	0.3	1.5	1.5
V_{th} (V)	-4.7	-3.2	-4.6	-2.5
I_{dss} (A) @ V_G= 0 V	0.76	0.47	0.7	0.3
I_{dmax} (A) @ V_G= 1 V	0.83	0.67	0.8	0.48
$R_{ds(on)}$ (Ω)	5.3	6.3	6.7	10.1
$R_{ds(on)}$*A (Ω-cm^2)	5.7	6.8	7.2	12.6
BV_{dss} (V)	1000	> 1750	1600	1000

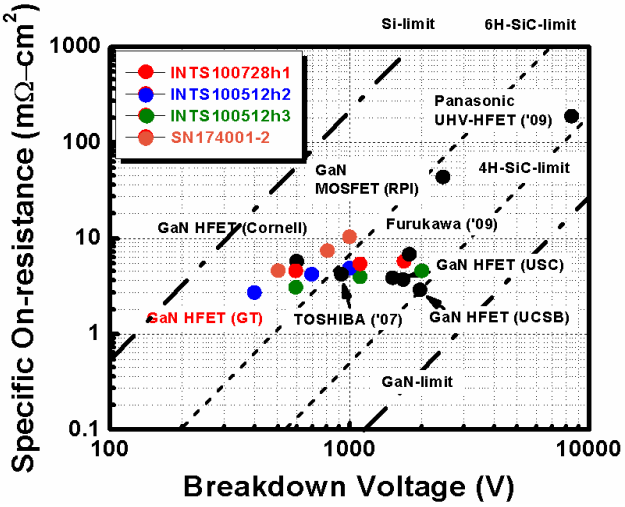


Figure 11. Breakdown voltage versus specific on-resistance for Si, and GaN devices on silicon (Furukawa, GT), GaN (Cornell), and sapphire (TOSHIBA, Panasonic, UCSB, USC, RPI) substrates.

Figure 11 shows a competitive performance comparison chart by plotting the $R_{ds(ON)}A$ versus the breakdown voltage for high-voltage GaN HEMTs [1-8]. When operating at V_{ds} > 800 V, it is clear that GaN HEMTs show a drastic reduction of the on-state resistance by at least a factor of 100 when compared to silicon counterparts. GaN HEMTs reported in this work are among the best high-voltage device performance achieved for GaN-on-silicon power transistors. Further processing development and device performance evaluation will be reported in the conference.

It is also noted that no field plates were included in the first-year study. According to the literatures, it has been found that the breakdown voltage can be improved by utilizing the field plate technology, which reduces the electrical field at the gate edge and, hence, the breakdown voltage can be increased. In addition, with reduction of gate length and contact resistance, it is expected that the trade-off characteristics between the breakdown voltage and the on-resistance could be further improved in the future. The optimized design of field plate should be studied.

I.3 TCAD simulation

The TCAD simulation for GaN HEMTs has been established at GT. In the 1st year, we studied standard D-mode HEMT structures, the impacts of AlGaN barrier thickness, Al mole fraction, and the dopant concentration in GaN buffer layer, etc. In addition, we setup the E-mode III-N HEMT simulation and focused on three major implementations, i.e., the recessed-gate MIS, p-gate HEMTs, and novel InAlN-based HEMTs. For the recessed-gate MIS structure, we investigated the impact on I-V characteristics with different recessing depth and Al_2O_3 gate dielectric thickness. It is found that the threshold voltage shift follows 0.16 V/nm trend in the simulation, which results will require further experiment validation and follow-up parameter modifications. For p-gate HEMTs, the E-mode operation could be achieved with the p-AlGaN doping concentration greater than 5×10^{18} cm^{-3} in the simulation. The optimization in the modeling for the dielectric and the interplay of the dielectric thicknesses and recess etching depths will need to be studied. The trap density and trap energy with different dielectric thickness at the interface will be also investigated in Year 2.

I.3.1 TCAD simulation for D-mode AlGaN/GaN HEMTs

The D-mode AlGaN/GaN HEMTs structure used in the TCAD simulation is shown in Figure 12. The un-intentional doping concentration for ud:GaN and ud:AlGaN layers are $1x10^{15}$ cm^{-3} and $1x10^{13}$ cm^{-3}, respectively. Starting from the standard AlGaN/GaN HEMT structure, the impacts of AlGaN barrier thickness, Al mole fraction, GaN dopant concentration, and device scaling will be summarized in the following subsections:

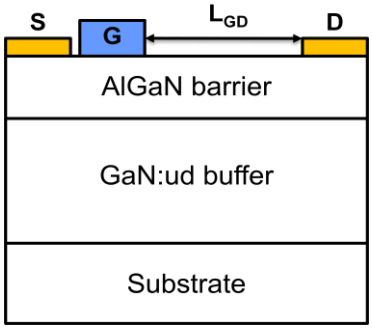
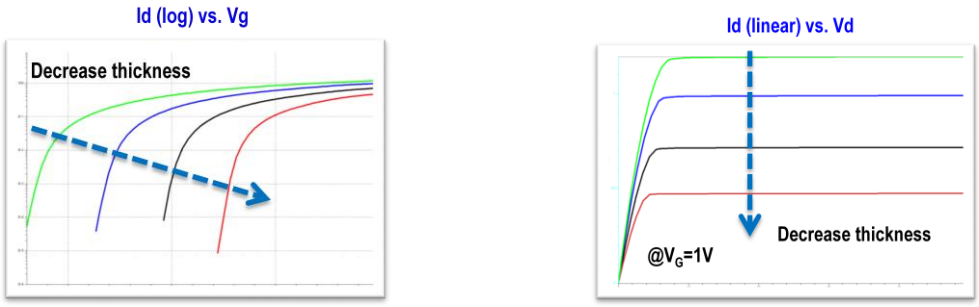


Figure 12. The schematic diagram of standard AlGaN/GaN HEMT structure.

I.3.1(a) Impact of AlGaN barrier thickness:

The AlGaN barrier thickness varies from 15 nm to 30 nm in the simulation. A constant Al mole fraction is set to be 0.2. Figure 13 shows the simulated drain

current (in log scale) plotting against the gate voltage. With reducing the AlGaN thickness, the threshold voltage is shifted toward the positive direction. However, the resultant drain current would decrease as well. The summary is shown in the Table 3.



(a) **(b)**

Figure 13. (a) The I_D-V_G (log scale) and (b) I_D-V_D characteristics for an AlGaN/GaN HEMT with different AlGaN thickness.

Table 3. Summary of the AlGaN/GaN HEMT with different AlGaN thickness.

t(AlGaN) (nm)	Al mole fraction	Threshold voltage (V)	I_{max} (mA/mm) @ V_G=1V	R_{on} (Ω) @ V_G=0V
10	0.2	-0.4	80	8.3
15	0.2	-1.6	180	5
20	0.2	-2.8	250	3.7
25	0.2	-4.2	320	3.2

I.3.1(b) Impact of AlGaN mole fraction:

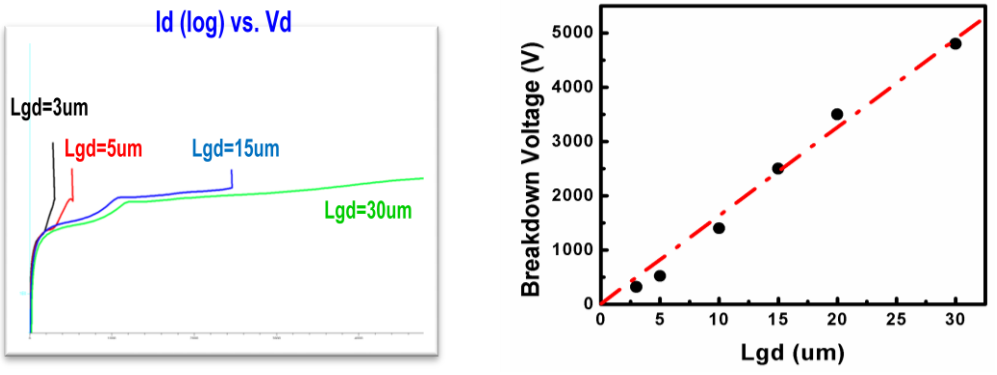
Second, the Al mole fraction in the AlGaN barrier layer is varied from 0.15 to 0.3. The AlGaN barrier thickness is fixed at 25 nm. I-V curve simulations show the threshold voltage is shifted toward more positive values with the reduction in the Al mole fraction However, the resultant drain current would decrease as well. The summary is shown in Table 4.

Table 4 Summary of the AlGaN/GaN HEMT with different Al mole fraction.

t(AlGaN) (nm)	Al mole fraction	Threshold voltage (V)	I_{max} (mA/mm) @ V_G=1V	R_{on} (Ω) @ V_G=0V
25	0.15	-3	220	4.8
25	0.2	-4.2	320	3.3
25	0.25	-5.5	400	2.5
25	0.3	-6.7	540	2

I.3.1(c) lateral scaling of breakdown voltage characteristics:

According to the literature study, it is suggested that the breakdown voltage is related to L_{GD}, deep level concentration, and the GaN buffer thickness. The lateral scaling of breakdown voltage is simulated by changing L_{GD} spacing from 3 um to 30 um. Figure 14 showed the BV_{ds} versus $L_{GD.}$ As L_{GD} increases from 3 μm to 30 μm, BV_{ds} increases from 320 V to 4.6 kV. The corresponding breakdown electric field is estimated to be ~1 MV/cm. A summary of the simulation results is shown in Table 5.



(a) **(b)**

Figure 14. (a) on-state I_D-V_D characteristics (in log scale) for an AlGaN/GaN HEMT with different L_{GD} spacing. (b) on-state breakdown voltage with respect to different L_{GD} spacing.

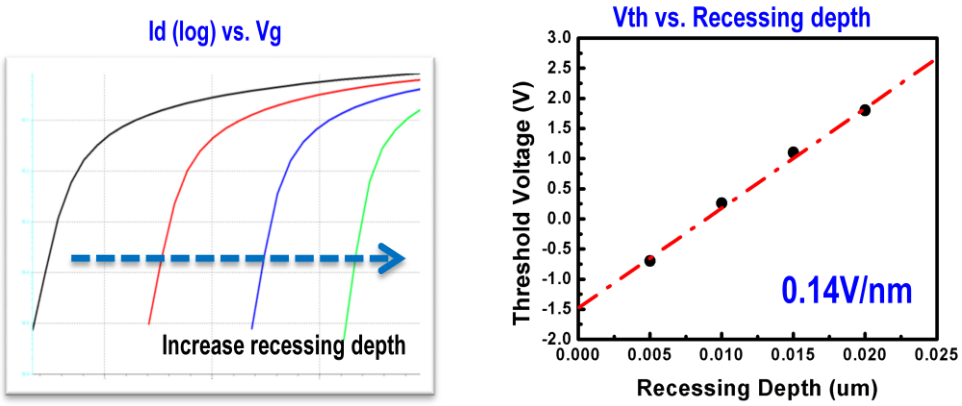
Table 5. Summary of the on-state breakdown voltage with respect to different L_{GD} spacing

t(AlGaN) (nm)	Al mole fraction	L_{GD} (μm)	Breakdown voltage (V)
20	0.2	3	320
20	0.2	5	520
20	0.2	15	2400
20	0.2	30	> 4600

I.3.2 TCAD simulation for AlGaN/GaN gate-recessed HEMTs

I.3.2(a) AlGaN/GaN gate-recessed HEMTs with schottky gate electrode

The characteristics of gate-recessed HEMTs with Schottky gate metal were evaluated in Santaurus TCAD. The thinning of AlGaN barrier layer in the gate region decreases the 2DEG while keeping the low resistance in the rest of the drift region. In this simulation, the AlGaN barrier layer has 20% of Al mole fraction and has a thickness of 30 nm. The recessing depth varies from 5 nm to 20 nm. Figure 15 (a) shows the drain current in log scale, plotting as a function of the gate voltage. Figure 15 (b) shows the threshold voltage versus recessing depths. It is observed that the threshold voltage shift is linear with a slope of 0.14 V/nm.

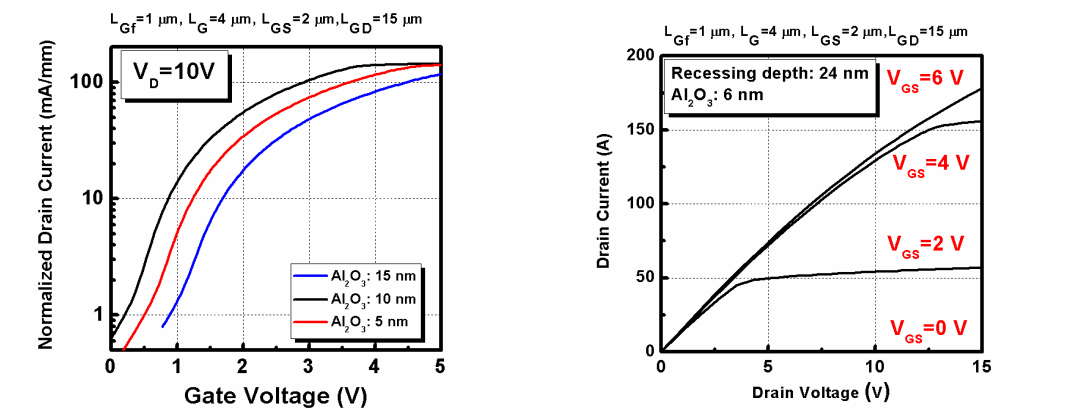


(a) **(b)**

Figure 15. (a) on-state I_D-V_G characteristics (in log scale) for a gate-recessed AlGaN/GaN HEMT with different recessing depth. (b) Threshold voltage with respect to different recessing depth.

I.3.2(b) AlGaN/GaN gate-recessed MIS-HEMTs with Al_2O_3 insulating layer

In order to extend the operable gate voltage range, the MIS-structures were investigated by the TCAD simulation as well. The layer structure consists of 30 nm-thick AlGaN barrier and 2 µm-thick GaN buffer. The impact of the recess depth and Al_2O_3 dielectric thickness were studied in the simulation. The devices dimensions under evaluation are L_{GD} = 15 µm, L_G = 1 µm, and L_{GS} = 2 µm. The Al_2O_3/AlGaN interface charge density is fixed at 1.4×10^{13} cm^{-2}. Figure 16(a) shows the I_d–V_{gs} characteristic at V_D = 10 V with 24-nm gate recessing and different Al_2O_3 dielectric thickness. V_{th} changed from 0.2 V to 0.9 V with increasing dielectric thickness. Figure 16 (b) shows the simulated I_d–V_{ds} of a device with 24 nm gate-recess depth and a 6 nm-thick Al_2O_3 dielectric layer. The $R_{ds(on)}$ can be calculated to be is 65 Ω-mm at V_{gs} = 6 V. The summary of this study is shown in Table 6.



(a) **(b)**

Figure 16 (a) on-state I_D-V_G characteristics (in log scale) for a gate-recessed AlGaN/GaN MIS-HEMT with different dielectric thickness. The recessing depth is 24 nm. (b) on-state I_D-V_D characteristics for a gate-recessed AlGaN/GaN MIS-HEMT. The gate-recessing depth and the dielectric thickness are 24 nm and 6 nm, respectively.

Table 6. Summary of gate-recessed MIS-HEMTs with different recessing depths and Al_2O_3 thicknesses

Recessing depth (nm)	Al_2O_3 Thickness (nm)	V_{th} (V)	Id_{Max} (mA/mm) @ V_G=6V
24	6	0.2	162
24	10	0.5	200
24	15	0.9	210
27	10	1.45	142
27	15	1.8	280
29	10	2	176
29	15	NA	127

I.3.3 TCAD simulation for *p*-gate AlGaN/GaN HEMTs

AlGaN/GaN HEMTs with p-AlGaN gate were simulated in Santaurus TCAD to investigate the impact of p-AlGaN doping concentration and the thickness for normally-off operation. The layer structure evaluated consists of a 50-nm-thick p-AlGaN gate, 30-nm-thick AlGaN barrier and 2-μm-thick GaN buffer layer. The mole fraction of p-AlGaN gate and undoped AlGaN barrier are 0.07 and 0.3, respectively. The p-AlGaN doping concentration varies from $1x10^{17}$ to $5x10^{18}$ cm^{-2}. As shown in the band diagram in Figure 17 (a), the p-AlGaN raises the band profile at the channel, which enables a normally-off operation. The calculated sheet carrier density versus the p-AlGaN doping concentration is shown in the Figure 17 (b). With an increase in the hole concentration in the p-AlGaN layer, the 2DEG under the gate region is decreased. Based on the simulation results, the E-mode operation could be achieved with the p-AlGaN doping concentration greater than $5x10^{18}$ cm^{-2}. The optimized field plate design will be evaluated and implemented in the p-AlGaN HEMTs.

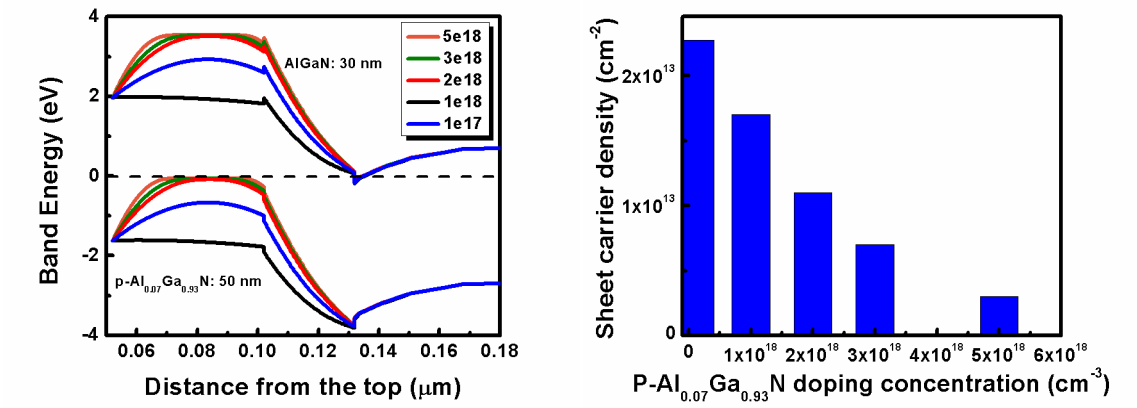


Figure 17. (a) A band diagram of p-AlGaN HEMTs design with different doping concentration. (b) The corresponding sheet charge density calculation of the designs.

I.4 P-(Al)GaN-gate regrowth technology development

The selective area growth (SAG) of the p-type gate was initiated and actively studied. We have worked to achieve the project goal of 100 nm thick p-type material selectively grown on the 3 μm wide pattern comprising the HFET gate. This is accomplished by depositing an oxide or SiN based mask and using photolithography with various etching techniques to open the gate pattern. However, we encountered several problems with the regrowth step including incomplete mask development yielding residual masking material in the window openings, surface damage induced by dry etching, and desorption in the initial stages of regrowth.

Experiments began with a test mask of circular patterns with thick electron beam SiO2. Selective area growth was performed using the same parameters as that for 1.7 μm of planar undoped GaN. While the regrowth window showed good morphology, the mask layer showed decomposition, as shown in Figure 18 (a). By reducing the thickness of the mask to 100 nm in line with the project specification, mask decomposition was averted, as shown in Figure 18 (b). The material quality of the regrowth was good as shown in the atomic force microscopy surface scan of Figure 19 demonstrating smooth morphology and step flow, however the thickness of the layer was above specifications at 2 μm.

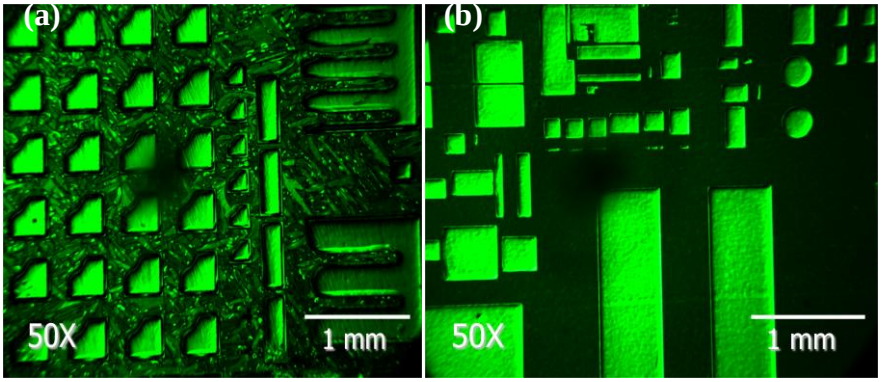


Figure 18. Optical microscope images of SAG performed on an SiO_2 mask with thicknesses of (a) 1.7 μm and (b) 100 nm

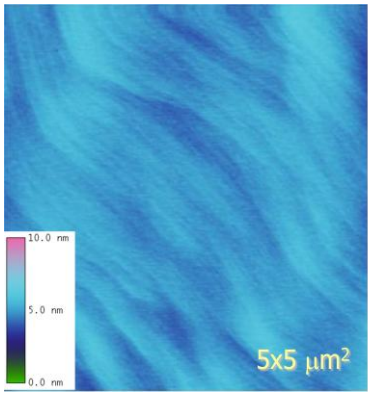


Figure 19. Atomic force microscopy surface scan of regrown material on the pattern from figure 1a with RMS roughness of 0.360 nm.

The next step was to reduce the thickness of the regrowth and to perform SAG on the actual HFET gate pattern. Significant challenges arose from the change in pattern geometry from relatively large to small windows just 3 μm wide. Due to the small fill factor of the HFET pattern, the growth rate of regrown GaN is very high, thus a significantly reduced growth time is required to grow just 100 nm of material for SAG as compared to planar GaN. During calibration runs, we observed that some patterns would be filled in, while adjacent patterns would not as shown in Figure 20, indicating that residual mask material was not being removed from the entire pattern. Optimization of pattern etching was needed to open all of the windows fully. For this purpose, we have explored various methods of mask deposition (PECVD SiO_2 and electron-beam SiO_2) and etching (lift-off, wet-etching, RIE, and ICP etching). We observed dry etching tended to damage the surface, inhibiting the re-growth step and liftoff was poor at maintaining window integrity (more material would be removed than desired). Thus a wet-etching process utilizing a pattern descum, extended buffered oxide etch and pre-run HF dip were utilized to ensure that all oxide was removed from the window area before regrowth.

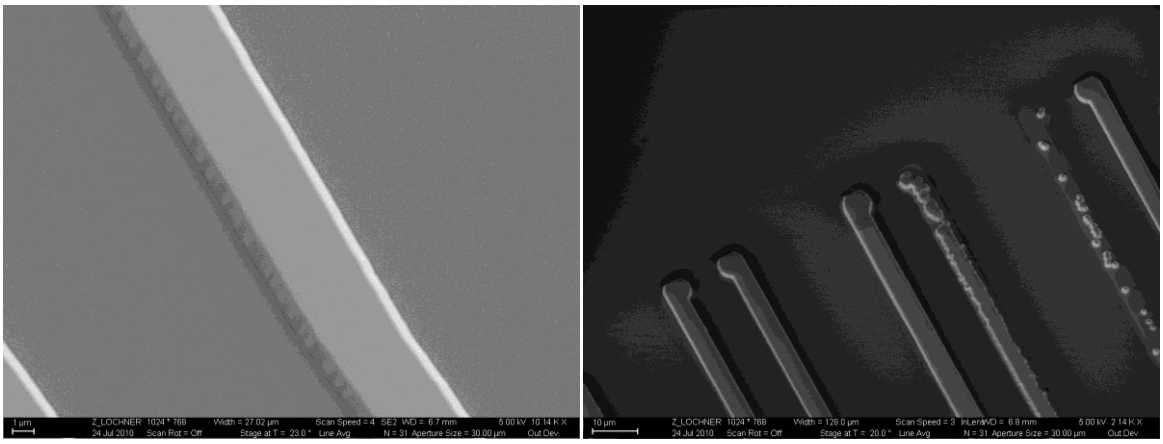


Figure 20. Scanning electron microscope images of GaN:Mg SAG at 1050 °C for 135 seconds on undoped GaN template. Mask was patterned by BOE on PECVD deposited SiO_2. Growth height of filled windows is ~1.9 μm.

Further problems arose when we reduced the growth time to achieve thinner regrowth layers. The thin SAG material was of very poor quality exhibiting rough surface morphology and columnar growth as shown in Figure 21. The problem was determined to be desorption during the initial stages of growth which damages the surface, and the short growth time did not allow for ample recovery to the good morphology seen for thicker layers. Thus a key development was reduction of growth temperature by 25 °C from 1050 to 1025 °C which lowers the desorption rate and reduces surface damage to the underlying material before the introduction of precursors for the growth step. The surface profiles taken by atomic force microscopy demonstrate the improvement observed by reducing temperature, with the damaged high temperature material in Figure 22 (a), and the single crystal material obtained by lowering the temperature shown in Figure 22 (b). Figure 23 shows the current quality of SAG under this growth condition as grown on an HFET on silicon sample.

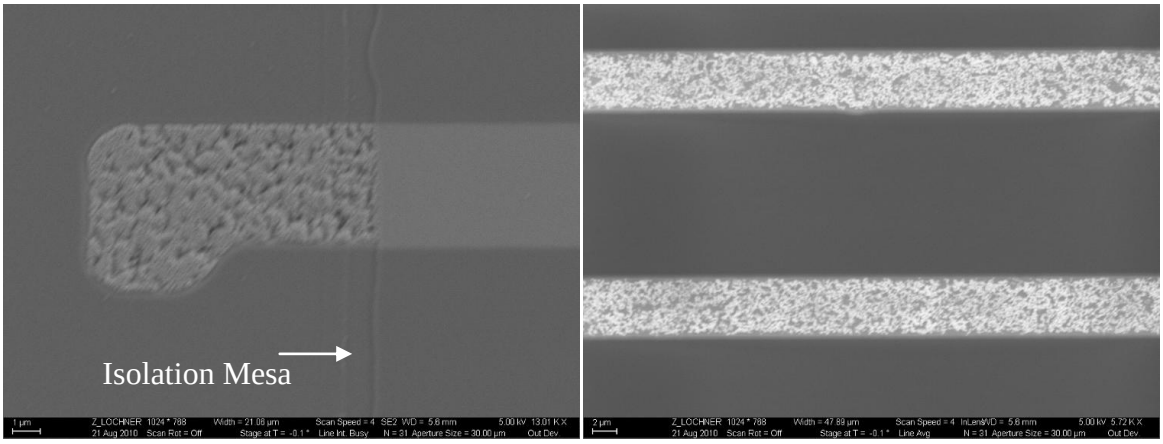


Figure 21. Scanning electron microscope images of GaN:Mg SAG at 1050 °C for 12 seconds on GaN HFET on silicon (INTS100512h2). Mask was patterned by BOE on electron-beam deposited SiO_2.

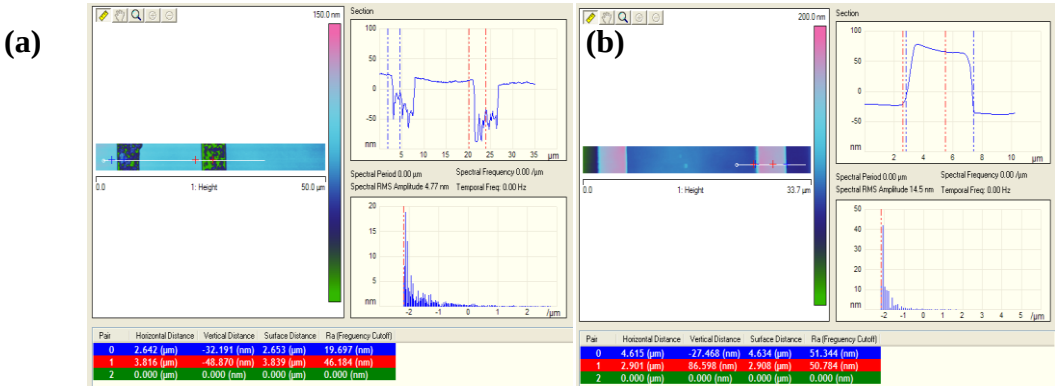


Figure 22. Atomic force microscopy profiles of regrown gates at (a) 1050°C and (b) 1025°C

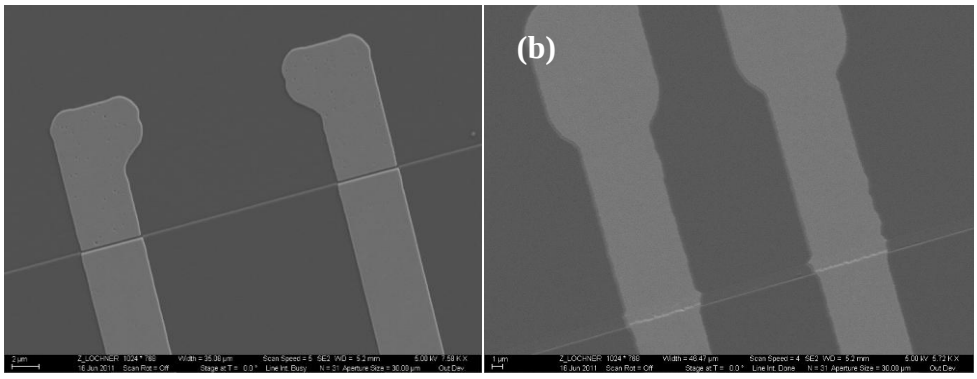


Figure 23. SEM images of GaN:Mg SAG done at 1025 °C for 20 seconds on (a) LPCVD deposited SiN with RIE mask patterning and (b) electron beam deposited SiO_2 with BOE patterning on GaN HFET on silicon (INTS100512h3).

In summary, at the end of the first year we have achieved selective area growth on the HFET gate patterns with good morphology at low growth time and thickness. Further

optimizations are in progress for growth thickness and p-type doping concentration to achieve an enhancement-mode device.

I.5 E-mode III-N HEMT development summary

One of the major efforts in the first year program is to explore new fabrication approaches to enable E-mode III-N HEMT implementation. To this end, we have embarked on several E-mode device approaches to be described in the following subsections. Through this study, we were able to compare the pros and cons of these approaches and proposed to consolidate our second year effort with focus on two major development tracks, i.e., the recessed-gate MIS and the p-gate regrowth, for the E-mode device implementation.

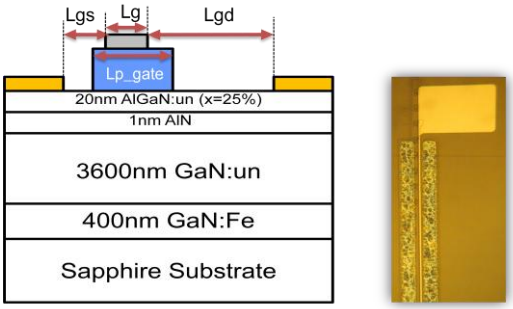
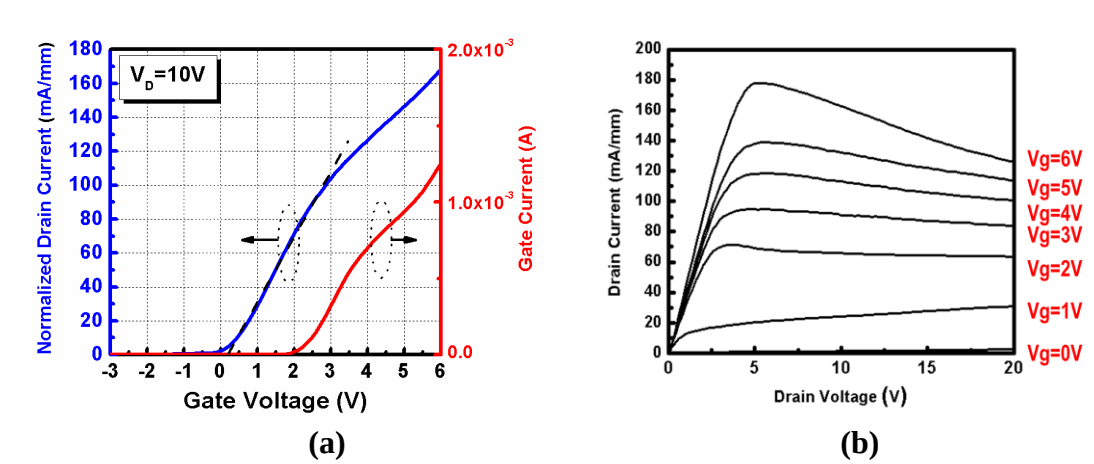


Figure 24. Cross sectional diagram and microscope image of fabricated blanket p-GaN HEMTs.

I.5.a Blanket p-AlGaN/p-GaN study

(A) Device Structure and Fabrication: The blanket p-GaN HEMTs was processed using wafer (1-1983-4). Figure 24 shows the cross sectional diagram and microscope image of the fabricated blanket *p*-GaN HEMTs. A p-GaN/AlGaN/GaN hetero-epitaxial structure is grown on sapphire substrate. The Al mole fraction and the thickness of i-AlGaN are optimized to be 25% and 20 nm, respectively. 100-nm *p*-GaN layer with nominal doping concentration of 1e18 cm^{-3} was grown on top of the standard HEMT structure. The p-type gate is formed by inductively coupled plasma (ICP) dry etching with the etching depth of 80nm. The used gate and source/drain metals are Ni and Ti/Al-based metal stack, respectively. The gate length (L_{p_gate}) is defined as the *p*-GaN width.

(B) Device Performance: Figure 25 (a) and (b) show the DC characteristics of the fabricated blanket p-GaN HEMTs. The device evaluated here has W_g = 300 μm, L_{GD} = 15 μm, L_{p_gate} = 3 μm , and L_{GS} = 3 μm. As shown in the figures, the forward gate voltage of 6 V can be applied while the forward gate voltage is limited up to 2 V in the conventional FET. The device is operated as an FET up to the V_{gs} of 3 V. Further increase of the V_{gs} linearly increases the drain current. By defining the threshold voltage as the gate voltage intercept of the extrapolation of the drain current, the threshold voltage of the fabricated blanket p-GaN HEMTs was found to be 0.3 V. The maximum drain current and on-state resistance $R_{ds(on)}$ are 140 mA/mm and 24 Ω-mm at V_{gs} = 5 V, respectively. In addition, the drain leakage current at V_G = -5 V, V_D = 200 V is 600 nA. However, we observed a non-uniform threshold voltage distribution on this wafer. The DC characteristics for unit cell devices are summarized in the Table 7.



(a) **(b)**

Figure 25. (a) The I_d-V_g and (b) I_d-V_d characteristics for blanket p-GaN HEMTs with L_{GD}=15 µm, and L_G=3 µm.

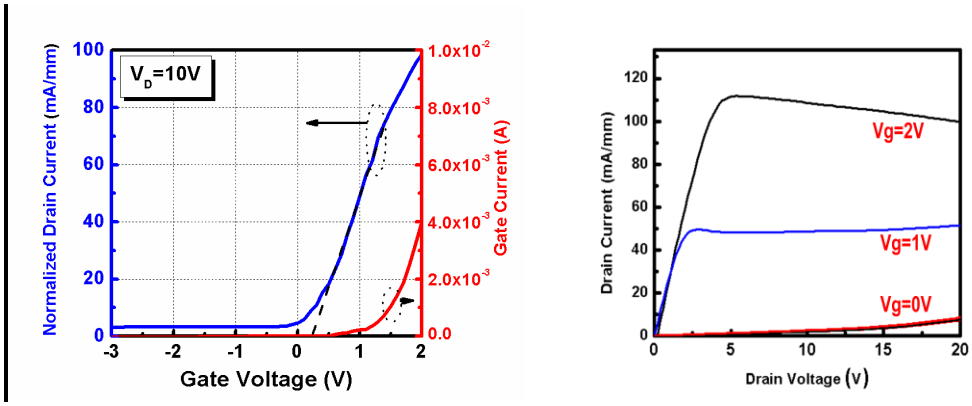
Table 7. DC performance for blanket p-GaN HEMTs (1-1983-4-4)

Lot	#	Wg(µm)	Lg(µm)	Lp_gate (µm)	Lgd (µm)	Lgs (µm)	Vth(V)	Imax(mA/mm) @ Vg=5V	Ron(Ω-mm) @Vg=5V	Leakage Current @200V
S_R9	18	300	1.5	3	10	3	-0.6	250	17	6uA
S_R9	24	300	1.5	4	15	3	-0.5	220	20	400nA
S_R9	26	300	1.5	3	15	2	0.2	120	31	250nA
S_R9	27	300	1.5	3	15	3	0.2	140	24	600nA
S_R9	29	300	1.5	3	15	2	-0.6	220	22	250nA

I.6 Blanket p-AlGaN HEMTs development and status update:

(A) Device Structure and Fabrication: The blanket p-AlGaN HEMTs was processed using wafer 1-1984-4. A 100-nm p-AlGaN layer with nominal doping concentration of $3x10^{17}$ cm^{-3} was grown on top of the standard HEMT structure. The p-type gate was then formed by ICP dry etching with the etching depth of 100nm, similar to those discussed in section 1.3.

(B) Device Performance: Devices with W_g =345 µm, L_G= 1.5 µm, L_{p_gate} =4.5 µm, and L_{GD} = 20 µm was evaluated. Figure 26 (a) and (b) show the DC characteristics of the fabricated blanket p-AlGaN HEMTs. As shown in the figures, the threshold voltage of the fabricated blanket p-AlGaN HEMTs is 0.2 V by extrapolating the gate voltage intercept of the drain current.. The maximum drain current and on-state resistance $R_{ds(on)}$ are 100 mA/mm and 36 Ω-mm at V_{gs} = 2 V, respectively. However, the buffer leakage could be observed in the Id-Vd characteristics shown in Figure 26 (b). The DC characteristics for unit cell devices are summarized in the Table 7. .



(a) **(b)**

Figure 26. (a) The I_d-V_g and (b) I_d-V_d characteristics for blanket p-AlGaN HEMTs with L_{GD}=20 µm, and L_G=1.5 µm.

Table 8. DC performance for blanket p-AlGaN HEMTs

Lot	#	W_g(µm)	L_g(µm)	L_{p_gate} (µm)	L_{gd} (µm)	L_{gs} (µm)	V_{th}(V)	I_{max}(mA/mm) @ Vg=2V	R_{on}(Ω-mm) @Vg=2V
C	1	345	2	4.5	20	2	0.1	100	30
C	2	345	2	4.5	10	2	0.2	95	33
C	4	345	2	4.5	10	2	0	70	45
C	5	345	2	4.5	20	2	0.2	100	30
C	6	345	2	4.5	20	2	0.3	80	36
C	7	345	2	4.5	20	2	-0.2	80	40
C	8	345	2	4.5	30	2	0.2	80	40

I.6.a Recessed gate processing development

We have investigated the gate recess process using a wet-etching based approach. The etching condition with different etching masks, i.e., silicon dioxide via PECVD and ALD-Al_2O_3, has been studied and compared. With a series of etching condition conducted, it seems that the PEC etching approach using PECVD silicon dioxide mask is controllable and feasible for recessed-gate processing. The etched surface morphology was also evaluated by AFM and surface scanning profiler. Figure 27, for example, shows the cross-sectional profile of recessed gate on the wafer (INTS100512h2) using profile meter. An etching time of 30 minutes resulted in a recessing depth of 22.7 nm, and the roughness is similar to the un-etched surface. . A series of studies and the results are summarized in the Table 9. It is proven that the wet-etching can

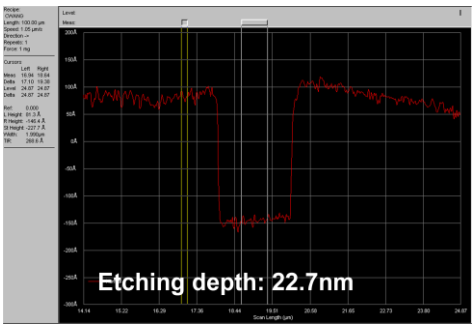


Figure 27. Cross-sectional profile of recessed gate on the wafer (INTS100512h2) using profile meter. The etching time is 30 mins.

be a reliable approach for recessed gate processing development. The obtained wet-etching process was then integrated with the recessed-gate E-mode GaN HEMTs fabrication on wafers INTS100512h1, INTS100512h2, and INTS100728h1 (see data in *I.6.c*).

Table 9. Summary of wet-etching process

Wafer ID	Date	Etching Mask	Etching Time	Measured depth (nm)	Surface Morphology
Intelliepi	May 5	ALD Al_2O_3 300nm	30 min	20nm	Comparable with the un-etched surface
Intelliepi	May 5	ALD Al_2O_3 300nm	15 min	15nm	Comparable with the un-etched surface
INTS100512h2-1	July 19	ALD Al_2O_3 300nm	37 min	21nm	Comparable with the un-etched surface
INTS100512h2-2	Aug. 12	ALD Al_2O_3 300nm	40 min	22nm	Rough surface due to the Al_2O_3 residue
INTS100512h2-3	Aug. 12	ALD Al_2O_3 300nm	50 min	24.8nm	Rough surface due to the Al_2O_3 residue
INTS100512h2-4	Aug. 12	ALD Al_2O_3 300nm	60 min	25.3nm	Incomparable with the un-etched surface
INTS100512h2-5	Aug. 20	PECVD SiO_2 1000 nm	30 min	23.5nm	Comparable with the un-etched surface
INTS100512h2-6	Aug. 20	PECVD SiO_2 1000 nm	40 min	25.4nm	Comparable with the un-etched surface
INTS100512h2-7	Aug. 20	PECVD SiO_2 1000 nm	50 min	26.5nm	Comparable with the un-etched surface
INTS100512h2-8	Aug. 20	PECVD SiO_2 1000 nm	60 min	27.1nm	Comparable with the un-etched surface
INTS100512h1-1	Sep. 27	PECVD SiO_2 1000 nm	50 min	26 nm	Comparable with the un-etched surface
INTS100512h1-2	Sep. 27	PECVD SiO_2 1000 nm	42 min	24 nm	Comparable with the un-etched surface
INTS100512h1-8	Nov. 12	PECVD SiO_2 1000 nm	30 min	22.5 nm	Comparable with the un-etched surface
INTS100728h1-3	Nov. 14	PECVD SiO_2 1000 nm	30 min	24 nm	Comparable with the un-etched surface
INTS100728h1-4/6	Nov. 30	PECVD SiO_2 1000 nm	30 min	24 nm	Comparable with the un-etched surface
INTS100728h1-5/7	Nov. 30	PECVD SiO_2 1000 nm	35 min	26 nm	Comparable with the un-etched surface

I.6.b MIS gate development

ALD-Al_2O_3 at GT was chosen for the gate dielectric. The ALD method is presumably better than the PECVD silicon nitride available in terms of surface roughness and interface-charge induced leakage current at high electric field. TMA and O_2 plasma were used as the metal precursor and oxidant, respectively. A monolayer can be deposited during each cycle. The AlGaN/GaN HEMTs with 6-nm-thick ALD-Al_2O_3 gate dielectric were first fabricated. As shown in Figure 28, we observed the inconsistent I_D-V_G curves during repeatedly scan, indicating the presence of trap charges at the Al_2O_3/AlGaN interface. To reduce/remove the hysteresis in the dielectric layer, we exploited a series of processing parameters for the post-growth annealing study including annealing temperature, annealing time, processing environment, and BOE pre-treatment.

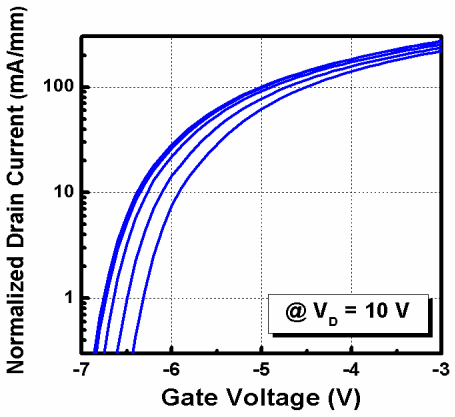
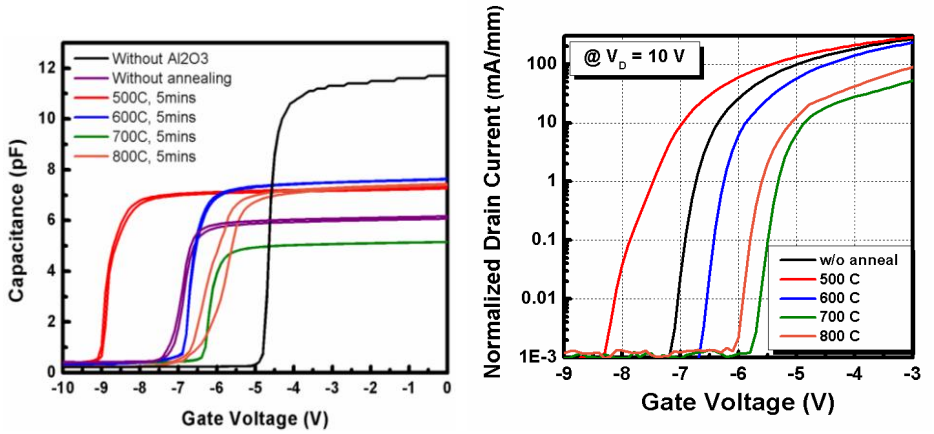


Figure 28. The I_D-V_G (log scale) characteristics for an AlGaN/GaN MIS-HEMT with 6 nm-thick Al_2O_3.

As shown in Figure 29 (b) and Figure 30, the I_D-V_G characteristics exhibit the device has more positive threshold voltage and lowest gate leakage current after a 700 ^oC post-annealing step when compared to other samples with different annealing temperatures. Most importantly, the C-V profiles in Figure 29 (a) indicate the device can operated at a virtually "zero hysteresis" behavior after a 700 ^oC post-annealing step under the nitrogen ambient. In addition, we found that the BOE pre-treatment can also be beneficial to reduce interface-charge induced leakage current. This process can be applied to future gate-recessed AlGaN/GaN MIS HEMT device fabrication.



(a) **(b)**

Figure 29. (a) The C-V profile for GaN MIS-HEMTs with different post-annealing temperature. The scan frequency is 1 MHz. (b) The I_D-V_G (log scale) characteristics for an AlGaN/GaN MIS-HEMT with different post-annealing temperature. The Al_2O_3 thickness is 6 nm.

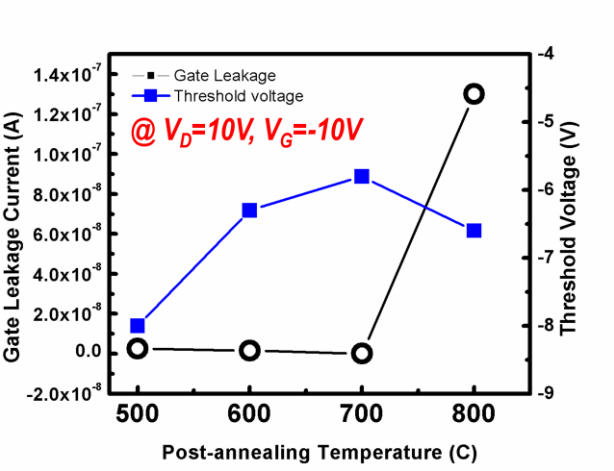


Figure 30. The gate leakage current (black circle) and the threshold voltage (blue square) as a function of post-annealing temperature.

I.6.c Gate-recessed AlGaN/GaN MIS HEMT summary

(A) Gate-recessed HEMTs with Schottky gate structure

The first-pass gate-recessed HEMT with schottky gate structure was processed using Intelliepi wafer as the precursor of E-mode operation via wet-etching approaches. The structure consists of 1 nm-thick GaN cap layer, AlGaN barrier with a thickness of 23 nm and 23% of Al mole fraction, 1.8 μm-thick GaN buffer, and 100 nm-thick AlN binary barrier grown on SiC substrate. Both D-mode device and gate-recessed devices with different etching time were fabricated for comparison.

For the gate recessing experiment, an atomic layer deposition system to deposit a thin layer of aluminum oxide (Al_2O_3) was served as the etching mask and the gate-recess is performed via PEC wet etching. The etching rate and etching condition were also investigated at this time. As shown in the Figure 31, an etching time of 30min resulted in a recessing depth of 20 nm. Also, the roughness of the etched surface is less than 0.1 nm. The gate-recessed HEMTs were fabricated on the same sample with etching time of 8 and 15 minutes, respectively. Both gate-recessed and conventional D-mode devices were fabricated simultaneously on the same wafer. A 200-nm-thick Ni was used as a gate electrode for the both devices. We have conducted a series of gate recessing experiments and fabricated the test MIS-HEMTs on

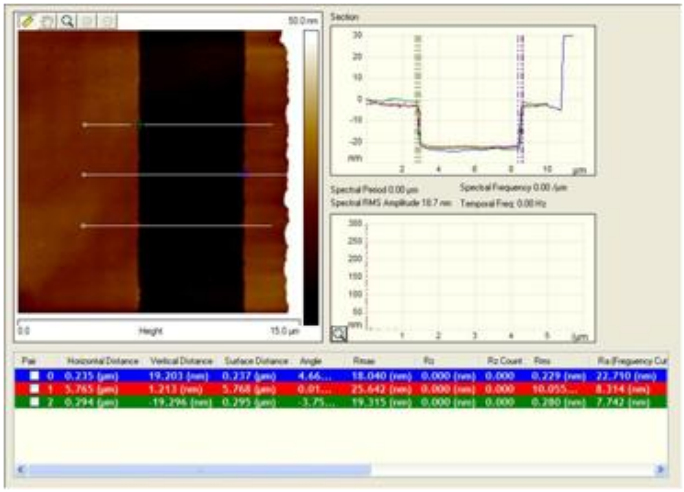


Figure 31. AFM image of the 30min PEC wet-etching.

reference wafers (GaN HEMTs on SiC substrate, supplied by IntelliEpi, Inc.) With the fabrication processing steps developed, we also exercise this set of fabrication processing on one of the GaN on Silicon wafers supplied by Intersil, as described in the following subsections.

(B) 1st - pass gate-recessed GaN MIS-HEMTs:

The first-trial of gate-recessed MIS-HEMT was processed using wafer ID: INTS100512h2. The device processing started with device isolation. Then, the gate-recessing was performed using the developed PEC wet etching. Figure 32 shows the cross-sectional profile of recessed gate using profile meter. The gate recessing depth is 27 nm, and the roughness is similar to the unetched surface measured by AFM. The ohmic and gate electrodes were Ti/Al/Ti/Au and Ni, respectively. Prior to the gate metal deposition, 30-nm-thick Al_2O_3 gate dielectric was deposited by plasma-enhanced ALD. It is noted that the dielectric film did not experience post-annealing in this batch.

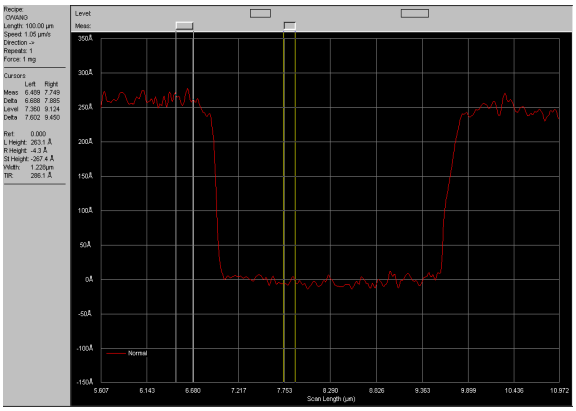


Figure 32. Cross-sectional profile of recessed gate on the wafer (INTS100512h2) using profile meter. The etching time is 27 mins.

The I_d–V_{gs} characteristic at V_D = 0-10 V is shown in Figure 33 (a). The gate-recessed structure dramatically changed the V_{th} from −4.5 (not shown here) to +9 V with the maximum current of 7 mA/mm at V_{gs} = 14 V before the gate dielectric breakdown. The V_{th} is defined as the gate voltage where drain current is 1 mA/mm. However, at different drain voltage, the threshold voltage shifts toward more positive values, which may be attributed to the trapped charge between the Al_2O_3/AlGaN interfaces. In Figure 33 (b), I_d–V_{ds} characteristic shows that the $R_{ds(on)}$ is 72 Ω-mm at V_{gs} = 14 V.

Figure 33 (c) shows the off-state characteristic of fabricated E-mode MIS-HEMTs. The applied gate voltage is 0 V, and the drain leakage current at V_D= 200 V is 9 nA (0.03 μA/mm). The recessed-gate GaN MIS-HEMTs implemented the proper enhancement-mode operation. However, high resistance and unstable threshold voltage will need to be addressed for further development.

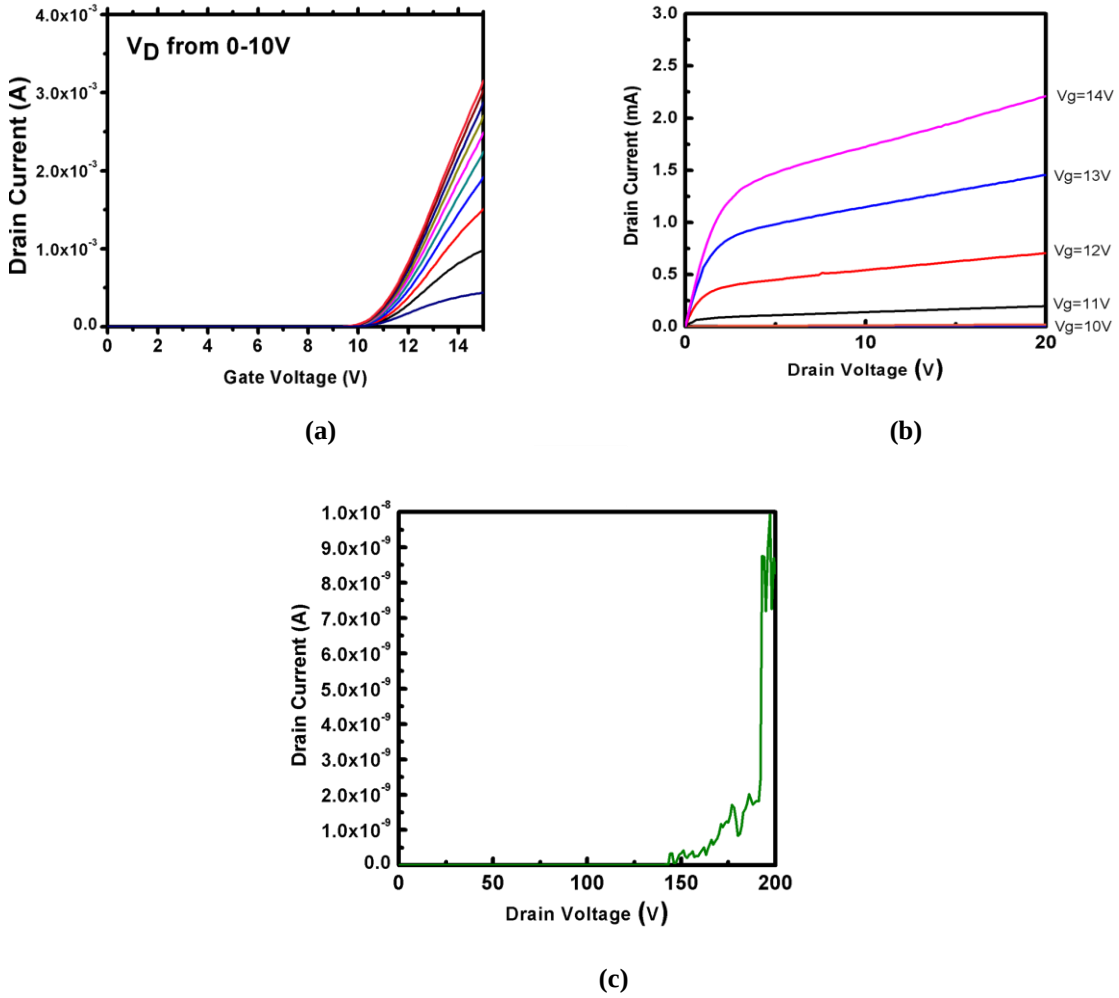


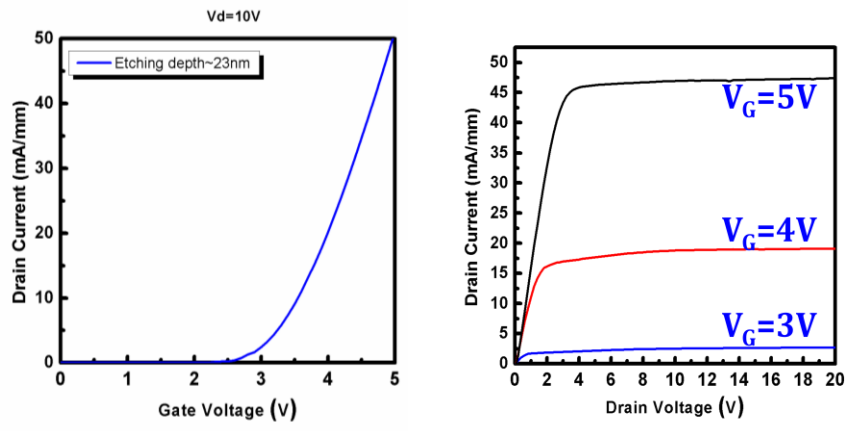
Figure 33. (a) The I_d-V_g and (b) I_d-V_d (c) off-state characteristics for gate-recessed MIS-HEMTs with W_G= 0.3 mm, L_{GD}=15 µm, L_{GS}=3 µm, and L_G=3 µm. The ALD-Al_2O_3 thickness is 30 nm.

(C) 2nd - pass gate-recessed GaN MIS-HEMTs with optimized Al_2O_3 post annealing:

With the optimization of post-annealing condition for Al_2O_3 gate dielectric, the 2nd-pass gate-recessed MISFET was processed using wafer INTS100512h1. In this batch, wet etching process with two different etching times of 42 min (2h-1) and 50 min (2h-2) was performed. The resulting etching depths of 42 min and 50 min etching time are 23 nm and 25 nm, respectively. Prior to the gate metal deposition, 6-nm-thick Al_2O_3 gate dielectric was deposited by plasma-enhanced ALD. After deposition, the film was annealed at 700 ^oC for 5 min under the Nitrogen ambient to eliminate the interface charge.

(i) The characteristics of gate-recessed MIS-HEMT (INTS100512h1-1): The recessing depth is around 23 nm using a surface profiler. The I_d–V_{gs} characteristic at V_D = 10 V is shown in Figure 34 (a). The gate-recessed structure changed the V_{th} from −4.7 to +2.5 V. In Figure 34 (b), I_d–V_{ds} characteristic shows the $R_{ds(on)}$ at V_{gs} = 5 V is about 50 Ω-mm with the maximum current drive of 45 mA/mm. The recessed-gate GaN MIS-HEMTs

implemented the proper enhancement-mode operation. The drain current at V_{gs} =0 V was 1.2 μA/mm. The threshold voltage however is stable during multiple voltage scans after the post annealing of ALD-Al_2O_3 deposition at > 700 ^oC. The performance of unit cell devices is summarized in the Table 10.



(a) **(b)**

Figure 34. (a) The I_d-V_g and (b) I_d-V_d characteristics for gate-recessed MIS-HEMTs (INTS100512h1-1) with W_G= 0.3 mm, L_{GD}=10 μm, L_{GS}=2.5 μm, L_F=1.5 μm and L_G=4 μm. The ALD-Al_2O_3 thickness is 6 nm.

Table 10. I-V characteristics of fabricated gate-recessed GaN HEMTs (INTS100512h1-1).

Lot	#	W_G(μm)	L_F(μm)	L_G(μm)	L_{GD} (μm)	L_{GS} (μm)	V_{th}(V)	I_{max}(mA/mm) @ V_G=5V	$R_{ds(on)}$(Ω-mm) @ V_G=5V	I_D (μA) @ V_D = 200 V, V_G = -10 V
SR9	14	300	1.5	3	10	2.5	2.5	30	85	> 500
SR9	15	300	1.5	4	10	2.5	2.5	50	50	> 500
SR9	17	300	1.5	4	10	2.5	2.5	46	60	100
SR9	19	300	1.5	6	10	2.5	2.5	40	60	200
SR9	20	300	1.5	6	10	2.5	2.5	53	42	300

(ii) The characteristics of gate-recessed MIS-HEMT (INTS100512h1-2): In this sample, the recessing depth is 25 nm. The I_d–V_{gs} characteristic at V_D = 10 V is shown in Figure 35 (a). The gate-recessed structure changed the V_{th} from −4.7 (not shown here) to + 3.0 V. In Figure 35 (b), I_d–V_{ds} characteristic shows the $R_{ds(on)}$ at V_{gs} = 5 V is about 60 Ω-mm with the maximum current drive of 23 mA/mm. The recessed-gate GaN MIS-HEMTs implemented the proper enhancement-mode operation. The drain current at V_{gs} =0 V was 0.2 μA/mm. The threshold voltage however is stable during multiple voltage scans after the post annealing of ALD-Al_2O_3 deposition at > 700 ^oC. The performance of unit cell devices is summarized in the Table 11.

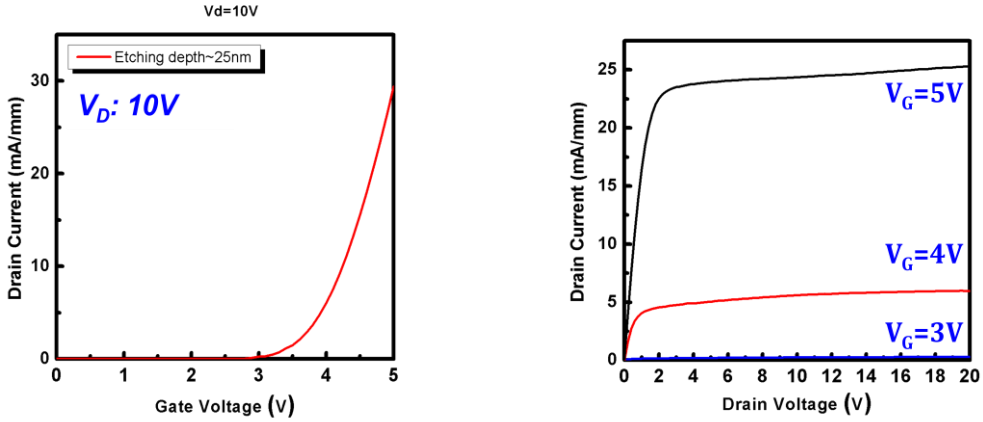


Figure 35. (a) The I_d-V_g and (b) I_d-V_d characteristics for gate-recessed MIS-HEMTs (INTS100512h1-2) with W_G= 0.3 mm, L_{GD}=10 µm, L_{GS}=2.5 µm, L_F=1.5 µm and L_G=4 µm. The ALD-Al_2O_3 thickness is 6 nm.

Table 11. I-V characteristics of fabricated gate-recessed GaN HEMTs (INTS100512h1-2).

Lot	#	W_G(µm)	L_F(µm)	L_G(µm)	L_{GD} (µm)	L_{GS} (µm)	V_{th}(V)	I_{max}(mA/mm) @ V_G=5V	$R_{ds(on)}$(Ω-mm) @ V_G=5V	I_D (µA) @ V_D = 200 V, V_G = -10 V
SR9	17	300	1.5	4	10	2.5	3	23	60	22
SR9	25	300	1.5	4	15	1.5	3	20	66	16
SR9	27	300	1.5	4	15	2.5	3	23	60	2
SR9	28	300	1.5	4	15	2.5	3	33	42	0.2

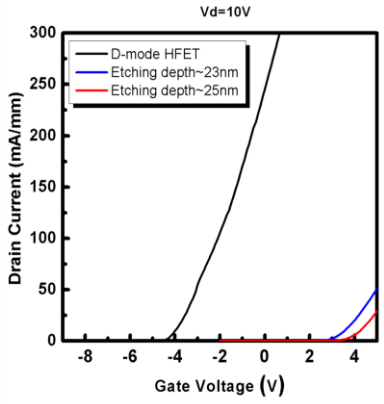


Figure 36. The I_d-V_g characteristics for gate-recessed MIS-HEMTs (INTS100512h1-1/2) and D-mode HEMTs with W_G= 0.3 mm, L_{GD}=10 µm, L_{GS}=2.5 µm, L_F=1.5 µm and L_G=4 µm.

Device Summary: As shown in the Figure 36, the recessed-gate GaN MIS-HEMTs implemented the proper enhancement-mode operation. The gate-recessing step shifts V_{th} from −4.7 to +2.5 and +3.0 V. However, as shown in Table 12, the maximum current drive of gate-recessed E-mode MIS-HEMTs is still low compared to that of D-mode devices.

Table 12. I-V characteristic comparison of fabricated gate-recessed and D-mode HEMTs.

Wafer	*Lot*	*#*	*Recessing depth (nm)*	W_G(μm)	L_F(μm)	L_G(μm)	L_{GD} (μm)	L_{GS} (μm)	V_{th}(V)	$R_{ds(on)}$(Ω-mm) @ V_G=5V	I_D (μA) @ V_D = 200 V, V_G = -10 V
D-mode HEMT INTS100512h1-4	SR9	17	0	300	--	4	10	2.5	-4.7	17	10
Gate-recessed MISFET INTS100512h1-1	SR9	17	23	300	1.5	4	10	2.5	3	60	100
Gate-recessed MISFET INTS100512h1-2	SR9	17	25	300	1.5	4	10	2.5	3.0	60	22

(D) Process flow optimization:

Figure 37 (a) and (b) show the original and optimized process flows for gate-recessed E-mode MIS-HEMTs fabrication, respectively. With the merged ohmic metal and ALD-Al_2O_3 post-annealing, the new process flow can not only simplify the process steps but also avoid the ohmic contact degradation during Al_2O_3 deposition. Most importantly, the ohmic contact resistance can be improved with lower annealing temperature. The obtained contact resistance is optimized to be $8x10^{-6}$ Ω-cm^2.

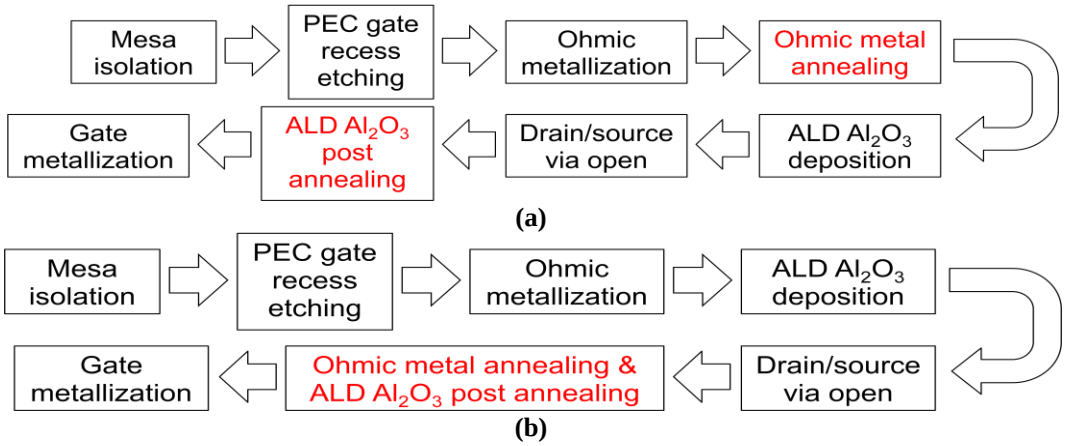
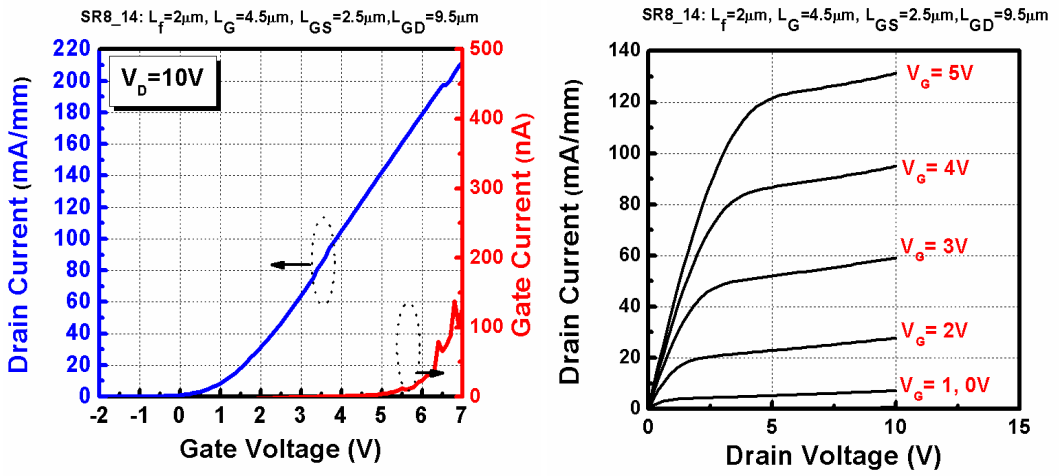


Figure 37. (a) Old and (b) new process flows for gate-recessed GaN MIS-HEMTs.

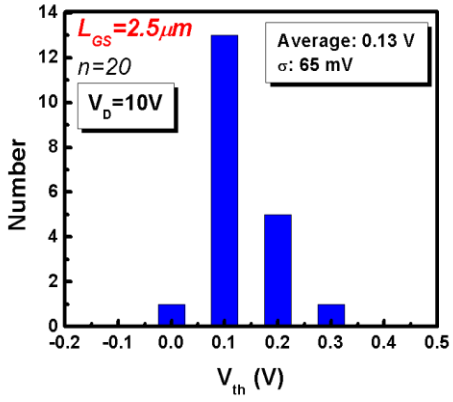
(E) 3rd - pass gate-recessed GaN MIS-HEMTs with optimized process flow:

With the optimization of processing flow, the 3rd-pass gate-recessed MISFET was processed using wafer INTS100728h1. The device process started with device isolation. Then, the gate-recessing was performed using the developed PEC wet etching. The etching depth (measured by AFM) is 23 nm. The ohmic and gate electrodes were Ti/Al/Ti/Au and Ni/Au, respectively. The typical gate length and gate width were 4 and 300 μm, respectively. The gate-to-drain space was 9.5 μm. Prior to the gate metal deposition, 6-nm-thick Al_2O_3 gate dielectric was deposited by plasma-enhanced ALD. After deposition, the film was annealed at 700 °C for 5 min under the Nitrogen ambient. The I_d–V_{gs} characteristic at V_D = 10 V is shown in Figure 38 (a). The gate-recessed structure shifted

the V_{th} from −4.6 to +0.1 V, while maintaining the maximum drain current of 210 mA/mm at V_{gs} = 7 V. The V_{th} is defined at I_{ds} = 1 mA/mm. Figure 38 (c) shows a histogram of V_{th} for fabricated devices. A standard deviation of 65 mV indicates the good uniformity of threshold voltage distribution in the full wafer. In Figure 38 (b), I_d–V_{ds} characteristic shows the $R_{ds(on)}$ at V_{gs} = 5 V is 24 Ω-mm. The recessed-gate GaN MIS-HEMTs implemented the proper enhancement-mode operation. The drain current at V_{gs} =0 V is 80 μA/mm, which is leakier than those in the D-mode device at the pinch-off. The threshold voltage however is stable during multiple voltage scans after the post annealing of ALD-Al_2O_3 deposition at > 700 ^oC. As shown in Figure 38 (a), the gate current start to increase at V_{gs}>5V, suggesting that the dielectric layer starts to breakdown beyond this point. The corresponding breakdown electrical field for the ALD-Al_2O_3 is approximately 8 MV/cm.



(a) **(b)**



(c)

Figure 38. (a) The I_D-V_G and (b) I_D-V_D characteristics for gate-recessed AlGaN/GaN MIS-HEMTs (INTS100728h1-3) with recessing depth =23 nm, L_{GD}=9.5 μm, and L_G=4.5 μm. (c) Threshold voltage histograms of the fabricated devices.

The devices were passivated with BCB-based polymer, followed by contact window opening and final overlay metal for the evaluation of the performance of multi-fingered E-mode MIS-HEMT. As shown in Figure 39, the measured I_d–V_{ds} characteristic for 3-mm device exhibits the maximum drain current of 500 mA with specific on-resistance $R_{ds(on)}$ of 10.2 Ω (or 9.6 mΩ-cm^2) at V_{gs} = 6 V. The gate leakage current at V_{gs} = 5 V is approximately 1.7 μA. However, we experienced a poor device yield and observed the significant gate current crowding issues in the larger-area devices. Further optimization for the device design and fabrication refinement will be required.

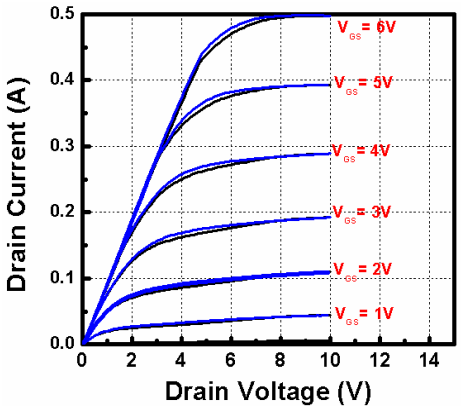


Figure 39. Measured I_D-V_D characteristics for gate-recessed AlGaN/GaN MIS-HEMTs (INTS100728h1-3) with recessing depth =23 nm, W_G= 3 mm, L_f= 1.5 μm, L_G= 4 μm, L_{GS}= 2 μm, L_{GD}= 9.5 μm.

(F) 4th - pass gate-recessed GaN MIS-HEMTs with different Al_2O_3 thickness:

To extend the dielectric breakdown voltage, a comparative study for different gate recessing depth and different ALD-Al_2O_3 was initiated. The I_d–V_{gs} characteristics and the corresponding V_{th} histograms of the fabricated devices at V_D = 10 V are shown in Figure 40, Figure 41, Figure 42 (a) and (b), respectively. We measured at least nine unit-cell devices on each wafer and populated the averaged threshold voltage values and corresponding standard deviation. Table 13 shows a comparison of device performance using different recessing depth and dielectric thickness. The small deviation for each wafer further proved that the wet-chemical recess-etching process step is potentially controllable and reliable to obtain a uniform recessed gate.

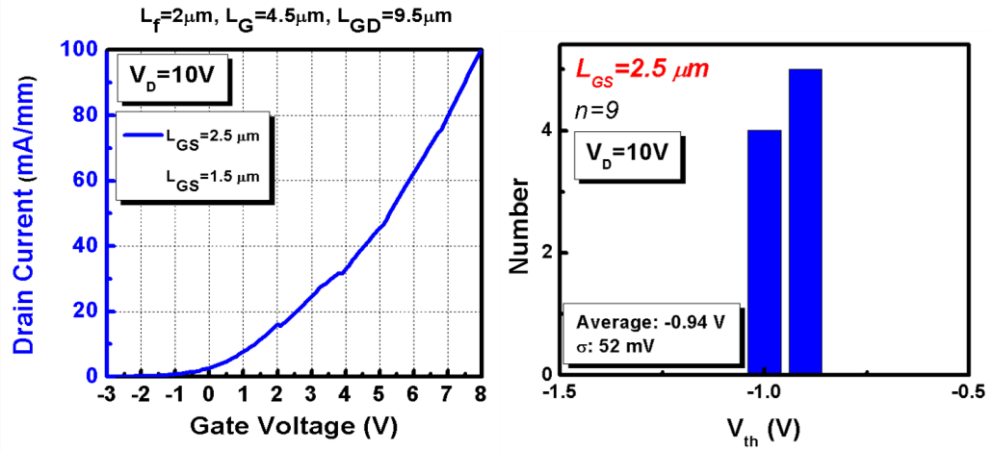


Figure 40. (a) The I_D-V_G characteristics for gate-recessed AlGaN/GaN MIS-HEMTs (INTS100728h1-4) with recessing depth =24 nm, ALD-Al_2O_3 thickness= 10 nm, L_{GD}=9.5 μm, L_{GS}=2.5 μm, L_F=2 μm, and L_G=4.5 μm. (b) Threshold voltage histograms of the fabricated devices.

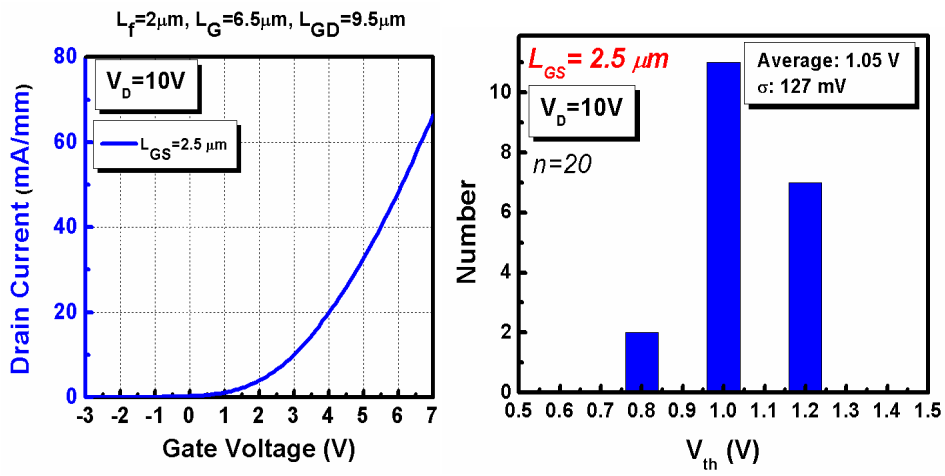


Figure 41. (a) The I_D-V_G characteristics for gate-recessed AlGaN/GaN MIS-HEMTs (INTS100728h1-5) with recessing depth =27 nm, ALD-Al_2O_3 thickness= 10 nm, L_{GD}=9.5 μm, L_{GS}=2.5 μm, L_F=2 μm, and L_G=6.5 μm. (b) Threshold voltage histograms of the fabricated devices.

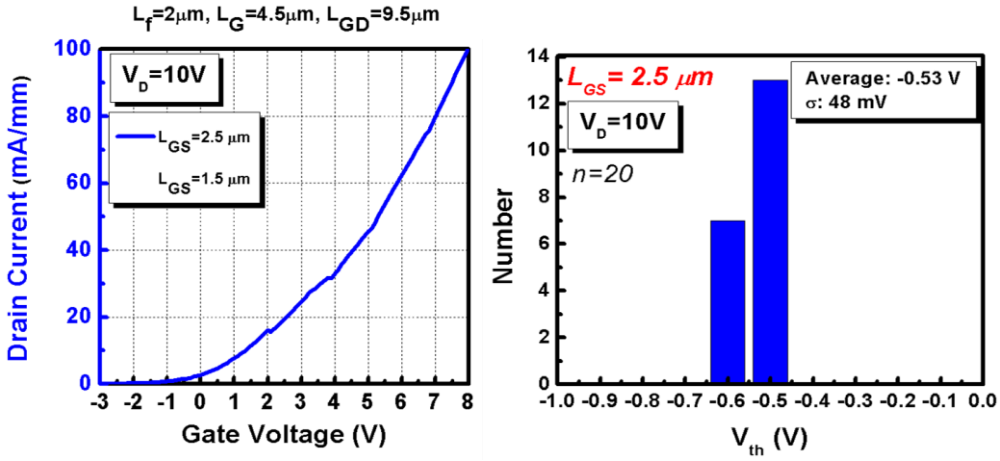


Figure 42. (a) The I_D-V_G characteristics for gate-recessed AlGaN/GaN MIS-HEMTs (INTS100728h1-4) with recessing depth =24 nm, ALD-Al_2O_3 thickness= 15 nm, L_{GD}=9.5 μm, L_{GS}=2.5 μm, L_F=2 μm, and L_G=4.5 μm. (b) Threshold voltage histograms of the fabricated devices.

Table 13. Device performance comparisons of gate-recessed MIS-HEMTs.

Wafer	Recessing depth (nm)	Al_2O_3 thickness (nm)	V_{th}		I_G (nA)@ V_D = 10 V, V_G = 8 V
			Avg. (V)	σ (mV)	
Gate-recessed MISFET INTS100728h1-4	24	10	-0.94	52	50
Gate-recessed MISFET INTS100728h1-5	27	10	1.05	127	300
Gate-recessed MISFET INTS100728h1-6	24	15	-0.53	48	5

Above all these developments, the field plate design still need to be optimized and integrated with E-mode MIS-HEMTs fabrication. With the reduction of gate-recessed length and the contact resistance, it is also expected that the trade-off characteristics between the breakdown voltage and the on-resistance could be further improved in the future.

I.7 LPCVD passivation experiment

The interface-state density at the insulator-semiconductor interface determines the viability of GaN MIS-HEMTs. Thus, high-quality dielectrics are required as either a passivation mean or the gate insulator for high-performance power switches. In recent years, much attention has been focused on the reduction of surface states using different dielectrics, such as PECVD silicon dioxide, silicon nitride, and sputtered-silicon dioxide. However, the research-grade dielectric materials available tend to cause large current dispersion due to the high charge density at the interface and inside the dielectrics. To reduce the impact of this variable in a research environment, BCB were used to passivate the devices for "quick" solutions to obtain high-performance transistors. In view of the requirement of the field plate designs and the need for high-temperature gate insulator, nevertheless, high-quality dielectric layers are still required. LPCVD nitride could be a suitable candidate to serve this purpose with low surface state density and high breakdown electrical field. The collaboration with Intersil at Palm Bay for LPCVD silicon nitride study was initiated in December, 2010. The development objective focuses on the controllability and dielectric quality of LPCVD nitride grown on GaN templates. The growth conditions, such as temperature and rate, will be studied. This part of work is continuing in the 2nd year project.

I.8 Novel InAlN-based structure design

We proposed and demonstrated a method of manufacture of a wide-bandgap HEMTs using versatile strain management in InAl(Ga)N semiconductors to achieve either enhancement mode (E-mode) or depletion mode (D-mode) HEMTs with extended drain-to-source breakdown voltage characteristics, higher current drive for E-mode operation, and lower on-state resistance for E/D-mode operation. Three InAl(Ga)N-based FET design examples are disclosed for pedagogical purposes. These novel III-nitride-based InAlGaN/GaN heterostructures consist of $In_xAl_{1-x}N$ and GaN heterostructures that can make E-mode transistors with improved current handling capacities. For realistic case study, double layered $In_xAl_{1-x}N$ ($x \geq 0.18$)/$In_yAl_{1-y}N$ ($y \leq 0.18$) HEMT designs are also disclosed to enable both E-mode and D-mode operation by taking advantage of the strain compensation in compressive and tensile semiconductor layers with low electric field at the surface for extended drain breakdown voltage, while maintaining high two-dimensional electron gas (2DEG) density in InAlN-based semiconductors. *Third*, multiple layers of strain-compensated InAl(Ga)N semiconductors can be grown and fabricated to achieve monolithic integration of the E/D-mode transistor technology for high-performance digital and analog integrated circuits (ICs).

This patent disclosure is based on a previously disclosed provisional patent entitled "Enhancement- and depletion-mode heterostructure field-effect transistors using InAIN/GaN heterostructures" (GTRC OTL Patent Disclosure ID # 5008) invented by some

of the inventors herein. In the provisional patent, the inventors described D-mode and E-mode operations of III-nitride HEMTs based on $In_xAl_{1-x}N$ cap layer. The present patent disclosure addresses several approaches to overcome issues observed in the real device implementation and offers effective III-N HEMT design strategies to exploit the expanded functionality of such unique material systems in a wide variety of high-power switching applications as well as next-generation radio-frequency (RF) mixed-signal and complementary ICs.

1. *Embodiment examples for strain-compensated InAlN HEMTs*

The proposed strain compensated InAlN HEMT designs in this approach is based on a bandgap engineering of the wide-gap barrier design through a compensation of the strain-induced polarization field in a monolithic integration of compressively strained and tensile strained InAlN layers. It is known that the piezeoelectric polarization field in a compressively strained InAlN is directing in the opposite direction to that in a tensile strained InAlN layer. By designing different indium composition and thickness of each compressively and tensile strained layer in the wide-bandgap barrier layer in an III-N HEMT, one may also achieve the following added features:

a. The surface potential may be reduced;
b. The Schottky barrier in a FET can be increased; and
c. Variable channel properties in the drain-to-source region for smart engineering in the electric field distribution in the drift region of III-N FETs.

In the embodiment of the proposed approach, three examples of the strain engineered InAlN HEMT are disclosed as followed:

2.1 EXAMPLE 1: RECESSED-GATE E-MODE IMPLEMENTATION

In the first example, as shown in Table 14. The layer structure of InAlN HEMT consists of a GaN cap layer (Layer # 1), 10-nm $In_xAl_{1-x}N$ top layer (Layer #2), 5-nm $In_yAl_{1-y}N$ bottom layer(Layer #3), an 1.5-nm AlN binary barrier (BB) layer (Layer #4), and undoped GaN buffer layer (Layer #5). The layer structure can be grown on any suitable substrates such as sapphire, silicon, silicon carbide, aluminum nitride, or gallium nitride, whenever applicable. The band diagram of the layer structures were simulated using a TCAD/Santarus simulation package.

Table 14. An example of the multiple layers InAlN HEMT implementation.

Layer	Material	x	Type	Thickness
1	GaN		UID	2nm
2	$In_xAl_{1-x}N$	0.14-0.24		10nm
3	$In_vAl_{1-v}N$	0.2	UID	5nm
4	AlN		UID	1.5nm
5	GaN		UID	2000nm
Strain-management buffer layers				
Substrate				

The bottom $In_yAl_{1-y}N$ has a fixed $y_{In} = 0.2$ (compressively strained relative to GaN) and the top compressively $In_xAl_{1-x}N$ layer has a varying x_{In} from 0.14 to 0.24. It should be noted

that the thicknesses and compositions of layers are fixed in this example for pedagogical illustration purposes but not unique in device embodiment of the disclosed inventions. The resulting zero-bias band diagrams of the varying y_{In} in the gate region are shown in Figure 43 (a). The sheet charge density in the gate region is shown in Figure 43 (b).

One may find that

a. The sheet charge density decreases as the x_{In} increases, implying that the E-mode operation can be achieved when x_{In} >0.22 in this design
b. The total electric field along the growth direction is reduced when x_{In} >0.22, leading to a change in the surface electric field in the gate region.

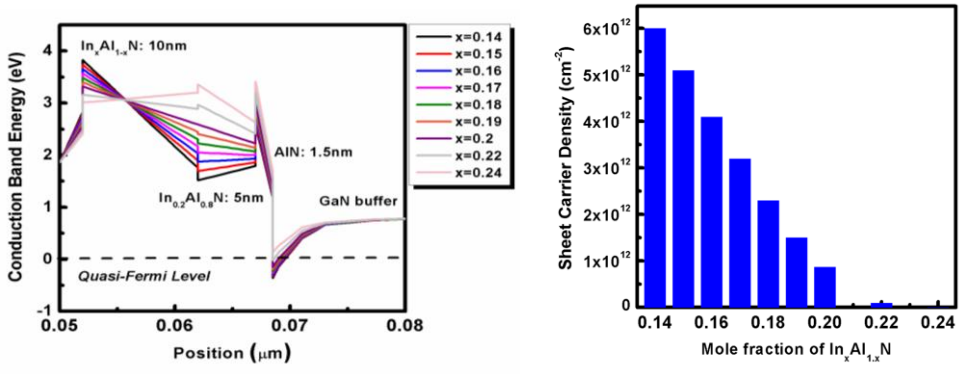


Figure 43. (a) A band diagram of InAlN barrier design with different indium composition in the top strained layer. (b) The corresponding sheet charge density calculation of the designs.

The E-mode device can therefore be implemented in the topology of Figure 44 and is re-illustrated as a case study. In this case study, the tensile strained top layer remains in the drift region of the FET and the top layer was removed in the gate region. As a result, the drift region may possess high concentration of the 2DEG and the gate region is

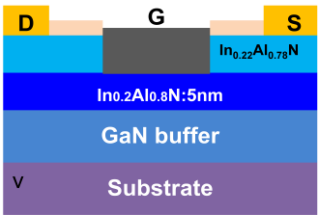


Figure 44. An example of E-mode InAlN HEMT implementation for topology disclosed in Error! Reference source not found.**Figure 43.**

depleted of the 2DEG.

2.2 Example 2: Recessed Channel E-mode HEMTs

Table 15. An example of the multiple layers InAlN HEMT implementation.

As shown in Table 15, the layer structure of InAlN HEMT consists of a GaN cap layer (Layer # 1), 10-nm $In_xAl_{1-x}N$ top layer (Layer #2), 20-nm $In_yAl_{1-y}N$ bottom layer(Layer #3), an 1.5-nm AlN binary barrier (BB) layer (Layer #4), and undoped GaN buffer layer (Layer #5). The layer structure can be grown on any applicable substrates.

Layer	Material	x	Type	Thickness
1	GaN		UID	2nm
2	$In_xAl_{1-x}N$	0.19-0.25		10nm
3	$In_yAl_{1-y}N$	0.2	UID	20nm
4	AlN		UID	1.5nm
5	GaN		UID	2000nm
Strain-management buffer layers				
Substrate				

The bottom $In_yAl_{1-y}N$ has a fixed y_{In} = 0.2 and the top compressively $In_xAl_{1-x}N$ layer has a varying x_{In} from 0.19 to 0.25. Again, it should be noted that the thicknesses and the compositions of layers are fixed in this example for pedagogical illustration purposes but not unique in device embodiment of the disclosed inventions. The resulting zero-bias band diagrams of the varying y_{In} in the gate region are shown in Figure 45.

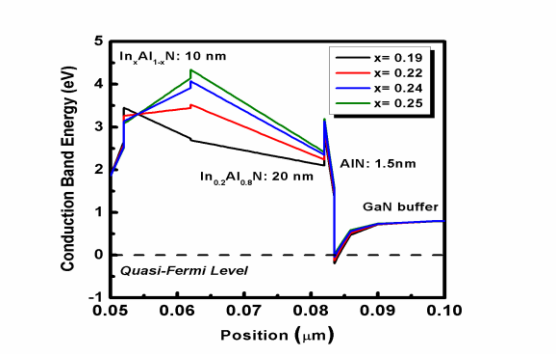


Figure 45 A band diagram of InAlN barrier design with different indium composition in the top strained layer.

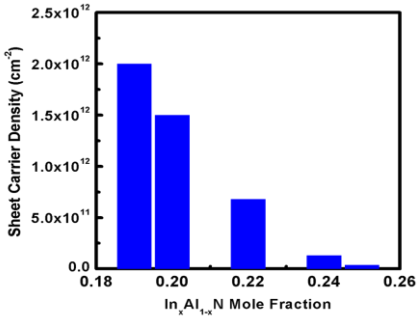


Figure 46. The corresponding sheet charge density calculation of the designs shown in Figure 45.

It is shown that, without the presence of the top InAlN layers, the device is inherently a D-mode device. With the addition of the compressively strained $In_xAl_{1-x}N$ layer, the device can convert from D-mode into E-mode and the surface potential changes accordingly. This is also evident from the sheet charge density calculation shown in Figure 46. In this example, the E-mode device implementation is identical to that indicated by a single epitaxial growth scheme. A case study is also shown in Figure 47 with x_{In} = 0.24. The gate region contains the highly compressively strained InAlN while the top epitaxial layer in the drift region is removed to retain high 2DEG concentration for improved channel conductivity.

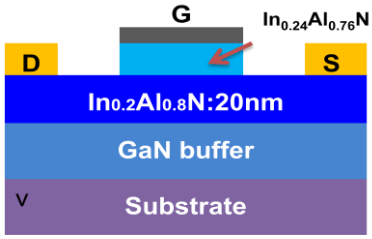
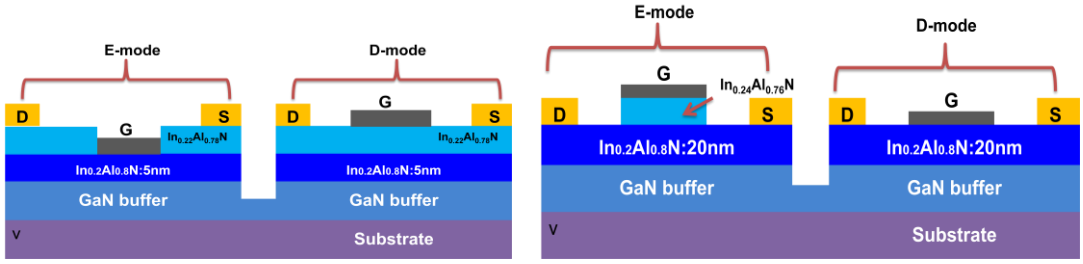


Figure 47. An example of E-mode InAlN HEMT implementation for topology disclosed in Error! Reference source not found.**Figure 45.**

2.3 Example 3: Monolithically Integrated E/D mode InAlN HEMTs

In further embodiments, we also propose to use this design approach to implement monolithic integrated E/D-mode HEMT using the strain-compensation InAl(Ga)N design approaches. Take Recessed channel E-mode InAlN HEMT for example, the D-mode and E-mode devices can be integrated in the same chip by laying the gate electron on the top layer for E-mode devices or on the bottom layer for D-mode devices, as shown in Figure 48 (a). Similar approach for E/D mode integrated circuits can be implemented for the recessed-gate E-mode approach, as shown in Figure 48 (b).



(a) **(b)**

Figure 48. A schematic drawings for the monolithic integration of E/D mode InAlN HEMT using strain compensated concepts with (a) recessed-gate E-mode approach and (b) recessed channel approach.

Bibliography

[1] N. Ikeda, J. Lee, S. Kaya, M. Iwami, T. Nomura, and S. Katoh, "High-power AlGaN/GaN HFETs on Si substrates for power-switching applications," in *Gallium Nitride Materials and Devices IV*, San Jose, CA, USA, 2009, pp. 721602-11.

[2] U. K. Mishra, P. Parikh, and W. Yi-Feng, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, pp. 1022-1031, 2002.

[3] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates," *Electron Device Letters, IEEE*, vol. 27, pp. 713-715, 2006.

[4] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "On-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage," *Electron Device Letters, IEEE*, vol. 28, pp. 676-678, 2007.

[5] X. Xiaobin, S. Junxia, L. Linlin, J. Edwards, K. Swaminathan, M. Pabisz, M. Murphy, L. F. Eastman, and M. Pophristic, "Demonstration of Low-Leakage-Current Low-On-Resistance 600-V 5.5-A GaN/AlGaN HEMT," *Electron Device Letters, IEEE*, vol. 30, pp. 1027-1029, 2009.

[6] Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "Recent advances of high voltage AlGaN/GaN power HFETs," in *Gallium Nitride Materials and Devices IV*, San Jose, CA, USA, 2009, pp. 721606-11.

[7] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," *Electron Device Letters, IEEE*, vol. 27, pp. 716-718, 2006.

[8] W. Huang, T. P. Chow, Y. Niiyama, T. Nomura, and S. Yoshida, "Lateral Implanted RESURF GaN MOSFETs with BV up to 2.5 kV," in *Power Semiconductor Devices and IC's, 2008. ISPSD '08. 20th International Symposium on*, 2008, pp. 291-294.