HIGHLY EFFICIENT LINEAR CMOS POWER

AMPLIFIERS FOR WIRELESS COMMUNICATIONS

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AMPLIFIERS FOR WIRELESS COMMUNICATIONS

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To my wife and parents

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LIST OF SYMBOLS AND ABBREVIATIONS

AM-AM	amplitude-to-amplitude
AM-PM	amplitude-to-phase
ACLR	adjacent channel leakage ratio
CDMA	code division multiple access
CE	collector efficiency
CG	common gate
CMOS	complementary metal oxide semiconductor
CS	common source
DA	driver amplifier
DE	drain efficiency
EDGE	enhanced data rates for GSM evolution
EVM	error vector magnitude
GaAs	gallium arsenide
GSM	global system for mobile
HBT	hetero-junction bipolar transistor
HEMT	high electron mobility transistor
HP	high-power
IC	integrated circuit
IP_3	third-order intercept point
IL	insertion loss
IMD_3	third order intermodulation distortion
InGaP	indium gallium phosphide

LP	low-power
LTE	long term evolution
MIM	metal-insulator-metal
MOSFET	metal oxide semiconductor field effect transistor
MP	medium-power
P_{1dB}	output referred 1-dB compression point
PA	power amplifier
PAE	power added efficiency
PAPR	peak-to-average power ratio
PCB	printed circuit board
PDF	probability distribution function
P_{sat}	saturated (peak) output power level
Q	quality factor
RF	radio frequency
SiGe	silicon germanium
SNR	signal-to-noise ratio
SRF	self-resonant frequency
WCDMA	wideband CDMA
WiMAX	worldwide interoperability for microwave access
WLAN	wireless local area network
3GPP	the 3rd generation partnership project

SUMMARY

The rapidly expanding wireless market requires low cost, high integration and high performance of wireless communication systems. Complementary metal oxide semiconductor (CMOS) technology provides benefits of cost effectiveness and higher levels of integration. However, the design of highly efficient linear CMOS power amplifier (PA) that meets the requirement of advanced communication standards is a challenging task because of the inherent difficulties in CMOS technology. The objective of this research is to realize PAs for wireless communication systems that overcome the drawbacks of CMOS process, and to develop design approaches that satisfy the demands of the industry.

In this dissertation, a cascode feedback bias technique is proposed for improving linearity and reliability of the multi-stage cascode CMOS PA. A fully-integrated single chip linear PA in a 0.18-μm CMOS process is implemented with the technique. This PA achieved 46.4% of peak PAE at 26 dBm output power and 40% of linear PAE at 23.5 dBm output power. In addition, to achieve load variation immunity characteristic and to enhance matching and stability, a fully-integrated balanced PA is implemented in a 0.18-μm CMOS process. Measurement results show the excellent load variation immunity characteristics. This dissertation also proposed a triple-mode balanced PA using a switched quadrature coupler. The method that uniquely utilizes the isolation port of the quadrature coupler as a signal path was analyzed. With the triple-mode operation, this work significantly reduced quiescent current and further improved the efficiency in the back-off power. For low losses and a high quality factor of passive output combining, a

transformer-based quadrature coupler is implemented using integrated passive device (IPD) process in this work. Various practical approaches for linear CMOS PA are suggested with the verified results, and they demonstrate the potential PA design approach for WCDMA applications using a standard CMOS technology.

CHAPTER 1

INTRODUCTION

1.1 Technology trends

Advances in semiconductor technology have prompted rapid growth in the wireless communication industry over the past twenty years. With emerging technologies, wireless mobile communication systems have undergone rapid development and become widely distributed, establishing their position as necessities in daily life. As market trends accelerate, users demand not only voice and simple messaging, but also various multimedia data services, necessitating the convergence of technologies, including video, music, camera, gaming, global positioning system (GPS), and mobile Internet access into one mobile device. The advent of smartphones has made communication using handset possible, exposing a new paradigm of communications. Smartphones allow data communications anytime and anywhere. Figure 1.1 (a) shows the growth and the forecast of smartphones. In the expanding wireless communication handset market, the number of smartphones is continuously increasing while the number of traditional handsets has become stagnant. Figure 1.1 (b) shows the forecast of the overall mobile data growth. As data communications using mobile handsets continue to expand, the market demand for higher data-rate of wireless communication systems is accelerating.

(a)   (b)
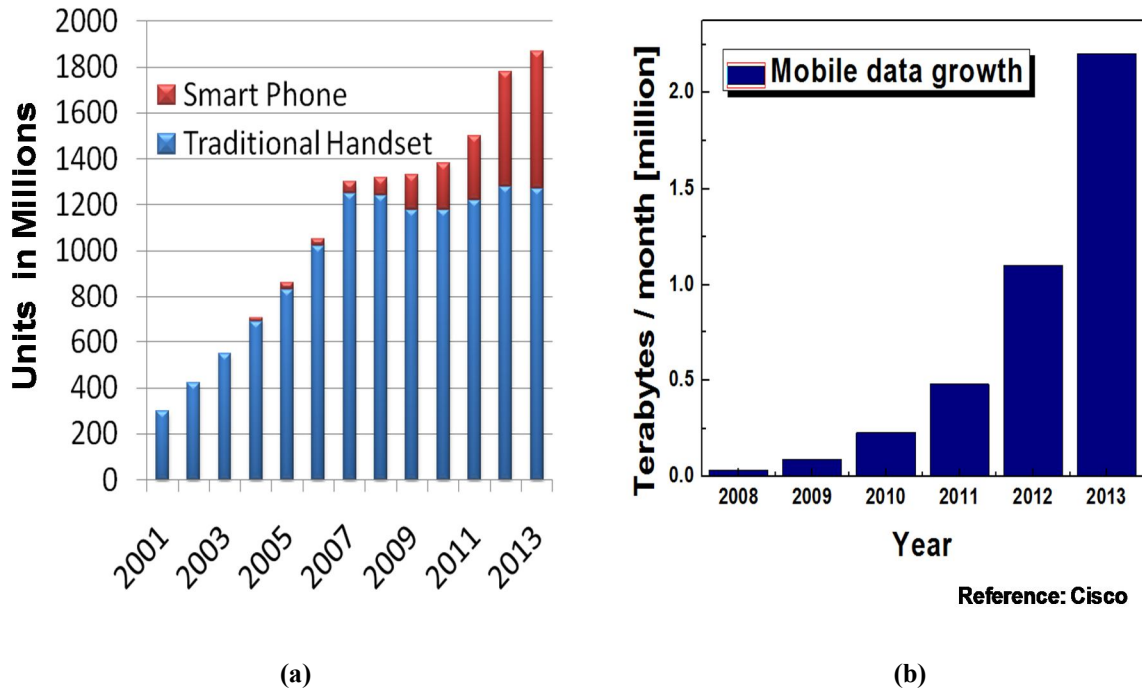
Figure 1.1 (a) Estimates of the cellular handset market. (b) Mobile data growth.

The rapid development of technology has compelled the release of standards for second generation (2G), third generation (3G), and fourth generation (4G) wireless communication systems. The standards include global system for mobile communications (GSM), code division multiple access (CDMA), Enhanced Data rates for GSM Evolution (EDGE), wideband CDMA (WCDMA), ultra mobile broadband (UMB), worldwide interoperability for microwave access (WiMAX), and long term evolution (LTE). Figure 1.2 shows the evolution of the 3rd generation partnership project (3GPP) standards. From 2G to 4G, the standards have evolved toward increasing efficiency, bandwidth, and data rates. For example, the 4G LTE standard requires peak-data rate up to 326.4 Mbit/s downlink and 86.4 Mbit/s uplink, while the 3G WCDMA standard requires peak-data rate of 384 Kbit/s for downlink and uplink.

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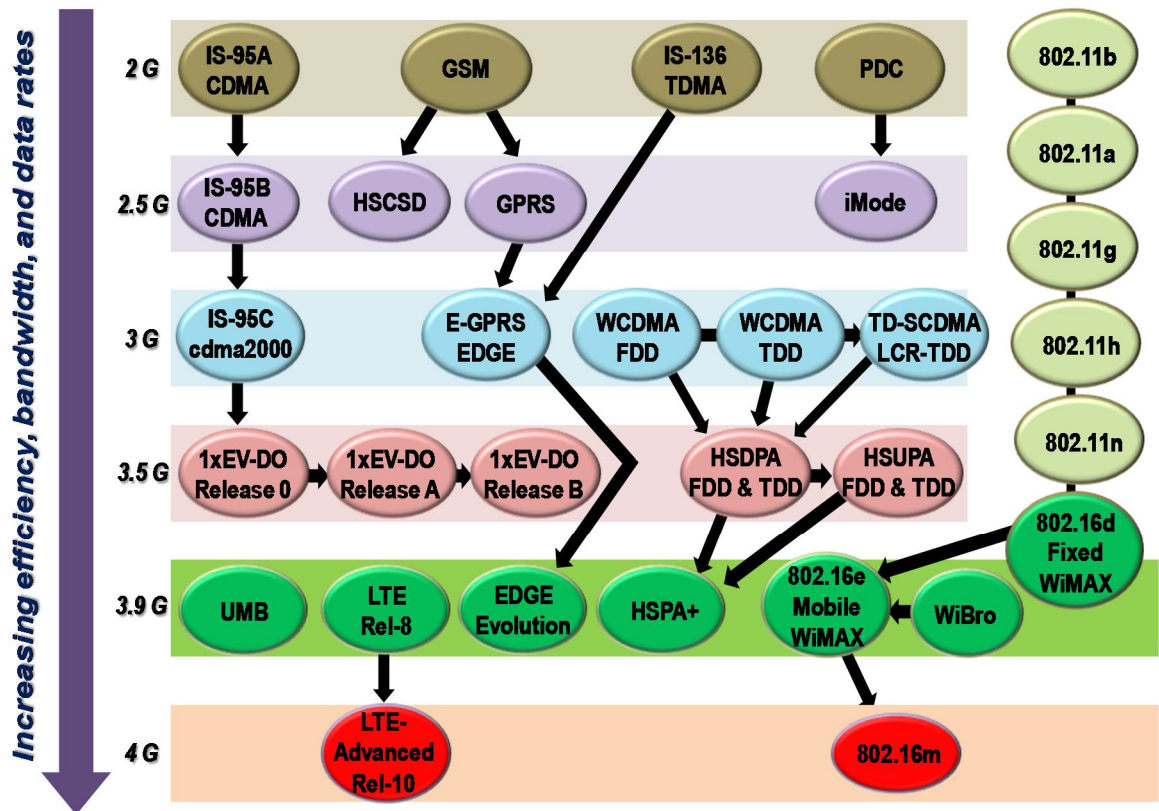
Figure 1.2 Evolution of 3GPP standards.

Figure 1.3 shows mobile phone sales by standards. The ratio of WCDMA applications, which have higher data rate communication than 2G, is continuously increasing and the 3G standards are becoming dominant in the mobile handset market.

In summary, the trend in the rapidly developing industry has moved toward the efficient operation and the high-data rate wireless communication systems. The WCDMA and the latest standard applications, which have higher data rate communications, will dominate the market and the necessity of linear PA that supporting the standard applications will increase.

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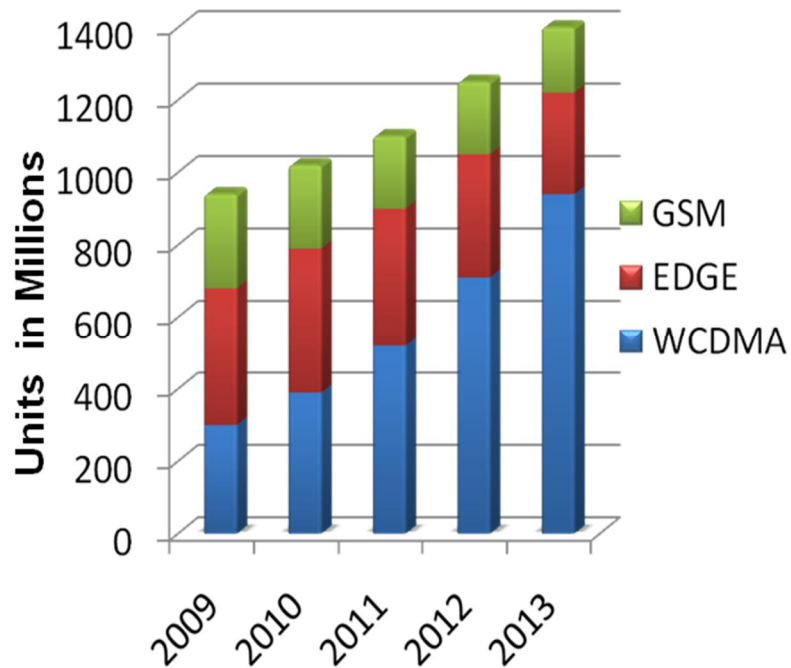
Figure 1.3 Mobile handset sales by standard.

1.2 Motivation

The wireless communication industry is becoming increasingly competitive in price as well as performance of its communication systems. For the price competitiveness, the complementary metal-oxide-semiconductor (CMOS) technology has lower wafer cost per area than other III-V compound technology. In addition, because most analog and digital circuits have been implemented by CMOS technology, this technology has been deemed an excellent candidate for benefiting both cost and performance through reductions in the front-end module costs and a high level of system integration.

Figure 1.4 presents a fundamental block diagram of a wireless communication system. Progress in CMOS technology has enabled the construction of most RF block circuits with enhanced performance in CMOS process. The complete integration of a

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single-chip transmitter in CMOS technology, however, is still constricted by power amplifiers (PAs) because of the inherent challenges of CMOS technology such as low breakdown voltage, low transconductance, poor linearity, an inaccurate RF model, and low substrate resistivity [1]. Most of the III-V compound technologies have been dominant in the PA handset market for various applications. However, because of the attractive advantages of low cost and high integration in CMOS technology, there has been a great deal of effort to overcome the drawbacks in CMOS PA and to implement a fully-integrated single-chip wireless system.
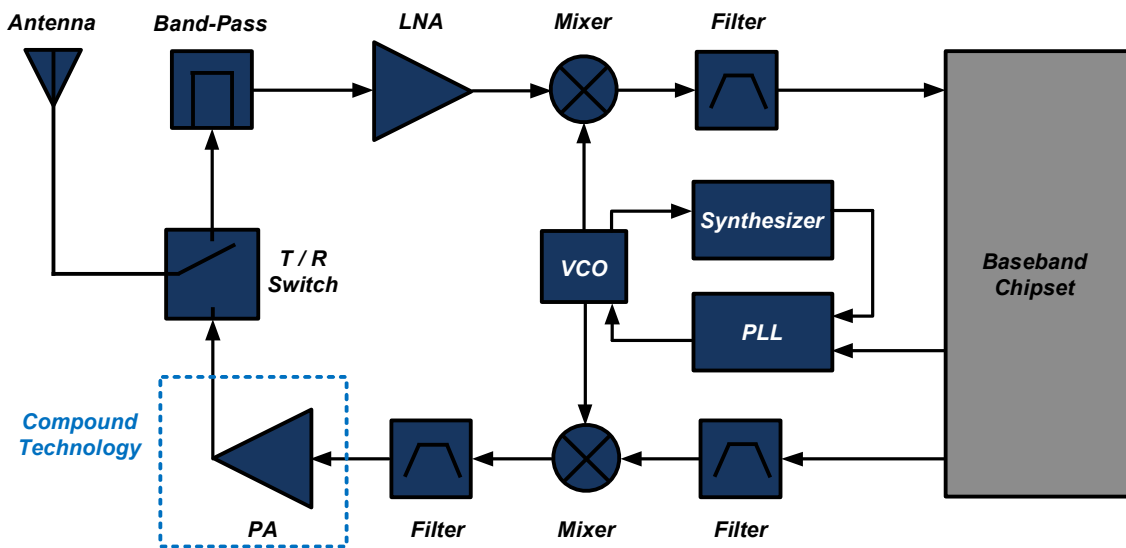
Figure 1.4 Fundamental block diagram of a wireless communication system.

As a second motivation of this work, the necessity of multi-mode operation is considered. With the mobility of wireless communication systems, the operating power of the systems varies. Figure 1.5 shows the basic idea of transmit power control for mobile devices. The mobile device transmits various levels of power, depending on the

distance from mobile devices to base stations. That is, the mobile device transmits strong power to communicate with a base station that is far away while it transmits weak power to one in a short distance, thereby continuously varying the operating output power of the wireless communication system. The probability of the system operation of transmit power control is studied for the efficient operation of the system, and the probability distribution functions (PDF) of DG 09 voice and data are shown in Figure 1.6. According to the PDF of the transmitted signal, the PA is more likely to be operated at a lower power level for voice communication and at a peak power level for data communication [2][3]. To extend the battery life of mobile devices, the efficiency of PAs must be optimized at both back-off power and peak power levels. Multi-mode operations can provide enhancement of the PA efficiency at a low output power level as well as minimizing quiescent currents, thereby increasing the battery life of the whole system.
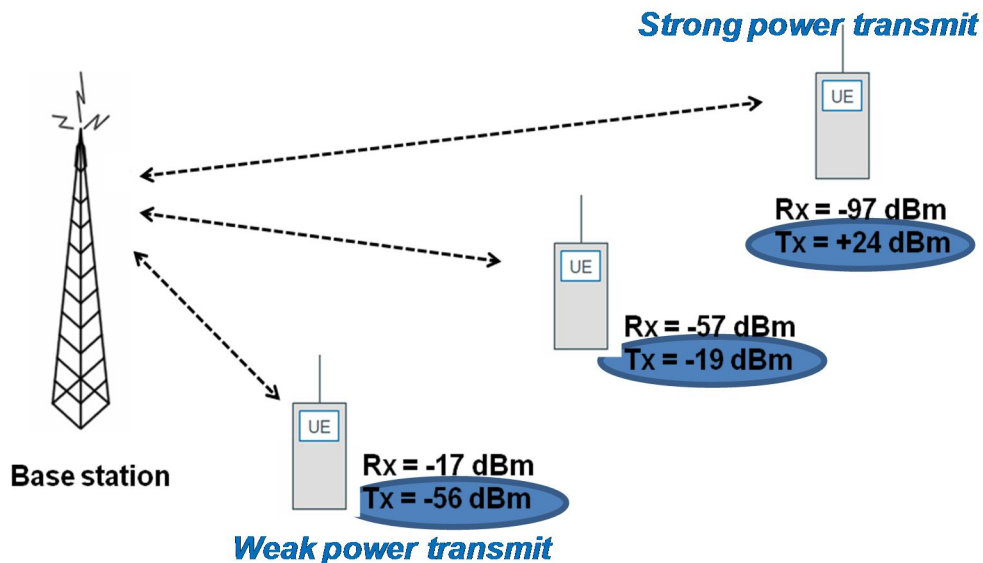
Figure 1.5 Transmit power control depending on the distance between the user and the base station.

Lastly, the load variation immunity of wireless system is contemplated. The changes of the operating environment conditions of wireless communication system, such as the changes in antenna impedance and contacts with conductive or grounded surfaces can cause load impedance variations. The load impedance mismatch under uncontrolled environment conditions can degrade the system performance and even cause critical reliability problems of wireless communication devices. The Apple's smartphone, Iphone 4, which experienced performance degradations by touching certain places of the phone, is an example for why the system should be immune to load impedance variation.
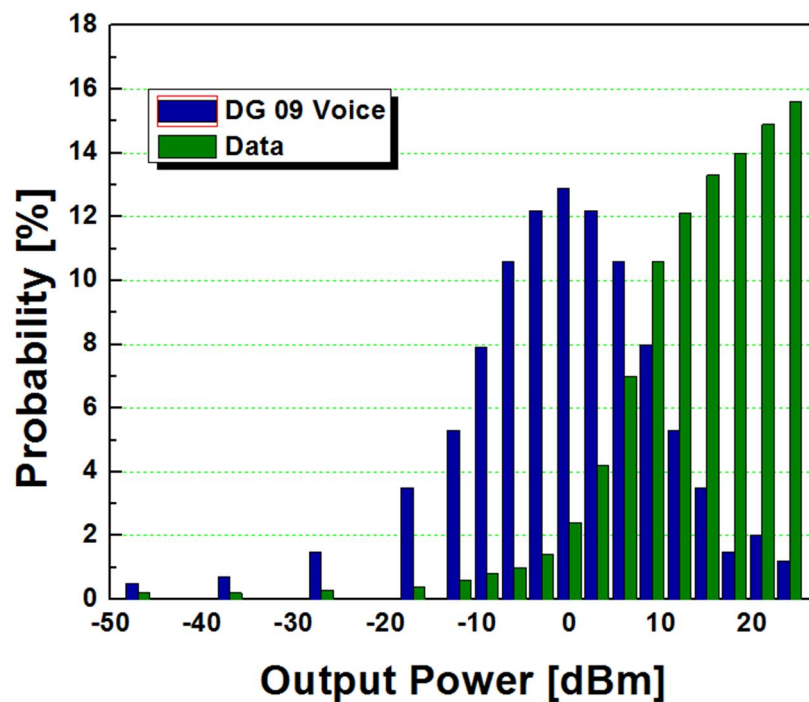
Figure 1.6 Probability distribution function of DG 09 voice and data.

This dissertation examines highly efficient CMOS PAs for wireless communication systems. In its examination, it covers the background of CMOS PA design, and the design parameters of the PA, including linearity, efficiency, gain, reliability, output power, and stability, all of which contribute to optimal PA performance. Then it analyzes the challenges of CMOS technology for PA design, and more specifically, investigates balanced PA configuration for load insensitivity and efficiency enhancement in back-off output power level by employing multi-mode operations.

This dissertation focuses on the following and includes three original contributions:

1. Development of a novel cascode feedback bias technique that is easily applicable to multi-stage cascode topology, and that improves linearity and alleviates the reliability issue of the PA.

2. Implementation of the first highly efficient balanced CMOS PA that addresses the load immunity of WCDMA applications.

3. Introduction of the first triple-mode balanced CMOS PA using a switched integrated passive device (IPD) quadrature coupler, including an analysis and demonstration of the concept of utilizing the isolation port of the quadrature coupler as a signal path with RF switches.

1.3 Organization of dissertation

This dissertation is organized as follows:

Chapter 1 presents the technology trends and market demands for wireless communication systems and introduces the motivation of this research for a highly

efficient CMOS PA with improvement of linearity and reliability, load immunity and multi-mode operation.

Chapter 2 reviews the background knowledge of the PA and prior attempts to overcome the obstacles to PA design.

Chapter 3 discusses the challenges of CMOS PA design, including the lossy substrate, the low quality factor of passive components, reliability, and nonlinearity issues of CMOS technology.

Chapter 4 proposes the cascode feedback bias technique that enhances linearity and alleviates the reliability problem of the single-ended CMOS PA, and presents a highly efficient linear CMOS PA for the WCDMA application.

Chapter 5 presents the balanced PA topology, analyzes its advantages, which are load immunity, matching network improvement, constant gain and enhanced stability, and demonstrates the implementation of a balanced linear CMOS PA for WCDMA applications.

Chapter 6 introduces the triple-mode balanced linear CMOS power amplifier using switched quadrature coupler. To enhance the efficiency at back-off power levels and reduce quiescent current, the PA utilizes triple-mode operations, and employs a balanced topology for load insensitivity. To obtain low loss and a high quality factor (Q) of passive output combining, a transformer-based quadrature coupler is implemented using a silicon-based integrated passive device (IPD) process.

Chapter 7 concludes the dissertation by summarizing the main contributions.

CHAPTER 2

RF POWER AMPLIFIERS

2.1 Introduction

Achieving desirable performance of a PA entails various RF PA challenges and design considerations. The key design parameters of the RF PA can be classified into efficiency, linearity, gain, output power, reliability, and stability, all of which involved trade-offs as shown in Figure 2.1. This chapter summarizes the background of the RF PA and reviews past approaches to enhancing its efficiency, linearity, and output power.
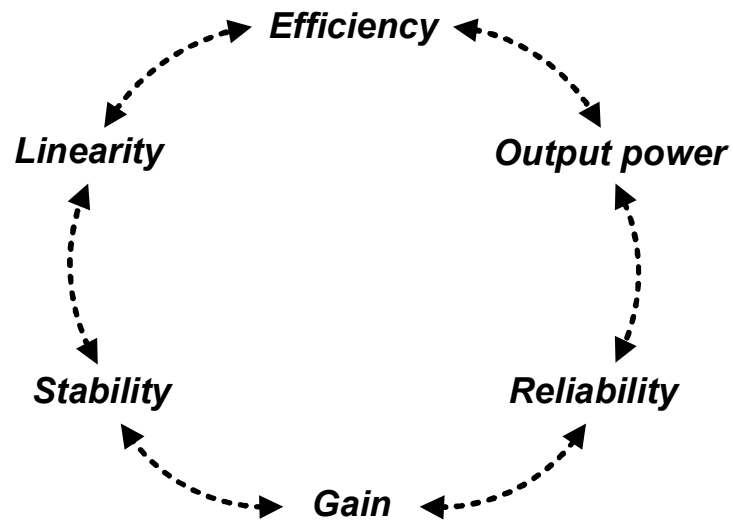
Figure 2.1. PA design parameters and trade-offs.

2.2 Key design factors of RF PA

2.2.1 Efficiency

As a brief definition, the PA is a block that converts the DC power to RF power by amplifying input signals, as shown Figure 2.2. Because the PA is the most "power-hungry" block in the wireless communication system, efficiency is considered the most important factor in the PA performance. The efficiency of the PA is defined as

$$\eta = \frac{P_{OUT}}{P_{DC}} \tag{2.1}$$

where P_{OUT} is the power delivered to the output and P_{DC} is the power consumption of the PA, and it is called the drain efficiency (DE) for the PAs with FET transistors or the collector efficiency (CE) for the PAs with BJT transistors.
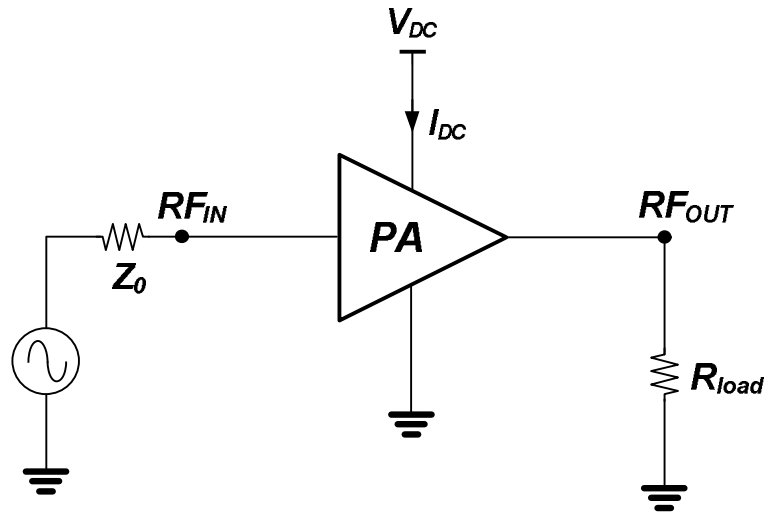
Figure 2.2. Brief definition of a power amplifier.

The power-added efficiency (PAE), the ratio of the RF power of the PA to the DC power consumption, is also defined as equation (2.2). The PAE includes the gain information of the PA, and it is almost same with DE/CE when the gain is high enough.

$$\eta_{added} = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.2}$$

where P_{IN} is the power delivered from the input.

The maximum efficiency of the PAs is determined by the operation of the PA that is based on the voltage and current waveforms at the output. The classes of the PAs categorize into two types: linear PA and switching PA operations. The linear PA operation includes class A, AB, B, and C, while the switching PA operation includes class D, E and F. Table 1 summarizes the classes of PA operations in terms of efficiency, and linearity.

TABLE 1. CLASSES OF AMPLIFIER OPERATION.

Classification	A	AB	B	C	D	E	F
Maximum Efficiency (%)	50	50-78.5	78.5	100	100	100	100
Linearity	Excellent	Good	Moderate	Poor	Poor	Poor	Poor

As presented in Table 1, the efficiency and the linearity are in trade-off for the linear PA operation. Because both efficiency and linearity can be optimized in the class AB operation, it is the most popular choice for linear PA designs. Moreover, class AB operation has a slightly larger fundamental current amplitude compared to class A or B operations, accompanying the increased output power to the load.

2.2.2 Linearity

Because the PA is a nonlinear component, the linearity is one of the key features of the PA performances. The linearity of the PA can be represented by the 1-dB gain compression point (P_{1dB}), the amplitude-to-amplitude distortion (AM-AM), the amplitude-to-phase distortion (AM-PM), the third-order intercept point (IP3), the error vector magnitude (EVM) and the adjacent channel leakage ratio (ACLR) for out of band.
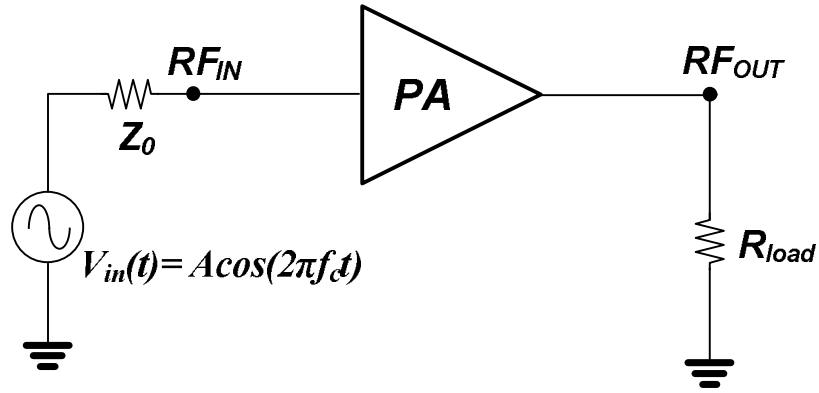
Figure 2.3. Distortion generations of a nonlinear PA.

The distortions of the PA can be mainly caused by 1) clipping at the large AC signal swings and 2) disrupting by the non-linear transconductance at small AC signal swings. Moreover, the transconductance distortion at the small AC signal swings (i.e., low amplitude signals) can be categorized into the harmonic distortion by a single carrier and the intermodulation distortion by multi-carriers (i.e., modulated signals). Figure 2.3 shows the harmonic generations of the non-linear PA by a single carrier of $Acos(2\pi f_c t)$. The harmonic generation is derived by the power series, as shown in equation (2.3), (2.4) and (2.5).

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$$V_{out}(t) = G[v_{in}(t)] = g_0 + g_1 v_{in}(t) + g_2 v_{in}(t)^2 + g_3 v_{in}(t)^3 + \cdots \tag{2.3}$$

$$V_{out}(t) = g_0 + g_1 A\cos(2\pi f_c t) + g_2 A^2 \cos^2(2\pi f_c t) + g_3 A^3 \cos^3(2\pi f_c t) + \cdots \tag{2.4}$$

$$V_{out}(t) = g_0 + \frac{g_2 A^2}{2} + (g_1 A + \frac{3 g_3 A^3}{4})\cos(2\pi f_c t) + \frac{g_2 A^2}{2}\cos(4\pi f_c t) + \frac{g_3 A^3}{4}\cos(6\pi f_c t) + \cdots \tag{2.5}$$

From the power series expansion, g_3 term and higher order terms cause the distortion of the linearity, specifically, the dominated g_3 term at the high power level results in the gain compression because of its negative sign. General wireless communication standards require the specific amount of power back-off to meet the stringent IMD or ACLR specifications. The P_{1dB} can be derived from the transconductance characteristic, as shown in equation (2.6).

$$P_{1dB} = \frac{g_1^2 A_{1dB}^2}{2 R_L} \cdot 10^{-1/10} \tag{2.6}$$

where A_{1dB} is the input power level that the fundamental term is decreased by 1-dB.

The third order intermodulation distortion (IMD3), which is generated by two tone carriers, is an important parameter that indicates the linearity of the PA. While the most of harmonic signals and higher frequency signals can be easily filtered out, the intermodulated components of the signals at the frequency of $2f_1 - f_2$ and $2f_2 - f_1$ are difficult to be filtered out, which degrades the linearity of the PA.

Figure 2.8 shows the third order intercept point (IP3) that is the virtual intercept point of the fundamental signal and the third-order intermodulated signal (i.e., IMD3). Because the increasing ratio of the IMD3 is three times larger than that of the fundamental signal, they can be extrapolated to be intercepted at the *IP3* point, as shown

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in Fig. 2.4. The P_{1dB} and the output referred IP3 (OIP3) have a theoretical relation of $OIP3 = P_{1dB} + 9.6dB$.
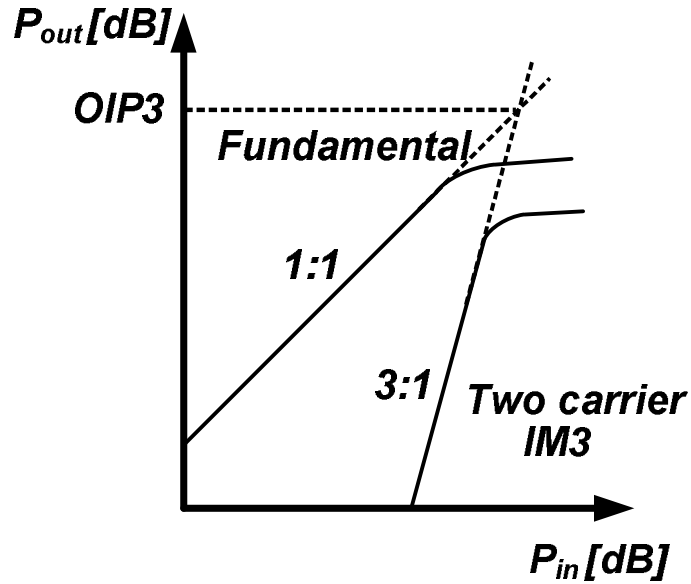
Figure 2.4. Definition of the third-order intercept point.

The AM-PM distortions caused by non-linear reactive impedance can result in a time-varying phase distortions, and it can degrade the linearity of the PA as well. Specifically, the input capacitance between the gate and the source, C_{gs}, is well known for the dominant source of AM-PM distortion.

The ACLR, the ratio of the signal power level at the center of the main channel to the signal power level at a specific offset in the adjacent channel, is the critical linearity specification of the code division multiple access (CDMA). Figure 2.9 presents the ACLR spectrum of the modulated signals. Usually, the ACLR specification of the PAs is more stringent than the EVM specification for WCDMA applications.
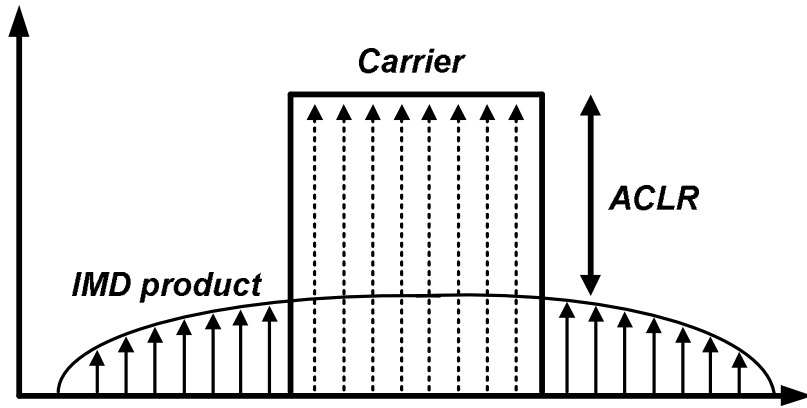
Figure 2.5. ACLR spectrum of the modulated carrier signal.

2.2.3 Output power and stability

The output power of a PA is an important in the evaluation of PA performance. Output power is defined as

$$P_{out} = \frac{V_{out}}{\sqrt{2}} \cdot \frac{I_{out}}{\sqrt{2}} = \frac{V_{out}}{\sqrt{2}} \cdot \frac{V_{out}}{\sqrt{2}R_L} = \frac{V_{out}^{2}}{2R_L} \qquad (2.7)$$

With the power supply voltage and the desired output power, the output impedance can be calculated. Because of the power restrictions of a transistor such as breakdown voltage, device impedance, and limited supply voltage, output power combining can be an effective way to avoid the reliability problems of technology and achieve higher output power.

The stability of PA should carefully be considered over frequency. The necessary and sufficient conditions for the PA to be unconditional stable are that the stability factor (K) is greater than unity and the stability measure factor (B) is positive. Derivations of stability factor and stability measure factor are shown in equation (2.8) and (2.9). The

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Mu factor, which represents the distance from the center of the Smith chart to the nearest output load stability circle, be used for the additional stability factor, and it requires greater than unity for unconditional stability. The unconditionally stable condition of PA should be satisfied with the small signal over frequency as well as the large signal of the operating frequency range.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \qquad (2.8)$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0 \qquad (2.9)$$

$$Mu = \frac{1 - |S_{11}|^2}{\{|S_{22} - *S_{11} \cdot (S_{11}S_{22} - S_{12}S_{21})| + |S_{12}S_{21}|\}} > 1 \qquad (2.10)$$

2.3 Prior arts

2.3.1 Linearity enhancement techniques of a PA

Wireless communication systems have been focus of a wide range of linearity improvement techniques. Concepts for linearity improvement such as predistortion, feedback, and feedforward techniques have been developed and adopted successfully in various applications. Also, at the device level, the efforts have been proposed toward improving linearity using harmonic traps and reducing the capacitive component variation.

2.3.1.1 Predistortion linearization technique

The predistortion (PD) linearization technique is conceptually simple. The basic concept of PD is to achieve a linear function of input, illustrated in Figure 2.10. At the

front of the PA, a predistorter provides an inverse function of the amplitude and phase distortion that the PA generates.

$$Y(t) = G(Z(t)) = G(F(X(t)))$$ (2.11)
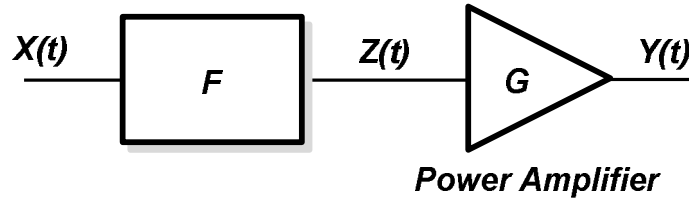
Figure2.6. Basic concept of the predistortion system.

The PD can be categorized as an analog PD, a digital PD, and a hybrid PD. Among the advantages of analog PD are their size, cost, and ease of implementation with RF PAs. However, exact PA models are required to predistort against the nonlinearity of the PA, and intermodulation distortion (IMD) suppression can be limited due to the lack of accuracy, so it generally focuses on the reduction of third order intermodulation distortion [4]-[6].

Compared to analog PD, digital PD provides superior linearity enhancement performance, and the correction is insensitive to temperature, supply voltage and device variation because of the inherent digital operation. However, a digital PD circuit requires complex, DSP-based system architecture, and the operational bandwidth is limited by the speed of digital circuits. Moreover, large DC power consumption for DSP operations is required, and the long time constant envelope memory effects of the PAs can be a bottleneck to further linearization [7][8].

Figure 2.11 depicts the hybrid PD linearization system, which implementing analog envelope PD and digital envelope PD simultaneously. The Hybrid PD compensates for the drawbacks of analog EPD and digital EPD, such that the digital EPD system provides accurate linearization while the analog EPD system makes up for the long-time memory effect that cannot be corrected by digital EPD [9].
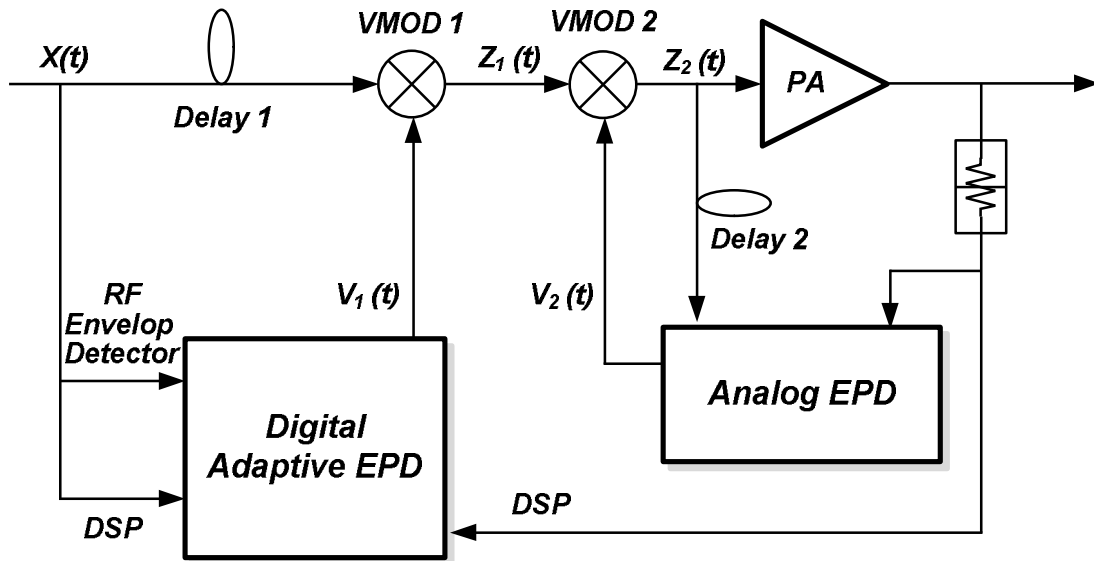
Figure 2.7. Digital/analog predistortion system.

It is generally known that analog PD provides 5 to 10 dB adjacent channel leakage ratio (ACLR) enhancements and digital PD provides more than 20 dB ACLR enhancements. Because predistortion occurs before amplification, the low power levels are handled for linearization so that they reduce the efficiency degradation of the system.

2.3.1.2 Feedforward linearization technique

The feedforward technique is known as the technique most effective at enhancing the linearity of a PA system [10]. Achieving 20 to 30 dB IMD/ACLR reduction, it can be employed for wideband linearization. Figure 2.12 describes the basic feedforward system. The feedforward system has two cancellation loops; the signal cancellation loop and the error cancellation loop. In the signal cancelation loop, the attenuated output signal is subtracted by the input signal, providing an error signal. In the error cancellation loop, the distortion of the PA is subtracted by the amplified error signal, suppressing the distortions of the PA. However, the imbalanced power summations between the main signal and the error signal are very critical, and the system is quite complicated, resulting in a physically large size. In addition, because a power summation occurs at the PA output, large losses can occur by the delay line and the combiner, lowering the efficiency of the system.
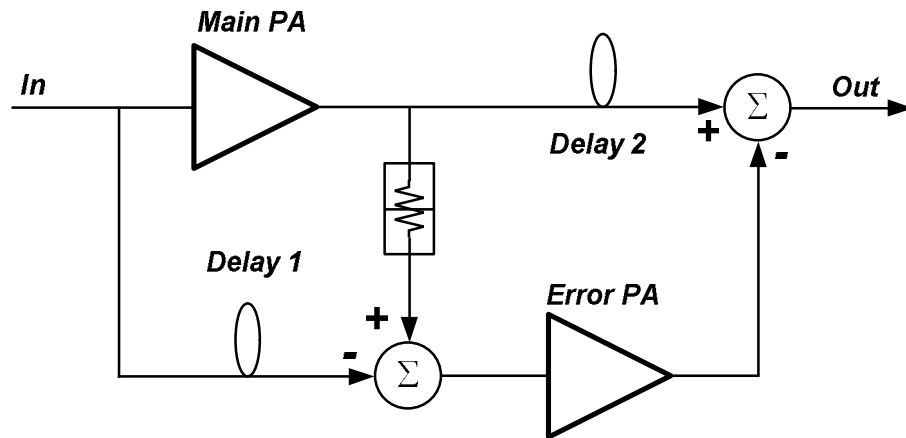
Figure 2.8. Feedforward system.

2.3.1.3 Feedback linearization technique

The feedback linearization technique is one of the most popular linearization techniques in analog and RF areas, reducing the distortion by a factor of loop gain. The simplest negative feedback system, shown in Figure 13, linearizes by driving the output to follow the input. In RF, however, the operating signal bandwidth is a main bottleneck for employing feedback linearization, and delays from the feedback loop can cause instability of the system.
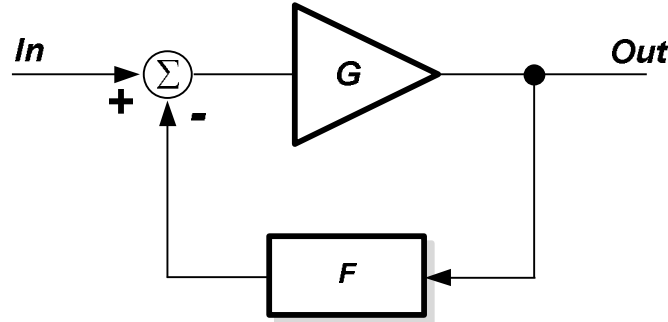
Figure 2.9. RF feedback system.

Envelope feedback alleviates the problem of delay by employing the signal envelope as the feedback parameter, and polar-loop feedback, which is added phase-locked loop to envelope feedback, enables the correction of the AM-PM distortion effect that cannot be controlled by envelope feedback [11][12]. However, polar-loop feedback suffers from the demands of the extremely large bandwidth of the phase feedback path compared to amplitude bandwidth, resulting in non-optimized performance of the system.
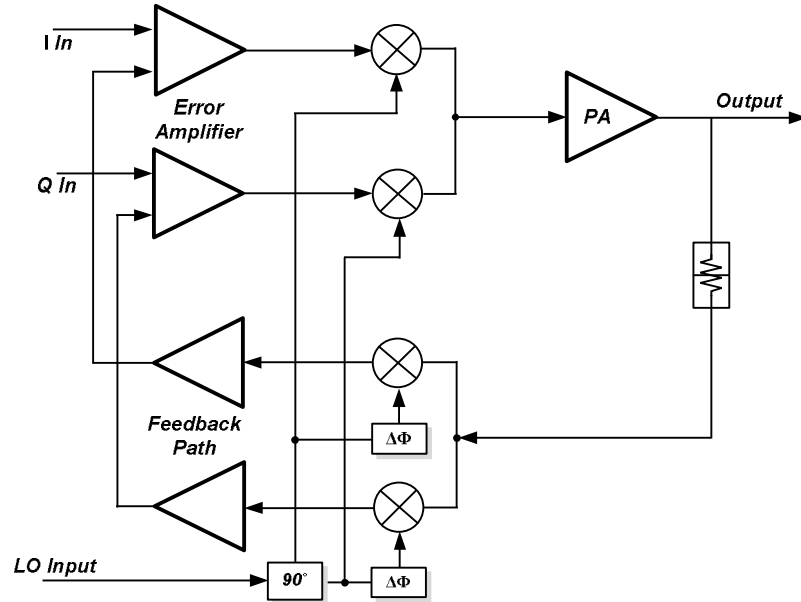
Figure 2.10. Cartesian feedback system.

Cartesian feedback relieves problems resulting from different bandwidth requirements by utilizing modulation feedback, and requires approximately the same bandwidth as that of the in-phase and quadrature-phase components [13]. As shown in Figure 2.14, Cartesian feedback consists of two identical feedback paths operated independently with the in-phase and quadrature channels. It performs down-conversion of the separated output of the in-phase and quadrature phases to the baseband frequency and feedback to the input, achieving two feedback paths. Although feedback linearization shows excellent performance, bandwidth limitations restrict it from performing wideband applications.

2.3.1.4 Harmonic traps

The harmonic trap is one of the simplest ways to enhance linearity of the PA. Utilizing the inductor and capacitor in series, it can terminate the signals of resonance frequency. Figure 2.15 depicts harmonic traps applied in the PA.

$$\omega^2 = \frac{1}{LC} : Resonance\, frequency \qquad (2.12)$$

Generally, the second and the third harmonic signal traps are employed at the input or the output in the multi-stage configuration. The prior work of using the second harmonic trap reported 6 dB of IMD3 improvement [14]. However, achieving the desired effects requires the accurate simulations and implementation, because the resonance frequency is vulnerable to mismatch due to unexpected implementation conditions.
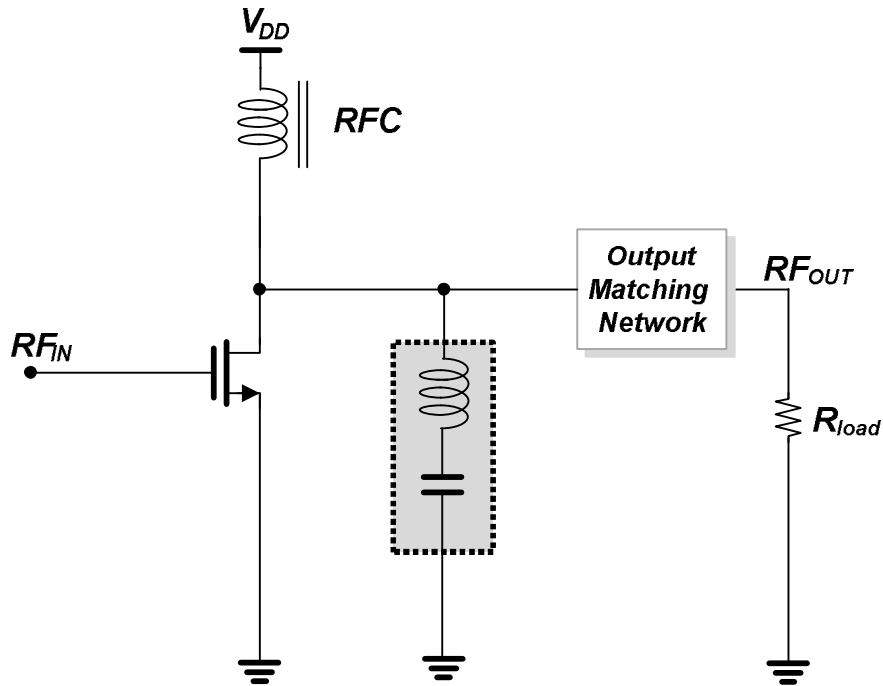
Figure 2.11. **Harmonic traps of the PA.**

2.3.1.5 Capacitance cancellation technique

The capacitance-compensation technique is applicable to CMOS PA for enhancing linearity. The intrinsic capacitances exist between the ports of transistors, specifically, the gate-source capacitor, C_{gs}, of common source transistor is a major source of nonlinearity under the g_m and g_{ds} optimized linear class AB operation [15]. The variation of input capacitance by large signal originates phase distortions. Figure 2.16 shows the concept of the capacitance-compensation technique. Because input capacitance of PMOS transistor has the reverse transition to that of NMOS transistor, by connecting the gate node of the PMOS transistor to the gate node of NMOS transistor, changes of C_{gs} in the NMOS transistor are compensated by those of C_{gs} in the PMOS transistor, preventing linearity degradation by AM-PM distortion. This prior art that employs this technique represented 8 dB of IMD 3 and ACLR improvement [16].
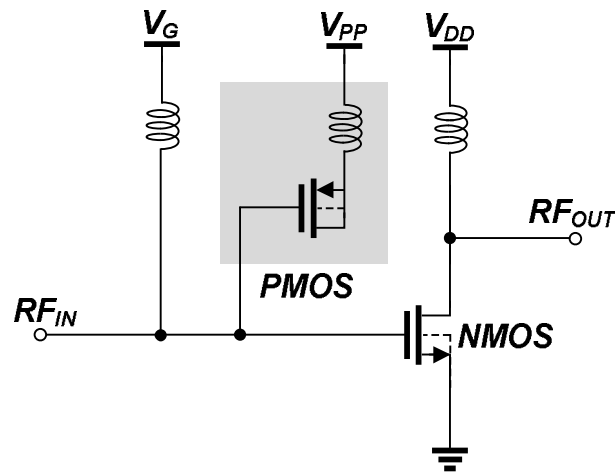
Figure 2.12. **Concept of the capacitance-compensation technique.**

2.3.2 Efficiency enhancement techniques of a PA

A great deal of effort has been devoted to improving the efficiency of PA operations through approaches such as the envelope elimination and restoration (EER) PA, the outphasing PA, Doherty PA and the envelope tracking system [17]-[22]. Among the efficiency enhancement techniques, the Doherty technique provides low power-level efficiency improvement. Because of this characteristic of this technique, it can be useful in the mobile handset, satisfying recent demand of the mobile handset market. Figure 2.4 shows the concept of the Doherty PA, which consists of a main PA, an auxiliary PA, and impedance inverters, so called quarter-wave transformers.
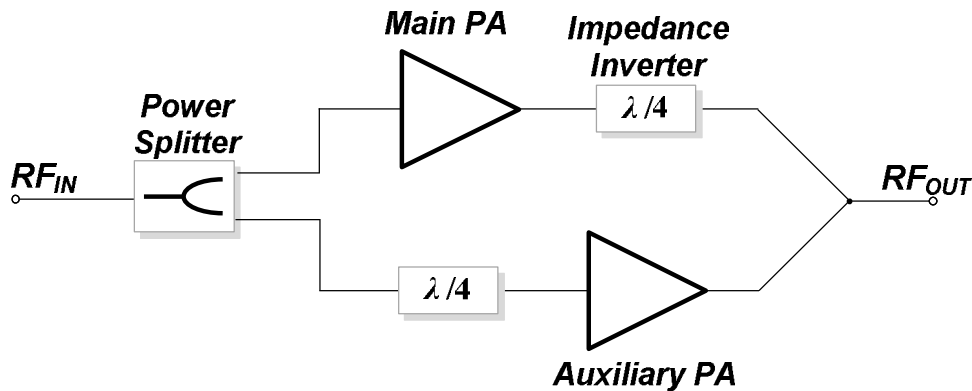
Figure 2.13. **Configuration of the Doherty PA.**

While the main PA usually has the bias of class B operation, the auxiliary PA has the bias of class C operation, such that the main PA operates alone until the input power is large enough to turn on the auxiliary PA. As the input power increases, the auxiliary PA turns on such that it supports the output power of the entire Doherty PA system, as shown in Figure 2.5(a). The overall efficiency is shown in Figure 2.5(b). The high efficiency at the back-off output power level is achieved by using the technique.
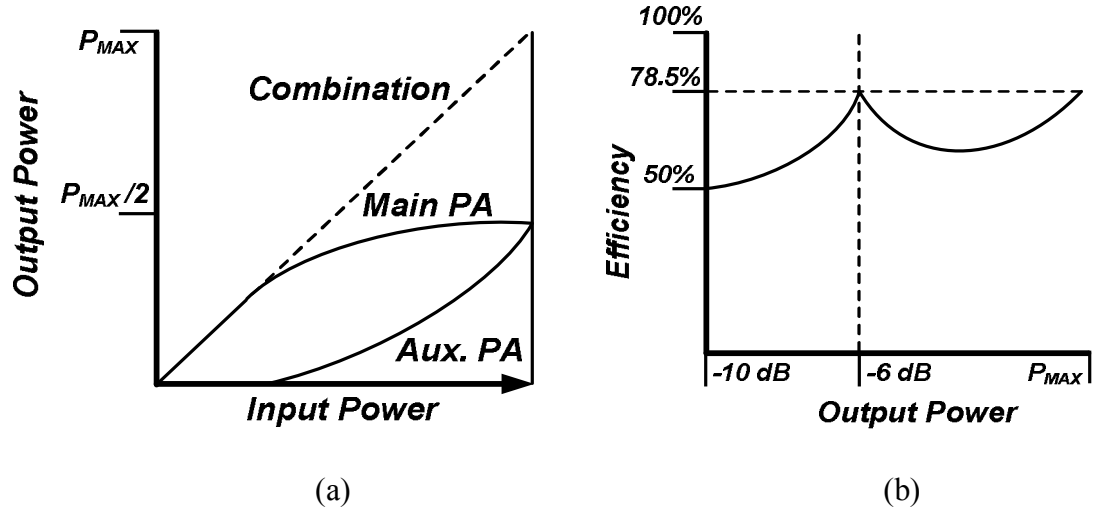
Figure 2.14. (a) Output power characteristics of the Doherty PA. (b) Efficiency characteristics of the Doherty PA.

2.3.3 Output power improvement techniques of a PA

As shown in Figure 2.17, the Wilkinson divider/combiner for in-phase combining is a well known method. For quadrature combining, the branch-line coupler and coupled-line directional couplers, which are often implemented using a microstrip or a stripline, can be used [23]. The push-pull PA shown in Figure 2.18, two identical PA biased class B that are driven differently, provides power combining and it has even product and harmonic cancellation merits [19]. A parallel topology based on a lattice-type LC balun can be attractive solutions [24].
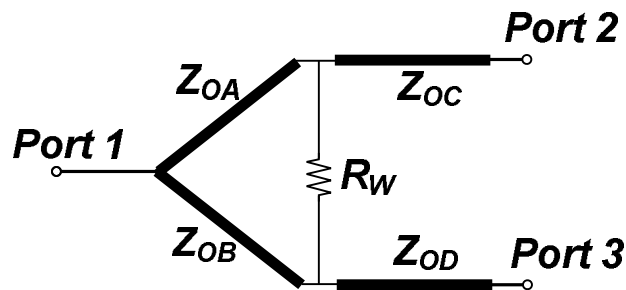
Figure 2.15. Wilkinson power divider/combiner.

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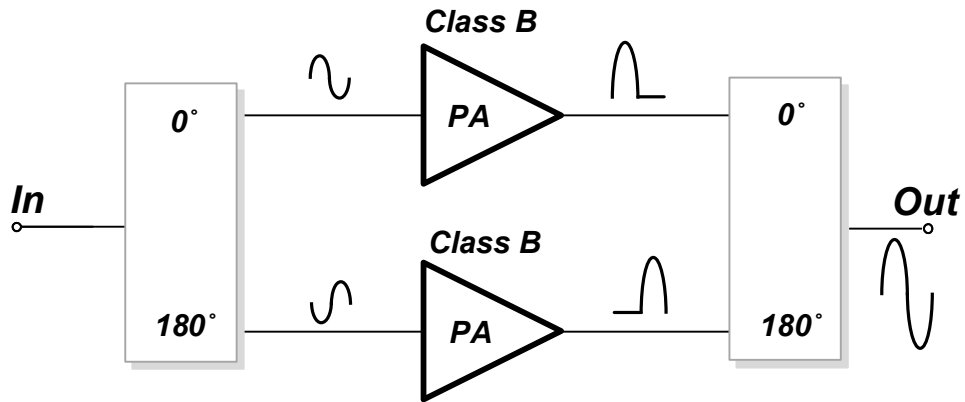
Figure 2.16. Push-pull power amplifier.

Transformer power combining, achievable in CMOS integration, provides the function of power combining as well as an impedance transformation for output matching. The distributed active transformer introduced by I. Aoki represents a series-combining transformer that combines voltage at the load, as shown in Figure 2.19 [25][26], and a parallel-combining transformer proposed by K. H. An presented in Figure 2.20 [27]. In the transformer type power-combining technique, lower input impedance, higher power combining ratio, and higher transformer efficiency are preferred to achieve better performance of the power combining.

A series-combining transformer has smaller input impedance as the power-combining ratio increases, enabling a large voltage swing when multiple PAs are combined. However, for input impedance, the power combining ratio can be sensitive to the parasitic resistance of the primary inductor. Furthermore, transformer efficiency is strongly dominated by the physical size of the secondary inductor, which is normally large when the number of combining PAs increases.
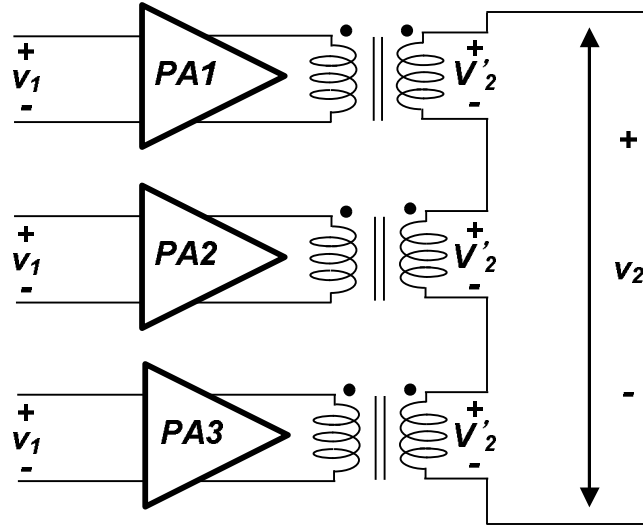
Figure 2.17. Series combining transformer.
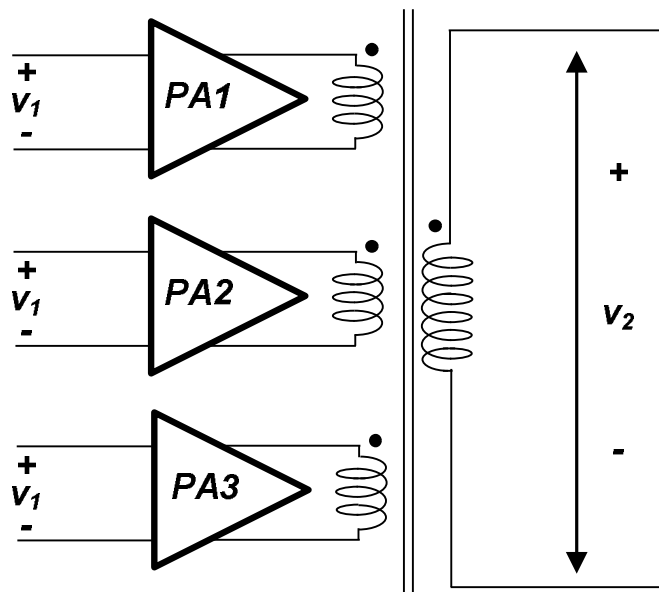
Figure 2.18. Parallel combining transformer.

A parallel-combining transformer combines power in the current domain, and the input impedance and the power-combining ratio are less sensitive to the parasitic resistance of the primary inductor compared to series power combining. However, the

input impedance increases as the number of combined power stages increases, which degrades the optimal matching conditions of individual PAs, which in turn weaken the overall efficiency of PA performance. Both techniques demonstrate excellent power-combining performance and usability for CMOS power amplifiers.

CHAPTER 3

CHALLENGES OF THE CMOS POWER AMPLIFIER

3.1 *Challenges*

Although CMOS technology has merits of low cost and high integration potential, it has inferior performance compared to III-V compound technology because of its low transconductance, low quality factor of passive components, lossy substrate, reliability and so on. The III-V compound technologies including metal-semiconductor field-effect-transistor (MESFET), pseudomorphic high electron mobility transistor (pHEMT), and Gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) with InGaP emitter have been dominant in designing the PA for various applications of the handset market, while PAs in CMOS technology have been released for only some applications such as Bluetooth, and GSM/GPRS. Table 1 shows a comparison of the GaAs and silicon technology properties. The table shows that the electron mobility of the GaAs HBT process is six times faster than that of CMOS technology. Therefore, it is not surprising that the PAs using CMOS process inherently have poorer performances compared to the PAs using III-V technology. However, because of the potential of CMOS technology to lower the production cost and facilitate integration, a great deal of effort has been dedicated to overcoming its drawbacks of CMOS technology, specifically, efficiency, linearity, and output power. In this chapter, the design challenges of CMOS PA will be discussed.

TABLE 2. COMPARISON OF SILICON VERSUS GaAs TECHNOLOGY.

Properties	Silicon	GaAs
Electron mobility $[cm^2/(V \cdot sec)]$	1400	8500
Resistivity $[\Omega - cm]$	10	10^6
Permittivity	11.8	12.9
Thermal conductivity $[W/(cm \cdot K)]$	1.49	0.55
Wafer size [inch]	8~12	4~6
Wafer cost	Cheap	Expensive
Energy band gap [eV]	1.12	1.424

3.2 Lossy substrate of CMOS technology

As shown in Table 1, CMOS technology has low substrate resistivity (10 Ω-cm) compared to GaAs technology (10^6 Ω-cm). Because RF blocks are built up on a bulk substrate, a highly resistive substrate will provide better isolation between the RF blocks. In RF blocks with a low resistive silicon substrate, the signal flowing passive components can be coupled to neighboring blocks through the silicon substrate, shown in Figure 3.1. Specifically, a PA that generates large signal swings can create critical noise coupling to neighboring blocks such as low noise amplifier (LNA), and phase locked loop (PLL), interrupting proper operation of the blocks. Thus, to strengthen the isolation between the

RF blocks, a triple-well CMOS process (deep N-well) and guard-rings are usually employed in CMOS PA design.
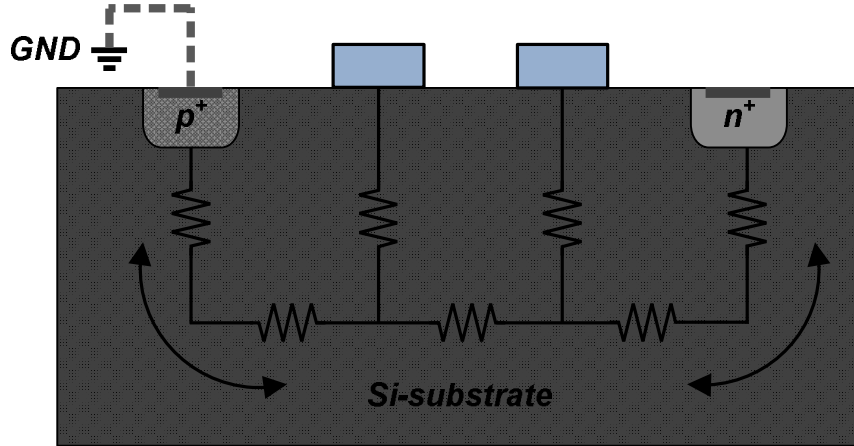
Figure 3.1. Signal coupling in the silicon substrate.

3.3 Losses of CMOS technology

3.3.1 Low quality factor of passive components

The low quality factor of passive components is also a challenge of CMOS PA. The definition of quality factor, the ratio of stored energy per cycle to the dissipated energy per cycle, is expressed as (3.1), and the quality factors of the inductor and capacitor are defined as (3.2) and (3.3), respectively.

$$Q = \frac{2\pi \cdot Energy_{stored/cycle}}{Energy_{dissipated/cycle}} \tag{3.1}$$

$$Q_L = \frac{2\pi \cdot \dfrac{1}{2}LI^2}{\dfrac{1}{2} \cdot I^2 R_s \cdot \dfrac{2\pi}{\omega_o}} = \frac{\omega_o L}{R_s} = \frac{2\pi f_o L}{R_s} \tag{3.2}$$

where R_s is the series resistance, f_0 is resonant frequency, and L is inductance.

$$Q_C = \frac{2\pi \cdot \frac{1}{2} C V^2}{\frac{1}{2} \cdot \frac{V^2}{R_P} \cdot \frac{2\pi}{\omega_o}} = \omega_o R_P C = 2\pi f_o R_P C \tag{3.3}$$

where R_p is the parallel resistance, f_0 the resonant frequency, and C the capacitance.

In a low resistivity substrate, the stored energy of passive components is dissipated through the lossy substrate, degrading the efficiency of the PA. Specifically, the quality factor of the inductor is one of the most critical factors to overall PA efficiency. Because the inductor in CMOS process has an inductor quality factor of less than 10, it can cause the low efficiency of CMOS PA. Therefore, integrated passive device (IPD) technology, which has an inductor quality factor of more than 25, can be employed for the high quality factor of passive components in CMOS PA design.

3.3.2 Eddy current

Eddy current is a source of degradation in the quality factor of inductors. Figure 3.2 shows the generation of eddy current in a substrate. When current flows through the inductor, eddy current is induced in the substrate in the opposite direction to the inductor current. Because silicon substrate has low resistivity, a considerable amount of eddy current originally generated in conductor is induced in the silicon substrate. Since the magnetic field generated by the eddy current compensates for the original magnetic field of the inductor, it reduces the energy stored in the inductor and in turn, weakening the quality factor of the inductor.
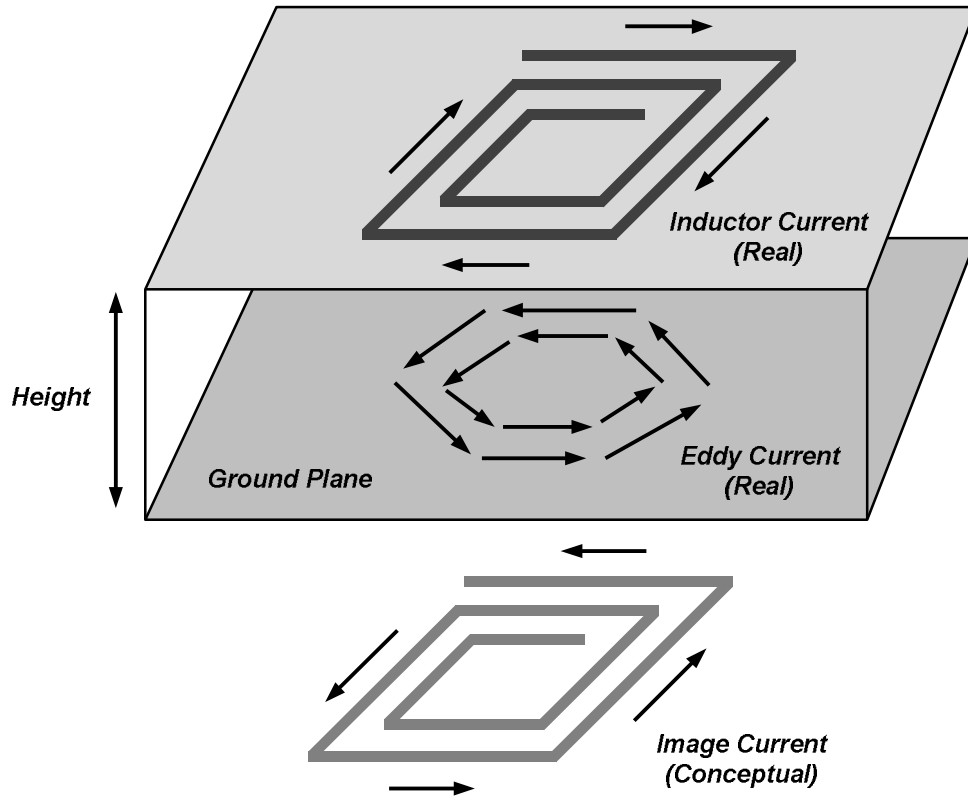
Figure 3.2. Generation of the eddy current in the silicon substrate.

3.3.3 Skin effect

The skin effect is the propensity of an AC current to flow to the outer side of the conductor as the frequency increases. The expression of skin depth is shown as (3.4).

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{3.4}$$

where δ is the skin depth, f the frequency, ρ the resistivity of the conductor, and μ (H/m) the absolute magnetic permeability of the conductor. The cross-section of a wide inductor is shown in Figure 3.3. As the frequency becomes higher, the skin depth

decreases, such that the current distribution of the conductor is biased to the outer skin of the conductor, resulting in an increase in the effective resistance of the conductor. That is, in the RF frequency, the skin effect can increase the resistance of passive components, thereby, degrading the quality factor of the inductor.
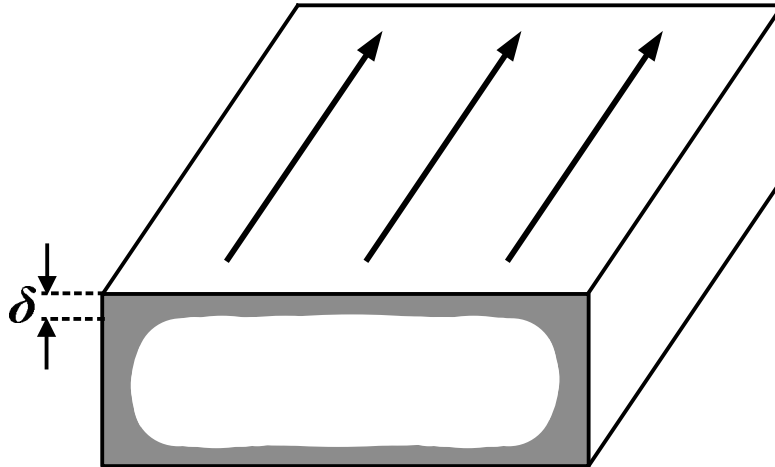
Figure 3.3. Skin effects in the wide conductor.

3.4   Reliability problems of CMOS technology

The most significant problem in CMOS PA design is reliability. The common reliability problems of CMOS technology are the mechanisms of time-dependent gate-oxide breakdown, punch-through, hot carrier effect, and junction breakdown [28], most of which stem from large signal swings between the ports of a transistor. The gate-oxide breakdown, especially in between the drain and gate terminals of the MOSFET device, is causing a catastrophic reliability problem. As CMOS technology scales down, the gate-oxide breakdown voltage of the technology decreases. However, to generate watt levels

of power, peak voltage swings can reach more than $2V_{dd}$, resulting in a breakdown of gate-oxide dielectric [29]. To prevent voltage stress in the transistor, CMOS PA designs typically employ cascode topology and a thick oxide transistor. Even with a cascode topology, the voltage swings between the drain and the gate of the common-gate (CG) device might be a bottleneck for reliability problem of CMOS PA because of large output drain signal swing, as shown in Figure 3.4. The hot-carrier injection means carriers are injected from the conducting channel in the silicon substrate to the gate dielectric destructing the transistor. It can increase the threshold voltage of the device [30]. Junction breakdown occurs when the reverse bias exceeds the limits of the p-n junction. These reliability problems limit the allowable voltage swing of devices, and it results in the constrictions to design of CMOS PA.
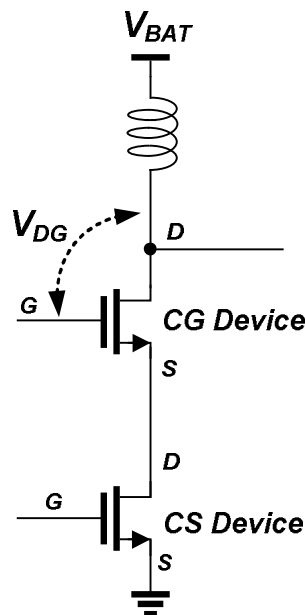
Figure 3.4. Reliability problem in the cascode CMOS PA.

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3.5 Linearity and transconductance of CMOS technology

In addition to efficiency, linearity of active devices is an important factor. The inherent large parasitic elements of the CMOS process are one of the main drivers of the nonlinearity of PA operations. The intrinsic capacitances exists between the ports of transistors, the capacitance between the gate and the source, C_{gs}, and drain junction capacitance, C_{jd}, of the transistors are bias-dependent and therefore are nonlinear parameters. Specifically, C_{gs} is able to originate the amplitude-to-phase distortion as well as the third order inter-modulation distortion, leading to the linearity degradation of the PA, and under the g_m and g_{ds} optimized linear PA operation, the distortion generated by C_{gs} can determine the overall linearity of the PA.

Moreover, the transconductance, g_m, is lower compared to III-V compound technologies. Thus, it demands large transistor size to achieve sufficiently large power, resulting in the increase of parasitic capacitances. Otherwise, additional cascaded-stages are required to achieve sufficient gain such that it demands the loss of the PA from passive components and matching networks between the stages.

CHAPTER 4

A NOVEL FEEDBACK BIAS TECHNIQUE FOR CMOS POWER AMPLIFIERS IN THE MULTI-STAGE CASCODE TOPOLOGY

4.1 Introduction

The strong demand for better wireless communication systems has accelerated the evolution toward more advanced standards for wireless communication systems. Corresponding trends in technology have moved toward higher integration of RF blocks into one single-chip and size reduction with fewer surface mounted device (SMD) count for low cost. An excellent candidate capable of satisfying this requirement is CMOS technology, with its inherent characteristics of high integration potential and continuously declining cost. Therefore, considerable effort has been devoted to implement PAs in CMOS technology, which has led to the introduction of PAs for Bluetooth, WLAN, and GSM/GPRS applications, penetrating the market of III-V compound PA [31]-[34].

However, compared to the PA design of III-V compound technology, the CMOS PA has faced several challenges such as low breakdown voltage, low transconductance, poor linearity, inaccurate RF model and low substrate resistivity. More specifically, CMOS technology seriously suffers from problems with reliability such as gate-oxide breakdown by large signal swings and the hot carrier effect, which can increase the threshold voltage. Reliability problems have been alleviated by employing cascode topology and thick oxide transistors, although they cannot entirely solve the problems. In addition, because

of the low transconductance of CMOS technology, CMOS PAs are required to have a cascaded-stage structure that allows them to achieve sufficiently high gain. Therefore, the multi-stage cascode topology has become one of the most common configurations in CMOS PA. However, the RF PAs based cascode topology can bring additional challenges in terms of linearity, reliability for the common-gate (CG) transistor in cascode topology. Extra nonlinearities from the CG transistor can degrade overall linearity performance of the PA, and the voltage stress between the drain and gate of CG transistor can be a bottleneck for the reliability of the cascode PA.

In this chapter, the cascode feedback bias technique, utilizing the leakage signals that fall on the gate of CG transistor in CMOS technology for negative feedback, is proposed to improve linearity and the reliability issues of the CMOS PA. This technique is also easily applicable to multi-stage cascode topology, which is the most common topology in CMOS PA design, without demanding additional components or space.

4.2   Cascode topology and design issues of CG transistor

This section focused on the PA design issues of the CG transistor in cascode topology. A conventional cascode topology, a stacked common-gate transistor to a common-source transistor, is shown in Figure 4.1. The gate node of CG transistor has a constant dc biasing with an ac ground, and bypass capacitor is required to establish the ac ground of the gate of the CG transistor.
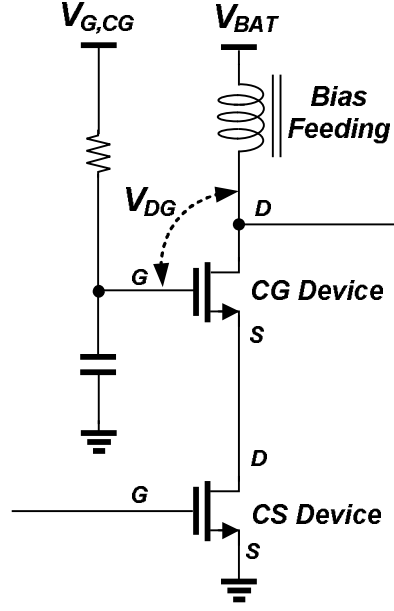
Figure 4.1. **Conventional cascode PA.**

In the cascode topology-based PA, CG devices experience fluctuation of operating regions as the input power increases in the conventional cascode configuration. Shown in Figure 4.2 (a) is the voltage waveform of the CG device between the gate and the source nodes with the increasing output power. The figure shows that V_{gs} starts to fall below the threshold voltage, V_{TH}, causing the CG device to operate in the cutoff region. Further, the large swing at the drain node can also drive the CG device from saturation to the triode region during the turn-on operation. Figure 4.2 (b) shows the voltage swing between the drain and the gate nodes of the CG device; for 25 dBm of output power, V_{DG} falls below $-V_{TH}$ and drives the CG device into the triode region. The operations of the cutoff and triode region are represented as shown in equations (4.1) and (4.2).

$$V_{GS} - V_{TH} < 0 : \text{cutoff region} \tag{4.1}$$

$$V_{DS} \le V_{GS} - V_{TH} : \text{triode region during turn-on operation} \tag{4.2}$$
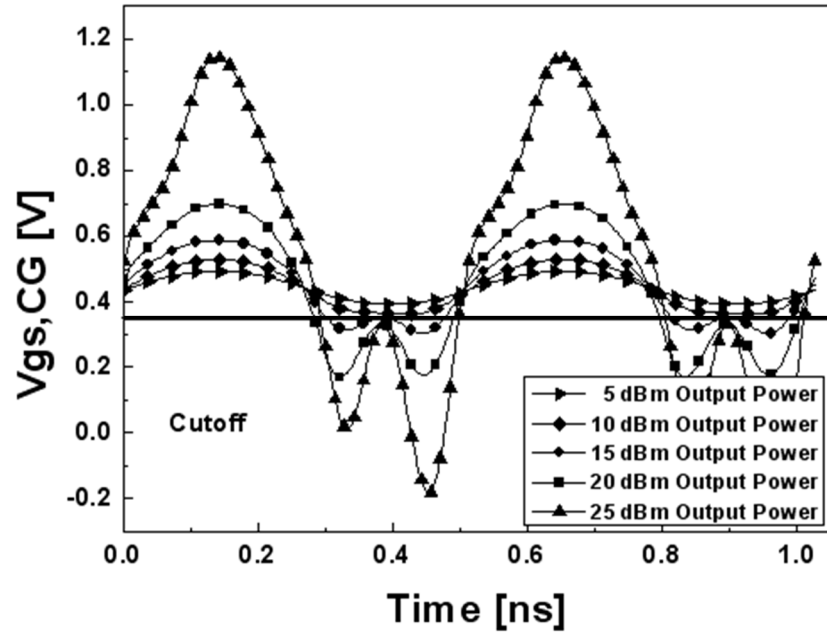
(a)
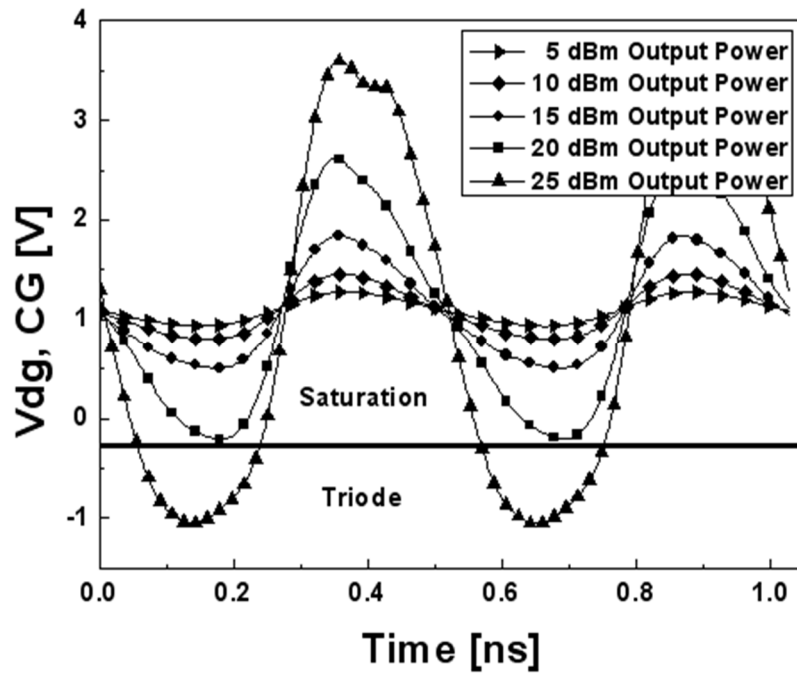
(b)

Figure 4.2. Voltage waveforms of the CG device in cascode topology. (a) Voltage difference between the gate and the source. (b) Voltage difference between the drain and the gate.

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Because of the large drain voltage swing of the CG transistor, the operation region of the transistor continuously changes, causing fluctuations of the intrinsic capacitances of the CG transistor, thereby, it generates the nonlinearity that effecting to the overall linearity performance of the PA.

In addition, the voltage stress of a CG transistor limits the reliability of the cascode PA. As shown in Figure 4.1, the voltage swing on the gate-drain of the CG transistor is larger than that of the CS transistor under large signal operation [30], causing a bottleneck that leads to a gate-oxide breakdown or hot carrier degradation from the CG transistor of the cascode topology. Employing a thick-oxide transistor for the CG transistor alleviates reliability problems. However, it leads to the gain reduction and degradation of RF performance of the PA because of the high knee voltage of the thick-oxide transistor compared to the standard transistor.

4.3   Cascode feedback bias technique

To solve the linearity and reliability problems of cascode topology, the cascode feedback bias technique is proposed, and it realized the negative feedback for cascode topology PAs in a novel method.

4.3.1   The negative feedback and distortion suppression

Negative feedback linearization is a well known linearization technique in analog and RF areas, and it suppresses the distortion by a factor of loop gain. The conventional negative feedback and distortion suppressions are derived. Figure 4.3 shows the simple

negative feedback system. It consists of open loop gain, $\alpha_o(s)$, and feedback factor, β. The feedback error, X_F, is defined as the equation (4.3)

$$X_F = X(t) - \beta Y(t) \qquad (4.3)$$

where $X(t)$ is input of the system, and $Y(t)$ is output of the system.
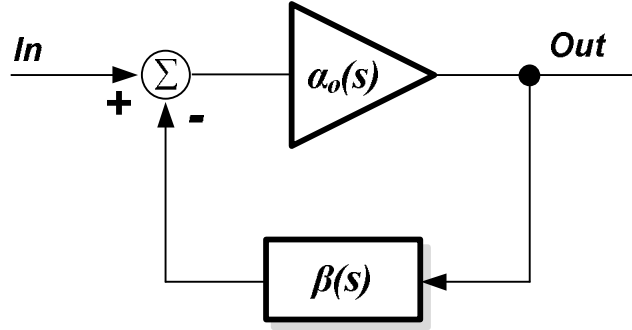
Figure 4.3. Negative feedback system.

With the assumptions that the input of the system is $X(t) = V_m cos(\omega t)$ and the approximated output of the system is $a\ cos(\omega t) + b\ cos(2\omega t) + c\ cos(3\omega t)$, the feedback error of the negative feedback system is presented in the equation (4.4).

$$X_F = (V_m - \beta a)\cos \omega t - \beta b \cos 2\omega t - \beta c \cos 3\omega t \qquad (4.4)$$

Then, the output of the negative feedback system can be derived in the equations (4.5), (4.6), and (4.7). The output is expanded up to the third order term, and the higher terms are neglected.

$$Y_F = \alpha_1(X_F) + \alpha_2(X_F)^2 + \alpha_3(X_F)^3 \qquad (4.5)$$

$$Y_F = \alpha_1[(V_m - \beta a)\cos \omega t - \beta b \cos 2\omega t - \beta c \cos 3\omega t] + \alpha_2[(V_m - \beta a)\cos \omega t - \beta b \cos 2\omega t - \beta c \cos 3\omega t]^2$$
$$+ \alpha_3[(V_m - \beta a)\cos \omega t - \beta b \cos 2\omega t - \beta c \cos 3\omega t]^3 \qquad (4.6)$$

$$Y_F = \alpha_1(V_m - \beta a)\cos \omega t - \alpha_1 \beta b \cos 2\omega t - \alpha_1 \beta c \cos 3\omega t + \alpha_2(V_m - \beta a)^2 \cos^2 \omega t$$
$$- 2\alpha_2 \beta b(V_m - \beta a)\cos \omega t \cdot \cos 2\omega t + \alpha_3(V_m - \beta a)^3 \cos^3 \omega t + \cdots \qquad (4.7)$$

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Among the output expansion of coefficients, the fundamental coefficient is summarized in the equation (4.8). Considering the quantity of the coefficients, α_2, α_3, β, b and c are assumed small enough. Under the condition, the fundamental coefficient, a, of negative feedback system can be derived as the equations (4.9), (4.10), and (4.11).

$$\cos\omega t(\alpha_1(V_m - \beta a) - \beta b \alpha_2(V_m - \beta a) - \alpha_2\alpha_3\beta c(V_m - \beta a)^2) \tag{4.8}$$

$$\cos\omega t(\alpha_1(V_m - \beta a)) \tag{4.9}$$

$$\alpha_1(V_m - \beta a) = a \tag{4.10}$$

$$a = \frac{\alpha_1}{(1+\alpha_1\beta)}V_m \tag{4.11}$$

As the equation (4.11) shows, the fundamental term is suppressed by $(1+\alpha_1\beta)$, resulting in the gain reduction. Likewise, the second coefficient, b, and the third coefficient, c, of the negative feedback system are presented in the equations (4.12), (4.13), (4.14), and (4.15), (4.16), (4.17), respectively.

$$\cos 2\omega t(\frac{\alpha_2(V_m - \beta a)^2}{2} - \alpha_1\beta b) \tag{4.12}$$

$$b(1+\alpha_1\beta) = \frac{\alpha_2(V_m - \beta a)^2}{2} = \frac{\alpha_2}{2}(\frac{a}{\alpha_1})^2 = \frac{\alpha_2}{2}\frac{V_m^2}{(1+\alpha_1\beta)^2} \tag{4.13}$$

$$b = \frac{\alpha_2}{2}\frac{V_m^2}{(1+\alpha_1\beta)^3} \tag{4.14}$$

$$\cos 3\omega t(\frac{\alpha_3(V_m - \beta a)^3}{4} - \alpha_1\beta c - \frac{\beta V_m^2\alpha_1^2(V_m - \beta a)^4}{2}) \tag{4.15}$$

$$c(1+\alpha_1\beta) = \frac{\alpha_3(V_m - \beta a)^3}{4} - \frac{\beta V_m^2\alpha_1^2(V_m - \beta a)^4}{2} = \frac{V_m^3\alpha_3(1+\alpha_1\beta) - 2\beta\alpha_1^2 V_m^6}{4(1+\alpha_1\beta)^4}$$

$$\tag{4.16}$$

$$c = \frac{V_m{}^3\alpha_3(1+\alpha_1\beta) - 2\beta\alpha_1{}^2 V_m{}^6}{4(1+\alpha_1\beta)^5} \tag{4.17}$$

The equation (4.14) and (4.17) show the coefficients of the second order term, b, and the third order term, c, and they are suppressed by $(1+\alpha_1\beta)^3$, and $(1+\alpha_1\beta)^5$, respectively, by employing negative feedback. The relative magnitude ratio of the fundamental term to the second order term is shown as the equation (4.18), and the second order term is relatively suppressed by $(1+\alpha_1\beta)^2$.

$$\frac{b}{a} = \frac{\alpha_2 V_m}{2\alpha_1(1+\alpha_1\beta)^2} \tag{4.18}$$

$$\frac{c}{a} = \frac{V_m{}^3\alpha_3(1+\alpha_1\beta) - 2\beta\alpha_1{}^2 V_m{}^6}{4(1+\alpha_1\beta)^4} \tag{4.19}$$

The equation (4.19) also presents the ratio of the fundamental to the third order term and the third order term is relatively suppressed by $(1+\alpha_1\beta)^4$. That is, although the negative feedback leads to the reduction of the fundamental term, it can relatively suppress the harmonic order terms. Therefore, the negative feedback of the PAs can achieve the harmonic signals suppression, thereby improving linearity of the PAs.

4.3.2 The coupled signals by intrinsic capacitors in transistor and the negative feedback formation of cascode feedback bias technique.

In CMOS technology, because of low substrate resistivity and large parasitic elements, signals are coupled through the silicon substrate and parasitic components of the CMOS circuits. Specifically, intrinsic capacitances between the ports of the transistors are unavoidable, and they can easily couple high frequency signals to other ports. Therefore, although the gate node of the CG device in the cascode topology is

ideally AC ground, signals from both the source and the drain are coupled to the gate of the CG device through intrinsic capacitances C_{gs} and C_{dg}, so the coupled signals exist on the gate of the CG device. The cascode feedback bias technique utilizes the coupled signals to improve the linearity of the PA for negative feedback and to alleviate the voltage stress of the CG transistor in the cascode topology. Figure 4.4 shows a conceptual diagram of the cascode feedback bias technique employed in the two-stage cascode PA. The leakage signals on the gate of the CG device are fedback through the bias network.
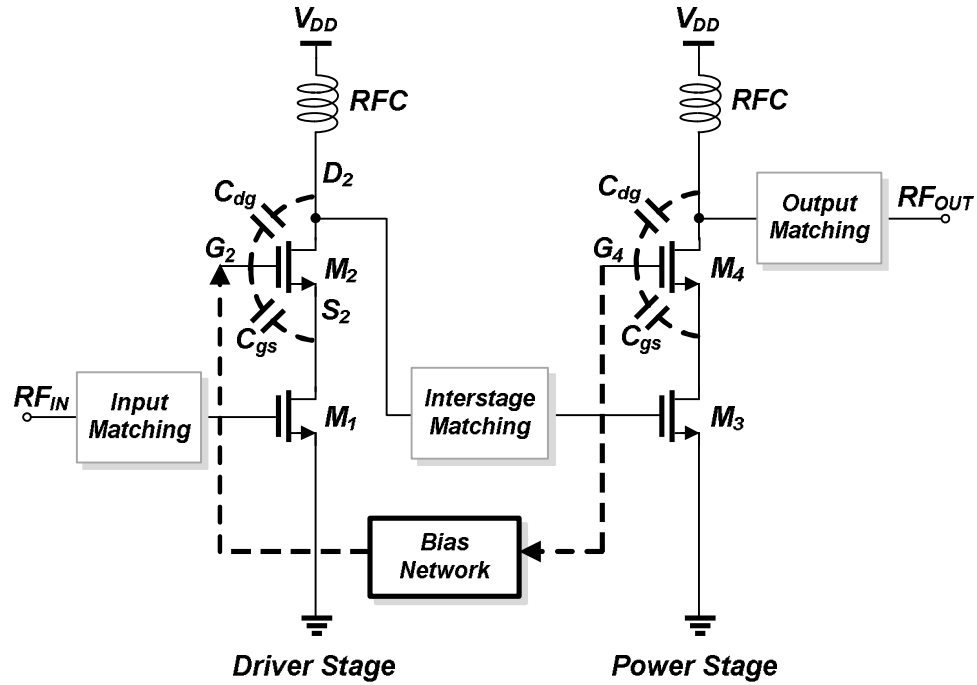
Figure 4.4. **Concept of the cascode feedback bias technique.**

Figure 4.5 (a) shows the negative feedback loop formation by the fundamental signal. The bias network is utilized to feedback the fundamental signal with 180 degree phase shift. First, the open loop gain of the PA is presented as the equation (4.20).

$$A_{open} = A_{DR} \cdot A_{PW} \cdot |\alpha_3| \qquad (4.20)$$
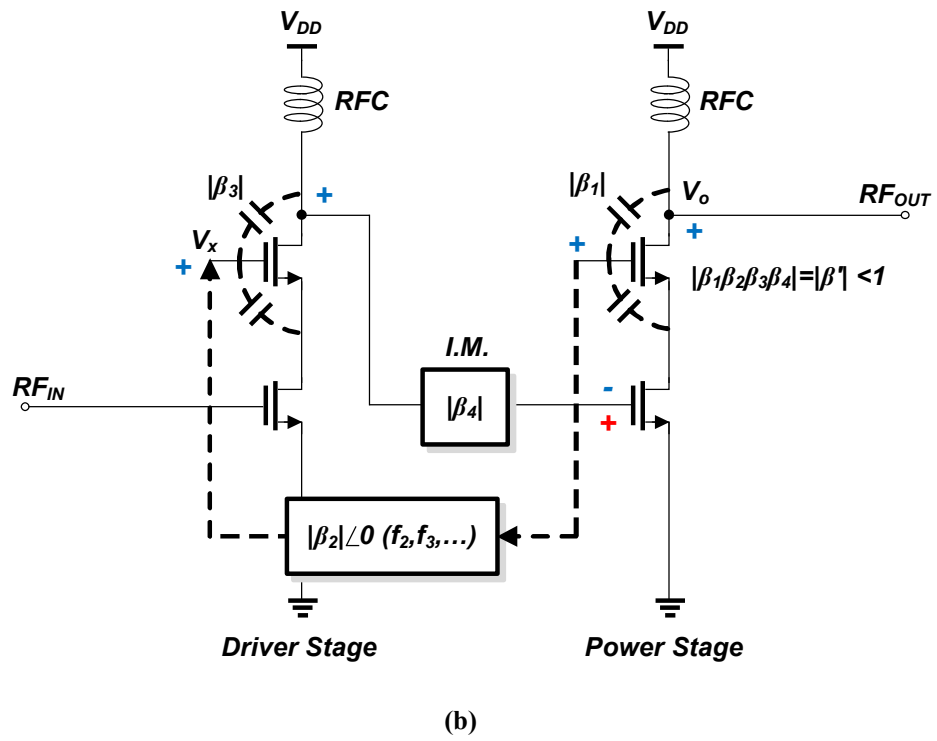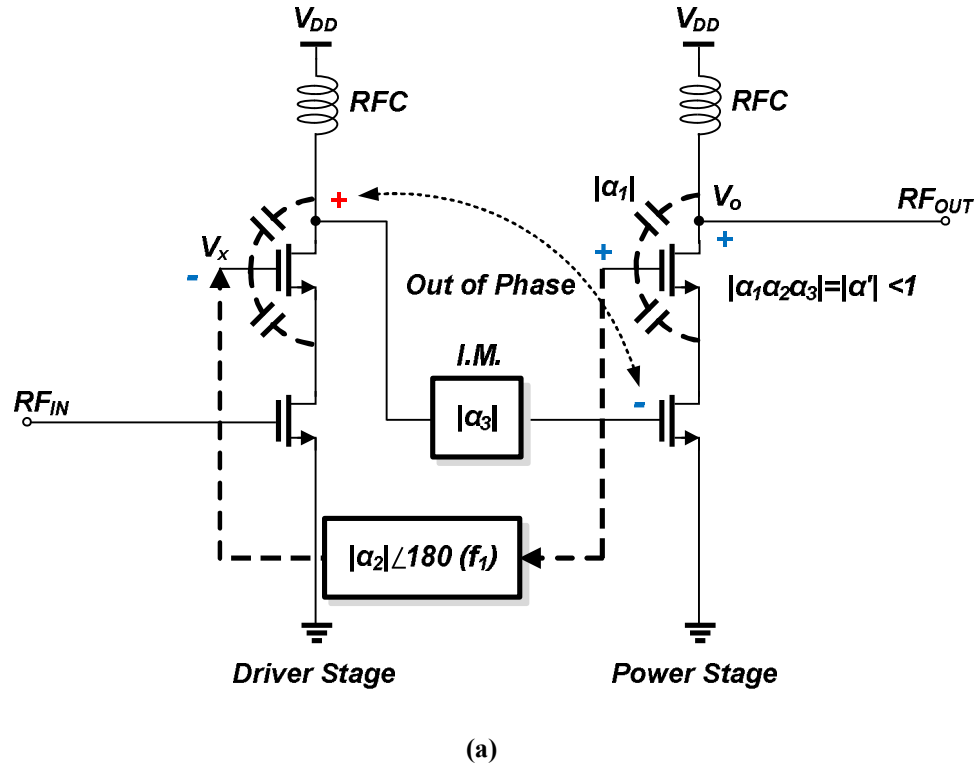
Figure 4.5. (a) Negative feedback loop formation by the fundamental signal. (b) negative feedback loop formation by the harmonic signals.

where A_{DR} is the gain of driver stage and A_{PW} is the gain of power stage, and α_3 is the insertion loss of interstage matching network for the fundamental signal.

The loop gain for the fundamental signal, LG_1, is derived as

$$LG_1 = |\alpha_1| \cdot |\alpha_2| \cdot |\alpha_3| \cdot A_{PW} \cdot \frac{g_{m2}}{1+g_{m2}Z_{S1}} \cdot (g_{m2}Z_{S1}Z_{S2} // Z_L) = |\alpha'| \cdot A_{PW} \cdot \chi \quad (4.21)$$

where Z_L is the impedance of the drain of CG transistor, Z_{S1} is impedance of looking into the drain of CS transistor and g_{m2} is the transconductance of CG transistor. The ratio that falls on the gate of CG device from the output is assumed as α_1, and the network loss of the bias network is assumed as α_2. The overall loss of negative feedback of the fundamental signal is assigned to α'. The network losses are calculated by the equation (4.22), and they are summarized in the Table 3.

$$NL = \frac{|S_{21}|^2}{(1-|S_{11}|^2)} \quad (4.22)$$

TABLE 3. NETWORK LOSS AND RELATIVE MAGNITUDE RATIO

	Feedback Network	Interstage Matching	Driver stage	Power stage
Fundamental frequency	α_2 =-0.490 dB	α_3 =-0.581 dB	-	α_1 =0.144
Second harmonic frequency	β_2 =-0.126 dB	β_4 =-0.190 dB	β_3 =0.078	β_1 =0.206

From the results, the overall-loss for the fundamental signal, α', is 0.1124 and the value of χ is 0.4145 with 0.00829 A/V of the transconductance with the CG device of the source degeneration. Because the power stage gain is 11 dB, the loop gain for the fundamental signal is 0.587. Therefore, the gain of fundamental signal is reduced by 1.587.

$$A_{F,f_0} = \frac{A_{open}}{(1+LG_1)} \qquad (4.23)$$

However, the second and the third harmonic signals are relatively suppressed by $(1+LG_1)^2$, and $(1+LG_1)^4$, respectively, as derived in the section 4.3.1, and they are shown in the equations (4.24) and (4.25). By the fundamental feedback loop, the second and the third harmonic are suppressed by 2.51 and 6.34, respectively.

$$\frac{A_{F,2f_0}}{A_{F,f_0}} = \frac{A_{open,2f_0}}{(1+LG_1)^2} \qquad (4.24)$$

$$\frac{A_{F,3f_0}}{A_{F,f_0}} = \frac{A_{open,3f_0}}{(1+LG_1)^3} \qquad (4.25)$$

Figure 4.5 (b) shows the negative feedback loop formation by the harmonic signals. Since the impedance of $Z_{intrinsic,1}$ and $Z_{intrinsic,2}$ decreases as the frequency increases, the harmonic signals can easily fall on the gate node of the CG devices. Moreover, because the bias network and the interstage matching network are formed by a high-pass filter type, harmonics are easily passing the networks, so that they form a negative feedback loop, thereby suppressing the harmonic effects of the entire PA system. The equation (4.26) shows the loop gain by the second harmonic signal. The overall loss of the second harmonic signal, β', is 0.0149 and the loop gain of the second harmonic signal, LG_2, is 0.1878 with 11 dB of the power stage gain. Therefore, with the negative feedback loop of harmonic signals, the second harmonic signal can additionally be suppress by 1.1878.

$$LG_2 = |\beta_1| \cdot |\beta_2| \cdot |\beta_3| \cdot |\beta_4| \cdot A_{PW} = |\beta'| \cdot A_{PW} \qquad (4.26)$$

$$A_{F,2f_0} = \frac{A_{open,2f_0}}{(1+LG_2)} \qquad (4.27)$$

The cascode feedback bias technique demonstrated the negative feedback loops for both the fundamental and the harmonic signals, and the negative feedback effects result in the harmonic suppressions, thereby leading to the linearity improvement of the PA.

4.3.3 The feedback bias network

The feedback bias network, consisting of an inductor and two capacitors in a T-configuration, is shown in Figure 4.6. Its original function was to achieve AC ground of both the driver and the gate of the power stage of the CG device in the cascode topology, and it also has the function of the feedback factor, β.

For a detailed analysis of the bias network function, the impedances of each node and the operations of the fundamental and harmonic signals in the bias network are discussed. The gates of the CG devices in the driver and power stages are labeled X and Y, respectively, and the node between the driver and power stages of the CG devices is labeled W. For the simple derivation, the additional parasitic capacitances that connected to the intrinsic capacitance are neglected. The impedance of the intrinsic capacitances of CG transistor in the driver stage and the power stage are shown in equations (4.28) and (4.29), respectively.
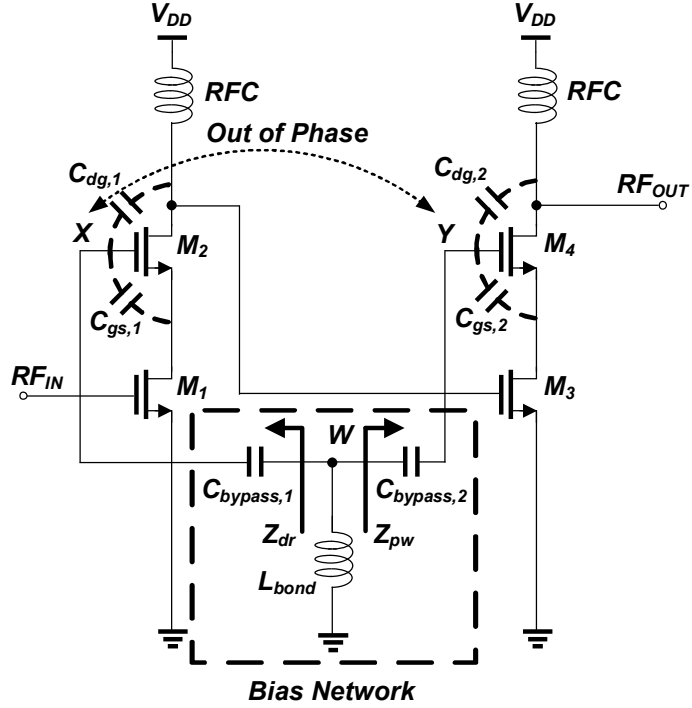
Figure 4.6. **Impedances depending on the node of the PA.**

$$Z_{Intrinsic,1} = \frac{1}{SC_{dg1} + SC_{gs1}} \tag{4.28}$$

$$Z_{Intrinsic,2} = \frac{1}{SC_{dg2} + SC_{gs2}} \tag{4.29}$$

where C_{dg1} is the intrinsic drain-gate capacitance of the driver stage, C_{dg2} is the intrinsic drain-gate capacitance of the power stage, C_{gs1} is the intrinsic gate-source capacitance of the driver stage, and C_{dg2} is the intrinsic gate-source capacitance of the power stage. Since the impedance of $Z_{intrinsic,1}$ and $Z_{intrinsic,2}$ decreases as the operation frequency increases, the harmonic signals can easily fall on the gate node of the CG devices.

Equation (4.30) represents the impedance looking into the driver stage at node W, while equation (4.31) shows the impedance looking into the power stage at node W.

$$Z_{dr} = \frac{1}{SC_{bypass,1}} + \frac{1}{SC_{intrinsic,1}} \tag{4.30}$$

$$Z_{pw} = \frac{1}{SC_{bypass,2}} + \frac{1}{SC_{intrinsic,2}} \tag{4.31}$$

where $C_{bypass,1}$ is the bypass capacitance of the driver stage, and $C_{bypass,2}$ is the bypass capacitance of the power stage.

The drain voltage swings that fall on the gate of the CG devices can be calculated by voltage division, and the leakage signal swings on the gate node of the driver stage and the power stage are represented in the equations (4.32) and (4.33).

$$V_X = \frac{(Z_{pw} // Z_{L,BOND}) + Z_{C,Bypass1}}{(Z_{pw} // Z_{L,BOND}) + Z_{C,Bypass1} + Z_{intrinsic,1}} V_{drain,1} \tag{4.32}$$

$$V_Y = \frac{(Z_{dr} // Z_{L,BOND}) + Z_{C,Bypass2}}{(Z_{dr} // Z_{L,BOND}) + Z_{C,Bypass2} + Z_{intrinsic,2}} V_{drain,2} \tag{4.33}$$

where $Z_{L.BOND}$ is the impedance of the wire bond inductor.

Then, the signal swing of node W, which is transferred from the gate of the power stage, is calculated by equations (4.34), (4.35), and (4.36). The approximated transfer function is shown in equation (4.37). The signal swing from the gate of the driver stage can also be calculated by the same method.

$$V_W = \frac{(Z_{dr} // Z_{L,BOND})}{(Z_{dr} // Z_{L,BOND}) + Z_{C,Bypass2}} V_Y = \frac{Z_{L,BOND}}{Z_{L,BOND} + Z_{C,Bypass2} + \dfrac{Z_{L,BOND} \cdot Z_{C,Bypass2}}{Z_{dr}}} V_Y \tag{4.34}$$

$$V_W = \frac{S^2 L_{Bond} C_{bypass,2}(C_{bypass,1} + C_{intrinsic,1})}{S^2 (L_{Bond} C_{bypass,2}(C_{bypass,1} + C_{intrinsic,1}) + L_{Bond} C_{bypass,1} C_{intrinsic,1}) + (C_{bypass,1} + C_{intrinsic,1})} V_Y \tag{4.35}$$

$$V_W = \frac{-w^2 L_{Bond} C_{bypass,2}}{1 - w^2 L_{Bond} C_{bypass,2} - (\dfrac{w^2 L_{Bond} C_{intrinsic,1} C_{bypass,1}}{C_{bypass,1} + C_{intrinsic,1}})} V_Y \qquad (4.36)$$

$$V_W \simeq \frac{-w^2 L_{Bond} C_{bypass,2}}{1 - w^2 L_{Bond} C_{bypass,2}} V_Y \qquad (4.37)$$

$$V_W \simeq V_X \qquad (4.38)$$

$$f_o < \frac{1}{2\pi \cdot \sqrt{L_{Bond} C_{bypass,2}}} = 2.4 GHz < 2 f_o \qquad (4.39)$$

Equation (4.37) shows the transferred leakage signal from the power stage, and it is delivered to gate of CG device in driver stage, as shown in equation (4.38). In the feedback bias network, each $C_{bypass,1}$ and $C_{bypass,2}$ is implemented by 11 pF, and L_{BOND} is implemented approximately 0.4 nH of multiple wire-bonds. With the design parameters, resonance frequency by L_{Bond} and $C_{bypass,2}$ is determined to 2.4 GHz, as shown in equation (4.39). Therefore, the operating fundamental frequency, which is between 1.92GHz and 1.98 GHz, is lower than the resonance frequency while harmonic signals are at higher frequency than the resonance frequency. In other words, under this condition of a transfer function, the fundamental signal has a 180 degree phase-shift, while the second, the third and higher harmonics have an in-phase shift in the feedback bias network, because the ω^2 term dominates as the frequency increases and $1 - \omega^2 L_{Bond} C_{bypass,2}$ term is lower than zero. Therefore, the reversed fundamental signal and in-phase harmonics are transferred through the feedback bias network.

The derivation of feedback bias network is verified by simulations. As the Figure 4.7 (a) shows, the phase of fundamental signal at X node and W node is almost the same, while having 180 degree phase difference to Y node. Figure 4.7 (b) and (c) present the

phase of the second and the third harmonic signals, respectively. The second harmonic phase between X node and Y node becomes in-phase, and the third harmonic phase between X node and Y node is even more equivalent, because the ω^2 term dominates.

(a)

(b)

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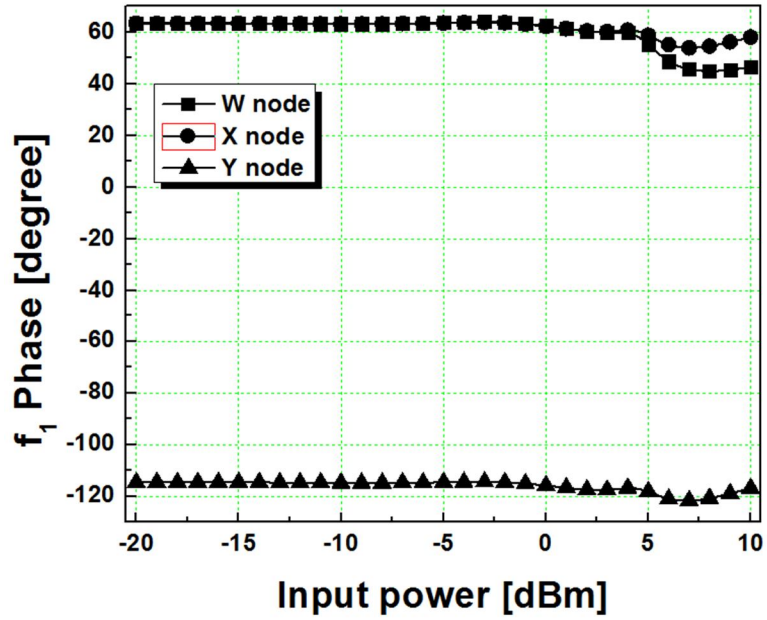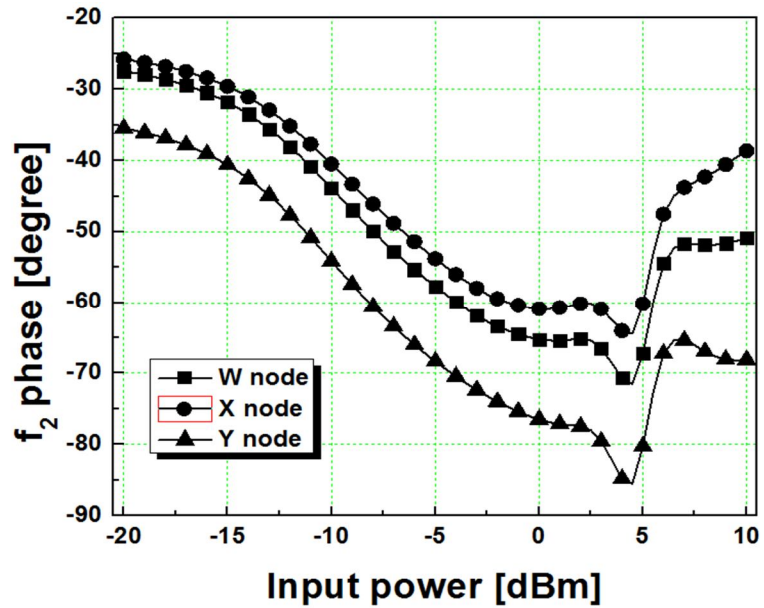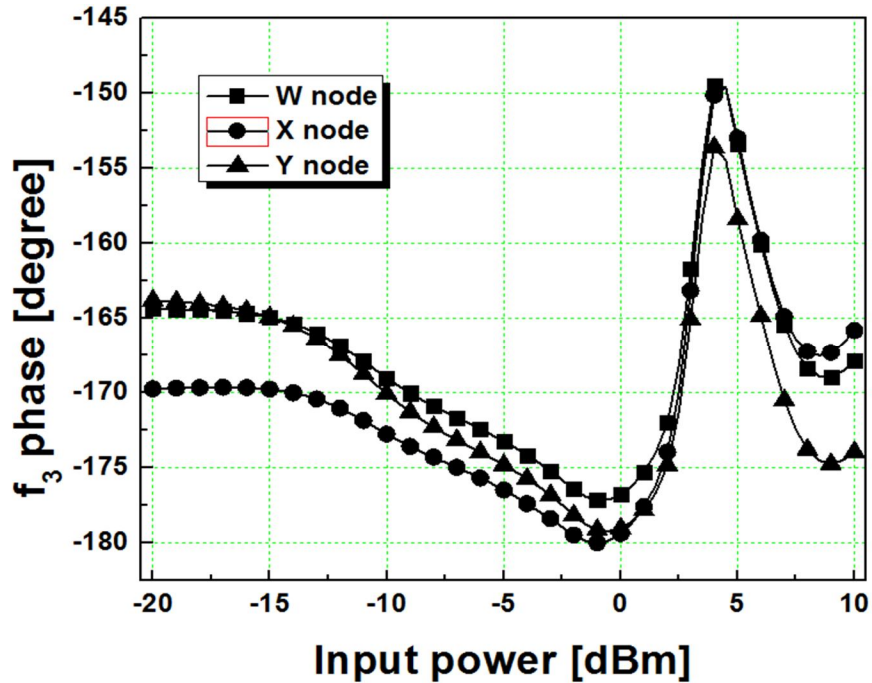
(c)

Figure 4.7. **Comparison of the signal phase depending on the nodes. (a) the fundamental signal. (b) the second harmonic signal. (c) the third harmonic signal.**

4.3.4   The effects of cascode feedback bias technique

As the section 4.3.1 presented, the negative feedback relatively suppresses the harmonic distortions by a feedback factor and it improves the linearity of the PA. Figure 4.8 (a), (b), and (c) show the magnitude comparison of the fundamental, the second and the third harmonic signals at the output of the driver stage and the power stage. By employing this technique, the harmonic signals are suppressed, especially; much of the suppression of the third harmonic is achieved at the high power region. From the simulation, this cascode feedback bias technique achieved the improvement of 6.5 dBc of IMD3 with 2 dB of gain reduction.
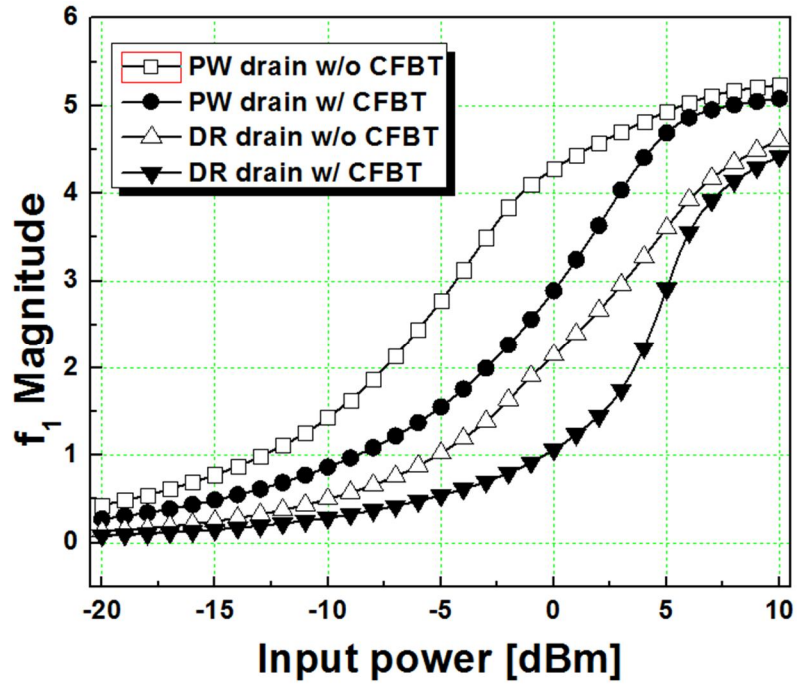
(a)
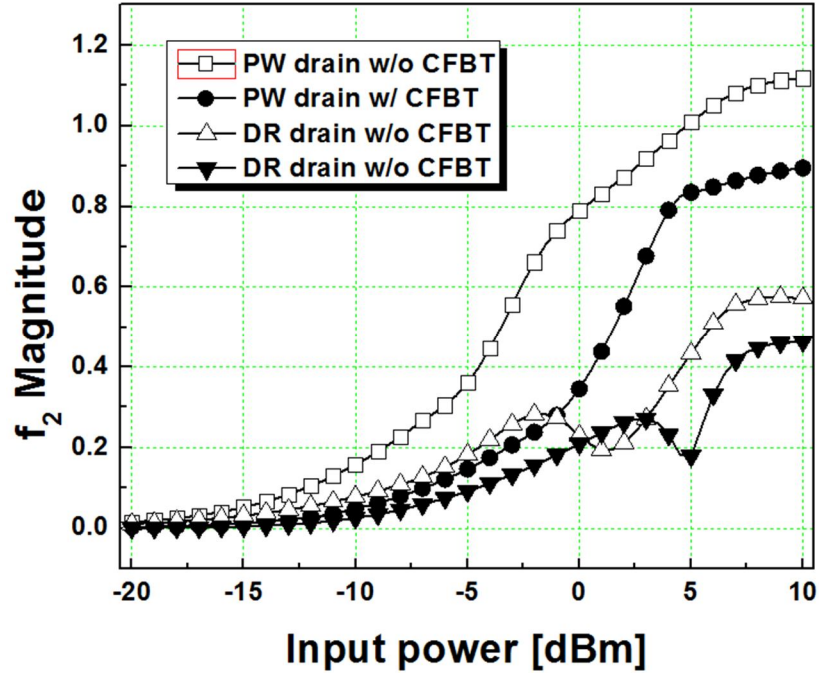
(b)
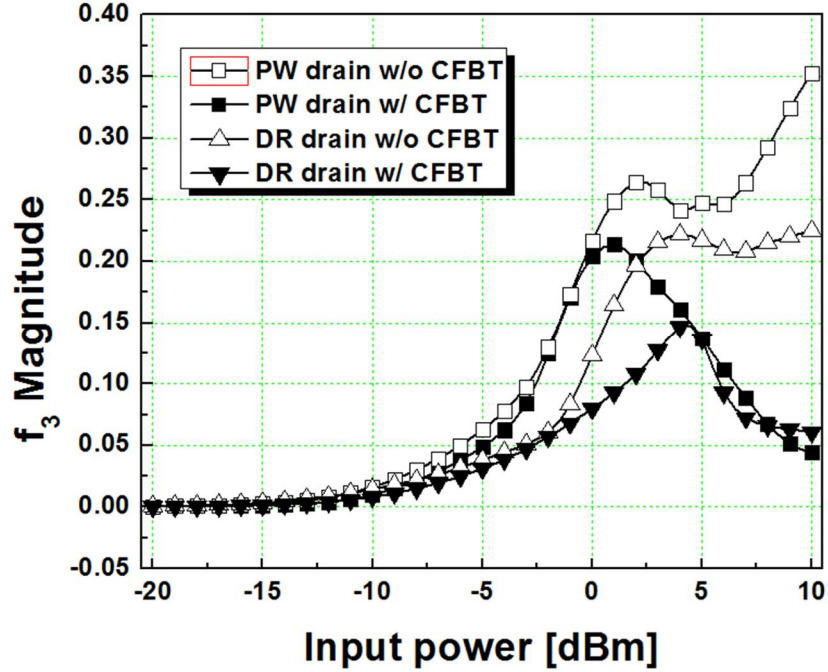
(c)

Figure 4.8. **Comparison of the signal magnitude. (a) the fundamental signal. (b) the second harmonic signal. (c) the third harmonic signal.**

Moreover, the reversed fundamental signal also provides the reduction of operation region variations and the alleviation of reliability of the cascode PA. Figure 4.9 (a) and (b) show the voltage waveform of the CG transistor at 25 dBm output power in the time domain. The operation region of the conventional cascode configuration with the fixed gate voltage of the CG device varies continuously because the large drain voltage swing reaches a lower point than the gate voltage, as shown in Figure 4.9 (a). By employing the technique, the gate node waveform of the driver stage G_1, follows the waveforms of drain node D_1, and source node S_1, with in-phase, as shown Figure 4.9 (b).

For the detail explanations, Figure 4.10 (a) and (b) present the variation of the operation region ratio of the CG device. As shown in Figure 4.10 (a), the ratio of the cutoff region has declined from 40% (1) to 20% (2) within one waveform cycle by

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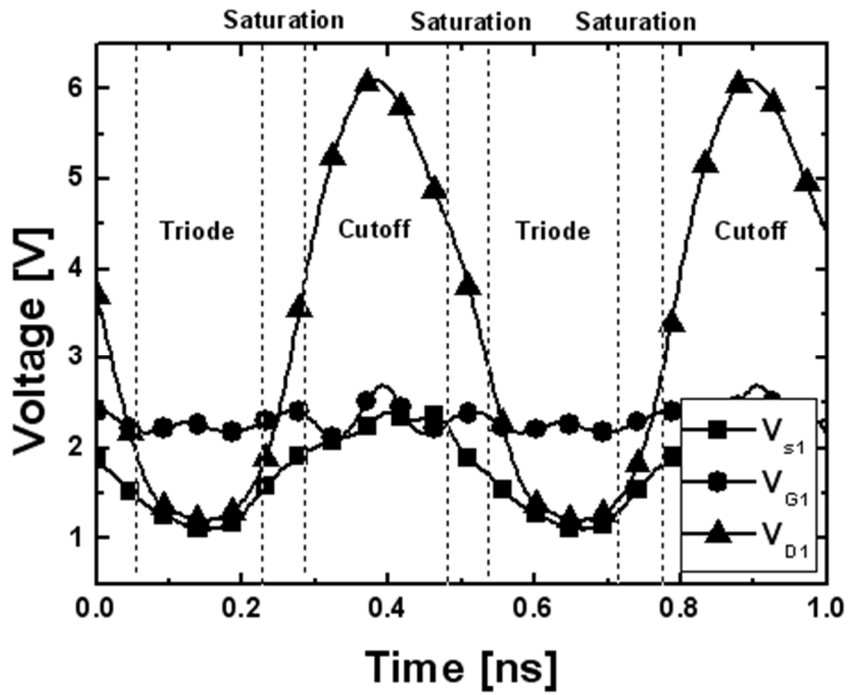
(a)
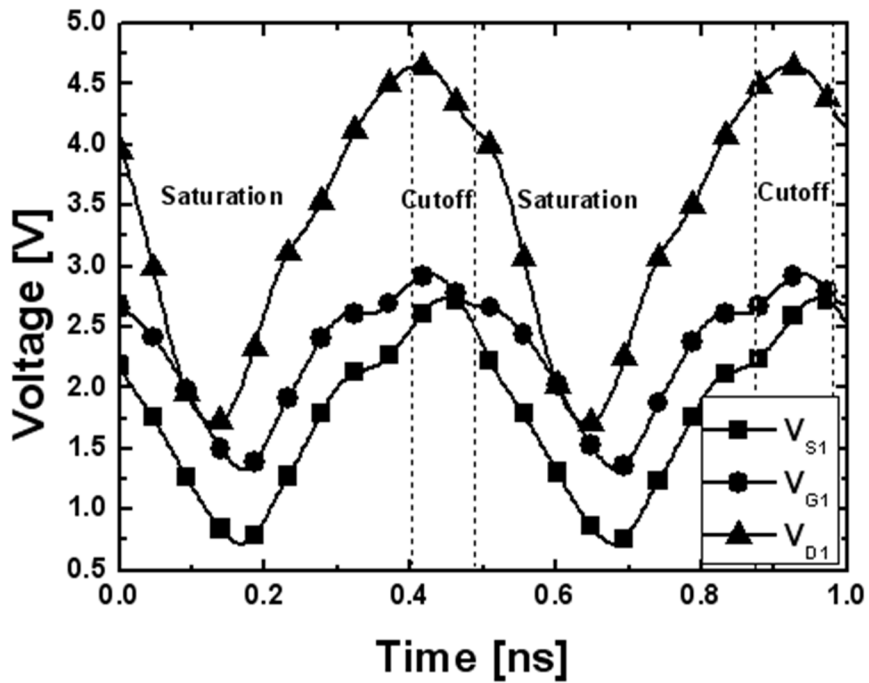
(b)

Figure 4.9. Voltage waveforms of the CG device at 25 dBm output power. (a) without the cascode feedback bias technique. (b) with the cascode feedback bias technique.

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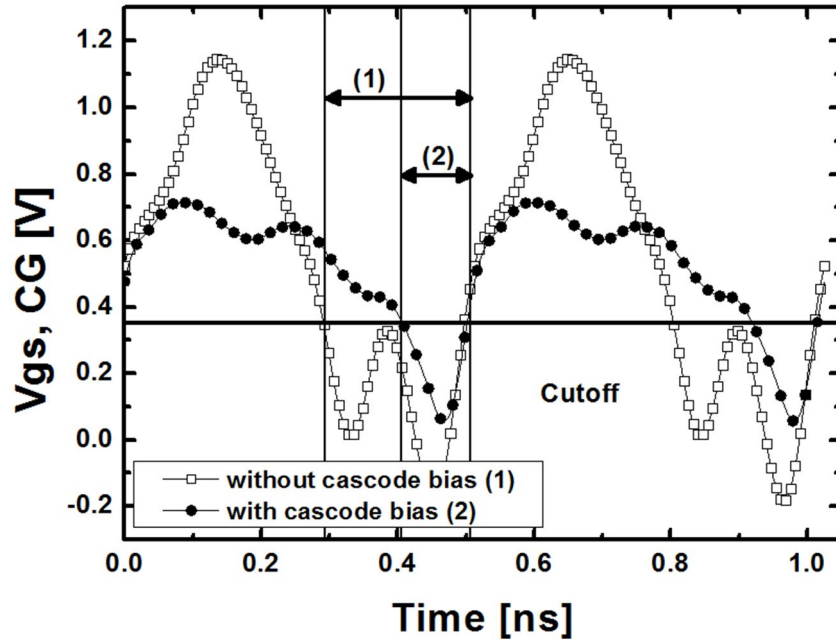
(a)
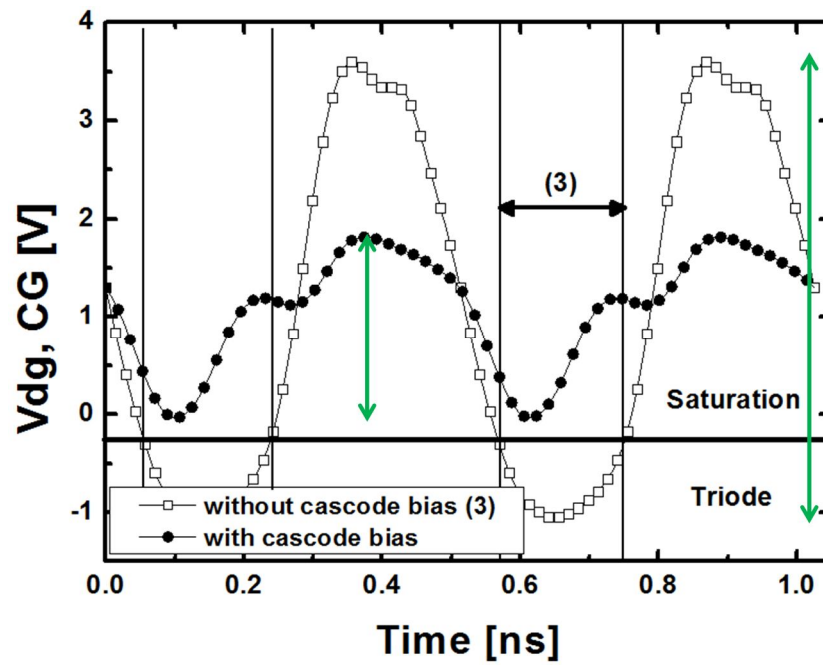
(b)

Figure 4.10. Comparison of the ratio of the operation region variations (a) turn-on vs. turn-off. (b) triode vs. saturation region during the turn-on region.

following the waveforms of D_1 and S_1. Figure 4.10 (b) represents the operation region ratio during the turn-on region of the device. The triode region without the cascode feedback bias technique is removed (3), and mostly operates in the saturation region. Variations of the operation region of transistor lead to fluctuation of transconductance g_m, output conductance g_{ds}, intrinsic capacitance of gate-source capacitance C_{gs}, and drain-gate capacitance C_{dg}, which can be several of the major sources of non-linearity.

To verify the effects of operation region variations, the phase deviation of CG transistors are simulated. Figure 4.11 (a) shows the comparison of the phase deviation of CG transistor in the driver stage. It shows the reduction of phase deviation from 30.8 degree to 9.8 degree over the output power level. Also, Figure 4.11 (b) shows the phase deviation of CG transistor in the power stage, and it presents the reduction of phase deviation from 36.3 degree to 14 degree. From the phase deviation results, amplitude-to-phase (AM-PM) is derived as shown in Figure 4.12 (a) and (b), and they verify the reductions of AM-PM distortion of CG transistors. That is, by employing this technique, the fundamental signals, which following the drain and the source signals of CG devices, reduced the fluctuation of transistor operations. They demonstrated the decrease of phase deviation, thereby, leading to the reduction of AM-PM distortion.

The reliability issue of the cascode PA is also alleviated. In the cascode PA topology, the voltage stress between the drain and the gate becomes bottleneck for the reliability of the PA. The technique reduces the voltage difference of the CG transistor from 4.5-V to 1.9-V by utilizing the gate signal to follow the source and the drain signals, as shown in Figure 4.10 (b), and it makes possible to employ a standard transistor for the

CG transistor, not a thick-oxide transistor. Using a standard transistor for CG device in cascode topology can provide better RF performance of the driver stage.

(a)

(b)
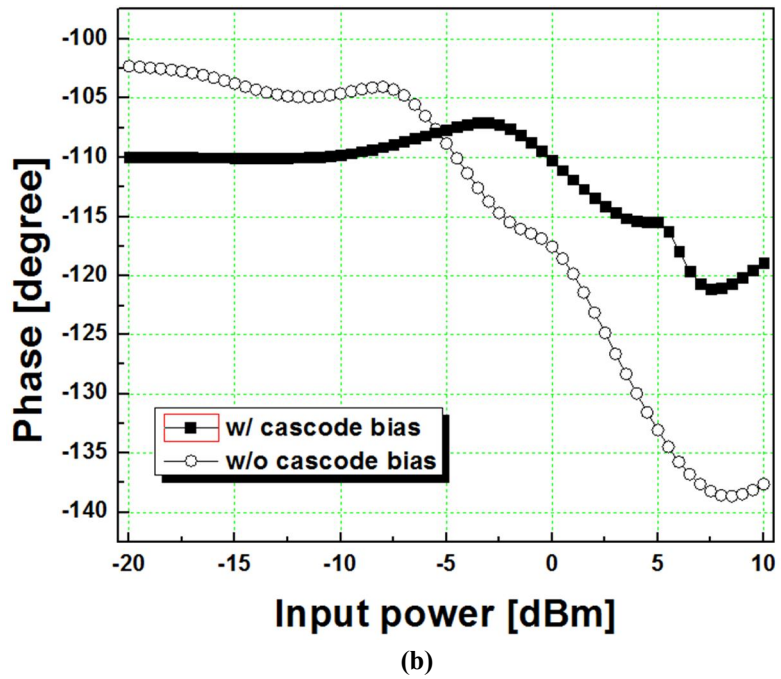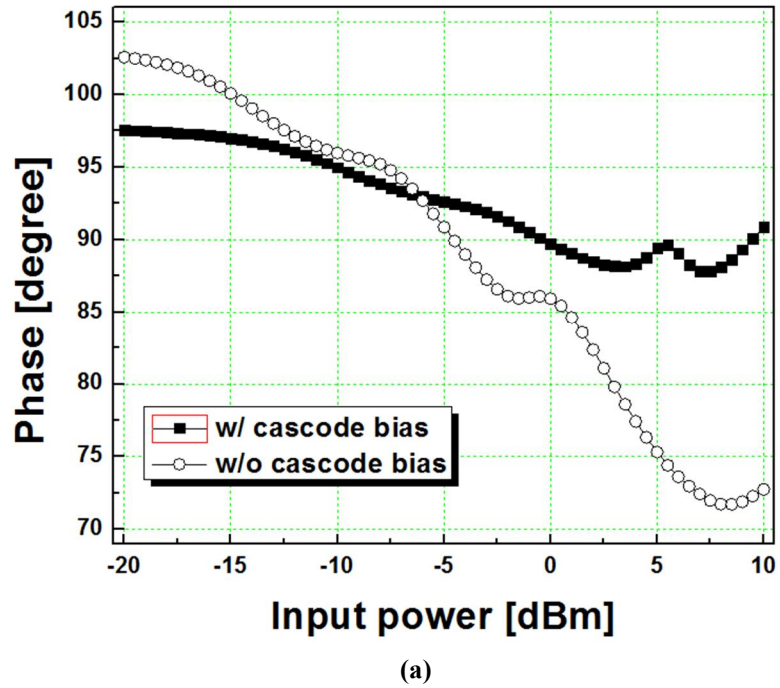
Figure 4.11. **The comparison of phase deviation of CG transistor. (a) the driver stage. (b) the power stage.**

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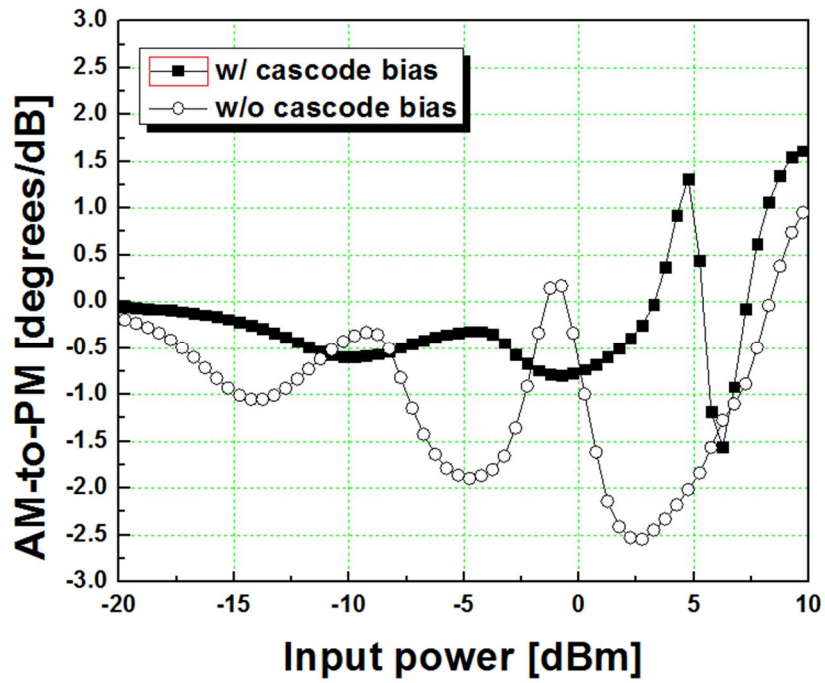
(a)
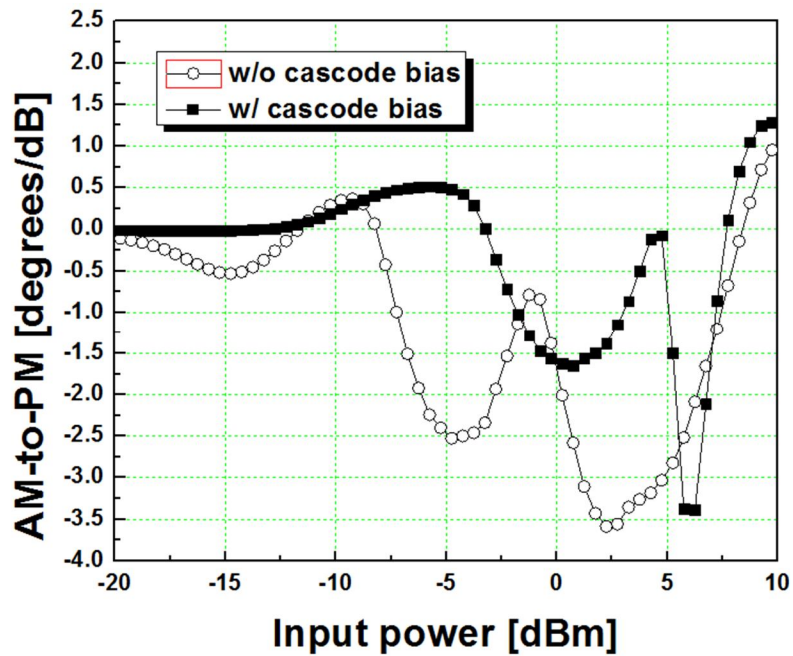
(b)

Figure 4.12. **The comparison of AM-to-PM of CG transistor (a) the driver stage. (b) the power stage.**

4.4 Design and implementation of the linear CMOS PA

Figure 4.13 is the overall schematic of the two-stage, single-ended CMOS linear PA. The PA cores are realized in single-ended configuration for avoidance of baluns and simple integration, and smaller area for cost reduction. They employ a deep N-well in both the driver and the power cells to reduce the noise and signal coupling with other components on the silicon substrate. The widths of M_2 and M_1 in the driver stage are 1.5-mm and 0.9-mm, and the widths of M_4 and M_3 in the power stage are 5.6-mm and 4.7-mm, respectively. To achieve minimal bond-wire inductor (better ac ground), multiple bonding wires to the ground are utilized to minimize source degeneration effects of both driver and power cells which typically can lead to the decrease of gain. With a supply voltage of 3.4-V, the gate bias voltage of the CS and CG device are set to 0.45-V and 2.5-V, respectively, and they are carefully adjusted to achieve the sweet spot at the desired output power near 22-dBm, resulting in lower IMD3 [35]. To ensure reliability of the devices at 3.4-V operation, a 0.4-um thick-oxide NMOS transistor is used in the power stage cascode CG transistor, and 0.18-um NMOS transistors are used for the both the CG and the CS in the driver stage to compensate for the low RF power gain of the thick-oxide CG transistor in the power stage. The interstage matching, consisting of a shunt inductor and two series capacitors in a T-network, is employed for the advantages of less inductor count, dc isolation, and tuning of shunt inductor value with bondwire inductor after the chip fabrication. To achieve compact size of the chip with optimized performances of the PA, the sensitivity of the inductors' quality factor is considered so that high quality factor of inductor is used for output matching network while smaller size

of inductors with less quality factor are used for input- and interstage-matching networks, and all of capacitors are implemented by on-chip MIM capacitor.
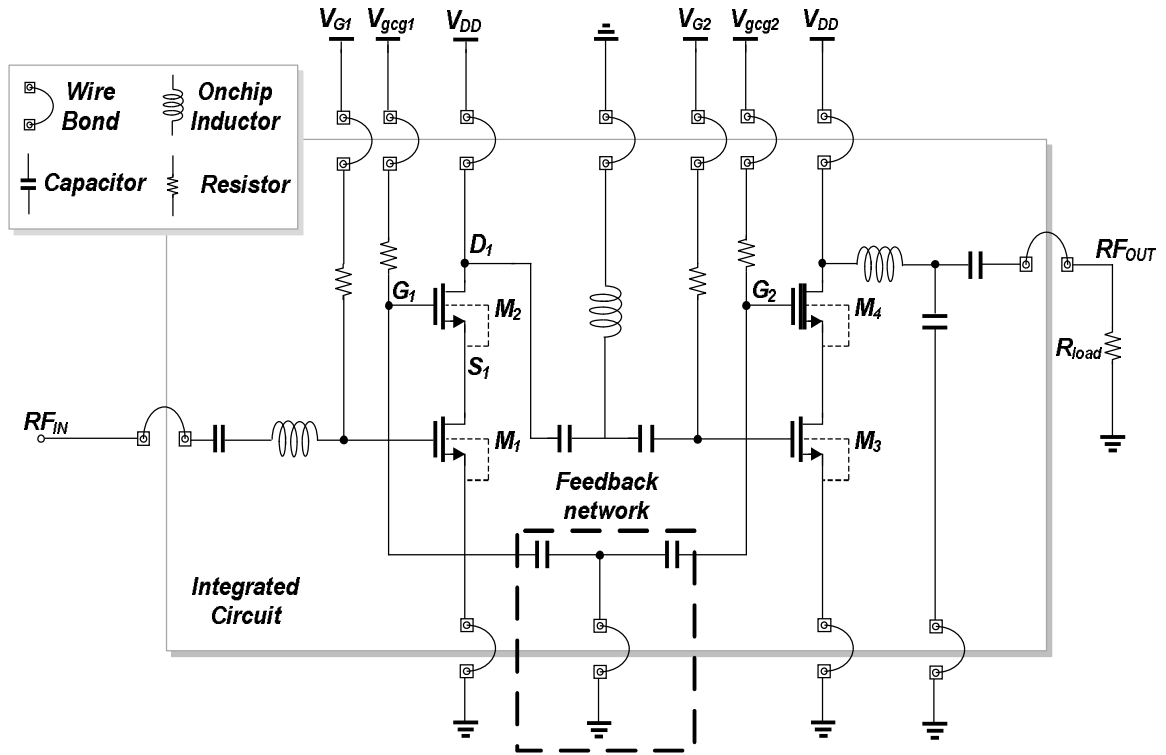
Figure 4.13. Overall schematic of the CMOS PA with the cascode feedback bias technique.

4.5   Measurement results

Figure 4.14 shows a photograph of the fabricated CMOS PA, which has a 1.60-mm × 0.52-mm chip area. All the components are fully integrated on single chip. To verify the chip, it is assembled to a 2-layer FR-4 printed circuit board (PCB) with 50-Ω input and output terminations. The PCB and cable losses are de-embedded while the wire bonding losses are included in the measurement results.
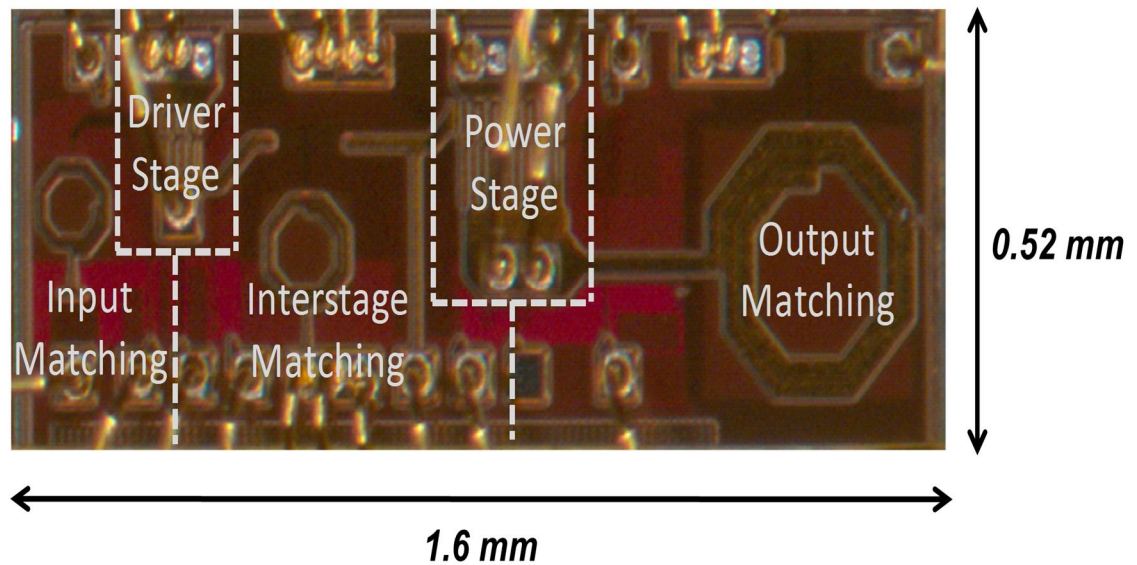
Figure 4.14. Microphotograph of the linear CMOS PA.

Small signal measurements were performed with 3.4-V supply voltage, shown in Figure 4.15 (a) and (b). The input port reflection coefficient, S11, and the output port reflection coefficient, S22, achieve less than -12-dB and -10-dB, respectively, at 1.95-GHz. The forward gain, S21, has 3-dB wide gain bandwidth from 1.5- to 2.1- GHz over a 23-gain, and the reverse gain, S12, is less than -33-dB of the bandwidth up to 5-GHz frequency.
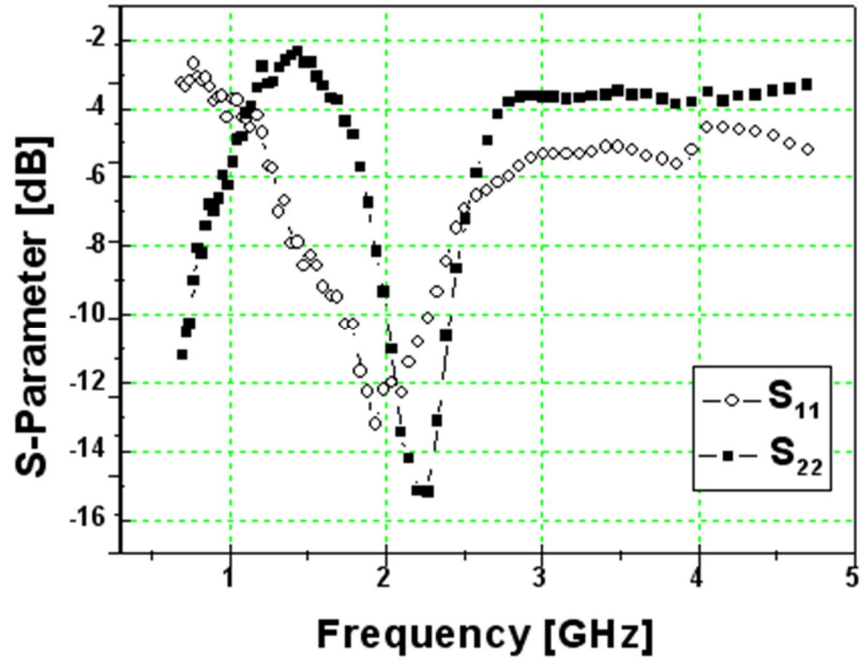
(a)
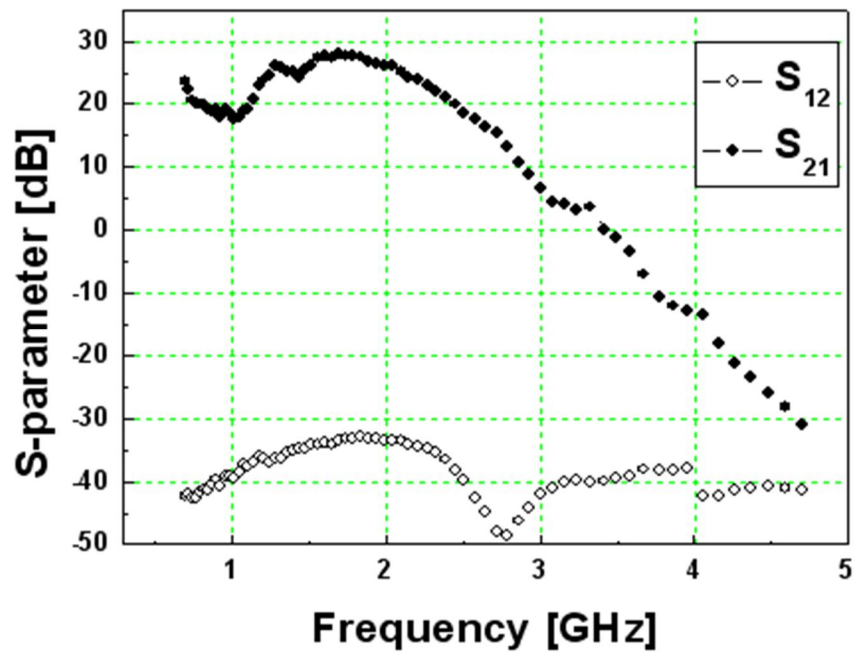
(b)

Figure 4.15. Measured small signal performances of the PA with cascode feedback bias technique. (a) S_{11} and S_{22}. (b) S_{21} and S_{12}.

Large signal measurements were performed using a 3GPP WCDMA modulated signal. Figure 4.16 (a) shows the comparison of the PAE and the gain of the two PAs, which are with the cascode bias and without the cascode bias. The graph illustrates the gain reduction from 28-dB to 26-dB, resulting from the negative feedback effect, while the PAE has a curve similar to the measurement. The PA with the cascode bias achieved 26-dBm of the maximum output power and 46.4-% of peak PAE, and the 1-dB gain compression point was 25.4-dBm. The linear output power using a 3GPP WCDMA modulated signal was 23.5-dBm with 40-% PAE and the DC current consumption of the driver and the power amplifier were 27-mA and 143-mA, respectively.

Figure 4.16 (b) shows the comparison of the measured IMD3 results. A two-tone test was performed at a center frequency of 1.95-GHz with tone-spacing of 5-MHz. The measurement results showed that the IMD3 is significantly improved near the compression output power level, and the sweet spot appeared at the desired output power of 22-dBm, resulting in lower IMD3. The measurement results compare ACLR performance with 5-MHz and 10-MHz spacing in Figure 4.17 (a) and (b), respectively. The cascode feedback bias technique improved ACLR at the desired high output power regime with a much margin of ACLR. The linear output power increased from 22.7-dBm to 23.5-dBm, thereby, enhancing efficiency from 37.2% to 40 % in the exponentially increasing PAE curve. From the measurement results of IMD3 and ACLR, we can infer that under the -25-dBc two-tone IMD3 guarantees the required linearity ACLR of -33-dBc.
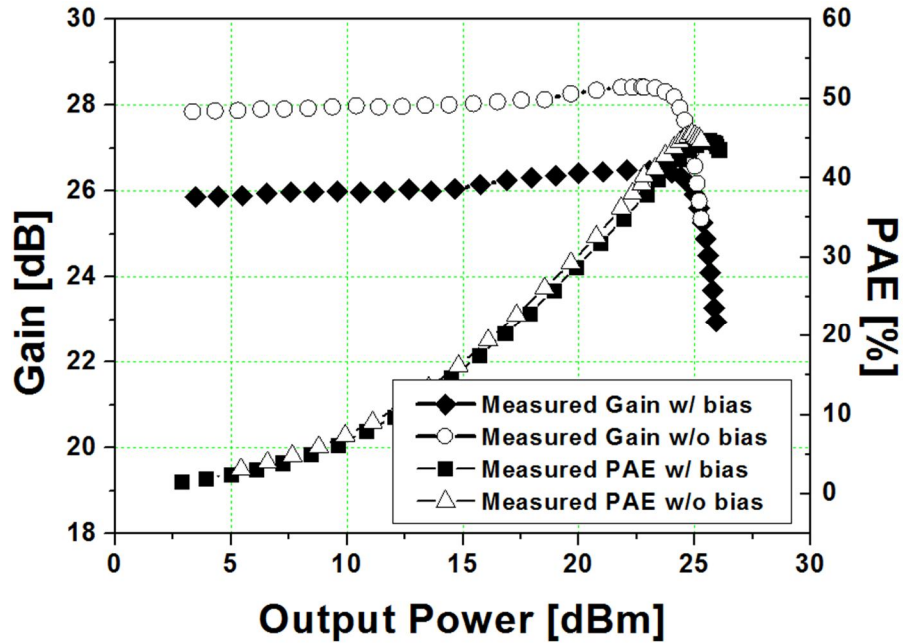
(a)
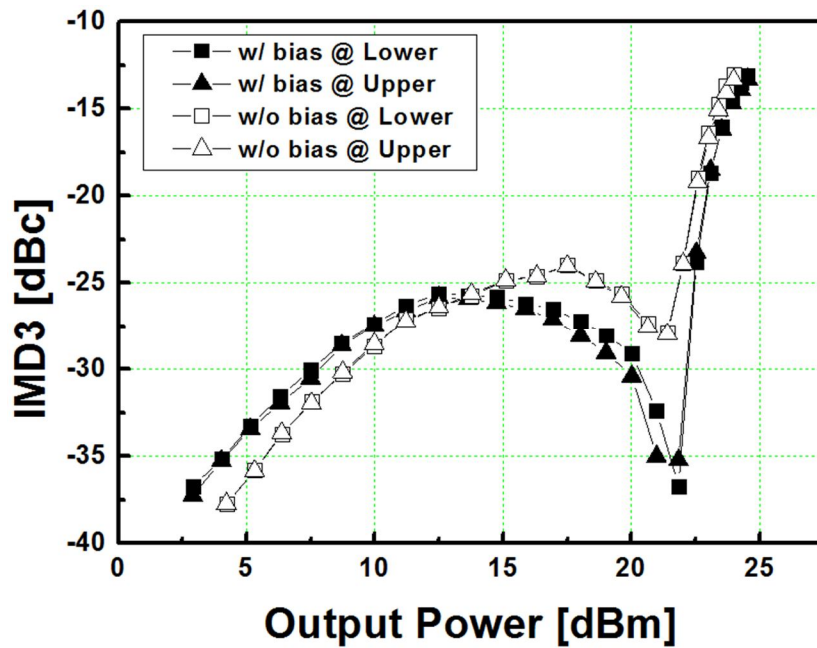
(b)

Figure 4.16. Measured PA performance. (a) Comparison of the gain and the PAE with and without the cascode feedback bias technique. (b) Comparison of IMD3 with and without the cascode feedback bias technique.
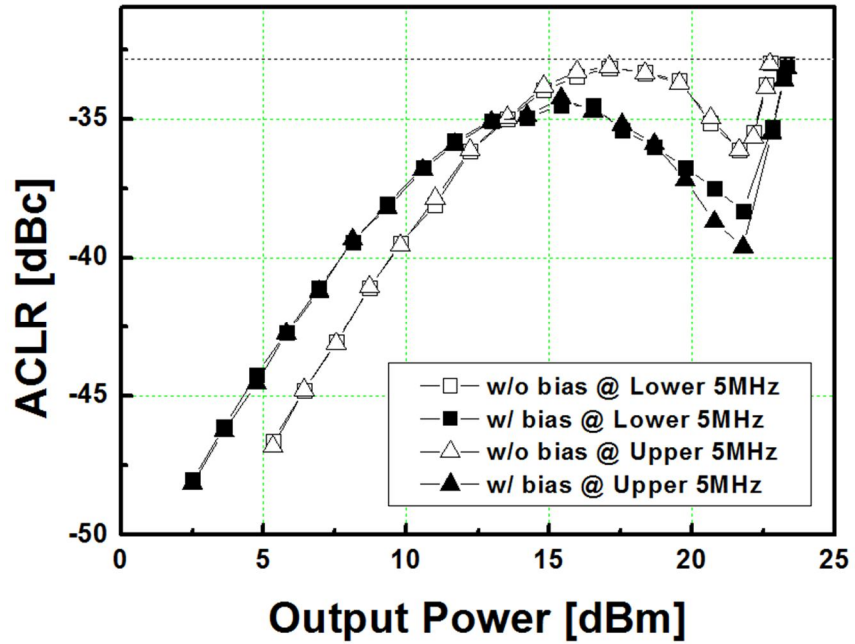
(a)
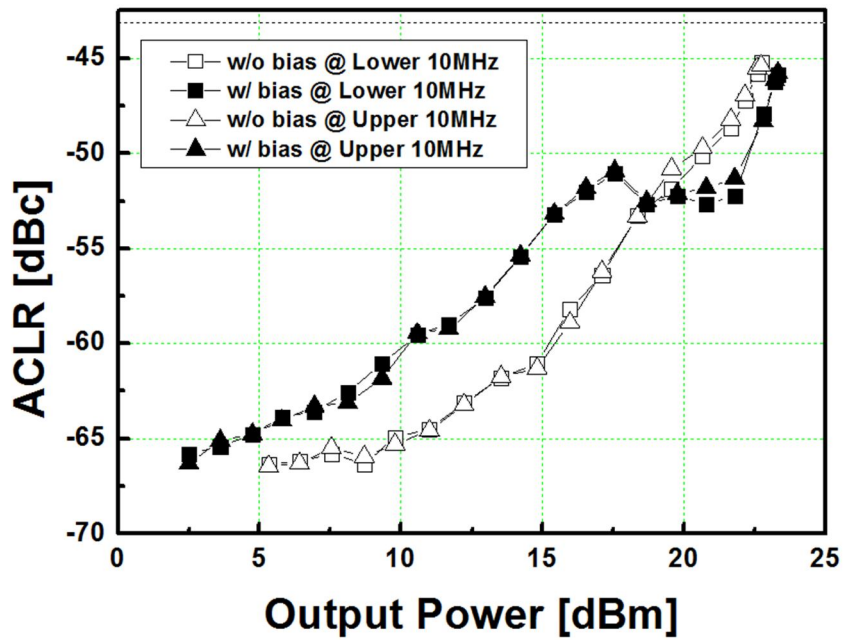
(b)

Figure 4.17. Comparison of measured ACLR. (a) 5MHz offset. (b) 10MHz offset.

In Figure 4.18, the measured WCDMA ACLR spectra with and without employment of the cascode feedback bias technique are compared. The results of the comparison demonstrated use of the technique enhanced linearity of the PA.
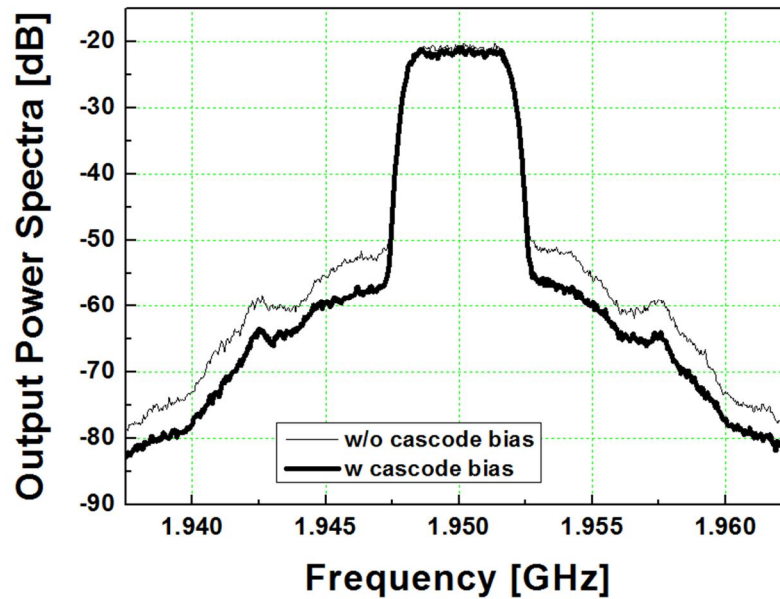
Figure 4.18. Comparison of the measured ACLR spectra with and without the cascode feedback bias technique at 23.5 dBm output power.

4.6 Conclusion

The cascode feedback bias technique utilizing the leakage signals of the gates of CG devices in a cascode topology for negative feedback is implemented in a novel method. The technique not only enhanced the linearity of the PA, but also alleviated reliability issue of the PA, although it causes non-optimal gain of the PA by negative feedback effects. The measurement results demonstrated ACLR enhancement of more than 5-dBc without degrading the efficiency of the PA, and the voltage stress between the drain and the gate of CG device, which is the bottleneck of the reliability problems for the cascode

PA configuration, decreased from 4.5-V to 1.9-V. Utilizing the essential bias network to implement the ac ground of cascode topology, the technique requires no additional components or space and easily applicable to the multi-stage cascode topology that is the most common structure of the CMOS PA design. The PA is fabricated in a 0.18-μm CMOS process, and it delivers a maximum output power of 26-dBm with a peak PAE of 46.4-%, and a linear output power of 23.5-dBm with a 40-% PAE using 3GPP modulated signal. This PA shows the potentials of highly efficient CMOS PA design approach for wireless communication standards.

CHAPTER 5

A HIGHLY EFFICIENT BALANCED CMOS LINEAR POWER

AMPLIFIER WITH LOAD IMMUNITY

5.1 Introduction

The operation environment of wireless communication systems varies, depending on the external conditions such as the changes in the impedance of the antenna, contacts with conductive or grounded surfaces, and so on; and the mismatch of the load impedance under the uncontrolled environment conditions can lead to critical performance degradations of wireless communication devices. Specifically, because of the lack of reliability of CMOS technology under load mismatch and matching mismatch conditions, implementing PAs for a single-chip transmitter in CMOS technology has become problematic. There has been increasing interests to establish robust and load-insensitive PAs in mobile devices. Because the balanced PA structure is inherently insensitive to variations in load impedance and load matching, it can be an excellent option for current mobile communication systems.

This chapter examines the balanced PA topology and its advantages and presents the implementation of a highly efficient balanced CMOS PA for WCDMA applications.

5.2 Balanced PA topology

The balanced PA topology, first introduced in 1965 [36], consists of two PAs and 90-degree phase shifters or a quadrature coupler at the input and the output, illustrated in Figure 5.1. The balanced PA achieves several inherent advantages by 90 degree phase-shift at the input and the output, including load insensitivity, a constant gain, enhanced stability, a wide bandwidth, and improved input and output matching [23],[37]-[42]. Moreover, the output power can be increased by 3-dB through the power combining of two identical amplifiers. The following sections discuss the advantages of the balanced PA configuration.
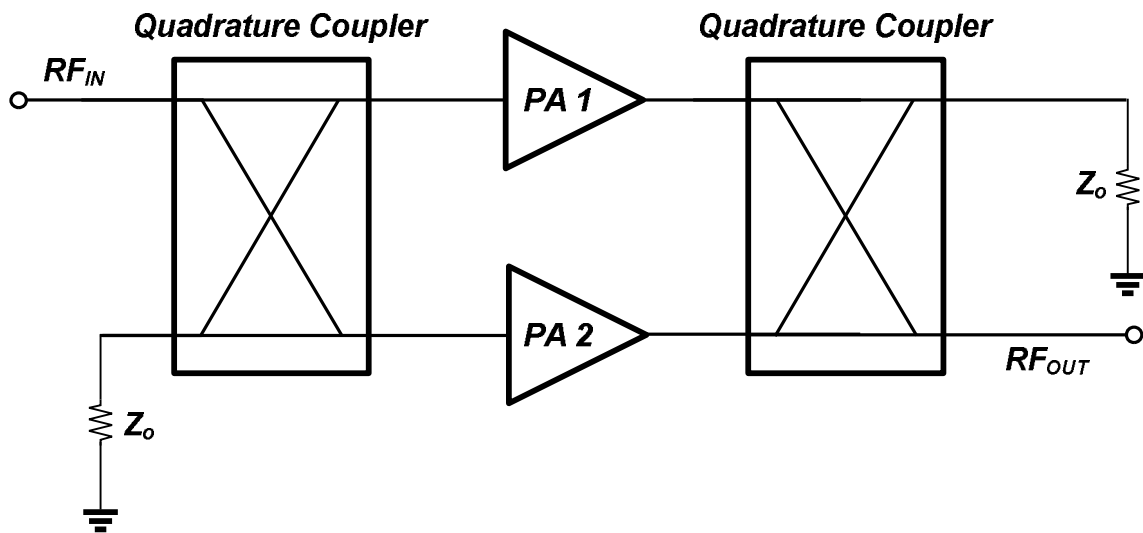
Figure 5.1. Block diagram of the balanced PA.

5.2.1 Load immunity

One of the most attractive advantages of the balanced PA is load insensitivity, which is essential for recent mobile wireless communication applications. When the output

impedance is not properly matched to 50 ohm, it changes the load impedance of the PAs via the output matching network transition, causing movement in the load impedance that in turn results in performance degradations of the PAs. Thus, recent mobile wireless systems demand that performance be robust and stable under 2.5:1 voltage standing wave ratio (VSWR) conditions, and also requires that it withstand harsher 10:1 VSWR conditions. The VSWR is expressed as the equation (5.1), and the PA under 10:1 VSWR condition can have up to 82% of reflection, which might bring a higher voltage swing to the devices and damage them.

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{5.1}$$

With the variations of the output load impedance, the PA also experiences the performance degradation. For example, the current consumption of the PA can be fluctuated and the linearity and the gain performances of the PA can be degraded by the load impedance variations. In the balanced configuration, each PA has a 90-degree phase difference, so the load impedance of the each PAs is always located in the opposite position in the Smith Chart because the chart has a 180 degree as one circle, as shown in Figure 5.2. Therefore, in case of current variation, when the current of one PA increases because of a change in the load impedance, the current of the other PA decreases, and vice versa; that is, one PA compensates for the variations in the current of the other PA. Figure 5.3 shows the simulation results of the normalized current variations of the balanced PA versus those of the single-ended PA under the 2.5:1 load mismatch condition. The results show that the balanced PA underwent significantly fewer current variations than the single-ended PA.
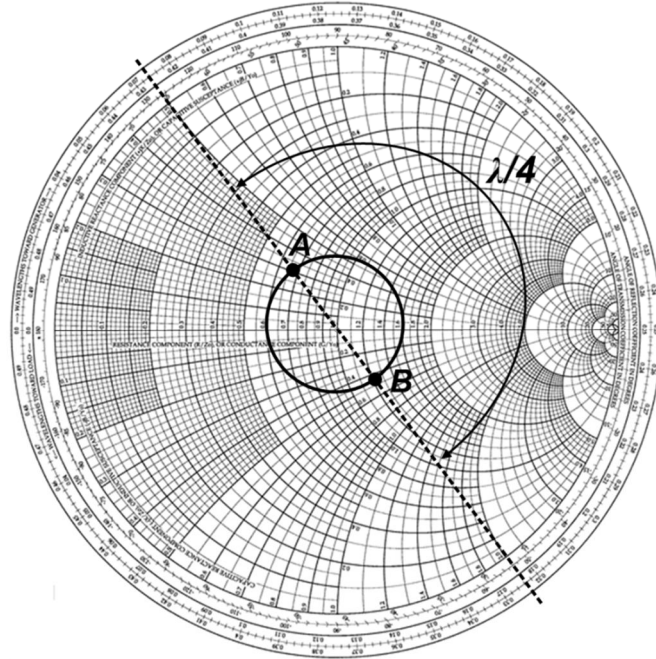
Figure 5.2. Load impedance transition of a balanced topology in the Smith Chart.
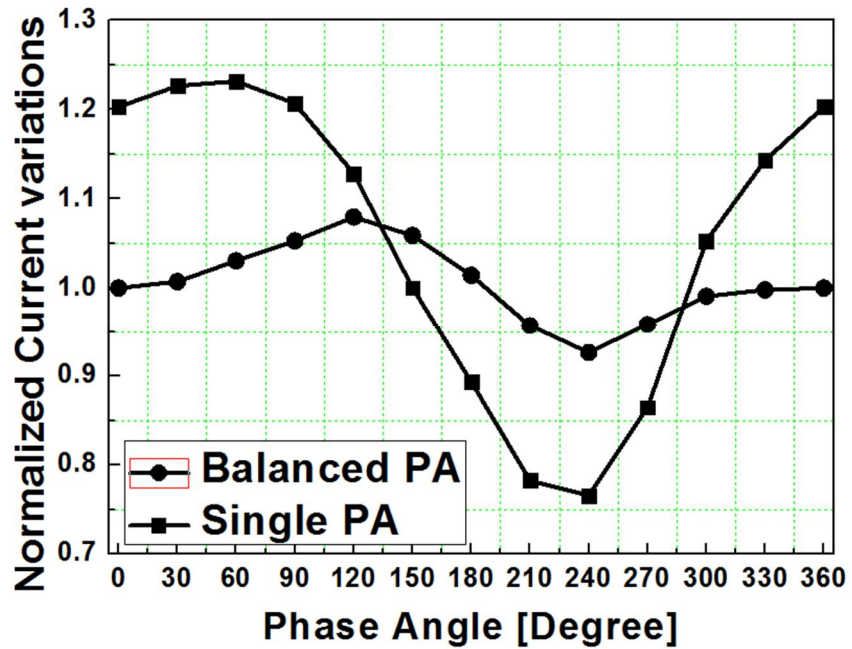
Figure 5.3. Simulated normalized current variations of the balanced PA vs the single-ended PA under a 2.5:1 VSWR condition.

5.2.2 Enhanced matching network and constant gain

In this section, the advantages of balanced topology for improved matching network and a constant gain will be explained. The quadrature operation of the balanced PA is shown in Figure 5.4. The first quadrature coupler divides the input signal into two paths of the PA with a 90 degree relative phase difference, and the second quadrature coupler combines the output signals with the same phase.
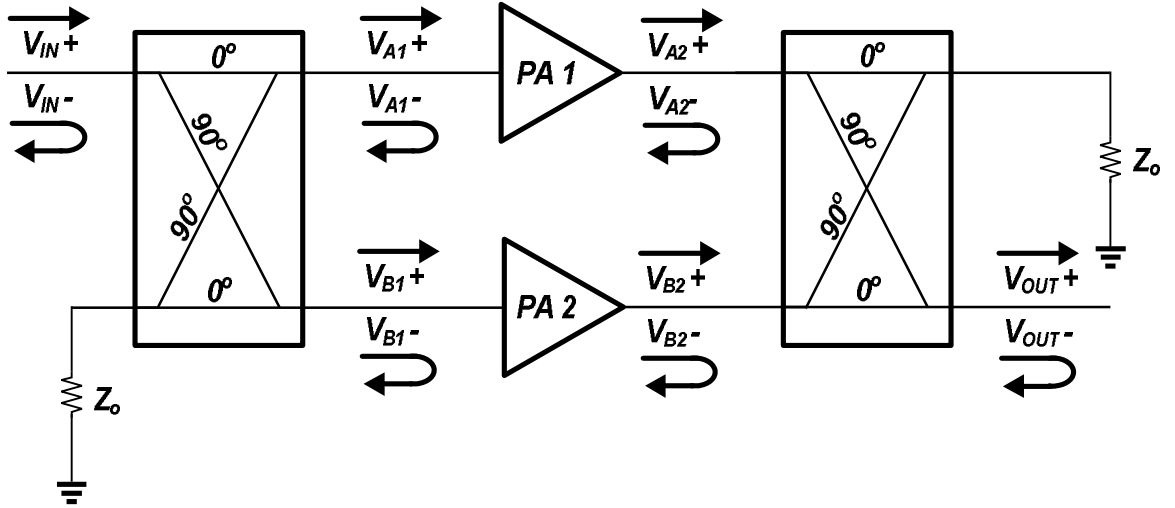
Figure 5.4 Quadrature operation of the balanced PA.

With the assumption that quadrature couplers are ideal components, the divided input signal, V_{a1}^+ and V_{b1}^+ can be expressed as

$$V_{a1}^+ = \frac{1}{\sqrt{2}} V_{in}^+ \tag{5.2}$$

$$V_{b1}^+ = \frac{-j}{\sqrt{2}} V_{in}^+ \tag{5.3}$$

The reflected signal at the input of the PA, V_{a1}^- and V_{b1}^-, can be shown as

$$V_{a1}^- = \Gamma_A V_{a1}^+ \tag{5.4}$$

where Γ_A is a reflection coefficient of the upper path amplifier, and

$$V_{b1}^- = \Gamma_B V_{b1}^+ \tag{5.5}$$

where Γ_B is a reflection coefficient of the lower path amplifier.

The total reflected signal of balanced amplification, V_{in}^- can be written as

$$V_{in}^- = \frac{1}{\sqrt{2}} V_{a1}^- + \frac{-j}{\sqrt{2}} V_{b1}^- = \frac{1}{2} V_{in}^+ (\Gamma_A - \Gamma_B) \tag{5.6}$$

That is, the reflected signal from the upper path, A, has no phase change while the reflected signal from the lower path, B, has two times of 90 degree phase change, resulting in 180 degree phase changes. From equation (5.6), the input port voltage reflection coefficient, S_{11}, is derived as

$$S_{11} = \frac{V_{in}^-}{V_{in}^+} = \frac{1}{2} (\Gamma_A - \Gamma_B) \tag{5.7}$$

Because the balanced PA consists of identical amplifiers, the reflection coefficient of each PAs, Γ_A and Γ_B are ideally the same. Therefore, with the negative sign causing by 180 degree phase shift between Γ_A and Γ_B, S_{11} can achieve zero or small enough value, thus enhancing the input match. The output port voltage reflection coefficient, S_{22}, can also be derived by the same analysis. As the derived analysis represents, the quadrature operation of balanced PA provides improved input and output matching.

The merit of the constant gain can also be achieved by the quadrature operation of balanced PA. The total delivered signal of balanced amplification, V_{out}^+, is derived as

$$V_{out}{}^{+} = \frac{-j}{\sqrt{2}}V_{a2}{}^{+} + \frac{1}{\sqrt{2}}V_{b2}{}^{+} = \frac{-j}{\sqrt{2}}G_A V_{a1}{}^{+} + \frac{1}{\sqrt{2}}G_B V_{b1}{}^{+} = \frac{-j}{2}V_{in}{}^{+}(G_A + G_B) \qquad (5.8)$$

From equation (5.8), S_{21} is derived as

$$S_{21} = \frac{V_{out}{}^{+}}{V_{in}{}^{+}} = \frac{-j}{2}(G_A + G_B) \qquad (5.9)$$

The overall gain of the balanced PA is the average of the gain of two PA, and therefore it is relatively constant over the impedance variation.

5.2.3 Improved stability

The balanced topology helps improve the stability of the PA [19]. The stability of the PA can be indicated by the factors of K, B, and Mu, as shown in equation (5.10), (5.11) and (5.12). As the equations express, S_{11} and S_{22} are two dominant factors of the stability of PA. When S_{11} and S_{22} decrease by balanced topology, as discussed in the previous section, the values of the stability factor increases. The stability improvement is verified by the simulations of each factor with both the small and the large signal, and described in Section 5.3.4.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \qquad (5.10)$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0 \qquad (5.11)$$

$$Mu = \frac{1 - |S_{11}|^2}{\{|S_{22} - {}^*S_{11} \cdot (S_{11}S_{22} - S_{12}S_{21})| + |S_{12}S_{21}|\}} > 1 \qquad (5.12)$$

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Advantages of balanced topology are discussed, and a comparison of single-ended PA versus balanced PA is listed in Table 4.

TABLE 4. COMPARISON OF A SINGLE-ENDED PA VERSUS A BALANCED PA.

	Strength	Weakness
Single-ended PA	• Simple structure and matching • A little higher PAE at peak power level	• An isolator may be required for the load sensitivity
Balanced PA	• Superior performances under mismatch condition • More stable • Applicable to dual-mode operation • Constant gain • No isolator required	• Bulky size with two quadrature coupler • More component count

5.3 *A highly efficient balanced CMOS linear PA design*

5.3.1 Balanced PA in CMOS technology

As discussed in the previous section, the quadrature nature of balanced PA topology can significantly benefit mobile communication systems. The power combining mechanism of the two identical amplifiers also provides dual-mode operations that can be utilized by deactivating/activating one of the paths of the balanced PA. As it saves the bias current, the efficiency at the back-off output power improves. As shown in Figure

5.5 (a), the proposed CMOS balanced PA utilizes simple L-C quadrature splitters/combiners at the input and the output. The overall circuit is fully-integrated in a single-chip. Figure 5.5 (b) shows efficiency versus output power in dual mode operations.
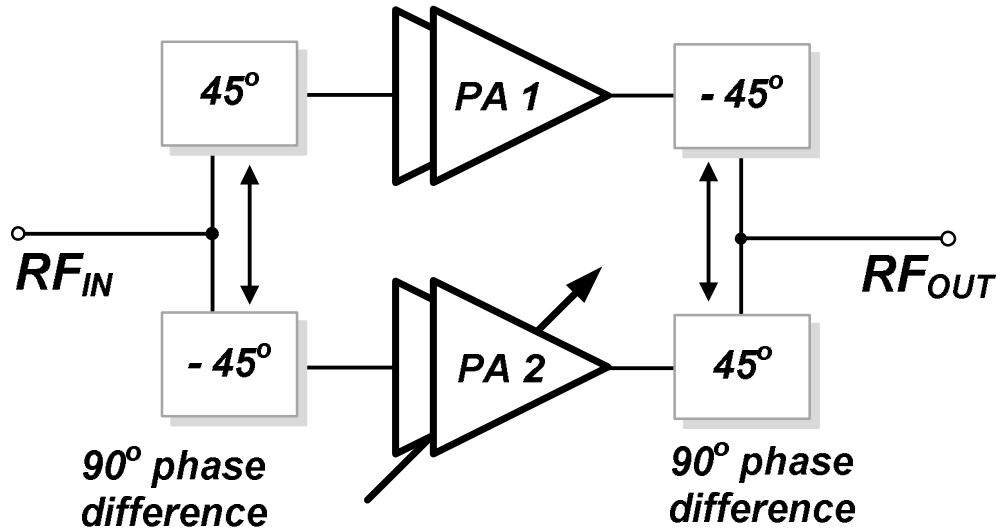
(a)
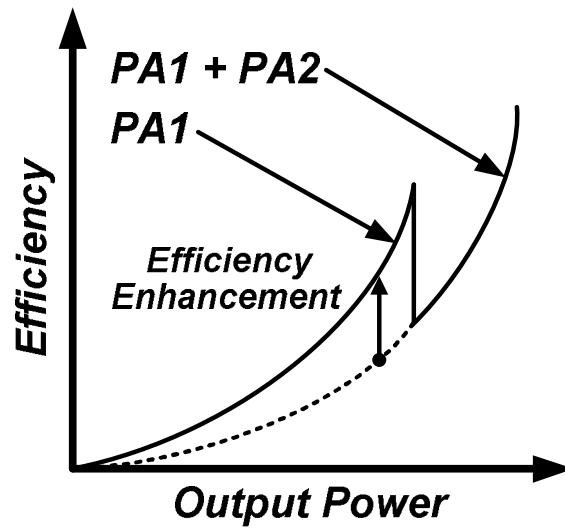
(b)

Figure 5.5. The balanced CMOS PA. (a) block diagram. (b) efficiency versus output power.

5.3.2 L-C quadrature splitter/combiner

To split the input signal into two with a quadrature phase difference, the inductor and the capacitor are utilized as shown in Figure 5.6. The inductor and the capacitor have the same impedance with opposite phase shifts of +45 and -45 degrees, respectively, leading to a 90-degree phase difference between the upper and lower paths [37]. The impedances at the output of each PA are derived as the equation (5.13) and (5.14), and they represent quadrature phase difference.

$$PA1_{output} = \frac{R}{R + \dfrac{1}{j\omega C}} = \frac{j\omega RC}{1 + j\omega RC} \tag{5.13}$$

$$PA2_{output} = \frac{R}{R + j\omega L} = \frac{1}{1 + j\omega \dfrac{L}{R}} \tag{5.14}$$

For the implementation of L-C quadrature splitter/combiner, the inductor value is calculated as

$$L_{in} = \frac{R}{(2 \cdot \pi \cdot freq)} \tag{5.15}$$

and the capacitor value is calculated as

$$C_{in} = \frac{1}{(2 \cdot \pi \cdot freq \cdot R)} \tag{5.16}$$
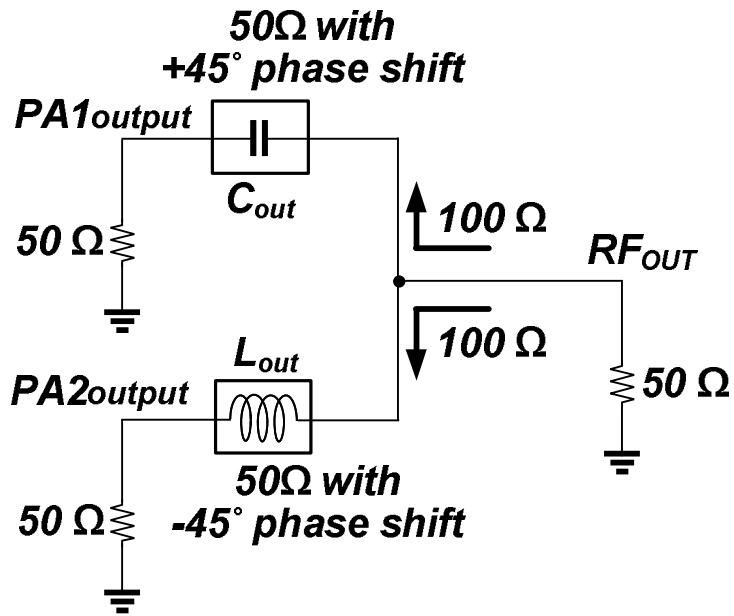
Figure 5.6. L-C quadrature splitter/combiner.

Figures 5.7 show the simulation results of the L-C quadrature splitter/combiner operating at 2GHz. It achieved -3 dB power dividing/ combining with 90 degree phase difference at the desired frequency. With the EM simulation and parasitic extractions, the values of the inductor and the capacitor with the equations are additionally optimized to provide an accurate 90-degree phase difference in the overall balanced PA implementation.
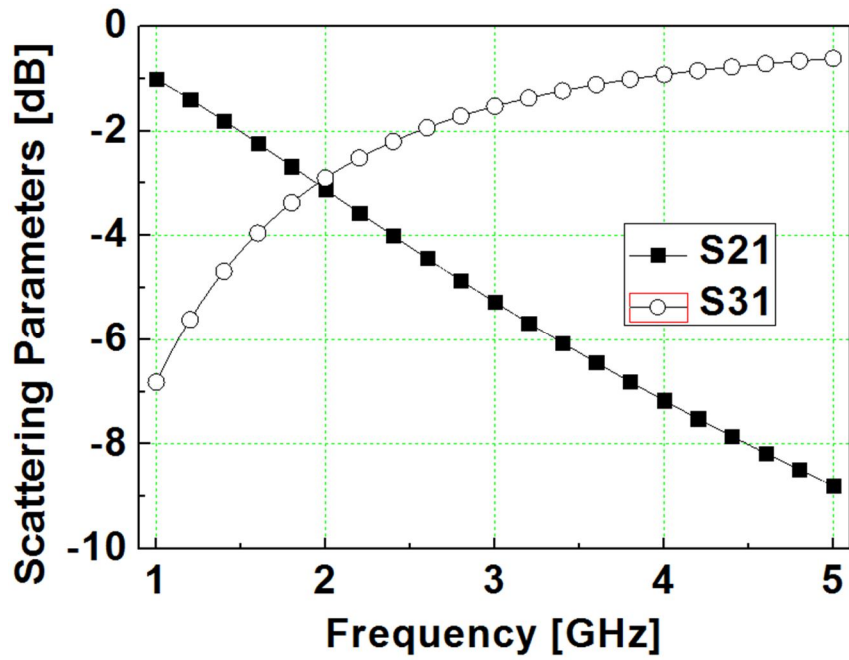
(a)
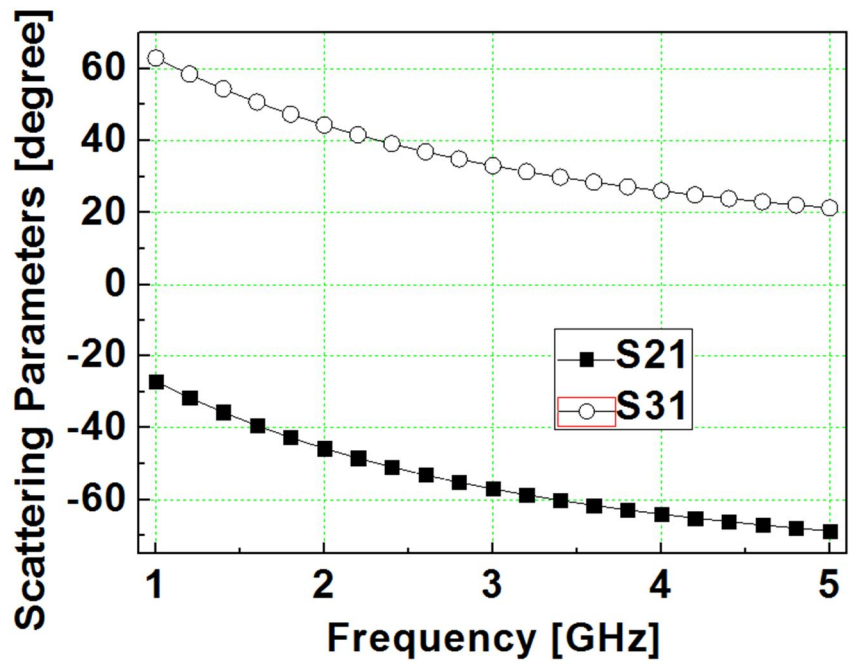
(b)

Figure 5.7. Simulation results of the L-C quadrature splitter/combiner (a) dB. (b) Phase.

5.3.3 PA design

The overall schematic diagram of the balanced PA is shown in Figure 5.8. The individual PA consists of input matching, a driver stage, interstage matching, a power stage, and output matching. The two-stage cascaded configuration is adopted to provide enough gain. The cascode topology also uses thick gate-oxide devices for the common-gate (CG) transistor in the power stage to alleviate the voltage stress and reliability problems. The power stage is a stack of 0.4-μm thick gate-oxide transistors for the CG device (M_4), and a 0.18-μm standard transistor for the common-source (CS) devices (M_3); the driver stage has 0.18-μm transistors for both the CG (M_2), and the CS (M_1) devices in order to compensate the low RF power gain and the high knee voltage of thick gate-oxide CG device (M_4). The widths of the M_2 and M_1 devices in the driver stage are 1536 μm (12 × 16 fingers × 8-μm width) and 960 μm (8 × 15 fingers × 8-μm width), respectively; and the widths of the M_4 and M_3 devices in the power stage are 5632 μm (44 × 16 fingers × 8-μm width) and 4752 μm (33 × 18 fingers × 8-μm width), respectively.
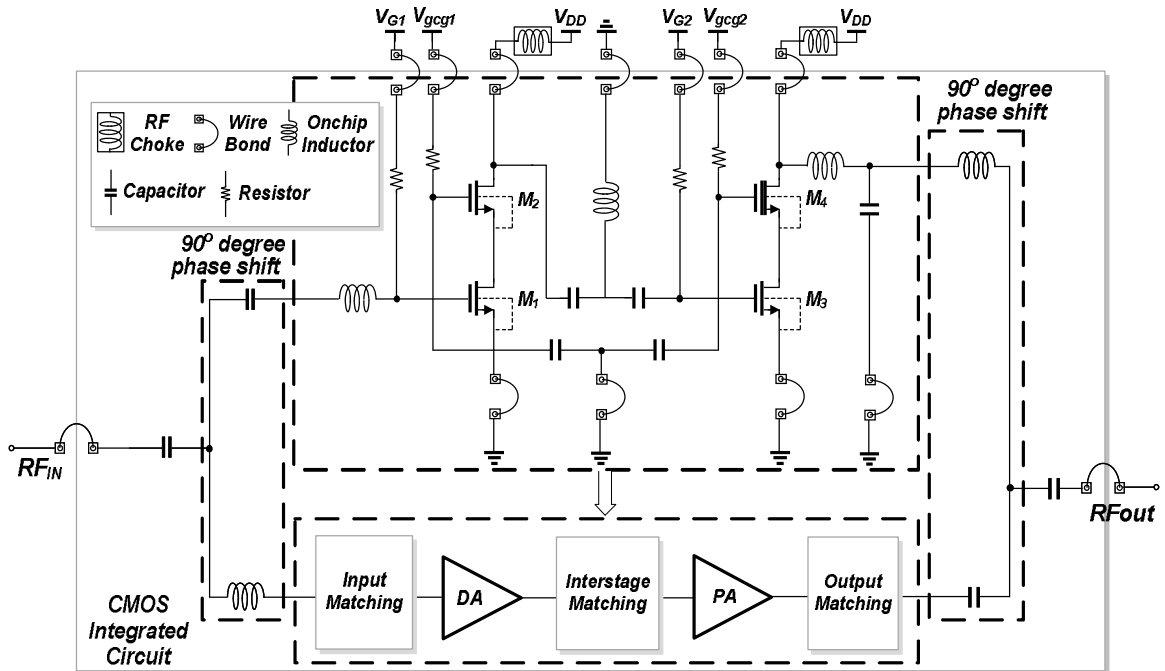
Figure 5.8. Overall schematic diagram of the balanced PA.

Both the driver and the power stages are biased for the class AB operation, which compromises the linearity and the efficiency of the PA. For enhanced linearity and reliability, the cascode feedback bias technique, which shares the same AC ground of the gate nodes of the CG devices in the driver and the power stage, is employed, and multiple bonding wires are used at the source node of each stage to minimize the degeneration effects.

5.3.4 Stability enhancement

The stability improvement is verified by comparing a balanced PA to the single-ended PA. The simulated stability factors K, B and Mu are plotted in Figures 5.9 (a), (b) and (c). As the figures show, the values of all three stability factors of balanced PA is larger than single-ended PA. With large signal at the operating frequency, the stability is

also improved, as shown in the figure 5.10 (a), (b), and (c).
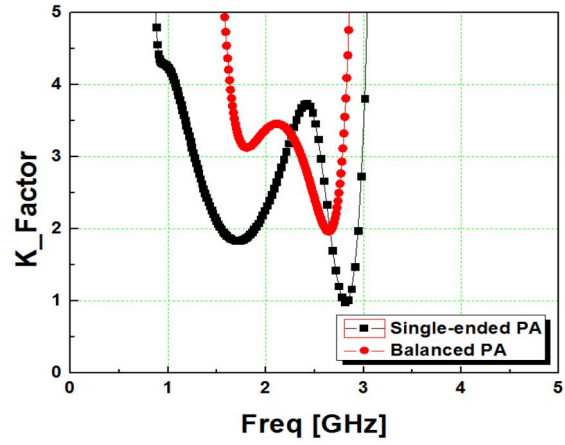
(a)
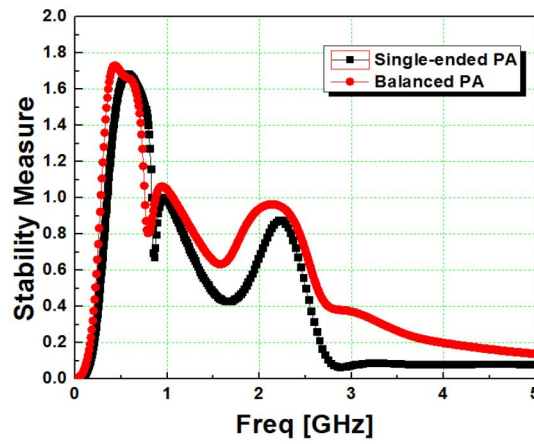
(b)
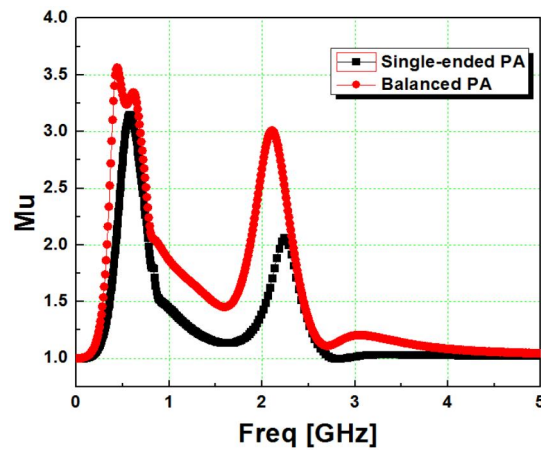
(c)

Figure 5.9. Stability comparison of single-ended PA versus balanced PA using small signal. (a) K factor (b) B factor (c) Mu factor.
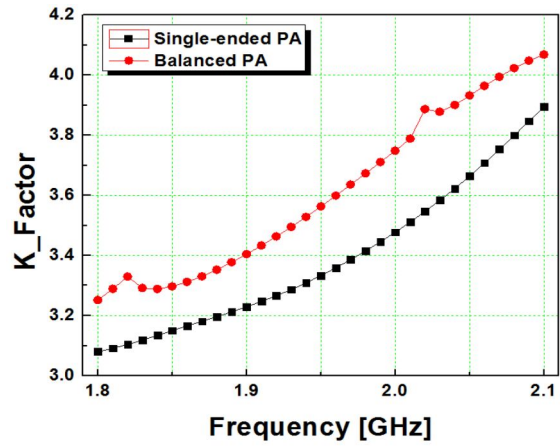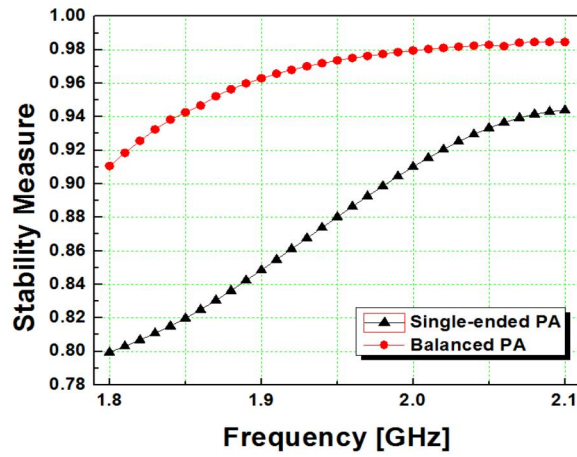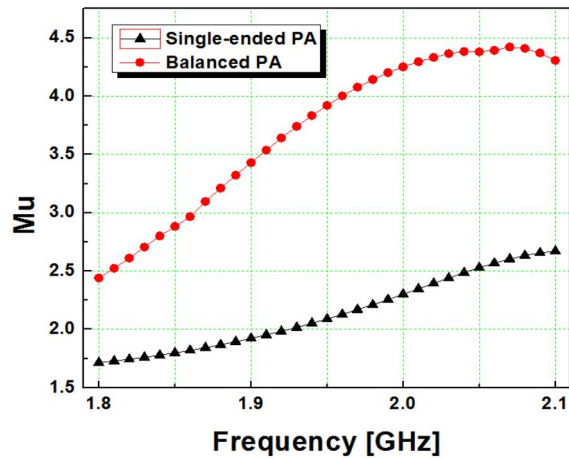
Figure 5.10. Stability comparison of single-ended PA versus balanced PA using large signal. (a) K factor (b) B factor (c) Mu factor.

5.4   Measurement results

The die microphotograph of the PA is shown in Figure 5.11. The PA is fabricated in IBM7RF 0.18-μm CMOS technology with a total die area of 1.60 mm × 1.02 mm, including bonding pads. The die is attached to a FR-4 printed circuit board (PCB) with 50-Ω input and output terminations for the measurement.
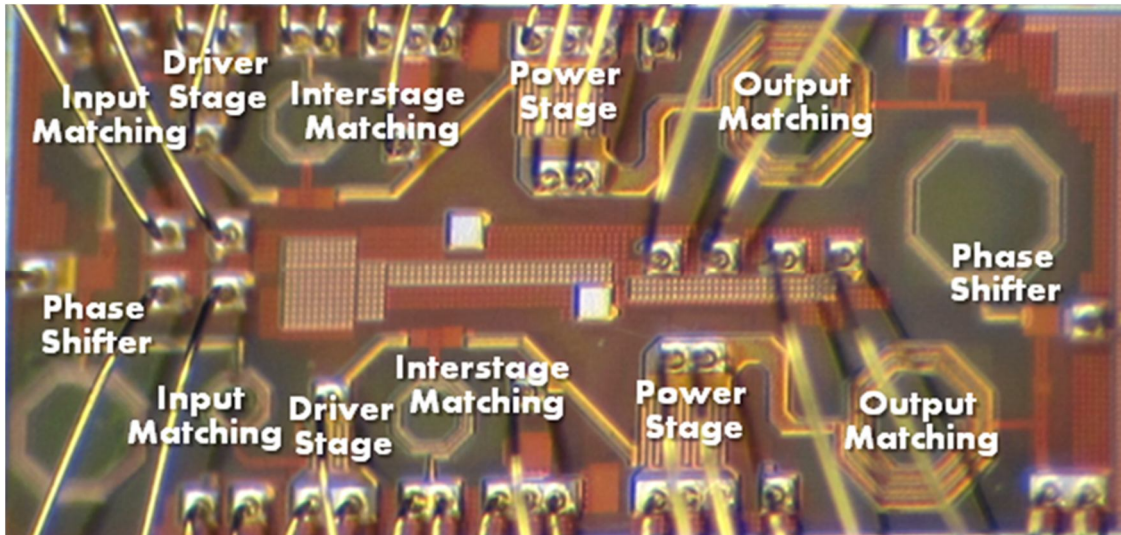
Figure 5.11. Microphotograph of the balanced PA.

Figure 5.12 shows the measured power sweep results of both high power (HP) and low power (LP) mode. The PCB and cable losses are de-embedded while the wire bonding losses are included in the performance measurements. Using a 3GPP WCDMA modulated signal, the PA provides 40.4% peak PAE at 29 dBm of maximum output power and a 35 % PAE at 26.4 dBm of linear output power. The output referred 1-dB compression point (P_{1dB}) for the high-power (HP) mode is 27.3 dBm. In the low- power

(LP) mode, the PA achieves 33.4% peak PAE at 23.1-dBm of maximum output power and produces 18.4-% PAE at 16 dBm. The PA exhibits a small signal gain of 21.2 dB in the HP mode and 19.6 dB in the LP mode.
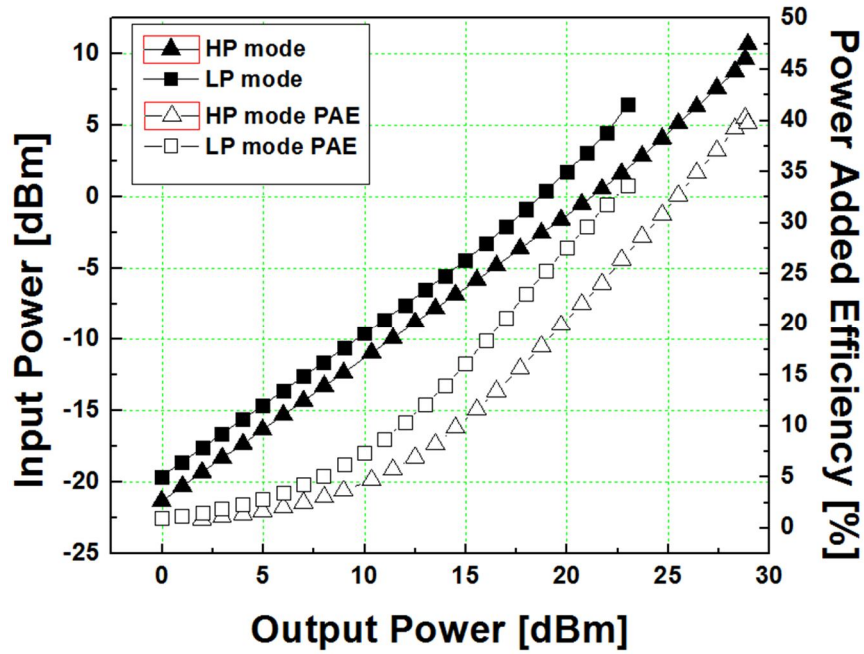
Figure 5.12. Measured power sweep results of both HP and LP mode.

The measured ACLR results in both the LP and HP modes are presented in Figure 5.13, and the required linearity specification of -33 dBc ACLR is guaranteed up to 26.4 dBm of output power. The ACLR spectrum is captured at the maximum linear output power as shown in Figure 5.14.
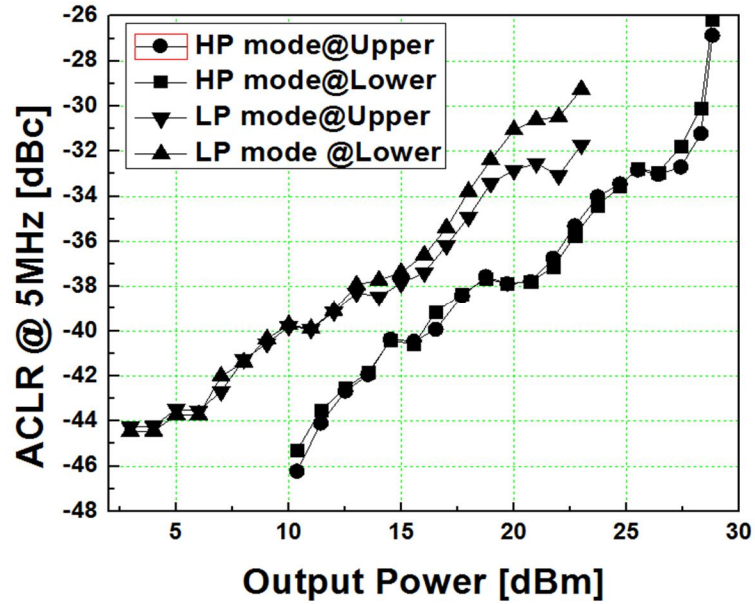
Figure 5.13. Measured ACLR results of both HP and LP mode.
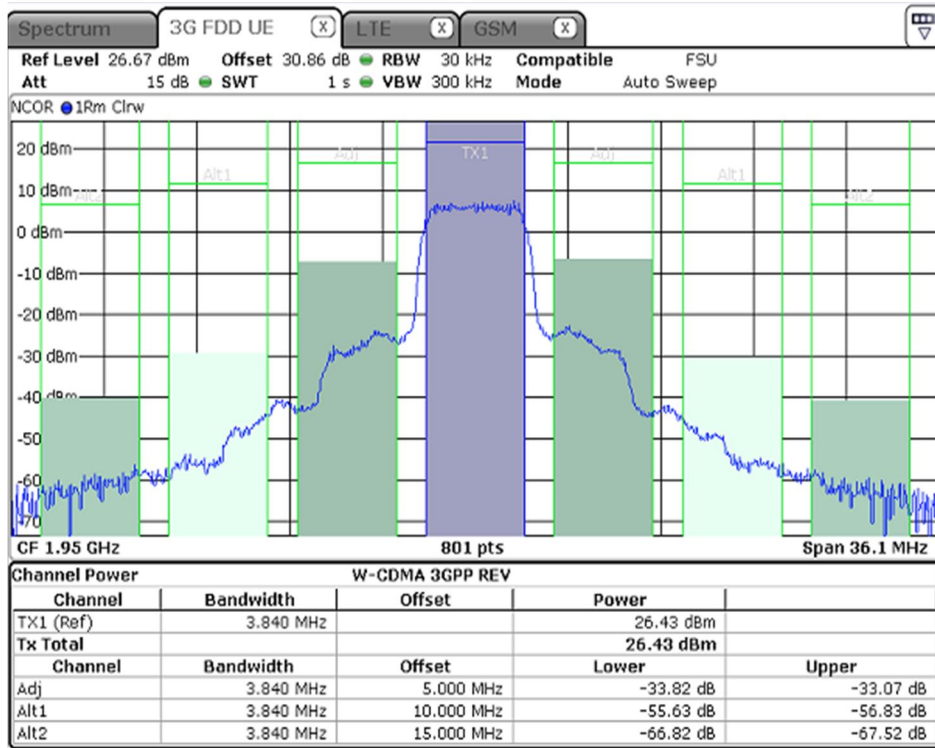
Figure 5.14. Captured ACLR spectrum at 26.4 dBm output power.

Because of the improved matching of the balanced topology, small return losses are excellently achieved, that is, S_{11} and S_{22} of the PA are better than -22 dB and -16.7 dB, respectively, as shown in Figure 5.15. Compared to the return losses of single-ended PA, which are -12 dB, and -10 dB, respectively, those of balanced PA are much lower, demonstrating the enhanced matching networks by quadrature operations.
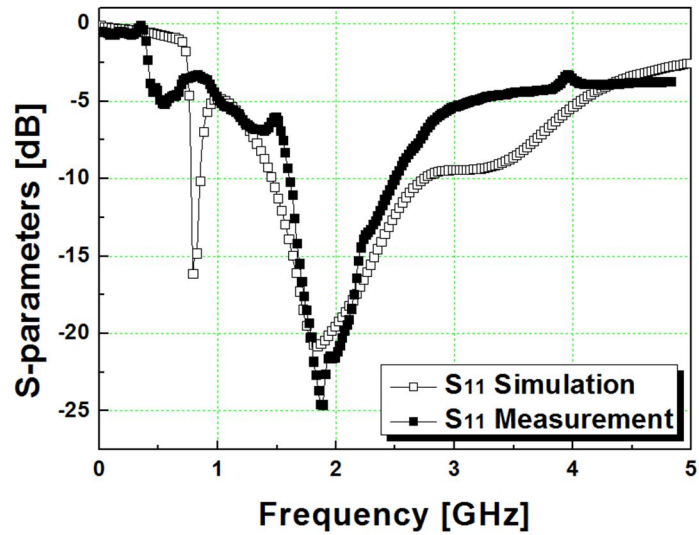
(a)
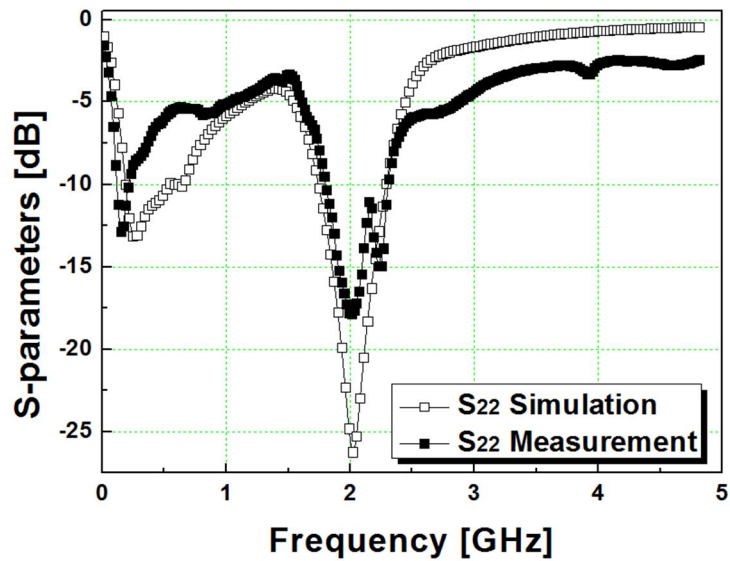
(b)

Figure 5.15. Measured scattering parameters of the balanced PA (a) S_{11}. (b) S_{22}.
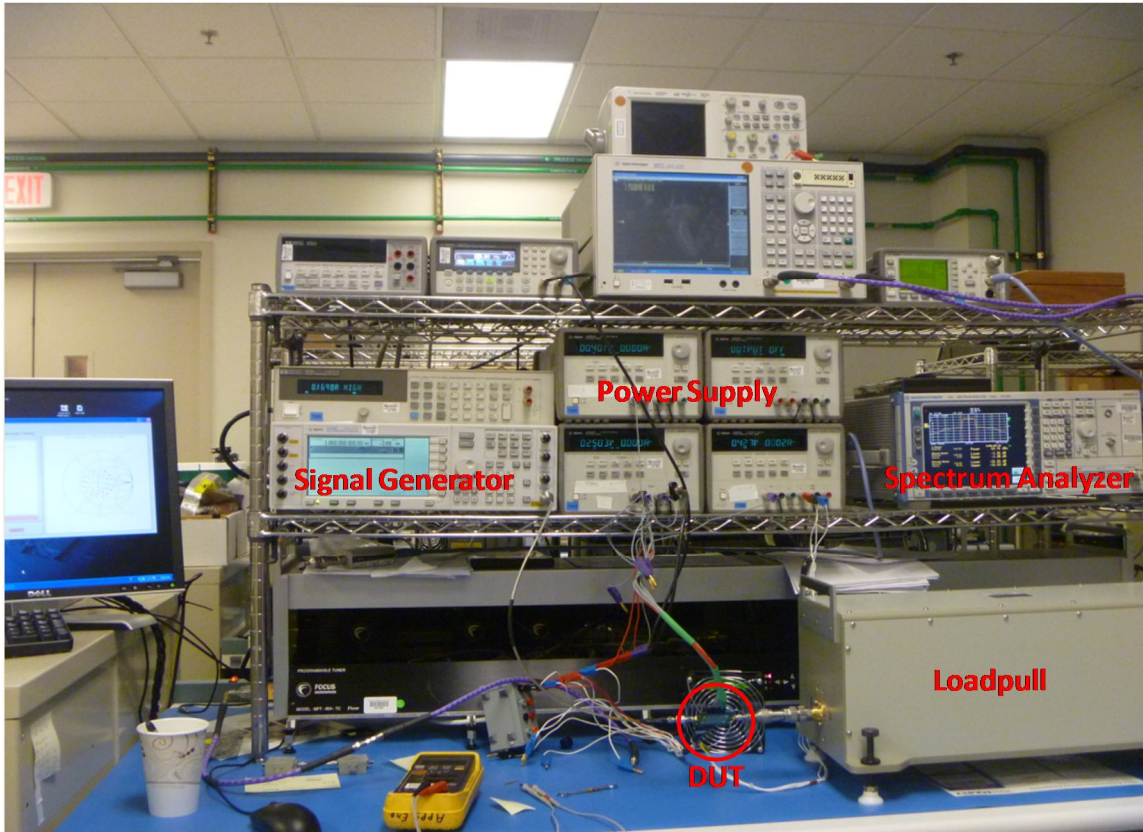
Signal Generator	AG4438C
Pulse Generator	AG33250A
Tuner	MT981BU
PA supply voltage	3.4 V
Modulation	GTC 1
Temperature	25 ˚C

Figure 5.16. Test bench for load-pull measurement and its equipments.

Figure 5.16 shows the test bench for the load-pull measurement and its equipments. The load-pull characteristics are measured at 23 dBm output power (back-off output power) under 2.5:1 of VSWR condition. Figure 5.17 (a) shows the captured load insensitivity characteristics of the single-ended PA for gain, current and EVM, and Figure

5.17 (b) plots the ACLR of a single-ended PA with 5 MHz and 10 MHz spacing, respectively.
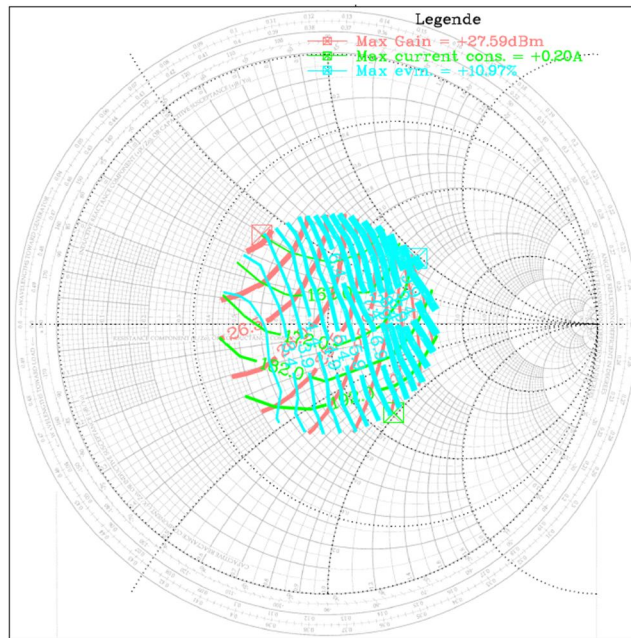
(a)
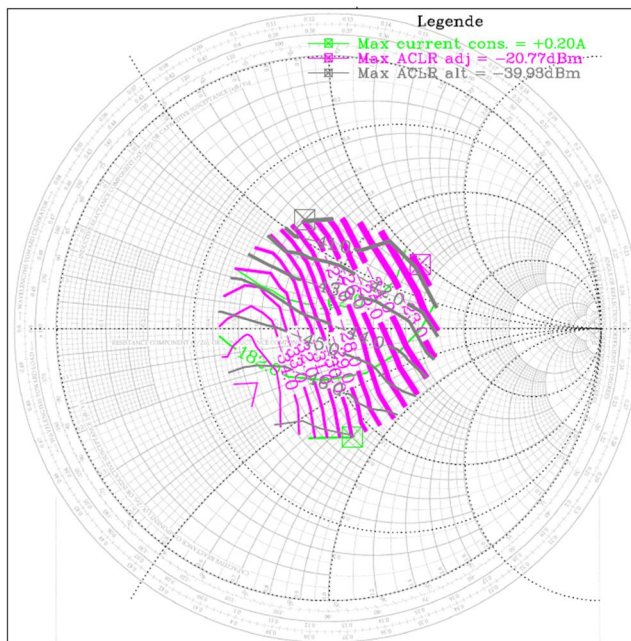
(b)

Figure 5.17. Captured load insensitivity characteristics of single-ended PA up to 2.5:1 of VSWR condition. (a) gain, EVM and current. (b) ACLR of 5MHz and 10MHz spacing.
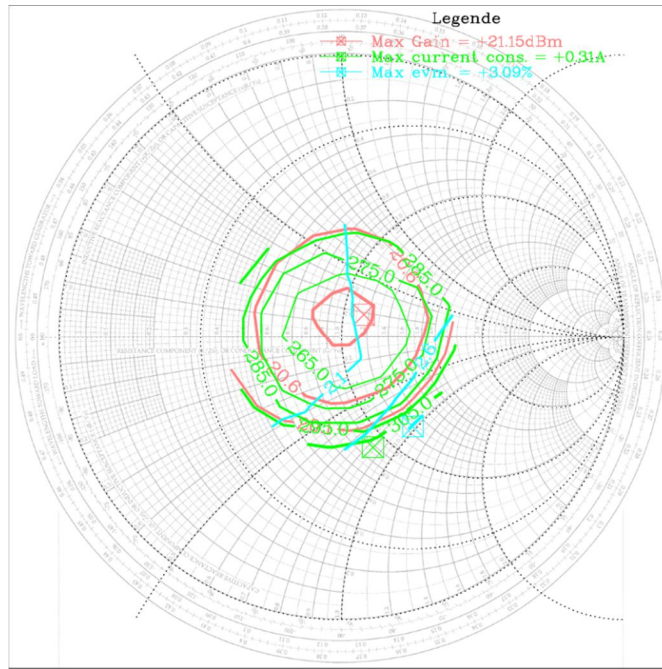
(a)
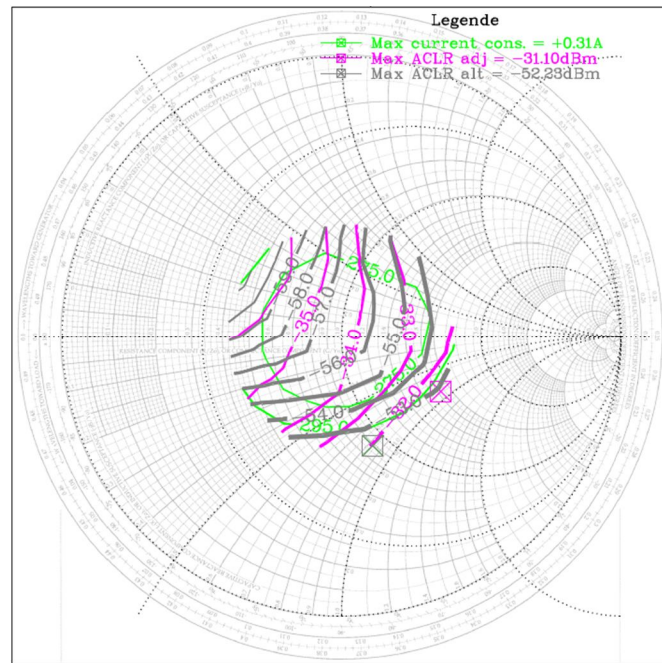
(b)

Figure 5.18. Captured load insensitivity characteristics of balanced PA up to 2.5:1 of VSWR condition. (a) gain, EVM and current. (b) ACLR of 5MHz and 10MHz spacing.

The captured load insensitivity characteristics of the balanced PA up to 2.5:1 VSWR condition are demonstrated in Figure 5.18 (a) and (b). Compared to a single-ended PA, balanced PA has much strong immunity than single-ended PA. The load variation immunity comparison of balanced PA versus single-ended PA with impedance on 2.5:1 of VSWR circle is shown in Figure 5.19. The balanced PA has 1-dB of gain variation and has less than 44 mA peak-to-peak current variation, while single-ended PA has 6 dB gain variation and 61 mA peak-to-peak current variation. That is, the balanced PA achieved robust operations under variations of the external environment.
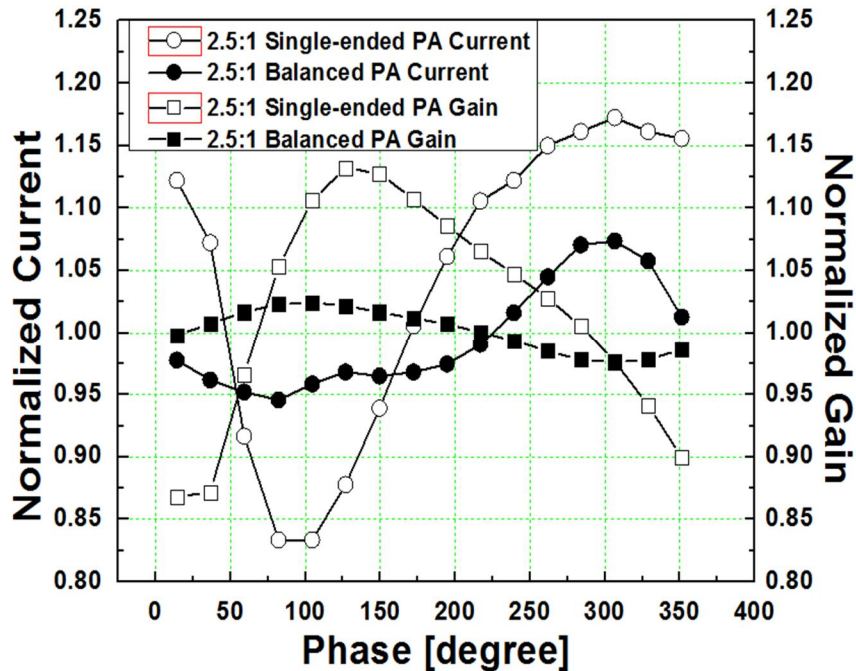
Figure 5.19. Comparison of balanced PA and single-ended PA under 2.5:1 VSWR condition.

A comparison of the recently reported linear PAs for WCDMA applications is shown in Table 5. The balanced CMOS PA demonstrates comparable performances to other efforts, and it achieves the most improved low-power efficiency at 16 dBm output power in CMOS technology.

TABLE 5. COMPARISON OF LINEAR PA PERFORMANCES FOR <u>WCDMA</u> APPLICATIONS.

Reference	Technology	Frequency [GHz]	V_{BAT} [V]	Linear P_{OUT} / Peak P_{out} [dBm]	Linear PAE/ Peak PAE [%]	Gain	Power Backoff [% / 16 dBm]
This Work	**CMOS 0.18 μm**	**1.95**	**3.4**	**26.4/ 29**	**35/ 40.4**	**21.2**	***18.4**
[16]	CMOS 0.5 μm	1.75	3.3	24/ 25	29/ 33	23.9	8
[43]	SiGe HBT	1.95	3	23.9/ 25.9	< 31/ 31	5.3	10
[44]	SOI 0.13 μm	1.9	6.5	29.4/ 31.6	41.4/ 47	14.6	8
[45]	SOI CMOS 0.13 μm	1.92	1.2	21.7/ 25.2	38/ 40 <	27	N/A
[37]	GaAs/InGap HBT	1.95	3.4	28/ N/A	44.5/ N/A	29	*21

* Multi-mode operations

5.5 Conclusion

A highly efficient balanced linear PA in a 0.18-μm CMOS process is presented. The proposed PA delivers a maximum output power of 29 dBm with a peak PAE of

40.4 %, and a linear output power of 26.4 dBm with a 35% PAE using a 3GPP modulated signal. The measurement results demonstrated excellent load insensitivity and high efficiency at peak power level as well as at back-off power level. The proposed PA, implemented in a single CMOS die, demonstrates a potential PA design approach for WCDMA applications using a standard CMOS technology.

CHAPTER 6

A TRIPLE-MODE BALANCED LINEAR CMOS POWR AMPLIFIER USING A SWITCHED QUADRATURE COUPLER

6.1   Introduction

It is intuitive to operate a balanced PA in dual-modes. To further optimize the battery life with better tracking of the probability distribution function of the transmitted signal, a more delicate power level control and mode operations are required. This chapter presents a triple-mode balanced linear PA for WCDMA applications. To enhance the overall efficiency, this work utilizes a novel triple-mode operation along with a balanced topology to accommodate load insensitivity characteristics, as shown in Figures 6.1. The PA uniquely utilizes the isolation port of the quadrature coupler for LP mode as a signal path with the control of RF switches, as shown in Figure 6.2. Then, an output matching network that provides the required conditions for both the LP and HP mode of operations is incorporated. To obtain low loss and a high quality factor (Q) of passive output combining, a transformer-based quadrature coupler is implemented using a silicon integrated passive device (IPD) process.
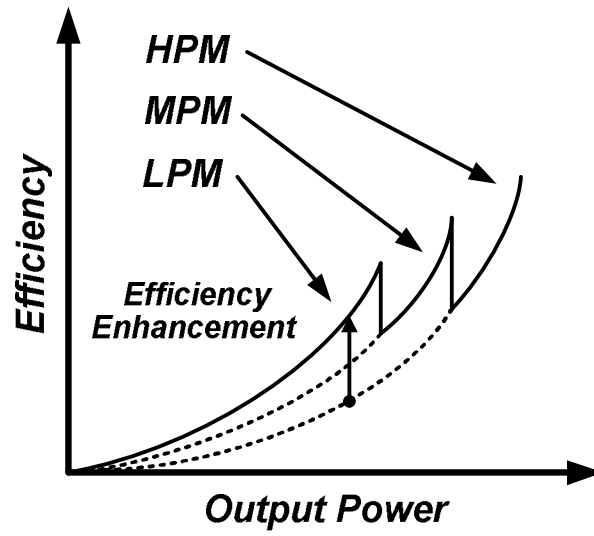
Figure 6.1. Efficiency enhancements at lower power level by multi-mode operations.
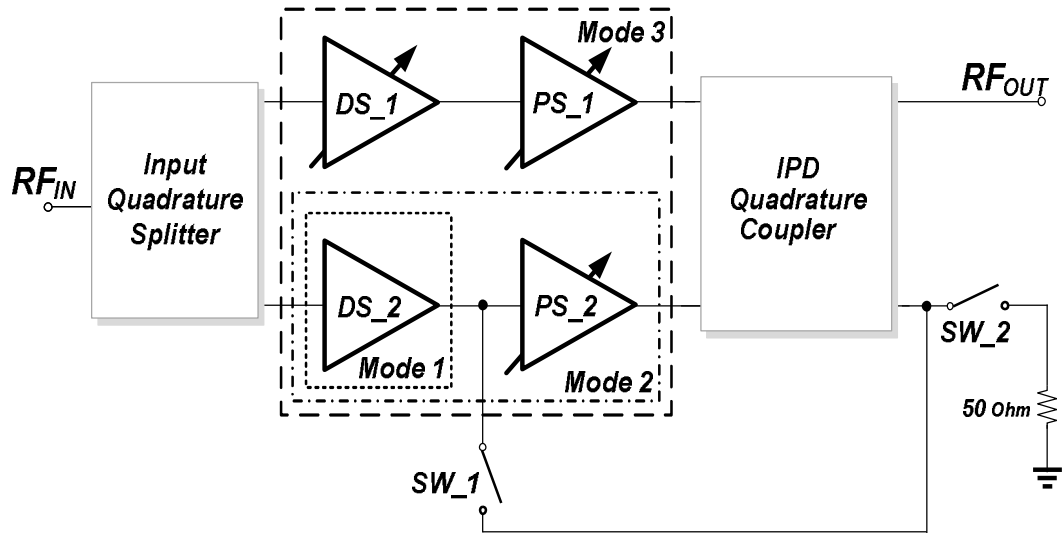
Figure. 6.2. Block diagram of the triple-mode balanced PA with a switched quadrature coupler.

6.2 Average efficiency enhancement

6.2.1 Analysis of four-port network operation under the termination of two ports

This section analyzes the four-port network under the condition of terminating two ports to create a signal path through the other ports. The proposed PA utilizes a four-port quadrature coupler at the output and creates a signal path by using the isolation port while terminating the through port and the coupled port of the quadrature coupler. Figure 6.3 shows a reciprocal four-port network with terminations of ports 3 and 4.
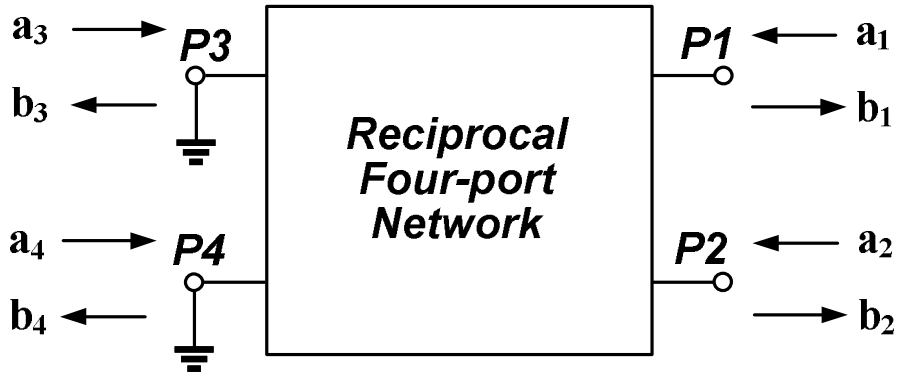
Figure 6.3. Reciprocal four-port network with terminations of port 3 and 4.

First of all, the nominal impedance of the scattering parameter is defined as Z_0, and the port impedances are presented as Z_n. The reflections of each port are

$$\Gamma_n = \frac{Z_n - Z_0}{Z_n + Z_0} \tag{6.1}$$

With the assumption that ports 3 and 4 are terminated, the reciprocal scattering equations are

$$b_1 = S_{11}a_1 + S_{12}a_2 + \Gamma_3 S_{13}b_3 + \Gamma_4 S_{14}b_4 \tag{6.2}$$

$$b_2 = S_{12}a_1 + S_{22}a_2 + \Gamma_3 S_{23}b_3 + \Gamma_4 S_{24}b_4 \tag{6.3}$$

$$(1-\Gamma_3 S_{33})b_3 = S_{13}a_1 + S_{23}a_2 + \Gamma_4 S_{34}b_4 \tag{6.4}$$

$$(1-\Gamma_4 S_{44})b_4 = S_{14}a_1 + S_{24}a_2 + \Gamma_3 S_{34}b_3 \tag{6.5}$$

Then, the equations can be defined with a_1 and a_2 by removing b_3 and b_4 in the equations:

$$b_1 = (S_{11} + \frac{\Gamma_3 S_{13}((1-\Gamma_4 S_{44})S_{13} + \Gamma_4 S_{14}S_{34}) + \Gamma_4 S_{14}((1-\Gamma_3 S_{33})S_{14} + \Gamma_3 S_{13}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_1 + (S_{12} + \frac{\Gamma_3 S_{13}((1-\Gamma_4 S_{44})S_{23} + \Gamma_4 S_{24}S_{34}) + \Gamma_4 S_{14}((1-\Gamma_3 S_{33})S_{24} + \Gamma_3 S_{23}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_2 \tag{6.6}$$

$$b_2 = (S_{12} + \frac{\Gamma_3 S_{23}((1-\Gamma_4 S_{44})S_{13} + \Gamma_4 S_{14}S_{34}) + \Gamma_4 S_{24}((1-\Gamma_3 S_{33})S_{14} + \Gamma_3 S_{13}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_1 + (S_{22} + \frac{\Gamma_3 S_{23}((1-\Gamma_4 S_{44})S_{23} + \Gamma_4 S_{24}S_{34}) + \Gamma_4 S_{24}((1-\Gamma_3 S_{33})S_{24} + \Gamma_3 S_{23}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_2 \tag{6.7}$$

$$b_3 = (\frac{(1-\Gamma_4 S_{44})S_{13} + \Gamma_4 S_{14}S_{34}}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_1 + (\frac{(1-\Gamma_4 S_{44})S_{23} + \Gamma_4 S_{24}S_{34}}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_2 \tag{6.8}$$

$$b_4 = (\frac{(1-\Gamma_3 S_{33})S_{14} + \Gamma_3 S_{13}S_{34}}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_1 + (\frac{(1-\Gamma_3 S_{33})S_{24} + \Gamma_3 S_{23}S_{34}}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}})a_2 \tag{6.9}$$

Therefore, the scattering parameters of the four-port network under the condition of terminated ports 3 and 4 are

$$S'_{11} = S_{11} + \frac{\Gamma_3 S_{13}((1-\Gamma_4 S_{44})S_{13} + \Gamma_4 S_{13}S_{34}) + \Gamma_4 S_{14}((1-\Gamma_3 S_{33})S_{14} + \Gamma_3 S_{13}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}} \tag{6.10}$$

$$S'_{22} = S_{22} + \frac{\Gamma_3 S_{23}((1-\Gamma_4 S_{44})S_{23} + \Gamma_4 S_{24}S_{34}) + \Gamma_4 S_{24}((1-\Gamma_3 S_{33})S_{24} + \Gamma_3 S_{23}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}} \tag{6.11}$$

$$S'_{12} = S_{12} + \frac{\Gamma_3 S_{13}((1-\Gamma_4 S_{44})S_{23} + \Gamma_4 S_{24}S_{34}) + \Gamma_4 S_{14}((1-\Gamma_3 S_{33})S_{24} + \Gamma_3 S_{23}S_{34})}{(1-\Gamma_3 S_{33})(1-\Gamma_4 S_{44}) - \Gamma_3 \Gamma_4 S^2_{34}} \tag{6.12}$$

Because the reflection coefficient of ports 3 and 4 are -1 when they are terminated to ground by using equation (6.1), $S_{12}{}'$ is represented as shown in equation (6.13).

$$S'_{12} = S_{12} + \frac{S_{13}(S_{24}S_{34} - (1+S_{44})S_{23}) + S_{14}(S_{23}S_{34} - (1+S_{33})S_{24})}{(1+S_{33})(1+S_{44}) - S^2{}_{34}} \qquad (6.13)$$

Under the terminated to ground condition of ports 3 and 4, S_{33}, S_{44}, and S_{34} are theoretically zero, because the quadrature coupler is in a matched condition. So, the equation (6.13) can be simplified to equation (6.14).

$$S'_{12} \simeq S_{12} - S_{13}S_{23} - S_{14}S_{24} \qquad (6.14)$$

$$S'_{12} \simeq S_{12} \qquad (6.15)$$

Again, the equation can be simplified to the equation (6.15), because ports 3 and 4 ports are almost shorted to ground, so that the transmission from the ports are nearly zero. Therefore, the signal path of quadrature coupler can be achieved under the terminated two port condition.

6.2.2 Triple-mode operation

To enhance efficiency at a lower power level, this work employs a triple-power mode, shown in Figure 6.2. In the high power (HP) mode, the two paths of the cascaded PAs (DS_1, DS_2, PA_1 and PA_2) are activated, so the PA operates as a balanced PA topology. The function of the output quadrature coupler is to combine output power with the quadrature phase difference. In the middle power (MP) mode, one of the driver and power stages (DS_1, PS_1) are deactivated so that the unnecessary bias current consumption of DS_1 and PS_1 is saved while the peak output power level is optimized. For the low power (LP) mode, the switched quadrature coupler using the isolation port is

incorporated by an additional signal path. Only one driver stage (DS_2) is activated while the other stages are kept in the off-state. The LP mode signal path includes RF switches, a matching network of the LP mode, and a quadrature coupler. Depending on the mode of operation, the RF switches are configured differently, shown in Figure 6.4 (a), (b) and (c). In the HP mode, switch 1 (SW_1) is turned off, which disconnects the output of the driver stage from the isolation port, and switch 2 (SW_2) is turned on, which achieves 50 ohm termination at the isolation port of the quadrature coupler. In the MP mode, SW_1 is and SW_2 are turned off to disconnect the path to the 50 ohm termination and to provide high enough impedance of the isolation port. In the LP mode, SW_1 is turned on, which connects the path from the output of the driver stage to the RF output port through the isolation port.

In the proposed PA design, the LP mode is utilized by using the isolation port while terminating the through port and the coupled port of the quadrature coupler, as presented in the section 6.2.1. To operate the isolation port of the quadrature coupler as a signal path, the quadrature coupler should satisfy the condition of $|\Gamma|=1$ at the idle ports connected to the end of the output matching networks. The detail explanation of output matching network will be followed. The MP mode also utilized the turning mechanism that optimizes the performance of the quadrature coupler. When one of the PAs turned off, (i.e., one port is terminated), the quadrature coupler has non-optimal operation for MP mode. However, as the impedance of isolation port increases, the operation of quadrature coupler can be optimized. Figure 6.5 shows the simulated quadrature coupler operations when the through port is terminated. With the 50-ohm termination of the isolation port, the quadrature coupler has -3.42 dB of the insertion loss S_{41}, -6.24 dB of

the return loss S_{11}, and -6.3 dB of the insertion loss S_{21}. As the impedance of the isolation port increases as shown in Figure 6.5, the S_{41} can be less than -1-dB with improving S_{11} and S_{21}, so that the quadrature coupler can provide better performances for the MP mode of the PA. The optimization of quadrature coupler for MP mode is theoretically the same as the LP mode operation, which utilizing signal path from the other two ports. In the proposed PA, SW_2 is turned off to provide large impedance of the isolation port. The load impedance seen by PA also has less deviation from the optimal load impedance. When the through port is turned off, the impedance of the coupled port changes from 50 Ω to 153 Ω. Through the output matching network, the load impedance seen by the activated PA is moved to 3.8 + j2.0 Ω, which is large deviation from the optimal impedance of 11 + j4.9 Ω. By providing high impedance of the ISO port in the MP mode, the impedance of the CPL port is decreased from 153 Ω to 81 Ω, resulting in the load impedance seen by the PA of 7.6 + j2.9 Ω that is less deviation from the optimal impedance. Therefore, the manipulation of the quadrature coupler with switched control for MP mode achieved the reduction of the S_{41} of quadrature coupler as well as less deviation of the load impedance seen by the PA, which led to improved efficiency of MP mode.

Quadrature Coupler

PS 1 Output *50 Ohm*

PS 2 Output *50 Ohm*

DS 2 Output

RF$_{OUT}$ *50 Ohm*

SW_2

SW_1

50 Ohm

(a)

Quadrature Coupler

PS 1 Output $|\Gamma|=1$

PS 2 Output *50 Ohm*

DS 2 Output

RF$_{OUT}$ *50 Ohm*

SW_2

SW_1

50 Ohm

(b)

(c)
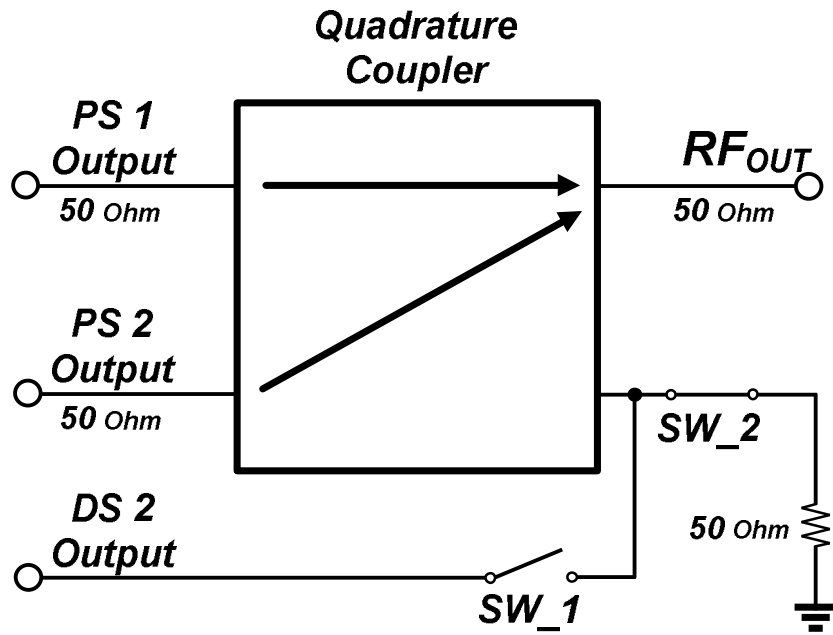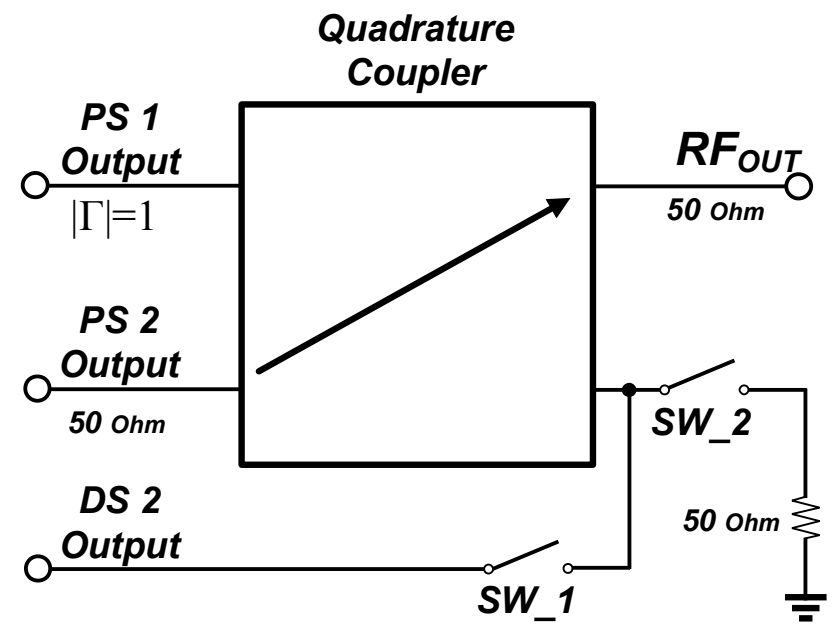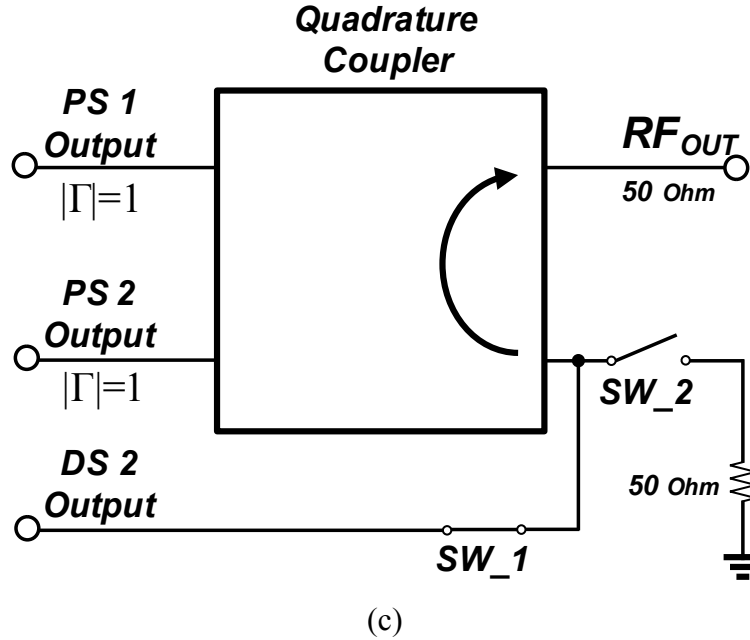
Figure 6.4. Switched quadrature coupler operations (a) High power mode. (b) Middle power mode. (c) Low power mode.
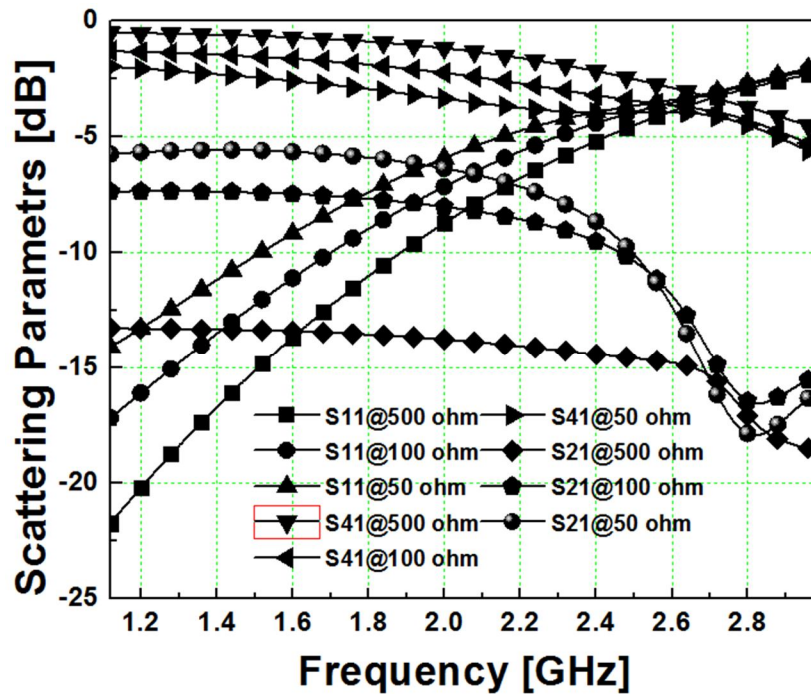
Figure 6.5. The quadrature coupler operation depending on the impedance of ISO port when the THRU port is terminated.

6.2.3 Output matching network

To operate the isolation port of the quadrature coupler as a signal path, the quadrature coupler should satisfy the condition of $|\Gamma|=1$ at the idle ports connected to the end of the output matching networks. In the proposed PA design, the output matching network is incorporated so that the impedance is sufficiently small (short), satisfying the $|\Gamma|=1$ condition from the quadrature coupler in the LP mode, while the output matching network provides necessary load-pull impedance from the PA output side in the HP mode. In the LP mode, when the power stages of the balanced PA are turned off, the impedance of the drain node, which includes parasitic capacitances of the common-gate (CG) device in the cascode configuration, operates as a shunt capacitor. By employing the optimized output matching network consisting of a series inductor, a shunt capacitor, and a bond wire inductor, as shown in Figure. 6.6, in the LP mode, the impedance looking back from the idle port of the coupler is transformed to $1.83+j2.6\ \Omega\ [Z_{L2}]$, which is small enough to be considered a short termination.
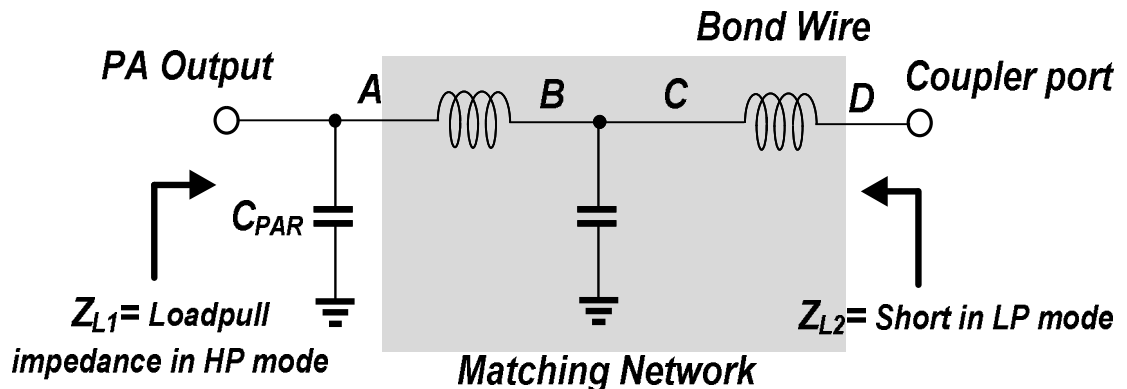
Figure 6.6. PA output matching network.

The impedance transitions of both the HP and LP modes are shown in Figure 6.7. By satisfying the condition of |Γ|=1, the quadrature coupler created a signal path from the isolation port to the output port without disturbing of the PA performance of the LP mode except for the insertion loss. In the HP mode, the output matching network transforms 50 ohm to the optimal load-pull impedance [Z_{L1}]. Thus, the output matching network provides the required impedance for optimal performance in the LP and HP modes, simultaneously.
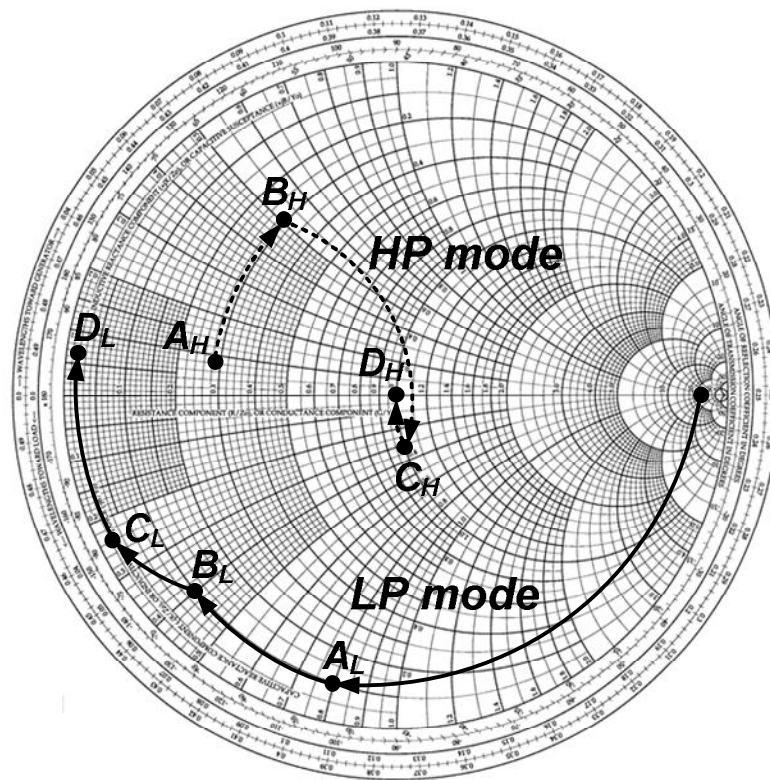
Figure 6.7. Impedance transitions depending on the power mode

6.3 Advantages of balanced topology

The balanced PA has advantages including load immunity, enhanced stability, and improved matching networks, as discussed in the previous work. The load immunity
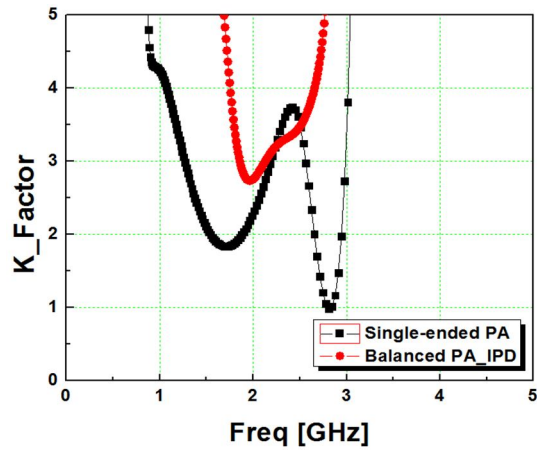
(a)
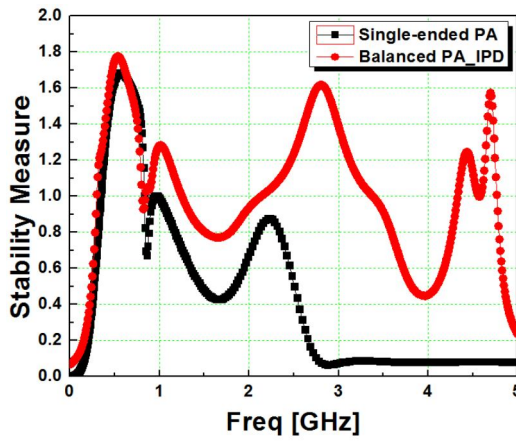
(b)
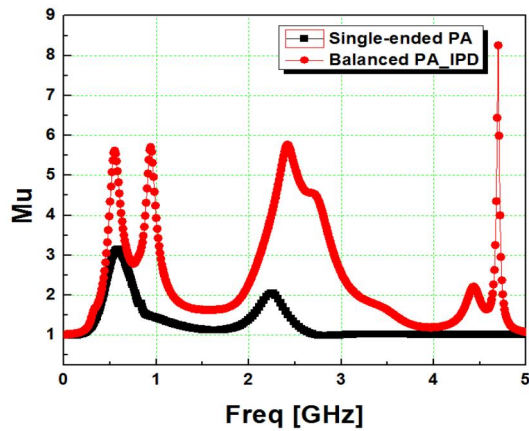
(c)

Figure 6.8. Stability comparison of single-ended PA versus balanced PA using small signal. (a) K factor (b) B factor (c) Mu factor.
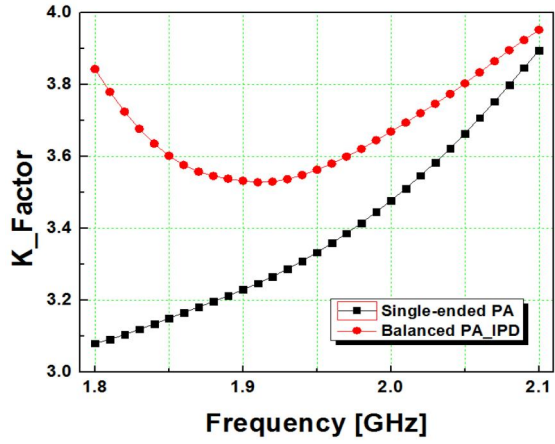
(a)
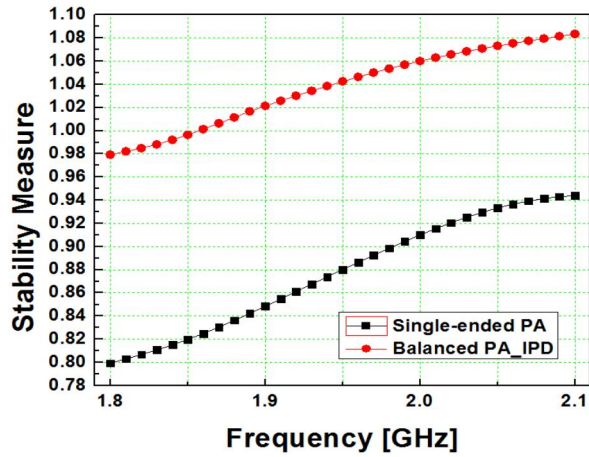
(b)
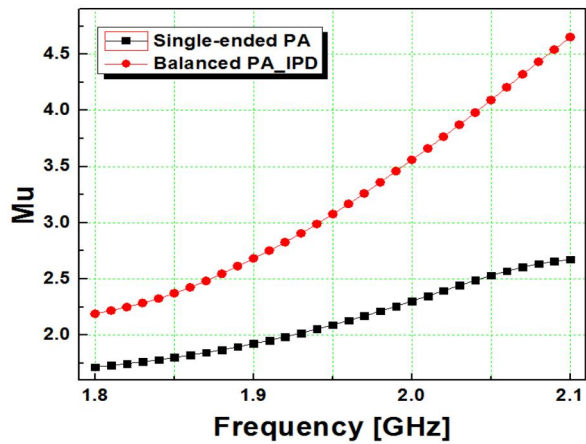
(c)

Figure 6.9. Stability comparison of single-ended PA versus balanced PA using large signal. (a) K factor (b) B factor (c) Mu factor.

characteristics and improved matching networks of balanced PA are demonstrated by the measurement results. The stability enhancement of a balanced PA is also verified compared to the single-ended PA. The simulated stability factor (K), stability measure factor (B), and Mu factor are plotted in Figures 6.8 (a), (b) and (c). As the figures show, the values of all three stability factors of the balanced PA are larger than that of the single-ended PA. With the large signal at the operating frequency, the stability is also improved, as shown in the figure 6.9 (a), (b), and (c).

6.4   Key design blocks

6.4.1 IPD quadrature coupler

For low loss output combining, the transformer-based quadrature coupler is implemented in a silicon IPD process. The coupler has the function of quadrature phase power combining. As shown in Figure 6.10, the cross section of the IPD process presents three metal layers (M1, M2, and M3) and three dielectric layers (SiN layer, Dielectric1, and Dielectric2). The top metal M3 layer, comprised of thick copper, has a 10 um thickness for a high-quality factor of a passive component, and it is mainly implemented for the inductor. The M1 and M2 layers have a thickness of 1-μm and 0.6-μm, respectively, and they are implemented to interconnect of metal 3 and to form MIM capacitors. The silicon substrate has a 250-μm thickness and a 5k Ω-cm of resistivity.
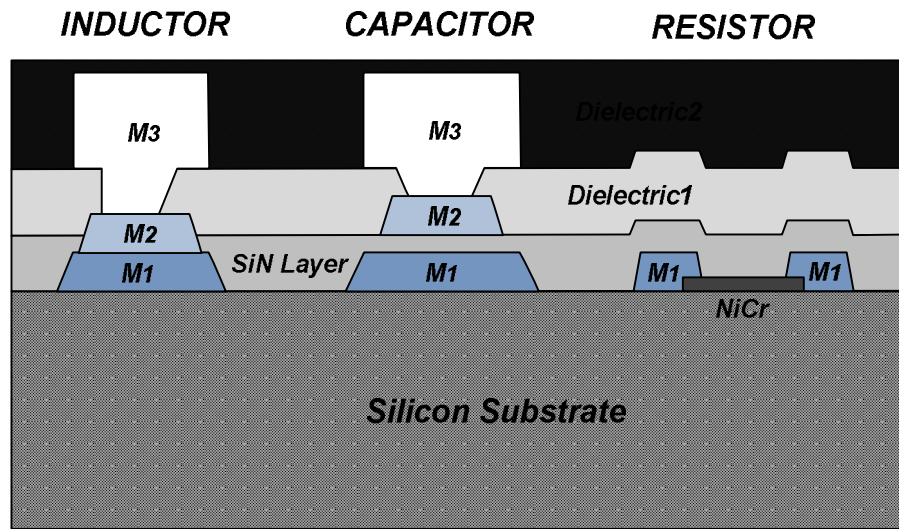
Figure. 6.10. Silicon integrated passive device (IPD) process.

The schematic and the layout diagram of the quadrature coupler are shown in Figures 6.11 (a) and (b). The through and coupled ports of the quadrature coupler are connected to the output matching network of the PA, and their signals are combined to the signal port. The isolation port is connected to the RF switch for maintaining 50 ohm termination.
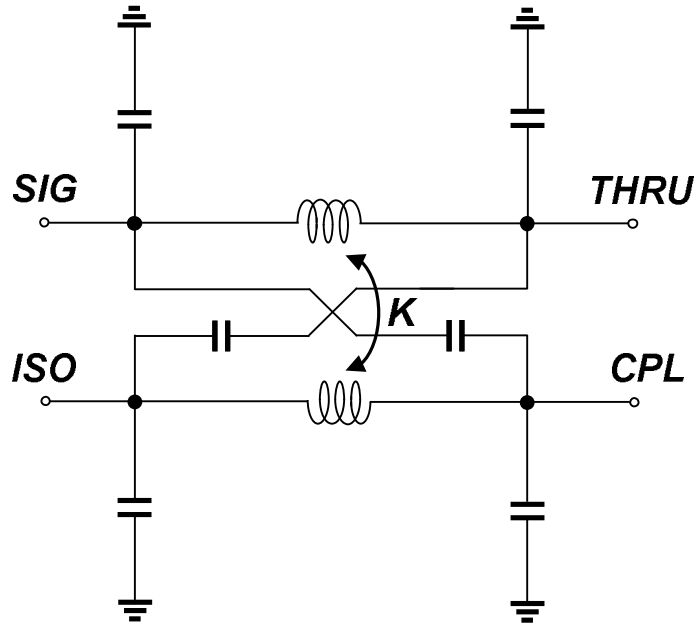
(a)
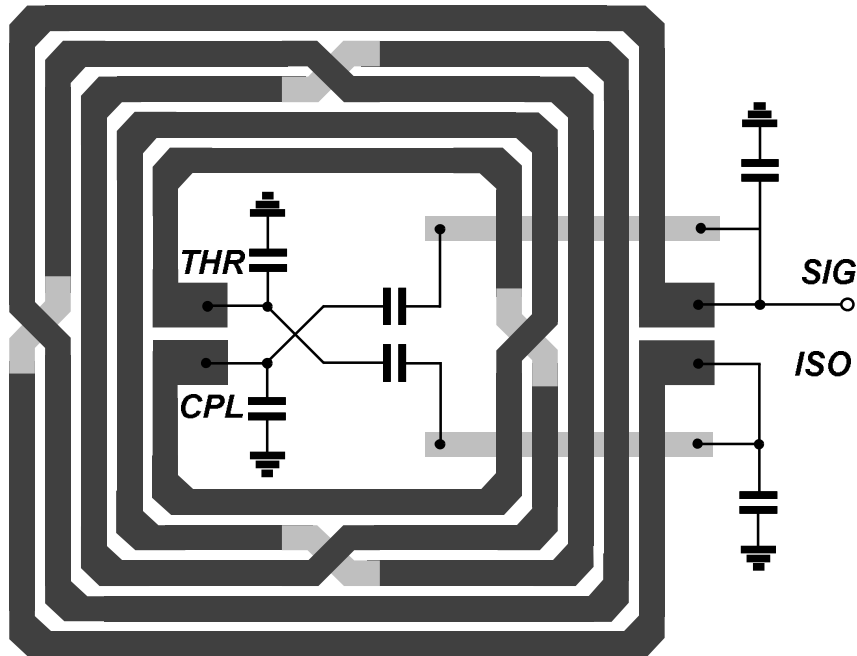
(b)

Figure 6.11. Implementation of the output quadrature coupler (a) Simplified schematic of the designed quadrature coupler. (b) Simplified diagram of the designed quadrature coupler.

Important parameters in this coupler design are the quality factor, the area, and the coupling coefficient. The designed coupler is categorized to the hybrid coupled line coupler, and transformer-based inductive coupling is incorporated in this design [46]. With regard to the quality factor, it is mainly affected by metal line resistance, and both capacitive and magnetic coupling to the substrate [47]. Because of the thick winding metal lines and high substrate resistivity of the IPD process, the quality factor of the inductor in the IPD process can be more than 35, while CMOS technology provides a quality factor of less than 10. The coupling coefficient is aimed to have 0.707 for a 3-dB hybrid coupling coefficient. To obtain this value, several coupler layouts are evaluated with EM simulation. With the same inductor value, the smaller amount of winding metal of the inductor requires a large chip area size, and it has a lower coupling coefficient. However, the number of turns in the inductor is a trade-off with the quality factor of the inductor as a result of longer metal line resistance, as shown in Figure. 6.12. Thus, five metal windings of an inductor with an outer dimension of 750 μm are chosen for the proposed quadrature coupler. The metal line of the inductor has a width of 10μm and spacing of 5μm, and it has a quality factor of 28 at 2GHz with a coupling coefficient of 0.73. Through the EM simulation, the design parameters are carefully determined.
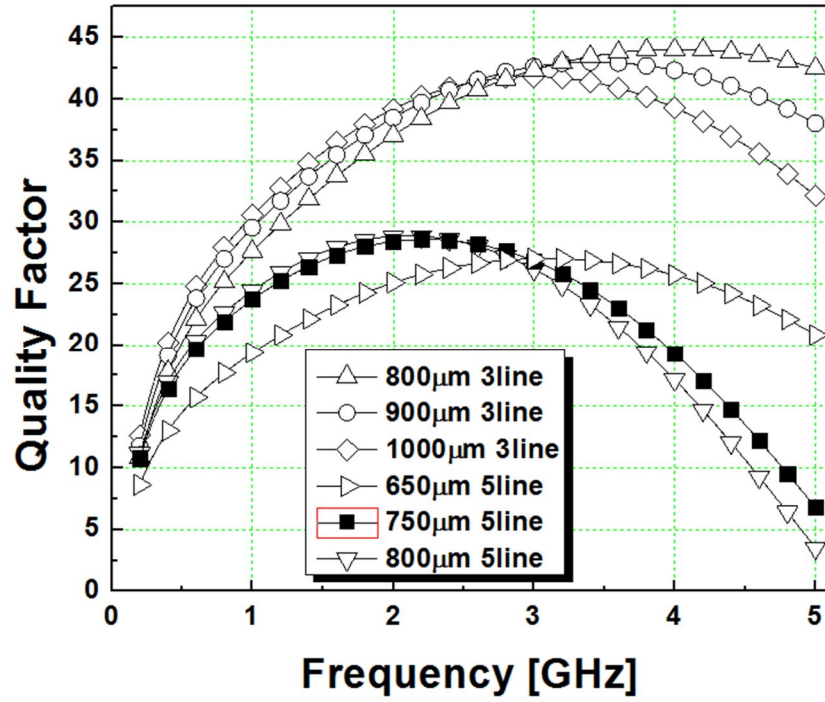
(a)
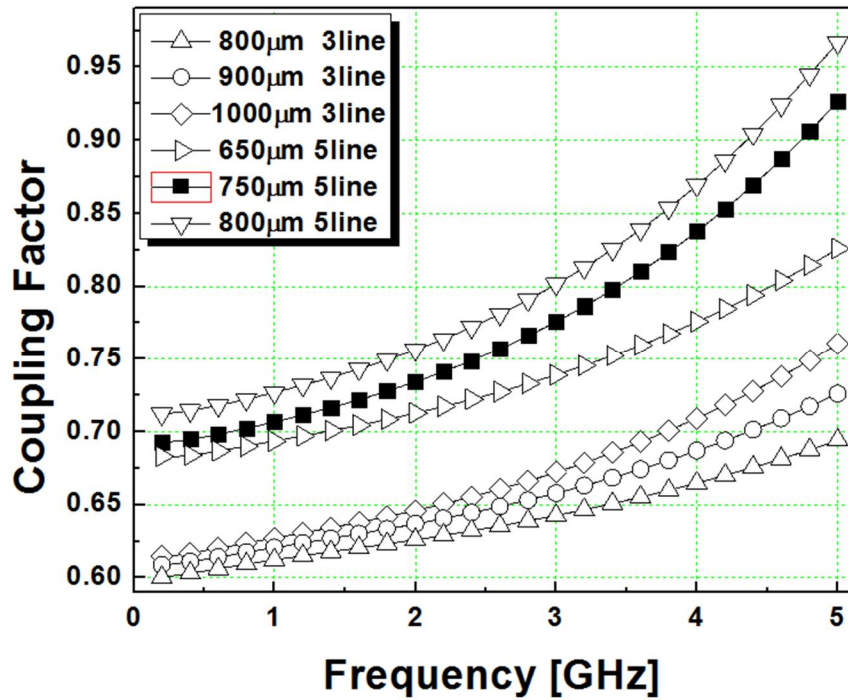
(b)

Figure 6.12. EM simulation results of the IPD quadrature coupler (a) The quality factor. (b) The coupling coefficient.

Figure 6.13 (a) shows the measured performance of the IPD quadrature coupler, which is separately measured with the PA. For the 3-dB combining output power, the insertion loss is calculated in the following equation.

$$IL = 10\log(\frac{0.5}{10^{\frac{Pout[dB]}{10}}})$$ (6.16)

The measurement results of the quadrature coupler show that the insertion loss from the through port to the signal port is

$$IL_{13} = 10\log(\frac{0.5}{0.4236}) = 0.72dB$$ (6.17)

Also, the insertion loss from the coupled port to the signal port is

$$IL_{14} = 10\log(\frac{0.5}{0.417}) = 0.788dB$$ (6.18)

With 50 ohm-terminations of each port, the measured return loss S_{11} was -26-dB, and the isolation S_{12} was -24-dB. In addition, S_{13} and S_{14} are measured as -3.72-dB and -3.79-dB, respectively, at 2GHz. The measured return loss S_{11} was -26-dB, and the isolation S_{12} was -24-dB. The IPD quadrature coupler exhibited a ± 2-degree phase error between 1.1GHz and 2.3GHz and less than a ±1-degree phase error in the operation bandwidth, as shown in Figure 6.13 (b). In the LP mode, the insertion loss from the quadrature coupler was 1.5-dB, doubling the insertion loss of the coupler, because the signal of isolation port was transferred to signal port after the signal was reflected by the through port and the coupled port under the condition of $|\Gamma|=1$.
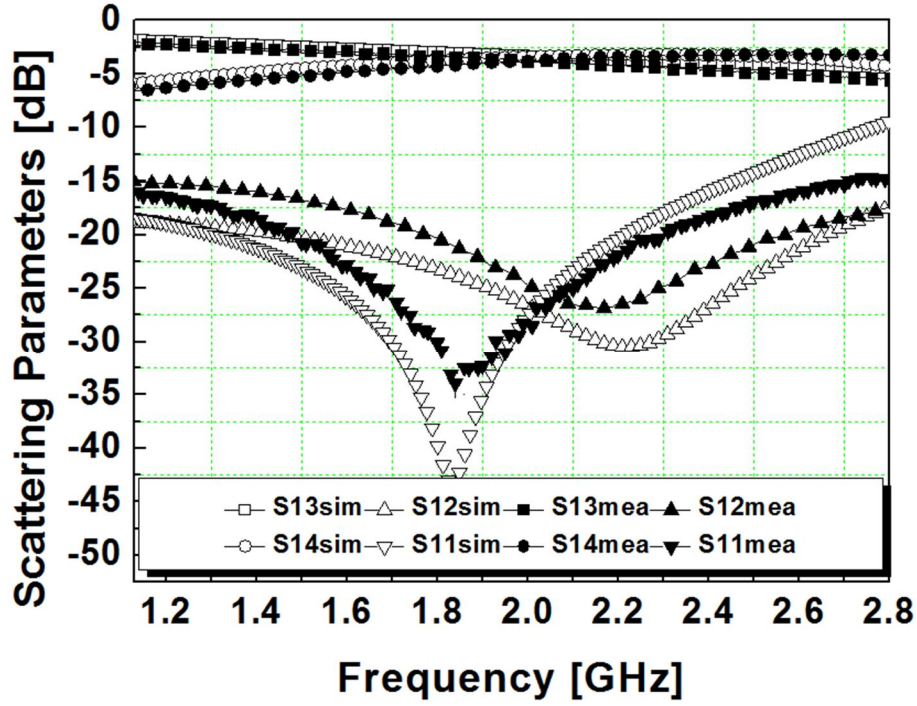
(a)
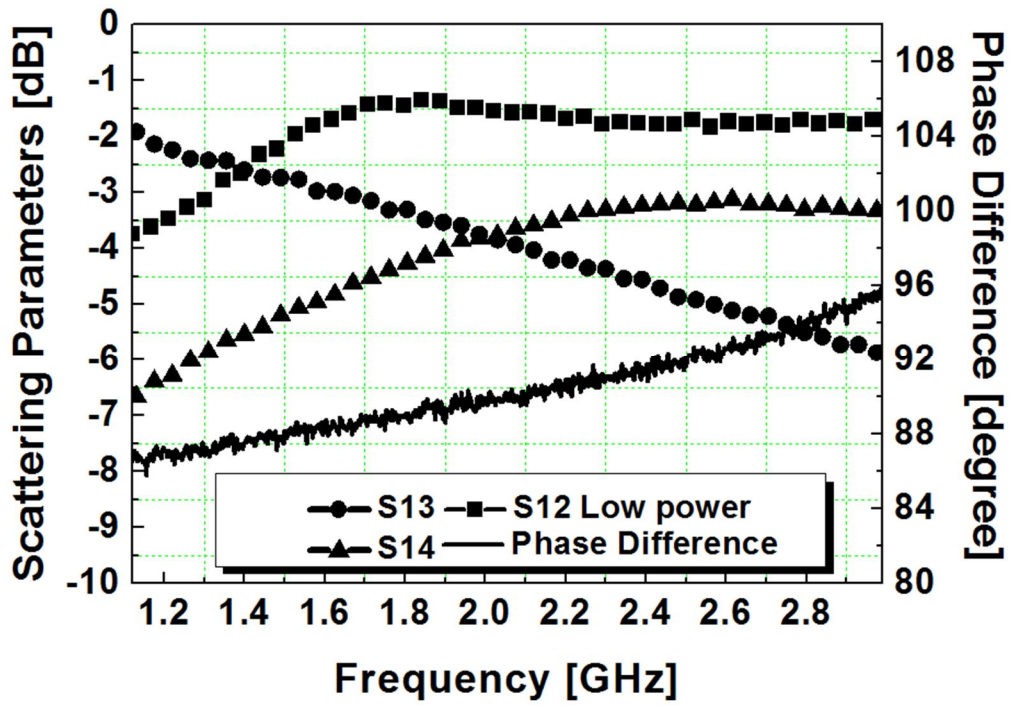
(b)

Figure 6.13. Measurement results of the IPD quadrature coupler.

6.4.2 RF switches

For the power mode change, we implement two RF switches. Switch 1 connects at the drain node of the driver stage amplifier to the matching network for the low power mode. Switch 2 connects at the isolation port of the quadrature coupler so that it provides 50 ohm impedance in the HP mode while providing infinite impedance in the LP mode. Schematics of the switches are shown in Figures 6.14 (a) and (b). In these switch designs, the isolations, the breakdown voltage, and transistor on-resistance are considered important design parameters. For switch 1, the series-shunt configuration, which turns on the shunt transistors while the series transistors are kept off, provides isolation of the switch [48]. Furthermore, employing a three-stacked cascode topology alleviates the reliability issues of the switches by dividing the signal voltage stress equally across each of the off-state transistors. Both switches are utilized in a 0.18-μm CMOS transistor for low on-resistance. In the inter-digitized transistor layout, the metal connections of the drain and the source are in parallel and next to each other, are employed to minimize severe coupling between the drain and the source of the transistors [49].
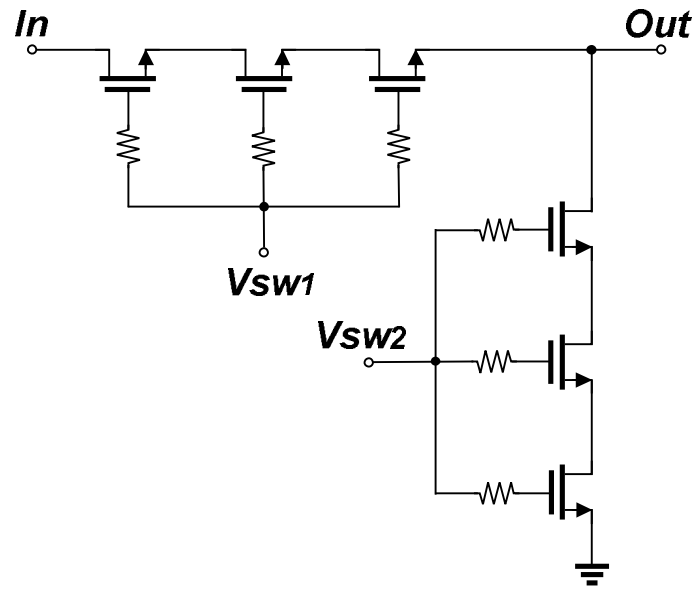
(a)
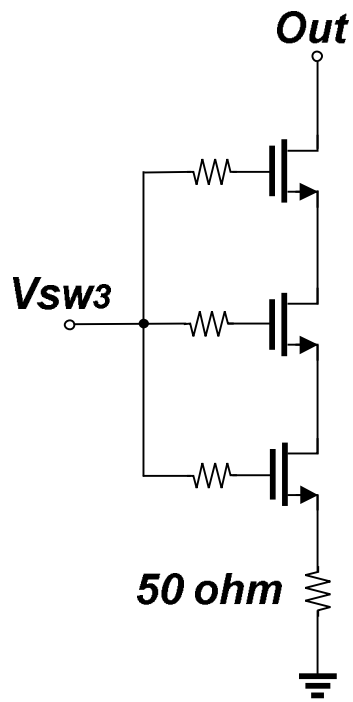
(b)

Figure 6.14. RF switches for the low-power mode operation (a) Schematic of switch 1. (b) Schematic of switch 2.

6.4.3 Amplifier design

The overall schematic diagram of the proposed PA is shown in Figure 6.15. The individual PA consists of input matching, a driver stage, inter-stage matching, a power stage, and output matching. Except for the IPD quadrature coupler, all the circuits are implemented in one CMOS die. The cascode topology is chosen to reduce the voltage stress of the PA, and a 0.4-μm thick gate-oxide transistor, which has the maximum allowable voltage of 7.2 V for gate-oxide breakdown, is used in the common-gate (CG) device in the power stage. To provide sufficient gain, the cascaded two-stage configuration is used. The optimal load impedance for the power stage was obtained from the load-pull simulation as Z_{OPT} = 11.1 + j4.9 Ω, while the optimal load impedance for the driver stage was obtained as Z_{OPT} = 22 + j8.8 Ω. The shunt bondwire inductor of the interstage matching network is aimed to provide tuning of interstage matching after fabrication of the PA. The sensitivity of every bond-wire was simulated for the PA performances, and multiple bond-wires and layout optimization were considered to minimize the bond-wire effects. Fig. 16 (a) shows the drain voltage waveforms at almost saturated output power, which has 7 dBm of input power, and Fig. 16 (b) presents one of the PA's the drain voltage waveforms under 10:1 of VSWR condition. Because of the robust operation of balanced topology, the peak-to-peak voltage swing remains under 11 V, which is allowed to withstand for the cascode topology using a thick-gate oxide transistor.

The PA, biased in a class AB operation to balance both efficiency and linearity, has an operation frequency of 1.95 GHz, the center frequency of the WCDMA Band I transmit. To further improve linearity and stability, the gate nodes of the CG devices in

the driver and the power stage share the same AC ground [50]. EM simulations and parasitic extractions are performed for accurate design parameters.

(a)

(b)
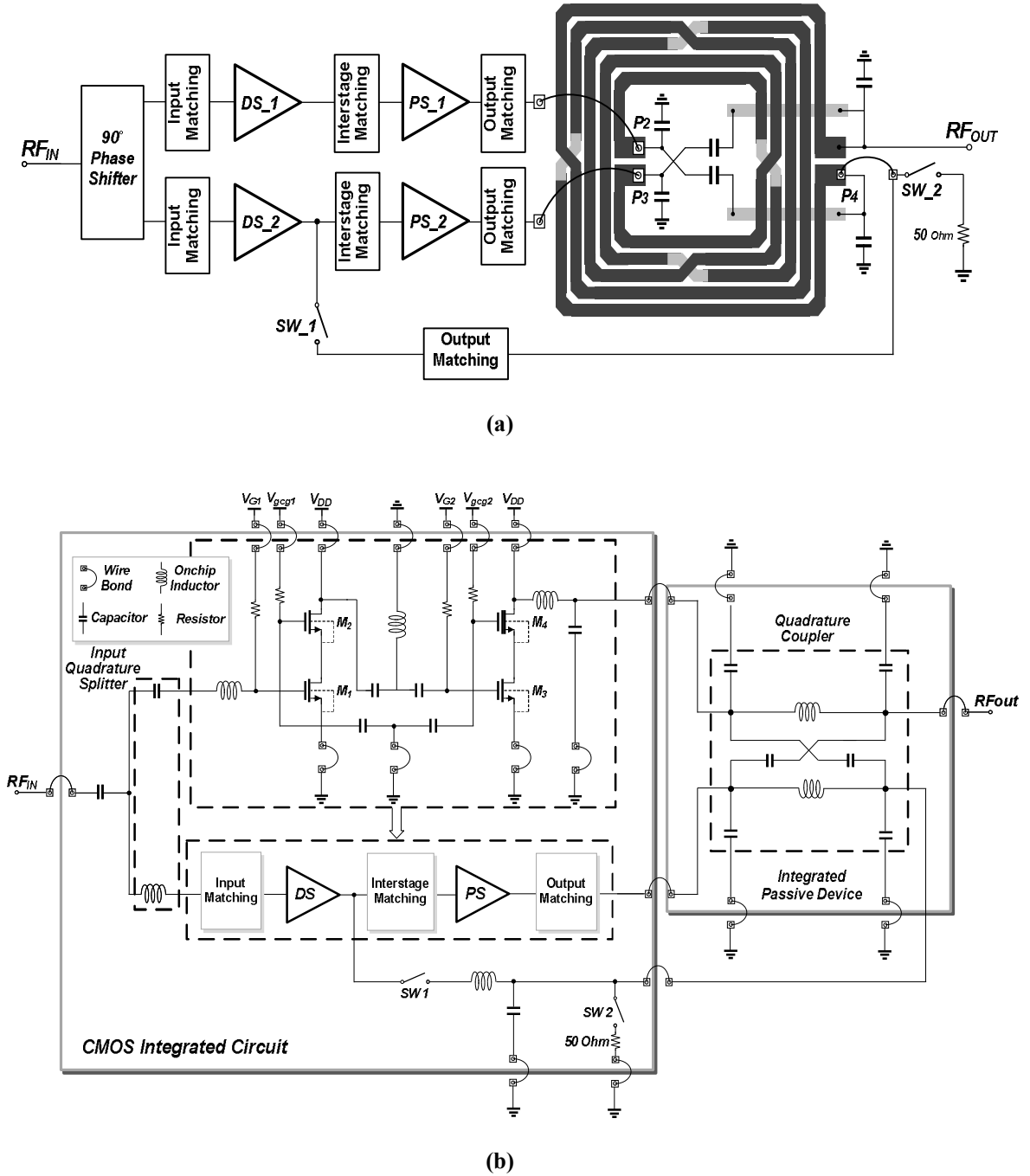
Figure 6.15. Triple-mode balanced PA (a) Simplified block diagram. (b) Overall schematic of the designed PA.
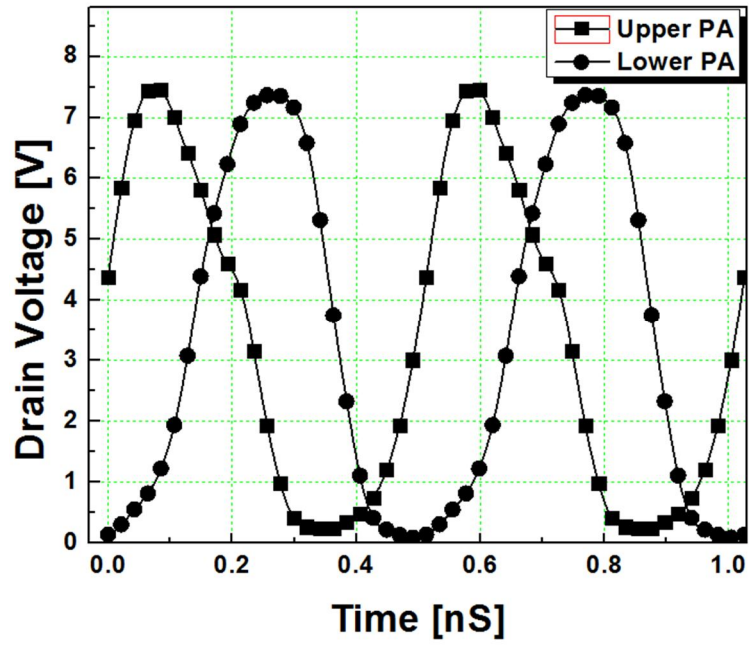
(a)
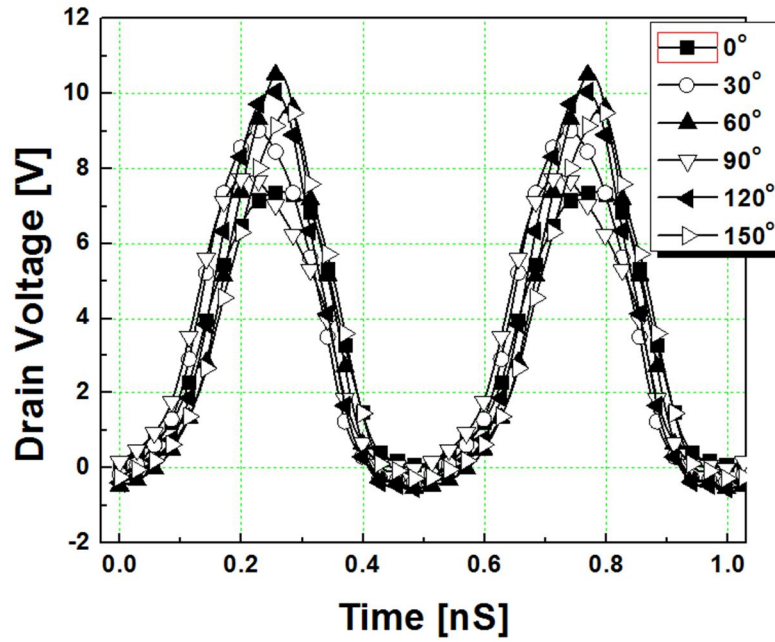
(b)

Fig. 16. Simulated drain voltage waveforms. (a) Both PA's waveform when the input power is 7 dBm. (b) Waveforms of lower path PA under 10:1 of VSWR condition.

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6.5 *Measurement results*

The microphotograph of the proposed PA is shown in Figure 6.17. The PA is fabricated in IBM7RF 0.18-μm CMOS technology and the quadrature coupler in the Telephus IPD process. The CMOS PA and the IPD quadrature coupler occupy areas of 1.25×1.7 mm^2 and of 0.875×0.75 mm^2, respectively, which include bond-wire pads. Chips are mounted on an FR4 printed circuit board (PCB) with 50-ohm input and output terminations for the measurements. PCB and cable losses are de-embedded while wire bonding losses are included in the performance measurements.
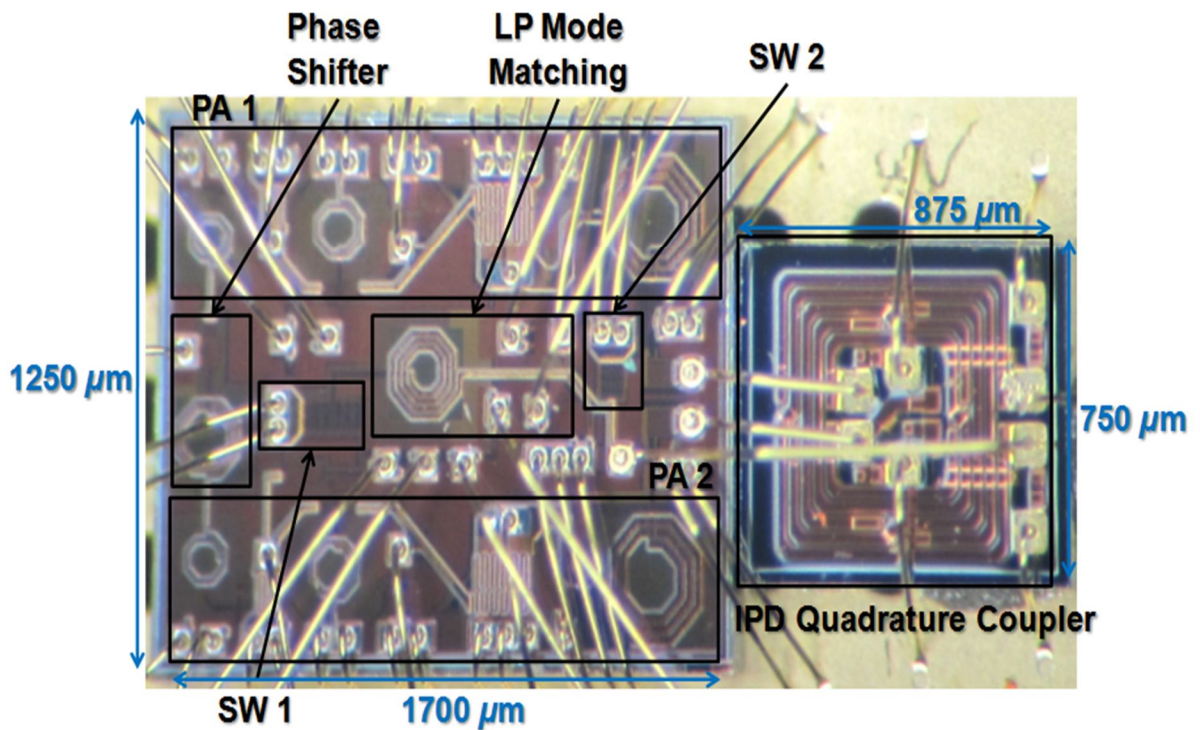
Figure 6.17. Microphotograph of the designed PA and the IPD quadrature coupler.

Small signal measurements were performed on the PA at 3.4-V supply voltage, shown in Figure 6.18. Because of the inherent enhanced input and output matching advantages of the balanced configuration, the input port reflection coefficient, S_{11}, and the output port reflection coefficient, S_{22}, achieve less than -15 dB and -20 dB, respectively, at 2 GHz as shown in Figure 6.18. (a). Compared to S_{11} and S_{22} of the single-ended PA, which are -12 dB and -10 dB, respectively, those of the balanced PA is enhanced, demonstrating the its advantage of balanced topology. In Figure 6.18 (b), the forward gain, S_{21}, has a 3-dB wide gain bandwidth from 1.5 to 2.1 GHz over a 20 dB gain, and the reverse gain, S_{12}, is less than -35 dB of the bandwidth.

Large signal measurements were performed using a 3GPP WCDMA modulated signal. The PAE and the gain of the triple-mode balanced PA are shown in Figure 6.19. The PA achieves a maximum output power of 28.4 dBm with a peak PAE of 40.7%, and a 1dB gain compression point in the HP mode occurs at 27 dBm. The PA also provides maximum output power of 25.4 dBm with a PAE of 35.6% in the MP mode, and maximum output power of 17.6 dBm with a PAE of 19% in the LP mode. By incorporating multiple power modes of operation, the PAE improves from 11.1-% to 17-% at 16 dBm, and more than 5-% over the low output power level. The power mode control is utilized at 22 dBm and 16 dBm of the output power, that is, the mode transition points from the HP mode to the MP mode and from the MP mode to the LP mode, respectively. The PA has a 23 dB small signal gain in the HP mode, 17.8 dB in the MP mode, and 8.7 dB in the LP mode.
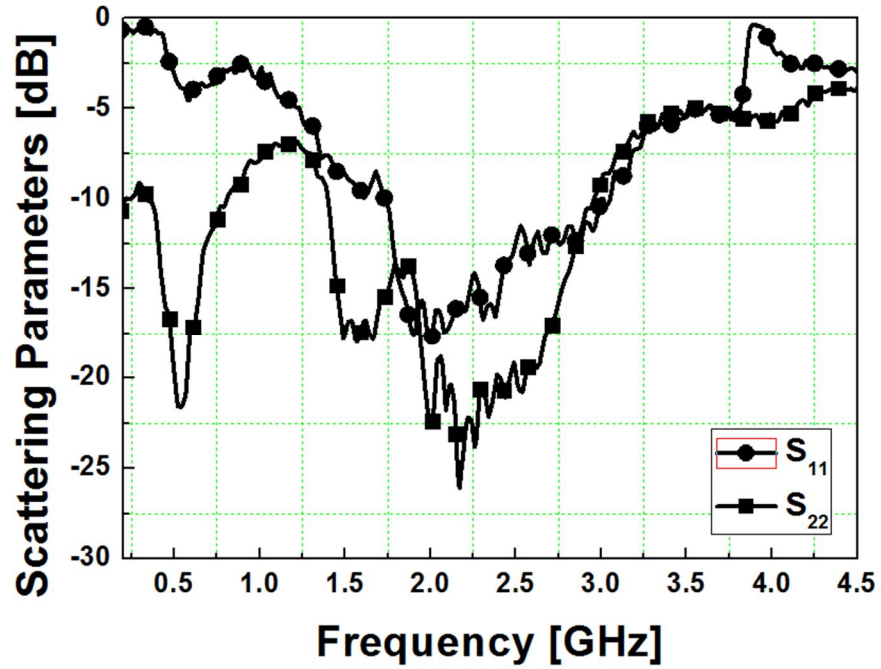
(a)
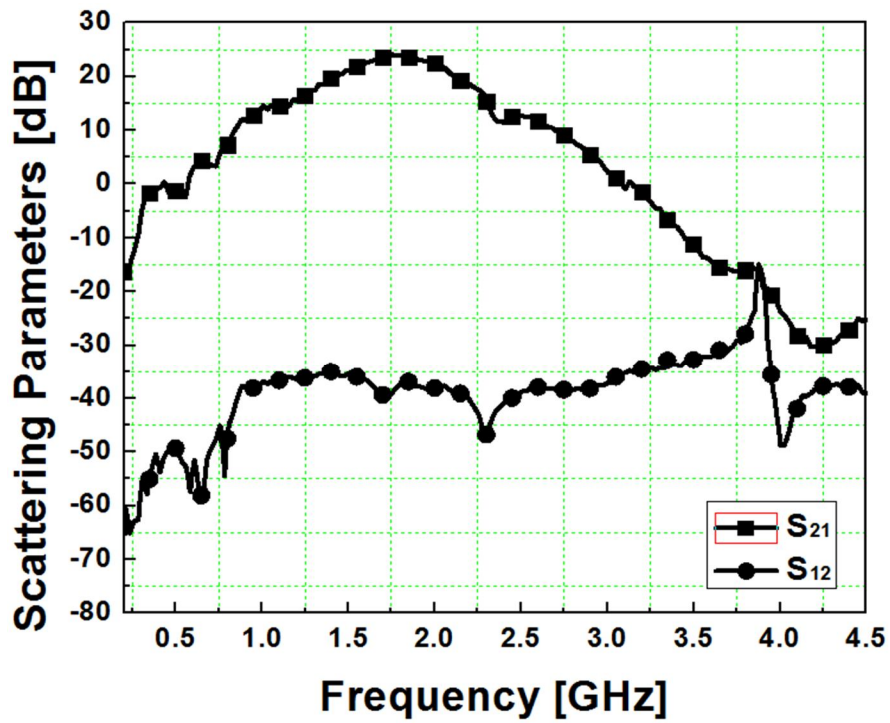
(b)

Figure 6.18. Measured small signal performance of the PA for HP mode. (a) S$_{11}$ and S$_{22}$

(b) S$_{21}$ and S$_{12}$.
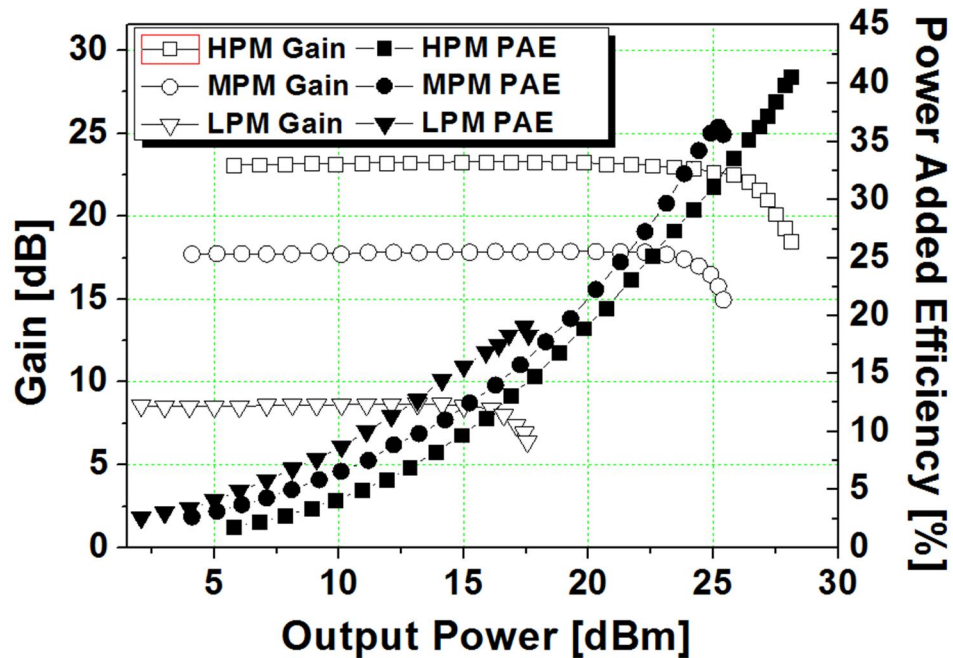
Figure 6.19. Measurement results of the PAE and the gain.

Figure 6.20 shows the current consumptions of the PA depending on the power modes. At maximum output power, the PA consumed 499 mA of DC current, and 392 mA of DC current at 26.6 dBm linear output power. With triple-mode operations, the PA saved 47 mA of quiescent current and 54mA of current at 16 dBm and 47 mA of quiescent current at lower power level.

Figure 6.21 shows the measured adjacent channel leakage ratio (ACLR) at 5 MHz offset using a 3GPP WCDMA modulated signal. The assumed transition points are for -33 dBc of ACLR of the linearity specification for WCDMA applications. Using a 3GPP WCDMA modulated signal, the PA satisfies the linearity specification up to 26.6 dBm output power with a PAE of 35%. Figure 6.22 shows the captured ACLR spectrum at 26.6 dBm output power.
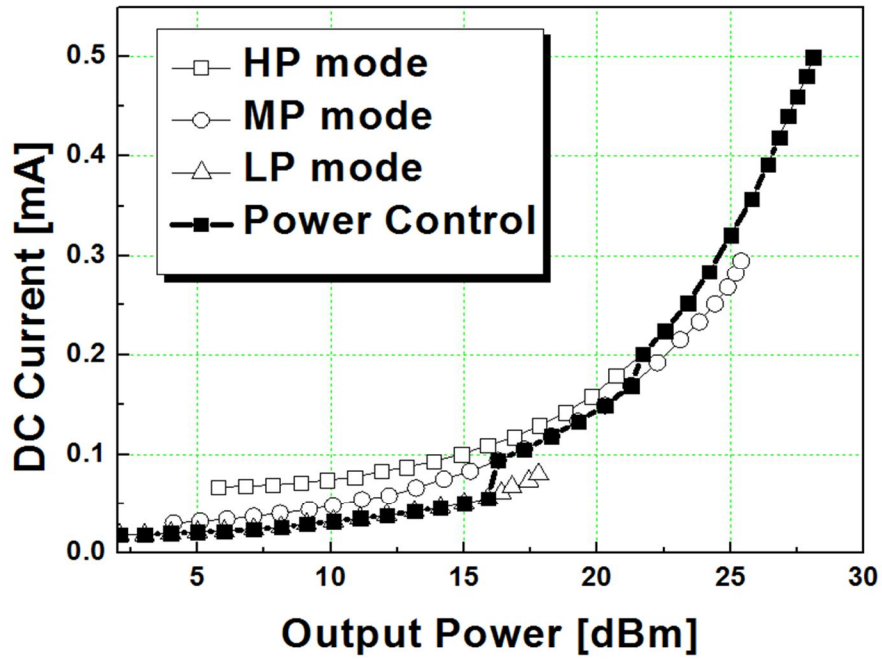
Figure 6.20. Measurement results of current consumption.
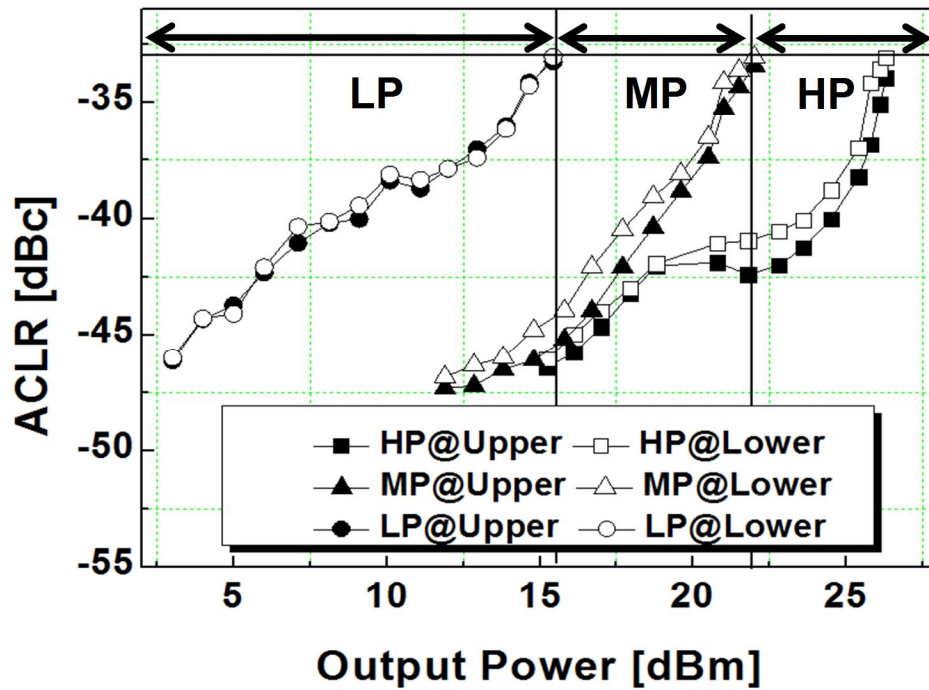
Figure 6.21. Measured results of a 5 MHz offset ACLR.

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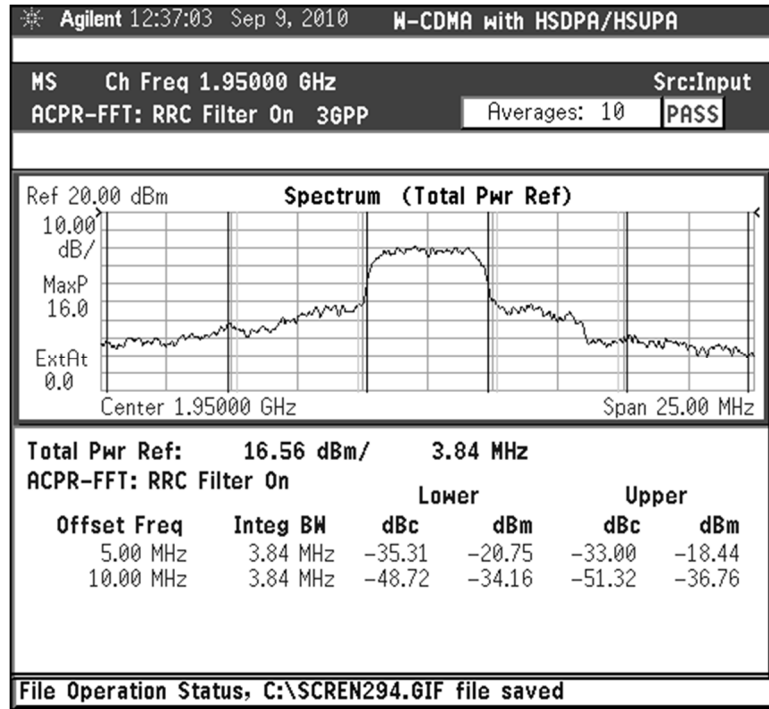
Figure 6.22. Output spectrum with the 3GPP modulated signal at 26.6 dBm.

The captured load insensitivity characteristics of the balanced PA up to 2.5:1 VSWR condition are demonstrated in Figure 6.23 (a) and (b). Compared to a single-ended PA, balanced PA shows much strong load variation immunity than single-ended PA.

The load variation immunity comparison of balanced PA versus single-ended PA with impedance on 2.5:1 of VSWR circle is shown in Figure 6.24. The balanced PA has 1-dB of the gain variation and has less than 43 mA peak-to-peak current variation, while single-ended PA has 6 dB gain variation and 61 mA current variation peak-to-peak current variations. The balanced PA also has less 3.9 dB of ACLR variation while the single ended PA has 15.3 dBc of ACLR variation. From the measurement results, the triple-mode balanced PA also achieved robust operations under variations of external environments.
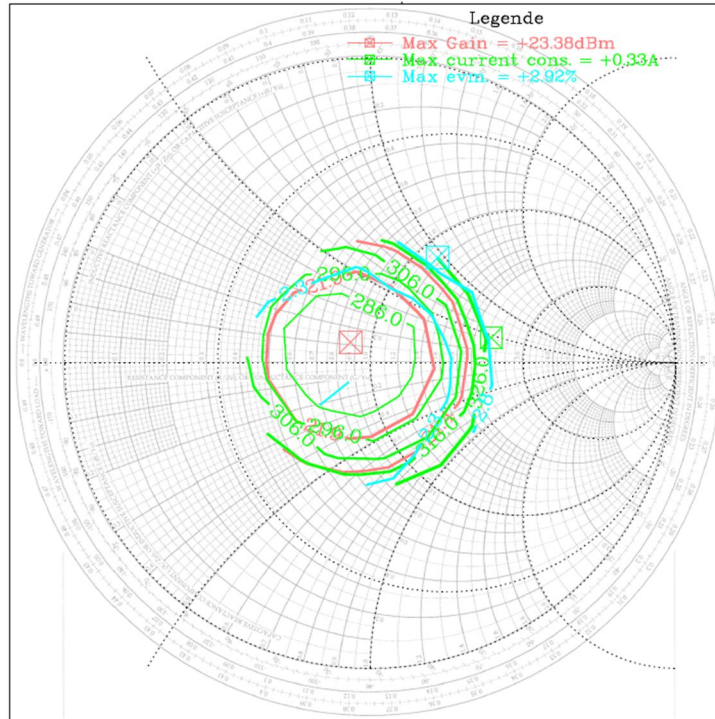
(a)
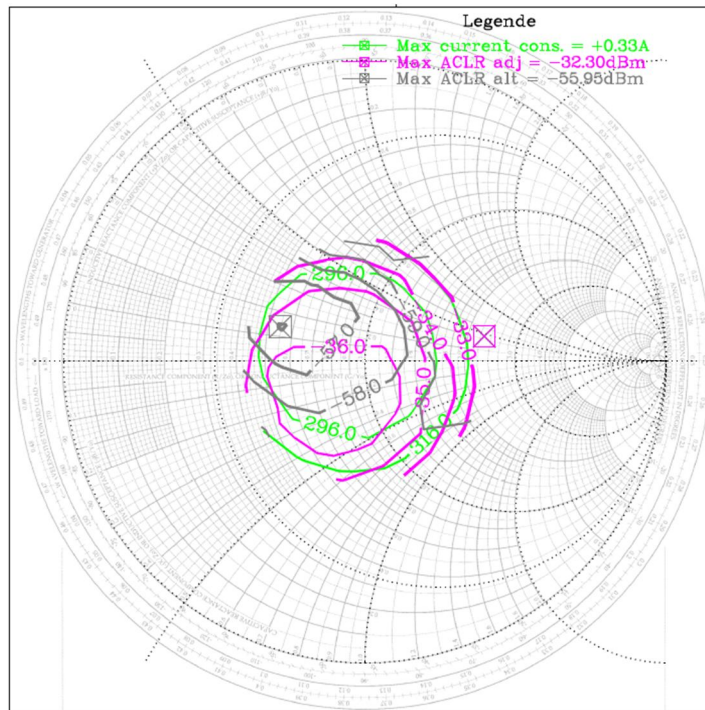
(b)

Figure 6.23. Captured load insensitivity characteristics of balanced PA up to 2.5:1 of VSWR condition. (a) gain, EVM and current. (b) ACLR of 5MHz and 10MHz spacing.
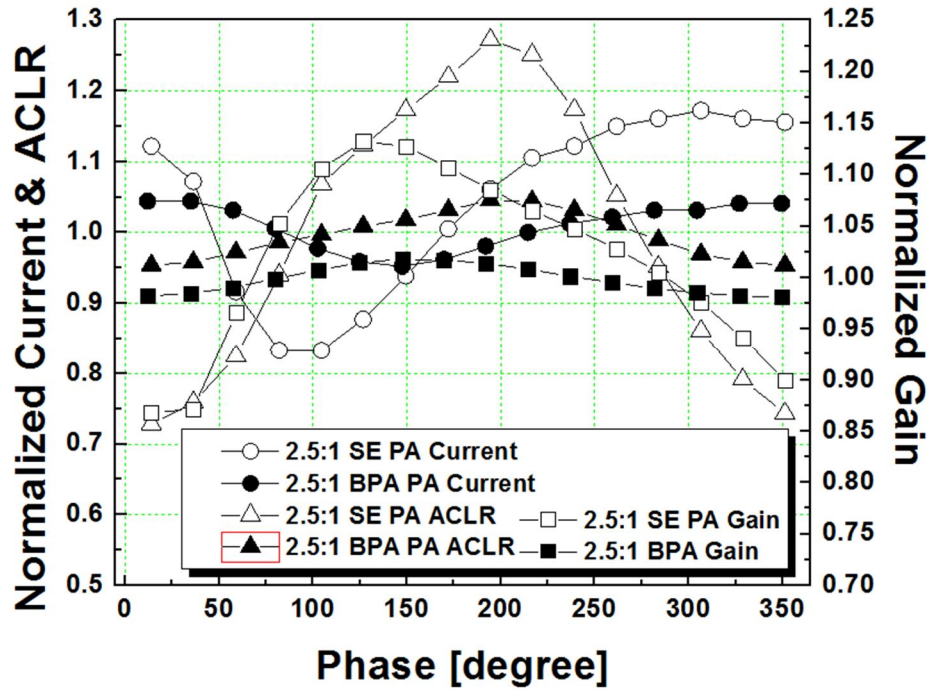
Figure 6.24. Comparison of balanced PA and single-ended PA under 2.5:1 VSWR condition.

6.6 Conclusions

This section described a triple-mode balanced linear PA for WCDMA applications in a 0.18-μm CMOS technology. For average efficiency enhancement, the triple-mode operation that incorporating a switched quadrature coupler is adopted, and a balanced topology to achieve robust load insensitivity is employed. To obtain low loss and a high quality factor of a passive quadrature coupler, the transformer-based silicon IPD process is implemented. With a 3.4 V power supply, the PA transmits linear output power up to 26.6 dBm with 35% of the PAE using a 3GPP WCDMA modulated signal. When driven into saturation, the PA provides 28.4 dBm with 40.7% PAE. The PA achieves 47mA of

quiescent current save and 6% PAE enhancement at 16 dBm with a multi-mode operation. The PA also demonstrates the robust operation under 2.5:1 of VSWR condition, achieving 1-dB of the gain variation and less than 3.9 dB of ACLR variation. This work presents the first demonstration of a triple-mode balanced linear CMOS PA and demonstrates the potential of a highly efficient PA for WCDMA applications using CMOS technology. The performance comparison of state-of-the-art multi-mode linear CMOS PAs is shown in Table 6.

TABLE 6. COMPARISON OF RECENTLY REPORTED <u>MULTI-MODE</u> LINEAR CMOS POWER AMPLIFIERS

Reference	Technology	Frequency [MHz]	V_{BAT} [V]	Size [mm^2]	PAE at -12 dB Back-off (%)	PAE at -6 dB Back-off (%)	PAE at P_{SAT} (%)	$P_{OUT,SAT}$ [dBm]
Liu 08 [34]	CMOS 0.13μm	2400	1.2	2	12	22	32	27
An 09 [33]	CMOS 0.18 μm	2400	3.3	2	8	17	33	31
Chowdhury 09 [51]	CMOS 90 nm	2400	3.3	4.32	6	16	33	30.1
Kim 10 [52]	CMOS 0.18 μm	2100	3.3	1.98	10.5	19.8	35.8	30.7
This work	**CMOS 0.18 μm with IPD technology**	**1950**	**3.4**	**2.12 with 0.66 (IPD)**	**17**	**27**	**40.7**	**28.4**

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Technical contributions

In the rapidly expanding wireless technology market, CMOS PAs, which have attractive advantages of low cost and capable of high integration, have shown considerable potential for implementing a fully-integrated one-chip wireless system. However, the design of highly efficient linear CMOS PA that meets the requirement of advanced communication standards is a challenging task because of inferior performances of CMOS process compared to III-V compound technology.

This dissertation has presented various design aspects, such as reliability, efficiency, linearity, load immunity and losses including those of the substrate and passive components, for CMOS PA.

The main focus of this dissertation and its three contributions are as follows.

- A novel cascode feedback bias technique for improving linearity and reliability of the CMOS PA is developed. The technique utilizes the leakage signals falling on the gate of CG device in cascode topology, and it can easily be applied to a multi-stage cascode configuration (the most common topology in CMOS PA) without demanding components or spaces. The measurement results demonstrated an enhancement of the ACLR by 6-dB without degrading the efficiency of the PA, and the voltage stress on the drain-gate junction is decreased from 4.5-V to 1.9-V. A fully-integrated single chip linear PA in a 0.18-μm CMOS process is implemented with the technique. The

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PA achieved 46.4% of peak PAE at 26 dBm output power and 40% of linear PAE at 23.5 dBm output power.

- A fully-integrated highly efficient balanced linear PA for WCDMA applications was implemented using a 0.18-μm CMOS process. This PA is immune to load variations and has enhanced matching and stability. The first two advantages were demonstrated through measurement, while stability improvement is verified by simulation. This PA achieved 40.4% of peak PAE at 29 dBm output power and 35% of linear output power at 26.4 dBm. By deactivating one of the paths of the balanced PA, dual-mode operation is realized.

- The first triple-mode balanced PA using switched quadrature coupler was developed. The method that uniquely utilizes the isolation port of the quadrature coupler as a signal path was analyzed. In addition, an output matching network that satisfies the $|\Gamma|=1$ condition of the quadrature coupler in the low-power mode and providing the necessary load-pull impedance from the PA output side in the high-power mode was incorporated. For the low losses and a high quality factor of passive output combining, a transformer-based quadrature coupler was implemented using IPD technology. The triple-mode operation enhanced 6% of PAE at 16-dBm and more than 5-% over the back-off output power level. It also saved 47 mA of quiescent current. The measurement results successfully verified the load immunity characteristics and improved matching of the balanced topology.

7.2   Future research directions

Although this research focused on various practical approaches to developing highly efficient RF CMOS PAs in terms of efficiency, linearity, reliability, and load immunity characteristics, these works are still a few steps away from becoming competitive commercial products. The major problem left is lack of 1.5 dB linear output power for WCDMA applications.   The proposed linear CMOS PA design should adopt more advanced design techniques to overcome the inferior performances of CMOS process. Power amplifiers with dynamically changing supply voltage might be the worth effort in the future high efficiency PA research.

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[1]   **H. Jeon**, Y. Park, Y.-Y. Huang, J. Kim, K.-S Lee, C.-H. Lee, and J. S. Kenney, "A triple-mode balanced linear CMOS power amplifier using switched quadrature coupler," *accepted to Solid-State Circuits, IEEE Journal of.*

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