# Next-Generation Microvia and Global Wiring Technologies for SOP

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*Abstract*—As microsystems continue to move toward higher speed and microminiaturization, the demand for interconnection density both on the IC and the package levels increases tremendously. The 2002 ITRS roadmap update identifies the need for sub-100-$\mu$m area array pitch and data rates of 10 Gb/s in the package or board by the year 2010, requiring much finer lines and vias than the current microvias of 50 $\mu$m diameter and lines and spaces of 25 $\mu$m. After a brief description of the future need for high-density substrates, the historical evolution of microvia technologies worldwide is summarized. With the move toward highly integrated and higher performance system-on-a-package (SOP) technology, the demand for microvia wiring density in the package is increasing dramatically requiring new innovations in fine line, ultralow-loss, and ultrathin-film dielectrics. The low-cost needs of this technology are driving research in high throughput and large area processes in dielectric and conductor deposition. The third section of this paper describes in detail some of the key emerging global microvia research and development in the fabrication of microminiaturized, multifunction SOP packages including rapid curing of low-loss dielectric thin films on organic substrates, environmentally friendly high-speed electroless copper plating, ultrafine lines, and spaces down to 5 $\mu$m and low-cost stacked via structures without chemical-mechanical polishing. This paper concludes with a perspective on future directions in dielectrics and conductor materials and processes leading to ultrahigh-density and low-cost microvia technologies for build-up SOP implementation.

*Index Terms*—Conductors, embedded passives, fine lines, global interconnect, high speed, low-loss dielectrics, microvia, PWB, stacked vias, system-in-a-package (SIP), system-on-a-package (SOP), thin film.

## I. INTRODUCTION

**T**HERE is a trend in electronic systems toward miniaturization and higher functionality, driving the demand for greater interconnect density at the IC, package, and board levels. Area array solutions such as flip-chip and wafer level packaging will become increasingly critical for chip to next level interconnections. Table I summarizes the needs for 5 $\mu$m line and space microvia technology identified by the IC roadmaps (2002 ITRS) and electronics product roadmaps (2000 NEMI).

The 2003 ITRS Roadmap calls for organic substrates with less than 100-$\mu$m area array pitch flip and data rates

of 10-15Gb/s in the package or board by the year 2010 [1]. The NEMI 2000 roadmap defines the need for 4–8 layers of 5–10-$\mu$m wiring for future system boards [2]. There is a critical need, therefore, for substrate technology with $>5000$ cm/cm$^2$ wiring density to interconnect I/O density of $>10\,000$/cm$^2$. Signal integrity for 10-15Gb/s data rates requires ultralow loss dielectric materials with loss tangent $\sim 0.001$. Power integrity to support $>200$ W power with $<60$ mV $\Delta$I noise translates to embedded decoupling in the package with $>0.1$ $\mu$F capacitance. Signal delay in global interconnects on ICs will dominate gate delay and thus impact system performance. With the availability of high-density substrates with 3–5 $\mu$m linewidths, system-on-a-package (SOP) provides a unique opportunity for global wiring to be off-loaded to the package for enhanced performance. In contrast, the current leading-edge microvia substrates in the industry provide only 500–1000 cm/cm$^2$ wiring density using epoxy-based materials with high loss and high moisture uptake. Further, low-loss laminate dielectric materials can only be used in 2–5 mil-thick films and, thus, pose wiring density limits. There is a further need to lower the cost, thus driving large area processing solutions such as the proposed SOP to meet ultrahigh-density wiring and ultrahigh-speed signals in a single package with integrated passive and active digital, RF, and optical components.

Some of the latest advances in microvia technology for next-generation SOP packaging are reviewed and discussed in this paper, along with a brief review of the historical evolution of this technology.

## II. HISTORICAL EVOLUTION OF MICROVIA TECHNOLOGIES

The historical evolution and future trend in microvia technology are shown in Fig. 1. Microvia technologies, also called build-up substrates or boards were pioneered at IBM Japan since 1987 to support the needs of area array assembly of ICs. There are two main classes of microvia technologies, thin film and thick film. The first group is based on thin-film technology combined with conventional PWB—cores with through hole plating such as SLC by Japan IBM [3], IBSS/AAP10 by Ibiden [4], DYCOstrate by Dyconex [5], VIL by Japan Victor [6], CLLAVIS by CMK [7] and others. These technologies are further classified by microvia formation processes as follows. SLC and IBSS/AAP10 are photo-via processes. DYCOstrate is by plasma via process and VIL and CLLAVIS are laser via processes. The second group is based on thick film technology combined with conventional through hole plating. These are ALIVH by Matsushita [8] and B$^2$it™ by Toshiba/DTCT/DNP [9]. The ALIVH microvias are formed by laser drilling and

TABLE I
IC AND SYSTEM BOARD ROADMAPS DOCUMENT THE NEED FOR 5 $\mu$m MICROVIA TECHNOLOGY

| Roadmap | System/IC Need | Microvia Substrate Need |
|---|---|---|
| **IC** <br> International Technology Roadmap for Semiconductors (ITRS 2003) [1] | • 0.07$\mu$m IC Gates <br> • 10000 I/Os /cm$^2$ <br> • 50-100 $\mu$m area array pad pitch | • 5-10$\mu$m lines and spaces <br> • 10-15$\mu$m stacked vias <br> • <1$\mu$m/inch warpage |
| | • Minimize Global Wiring Delay | • Transfer from IC to Board <br> • 5$\mu$m lines and spaces |
| **Electronic Systems** <br> National Electronics Manufacturing Initiative (NEMI) Roadmap, 2000 [2] | • High Performance Systems Wiring | • 5-10$\mu$m wiring <br> • 4-8 layers of wiring |
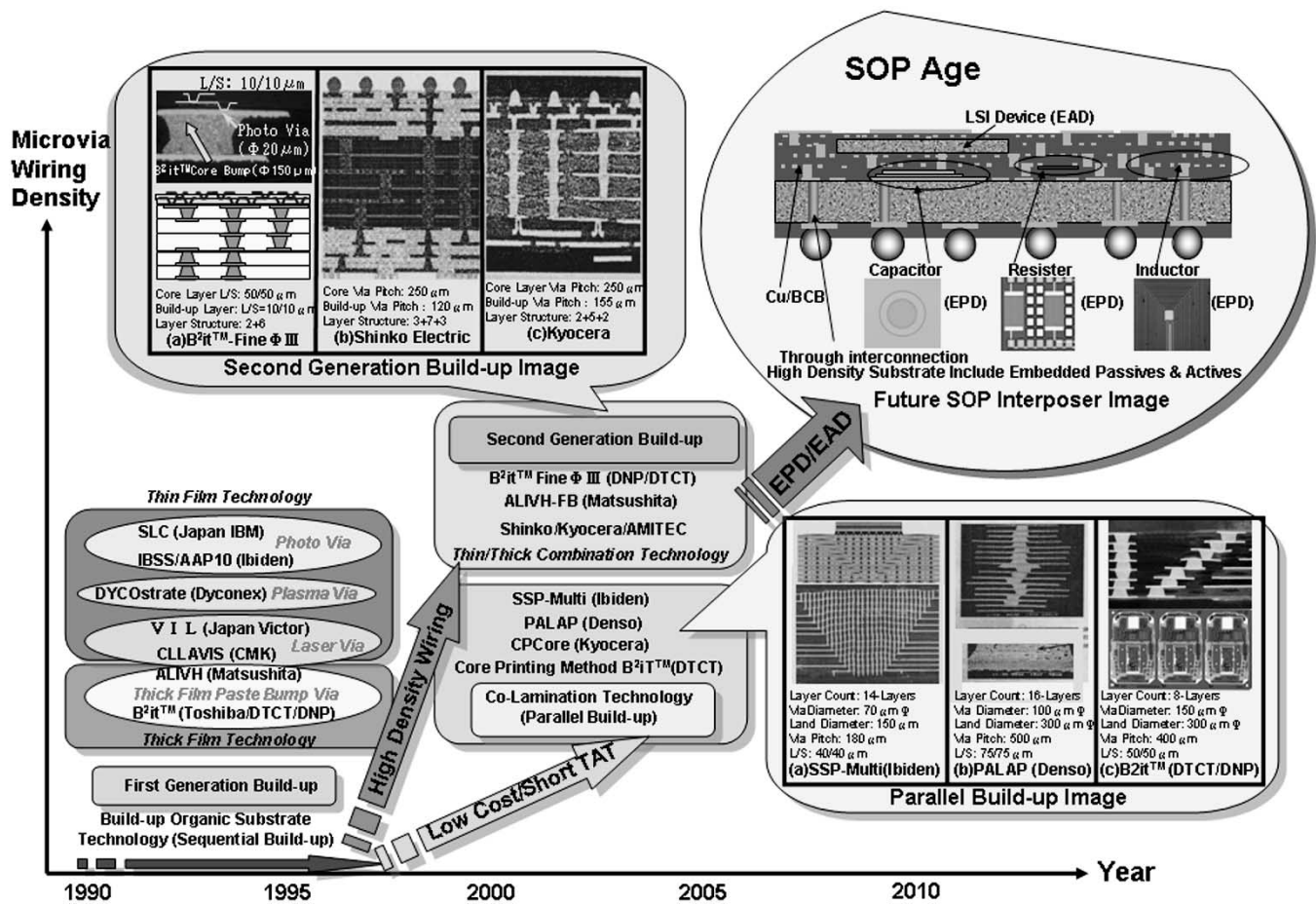


Fig. 1.   Historical progress and current status of microvia technology.

subsequent filling with Cu thick-film paste and the B$^2$it™ is formed by piercing prepreg by Ag conductive thick-film paste.

To meet lower cost and shorter-turn around time requirements, colamination technologies such as SSP-Multi by Ibiden [10], PALAP by Denso [11], CPCore by Kyocera [12], and Core Printing Method of B$^2$it™ [9] by DTCT have been developed since 1999. These technologies are called parallel build-up technologies because each layer is separately built and then laminated in one vacuum colamination press process using advanced manufacturing processes. To further extend the wiring density of these parallel build-up substrates, ultra-high-density multilayer wiring using ultrasmall microvias has been developed using thin-film technologies. Therefore, second-generation build-up substrates are based on a combination of thin- and thick-film technologies, and are being developed aggressively by DNP/DTCT, Shinko, and Kyocera in Japan and AMITEC [13] in Israel.

The SOP technologies are expected to lead packaging developments starting around 2007. To meet the electrical and thermal characteristics of these type of packages, ultrahigh-den-

TABLE II
GENERAL DESIGN RULES OF EACH GENERATION OF MICROVIA TECHNOLOGY

| | First Generation Build-up (Sequential Build-up) | Co-Lamination Technology (Parallel Build-up) | Second Generation Build-up | Future SOP Interposer Substrate |
|---|---|---|---|---|
| Line/Space[μ m] | 75/75-100/100 | 50/50-75/75 | 10/10-30/30 | 3/3-10/10 |
| Via/Land/Pith[μ m] | 150-200/300-400/400-500 | 70-100/170-300/210-300 | 30-50/60-80/100-150 | 10-30/20-50/30-100 |
| Layer Counts | 2+n+2 | 6-20 | 3+n(+3) | 3-5 |
| Conductor Thickness[μ m] | 35,18 | 12,9 | 3-10 | 3-10 |
| Dielectric Thickness[μ m] | 70-100 | 50-100 | 10-15 | 10-15 |
| Dielectric Constant | 4.8 | 3.0-4.8 | 2.7-3.3 | 2.2-3.3 |
| Tanδ | 0.02 | 0.003-0.02 | 0.0008-0.02 | 0.0008-0.008 |

sity interposer substrates are being developed worldwide, including not only with embedded passive devices (EPD) such as capacitors, resistors, and inductors, but also embedded active devices (EAD) within the ultrahigh-density multilayer thin film wiring with low dielectric constant and low dissipation factor materials on high strength core substrates having through microvia interconnections [14]. One such ultramicrovia Si-interposer substrate structure is shown in Fig. 1, as an example of a future SOP package. In general, three kinds of EPD materials are now available: (1) low cure temperature polymer thick-film paste compatible with organic substrates; (2) high-temperature fired inorganic thick-film paste compatible with ceramic substrates; and (3) thin-film passive materials using vacuum processes. In general, better tolerance of passive elements can be obtained with thin film technology. However, most current materials have limitations on values of resistance, capacitance and inductance as well as power dissipation, breakdown voltage, high-frequency characteristics, and so on. Therefore, a new generation of EPD materials based on nano technology is anticipated in the near future. General design rules of the aforementioned microvia technology generations are summarized in Table II. The ultrafine wiring on future interposer substrates will need to be 3–10-μm lines and spaces and electrical modeling will be essential in determining maximum wiring lengths to meet high-speed signals with acceptable conductor loss.

## III. EMERGING MICROVIA RESEARCH AND DEVELOPMENT

The next generation of microvia substrates for fully integrated SOP will have not only extremely high-density wiring, but also interconnections for embedded passive and active components as well as provide global wiring on the package. Innovative solutions are needed to address these challenges in electrical and thermomechanical design, integration of ultralow loss, low- and high-k dielectrics, conductor geometries with submicron precision, and low-cost processes for multilayer stacked via interconnects. The following sections review some of the key recent developments in next-generation build-up microvia for SOP substrate at the Packaging Research Center, Georgia Tech.

### A. Electrical and Thermomechanical Design

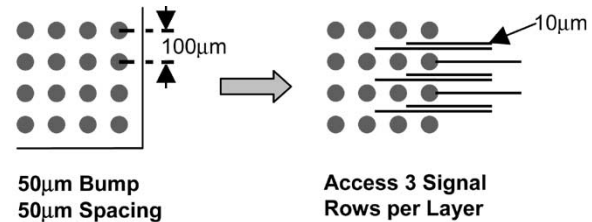Fig. 2 illustrates the escape routing necessary for 100 μm pitch area array packaging using 50 μm bumps and spacing.



Fig. 2. Challenges in routing 100-μm pitch package.
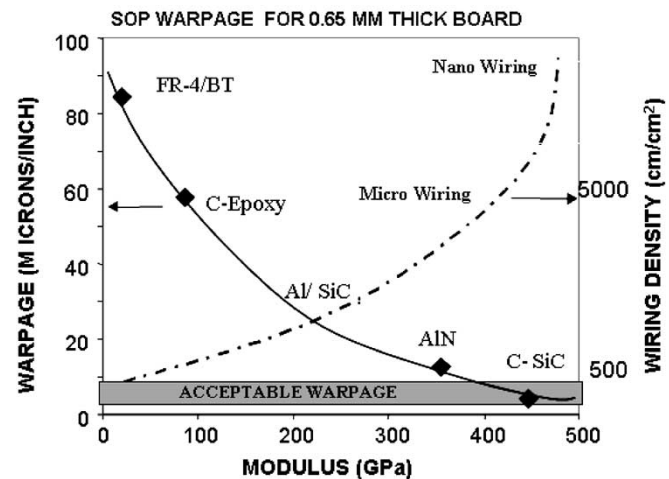


Fig. 3. Effect of substrate modulus on warpage.

For area array pitch of 100 μm and lower, multilayer wiring up to 10 signal layers with 10 μm lines and spaces is necessary. The design of 50 Ω impedance microstrip transmission lines for such fine conductor geometries requires low-loss dielectric thin films in the thickness range of 10–15 μm. Signal speeds in the multiple-GHz range in the package imposes submicron tolerances on conductor geometry and dielectric loss below 0.001. Global wiring on chip is typically less than 1 μm width using 1–2 μm dielectric thickness. The resistivity and conductor loss of such fine lines limits the high-speed performance of global interconnects on large (1.5–2 cm) ICs. The ability to fabricate 50 Ω copper lines in 3–5 μm widths using 5-μm-thick dielectric films will enable the integration of global interconnects in the SOP package substrate for enhanced performance and reducing global wiring delay.

TABLE III
HIGH–PERFORMANCE MICROVIA DIELECTRICS AND KEY PROPERTIES

| Dielectric Material | Dielectric Constant @ 1GHz | Loss Tangent @ 1GHz | Modulus GPa | X,Y CTE ppm/°C | Availability | Via Formation | Via Metallization |
|---|---|---|---|---|---|---|---|
| Polyimide | 2.9-3.5 | 0.002 | 9.8 | 3-20 | Film, Liquid | Excimer Laser, Photo | Sputter Seed |
| BCB | 2.9 | <0.001 | 2.9 | 45-52 | Liquid | Photo, RIE | Sputter Seed |
| LCP | 2.8 | 0.002 | 2.25 | 17 | Laminate | UV Laser, Mech. Drill | Electroless Copper |
| PPE | 2.9 | 0.005 | 3.4 | 16 | RCC | UV, $CO_2$ Laser | Electroless Copper |
| Poly-norbornene | 2.6 | 0.001 | 0.5-1 | 83 | Liquid | Photo, RIE | Sputter Seed |
| Epoxy | 3.5-4.0 | 0.02-0.03 | 1-5 | 40-70 | Film, RCC, Liquid | UV, $CO_2$ Laser, Photo | Electroless Copper |

TABLE IV
EXTENT OF IMIDIZATION ACHIEVED IN POLYIMIDE PI2611 FILMS CURED ON BLANK FR4 SUBSTRATE
BY VFM AND CONVENTIONAL THERMAL FURNACE UNDER DIFFERENT CURE CONDITIONS

| Cure Method | Ramp Rate | Temperature | Hold Time | % Imidization |
|---|---|---|---|---|
| | °C/min | °C | Min | |
| Thermal Cure | 3 | 175 | 60 | 31 |
| | 3 | 175 | 240 | 50 |
| | 3 | 200 | 60 | 73 |
| | 3 | 250 | 60 | 100 |
| VFM | 15 | 175 | 5 | 92 |
| | 15 | 200 | 5 | 100 |

The substrate design process also requires attention to package or board core materials, both to achieve stacked vias without capture pads as well minimize stress on the solder joint between IC and the SOP package. There is increasing acceptance of the need for low CTE package substrates and a number of new materials in the 8–12 ppm/C CTE range are being developed for enhanced reliability of fine pitch area array packages. Examples include Hitachi MCL-E-679F and 679LD laminates with CTE in the 9–12 ppm/C range and organic laminates with Cu-Invar-Cu cores. CTE match between package substrate and the silicon chip has the potential to eliminate the use of expensive underfill process and materials for reliable flip-chip interconnect. Multilayer buildup with layer to layer registration better than 1–5 $\mu$m requires package substrates with exceptional dimensional stability and minimum warpage during processing. Ultrahigh modulus (>450 GPa), large area C-SiC composite substrates are being developed and evaluated for ultrahigh-density buildup of SOP packages [15], [16]. The role of low CTE and high modulus in multilayer thin-film build-up process has been evaluated through extensive thermomechanical modeling [17]. Fig. 3 illustrates the effect of substrate modulus on warpage during high-density wiring fabrication.

### B. Dielectric Materials, Processes, and Properties

There are several critical performance requirements that a polymeric dielectric material must meet for use as a dielectric build-up layer in the microvia fabrication process. For high-frequency mixed-signal SOP packages, a material with a low dielectric constant and a low dielectric loss tangent is needed. Differences in the coefficient of thermal expansion (CTE) of the materials used in the high-density interconnection packages are primary sources of stress. Hence, selection of dielectrics with matched-CTE throughout the package is desirable. Cracking of the dielectric layer can also be minimized by utilizing materials with a high elongation-to-break and a lower modulus. The dielectric material must be thermally stable and not outgas at all temperatures experienced during processing and use. Degradation and solvent loss from the material can lead to delamination and degradation of properties, including adhesion, dielectric properties, and mechanical properties. In addition, the dielectric must possess a processing temperature window that is below the degradation temperature of all materials present in the package. The dielectric material should adhere well to the substrate and metal interconnect present in the microvia board in addition to adhering well to itself. Delamination of the dielectric layer can result in package failure or long-term reliability problems. The dielectric should have a low moisture uptake. Water absorption in the dielectric layer can result in undesirable changes in adhesion, electrical properties, and stress.

*1) Current Dielectric Materials:* Currently, most microvia build-up layers in high-density packages use epoxy-based dielectrics and low-cost organic core substrates (e.g., FR4 epoxy fiberglass boards) [18]. Epoxies have been widely used in the microvia boards due to their excellent adhesion to a variety of substrates, good thermal stability, low processing temperature (<150 °C), and low cost. However, epoxies also have higher dielectric constants (3.5–5.0) than many other polymer
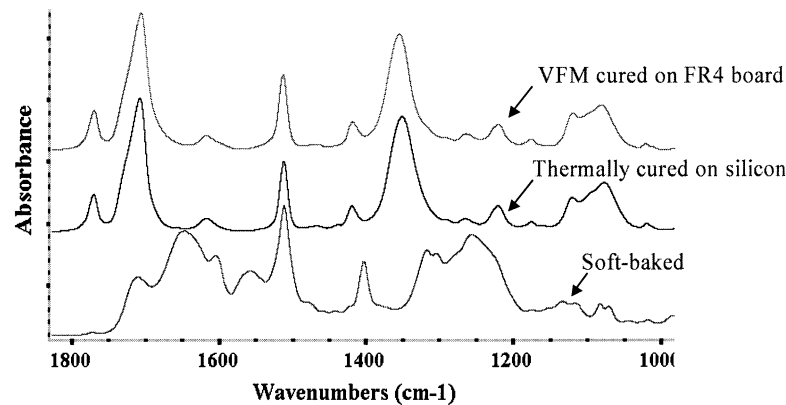
Fig. 4. Infrared spectra of PI2611 Films. (1) Soft-baked. (2) VFM cured on silicon ramped at 3 °C/min to 350 °C and held for 1 h at 350 °C and (3) VFM cured on FR4 substrate, ramped at 15 °C/min to 200 °C and held at 200 °C for 5 min.

dielectrics and have high water uptake (0.3–1.0 wt%). New materials, with lower stress are required to minimize film fracture along via holes in high-density packages. Some high-performance dielectrics like A-PPE from Asahi-Kasei, LCP from Rogers and Gore, and hydrocarbon-ceramic 4000 series from Rogers are gaining acceptance for high-frequency applications. A summary of high-performance build-up dielectric materials used in microvia substrates is shown in Table III along with their key electrical properties and processing methods.

The ideal dielectric material for future high-density packaging should have low loss and dielectric constant at GHz frequencies along with low CTE and high strength, and very low moisture absorption and stability over operating temperatures. Thin films are essential to satisfy impedance requirements for high routing density traces and materials like BCB, polynorbornene and polyimide are good candidates although they have some property limitations. Low-cost large-area manufacturing processes for thin dielectrics will be crucial for low package cost.

*2) Next-Generation Microvia Dielectrics:* Future requirements of higher interconnect density and improved thermomechanical stability necessitates the use of higher performance dielectric materials than epoxies. However, many of the existing higher performance polymers require high thermal processing temperatures which are well above the degradation temperature of traditional low-cost FR-4 substrates. One approach to address this issue is through the development of new low temperature processes. Another approach involves the development of new dielectric chemistries which require low processing temperatures yet possess high performance properties. Examples of advances in both approaches are described later.

Variable frequency microwave (VFM) curing of high-performance polymers has been investigated as a low-temperature curing alternative to conventional heating in a thermal oven [19]–[23]. The unique feature of VFM heating, as compared to conventional heating, is the ability to quickly and repeatedly step through a range of frequencies. This stepping process provides a time-averaged uniformity in the energy distribution throughout the cavity and thereby eliminates the nonuniformities in temperature that occur in single frequency microwave chambers [24]. The VFM technique also allows metals and

conducting materials to be placed in the microwave cavity. By cycling through thousands of frequencies in less than one second, the residence time of any established wave pattern is on the order of microseconds and problems with charge buildup and arcing are eliminated [25].

Tanikella [19] demonstrated the feasibility of rapid curing polyimides on organic substrates using VFM processing. Organic boards, such as FR4 are not significantly heated by microwave energy, but the precursor solutions of polyimide couple the microwave energy efficiently. As a result, full curing of the polyimide precursor is achieved without thermal degradation of the temperature sensitive organic board. For example, Table IV shows the extent of imidization achieved in a particular polyimide film (HD Microsystems PI 2611, whose monomeric system consists of biphenyltetracarboxylic acid and phenylenediamine) processed on an FR-4 board using both conventional heating in a thermal oven and VFM processing.

It can be seen that a higher extent of imidization can be achieved by VFM processing for a much shorter cure time as compared to conventional thermal curing. For example, a 4-h thermal furnace cure at 175 °C gives 50% imidization while a 5-min VFM cure at 200 °C gives an extent of imidization of 92%. Further, a 5-min VFM cure at 200 °C gives 100% imidization without degradation of the epoxy board. Only 73% imidization is achieved in a film cured for 1 h in a conventional thermal furnace at 200 °C and films cured for 1 h at 250 °C achieve 100% imidization, but the FR-4 board is decomposed. Moreover, Fourier transform infrared analysis confirms that there are no differences in chemical structure between a fully imidized system processed using VFM curing at 200 °C compared with a film processed in a conventional thermal oven at 350 °C (see Fig. 4). Hence, it has been demonstrated that a high-performance polymer dielectric can be fully processed on a temperature sensitive organic board, without obtaining board degradation.

In addition to the development of new processing techniques, the formulation of new chemistries may enable the formation of high-performance insulation layers with sufficiently low processing temperatures to prevent degradation of temperature sensitive boards. Photosensitive dielectric materials based on polynorbornene chemistry have been developed with low processing temperatures (<160 °C) as well as superior elec-

trical and thermomechanical properties [26]–[28]. Performance properties include a dielectric constant of 2.5 (measured at 50 MHz), moisture uptake of 0.3 wt%, a tensile modulus of 0.5 GPa and residual stress (measure on a silicon substrate) of less than 4 MPa. This chemistry represents a substantial improvement in performance properties over epoxy-based systems, and still enables low temperature processing on FR-4 boards.

As the demand for lower dielectric constant materials continues, increasing attention has been focused on porous dielectric materials to satisfy future high-density interconnection requirements. The advantage of these materials is clear: no fully densified materials can match the ultralow dielectric constant values that can be obtained when air (i.e., pores) is added to the films. The formation of porous dielectric films and the effect of adding porosity on lowering the dielectric constant have been established [29]–[32]. However, formation of nanoporous films frequently requires high-processing temperatures and, therefore, is incompatible with microvia formation on FR-4 boards. Although the technology is promising for obtaining low dielectric constant goals, new porous dielectric chemistries are required for low temperature processing on organic boards.

*3) New Conductor Metallization Processes:* Metallization of SOP substrates is typically accomplished by electroless and/or electroplating. The simplest and potentially lowest cost metallization process is the "fully additive" process where electroless plating is used to build the full thickness of the metal layer [33]. Electroless plating is a low cost and batch processing technique suited for high-volume manufacturing. However, traditional electroless baths have low deposition rates and use formaldehyde, a carcinogen. Also, the high pH of traditional electroless copper baths can degrade some photoresist. A novel formaldehyde-free electroless copper plating chemistry with low pH ($\sim 9.0$) and high deposition rates (3–4 $\mu$m/h) has been developed to meet the wiring needs of future SOP packages.

Electroless copper plating involves the reduction of $Cu^{2+}$ ions to copper metal and the surface catalyzed oxidation of a reducing agent [34], [35]. The catalytic oxidation of formaldehyde increases with hydroxide concentration and is only effective at pH above 11. Several electroless copper solutions using nonformaldehyde reducing agents have been reported and the process involving hypophosphite is shown in (1) [36]–[41]

$$Cu^{2+} + 2H_2PO_2^- + 2OH^- \rightarrow Cu + 2H_2PO_3^- + H_2. \quad (1)$$
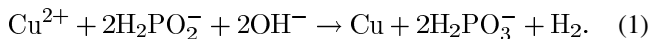
However, the inherent drawback for using hypophosphite as the reducing agent is the weak catalytic activity for the oxidation of hypophosphite on copper. While the initial substrate surface is palladium-activated, once it is coated with copper, the reaction slows because copper is not a catalytic material. One way to compensate for the poor catalytic activity of copper is to add nickel ions to the solution. The codeposited nickel in the copper deposit serves to catalyze the oxidation of hypophosphite, thus increasing the overall deposition rate [42]. Thiourea (tu) and diphenylthiourea (DPTU) have been shown to increase the deposition rate of electroless copper plating solutions that use HEDTA as the complexing agent and sodium hypophosphite as the reducing agent.

TABLE V
COMPOSITION AND OPERATING CONDITIONS OF THE ELECTROLESS COPPER PLATING SOLUTION

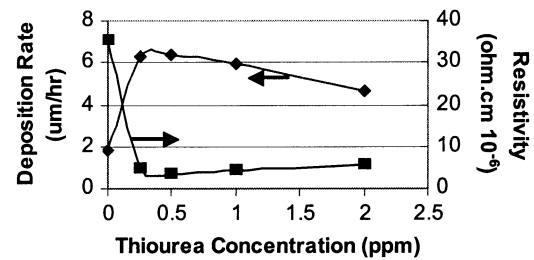| $CuSO_4 \cdot 5H_2O$ | 0.04 M |
|---|---|
| $NaH_2PO_2 \cdot H_2O$ | 0.12 M |
| HEDTA | 0.08 M |
| $H_3BO_3$ | 0.48 M |
| $NiSO_4 \cdot 6H_2O$ | 500 ppm |
| Polyethylene Glycol | 200 ppm |
| pH | 9.3 |
| T(°C) | 70 |



Fig. 5. Effects of the thiourea concentration in the copper plating solution on the deposition rates and resistivity of the electroless copper deposits.
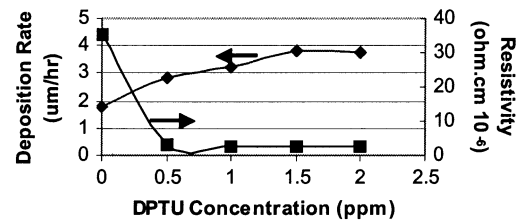


Fig. 6. Effects of the DPTU concentration in the electroless copper plating solution on the deposition rates and resistivity of the copper.

*a) The Effect of tu and DPTU on Deposition Rates:* When only a small amount of tu was added into the electroless copper plating solution (see Table V) with N-(2-hydrox-yethyl)ethylenediaminetriacetic acid trisodium salt hydrate (HEDTA) as the complexing agent and hypophosphite as the reducing agent, the deposition rate of copper plating increased significantly, as shown in Fig. 5. The color of the deposits changed from black in the absence of tu in the solution to semibright at 0.5 ppm tu. In addition, the resistivity of the copper deposits decreased due to changes in the structure of the deposits. Unfortunately, as the tu concentration was increased, the plating rate decreased slightly. When the tu concentration was more than 1.0 ppm, the copper deposit became brittle and appeared black, similar to when there was no tu.

DPTU had a similar beneficial effect on the deposition rate as tu in the electroless copper plating solution. Fig. 6 shows the average deposition rate of the electroless copper plating solution
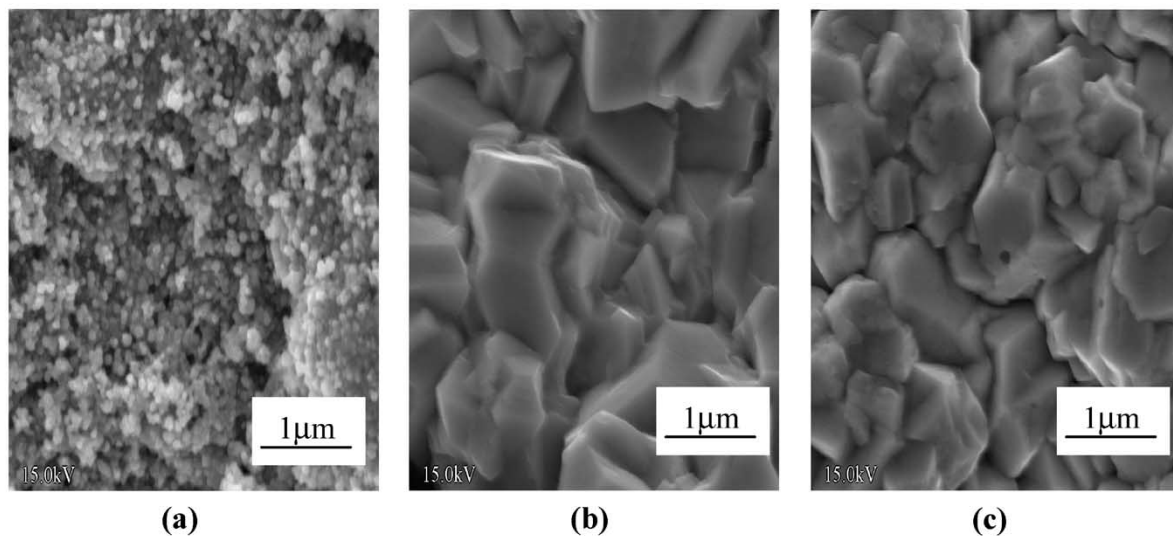
Fig. 7.   Surface morphologies of the copper deposited from (a) basic electroless copper solution. (b) Electroless copper solution containing 0.5 ppm thiourea. (c) Electroless copper solution containing 1.0 ppm DPTU.
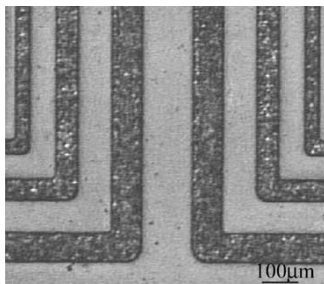


Fig. 8.   Fine lines and spaces on build-up substrate fabricated using fully additive electroless copper plating.
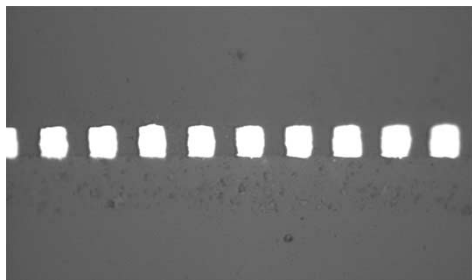


Fig. 10.   An extremely fine structure made by 4 $\mu$m lines on SBU layer.



Fig. 9.   Cross section of 10-$\mu$m lines and spaces on FR-4.
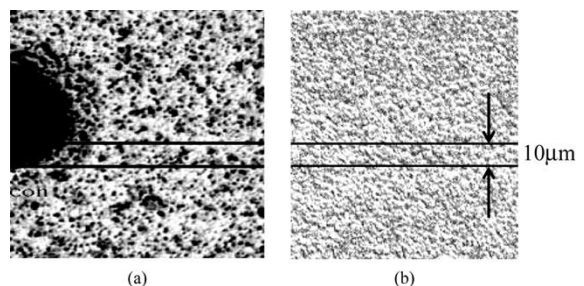


Fig. 11.   Surface roughness profile for SBU epoxy dielectric using (a) permanganate and (b) CF$_4$/O$_2$ plasma.

and resistivity of the deposit as a function of DPTU concentration. Although the deposition rate with DPTU was less than that with tu, the resistivity of the copper deposit was lower and nearly the same as that obtained with formaldehyde-based electroless copper solutions [43].

*b) Surface Morphologies of Copper Deposits:* Fig. 7 shows the surface morphologies of the copper deposits from the electroless solutions with and without additives. The topography of the copper deposited from the hypophosphite electroless copper plating solution was relatively rough with small growth colonies and resulted in higher resistivity. When tu and DPTU were added in the solution, the copper deposits became more uniform and the growth colony size increased.
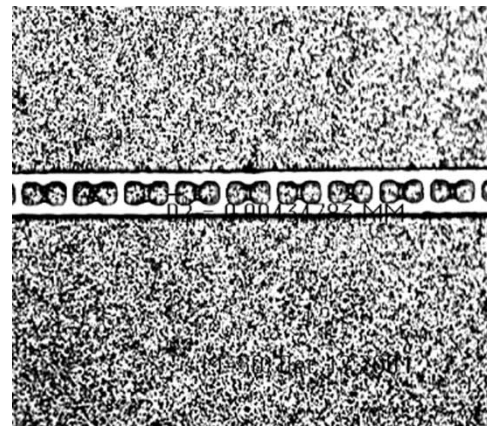
The optimized low pH formaldehyde-free plating chemistry shown in Table V with small additions of thiourea and DPTU was used in a fully additive build-up process on photodefinable epoxy dielectric. The photoresist used was Shipley Eagle NT-90, a negative acting liquid resist with 3–5 $\mu$m resolution. Fig. 8 shows the top view of 25–75 $\mu$m fine lines and spaces fabricated to 10-$\mu$m copper thickness.
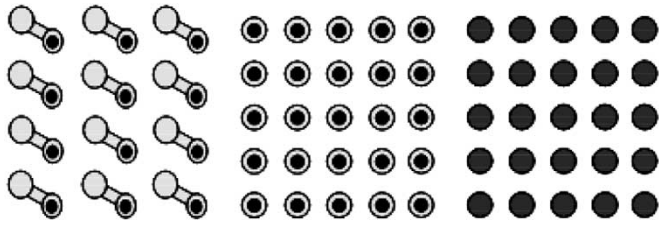
Fig. 12. Today versus tomorrow's PWB pad footprint for area array IC assembly. (a) Today's dog bone pad. (b) Via-in-pad. (c) Tomorrow's nonconformal pad.

### C. Novel Structures for Future Microvia Boards

The typical methodologies used to increase wiring density are (1) reducing the linewidth and line space; (2) increasing the number of layers; and (3) using small capture pads. Additionally, next generation of microvia substrates also require low cost processes. The research at PRC is focused on all of these including (1) ultrafine lines of 3–5 $\mu$m dimensions; and (2) stacked microvias of 10–15 $\mu$m diameter. Precise control of the photolithography process was combined with high-resolution liquid photoresists coated as thin films to achieve copper lines with <5% control of X, Y, and Z dimensions.

Recent research has showed that the above feature sizes are indeed achievable [44]–[46]. A cross-section micrograph of a comb structure having linewidths of 10 $\mu$m and space of 10 $\mu$m on a build-up high-Tg FR-4 substrate is shown in Fig. 9. The metal thickness of the comb is 10 $\mu$m $(\text{Aspect Ratio} = 1.0)$. Fig. 10 illustrates the top view of an extremely fine structure. Here, a 20-$\mu$m-wide and 9 500-$\mu$m-long structure made of 4 $\mu$m copper lines were formed on a build-up epoxy dielectric layer coated on a high Tg FR-4 laminate. Semiadditive metallization using electroless copper thin seed layer and pattern electroplating were used to form the structure on a build-up layer. The thickness of the plated copper was 4 $\mu$m $(\text{Aspect Ratio} = 1.0)$. These structures were obtained by using Shipley Eagle NT-90 liquid photoresist and a chrome on glass photomask.

Surface roughness is a critical factor for both fine line lithography and metallization. Comparisons of typical epoxy dielectric surfaces obtained by permanganate desmear treatment and $CF_4/O_2$ plasma roughening is shown in Fig. 11. Permanganate or other wet etch processes result in a dielectric surface with roughness of the order of 2–3 $\mu$m depth and large pits, as seen in Fig. 10(a). Multilayer thin-film wiring on such a surface would result in latent defects in the traces and inconsistent dielectric separation between metal layers. The plasma treatment on the other hand produces a fairly uniform roughness on the surface that is typically <1 $\mu$m deep. The plasma process has been successfully implemented to fabricate the fine lines shown in Figs. 8 and 9. Additionally, a planar surface is required for fabrication of fine lines on large substrates due to depth of field and contact limitations during lithography. The adhesion of the photoresist during metallization and copper to dielectric peel strength are also lower for finer geometries due to the smaller contact area.

An additional barrier to achieving the target wiring density is the size of capture pads. The via grid and pitch have to be of similar dimensions as the I/O pads. Via and pad geometries have
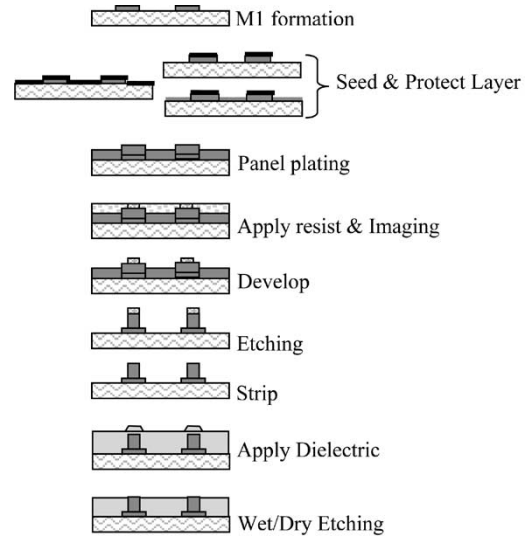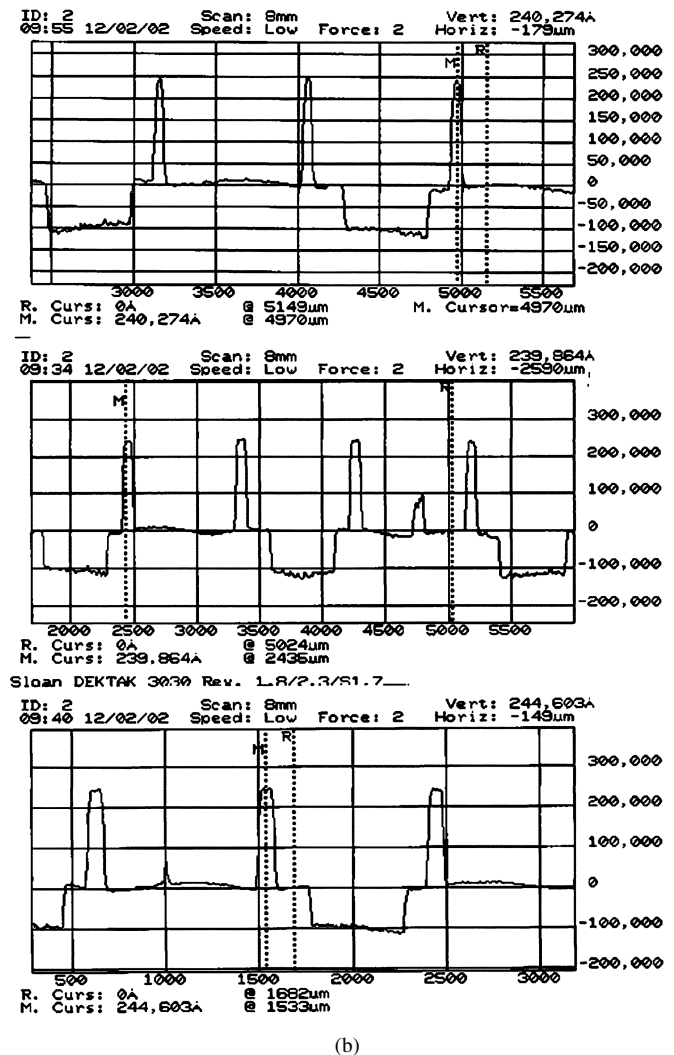


Fig. 13. (a) P²ES process flow of uniform Cu stud formation. (b) Copper stud height uniformity within 1 $\mu$m on 50-, 75-, and 100-$\mu$m diameter microvias.

migrated from the conventional dogbone structure to via-in-pad structures with conformal vias (shown in Fig. 12). For future fine pitch flip-chip interconnects, it will be necessary to migrate
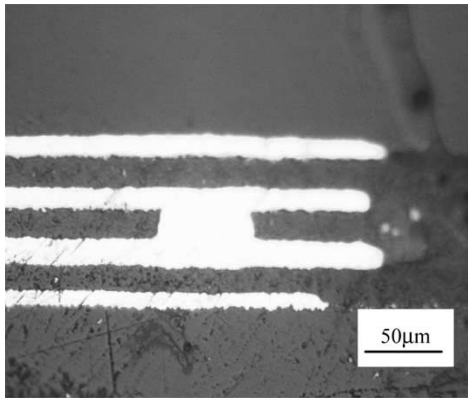
Fig. 14.   Four-metal layer build-up structure on high Tg FR-4 with filled via vertical interconnection.

to planar pad structures with filled and stacked vias and minimum capture pad size as shown in Fig. 12.

A novel low-cost process for fabricating multilayer stacked via structures has been developed using a panel electroplating and subtractive etch process called P$^2$ES (panel plating etched stud) [47]. Filled stacked vias of 50, 75, and 100 $\mu$m diameter up to four metal layers have been demonstrated using this low cost large area approach that does not involve any chem.-mech polishing (CMP). A schematic of the process sequence for the P$^2$ES process is shown in Fig. 13(a). Since this process utilized photoresist to define the via structures, it does not have any minimum size limitations common to conventional laser and photovia processes. Furthermore, this process is versatile and can be used in conjunction with most liquid, dry film, and RCC dielectrics. Stud height uniformities of less than 1 $\mu$m have been demonstrated using this technique on 300 mm $\times$ 300 mm FR-4 substrates as seen in Fig. 13(b). A typical four-metal layer structure used in a build-up SOP application is shown in Fig. 14. This process is currently being extended to ultrafine microvias of 10–15 $\mu$m diameters. The stacked via structure along with the ultrafine lines can potentially meet the interconnection and global wiring requirements of next-generation SOP packages.

## IV. CONCLUSION

In spite of the tremendous progress in microvia and high-density substrate technologies in the last two decades, a new set of substrate and dielectric materials and processes are needed. Several dielectric materials including BCB, A-PPE, LCP offer the potential to satisfy the electrical performance specifications in the short run but new materials with low dielectric loss and processable into thinner films at lower cost are needed in the long run. These, together with high-k dielectrics processed as thin films, form the basis of highly integrated and high performance packages to provide digital functions of the SOP mixed signal systems. Thus, lower k and low-loss compatible dielectrics along with innovative conductor metallization processes for multilayer build-up processes are expected to lead to microminiaturized and multifunction SOP packages with unparalleled performance, cost, and reliability.

## REFERENCES

[1] "Flip Chip Substrate Top-side Fan-out Potential Solutions", Table 100, and "Single Chip Packaging Technology Requirements", Table 93, Assembly & Packaging, The International Technology Roadmap for Semiconductors, 2002 Update to the 2001 Roadmap," SIA Semiconductor Industry Association, Alexandria, VA, 2003 ed..

[2] *National Electronics Manufacturing Initiative (NEMI)*, 2000.

[3] Y. Tsukada, S. Tsuchida, and Y. Mashimoto, "Surface laminar circuit packaging," in *Proc. 42nd Electronic Components and Technol. Conf.*, 1992, pp. 22–27.

[4] M. Asai, "New packaging substrate technology IBSS (interpenetrating polymer network build up structure system)," in *Electronic Packaging Materials Science IX. Symp.*, 1997, pp. 117–124.

[5] M. Stampanoni and W. Schmidt, "Modern interconnect solutions for miniaturized medical electronic devices," in *Proc. HD Int. Conf. High-Density Interconnect and Systems Packaging (SPIE)*, vol. 4217, 2000, pp. 526–530.

[6] K. Segawa, "Build-up PWB with laser-processed via holes "VIL"," in *Proc. SPIE—The Int. Soc. Opt. Eng.*, vol. 3582, 1999, pp. 419–424.

[7] CLLAVIS build-up substrate (2003). [Online]. Available: www.cmk-corp.com

[8] D. Andoh, Y. Tomita, T. Nakamura, and F. Echigo, "The progress of the ALIVH substrate," in *Proc. 52nd Electronic Components and Technology Conf.*, 2002, pp. 1419–1424.

[9] Y. Fukuoka, T. Oguma, and Y. Tahara, "New high density substrates with buried bump interconnection technology (B$^2$it™) -design features of electrical and thermal performance with the actual applications," in *Proc. 1998 Int. Symp. Microelectronics (IMAPS)*, San Diego, CA, Nov. 1998, pp. 405–412.

[10] T. Kariya and R. Enomoto, "Development of multilayer printed wring board with stacked via holes using single step laminating process," in *Proc. 3rd IEMT/IMC Symp.*, 1999, pp. 194–199.

[11] Patterned Prepreg Layup Process (PALAP) [Online]. Available: http://www.denso.co.jp/en/newsreleases/020 529-01.html

[12] CPCore Package [Online]. Available: http://www.kyocera-slc.co.jp/english/products/cpcore.html

[13] D. Hurwitz, E. Igner, B. Yofis, and D. Katz, "Electronic interconnect structure and method for manufacturing it,", 2001.

[14] M. Akazawa, S. Kuramochi, T. Maruyama, K. Nakayama, A. Takano, M. Yamaguchi, and Y. Fukuoka, "High-density packaging technologies on silicon substrates," in *Proc. 53rd Electron. Components and Technology Conf.*, 2003, pp. 647–651.

[15] P. M. Raj, K. Shinotani, S. Mancheol, S. Bhattacharya, V. Sundaram, S. Zama, L. Jicun, C. Zweben, G. E. White, and R. R. Tummala, "Selection and evaluation of materials for future system-on-package (SOP) substrate," in *Proc. 51st Electron. Components and Technology Conf.*, 2001, pp. 1193–1197.

[16] S. Banerji, P. M. Raj, K. Shinotani, M. Seo, C. Zweben, S. K. Bhattacharya, and R. R. Tummala, "Control of warpage during build-up of multilayered high-density wiring with stiff and low-CTE base substrates," in *Proc. 2001 HD Int. Conf. High-Density Interconnect and Systems Packaging (SPIE)*, vol. 4428, 2001, pp. 279–284.

[17] S. Banerji, P. M. Raj, F. Liu, K.-i. Shinotani, S. Bhattacharya, and R. R. Tummala, "The role of stiff base substrates in warpage reduction for future high-density-wiring requirements," in *Proc. 8th Int. Advanced Packaging Materials Symp.*, Stone Mountain, GA, 2002, pp. 221–225.

[18] R. R. Tummala, *Fundamentals of Microsystems Packaging*.   New York: McGraw-Hill, 2001.

[19] R. V. Tanikella, "Variable frequency microwave processing of materials for microelectronic applications," Ph.D. degree dissertation, School of Chemical Engineering, Georgia Tech, 2003.

[20] T. Sung, "Variable frequency microwave curing of polymer dielectrics on metallized organic substrates," M.S. degree thesis, School of Chemical Engineering, Georgia Tech, 2003.

[21] K. Farnsworth, R. V. Manepalli, S. A. Bidstrup Allen, and P. A. Kohl, "Variable frequency microwave curing of 3, 3', 4, 4-biphenyltetracarboxylic acid dianhydride/P-phenylenediamine (BPDA/PPD)," in *Int. J. Microcircuits Electron. Packag.*, vol. 23, 2000, pp. 162–171.

[22] ——, "Variable frequency curing of photosensitive polyimides," *IEEE Trans. Comp. Packag. Technol.*, vol. 24, pp. 474–481, 2001.

[23] R. V. Tanikella, S. A. Bidstrup Allen, and P. A. Kohl, "Variable frequency microwave curing of benxocyclobutene," *J. Appl. Polymer Sci.*, vol. 83, pp. 3055–3067, 2002.

[24] R. Lauf *et al.*, "2 to 18 GHz broadband microwave heating systems," *Microwave J.*, p. 24, Nov. 1993.

[25] B. Panchapakesan, P. F. Mead, Z. Fathi, and D. Tucker, "Variable frequency microwave: A new approach to curing," *Adv. Packag.*, vol. 60, Sept./Oct. 1997.

[26] Y. Bai, P. Chiniwalla, E. Elce, S. A. Bidstrup Allen, and P. A. Kohl, "Photosensitive polynorbornene based dielectric: Part I, structure-property relationships," *J. Appl. Polymer Sci.*, vol. 91, no. 5, pp. 3023–3030, 2004.

[27] ——, "Photosensitive polynorbornene based dielectric: Part II, sensitivity and spacial relationships," *J. Appl. Polymer Sci.*, vol. 91, no. 5, pp. 3031–3039, 2004.

[28] P. Chiniwalla, Y. Bai, E. Elce, R. Shick, S. A. Bidstrup Allen, and P. A. Kohl, "Crosslinking and decomposition reactions of epoxide functionalized polynorbornene: Part I: FTIR and thermogravimetric analysis," *J. Appl. Polymer Sci.*, vol. 89, no. 2, pp. 568–577, 2003.

[29] J. F. Remenar, C. J. Hawker, J. L. Hedrick, S. M. Kim, R. D. Miller, C. Nguyen, M. Trollsas, and D. Y. Yoon, "Templating nanopores into poly(methylsilsesquioxane): New low dielectric coatings suitable for microelectronic applications," in *Low Dielectric Constant Materials IV*, C. Chiang, P. S. Ho, T. M. Lu, and J. T. Wetzel, Eds. Warrendale, PA: Mater. Res. Soc. Symp., 1998, vol. 511, pp. 69–74.

[30] A. M. Padovani, L. Rhodes, L. Riester, G. Lohman, B. Tsuie, J. Conner, S. A. Bidstrup Allen, and P. A. Kohl, "Porous methylsislsesquioxane for Low-k dielectric applications," *Elect. Solid-State Lett.*, vol. 4, no. 11, pp. F25–F28, 2001.

[31] S. Nitta, A. Jain, V. Pisupatti, W. N. Gill, P. C. Wayner Jr., and J. L. Plawsky, "Fabrication and characterization of spin-on silica xerogel films," in *Low Dielectric Constant Materials IV*, C. Chiang, P. S. Ho, T. M. Lu, and J. T. Wetzel, Eds. Warrendale, PA: Mater. Res. Soc. Symp., 1998, vol. 511, pp. 99–104.

[32] T. Ramos, K. Rhoderick, R. Roth, L. Brungardt, S. Wallace, J. Drage, J. Dunne, D. Endisch, R. Katsanes, N. Viernes, and D. M. Smith, "Nanoporous silicca for low K dielectrics," in *Low Dielectric Constant Materials IV*, C. Chiang, P. S. Ho, T. M. Lu, and J. T. Wetzel, Eds. Warrendale, PA: Mater. Res. Soc. Symp., 1998, vol. 511, pp. 105–110.

[33] W. T. Tseng, C. H. Lo, and S. C. Lee, "Electroless deposition of Cu thin films with $CuCl_2$-$HNO_3$ based chemistry: I. Chemical formulation and reaction mechanisms," *J. Electrochem. Soc.*, vol. 148, no. 5, pp. C327–C332, 2001.

[34] M. Matsuoka, J. Murai, and C. Iwakura, "Kinetics of electroless copper plating and mechanical properties of deposits," *J. Electrochem. Soc.*, vol. 139, no. 9, pp. 2466–2470, 1992.

[35] S. Nakahara, Y. Okinaka, and H. Straschil, "The effect of grain size on ductility and impurity content of electroless copper deposits," *J. Electrochem. Soc.*, vol. 136, p. 1120, 1989.

[36] A. Hung and K. M. Chen, "Mechanism of hypophosphite-reduced electroless copper plating," *J. Electrochem. Soc.*, vol. 136, no. 1, pp. 72–75, 1989.

[37] J. Rangarajan, K. Mahadevaiyer, and W. Gregory P., "Electroless Copper Plating Bath,", 1989.

[38] D. H. Cheng, W. Y. Xu, Z. Y. Zhang, and Z. H. Yiao, "Electroless copper plating using hypophosphite as reducing agent," *Metal Finishing*, vol. 95, no. 1, pp. 34–37, 1997.

[39] A. Hung, "Electroless copper deposition with hypophosphite as reducing agent," *Plat. Surf. Fin.*, vol. 75, no. 1, pp. 62–65, 1988.

[40] L. D. Burke, G. M. Bruton, and J. A. Collins, "The redox properties of active sites and the importance of the latter in electrocatalysis at copper in base," *Electrochim. Acta*, vol. 44, pp. 1467–1479, 1998.

[41] A. Hung, "Kinetics of electroless copper deposition with hypophosphite as a reducing agenT," *Plat. Surf. Fin.*, vol. 75, no. 4, pp. 74–77, 1988.

[42] P. E. Kukanski, J. J. Grunwald, D. R. Ferrier, and A. Sawaska, "Electroless copper composition solution using a hypophosphite reducing agent,", 1980.

[43] Y. M. Lin and S. C. Yen, "Effects of additives and chelating agents on electroless copper plating," *Appl. Surf. Sci.*, vol. 178, pp. 116–126, 2001.

[44] F. Liu, V. Sundaram, S. Mekala, G. White, D. Sutter, and R. R. Tummala, "Fabrication of ultrafine line circuits on PWB substrates," in *Proc. 52nd Electron. Comp. Technol. Conf.*, May 2002, pp. 1425–1431.

[45] F. Liu, V. Sundaram, G. White, and R. Tummala, "Ultra fine line HDI technology at georgia tech PRC," *HDI-The Magazine of High-Density Interconnect*, pp. 20–24, Aug. 2000.

[46] F. Liu, V. Sundaram, G. White, D. Sutter, and R. R. Tummala, "Ultra-HDI with low cost photo-imageable polymers," in *Proc. Int. Symp. Adv. Packag. Mater.: Processes, Properties and Interfaces*, Mar. 2001, pp. 153–158.

[47] F. Liu, G. White, V. Sundaram, A. O. Aggarwal, S. M. Hosseini, D. Sutter, and R. Tummala, "A novel technology for stacking microvias on printed circuit boards," in *Proc. 53rd IEEE ECTC*, May 2003, pp. 1134–1139.
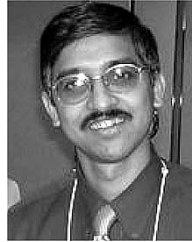
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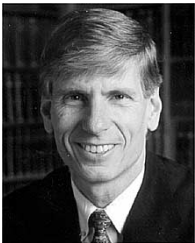
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