Heat Dissipation in High-Power GaN Electronics on Thermally Resistive Substrates

Adam Christensen, William A. Doolittle, *Member, IEEE*, and Samuel Graham

***Abstract*—The heat dissipation in GaN devices grown on low thermal conductivity lithium gallate (LGO) substrates was investigated. The thermal conductivity of single-crystal LGO was measured utilizing the 3ω technique for temperatures ranging from 100 K–500 K. For the GaN layer, the thermal conductivity was estimated using a phonon transport model which included dislocation density and temperature dependence. These data were then used in a finite element program to determine the thermal behavior of a heterojunction field-effect transistor. Based on a maximum junction temperature of 500 K, it was found that devices with a power dissipation of 1 W/mm were possible if the primary heat dissipation path was through the low thermal conductivity substrate. However, in using a front side cooling scheme, results suggest that it may be possible to develop devices with power dissipation in the range of 10 W/mm.**

***Index Terms*—Gallium nitride (GaN), lithium gallate (LGO), power electronics, thermal conductivity.**

I. Introduction

THE development of wide-band gap semiconductors using GaN has enabled technological progress in the areas of advanced communications, solar blind UV sensors, and solid state optical devices. While devices made with GaN have the ability to operate stably at elevated temperatures (200 °C), challenges arise in dissipating the heat from these high power density devices in order to maintain reasonable operational temperatures [1]. Several system-level cooling schemes have been presented for efficient heat dissipation, such as flip-chip bonding, two-phase spray cooling, and mounting devices onto high thermal conductivity substrates [2]–[7]. In many of the thermal management strategies presented, a significant portion of the heat removal occurs from dissipation of thermal energy through the substrate of the GaN device. Thus the contributions of the substrate to the device thermal resistance must be understood. In general, this contribution is more complicated than the substrate simply adding its own thermal resistance to the heat dissipation path. While GaN is typically grown on a number of high thermal conductivity substrates, passive heat dissipation into these materials can be adversely affected the by dislocation densities induced in the GaN from lattice mismatch during epitaxial growth and the interface resistance with the substrate material. In order to dissipate thermal energy under a minimal temperature rise, an accurate understanding of the thermal behavior of the materials used in construction of the device must be obtained.

Currently, GaN-based devices are grown on a limited number of substrates, most popular being sapphire due to its low cost. However, sapphires lattice mismatch with GaN along the a axis is -13.62% [8]. This mismatch results in difficulties when trying to grow high-quality thin-films because of large dislocation densities that are inherent in an epitaxial process ($> 10^9$ cm^{-2}) [9], [10]. Low-temperature deposited GaN buffer layers and lateral epitaxy overgrowth can help to reduce the dislocation density in the active region of the device but induces layers of lower thermal conductivity material near the substrate interface. To alleviate this issue, a substrate that has a closer lattice match would help to simplify the growth and heat dissipation processes. Of the available substrates which are closely matched with GaN, lithium gallate (LGO) possesses a lattice mismatch of only 0.19% and would therefore be a strong candidate for growing high quality GaN films without the need for buffer layers [8]. The growth of GaN on LGO has been demonstrated and is currently being considered for applications involving LEDs, laser diodes and metal–semiconductor–metal (MSM) photodetectors. Some acoustic devices have also shown promise due to the low defect density compared to alternatives [10].

However, the heat dissipation in GaN–LGO devices may be of concern since it is expected that LGO will have a low thermal conductivity, limiting conduction pathways. This technological challenge is also seen in other low thermal conductivity substrate materials like sapphire. In spite of the fact that growth technologies have shown the ability to produce high quality GaN on a number of thermally resistive substrates their low thermal conductivity generally precludes their wide use in high power applications. Of all the low thermal conductivity substrates, LGO is expected to be the most resistive to heat dissipation, but provides one of the closest lattice matches with GaN. However, the thermal performance estimations of GaN–LGO devices are limited by the lack of thermal conductivity of LGO and an understanding of the temperature dependence and defect dependent thermal conductivity in the GaN active layer. To address these issues, thermal conductivity measurements were made on single crystal LGO and estimates of GaN thermal conductivity were made using a phonon transport model with a relaxation time approximation. These methods, their results, and impact on heat dissipation modeling are discussed in the following sections.

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A. Christensen and S. Graham are with the Woodruff School of Mechanical Engineering. Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: sam.graham@me.gatech.edu).

W. A. Doolittle is with the Department of Electrical Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

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II. Experimental Procedure

Measurements of the thermal conductivity of the LGO samples followed the 3ω method outlined in [11]. Samples were prepared from a 1×1 cm sample of LGO on which a metal line heater was microfabricated using a standard photolithography and a liftoff process. The geometry of the line heaters was 50 μm wide with a 3500 μm long gage section. The metal line structure was deposited by dc sputtering and consisted of a titanium adhesion layer (600Å) and a copper layer serving as the primary device (2500Å). Since the line heater also serves as an electrical resistance thermometer, the patterned lines were annealed at 400 °C for 1 h in flowing argon in order to anneal the metal and ensure a constant temperature coefficient of resistivity over intended test regime. It was found that unannealed samples could experience a change in the thermal resistivity coefficient by as much as 40% which makes device calibration difficult. After the annealing, it was found that the electrical resistivity (R) as a function of temperature was highly linear, with a $\Delta R/R$ on the order of 0.8%/K.

Since the sample of LGO was not electrically conductive, there was no need for a passivation layer to electrically isolate the line heater. Large contact pads were utilized in order to bond wire leads to with a high-temperature electrically conductive ceramic adhesive. After attaching the wire leads, the sample was mounted onto a cold finger in an evacuated ($\sim 10^{-7}$ torr) open flow liquid nitrogen cryostat (Janis Research) and connected to the 3ω signal conditioning circuit and a lock-in amplifier (SRS Model SR830). Samples were tested over a frequency range of 50–300 Hz while the temperature of the cryostat was controlled from 100 K–500 K (Lakeshore 331 Controller). By measuring the magnitude of the in-phase component of the 3ω voltage drop across the heater, the thermal conductivity can be determined. It is important to note that radiative heat losses over the range of temperatures tested are considered to be negligible [11].

III. Results and Discussion

The results of the thermal conductivity measurements on LGO are shown in Fig. 1. These measurements were repeated several times with less than a 10% variation in thermal conductivity values across all measurements. The data shows a strong temperature dependent thermal conductivity which increases with decreasing temperature. Values in these experiments ranged from 9 W/mK at 500 K up to 140 W/mK at 100 K. This behavior is typical of that seen in crystalline semiconductors where temperature dependent phononphonon scattering processes dominate the thermal resistance. The room temperature thermal conductivity of LGO, 17 W/mK, is lower than that of sapphire and may present increased power dissipation limitation issues as seen in GaN-sapphire devices. However, by cooling the GaN-LGO devices below room temperature, it may be possible to operate moderately powered devices as discussed later.

IV. LGO Thermal Conductivity Correlation

In order to correlate and predict the temperature-dependent behavior of the LGO, a modified Callaway model for thermal conductivity was utilized which employs a relaxation time approximation to the Boltzmann Transport Equation [12]. In the limit of the Debye approximation, the thermal conductivity can be given by [13]–[16]

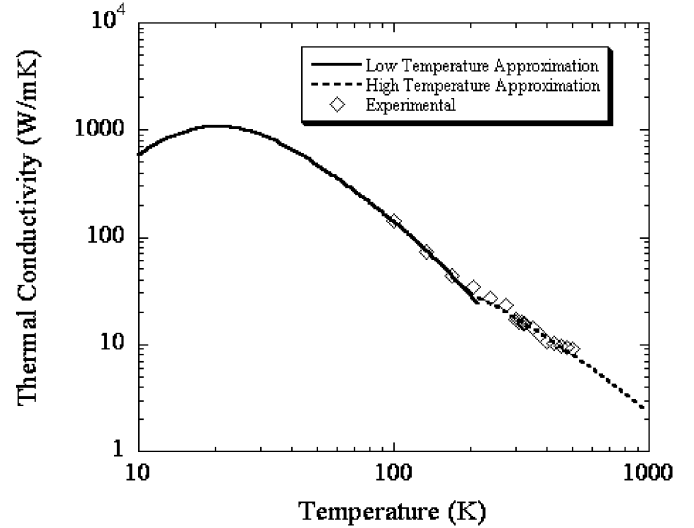

Fig. 1. Experimental data obtained on lithium gallate. Experimental data is accompanied by phonon transport models that were developed. "Low" and "high" temperature approximations were made in order to account for the dominant scattering processes at the corresponding temperatures. The maximum thermal conductivity 1081 W/mK was found at 21 K.

TABLE I
SUMMARY OF LGO MATERIAL PROPERTIES

Property	Value
Density	4170 kg/m^3
Molecular Weight	108.6628 g/mol
Transverse Acoustic Speed [17]	3700 m/s
Longitudinal Acoustic Speed [17]	5794.23 m/s
θ_D (Debye Temperature)	547.39 K
ω_D (cut off frequency)	7.1661x10^{13} s^{-1}

$$k = \frac{1}{3}\left(\frac{k_B T}{\hbar}\right)^3 \frac{k_B}{2\pi^2} \sum_j \frac{1}{v_j} \int_0^{\theta/T} \frac{x_\omega e^{x_\omega} \tau_j}{e^{x_\omega} - 1} dx_\omega \quad (1)$$

where x_ω is the nondimensional frequency, k_B is the Boltzmann constant, v is the phonon velocity, τ is the phonon relaxation time, and $\hbar$ is Planck's constant divided by 2π. The summation in (1) is over the longitudinal and two acoustic phonon polarizations which are assumed to be the dominant heat carriers as seen in other semiconductor materials. Several simplifying assumptions can be used in order to aid in the solution of this equation. In this study it has been assumed that the LGO has a diffuse-gray phonon dispersion relationship due to the lack of data on dispersion properties in LGO. The longitudinal and transverse acoustic phonon speeds have been calculated from the elastic constants of LGO [16], [17]. A power mean technique was used to calculate an effective velocity over the three phonon polarizations and is in the form shown in (2) [18]

$$v = \left(\frac{1}{3}\sum_{j=1}^{3} v_j^{-3}\right)^{-1/3}. \quad (2)$$

Here, j is the phonon polarization index. LGO material properties used in the calculations have been outlined in Table I.

TABLE II
SUMMARY OF RELAXATION TIMES

Scattering Process	Inverse Relaxation Time
Impurities (mass difference)	$\tau_I^{-1} = A\omega^4$
Three Phonon Scattering:	
N Process	
Low Temperature	$\tau_N^{-1} = B_1T^3\omega^2$
High Temperature	$\tau_N^{-1} = B_1T\omega^2$
U Process	$\tau_U^{-1} = B_2T^3\omega^2$

TABLE III
SUMMARY OF RELAXATION TIME COEFFICIENTS

Coefficient	High Temperature	Low Temperature
A (sec^3)	2.3283x10^{-42}	7.246x10^{-45}
B1 (sec deg^{-3})	1.0688x10^{-24}	1.8836x 10^{-23}
B2 (sec deg^{-3})	2.9939x10^{-24}	2.4177x 10^{-23}

Using this averaging technique the phonon velocity used in the calculations was 4066.1 m/s. This sound speed led to a Debye temperature of $\theta_D = 547.39\ K$. The relaxation time relationships used have been summarized in Table II.

The phonon scattering processes are summed up through the use of Mathessien's Rule

$$\tau_C^{-1} = \tau_I^{-1} + \tau_N^{-1} + \tau_U^{-1} \tag{3}$$

where τ_I is impurity scattering, τ_N is normal phonon scattering (N), and τ_u is Umklapp phonon scattering processes (U). The forms for these equations are listed in Table II.

A high-temperature and low-temperature fit was used in order to properly weight the N-phonon process relaxation times; "high" temperature is considered to be above 240 K. In applying the model, the coefficients A, B_1, and B_2 were determined by minimizing the error between the experimental data and the model prediction by using the Nedler–Mead simplex method. The resulting coefficients have been outlined in Table III. The model shows good agreement with the experimental data with the largest deviation at room temperature where the transition from the high-temperature to the low-temperature model occurs. Based on this model, a peak thermal conductivity of 1081 W/mK is expected to occur near 21 K

V. DEVICE MODEL

To estimate the performance of a GaN–LGO device, a model heterojunction field effect transistor (Fig. 2) was modeled using finite element analysis. The governing differential equation that was solved is the familiar two-dimensional Fourier equation with a heat generation term (4)

$$-\nabla^2 \cdot [k(T)T(x,y)] = Q. \tag{4}$$

The device had a gate length of 194 μm; both the source and drain were 80 by 1 μm thick; the gate was 0.8 by 1 μm thick. The spacing between the source and gate was 1.8 μm and there

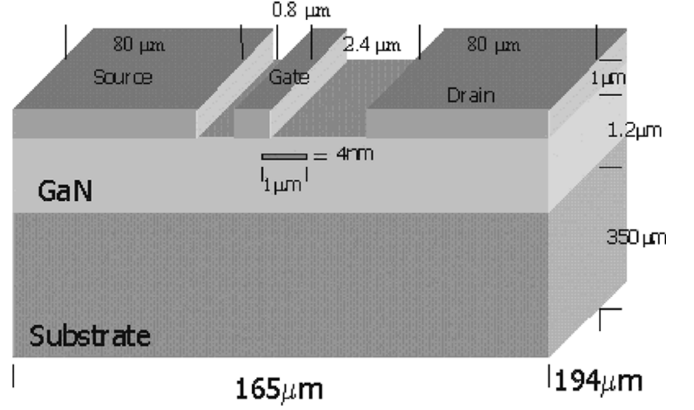

Fig. 2. Dimensions of HFET device modeled. The heat generation zone is shown within the active GaN layer just below the gate.

was a 2.4-μm gap between the gate and the drain, yielding an asymmetric gate structure. The GaN layer was 1.2 μm while the LGO substrate was 350 μm. Other pertinent dimensions are given in Fig. 2.

Heat generation in the structure was assumed to be in a highly localized region on the drain side of the gate as specified by Anholt [19] and verified experimentally by Kuball et al. [20]. This region is also the location of the peak electrical field in the device. Current state of the art GaN HFETs have been known to operate for brief periods at 30 W/mm but a more common value is 10 W/mm [21]. If this power is used in the geometry above, an overall volumetric generation value of 2.5 $\times 10^{18}$ W/m^3 is calculated. Thermal boundary conditions were chosen such that all sides are adiabatic except the bottom of the substrate which was held at a constant temperature. This fixed temperature of the bottom surface was varied from 100–350 K to simulate the performance of devices with backside liquid cooling, including cryogenics.

Interface thermal resistance between the GaN and LGO as was estimated using the diffuse mismatch model (DMM) as described in [22] and was found to be 5.34 $\times 10^{-10}$ m^2 K/W. The diffuse mismatch model allows for the transmission of phonons across the boundary based on the ratio of the density of states. Also included was the interface resistance between the metal interconnects and the GaN. Since electrons are the major heat carrier in metals the interface resistance calculation takes into consideration the additional resistance that is present as a result of electron-phonon coupling between the metal and dielectric layers [23]. In the numerical model Pt/Ti ohmic contacts were included to simulate the source, gate and drain. The interface resistance due to phonon anharmonicity at the interface (the so-called phononphonon interaction) was found to be $\sim\ 4.4606 \times 10^{-10}$ m^2 K/W again using the DMM. The added electron-phonon coupling resistance was estimated using typical values of conductance coefficients found from performing femtosecond photoexcitation experiments by the following equation:

$$h_{\rm ep}^{-1} = (Gk_p)^{-1/2} \tag{5}$$

where $h_{\rm ep}$ is the electron-phonon coupled conductance; G is the conductance coefficient between the electrons and

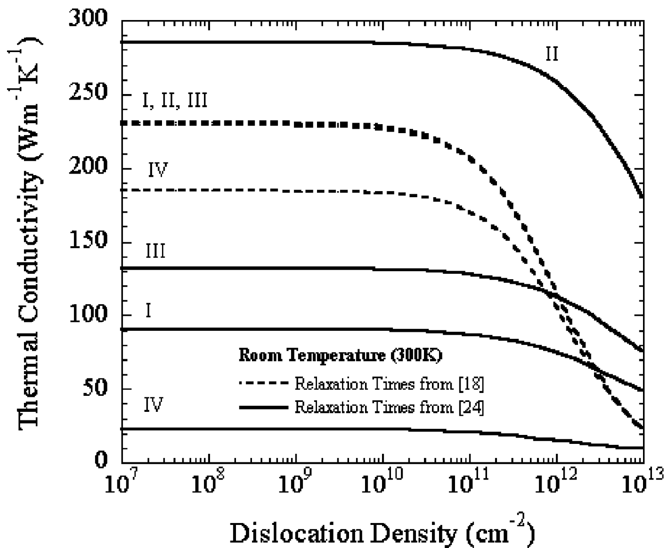

Fig. 3. Thermal conductivity of GaN as a function of dislocation density estimated from a phonontransport calculation based on (1). Roman numerals correspond to the different impurity profiles listed in Table IV. Note the negligible difference in I, II, and III using the relaxation times specified in [18].

TABLE IV
IMPURITY CONCENTRATION PROFILES INVESTIGATED

Atom	I (cm^{-3})[a]	II (cm^{-3})[b]	III (cm^{-3})[b]	IV (cm^{-3})[b]
Hydrogen	4x10^{18}	2x10^{17}	3x10^{18}	1.4x10^{20}
Carbon	1.5x10^{18}	3x10^{16}	6x10^{15}	2x10^{17}
Oxygen	2x10^{18}	1x10^{17}	6x10^{16}	3x10^{16}
Silicon	8x10^{17}	3x10^{16}	1.5x10^{18}	1.4x10^{20}

[a] From [18] [b] From [24]

phonons, and k_p is the phonon thermal conductivity from kinetic theory

$$k_p = \frac{1}{3} c_p v_p \lambda_p. \tag{6}$$

Here, c_p is the phonon specific heat, v_p is the sound speed in the material and λ_p is the phonon mean-free path. Typical values of G are reported to be $10^{16} - 10^{17}$ W/m^{3}K and the range of k_p is usually 10–20 W/mK [23]. As a first estimate the median value was used for each parameter that resulted in a coupling resistance of 1.934×10^{-9} m^2 K/W.

To complete the analysis, the effects of dislocations and temperature on the thermal conductivity of the GaN layer were estimated using the relaxation time approximation to the Boltzmann Transport equation. The relaxation time expressions that were used are referenced in [18] and [24]. The results of integrating (1) are shown in Fig. 3. It should be noted that the results in Fig. 3 were calculated using a Debye temperature of 613 K for GaN. This value varies significantly from the results in [18] and [24] however it is supported by [25]. Variation in the Debye temperature will alter the upper limit of integration in (1). In all the cases that are plotted, the effect of dislocation densities below 10^{13} cm^{-2} plays a minor role in thermal conductivity of GaN.

Fig. 4 depicts the temperature dependent thermal conductivity of GaN with a dislocation density of 10^8 cm^{-2}. This value

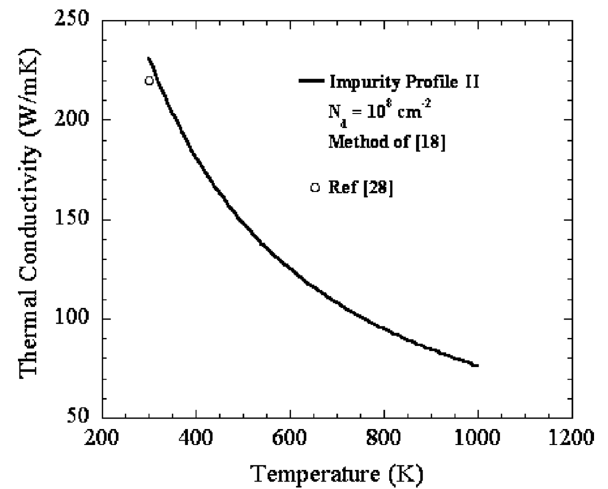

Fig. 4. Temperature dependent thermal conductivity of GaN, with a fixed dislocation density of 10^8 cm^{-2}, estimated from a phonon transport calculation based on (1). Included in the figure is a data point from [28] for comparison.

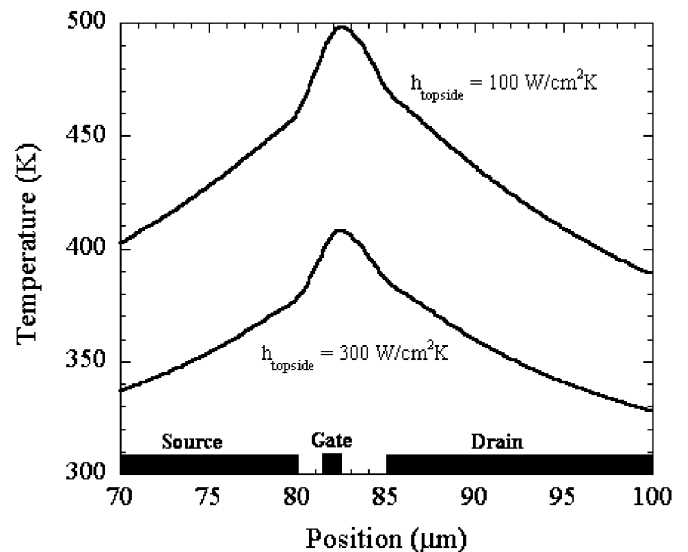

Fig. 5. Results from finite element analysis showing the surface temperature distribution localized around the gate. Two different topside cooling techniques were simulated by varying the convective coefficient along the upper surface.

was chosen as a conservative estimate of the number of dislocations which would exist in a GaN layer on LGO. Based on these phonon transport calculations, variations in the dislocation density by an order of magnitude above and below 10^8 cm^{-2} will have a negligible effect on the thermal conductivity at temperatures above 100 K. Polynomial fits to the thermal conductivity data in Figs. 1 and 4 were used to input temperature dependent data in the finite element analysis, the third-order approximations (7) and (8) are provided and are valid between 100 K and 1000 K (units are in W/mK). The conductivity model that was used for the finite element analysis was based on impurity profile II and relaxation times outlined in [18]

$$k_{\mathrm{LGO}} = -9 \times 10^{-8} T^3 + 0.0002 T^2 - 0.172 T + 52.907 \tag{7}$$
$$k_{GaN} = -4 \times 10^{-7} T^3 + 0.0011 T^2 - 1.0515 T + 453.74. \tag{8}$$

A surface temperature plot is presented in Fig. 5 for an HFET device outputting 10 W/mm under a topside cooling scheme.

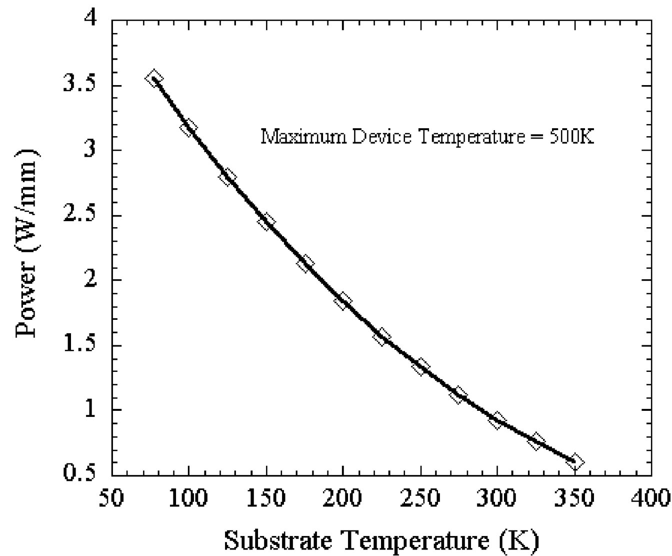

Fig. 6. Results from finite element analysis showing the maximum device power dissipation that yields a junction temperature of 500 K as a function of substrate backside temperature.

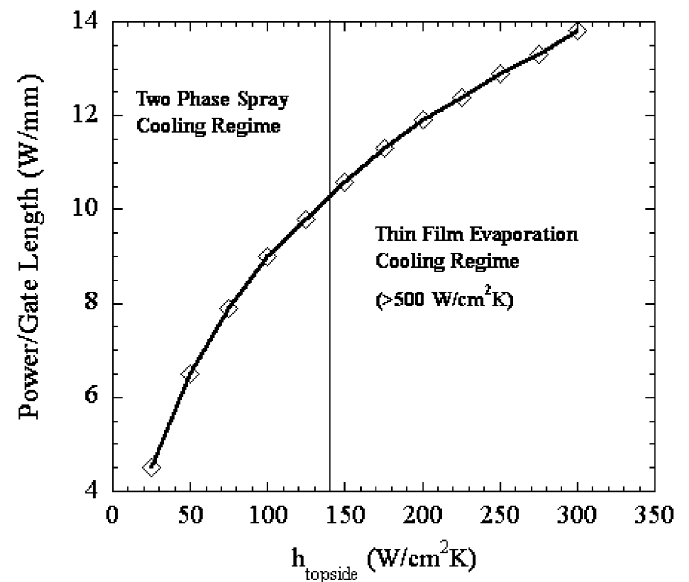

Fig. 7. Finite element results showing maximum power dissipation as a function of front side convection heat transfer conditions. Model assumes an ambient temperature of $T_{amb} = 295$ K, backside convection coefficient of $h = 50$ W/K^{2}K.

The results of the finite element model are shown in Fig. 6 which show the maximum power dissipation which will result in a junction temperature of 500 K. The data in the graph show that GaN–LGO devices will be limited to low power operation (< 1 W/mm) when the backside of the substrate is held at 300 K. Maximum power dissipation increases if the bottom of the substrate is cooled below room temperature, which will require cryogenic cooling. A maximum power dissipation of 3 W/mm can be obtained when the substrate is held at 100 K. However, this will place a severe temperature gradient across the device, making this operating condition difficult to achieve reliably. Thus, with heat dissipation primarily through the substrate, GaN–LGO devices will be limited to low-power operation.

In order to explore heat dissipation options which may enable high power GaN–LGO devices or devices grown on other thermally resistive materials, removal of the heat from the active transistor side was investigated. Since high heat flux removal is necessary for this application, two phase cooling was considered. For this study, a convective heat transfer boundary condition was added to the transistor side of the device in Fig. 2 while a fixed convection boundary condition with $h = 50$ W/M^{2}K was applied to the bottom of the substrate. Fluid temperatures for the front and rear side convection were both 295 K. In order to allow both dielectric and nondielectric fluids to be used on the transistor side, a 1-μm-thick polycrystalline diamond layer with a thermal conductivity of 40 W/mK was also added to the top of the device.

It can be seen from Fig. 7 that power dissipation in GaN-LGO structures increases dramatically over the rear side cooling scheme with power levels greater than 4 W/mm. Based on convection cooling regimes discussed in [26], the use of two-phase spray cooling and thin-film evaporation may eventually allow GaN-low conductivity substrate devices to reach power dissipation levels of 10 W/mm. Improvements in the performance of RF-power devices from top side spray cooling using water and parylene as the dielectric layer has been recently demonstrated [27], showing the viability of this concept. While the highest convective heat transfer coefficients are obtained with deionized water, the use of dielectric fluids may be more practical from a reliability standpoint or the engineering of reliable dielectric coatings must be investigated. In general, the development of front side cooling schemes will extend the useful range of low thermal conductivity substrates like LGO and even sapphire for power semiconductor applications. This technology may also lead the way to the development of GaN devices on a variety of other well lattice matched substrates independent of their thermal conductivities.

VI. Conclusion

The heat dissipation in GaN-LGO devices was modeled using a finite element numerical approach along with measurements and calculations of thermal conductivity of the LGO and GaN layers, respectively. These results show that relatively low-power electronic devices are obtainable if the primary mode of heat dissipation is through the rear of the substrate. However, the use of cooling schemes on the front side of the device where the active transistors are located will yield high-power devices. This result is significant since high-power devices may be achieved with a low thermal conductivity substrate with nearly latticed matched to the active GaN layer. This result also allows for the development of high-quality GaN layers on substrates irrespective of its thermal conductivity, which is in direct contrast to current technological approaches.

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Adam Christensen was born in Grayslake, IL. He received the B.S. degree in mechanical engineering, with minors in both physics and mathematics, from the Milwaukee School of Engineering (MSOE), Milwaukee, WI, in 2003.

He attended one semester at the Electrical Engineering Department, Czech Technical University, Prague, Czech Republic. After a summer fellowship program with Pacific Northwest National Laboratory, Richland, WA, he joined the Georgia Institute of Technology, Atlanta, where he is currently a Graduate Research Assistant. His work investigates both experimental and theoretical thermal conductivity values of wide bandgap semiconductors, GaN, and the substrates used to grow GaN.

William A. Doolittle (M’00) received the B.E.E. (with highest honors) and Ph.D. degrees from the Georgia Institute of Technology (Georgia Tech), Atlanta, in 1989 and 1996, respectively, both in electrical engineering.

He is currently an Assistant Professor, School of Electrical and Computer Engineering, Georgia Tech. He was a Research Engineer II until he was appointed to the academic faculty in January 2001. His principal interest is in the development of nitride-based and crystalline oxide-based devices on innovative substrate materials as well as applying new growth techniques to facilitate material and device improvements. He has pioneered the area of wide bandgap material growth on lithium metal oxides. He has authored or coauthored over 80 research papers/presentations as well as numerous technical reports and patents. His research interests have centered on plasma-enhanced molecular-beam epitaxy for III-nitride growth for RF power electronic and optoelectronic devices, mixed III-nitride/carbide growth, high-temperature CVD silicon carbide growth, and the electrical and optical characterization of electronic materials including silicon, silicon carbide, III-nitrides, dielectrics, and arsenide/phosphide/antimonide-based III-V materials. His current focus is on Fermi-energy control during growth for 3-D epitaxy and enhanced doping in semiconductors, growth of high-quality III-nitride materials for RF electronic and optoelectronic devices, and growth of single-crystal ferroelectric materials.

Samuel Graham received the B.S. degree from Florida State University, Tallahassee, and the Ph.D. degree from the Georgia Institute of Technology (Georgia Tech), Atlanta, both in mechanical engineering.

After his doctoral studies, he served as Senior Member of Technical Staff, Sandia National Laboratories, where he worked on the development of EUV lithography and the thermophysical property characterization of MEMS materials. He is currently an Assistant Professor in the Department of Mechanical Engineering, Georgia Tech, where his work focuses on thermal characterization and reliability of wide bandgap semiconductor devices, thermal MEMS, and the development of organic semiconductors.

Dr. Graham is the recipient of the 2005 National Science Foundation’s CAREER Award.