# DEVELOPMENT OF HIGH POWER NPN GAN/INGAN DOUBLE-HETEROJUNCTION BIPOLAR TANSISTOR

## Final Report

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## I SUMMARY OF PROGRAM ACHIEVEMENT

The Georgia Tech team developed state-of-the-art GaN heterojunction bipolar transistor (HBT) technology in this NSF program. Throughout the project period, baseline device fabrication and material growth techniques were actively studied and significant technological advancement was achieved in III-Nitride (III-N) HBT research. We successfully demonstrated high-current gain (> 100) InGaN HBT on sapphire substrates using a single-pass epitaxial layer growth approach. With the knowledge accumulated in the program, we also demonstrated GaN/InGaN HBTs that can handle ultra-high-d.c. power density > 3MW/cm$^2$, a power density level that none of currently available transistor technologies have ever achieved. Leveraged by the advanced HBT development in this program, we also successfully demonstrated the first microwave III-N HBTs with $f_T$ > 5 GHz. These breakthrough results are important milestones for GaN bipolar transistors to become viable transistor technology for next-generation high-power, high-frequency electronics.

A summary of the work during this period is listed below:

1. High current gain GaN/InGaN HBT with common-emitter current gain > 100 and a collector current density ($J_c$) > 6.7 kA/cm$^2$ was demonstrated. This is the best device performance for direct-growth GaN/InGaN HBT grown on sapphire reported to date.
2. GaN/$In_{0.03}Ga_{0.97}N$ and GaN/$In_{0.05}Ga_{0.95}N$ DHBT structures were implemented on sapphire substrates for study on the effect of indium content in the base layer. The results indicate the GaN/$In_{0.03}Ga_{0.97}N$ DHBT has higher base surface recombination current ($K_{B,urf}$) but lower bulk recombination current ($J_{bulk}$) than GaN/$In_{0.05}Ga_{0.95}N$ DHBT due to lower growth-related defect density in the base layer.
3. GaN/$In_{0.03}Ga_{0.97}N$ DHBT structure was implemented on both sapphire and free-standing (FS) GaN substrates for study on the effect of substrate. With optimized fabrication processes and post-etching surface treatment, a highest

current gain ($h_{fe}$) of 80 on sapphire substrate and 110 on GaN substrate were achieved. The maximum achievable current density ($J_C$) also reached 50 kA/cm$^2$ and 125 kA/cm$^2$ on sapphire and GaN substrates respectively. Using quasi-static pulse measurement, the maximum power density reaches 3 MW/cm$^2$ on GaN substrate which is the highest value reported to date.

4. High temperature (250C) operation is achieved on GaN/InGaN DHBTs on FS-GaN substrate. The current gain remains >43 when the temperature is increased from 25 °C to 250 °C. The breakdown voltage is also increased from 90V to 157V.
5. A significant burn-in effect was found in the GaN/InGaN DHBTs after current-stressing. A significant improvement in current gain from 60 to105 is observed on GaN/InGaN DHBTs on sapphire substrate after a post-process constant current stress step.
6. RF GaN/InGaN DHBT with $f_T$ = 5.3 GHz and $f_{max}$ = 1.2 GHz was successfully demonstrated on sapphire substrate. This is the first demonstration of RF GaN HBT in GHz-range to date.

# II RESEARCH RESULTS

## *II.1 Materials and Epitaxial Structure Development of GaN/In$_x$Ga$_{1-x}$N DHBTs*

The majority of efforts in III-nitride bipolar transistors have been focused on *Npn*-AlGaN/GaN HBTs with *p*-GaN as the base. These devices benefit from high breakdown fields and large bandgap variance for efficient hole blocking at the base-emitter junction, but their performance is limited by the relatively high acceptor activation energy (~170 meV) in Mg-doped GaN. This reduces the p-type doping efficiency of GaN to about 1%, and the resulting lack of carriers leads to low D.C. gain and a highly resistive base region, which increases the contact resistance and limits high frequency operation of the device. Furthermore, since GaN is chemically resistant to wet etchants, dry etching must be used to expose the base. However, this process damages the *p*-type base, and can lead to type conversion – from *p*- to *n*-type – at the etched surface due to a plasma-etching induced N deficiency. This makes it challenging to create a *p*-type ohmic contact to an HBT base region. While some work has been done with pnp designs, low hole doping efficiencies, low hole mobility, collector etch damage and the Cp2Mg "memory effect" in metalorganic chemical vapor deposition all add extra layers of complexity to the structure. The acceptor activation energy of InGaN is lower than that of GaN and, as the bandgap decreases for increased indium content. Thus, higher hole concentrations can be achieved ($p \geq 1\times10^{18}$ cm$^{-3}$) in *p*-InGaN:Mg than p-GaN:Mg. The lower bandgap of InGaN also makes it suitable for the p-type base region of an InGaN/GaN HBT. Reduced etch damage to the base in conjunction with indium incorporation has also been reported. To further eliminate base damage as an inhibitor to device performance, some groups have employed a base regrowth design, where epitaxy is repeated after the base has been exposed. While this method has demonstrated impressive results, its added cost, complexity, and time of manufacture warrants further investigation of single growth designs.

One technical challenge of InGaN growth is its temperature requirement and thermal stability. Indium content decreases with increasing growth temperatures so a low temperature is required to ensure sufficient indium incorporation, typically on the order of 850 °C for low In content $In_xGa_{1-x}N$. Since high quality GaN is typically grown around 1050 °C, some compromise must be made between the growth conditions of the InGaN base and the overlying GaN emitter. Higher temperatures preclude higher indium contents, so the compromise must be made by the emitter–especially in the growth temperature to protect the InGaN base layer–which inevitably results in reduced GaN emitter crystal quality, and is a limiting factor on the performance of the device as a whole. Another challenge lies in avoiding lattice strain between the GaN and InGaN layers. Highly strained interfaces may result in relaxation and defect formation, which will degrade device performance. To assist in strain relief and improve crystal quality, grading layers have been developed for the base-collector and base-emitter junctions. These grading layers also serve to eliminate the effects of conduction band discontinuities at each heterojunction, decreasing current blocking at high injection currents.

In this program, we investigated the effects of base indium content on the operation of HBTs. We have grown two $In_xGa_{1-x}N$/GaN HBT structures, with $x_{In}$ = 0.03 and 0.05. If we consider the band offset between the InGaN base and GaN layers, the HBTs with *p*-$In_{0.05}Ga_{0.95}N$ base are expected to show higher current gain than HBTs with *p*-$In_{0.03}Ga_{0.97}N$ base. At the same time, higher strain conditions and defect formation in the $In_{0.05}Ga_{0.95}N$ base could compensate the advantages offered by higher indium content.

The separate base-only samples, $x_{In}$ = 0.03 and 0.05 for $In_xGa_{1-x}N$, were grown and characterized first. Atomic force microscopy scans of these samples, taken over 5×5 $\mu m^2$, are shown in Figure 1. A higher density of pits is observed for the sample with $x_{In}$=0.05 in the base. These are due to the formation of V-defects, associated with threading dislocations and strain relaxation mechanisms, which are known to become more severe with higher indium content in terms of both density and size. The presence of these pits is also reflected in the emitter surface morphology of the full structure. Since the emitter growth conditions are identical for the two structures, the reduction in emitter quality for the HBT with $x_{In}$=0.05 in the base is attributed to the V-defects at the base-emitter interface which degrade the BE junction.

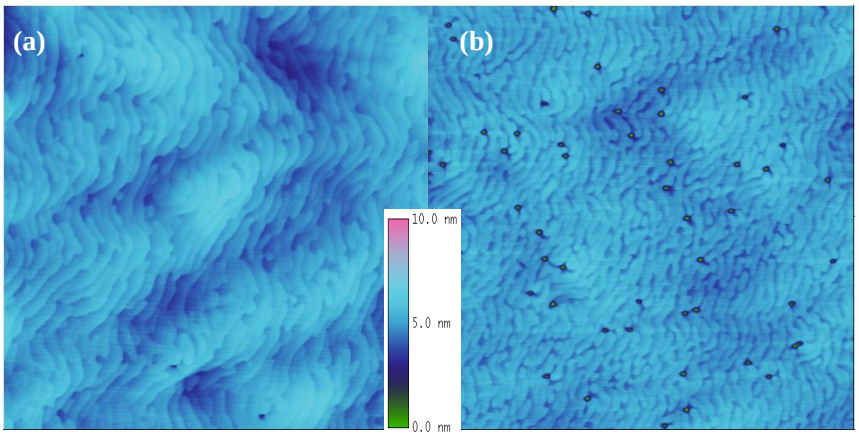


**Figure 1** 5×5 $\mu m^2$ AFM scans of the "base-only" samples with (a) $x_{In}$ = 0.03 and (b) $x_{In}$ = 0.05.

In addition to the study on the effect of base InGaN layer, we explored other growth and epitaxial structure parameters, including (1) strain management, (2) suppression of the effect of "memory effect", (3) mitigation of polarization effect, (4) further improved p-type and n-type doping for base and emitter layers, etc. A epitaxial layer structure was set up base on the extensive study in the growth and epitaxial structure design space. A representative layer structure is shown in **Table 1**.

### *II.2 GaN/$In_{0.03}Ga_{0.97}N$ and GaN/ $In_{0.05}Ga_{0.95}N$ npn DHBT on sapphire substrate*

Two device structures ("Structure-A": GaN/$In_{0.03}Ga_{0.97}N$ DHBTs and "Structure-B": GaN/$In_{0.05}Ga_{0.95}N$ DHBTs) were implemented on sapphire substrates. They have similar epitaxial layer structures except for the indium composition in the base layers, as shown in **Table 1**. The DHBT structures were grown using a Thomas–Swan metalorganic chemical vapor deposition (MOCVD) system. The electron and hole concentrations were calibrated in test samples prior to actual DHBT epitaxial material growth runs.

**Table 1** A summary of layer structure variations of *npn* GaN/InGaN DHBTs on sapphire substrate.

| Layer | Material | | Thickness | Free carrier concentration |
|---|---|---|---|---|
| | Structure-A | Structure-B | | |
| Emitter cap | GaN | GaN | 70nm | $n = 1 \times 10^{19}$ cm$^{-3}$ |
| Emitter grading | $In_xGa_{1-x}N$ (x = 0–0.03) | $In_xGa_{1-x}N$ (x = 0–0.05) | 30nm | $n = 1 \times 10^{18}$ cm$^{-3}$ |
| Base | $In_xGa_{1-x}N$ (x = 0.03) | $In_xGa_{1-x}N$ (x = 0.05) | 100nm | $p = 2 \times 10^{18}$ cm$^{-3}$ |
| Collector grading | $In_xGa_{1-x}N$ (x = 0.03–0) | $In_xGa_{1-x}N$ (x = 0.05–0) | 30nm | $n = 1 \times 10^{18}$ cm$^{-3}$ |
| Collector | GaN | GaN | 500nm | $n = 1 \times 10^{17}$ cm$^{-3}$ |
| Subcollector | GaN | GaN | 1000nm | $n = 3 \times 10^{18}$ cm$^{-3}$ |
| Buffer layer | GaN | GaN | 2500nm | UID |
| Sapphire Substrate | | | | |

The device fabrication process starts with a two-step chlorine-based mesa etching in a STS™ inductively coupled plasma (ICP) etching system using e-beam evaporated $SiO_2$ layers as etching masks. The first mesa etching step is to expose the base layer, and the second mesa etching stops at the sub-collector. After the ICP etching steps, these samples are treated in a diluted KOH/$K_2S_2O_8$ solution under the ultraviolet light illumination to remove the dry-etching-induced etching damage. Ni/Ag/Pt stacks are patterned and annealed for the base contact formation and Ti/Al/Ti/Au films are used for the collector and emitter contacts. No passivation is used on these samples in order to study the intrinsic properties of GaN/InGaN DHBTs.

Fabricated GaN/InGaN DHBTs were characterized using a Keithley 4200 semiconductor characterization system (SCS-4200) at room temperature. A set of typical common-emitter family curves of Structure-A and Structure-B DHBTs that have the same emitter area ($A_E$) of 20 × 20 μm$^2$ is shown in Figure 2.

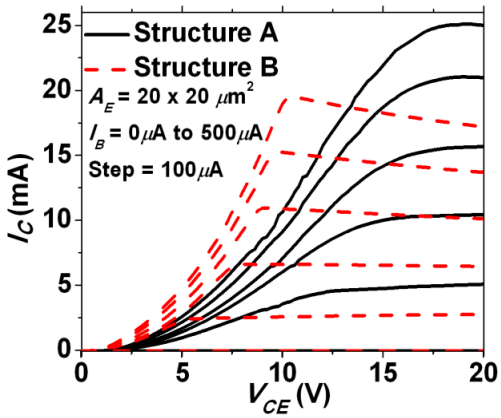


**Figure 2** A comparison of common-emitter characteristics of a Structure-A DHBT (solid lines) and a Structure-B DHBT (dashed lines) with $A_E$ = 20 × 20 μm$^2$.

In Figure 2, the Structure-A shows larger maximum $J_C$ (6.25 kA/cm$^2$) than the Structure-B (5 kA/cm$^2$) at $I_B$ = 500 $\mu$A. The offset voltage ($V_{offset}$) is 1.8 V and 1V for Structure-A and Structure-B respectively. The larger knee voltage ($V_{knee}$) in Structure-A (12V) than in Structure-B (5V) at $I_B$ = 100 $\mu$A indicates that the base resistance is larger in Structure-A. Figure 3 shows Gummel plots of these devices at $V_{CB}$ = 0 V. The cross-over points of $I_B$ and $I_C$ are 230 nA at $V_{BE}$ = 4.5V for Structure-A and 800 nA at $V_{BE}$ = 4.3V for Structure-B respectively. Beyond the cross-over point, the differential current gain ($h_{fe}$ ≡$dI_C/dI_B$) increases monotonically and reaches 60 at $V_{BE}$ = 13 V for the Structure-A device and 50 at $V_{BE}$ = 11 V for the Structure-B device.

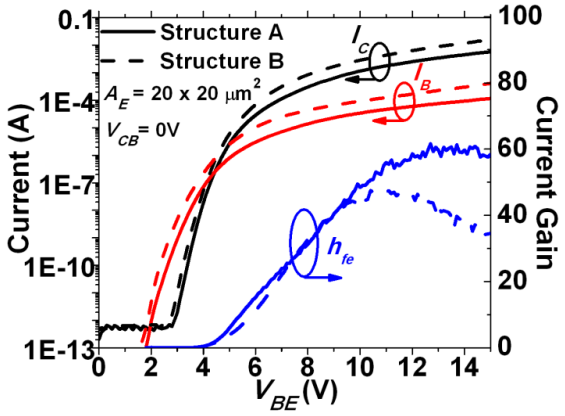


**Figure 3** The Gummel plots of a Structure-A DHBT (solid lines) and a Structure-B DHBT (dashed lines) with $A_E$ = 20 × 20 μm$^2$.

To investigate current components in the base layer of fabricated devices, normalized current density ($J_C/\beta$) is plotted against the emitter's perimeter-to-area ratio ($L_E/A_E$) to extract the perimeter-dependent surface recombination current ($K_{B,surf}$) and the area-dependent current component ($J_{Bulk}$). Figure 4 shows a plot of $J_C/\beta$ versus $L_E/A_E$ for Structure-A and Structure-B DHBTs respectively. $J_C$ was chosen to be 50 and 100 A/cm$^2$ to exclude self-heating problems. The DHBTs under evaluation have $A_E$ = 20×20, 40×40, 60×60 and 100×100 $\mu$m$^2$, respectively, for both structures. $K_{B,surf}$ is evaluated using the

linear regression fitting of $J_C/\beta$ versus ($L_E/A_E$) and $J_{Bulk}$ is extracted at the intercept of the *y*-axis (at $L_E/A_E$ = 0). The calculated $K_{B,surf}$'s and $J_{Bulk}$'s are listed in **Error! Reference source not found.**. For a given $J_C$, Structure-B devices show lower $K_{B,surf}$ than that for Structure-A devices. On the other hand, $J_{Bulk}$ values for Structure-B are always higher than those for Structure-A. The lower surface recombination current in Structure-B devices may indicate that the surface recombination velocity decreases as the indium composition increases. The increased bulk base recombination current may be attributed to increased growth-related defects such as dislocations and the V-defect formation. These results indicate that a higher indium composition in the base layer may help achieve lower base resistance and reduce the surface recombination current. These benefits however may be compromised by increased recombination centers in the base layer, resulting in lower current gain.

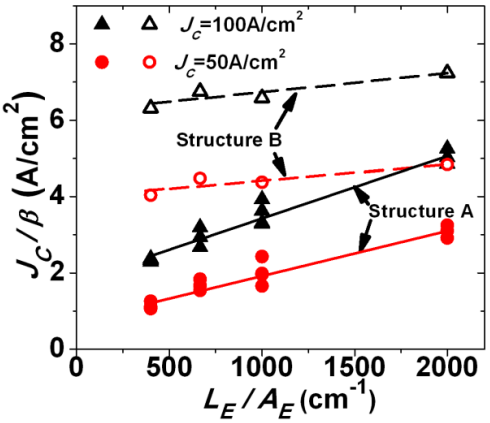


**Figure 4** A plot showing $J_C/\beta$ versus the emitter perimeter-to-area ratio ($L_E/A_E$) at $J_C$ = 50 and 100 A/cm$^2$, respectively, for Structure-A and Structure-B DHBTs.

**Table 2** A summary of extracted $J_{Bulk}$ and $K_{B,surf}$ at different $J_C$ for Structure-A and Structure-B DHBTs.

| **Device Structure** | **$J_C$ = 100A/cm$^2$** | | **$J_C$ = 50A/cm$^2$** | |
|---|---|---|---|---|
| | **$J_{bulk}$(A/cm$^2$)** | **$K_{B,surf}$(A/cm)** | **$J_{bulk}$(A/cm$^2$)** | **$K_{B,surf}$(A/cm)** |
| Structure-A | 1.79 | $1.66 \times 10^{-3}$ | 0.8 | $1.16 \times 10^{-3}$ |
| Structure-B | 6.36 | $6.1 \times 10^{-4}$ | 4.2 | $2.9 \times 10^{-4}$ |

### *II.3 GaN/In$_{0.03}$Ga$_{0.97}$N npn DHBT on sapphire and FS-GaN substrates*

To improve the power performance of GaN/InGaN DHBTs, free-standing (FS) GaN substrate could be a suitable choice because of its low dislocation density and the relatively higher thermal conductivity when compared to sapphire substrates. FS-GaN substrates also provide an advantage to grow thick GaN/InGaN HBT structure without defects and cracks induced by the lattice mismatch.

To study the impact of substrates to the DHBTs, the same structure (Structure-A) is implemented on sapphire and free-standing (FS) GaN substrates. To achieve better device performance, the fabricated samples were passivated by benzocyclobutene (BCB) to suppress the surface recombination current. The device size is also reduced from 20×20

μm$^2$ to 3×3 μm$^2$ in order to reduce the bulk recombination current and emitter crowding effect.

In Figure 5, the measured Gummel plots for a 3×3μm$^2$ GaN/InGaN DHBT ($A_E$ =11.7 μm$^2$) on GaN and sapphire substrate are shown. In this plot, $I_B$ and $I_C$ of both samples cross over at 450nA. Beyond the cross-over point, the differential current gain ($h_{fe}$ =$dI_C/dI_B$) increases and reaches the maximum of 110 and 70 at $V_{BE}$ = 11.5V respectively.

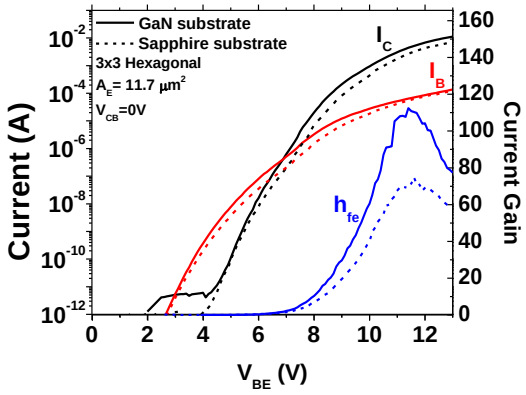


**Figure 5** The Gummel plots of a Structure-A DHBTs with $A_E$ = 3 × 3 $\mu$m$^2$ on a FS-GaN substrate (solid lines) and on a sapphire substrate (dashed lines) at room temperature.

The common-emitter current-voltage characteristics of both fabricated DHBTs are shown in Figure 6. $J_C$ > 125 kA/cm$^2$ is achieved at $I_B$ = 175 μA on GaN substrate. For the DHBT on sapphire substrate, the maximum $J_C$ is limited by the high thermal resistance and only reaches is 51kA/cm$^2$. Nevertheless, to our best knowledge, these values are the highest $J_C$ reported on fabricated GaN/InGaN DHBTs on FS-GaN and sapphire substrates to date.

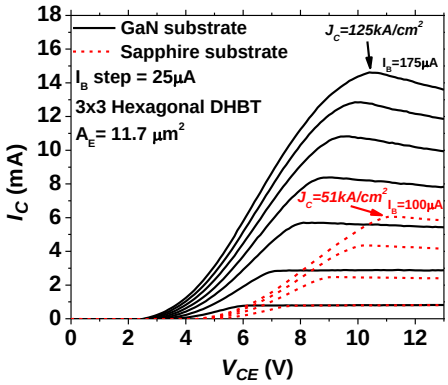


**Figure 6** The common-emitter characteristics of 3×3μm$^2$ DHBTs on FS-GaN substrate (solid lines) and on sapphire substrate (dashed lines) at room temperature.

To explore the power handling capability of the fabricated GaN/InGaN DHBTs on FS-GaN substrate, a quasi-static measurement is conducted on the same DHBT using 1 ms pulse with a repetition rate of 2 Hz (Duty cycle of 2%). The measured common-emitter characteristics are shown in Figure 7. With reduced joule heating, a maximum $J_C$ of 141 kA/cm$^2$ is measured at $V_{CE}$ = 20 V. A d.c. power density of 3.05 MW/cm$^2$ is also achieved at $V_{CE}$ = 22.5 V. The high $J_C$ characteristics is attributed to the reduced emitter-current crowding effect using a small area DHBT ($A_E$ = 11.7 μm$^2$). The use of the FS-GaN substrate also helps reduce the junction temperature due to its high thermal conductivity when compared to the sapphire substrates, which prevents premature junction failure at high current drive. To our best knowledge, the achieved $J_C$ are the highest value reported for III-N DHBTs to date.

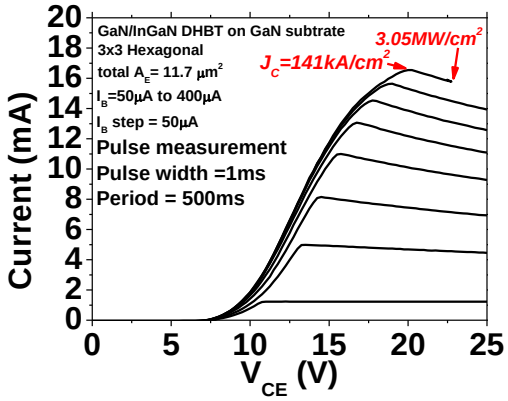


**Figure 7** A quasi-static common-emitter characteristics of a DHBT ($A_E$ =11.7 μm$^2$) grown on a GaN substrate at room temperature.

By plotting ($J_C/\beta$) versus ($L_E/A_E$), base recombination components can be extracted. The extracted values are summarized in It is noticed that the bulk recombination current ($J_{bulk}$) is significantly reduced on FS-GaN substrate while the surface recombination current ($K_{B,surf}$) is also slightly reduced. This is attributed to the low dislocation density on the FS-GaN substrate.

**Table 3** A summary of extracted $J_{Bulk}$ and $K_{B,surf}$ at different $J_C$ for GaN/InGaN DHBTs on FS-GaN and sapphire substrates.

| Device Structure | $J_C$ = 1000A/cm$^2$ | | $J_C$ = 500A/cm$^2$ | | $J_C$ = 100A/cm$^2$ | |
|---|---|---|---|---|---|---|
| | $J_{bulk}$ (A/cm$^2$) | $K_{B,surf}$ (A/cm) | $J_{bulk}$ (A/cm$^2$) | $K_{\backslash B,surf}$ (A/cm) | $J_{bulk}$ (A/cm$^2$) | $K_{\backslash B,surf}$ (A/cm) |
| FS-GaN substrate | 10.47 | 5.39E-3 | 6.52 | 3.7E-3 | 2.05 | 1.58E-3 |
| Sapphire substrate | 45.16 | 6.4E-3 | 28.18 | 4.22E-3 | 9.96 | 1.78E-3 |

### *II.4 High temperature (250C) operation on FS-GaN substrate*

High-temperature applications of GaN-based transistors are one of the important research fields. It has been reported that GaN-based HEMTs can be operated at 1000 °C. Therefore, III-N HBTs are expected to have the capability to operate at high temperature

with high-power density and high current density. In Georgia Tech, Structure-A GaN/InGaN *npn* DHBTs are fabricated on FS-GaN substrate and measured on a temperature controlled chuck to study the impact of high temperature to the device performance and breakdown mechanism.

In Figure 8, the Gummel plots for a 40 × 40 μm$^2$ GaN/InGaN DHBT on FS-GaN substrate at 250C and room temperature(25C) are shown. In this plot, $I_B$ and $I_C$ cross over at 3.28 μA and 1.68 μA at 250C and 25C respectively. Beyond the cross-over point, the differential current gain ($h_{fe}$ =$dI_C/dI_B$) increases and reaches the maximum of 115 and 43 at $V_{BE}$ = 11.2V. It is worth to note that the base current is significantly increased at 250C in Figure 8. This indicates that the free-hole concentration is increased at 250C due to enhanced Mg ionization efficiency in the base layer. The reduced current gain is attributed to the increased trap-state recombination rate and possibly a lower emitter injection efficiency caused by the higher free-hole concentration at 250C.

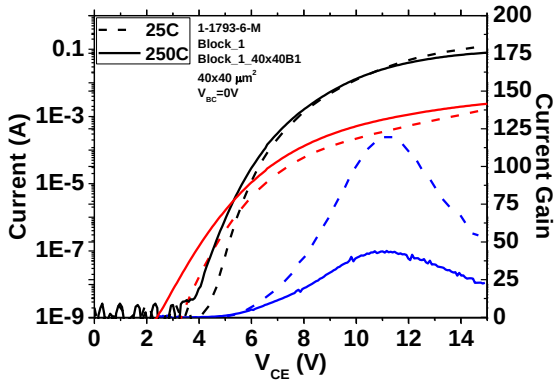


**Figure 8** The Gummel plots of a Structure-A DHBTs with $A_E$ = 40 × 40 μm$^2$ on a FS-GaN substrate at 250C (solid lines) and 25C (dashed lines).

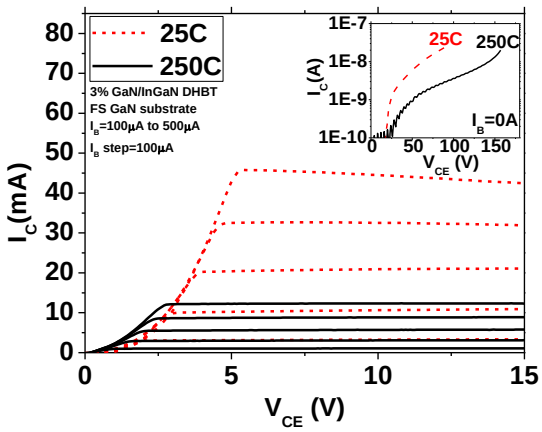


**Figure 9** The common-emitter characteristics of a DHBT with $A_E$ = 40 × 40 μm$^2$ grown on FS-GaN substrate at 25C (dashed lines) and 250C (solid lines).

The measured common-emitter current-voltage characteristics are shown in Figure 9. The results show that the offset voltage is reduced from 0.8 V at 25C to 0.3 V at 250C. Similarly, the knee voltage is reduced from 5.2 to 2.75 V at $I_B$ = 500 μA as the

temperature increases from 25C to 250C. The improvement of the offset voltage and the knee voltage are attributed to the reduction in base resistance at high temperature.

The $BV_{CEO}$ of the device at different temperature is shown in the inset of Figure 9. The current compliance is kept at 20 nA ($J_C$ = 1.25 mA/cm$^2$) to prevent possible damage to the device at high voltage. The results show that $BV_{CEO}$ increases from 90 V to 157 V as the temperature progresses from 25C to 250C. The positive temperature coefficient for $BV_{CEO}$ indicates that the impact ionization process is the major breakdown mechanism for the fabricated GaN/InGaN DHBTs grown on a FS-GaN substrate.

### *II.5 Burn-in effect in GaN/In$_{0.03}$Ga$_{0.97}$N npn DHBTs on sapphire substrate*

"Burn-in effect" is commonly observed in MOCVD-grown InP/InGaAs or InGaP/GaAs HBTs. It is concluded that the burn-in effect is related to the hydrogen passivation in the base layer. It is also known that the hydrogen passivation may be significant in MOCVD-grown Mg-doped *p*-type III-N epitaxial layers. Atomic hydrogen forms complexes with Mg in *p*-type III-N materials and the free-hole activation of InGaN:Mg can be achieved using a post-growth annealing step .To study the burn-in effect in GaN/InGaN DHBTs, a post-processing current stressing (the "burn-in") is also applied on fabricated DHBTs to reduce or eliminate the hydrogen passivation in the *p*-type base layer.

As shown in Figure 10, a Structure-B DHBT ($A_E$ = 20×20 μm$^2$) was stressed at $I_B$ = 200 $\mu$A and $V_{CE}$ =15V for a period of 50. $V_{BE}$ and $I_C$ were sampled every 5 seconds during the constant-current stressing period. It is observed that $I_C$ first increased and then reached a stabilized value of 9.7 mA beyond $t$ > 30 min. At the same time, $V_{BE}$ drops slightly from 12.4 V at $t$ = 0 to 12 V for $t$ > 20 min. After the 50-minute constant-base-current stressing, the peak $h_{fe}$ was increased from 42 to 66 and stayed unchanged afterward for > 1 month.

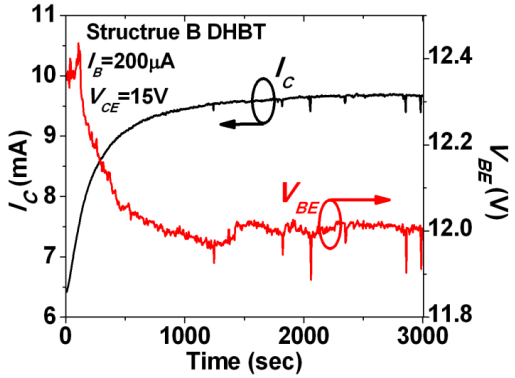


**Figure 10** A time-dependent $I_C$ and $V_{BE}$ measure for a Structure-B DHBT with $A_E$ = 20 × 20 $\mu$m$^2$ under constant base current stressing ($I_B$ = 200 $\mu$A).

Using the ($J_C/\beta$) versus ($L_E/A_E$) plot, the recombination current components were then extracted and compared with those obtained prior to the device burn-in at $J_C$ = 100A/cm$^2$, as shown in Figure 11. The result shows that $K_{B,urf}$ remains approximately unchanged before and after the current stressing. However, $J_{Bulk}$ is reduced from 6.2 A/cm$^2$ to 3.8A/cm$^2$ after the burn-in. Among the three current components in $J_{Bulk}$, the junction

properties are assumed to remain unchanged under the relatively low current stressing. In other words, the barrier height and the recombination centers that arising from the growth-related defect densities may not be altered after the burn-in step. As a result, the reduction in $J_{Bulk}$ through the device burn-in step suggests that the hydrogen passivation in the p-type region is alleviated. It is then expected that the base layer should also have higher free-hole concentration after the device burn-in.

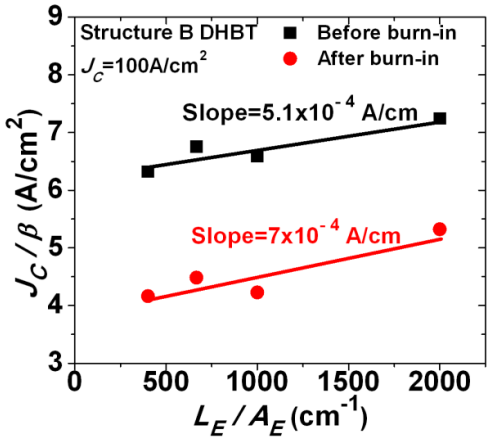


**Figure 11** ($J_C/\beta$) plotted against ($L_E/A_E$) for a Structure-B DHBT before and after the device burn-in procedure.

To verify this hypothesis, small-signal capacitance-voltage (C-V) measurements were performed for both BE and BC junctions before and after the device burn-in. Since the emitter is degenerately doped ($2\times10^{19}$ cm$^{-3}$), the emitter electron concentration is at least one order of magnitude higher than the free-hole concentration in the base. Consequently, the depletion width of the BE junction falls mostly in the base layer. Similarly, the depletion region of the BC junction will fall mostly in the lightly-doped collector region. The free-carrier concentration of the lightly-doped semiconductor layer ($N$) in the one-sided abrupt junction can therefore be estimated as:

$$\frac{1}{C^2} = \frac{1}{A^2}\cdot\frac{2}{q\varepsilon_s\varepsilon_0 N}\left(V_{bi} - V\right),$$

where $\varepsilon_0$ is the free-space permittivity, $A$ is the junction area $V_{bi}$ is the built-in potential that includes the heterojunction bandgap discontinuity, and $\varepsilon_s$ is the relative permittivity of the lower-doped side of the junction. $p_B$ can be determined by the slope of the $1/C^2$ curve for the reverse-biased BE junction. Likewise, $n_C$ can be determined from the slope of $1/C^2$ for the BC junction.

Figure 12 shows $1/C^2$ curves for the reverse-biased BE junction and the BC junction, respectively, for a Structure-B DHBT with $A_E$ = 40×40 μm$^2$ and $A_C$= 65×100 μm$^2$. The C-V measurement is carried out in a LCR meter (Agilent 4284A) at a frequency of 1 MHz. Before the burn-in step, $p_B$ is $8.76\times10^{17}$ cm$^{-3}$ and $n_C$ is $1.1\times10^{17}$ cm$^{-3}$. After the constant base-current stressing, $p_B$ is increased to $1.16\times10^{18}$ cm$^{-3}$, which corresponds to > 25% increase in the free hole concentration. On the other hand, the $1/C^2$ curve and $n_C$ for the BC junction remain approximately unchanged, indicating that the BC junction

remains an abrupt *p-n* junction after the device burn-in. The extracted $V_{bi}$ for the BE junction is ~ 4.1 V and that for the BC junction is 4.3 V.

In Figure 13, two sets of common-emitter family curves for a Structure-A GaN/InGaN DHBT are plotted for comparison. The device has $A_E$ = 20×20 μm$^2$ and the burn-in step was carried out at $I_B$ = 200 μA and $V_{CE}$ = 15 V. It can be seen that the collector current drive is greatly improved after the device burn-in. For example, $I_C$ is increased from 5 mA to 8.4 mA at $I_B$ = 100 μA, which shows > 60% of increase in $I_C$. $V_{knee}$ is reduced from 12 V to 10 V at $I_B$ = 100 μA and $I_C$ reaches >26 mA ($J_C$ > 6.5 kA/cm$^2$) at $I_B$ = 500 μA. The Gummel plots before and after the device burn-in procedure are also shown in Figure 14. After the device burn-in, the peak $h_{fe}$ is improved from 60 to 105 and $V_{BE}$ at which the peak current gain occurs is reduced from 13 V to 10 V. The reduction in the knee voltage is also observed after burn-in step, indicating that the base series resistance is reduced due to the increased free-hole concentration.

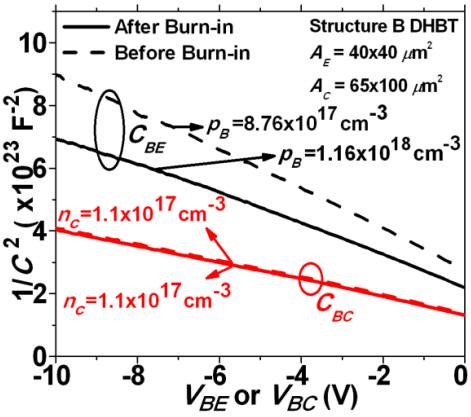


**Figure 12** A plot showing $1/C^2$ versus $V$ for the BE and the BC junctions of a Structure-B DHBT with $A_E$ = 40 × 40 μm$^2$ before (dashed lines) and after (solid lines) the device burn-in.

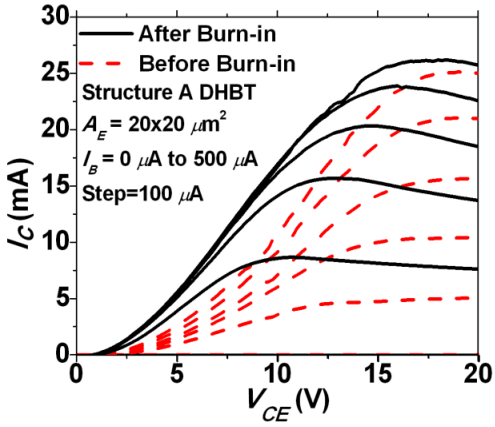


**Figure 13** The common-emitter characteristics of a Structure-A DHBT with $A_E$ = 20 × 20 μm$^2$ before (dashed lines) and after (solid lines) the device burn-in.

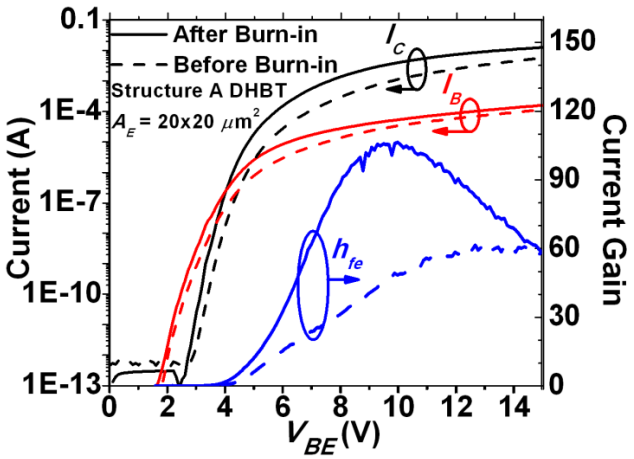


**Figure 14** A Gummel plot of a Structure-A DHBT with $A_E$ = 20 × 20 μm$^2$ before (dashed lines) and after (solid lines) the device burn-in.

### *II.6 RF GaN/In$_{0.03}$Ga$_{0.97}$N npn DHBT on sapphire substrate*

For RF applications, HBTs can provide more uniform turn-on characteristics and higher power density than high electron mobility transistors (HEMTs). With wider bandgap, III-N HBTs are expected to provide superior breakdown voltage than InP/InGaAs or InGaP/GaAs HBTs. Today, it is common to see reports of III-N HEMTs with high cut-off frequencies greater than 200 GHz. The development of III-N HBT technologies, however, has been less successful due to technological barriers in the growth and the fabrication of III-N bipolar transistors.

In Georgia Tech, the high-quality epitaxial growth and optimized processing techniques developed have improved d.c performance of *npn* GaN/InGaN DHBTs. With these techniques, we successfully demonstrated a DHBT with a cut-off frequency ($f_T$) > 5 GHz and a maximum oscillation frequency ($f_{max}$) > 1.3 GHz.

Structure-A GaN/InGaN *npn* DHBTs is implemented on *c*-plane sapphire substrate and processed with the same optimized processing techniques reported in previous sections. The base contact is placed in close proximity to the emitter mesa (< 0.8 μm) to reduce the extrinsic base resistance. A narrow-emitter stripe is also used to reduce the location-dependent variation of the junction voltage.

The fabricated DHBTs are characterized in Keitkely semiconductor characterization system (SCS-4200) for d.c performance before S-parameter measurement. The S-parameters are measured in an Anritsu 37397D Vector Network Analyzer from 40 MHz to 20 GHz at room temperature. The devices are measured in the common-emitter coplanar waveguide (CPW) configuration. On-wafer short-open-load-through (SOLT) calibrations are used to move the RF reference planes to the lines indicated in Figure 15.

In Figure 16, the frequency-dependent $|h_{21}|^2$, the Mason's unilateral gain (*U)*, and *MAG* are measured at $V_{CE}$ = 7 V and $J_C$ = 4.7 kA/cm$^2$ for a DHBT with $A_E$ = 4×20 μm$^2$. An asymptotic 20 dB/decade line fitting is drawn on the measured $|h_{21}|^2$ curve and $f_T$ of 5.3 GHz is determined. A study of the small signal model of the device suggests that the high-frequency tailing of the $|h_{21}|^2$ curve (i.e. the deviation of the 20 dB/decade roll-off at

high frequency regime) was partly due to the capacitive coupling between the collector and the emitter. This parasitic component comes from the extensive overlay of the emitter ground plane metal and the underlying thick (2500 nm) unintentionally doped ($n \approx 10^{16}$ cm$^{-3}$) GaN buffer layer that electrically connects to the sub-collector in the common-emitter CPW design. $f_{max}$ of 1.3GHz is determined at $U$ = 0 dB. The device is unconditionally stable for frequencies up to 20GHz. $U$ does not show the 20 dB/decade roll-off characteristics as seen in typical HBTs. It is because the curve is still transitioning from the low-frequency gain region to the high-frequency roll-off region before it reaches the unit-gain frequency.

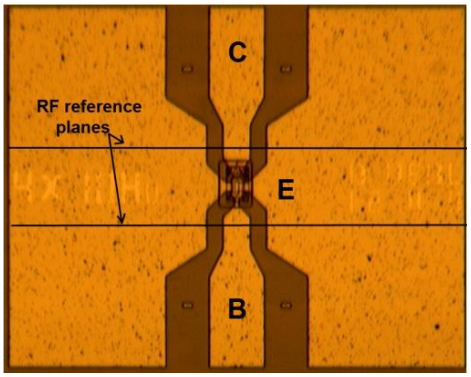


**Figure 15** A microscope picture of a fabricated GaN/InGaN DHBT with $A_E$ = 4 × 10 μm$^2$. The device is designed in G-S-G coplanar waveguide configuration for common-emitter RF measurement.

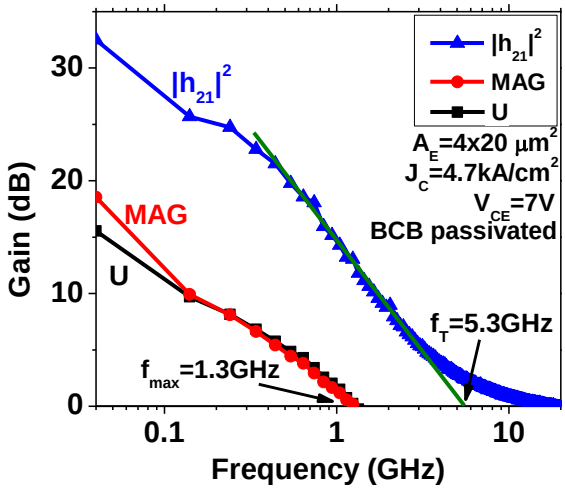


**Figure 16** The measured $|h_{21}|^2$, *MAG*, and *U* of a GaN/InGaN DHBT with $A_E$ = 4×20μm$^2$.

The $J_C$-dependent $f_T$ and $f_{max}$ values of the 4×20 μm$^2$ HBT are plotted in Figure 17. $f_T$ increases monotonically with $J_C$ and reaches the maximum value of 5.3GHz at $J_C$ > 5 kA/cm$^2$. A similar trend is found for $f_{max}$. For $J_C$ > 3 kA/cm$^2$, $f_{max}$ also reaches its maximum value of 1.3GHz. When plotting $\tau_{ec}$ (= $1/(2\pi f_T)$) against $1/I_C$ (the inset of Figure 17), the sum of the base-to-collector transit time and the collector RC charging

time is estimated at 26 ps when one linearly extrapolates the curve to $1/I_C = 0$. However, the devices suffer from thermal runaway and catastrophic damage at higher current stressing condition and hence the RF characteristics were not measured on these HBTs on sapphire substrates for $J_C > 7$ kA/cm$^2$. Possible RF performance improvements for GaN/InGaN HBTs include further reduction in the base resistance and growing these structures on substrates with better thermal conductivity for high-current operation.

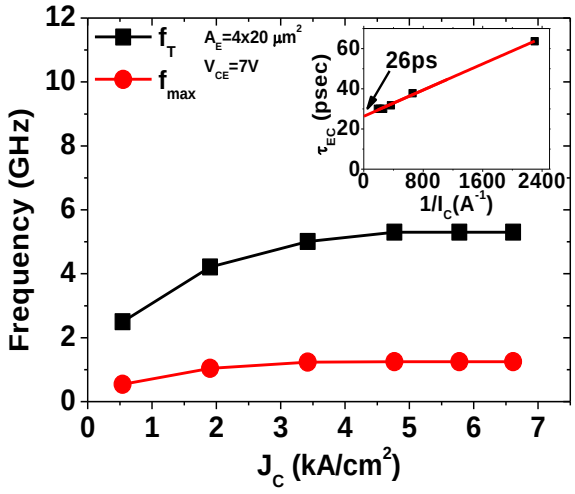


**Figure 17** The $f_T$ and $f_{max}$ of a GaN/InGaN DHBT $A_E$ = 4×20 μm$^2$ at different collector density ($J_C$).

### II.7 Modeling and Simulation of SPSL-Base HBTs

Efficient power amplification at high frequencies depends critically upon achieving sufficient lateral conductivity within the base region. Due to a high activation energy, a large chemical concentration of Mg dopant atoms does not guarantee large free hole concentrations at room temperature, making the goal of low base resistance particularly challenging. One strategy for improving lateral conductivity within the base region is the use of a superlattice. If the valence band discontinuity of an SPSL base is comparable to the dopant activation energy (for Mg in GaN it is thought to be between 170 and 200 meV), a substantial fraction of dopant atoms in the barrier material may be electrically active by virtue of adjacent quantum confined hole states in the well regions. In the following paragraphs, we summarize the results of our comparative study of SPSL base HBT designs using AlGaN and InGaN ternary materials.

The epitaxial layer structures that have been used for both homogenous and SPSL base designs are as follows:

| Layer Name | Material for AlGaN HBT | Material for AlGaN/InGaN SPSL HBT | Doping ($cm^{-3}$) | Thickness (micron) | Lateral Length (micron) |
|---|---|---|---|---|---|
| Emitter | $AL_{0.25}GaN$ | $AL_{0.25}GaN$ | $1x10^{18}$ | 0.3 | 2 |
| E-B Grading | $AL_{0.25\sim0.21}GaN$ | $AL_{0.25\sim0.21}GaN$ | $1x10^{16}$ | 0.03 | 2 |
| Base | $AL_{0.25}GaN$ | $AL_{0.25}GaN/In_{0.18}GaN$ | $3x10^{19}$ | 0.058 | 4 |
| C-B Grading | $AL_{0.21\sim0.25}GaN$ | $AL_{0.21\sim0.25}GaN$ | $1x10^{16}$ | 0.03 | 4 |

| | | | | | |
|---|---|---|---|---|---|
| Collector | $AL_{0.25}GaN$ | $AL_{0.25}GaN$ | $1x10^{17}$ | 0.4 | 4 |
| Subcollector | $AL_{0.25}GaN$ | $AL_{0.25}GaN$ | $5x10^{18}$ | 0.6 | 6 |
| Substrate | GaN | GaN | | | |

**Table 4. Epitaxial Layer Structure for AlGaN HBT and AlGaN/InGaN SPSL HBT**

The device structure used for both the AlGaN HBT and the AlGaN/InGaN SPSL HBT is shown below in Figure 18. Lateral dimensions have been scaled for numerical simplicity. Figure 19 documents the corresponding band diagrams.

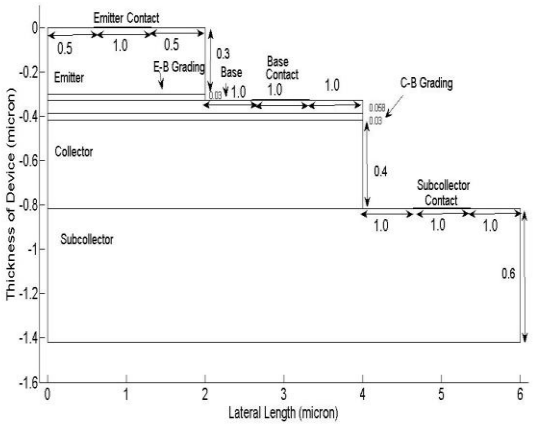


**Figure 18 Cross-section of AlGaN HBT (reference) and AlGaN/InGaN SPSL HBT.**

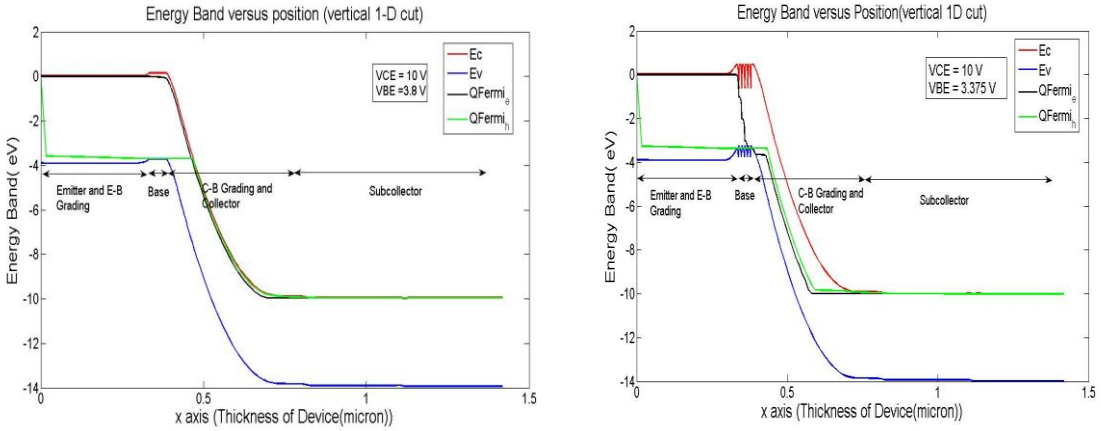


**Figure 19 Band diagrams of AlGaN and AlGaN/InGaN SPSL HBTs**

..

We consider first AlGaN/InGaN short period superlattice HBTs. The base region of this device consists of 5 quantum wells and 6 barriers. The activiation energy of the Mg dopant used in the base region is approximately 170 meV. Therefore, if the valence band discontinuity between base barrier region and base well region approaches or exceeds the dopant activation energy, then a substantial fraction of Mg dopants within the barrier region may be ionized as a result of the accessible states for holes at lower energies within the adjacent well regions. In order to achieve this phenomenon, the material composition of the base, well and base barrier must be chosen carefully.

The epitaxial layer structure for the base region of the AlGaN/InGaN SPSL HBT considered in this report is shown in the table below:

| Layer Name | Material | Thickness (micron) |
|---|---|---|
| Base 1st Barrier | $Al_{0.21}GaN$ | 0.008 |
| Base 1st well | $In_{0.18}GaN$ | 0.002 |
| Base 2nd Barrier | $Al_{0.21}GaN$ | 0.008 |
| Base 2nd well | $In_{0.18}GaN$ | 0.002 |
| Base 3rd Barrier | $Al_{0.21}GaN$ | 0.008 |
| Base 3rd well | $In_{0.18}GaN$ | 0.002 |
| Base 4th Barrier | $Al_{0.21}GaN$ | 0.008 |
| Base 4th well | $In_{0.18}GaN$ | 0.002 |
| Base 5th Barrier | $Al_{0.21}GaN$ | 0.008 |
| Base 5th well | $In_{0.18}GaN$ | 0.002 |
| Base last Barrier | $Al_{0.21}GaN$ | 0.008 |

**Table 5** Epitaxial layer structure for AlGaN/InGaN base region of AlGaN/InGaN SPSL HBT.

In the case of the SPSL base design, we observe a valence band discontinuity of approximately 200 meV within the SPSL. From Figure 20, depicting mobile hole density, it is clear that hole concentration within the well regions is much higher than in the barrier regions, with a peak value of approximately $2x10^{20}$ $cm^{-3}$. In spite of the fact that the narrow-gap well material represents only a fraction of the thickness of the base, the short period superlattice design achieves a higher mobile hole concentration in the base than does the reference homogeneous based design with the same uniform doping level of $3x10^{19}$ $cm^{-3}$.

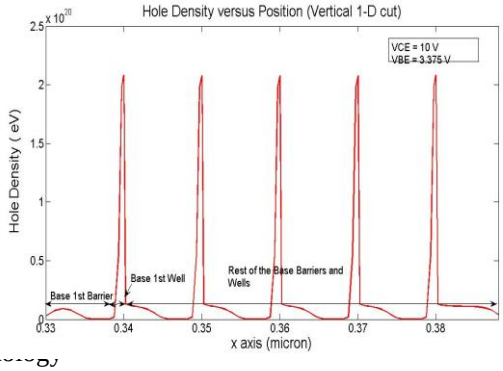


**Figure 20** Hole density profile of AlGaN/InGaN SPSL HBT in base region at C-E voltage of 10 V and B-E voltage of 3.8 V

Figure 21 depicts the conduction band diagram and electron density in base region of the SPSL design. It is clear that the SPSL design is characterized by a very large conduction band discontinuity of approximately 0.8 eV, resulting in exceedingly high electron trapping and subsequent recombination in the first quantum well. The situation can be improved by lowering the conduction band discontinuity energy.

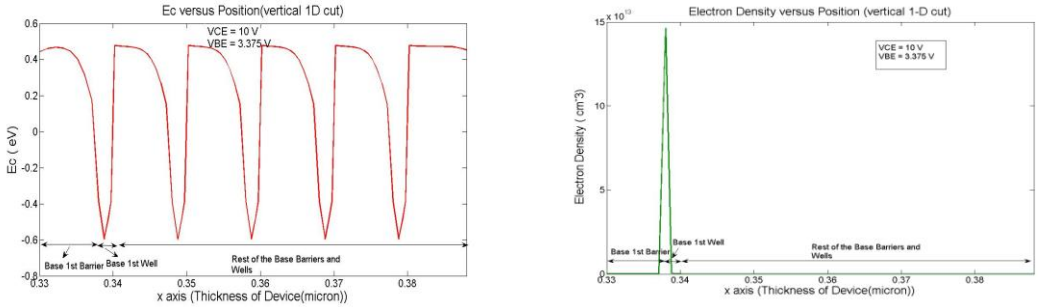


**Figure 21** Conduction Band diagram (left) and electron density (right) of AlGaN/InGaN SPSL HBT in base region.

The lateral conductivity (integrated average) in the base regions of the AlGaN and AlGaN/InGaN SPSL HBTs are $2.0347 \times 10^4$ $\Omega^{-1}$ $m^{-1}$ and $1.1033 \times 10^5$ $\Omega^{-1}$ $m^{-1}$, respectively. In the calculation of lateral conductivity, detailed spatial variation of the hole mobility and hole density has been considered. We observe that the SPSL base design exhibits significantly lower base resistance than the homogeneous base HBT.

We next present SPSL HBT simulation results for both AlGaN/InGaN and InGaN/InGaN structures. The epitaxial layer used for these above two SPSL HBTs having 5 quantum wells and 6 quantum barriers in base is shown in Table 6 below:

| Layer Name | Material for AlGaN/InGaN SPSL HBT | Material for InGaN/InGaN SPSL HBT | Doping ($cm^{-3}$) | Thickness (micron) | Lateral Length (micron) |
|---|---|---|---|---|---|
| Emitter | $AL_{0.3}GaN$ | GaN | $8 \times 10^{18}$ | 0.07 | 1 |
| E-B Grading | $AL_{0.3\sim0.28}GaN$ | $In_{0\sim0.1}GaN$ | $1 \times 10^{16}$ | 0.03 | 1 |
| Base | $AL_{0.28}GaN/In_{0.18}GaN$ | $In_{0.1}GaN/In_{0.13}GaN$ | $2 \times 10^{19}$ | 0.046 | 2 |
| C-B Grading | $AL_{0.28\sim0.3}GaN$ | $In_{0.1\sim0.0}GaN$ | $1 \times 10^{16}$ | 0.03 | 2 |
| Collector | $AL_{0.28}GaN$ | GaN | $5 \times 10^{17}$ | 0.15 | 2 |
| Subcollector | $AL_{0.28}GaN$ | GaN | $7 \times 10^{18}$ | 0.15 | 2.75 |
| Substrate | GaN | GaN | | | |

**Table 6** Epitaxial layer structure for both $AL_{0.28}GaN/In_{0.18}GaN$ and $In_{0.1}GaN/In_{0.13}GaN$ SPSL HBT.

The device cross-section used for both SPSL HBTs is shown below:

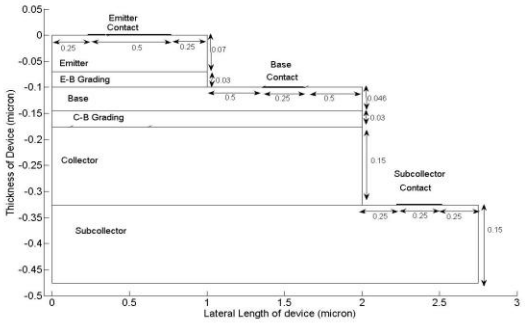


**Figure 22** Layout of both AlGaN/InGaN SPSL HBT and InGaN/InGaN SPSL HBT

The detailed epitaxial layer structures in the base regions for both the AlGaN/InGaN and InGaN/InGaN SPSL HBTs are shown in the table below:

| Layer Name | Material for AlGaN/InGaN SPSL HBT | Material for InGaN/InGaN SPSL HBT | Thickness (micron) | Doping level (meV) |
|---|---|---|---|---|
| Base 1st Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |
| Base 1st well | $In_{0.18}GaN$ | $In_{0.13}GaN$ | 0.002 | 170 |
| Base 2nd Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |
| Base 2nd well | $In_{0.18}GaN$ | $In_{0.13}GaN$ | 0.002 | 170 |
| Base 3rd Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |
| Base 3rd well | $In_{0.18}GaN$ | $In_{0.13}GaN$ | 0.002 | 170 |
| Base 4th Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |
| Base 4th well | $In_{0.18}GaN$ | $In_{0.13}GaN$ | 0.002 | 170 |
| Base 5th Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |
| Base 5th well | $In_{0.18}GaN$ | $In_{0.13}GaN$ | 0.002 | 170 |
| Base last Barrier | $Al_{0.28}GaN$ | $In_{0.1}GaN$ | 0.004 | -5 |

**Table7**. Epitaxial layer structure for both AlGaN/InGaN and InGaN/InGaN SPSL HBT in base region.

The valence band diagram and corresponding hole density profile for the $Al_{0.28}GaN/In_{0.18}GaN$ structure are shown below:

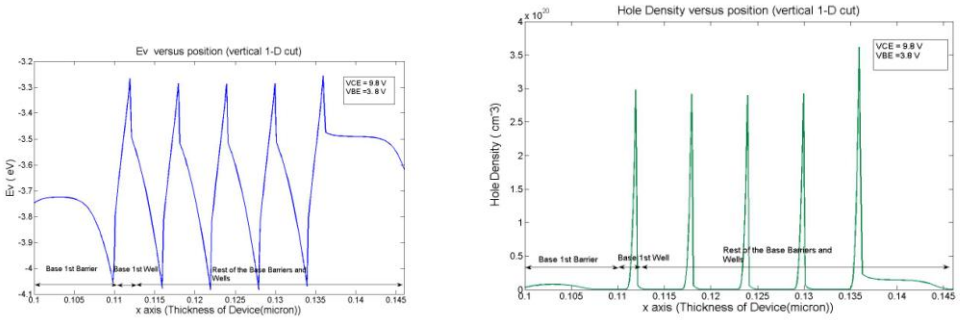


**Figure 22** Valence Band diagram (left) and hole density profile (right) of $Al_{0.28}GaN/In_{0.18}GaN$ SPSL HBT at C-E voltage of 9.8 V and B-E voltage of 3.8 V

From Figure 22, we observe that the valence band discontinuity in the base exceeds 210 meV for $Al_{0.28}GaN/In_{0.18}GaN$ SPSL HBT, a precondition for high lateral conductivity.

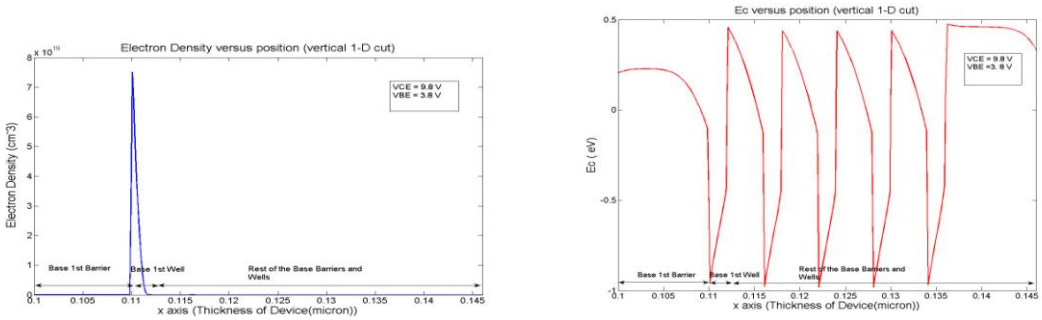


**Figure 23** Conduction Band diagram (left) and electron density profile (right) of $Al_{0.28}GaN/In_{0.18}GaN$ SPSL HBT in base at C-E voltage of 9.8 V and B-E voltage of 3.8V

For this same structure, however, it is again visible in Figure 23 that most injected minority electrons are effectively trapped by the first quantum well. Again, the large conduction band discontinuity is responsible for a high electron recombination rate, and low current gain.

We next present results for the $In_{0.1}GaN/ In_{0.13}GaN$ SPSL HBT design. From the conduction band and electron density profiles depicted in Figure 24, it is observed that the $In_{0.1}GaN/ In_{0.13}GaN$ SPSL HBT has a conduction band discontinuity of around 80 meV. As a result, the amount of trapped electrons inside the base well substantially reduced. Also, we see from the electron density profile that a substantial fraction of injected minority electrons reach the collector, resulting in a dramatic improvement in current gain.

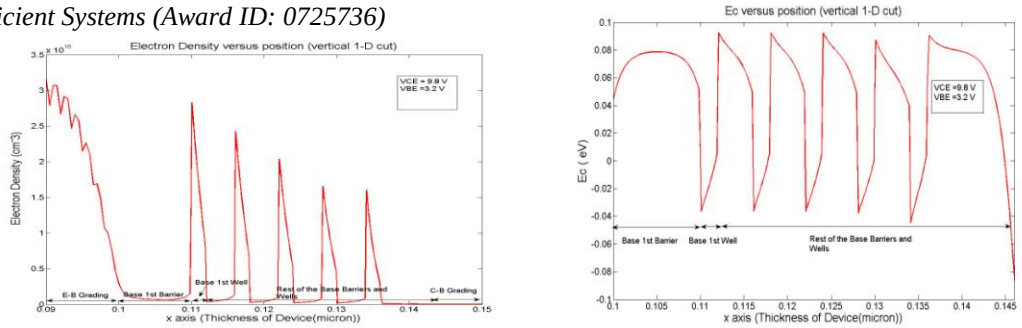


**Figure 24** Conduction Band diagram (left) and electron density profile (right) of $In_{0.1}GaN/In_{0.13}GaN$ SPSL HBT in base at C-E voltage of 9.8 V and B-E voltage of 3.2V

We observe that SPSL-base HBT designs can improve the base lateral conductivity, albeit with several design hurdles to overcome. The valence band discontinuity in the base must be comparable with the dopant activation energy, while the conduction band discontinuity and width of the base well must be optimized to minimize the trapping and subsequent recombination of injected electrons within the base.

### II.8 Device Technology Development Summary

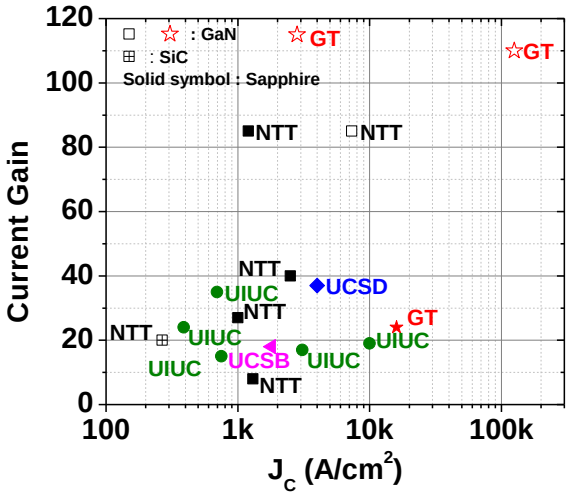


**Figure 25** A comparison chart showing the current gain versus $J_C$ of reported III-N HBTs grown on different substrates.

In Summary, Georgia Tech team has demonstrated a robust direct-grown GaN-InGaN *npn* DHBTs with high current gain (>115), high current density (>141kA/cm$^2$) and high power density (>3MW/cm$^2$). In Figure , a comparison of reported III-N HBTs is shown. Among the reported III-N HBTs, our GaN/InGaN npn DHBTs show the highest current gain and current density. We also demonstrated that GaN/InGaN DHBTs are capable to operate at 250C with current gain of 43 and breakdown voltage of 157C. With this technique, a RF GaN/InGaN DHBT is also demonstrated with cut-off frequency $f_T$ = 5.3GHz and $f_{max}$ = 1.3GHz.

## III EDUCATIONAL ACTIVITIES SUMMARY

The funding was used to partially support several graduate students throughout the projects. Five undergraduate research students were also involved in the III-Nitride device research project during the period of program supported by the Georgia Tech's undergraduate research program (UROP) and NSF-funded Summer Undergraduate Research Experience (SURE) program. The research outcome yielded seven journal publications and 12 presentations in refereed technical conferences. One book chapter was formulated and contributed in "Nano-Semiconductor: Device and Technology" (Taylor and Francis, Editor: Kris Iniewski, in press). The most recent results of InGaN HBT with $f_T$ > 5 GHz were also highlighted in the Compound Semiconductor magazine.

## IV A LIST OF PUBLICATIONS

**Book Chapter:**

1. S.-C. Shen, J.-H. Ryou, and R. D. Dupuis, "III-N Heterojunction Bipolar Transistor Technologies," in "*Nano-Semiconductors: Devices and Technology*", Editor: Kris Iniewski, Publisher: Taylor and Francis, LLC, in press.

**Refereed Journal Publications:**

1. S.-C. Shen, Y.-C. Lee, H.-J. Kim, Y. Zhang, S. Choi, R. D. Dupuis, and J.-H. Ryou, "Surface leakage in GaN/InGaN double heterojunction bipolar transistors," *IEEE Electron Device Letters*, vol. 30, no 11, pp. 1119-1121, November, 2009.
2. Y.-C. Lee, H.-J. Kim, Y. Zhang, S. Choi, R. D. Dupuis, J.-H. Ryou, and S.-C. Shen, "High-performance GaN/InGaN heterojunction bipolar transistors using a direct-growth approach," *Phys. Status Solidi C*, vol. 7, No. 7–8, pp. 1970–1973, May, 2010.
3. Y.-C. Lee, Y. Zhang, H.-J. Kim, S. Choi, Z. Lochner, R. D. Dupuis, J.-H. Ryou, and S.-C. Shen, "High-current-gain direct-growth GaN/InGaN double heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, Vol. 57, No. 11, pp. 2964-2969, November 2010.
4. Z. Lochner, H.-J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, S.-C. Shen, J.-H. Ryou, and R. D. Dupuis, "Growth and characterization of NpN heterojunction bipolar transistors with $In_{0.03}Ga_{0.97}N$ and $In_{0.05}Ga_{0.95}N$ bases," *Journal of Crystal Growth*, vol. 315, no. 1, pp. 278-282, 2011.
5. Y. Zhang, Y. Lee, Z. Lochner, H. Kim, S. Choi, J.-H. Ryou, R. D. Dupuis, and S.-C. Shen, "High-Performance GaN/InGaN double heterojunction bipolar transistors on with power density > 240 kW/cm$^2$," *Physica Status Solidi (c)*, vol. 8, no. 7-8, pp. 2451-2453, 2011.
6. S.-C. Shen, R. D. Dupuis, Y.-C. Lee, H.-J. Kim, Y. Zhang, Z. Lochner, P. D. Yoder, and J.-H. Ryou, "GaN/InGaN Heterojunction Bipolar Transistors with $f_T$ > 5 GHz," *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1065-1067, August 2011.
7. Z. Lochner, H.-J. Kim, Y.-C. Lee, Y. Zhang, S. Choi, S.-C. Shen, P. D. Yoder, J.-H. Ryou, and R. D. Dupuis, "*NpN*-GaN/InGaN/GaN heterohunction bipolar

transistor on free-standing GaN substrate," submitted to *Applied Physics Letters* on May, 16. 2011 (revision submitted in August, 2011).

**Conference Presentations**

1. Y. Zhang, M. Britt, J.-H. Ryou, R.D. Dupuis, and S.-C. Shen, "A surface treatment technique for III-N device fabrication," in the *Digest of Papers, 2008 CS MANTECH conference*, p. 13.3, Chicago, IL, April 16, 2008.
2. Y.-C. Lee, S.-C. Shen, H.-J. Kim, Y. Zhang, S. Choi, J.-H. Ryou, and R. D. Dupuis, "High performance GaN/InGaN heterojunction bipolar transistors using a direct-growth approach," presented at the *8th International Conference on Nitride Semiconductors (ICNS-8)*, Jeju, Korea, Oct. 18-23, 2009.
3. Y.-C. Lee, H.-J. Kim, S. Choi, R. D. Dupuis, J.-H. Ryou, and S.-C. Shen, "A study on the base recombination current in *npn* GaN/InGaN DHBTs using a direct-growth technique," in the *Digest of the 2010 CSMANTECH Conference*, pp. 211-214, Portland, OR, May 17-21, 2010.
4. Z. Lochner, H.-J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, J.-H. Ryou, S.-C. Shen, R. Dupuis, "Growth and characterization of *npn* heterojunction bipolar transistors with $In_xGa_{1-x}N$ bases," presented at the *15th International Conference on Metal Organic Vapor Phase Epitaxy*, Lake Tahoe, NV, May 23-28, 2010.
5. Z. Lochner, H. J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, J.-H. Ryou, S.-C. Shen, and R. D. Dupuis, "Growth and characterization of InGaN heterojunction bipolar transistors" (L9), presented at the *52nd Electronic Materials Conference (EMC 2010)*, Notre Dame, Indiana, June 2010.
6. Z. Lochner, H.-J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, J.-H. Ryou, S.-C. Shen, and R. D. Dupuis, "Growth and characterization of InGaN/GaN Heterojunction bipolar transistors," presented at the *International Workshop on Nitride Semiconductors 2010*, Tampa, Florida, September 19-24, 2010.
7. Y. Zhang, Y. Lee, Z. Lochner, H. Kim, S. Choi, J.-H. Ryou, R. D. Dupuis, and S.-C. Shen, "GaN/InGaN double heterojunction bipolar transistors on sapphire substrates with current gain > 100, $J_C$ > 7.2 kA/cm$^2$, and power density > 240 kW/cm$^2$," presented at the *International Workshop on Nitride Semiconductors 2010*, Tampa, Florida, September 19-24, 2010.
8. Y. Zhang, Y.-C. Lee, Z. Lochner, H. J. Kim, J.-H. Ryou, R. D. Dupuis, and S.-C. Shen, "GaN/InGaN heterojunction bipolar transistors with collector current density > 20 kA/cm$^2$," presented at the *2011 CSMANTECH Conference*, Palm Springs, CA, May 16-19, 2011.
9. Z. Lochner, H. J. Kim, Y. Zhang, S. Choi, Y.-C. Lee, J.-H. Ryou, S.-C. Shen, and R. D. Dupuis, "Growth and characterization of npn-GaN/InGaN/GaN double-heterojunction bipolar transistors on a free-standing GaN substrate" (H10), presented at the *53rd Electronic Materials Conference (EMC 2011)*, Santa Barbara, California, June 2011.
10. Y.-C. Lee, Y. Zhang, Z. Lochner, H.-J. Kim, J. H. Ryou, R. D. Dupuis, and S.-C. Shen, "Ultra-high-power characteristics of GaN/InGaN HBTs," presented at the *9th International Conference on Nitride Semiconductors* (*ICNS-9*), Glasgow, UK, July 10-15, 2011.
11. Z. Lochner, H.-J. Kim, Y. Zhang, Y.-C. Lee, S. Choi, S.-C. Shen, P. D. Yoder, J.-H. Ryou, and R. D. Dupuis, "Epitaxial growth and characterization of *npn*-GaN/InGaN/GaN heterojunction bipolar transistors on foreign and native

substrates," presented at *ACCGE-18/OMVPE-15*, Monterey, CA, July 31-Aug. 5, 2011.

12. R. D. Dupuis, S.-C. Shen, Z. Lochner, H.-J. Kim, Y.-C. Lee, Y. Zhang, and J.-H. Ryou, "III-Nitride heterojunction field-effect transistors and heterojunction bipolar transistors for next-generation power electronics" (E10-2171), invited to be presented in the *220th ECS Meeting & Electrochemical Energy Summit*, Boston, MA, October 9-14, 2011.