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High-performance C_{60} *n*-channel organic field-effect transistors through optimization of interfaces

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High-performance C_{60} organic field-effect transistors (OFETs) have been obtained by engineering the essential electrode/semiconductor and dielectric/semiconductor interfaces. By using calcium (Ca) as the source and drain electrodes, the width-normalized contact resistance ($R_C W$) at the electrode/semiconductor interface for devices with channel lengths ranging from 200 down to 25 μm could be reduced to a constant value of 2 kΩ cm at a gate-source voltage (V_{GS}) of 2.6 V, leading to electrical properties that are dominated by gate-modulated resistance of the channel as in conventional metal-oxide-semiconductor field-effect transistors. Channel length scaling of the source-drain current and transconductance is observed. Average charge mobility values of 2.5 $cm^2/V\,s$ extracted at $V_{GS} < 5$ V are found independent of channel length within the studied range. Besides high mobility, overall high electrical performance and stability at low operating voltages are demonstrated by using a 100-nm-thick high-κ gate dielectric layer of aluminum oxide (Al_2O_3) fabricated by atomic layer deposition and modified with divinyltetramethyldisiloxane-bis (benzocyclobutene). The combined operating properties of these OFETs, obtained in a N_2-filled glovebox, are comparable to the best *p*-channel OFETs and outperform those of amorphous silicon thin-film transistors. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3020533]

I. INTRODUCTION

Driven by the demand for low-cost, large-area, and flexible devices processed at low temperature, low-power complementary organic-based circuits (utilizing both *n*-channel and *p*-channel transistors) are of great interest in organic electronics. To date, a major challenge has been to improve the discrete device performance of *n*-channel organic field-effect transistors (OFETs). Recently, Klauk *et al.*[1] demonstrated ultralow-power consumption complementary circuits using monolayer gate dielectrics. However, as in many other reports of organic complementary circuits,[2,3] F_{16}CuPC *n*-channel OFETs showed inferior performance to their counterpart (pentacene *p*-channel OFETs) with a mobility more than one order of magnitude lower. On the other hand, electron mobilities as high as 4.9 and 6 $cm^2/V\,s$ have been reported by Itaka *et al.*[4] and Anthopoulos *et al.*[5] in C_{60} devices when operated at high voltage (>60 V). In the former report, the on/off current ratio was reduced by the use of a pentacene (a well-known *p*-type semiconductor) layer at the dielectric/semiconductor interface. In the latter report, C_{60} was deposited by hot wall epitaxy requiring deposition temperatures as high as 250 °C. Although low-voltage C_{60} OFETs were demonstrated with a triple-layer gate insulator of $SiO_2/ZSO/SiO_2$ and a low level of hysteresis,[6] the threshold voltage of 1.9 V was high compared with the applied voltage of 5 V. Recently, we reported on high-mobility OFETs based on C_{60} processed at room temperature, but the performance was shown to degrade at short channel lengths.[7]

Many reports on *n*-channel OFETs focus on the design and synthesis of novel *n*-type semiconductors to improve air stability, solution processibility, and mobility through tailoring of the chemical structures.[8–11] However, the electrical characteristics of OFETs are governed not only by the properties of the semiconductor material but also by the boundary conditions imposed by the device architecture at contacts and interfaces. For example, low electron mobilities measured in *n*-channel OFETs are often due to high contact resistance imposed by the injection barrier height between the *n*-type organic semiconductor and the source and drain electrodes. This high contact resistance can greatly limit the switching frequency of the *n*-channel OFETs due to a significant degradation of effective electron mobility upon channel scaling. However, the issue of contact resistance in *n*-channel OFETs, which is far more severe than that of *p*-channel OFETs, has not yet been widely studied. It has been established that for *p*-channel OFETs, the performance of devices is also governed by the dielectric surface properties at the insulator/semiconductor interface that often affect the structural ordering of the semiconductor film.[12,13] In the case of *n*-channel OFETs, electron trapping at the interface from carbonyl, hydroxyl, and silanol groups has been confirmed as a primary limiting factor for *n*-channel conduction and a major contribution to large threshold voltage.[14,15] Hence, *n*-channel OFET performance is often limited by the essential electrode/semiconductor and dielectric/semiconductor interfaces rather than the properties of the semiconductors themselves.

In this work, we used the well-known commercially available electron transport semiconductor C_{60} as *n*-channel active material. To obtain high-performance devices, the interface of C_{60} and the gate dielectric Al_2O_3 was

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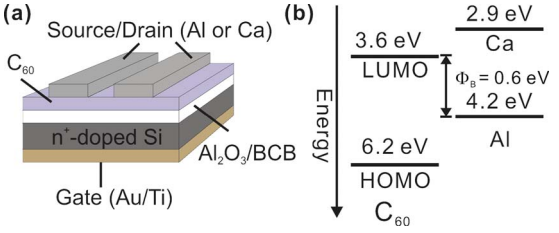

FIG. 1. (Color online) (a) Schematics of a C_{60} OFET with Al_2O_3/BCB dielectric and Al or Ca source/drain contacts. (b) Simplified energy band diagram of a C_{60} OFET at equilibrium (no biases applied) showing a Schottky contact formed at Al contact and C_{60} with a barrier height Φ_B of 0.6 eV.

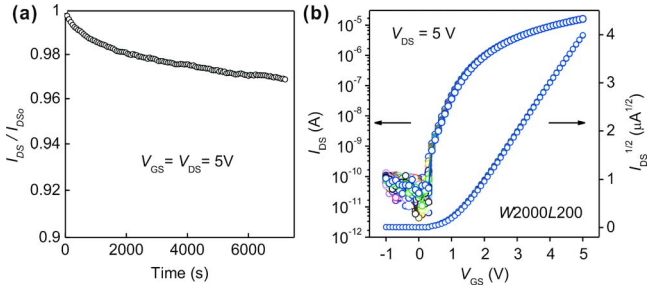

FIG. 2. (Color online) (a) Time-dependent decay of I_{DS} of a C_{60} OFET with Ca as source/drain contacts. (b) Superimposed transfer curves of 100 cycles from a C_{60} OFET with Ca as source/drain contacts.

engineered with a thin layer of hydroxyl-free divinyltetramethyldisiloxane-bis (benzocyclobutene) (BCB) with low trap density, and the low-work-function metal Ca was used for the source and drain electrodes. The gate dielectric is essentially a dual-layer dielectric with Al_2O_3 to provide high capacitance and low leakage, and a thin BCB buffering layer on top to provide properties compatible with C_{60}. The active C_{60} layers were formed using physical vapor deposition (PVD) with the substrates kept at room temperature, which enables the fabrication of C_{60} devices and circuits on plastic substrates. The combination of Al_2O_3:BCB (gate dielectric)/C_{60} (semiconductor)/Ca (source/drain electrodes) as a device architecture not only enhances device performance over a wide range of channel lengths at a low operating voltage, but also greatly improves the electrical stability and reproducibility.

II. EXPERIMENT

With a top-contact geometry, as shown in Fig. 1(a), OFETs were built on heavily *n*-doped silicon substrates (n^+-Si, 5×10^{-3} Ω cm) processed with a buffered oxide etchant (1:6 diluted HF in H_2O) to remove the native oxide. Ti/Au (10/100 nm) metallization on the backside of the substrate was used to enhance the gate electrical contact. The front surface was coated with a 100-nm-thick layer of Al_2O_3 as the gate dielectric that was deposited at 100 °C by atomic layer deposition, a deposition technique that allows for the deposition of highly conformal, defect-free dielectric layers at lower temperature.[16] The details of the gate dielectric film preparation have been published elsewhere.[17] To better control the interfacial properties at the dielectric and C_{60}, the Al_2O_3 dielectric surface was passivated with a thin buffer layer of BCB (Cyclotene™, Dow Chemicals). Crosslinkable BCB can provide a high-quality hydroxyl-free interface[7,14] to the organic semiconductor with a high dielectric breakdown strength exceeding 3 MV/cm.[18] The thin buffer layers (approximately 10 nm) were spin coated from diluted Cyclotene™ BCB and crosslinked at 250 °C on a hot plate for 1 h in a N_2-filled glovebox.[18] The total capacitance density (C_{ox}) measured from parallel-plate capacitors with 12 varying contact areas was 50 nF/cm^2. The leakage current density through the gate dielectrics was negligible (below 10^{-8} A/cm^2) under an applied field of 2 MV cm^{-1}.

Sublimed grade C_{60} (Alfa Aesar) was purified using gradient zone sublimation prior to deposition. A 50-nm-thick film of C_{60} was deposited at a rate of 0.6 Å/s using PVD at a constant pressure of 5×10^{-8} Torr while the substrates were held at room temperature. Subsequently, without breaking vacuum, 150-nm-thick top source/drain electrodes were deposited and patterned using a shadow mask. Devices had a wide range of width to length ratios, between 1 and 80, with channel lengths ranging from $L=25$ to 200 μm and channel widths ranging from $W=200$ to 2000 μm. With a low work function of 2.9 eV, Ca was chosen for the source/drain electrodes to facilitate electron injection into the lowest unoccupied molecular orbital (LUMO) (3.6 eV) level of C_{60} (Refs. 19 and 20) since there is no barrier (Φ_B) between the C_{60} LUMO level and the Ca Fermi level (E_F) according to the conventional Mott–Schottky model, as shown in Fig. 1(b). Control devices were also fabricated with aluminum (Al) as source/drain electrodes. In this case, a high barrier height of 0.6 eV is present for electron injection due to the higher work function of 4.2 eV of Al. The electrical measurements were performed in a N_2-filled glovebox (O_2, H_2O <0.1 ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit. All transistors, for which data are reported here, underwent the same fabrication process, measurement, and analysis steps.

III. RESULTS AND DISCUSSIONS

A. Electrical characterization

Electrical stability under repeated and continuous electrical stress has been a key issue in the accurate measurement, analysis, and prediction of electrical performance of discrete devices and integrated circuits. Previous studies from Chua *et al.*[14] established that electron traps (especially $SiOH^-$ and OH^-) at the dielectric/semiconductor interface are responsible for electrical instability of *n*-channel OFETs and lead to hysteresis and threshold voltage shift under dc bias stress. *n*-channel OFETs with a large shift often exhibit high threshold voltage since a large positive gain-source voltage V_{GS} is needed to fill the traps. dc bias stress tests were conducted to demonstrate the stability of devices with Ca electrodes. The time-dependent decay of the drain-source current I_{DS} in C_{60} OFETs was less than 3% under continuous dc biases of $V_{GS}=V_{DS}=5$ V for 2 h, as seen in Fig. 2(a). Neither current degradation nor threshold voltage shift was observed in the transfer characteristics when the devices were repeatedly measured 100 times with a 2 s waiting time between scans, as shown in Fig. 2(b). The electrical stability

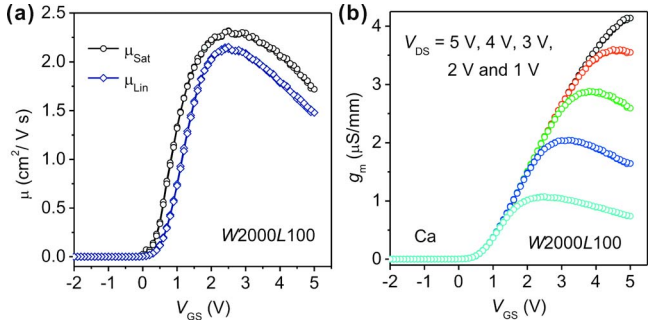

FIG. 3. (Color online) (a) Mobility and (b) transconductance degradation of a C_{60} OFET with Ca as source/drain contacts as a function of gate-source voltage V_{GS}. The mobilities were extracted both in the linear regime with V_{DS}=1 V and in the saturation regime with V_{DS}=5 V in a C_{60} OFET (L =100 μm/W=2000 μm).

shown here can be attributed to a low interface trap density at the interface between C_{60} and the gate dielectric. A maximum interfacial trap density can be estimated from[21,22]

$$N_{\text{trap}}^{\max} = \frac{C_{\text{ox}}}{q}\left(\frac{qS \log e}{k_B} - 1\right), \tag{1}$$

where k_B is Boltzmann's constant, T is temperature, q is the electronic charge, e is the base of the natural logarithm, C_{ox} is the capacitance density of the gate insulator, and S is the subthreshold slope in V/decade. The trap density at the interface with BCB is calculated to be near or below 10^{12} cm^{-2} V^{-1} with average values of S below 0.3 V/decade. This value is lower than the best values reported for OFETs.[22,23]

As reported in pentacene p-channel OFETs,[24] a decrease in mobility with increasing gate voltage was observed in C_{60} OFETs, as shown in Fig. 3(a). The field-effect mobility is found to be gate dependent both in the linear regime and the saturation regime. Initially, the mobility increases almost linearly with gate bias and reaches a peak value where all the surface traps are filled and the contact resistance is minimized. In our devices, it only takes about 2–3 V to reach the peak. Unlike the constant mobility in idealized metal-oxide-semiconductor field-effect transistors (MOSFETs), the mobility falls off slightly due to surface scattering, which slows down the carriers, a typical phenomenon observed in MOSFET devices.[25] The slight decrease in mobility at higher gate bias is also reflected in the transconductance g_m, as seen in Fig. 3(b). In this work, the mobility peak values were used to characterize C_{60} OFETs while the surface scattering effects on the mobility are not discussed. The threshold voltage V_T

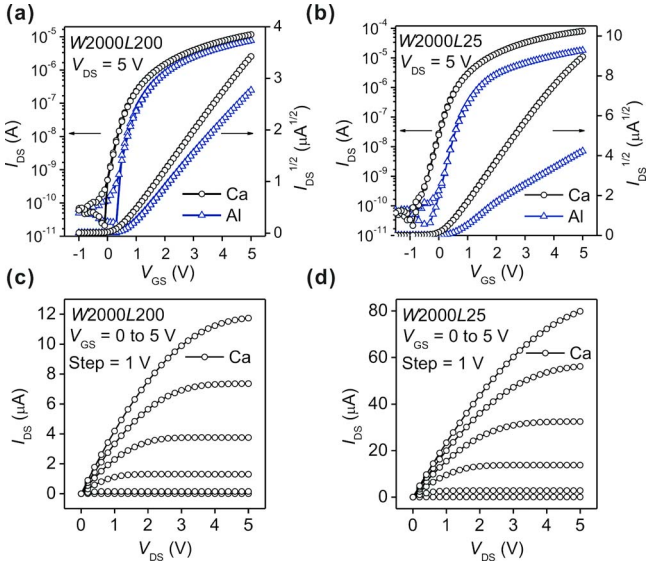

FIG. 4. (Color online) [(a) and (b)] Comparison of hysteretic transfer characteristics of both long-channel (L=200 μm/W=2000 μm) and short-channel (L=25 μm/W=2000 μm) C_{60} OFETs with Ca or Al as source/drain contacts. [(c) and (d)] Output characteristics of both long-channel and short-channel C_{60} OFETs with Ca as source/drain contacts.

was determined at the maximum of the second derivative of I_{DS} with respect to V_{GS} in the linear regime where V_{GS} of 5 V is much larger than V_{DS} of 0.05V. The V_T values calculated using this method are less sensitive to changes in both mobility and contact resistance.[26]

Figures 4(a) and 4(b) compare representative hysteretic transfer characteristics for both long-channel devices [L =200 μm, Fig. 4(a)] and short-channel devices [L=25 μm, Fig. 4(b)] with the same channel width W=2000 μm and source/drain electrodes with Ca and Al, respectively. Representative output characteristics of C_{60} OFETs with Ca are shown in Fig. 4(c) (L=200 μm) and Fig. 4(d) (L=25 μm). The electrical parameters field-effective mobility (μ), threshold voltage (V_T), subthreshold slope (S) and on/off current ratio ($I_{on/off}$) are summarized and compared in Table I. For each type of transistor, two to four devices with identical geometry were measured to obtain a mean value and standard deviation (sd). As shown previously by our group,[7] when using hydroxyl-free and high-purity BCB polymer to modify the dielectric interface, C_{60} OFETs presented no hysteresis and threshold voltage shift during hysteretic gate bias scans. For long-channel devices (W=2000 μm/L =200 μm) as shown in Fig. 4(a), devices with both Ca and Al electrodes show excellent performance with a V_T close to

TABLE I. Summary of the electrical parameters for C_{60} OFETs. Each data point represents the mean value and the sd calculated from two identical devices. S/D stands for source/drain electrodes, μ denotes field-effect mobility, V_T denotes threshold voltage, S denotes subthreshold slope, and $I_{on/off}$ denotes on/off current ratio.

	S/D	μ (cm^2/Vs)	V_T (V)	S (V/decade)	$I_{on/off}$($\times 10^6$)
	Al	1.7 ± 0.1	0.3 ± 0.1	0.1 ± 0.02	0.4 ± 0.1
*W*2000*L*200(W/L=10)	Ca	2.3 ± 0.2	0.2 ± 0.1	0.1 ± 0.04	1.0 ± 0.3
	Al	0.4 ± 0.05	0.2 ± 0.1	0.3 ± 0.06	1.0 ± 0.2
*W*2000*L*25(W/L=80)	Ca	2.3 ± 0.1	0.1 ± 0.1	0.3 ± 0.03	4.0 ± 0.3

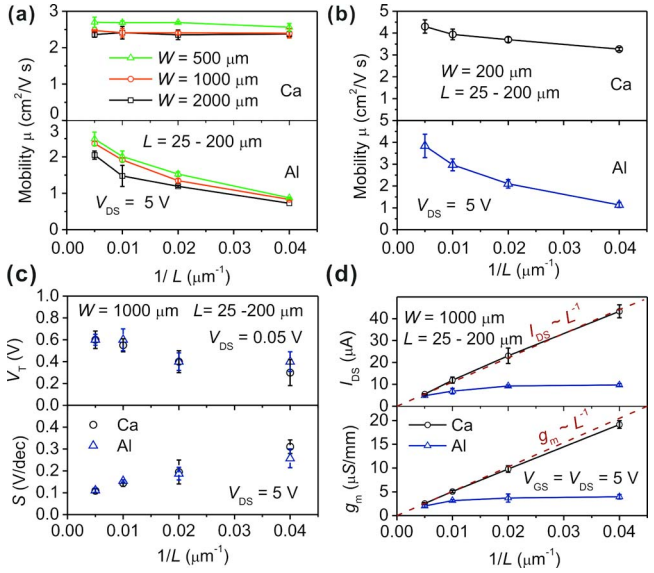

FIG. 5. (Color online) [(a) and (b)] Effect of channel scaling on mobility μ, (c) threshold voltage and subtrheshold slope, drain-source current I_{DS}, and (d) transconductance g_m in n-channel C_{60} OFETs with different source/drain contacts: Ca or Al. Each data point represents the mean value and the error bars represent the sd calculated from two to four identical devices (two for $W=2000$ μm and four for others).

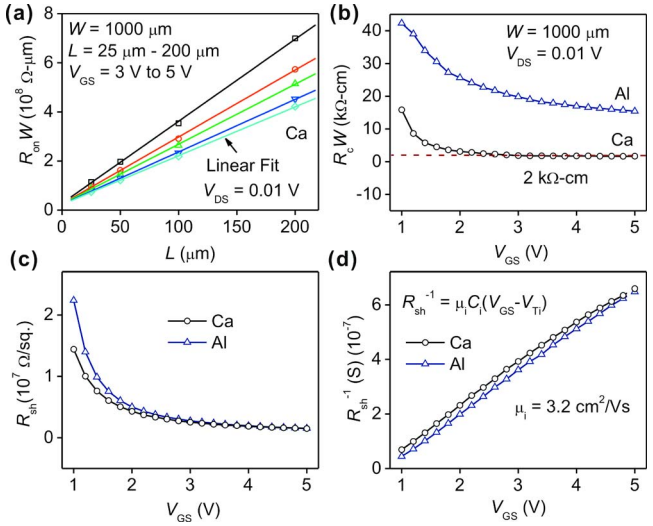

FIG. 6. (Color online) (a) Total width-normalized contact resistance $R_{on}W$, (b) width-normalized contact resistance R_CW, (c) sheet channel resistance R_{sh}, and (d) sheet channel conductance R_{sh}^{-1} of C_{60} OFETs shown as a function of gate-source voltage V_{GS} for a drain-source voltage $V_{DS}=0.01$ V.

zero and S around 0.1 V/decade, while the mobility μ with Ca $(2.3\pm0.2$ cm^2/V s) is slightly higher than with Al $(1.7\pm0.1$ cm^2/V s). In contrast, when the channel length is scaled down to 25 μm, both devices start to show short-channel effects, such as a less pronounced saturation of I_{DS}, earlier turn-on, and higher subthreshold voltage,[27] as shown in Fig. 4(b). However, while the devices with Ca contacts remain unaffected in mobility, the field-effect mobility for the devices with Al is greatly reduced to 0.4 cm^2/V s in devices with shorter channels.

B. Channel length scaling

To investigate the dependence of mobility on channel length L, field-effect mobilities of devices are statistically plotted over the inverse of channel length (L^{-1}) with channel width $W=500$, 1000, and 2000 μm in Fig. 5(a) and $W=200$ μm in Fig. 5(b). In devices with Al as the source/drain electrodes, the mobility is greatly reduced with narrowing channel length. This is a characteristic of many organic transistors since the carrier injection current is often primarily contact limited due to the large Schottky barrier at the metal/organic interface, especially in n-channel OFETs. The Schottky barrier is removed when Ca is used for the source/drain electrodes. The mobility for devices with Ca thus becomes independent of channel length in the range of $L=200$ μm down to 25 μm. However, it is worth mentioning that the mobility values become exceptionally high (up to 4.5 cm^2/V s) for devices with $W=L=200$ μm, where fringe current may lead to higher effective mobility, as seen in Fig. 5(b). In the case of V_T and S, as shown in Fig. 5(c), the values do not scale with channel length as mobility does, but they do change slightly with decreasing channel length due to the higher transverse electric field in shorter channels. The field-effect current I_{DS} and transconductance g_m as a function of the inverse of channel length (L^{-1}) are also plotted and compared to those of devices with Al electrodes in Fig. 5(d). With I_{DS} and g_m starting from similar values at $L=200$ μm, devices with Al electrodes show typical contact-limited current, where I_{DS} saturates and stops growing with decreasing channel length, while devices with Ca as the source/drain contacts show channel scaling with MOSFET-like characteristics where I_{DS} and g_m are proportional to L^{-1} with g_m larger than 15 $\mu S/mm$ achieved for the short-channel devices with $L=25$ μm.

C. Contact resistance

To gain a better understanding of effect of the contacts on the mobility, the contact resistance of each metal with C_{60} was extracted using a transmission line method based on the dependence of current-voltage characteristics on channel length. In the linear regime, the overall device resistance R_{on} can be considered as the sum of the channel resistance R_{ch} and a total contact resistance R_C according to[28]

$$R_{on} = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{\substack{V_{GS} \\ V_{DS}\to 0}} = R_{ch} + R_C = R_{sh}\frac{L}{W} + R_C, \tag{2}$$

$$R_{on}W = R_{sh}L + R_CW, \tag{3}$$

$$R_{sh} = \frac{1}{\mu_c C_i (V_{GS} - V_{Ti})}, \tag{4}$$

where R_{sh}, μ_c, and V_{Ti} are the sheet channel resistance, the corrected mobility, and the threshold voltage, respectively.

According to Eqs. (2) and (3), the total width-normalized contact resistance R_CW was extracted by plotting the width-normalized $R_{on}W$ as a function of L for different gate voltages, as shown in Fig. 6(a). A set of devices with channel lengths ranging from $L=25$ to 200 μm and a fixed channel width of $W=1000$ μm was used to calculate the contact resistance at a low drain-source voltage (V_{DS}) of 0.01 V for

V_{GS} values ranging from 1 to 5 V. By extrapolating $R_{on}W$ to $L=0$ μm, the y intercept of the least-squares fit yields $R_C W$ and the slopes correspond to sheet channel resistance R_{sh}. The width-normalized contact resistance ($R_C W$) and the sheet channel resistance (R_{sh}) of C_{60} transistors with Ca or Al contacts are shown in Figs. 6(b) and 6(c), respectively. Similar to reports from many different groups,[23,29–31] the contact resistance with Al electrodes is strongly dependent on V_{GS}, as seen from Fig. 6(b) with a contact resistance of 20 kΩ cm at $V_{GS}=5$ V. In general, there are two contributions to contact resistance in top-contact OFETs: the resistance of the metal contact/organic interface and the resistance of the organic film itself from the metal to the channel. The former can be reduced by tuning the Fermi level (E_F) of the metal with V_{GS} to lower the injection barrier, and the latter can be reduced by increasing the induced charge density in the accumulation regime with V_{GS}. In the case of Ca, the contact resistance drops drastically and rapidly reaches a constant value of 2 kΩ cm by applying only 2.6 V, which is in contrast to the tens of volts needed for most OFETs. The residual contact resistance (which is no longer modulated by the gate bias) could be governed by the intrinsic conductivity of the C_{60} film. The low residual contact resistance achieved at extremely low V_{GS} is attributed to the combination of a low injection barrier between C_{60} and Ca and the high intrinsic mobility of C_{60} (therefore high conductivity). These findings are of significance in guiding the design of complementary circuits, especially when the inferior performance of n-channel OFETs is a limiting factor primarily due to their large contact resistance.

As shown in Fig. 6(c), the sheet channel resistance R_{sh} is decreased when increasing V_{GS} due to an increase of induced charge density in the channel. According to Eq. (4), a corrected mobility (μ_c) from the contact resistance can be calculated from the slope of the linear least-square fit of R_{sh}^{-1}, which is equivalent to the channel sheet conductance, as shown Fig. 6(d). As expected, since the C_{60} films were deposited during the same deposition run, a similar mobility of 3.2 $cm^2/V\,s$ is obtained for both types of devices with Ca and Al as source/drain electrodes after the mobility is corrected for the contact resistance. From these calculations, using devices with a channel width of $W=2000$ μm (see Table I) as an example, we can assess that the contact resistance from the C_{60} film accounts for a mobility degradation of less than 30%, from 3.2 to 2.3 $cm^2/V\,s$ for Ca devices. On the other hand, the high injection barrier for Al devices account for an additional mobility degradation of more than 60%, from 3.2 to 0.4 $cm^2/V\,s$ in short-channel devices with $L=25$ μm. Consequently, the critical channel length, where the contact resistance starts to dominate, is calculated to be $L=100$ μm with Al and only 10 μm with Ca. The latter is similar to the best results obtained from top-contact OFETs with pentacene and Au.[23]

IV. CONCLUSIONS

In summary, high-performance n-channel C_{60}-based OFETs with MOSFET-like electrical characteristics were fabricated. High electron mobilities (2.3 $cm^2/V\,s$ for high W/L ratios and up to 4.3 $cm^2/V\,s$ for low W/L ratios), threshold voltages near zero ($V_T<1$ V), low subthreshold slopes ($S<0.3$ V/decade), on/off current ratios larger than 10^6, and a maximum transconductance g_m larger than 15 $\mu S/mm$, along with excellent electrical stability under multiple test cycles (100 times) and continuous electrical stress were demonstrated. These combined properties were obtained by engineering the dielectric/organic semiconductor interface and by reducing the contact resistance at the metal contact/organic semiconductor interface. A mobility of 3.2 $cm^2/V\,s$ corrected for contact resistance is shown to be independent of the nature of the metal contact. In addition, the electrical hysteresis/instability has been significantly reduced to a level where the OFETs exhibit excellent reproducibility and superior lifetime. Due to the sensitivity of both the C_{60} semiconductor and the Ca electrode to ambient conditions, these devices will require encapsulation to protect them from oxygen and moisture.

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