A Control Algorithm Based on the Conservative Power Theory for Cooperative Sharing of Imbalances in 4-Wire Systems

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Abstract—— A cooperative control scheme based on the Conservative Power Theory (CPT) is proposed which can share imbalances in three-phase four-wire droop-controlled systems. By utilising the CPT, the balanced, unbalanced and distorted components of the currents and powers in a micro-grid can be identified. Using control loops based on virtual impedances and implemented in the stationary a-b-c frame, the imbalances and harmonics are shared between the different 4-leg inverters in the microgrid. A secondary control loop is implemented to regulate the maximum voltage imbalance/distortion at the Point of Common Coupling (PCC) or any other point in the microgrid. The theoretical background of the method is presented, and experimental validation is demonstrated using a laboratory-scale microgrid with two inverters operating at 5 kW.

Index Terms— 4-wire microgrids, CPT, cooperative imbalance sharing, harmonic distortion, droop control.

I. INTRODUCTION

Microgrids (MGs) are an attractive solution for electrification in rural areas, industrial parks, commercial and institutional campuses, among other places [1] [2]. A MG is typically composed of a cluster of loads, Distributed Generators (DGs) and Energy Storage Systems (ESSs), connected to the main AC power system at the distribution level at a single Point of Common Coupling (PCC) [3]. These components may be designed for single or three phase applications and usually, a four wire microgrid is required to include a neutral connection. Many of the generating units are connected to the PCC through voltage source inverters (VSIs). When a 4-leg converter topology is utilized, the neutral connection is usually provided by a dedicated power converter leg. This approach is preferred for creating the neutral connection since it does not require either a bulky transformer or large DC link capacitors [4].

Cooperative sharing of active (P) and reactive (Q) power in microgrids has been widely studied and can be achieved using the droop control method [5]. However, there is no straightforward solution for sharing imbalances collaboratively between inverters. Moreover, very few papers discuss collaborative control systems for 4-wire microgrids which contain single-phase loads, where the imbalances are produced not only by the presence of negative sequence components, but also by the zero sequence. In fact, the presence of unbalanced loads in an MG could produce voltage imbalances at other points of the 4-wire system due to the circulation of unbalanced currents through the line and converter impedances in the microgrid [6] [7]. To solve the problems produced by imbalances, two approaches can be utilised. Firstly, active power filters (APFs) can be applied to inject currents and/or voltages to compensate for imbalances and/or harmonics that are produced by the load [8] [9]. However, APFs are not attractive in MGs - they constitute additional hardware and higher costs. The second and more cost-effective approach is to embed imbalance and harmonic compensation capabilities into the control algorithms of the inverters that are already available in the MG, thus maximising the utilisation of the hardware [10]-[13]. For example, in [11] a cooperative method for compensating unbalanced voltages at the inverters' output is proposed. The goal is to use the remaining VA capability of the converters as part of a negative sequence droop control scheme (called $Q^- - G$). The compensation reference is injected at the output of the voltage control loop and thus can be considered as a disturbance to be rejected by this control loop. However, the cooperative performance is affected by the line impedance and the droop coefficients. In [13] the unbalanced output voltage of the inverters is compensated by adding a negative sequence voltage component to their references. The paper proposes the direct change of the voltage reference of the inverters to compensate the voltage imbalances in a MG. In this case, the compensation reference is considered a command to be followed by the voltage controllers. However, these references depend on the load characteristics and it is difficult to calculate them in MGs with a high number of converters and with variable loads. In [12], a control method for reducing the voltage imbalance at the inverters' outputs is proposed. The voltage compensation introduces negative sequence currents through the current-controlled converters. This method is not suitable for voltage-controlled converters. In [10] a method for compensating harmonics and imbalances in an MG is proposed that modifies both the virtual impedance loop and the inner voltage control loop. The method is effective; however, it is aimed at operation with a single DG. Note that, the works of [10]-[13] are performed for three-phase three-wire MGs and they require an algorithm for sequence separation. This issue could be a drawback considering that

sequence separation algorithms are affected by noise, harmonic distortion, etc. [14] [15]. Moreover, in [10]-[13] zero sequence components are not considered because three-phase three-wire systems are studied.

The aim of the works discussed in [10]-[13] is predominantly to achieve cooperative imbalance voltage compensation among the inverters when the load is unbalanced. Another interesting goal is to improve the unbalanced power load sharing among the inverters located in an MG according to their power rating. The challenge here is to prevent a disconnection of an inverter due to overload and therefore to prevent stability issues in the whole MG, especially under heavy load conditions. This aim can only be achieved at the expense of increasing voltage imbalance at the inverter outputs as discussed in [6] [7] [16]. Obviously, the maximum unbalanced voltage and voltage distortion allowed in the microgrid has to be regulated to avoid power quality issues, for instance defined by the standards ANSI C84.1-2006 [17] (stating maximum voltage imbalances) and IEEE 519-1992 [18] (stating maximum THD values). However, in the planning of a 4-wire microgrid, the fact that not all the loads have the same sensitivity to the voltage imbalance should be considered [19]. Therefore, buses where sensitive loads may be located have to be subjected to more stringent voltage requirements than those buses where no sensitive loads are connected. Therefore, imbalance sharing methods should be designed to fulfil the voltage requirements of buses where sensitive loads may be located. Power quality in other non-critical buses of the MG could be improved using a hierarchical control system [6] [16] [19].

In the context of voltage imbalance control of microgrids considering sensitive and non-sensitive loads, an algorithm to improve unbalanced current sharing for a three-phase four-wire MG is proposed in [7]. Since the voltage quality could be degraded when the proposed method is enabled, the authors proposed a decentralized control scheme to improve selectively the voltage quality in buses where sensitive loads are connected. It is argued in [7] that critical loads should be placed close to inverters and therefore the increase of voltage imbalance at the PCC when the proposed control scheme is working, is not an important concern.

On the other hand, in [6] it is assumed that a sensitive load is placed at the PCC. A method is proposed for improving the current sharing for both imbalance and harmonics in a three-phase three-wire MG, and because the voltage imbalance is increased at the PCC when the proposed method is enabled, the authors proposed a secondary control scheme for improving the voltage quality at this point. In [6] [7] the use of a sequence extraction algorithm is required. Cooperative imbalance sharing is achieved, defining both negative and zero sequence impedances in [7], while in [6], only a negative sequence impedance is used since only a three-phase three-wire system is discussed.

In this paper, a decentralized collaborative control scheme for sharing load imbalance in a 4-wire MG is proposed. The term collaborative is used to indicate the capability of each inverter to supply unbalanced power (as defined by the CPT in the next section) to the load according to its residual power capacity, which changes with time. The control scheme proposed in this paper is performed in the fixed *abc* coordinate

reference frame and sequence separation is not required. The Conservative Power Theory (CPT) [20]- [25] is used as the theoretical framework to achieve imbalance sharing between the inverters. The contributions of this paper can be summarised as follows:

• The proposed sharing algorithm uses a novel approach based on the CPT methodology that can be used to implement a simple identification of the balanced, unbalanced and non-linear components of the currents and powers. Separation of the sequence components is not required. This produces a more robust imbalance sharing algorithm, particularly because most of the sequence separation algorithms are strongly affected by, noise, harmonic distortion, small variations in the sampling time, etc. [14] [15]

• A very simple method to share harmonic distortion between the generation sources can be obtained using the CPT transform. In this paper, the method is described and experimentally validated.

• A new method for defining the preliminary unbalanced voltage set points is introduced. The methodology (see Section IV.C) is based on an optimising problem subjected to restrictions and is solved using a genetic algorithm.

• To the best of our knowledge, there is only one paper where a control scheme for cooperative imbalance sharing in 4-wire MGs is discussed ([7]). The other control schemes are proposed for 3-wire MGs. The control system discussed in [7] considers sequence separation, with all the aforementioned robustness problems. Moreover, the application of the scheme proposed in [7] to a system with relatively high harmonic distortion (see [18]) could be difficult to realise considering (i) the complexity of the extraction of the main harmonics and (ii) the harmonics extraction is sequence-separation-dependant. The control algorithm proposed in this work is based on the CPT which is very robust to issues such as distortion, noise, differences in the sampling time etc. As is demonstrated in this work, it is very simple to extend the proposed methodology to include harmonic distortion.

The rest of this paper is organised as follows: For completeness in Section II a brief review of the CPT is provided; Section III introduces the proposed unbalanced power sharing concept; Section IV discusses in detail the proposed imbalance sharing control scheme. Finally, section V reports both simulation and experimental validation of the proposed imbalance control and sharing scheme. To realise the experimental validation, load conditions and the voltage/currents measured in a real microgrid located in the north of Canada are considered. (See [9])

II. REVIEW OF CONSERVATIVE POWER THEORY (CPT)

The CPT defines two main instantaneous quantities: the instantaneous power $p(t)$, which is defined as the scalar product of the instantaneous line-to-phase voltages and currents (1), and the instantaneous reactive energy $w(t)$ defined as the scalar product of the instantaneous values of the integral of the unbiased voltages $\hat{v}$ and the currents [20]- [23].

$$\begin{cases} p(t) = [v_a \ v_b \ v_c] \circ [i_a \ i_b \ i_c]^T \\ w(t) = [\hat{v}_a \ \hat{v}_b \ \hat{v}_c] \circ [i_a \ i_b \ i_c]^T \end{cases} \tag{1}$$

where the unbiased voltage integral $\hat{v}$ is defined as:

$$\hat{v}_\mu = \int_0^t v_\mu(\tau)d\tau - \bar{v}_{\int \mu} \qquad \mu = a, b, c \qquad (2)$$

In (2) the term $\bar{v}_{\int \mu}$ is the mean value of each voltage integral. In a three-phase four-wire MG, the phase voltages are measured with respect to the neutral point. Based on the mean values of $p(t)$ and $w(t)$, the active power (P) and the reactive energy (W) are defined as shown in (3).

$$P = \frac{1}{T}\int_0^T v \circ i \, dt, \qquad W = \frac{1}{T}\int_0^T \hat{v} \circ i \, dt \qquad (3)$$

Based on (1)-(3) it is possible to decompose the load current i_μ as the sum of five orthogonal current components. These are:

The *balanced active currents*, defined as:

$$i_{a\mu}^b = \frac{P}{V^2}v_\mu = G^b v_\mu \qquad (4)$$

where $V = \sqrt{V_a^2 + V_b^2 + V_c^2}$ is the collective RMS value (Euclidean norm) of the voltages, G^b is the equivalent balanced conductance and P is the active power given by (3).

The *balanced reactive current* is given by:

$$i_{r\mu}^b = \frac{W}{\hat{V}^2}\hat{v}_\mu = \mathcal{B}^b \hat{v}_\mu \qquad (5)$$

where $\hat{v}_\mu$ is the unbiased voltage integral (2), $\hat{V}$ is the collective RMS value of the unbiased voltage integrals, $\mathcal{B}^b$ is the balanced reactivity and W is the reactive energy (3).

The *unbalanced current* is defined as:

$$i_\mu^u = i_{a\mu}^u + i_{r\mu}^u = \left(\frac{P_\mu}{V_\mu^2} - G^b\right)v_\mu + \left(\frac{W_\mu}{\hat{V}_\mu^2} - \mathcal{B}^b\right)\hat{v}_\mu \qquad (6)$$

Note that the unbalanced currents shown in (6) only exist if $\frac{P_\mu}{V_\mu^2} \neq G^b$ and/or $\frac{W_\mu}{\hat{V}_\mu^2} \neq \mathcal{B}^b$, i.e. when the load is unbalanced.

The *void current* is the remaining current that does not transfer active or reactive energy and is given by:

$$i_{v\mu} = i_\mu - i_{a\mu}^b - i_{r\mu}^b - i_\mu^u \qquad (7)$$

Finally, the current vectors $\underline{i}_a^b, \underline{i}_r^b, \underline{i}_a^u, \underline{i}_r^u, \underline{i}_v$ are orthogonal. Moreover, if the voltages have little distortion, then the harmonics present in the current are going to be reflected in the void current $\underline{i}_v$ (see [20]- [23]).

Based on the RMS values of currents and voltage, the CPT defines the power terms [20], where $P = V \cdot I_a^b$ is the active power, $Q = V \cdot I_r^b$ is the reactive power, $N = V \cdot I^u$ is the unbalanced power and $D = V \cdot I^v$ is the void power. Notice that the capital letters I and V denote RMS values. The term I^u is the RMS value of the sum of $\underline{i}_a^u$ and $\underline{i}_r^u$ (6)].

III. UNBALANCED POWER SHARING CONCEPT

A. *Analysis of an Inverter Feeding an Unbalanced Load*

Considering the 4-leg inverter in Fig. 1, where the load current $\underline{i}_o$ includes positive, negative, and zero sequence components as in (8), and considering the fact that the maximum allowed voltage imbalance in power systems is 3% as defined by the ANSI C84.1-2006 standard (see [17]). The positive sequence voltage is dominant. Therefore, the voltage at the converter´s outputs can be considered as shown in (9) [16] [26]. This can be corroborated using the voltages and currents measured in a real microgrid [9].

With these assumptions, the system shown in Fig. 1 can be analysed using the CPT definitions given in section II. Defining the balanced current vector ($\underline{i}^b$) as the sum of the active and reactive balanced currents [defined by (4) and (5) respectively], it is demonstrated that $\underline{i}^b$ is given by (10). Note that this new vector ($\underline{i}^b$) only contains the positive sequence of $\underline{i}_o$ [see (8)]. In a similar way, based on the unbalanced active ($\underline{i}_a^u$) and reactive ($\underline{i}_r^u$) currents defined by the CPT in (6), a new unbalanced vector $\underline{i}^u$ is obtained as shown in (11). Note that $\underline{i}^u$ contains both the negative and the zero sequence current components of $\underline{i}_o$ (8). Finally, as the newly proposed vectors are orthogonal, this result verifies that the CPT also provides a robust methodology to decouple the positive sequence current from both negative and zero sequence currents in the stationary *abc* frame.
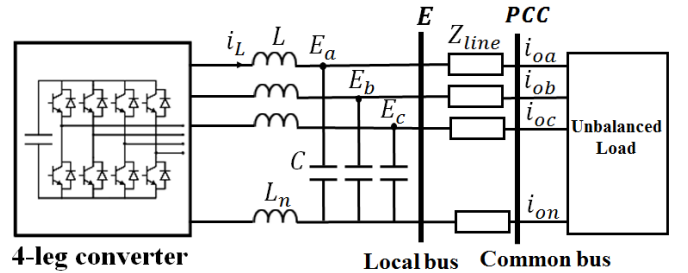

Fig. 1. Example of 4-leg converter feeding unbalanced load in an islanded microgrid

$$\underline{i}_o = \begin{bmatrix} \sqrt{2}I^+ sin(\omega t + \varphi^+) + \sqrt{2}I^- sin(\omega t + \varphi^-) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \\ \sqrt{2}I^+ sin\left(\omega t - \frac{2\pi}{3} + \varphi^+\right) + \sqrt{2}I^- sin\left(\omega t + \frac{2\pi}{3} + \varphi^-\right) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \\ \sqrt{2}I^+ sin\left(\omega t + \frac{2\pi}{3} + \varphi^+\right) + \sqrt{2}I^- sin\left(\omega t - \frac{2\pi}{3} + \varphi^-\right) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \end{bmatrix} \qquad (8)$$

$$\underline{E} = \begin{bmatrix} \sqrt{2}E \cdot sin(\omega t + \delta) \\ \sqrt{2}E \cdot sin\left(\omega t - \dfrac{2\pi}{3} + \delta\right) \\ \sqrt{2}E \cdot sin\left(\omega t + \dfrac{2\pi}{3} + \delta\right) \end{bmatrix} \tag{9}$$

$$\underline{i}^b = \underline{i}_a^b + \underline{i}_r^b = \begin{bmatrix} \sqrt{2}I^+ sin(\omega t + \varphi^+) \\ \sqrt{2}I^+ sin\left(\omega t - \dfrac{2\pi}{3} + \varphi^+\right) \\ \sqrt{2}I^+ sin\left(\omega t + \dfrac{2\pi}{3} + \varphi^+\right) \end{bmatrix} \tag{10}$$

$$\underline{i}^u = \underline{i}_a^u + \underline{i}_r^u = \begin{bmatrix} \sqrt{2}I^- sin(\omega t + \varphi^-) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \\ \sqrt{2}I^- sin\left(\omega t + \dfrac{2\pi}{3} + \varphi^-\right) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \\ \sqrt{2}I^- sin\left(\omega t - \dfrac{2\pi}{3} + \varphi^-\right) + \sqrt{2}I^0 sin(\omega t + \varphi^0) \end{bmatrix} \tag{11}$$

B. Two Inverters Feeding a Common Unbalanced Load

The scenario discussed for Fig. 1 for a single 4-leg converter feeding an unbalanced load is now extended to the case of two inverters as is shown in Fig. 2. In this figure, the load is modelled as a current source and the distributed generation units are modelled as voltage sources E generated across the capacitors of the inverter output filter, as shown in Fig. 1. Based on the discussion presented in section III-A, it is possible to calculate the balanced and unbalanced current vectors [given by (10) and (11)] for each inverter. It is worth remembering that, under the assumption of negligible voltage imbalance, the two current vectors are orthogonal, and decoupled from a control perspective. Notice that these current vectors depend on $\underline{E}_1$ and $\underline{i}_1$ for inverter 1 and on $\underline{E}_2$ and $\underline{i}_2$ for inverter 2 (Fig. 2). In Fig. 2, by applying the superposition principle, $\underline{i}_1$ and $\underline{i}_2$ can be written as (12) and (13).
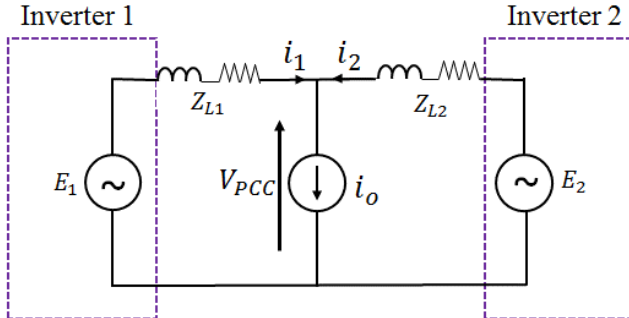

Fig. 2. Two inverters feeding an unbalanced load – unifiliar equivalent circuit

$$\underline{i}_1 = \underline{i}_{11} + \underline{i}_c \tag{12}$$
$$\underline{i}_2 = \underline{i}_{22} - \underline{i}_c \tag{13}$$

where $\underline{i}_{11}$ and $\underline{i}_{22}$ are the current components due to $\underline{i}_o$ while $\underline{i}_c$ is a circulating current component depending on the voltage difference between $\underline{E}_1$ and $\underline{E}_2$. The two currents $\underline{i}_1$ and $\underline{i}_2$ can be rewritten explicitly as:

$$\underline{i}_1 = \frac{Z_{L2}}{Z_{L1} + Z_{L2}} \cdot \underline{i}_o + \frac{E_1 - E_2}{Z_{L1} + Z_{L2}} \tag{14}$$

$$\underline{i}_2 = \frac{Z_{L1}}{Z_{L1} + Z_{L2}} \cdot \underline{i}_o - \frac{E_1 - E_2}{Z_{L1} + Z_{L2}} \tag{15}$$

From these equations, it can be observed that, whether the impedances $\underline{Z}_{L1}$ and $\underline{Z}_{L2}$ are predominantly inductive, only the circulating current $\underline{i}_c$, produced by the different voltage references of the two inverters, causes a phase shift between $\underline{i}_1$ and $\underline{i}_2$. Considering that in a typical microgrid, $\underline{E}_1 \approx \underline{E}_2$ because the magnitudes are similar and the phase difference is small, it is assumed that $\underline{i}_c$ is smaller than $\underline{i}_o$. Based on that, calculating both balanced and unbalanced current vectors [given by (10) and (11) respectively] in the inverters and the load, the following relationships can be obtained.

$$\underline{i}_o^b \approx \underline{i}_1^b + \underline{i}_2^b \tag{16}$$
$$\underline{i}_o^u \approx \underline{i}_1^u + \underline{i}_2^u \tag{17}$$

From (16)-(17) it can be concluded that the current imbalance in the load ($\underline{i}_o^u$) depends mainly on the unbalanced current vectors calculated in both inverters ($\underline{i}_1^u$, $\underline{i}_2^u$). Conversely, the positive sequence current in the load ($\underline{i}_o^b$) is mainly a function of the balanced current vectors in both inverters ($\underline{i}_1^b$, $\underline{i}_2^b$).

IV. PROPOSED IMBALANCE SHARING CONTROL SCHEME

The proposed control scheme is based on the property described in section III where the positive current sequence is decoupled from both negative and zero current sequences through the current vectors $\underline{i}^b$ and $\underline{i}^u$ [see (10) and (11)]. The proposed imbalance sharing control scheme implemented in inverter 1 of Fig. 2 is shown in Fig. 3 (in the Laplace domain), where the inverter output current $i_1(s)$ is divided into $i_1^b(s)$ and $i_1^u(s)$. With the balanced current $i_1^b(s)$ a virtual impedance loop [13] [19] is implemented to achieve decoupling between active and reactive powers and also for stability purposes. [13] [19]
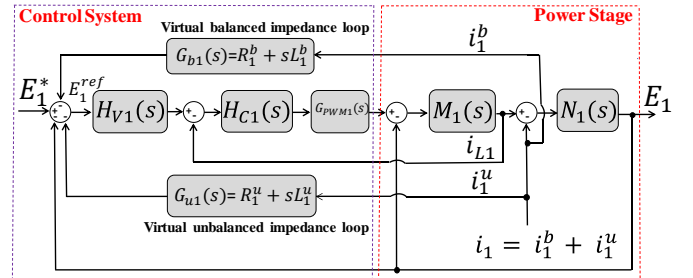

Fig. 3. Proposed control scheme of each four-leg inverter

A new virtual unbalanced impedance loop is proposed for the unbalanced current $i_1^u(s)$ to control the unbalanced voltage at the inverter output. The proposed control scheme shown in Fig. 3, is implemented in the *abc* reference frame and sequence separation is not required. Notice that the virtual impedance loops are equivalent to output impedances where voltage drops are produced by the circulation of balanced and unbalanced currents respectively. These voltage drops are given in (18).

$$E_1(s) = K_1(s)E_1^*(s) - Z_{out1}^b(s)i_1^b(s) - Z_{out1}^u(s)i_1^u(s) \tag{18}$$

$$K_1(s) = \frac{N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s)}{1 + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s) + M_1(s)G_{PWM1}(s)H_{C1}(s) + N_1(s)M_1(s)} \tag{19}$$

$$Z_{out1}^b(s) = \frac{N_1(s) + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s) + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s)G_{b1}(s)}{1 + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s) + M_1(s)G_{PWM1}(s)H_{C1}(s) + N_1(s)M_1(s)} \tag{20}$$

$$Z_{out1}^u(s) = \frac{N_1(s) + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s) + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s)G_{u1}(s)}{1 + N_1(s)M_1(s)G_{PWM1}(s)H_{C1}(s)H_{V1}(s) + M_1(s)G_{PWM1}(s)H_{C1}(s) + N_1(s)M_1(s)} \tag{21}$$

In Fig. 3, i_{L1} is the current in the inductance of the LC inverter output filter (see Fig. 1), $H_{V1}(s)$ is the transfer function associated with the voltage control loop, $H_{C1}(s)$ is the transfer function related to the current control loop, $G_{PWM1}(s)$ is the PWM transfer function and $M_1(s)$ and $N_1(s)$ are the transfer functions of the LC output filter (see Fig. 1). $G_{b1}(s)$ is the transfer function for the implementation of the virtual balanced impedance loop and $G_{u1}(s)$ is the transfer function of the virtual unbalanced impedance loop (see Fig. 3). Note that in this work, PR controllers will be used because the proposed control scheme is defined in the stationary abc frame and PR controllers can provide zero steady state error to sinusoidal signals. Therefore, $H_{V1}(s)$ and $H_{C1}(s)$ are PR controllers. The closed-loop transfer function of the proposed control scheme (see Fig. 3) is shown in (18), where $E_1^*(s)$ is the voltage reference obtained from the droop control system; $K_1(s)$ is the closed-loop transfer function of the voltage controller (19); $Z_{out1}^b(s)$ is the balanced output impedance; and $Z_{out1}^u(s)$ is the unbalanced output impedance.

Based on (18), the proposed scheme achieves a decoupled control of the voltage drop produced by the balanced current and the voltage drop caused by the unbalanced current. The first voltage can be controlled through R_1^b and L_1^b, as shown in Fig. 3 and (20). These parameters are set to be constant and they are used to implement the virtual impedance loop [13] [19]. The unbalanced voltage drop at the output of the inverter can be controlled with $Z_{out1}^u(s)$ through the transfer function $G_{u1}(s)$. From Fig. 3 and (21) it can be concluded that to control $Z_{out1}^u(s)$ there are two degrees of freedom represented by R_1^u and L_1^u respectively (see Fig. 3). From simulation work it was concluded that good results are obtained using a resistance, i.e $G_{u1}(s) = R_1^u$ (see [7]).

(18) can be rewritten in terms of balanced and unbalanced terms as shown in (22). In this equation $E_1^b(s)$ corresponds to the balanced terms in (18) and $E_1^u(s)$ is the unbalanced voltage drop produced by the unbalanced output impedance. These voltages are given by (23), from which it can be appreciated that the matrix associated with both balanced and unbalance currents is a diagonal matrix and therefore it can be concluded that based on the assumptions discussed in section III, the voltages $E_1^b(s)$ and $E_1^u(s)$ are decoupled.

In this section, inverter 1 of Fig. 2 was used as an example to show the mathematical analysis of the proposed control scheme. This scheme has also been implemented in inverter 2 of Fig. 2 and in a general way it can be implemented in "n" 4-leg converters feeding a common load.

$$E_1(s) = E_1^b(s) + E_1^u(s) \tag{22}$$

$$\begin{bmatrix} E_1^b(s) \\ E_1^u(s) \end{bmatrix} = \begin{bmatrix} K_1(s)E_1^*(s) \\ 0 \end{bmatrix} - \begin{bmatrix} Z_{out1}^b(s) & 0 \\ 0 & Z_{out1}^u(s) \end{bmatrix} \begin{bmatrix} i_1^b(s) \\ i_1^u(s) \end{bmatrix} \tag{23}$$

A. Cooperative Sharing of Imbalance between Inverters

Assuming that the inverters shown in Fig. 2 are controlled using the control methodology depicted in Fig. 3, the load voltage V_{PCC} can be written as the sum of a balanced and an unbalanced voltage. The voltage V_{PCC} as a function of the voltages and currents of inverter 1 is shown in (24). Analogously, V_{PCC} as a function of the voltages and currents of inverter 2 is given by (25). Equating these two expressions yields (26).

$$\begin{bmatrix} V_{PCC_b} \\ V_{PCC_u} \end{bmatrix} = \begin{bmatrix} K_1(s)E_1^*(s) \\ 0 \end{bmatrix} - \begin{bmatrix} Z_{out1}^b(s) + Z_{L1}(s) & 0 \\ 0 & Z_{out1}^u(s) + Z_{L1}(s) \end{bmatrix} \begin{bmatrix} i_1^b(s) \\ i_1^u(s) \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} V_{PCC_b} \\ V_{PCC_u} \end{bmatrix} = \begin{bmatrix} K_2(s)E_2^*(s) \\ 0 \end{bmatrix} - \begin{bmatrix} Z_{out2}^b(s) + Z_{L2}(s) & 0 \\ 0 & Z_{out2}^u(s) + Z_{L2}(s) \end{bmatrix} \begin{bmatrix} i_2^b(s) \\ i_2^u(s) \end{bmatrix} \tag{25}$$

$$[Z_{out1}^u(s) + Z_{L1}(s)] \cdot i_1^u(s) = [Z_{out2}^u(s) + Z_{L2}(s)] \cdot i_2^u(s) \tag{26}$$

Based on (17) and (26) the sharing principle of the proposed control scheme can be derived. This principle is shown in (27) and (28) where the line impedances are neglected for simplicity. From these equations, it is concluded that the unbalanced current in the load $i_o^u(s)$ can be shared between the inverters according to a factor which depends on the unbalanced output impedances defined in this section. These impedances can be actively controlled, through $G_{u1}(s) = R_1^u$ in inverter 1 [see (21)] and through $G_{u2}(s) = R_2^u$ in inverter 2, thus providing active control of the imbalance sharing.

$$i_1^u(s) \approx \frac{Z_{out2}^u(s)}{Z_{out1}^u(s) + Z_{out2}^u(s)} \cdot i_o^u(s) \tag{27}$$

$$i_2^u(s) \approx \frac{Z_{out1}^u(s)}{Z_{out1}^u(s) + Z_{out2}^u(s)} \cdot i_o^u(s) \tag{28}$$

Using (27)-(28) to calculate the unbalanced power in each inverter (this power is defined by the CPT as described in section II), (29) and (30) are obtained, where N_1 and N_2 are the unbalanced powers in inverter 1 and inverter 2 respectively. The unbalanced power is shared between the inverters according to the same principle as the unbalanced currents.

$$N_1 \approx 3 \cdot \left| \frac{Z_{out2}^u}{Z_{out1}^u + Z_{out2}^u} \right| \cdot E_1 \cdot I_o \qquad (29)$$

$$N_2 \approx 3 \cdot \left| \frac{Z_{out1}^u}{Z_{out1}^u + Z_{out2}^u} \right| \cdot E_2 \cdot I_o \qquad (30)$$

B. Practical Implementation of the Proposed Scheme

In section IV-A the unbalanced sharing principle was discussed, based on the insertion of virtual unbalanced output impedances into the control of the inverters. However, the insertion of large unbalanced impedances might induce large voltage imbalance at the output of the inverters, possibly exceeding regulatory limits. For this reason, the Phase Voltage Unbalance Rate index [27] [28] (PVUR, (31)) is introduced to control imbalance sharing, by adjusting the magnitude of the unbalanced output impedance in each inverter. This is achieved according to the unbalanced voltage requirement at the output of each inverter. Note that in (31) the voltages are measured with respect to the neutral point.

$$PVUR = \frac{max(|E_{an}| - \bar{E}, |E_{bn}| - \bar{E}, |E_{cn}| - \bar{E})}{\bar{E}} \qquad (31)$$
$$\bar{E} = (|E_{an}| + |E_{bn}| + |E_{cn}|)/3$$

The practical implementation of the proposed control scheme in inverter 1 of Fig. 2 is shown in Fig. 4. Both the output currents and output voltages of the 4-leg inverter are measured. With these signals and using the CPT definitions described in section II and III, the following quantities are calculated: (i) Active (P_1) and Reactive (Q_1) powers, (ii) balanced currents (i_{1abc}^b), (iii) unbalanced currents (i_{1abc}^u) and (iv) the $PVUR_1$ index at the output of the inverter. To share and regulate P_1 and Q_1, standard droop controllers are implemented. The implementation of these controllers is shown in (32), where m_1 and n_1 are the frequency and voltage droop coefficients and ω_n and E_n are respectively, the nominal frequency and voltage of the MG. Additionally, using i_{1abc}^b the voltage drop due to the virtual impedance loop is calculated [13] [19] (Fig. 3), thus improving decoupling between active and reactive power control. With i_{1abc}^u and the $PVUR_1$ index, the virtual resistance computation block shown in Fig. 4 and Fig. 5 is implemented, to adjust dynamically the value of R_1^u and therefore, the magnitude of Z_{out1}^u (21). As shown in Fig. 5, the reference for this block is the desired $PVUR_1^*$ which can be tolerated by the inverter. The control is based on a PI controller plus a low pass filter (for removing noise), whose output is R_1^u. This is multiplied by the unbalanced current to generate the unbalanced voltage reference. Through this, the magnitude of the output impedance Z_{out1}^u in inverter 1 is controlled through $G_{u1}(s) = R_1^u$ according to (21). Similarly, in the control algorithm of inverter 2 (see Fig. 2) $PVUR_2^*$ generates the output impedance Z_{out2}^u and, based on Z_{out1}^u and Z_{out2}^u the load imbalance is shared between the inverters according to (27)-(30). Note that the proposed control can adjust dynamically and in real-time the values of Z_{out1}^u and Z_{out2}^u in each inverter to operate with different degrees of load imbalance, maintaining the PVUR references ($PVUR_1^*$ and $PVUR_2^*$) in each inverter. Moreover, as shown in Fig. 7, a secondary control system could be used to dynamically regulate the values of $PVUR_1^*$ and $PVUR_2^*$

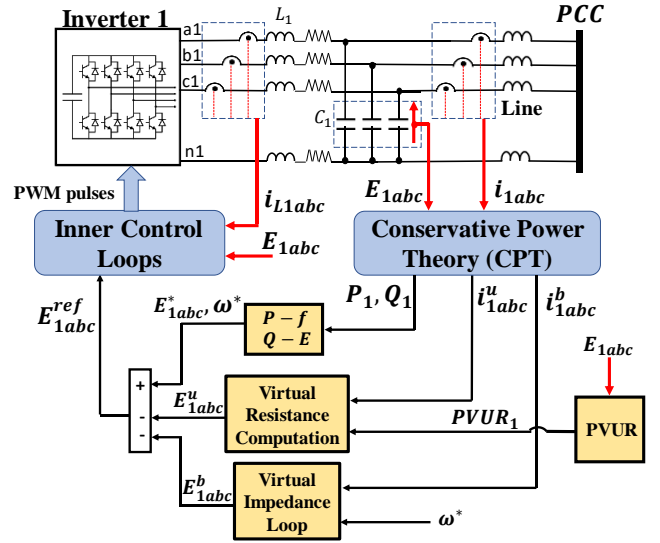controlling the *PVUR* at another point of the microgrid, for instance at the PCC.

Fig. 4. Practical implementation of the proposed control scheme. (The inverter 1 was used as an example)

$$\begin{cases} \omega^* = \omega_n - m_1 P_1 \\ E_1^* = E_n - n_1 Q_1 \end{cases} \qquad (32)$$
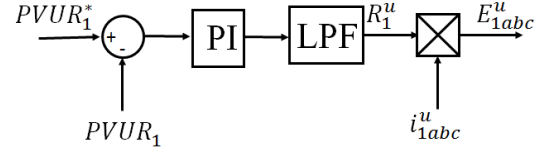

Fig. 5. Details of the virtual resistance computation block shown in Fig. 4. (Only inverter 1 is shown)

The implementation of the virtual impedance loop in inverter 1 of Fig. 2 is shown in Fig. 6 (the same methodology is used for inverter 2). In this paper, R_1^b and L_1^b (see Fig. 6) are chosen to maintain the inverter output voltage within 5% [29] of the nominal value. More information about the characteristics of this loop is presented in [13] [19]. It is worth considering that the virtual impedance loop and the virtual resistance computation block shown in Fig. 4 and Fig. 5 are decoupled since the former is implemented with the balanced current vector and the latter utilises the unbalanced current vector and these vectors are decoupled (see section III-B). The inner voltage and current control loops shown in Fig. 4 are implemented in the *abc* reference frame using self-tuning proportional plus resonant (PR) controllers in each phase [9]. Finally, it is worth remembering that an important characteristic of the proposed control scheme is its capacity for being embedded and locally implemented in each converter. Therefore, a communication channel between the converters is not required for the primary control system.
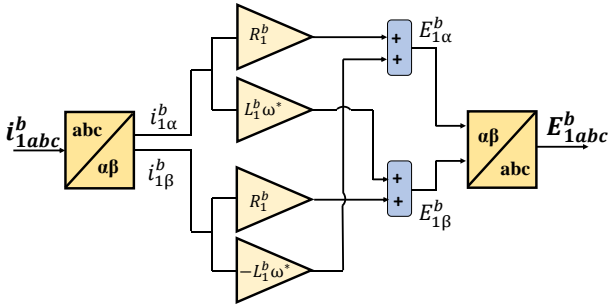
Fig. 6. Implementation of the virtual impedance loop shown in Fig. 4

C. Methodology to choose the PVUR set points for each inverter

To validate the effectiveness of the proposed cooperative imbalance sharing method, in this section, a general methodology for calculating the PVUR initial set points for "n" converters feeding a common load is proposed. It is worth remembering that the choice of these references will determine the effort of imbalance sharing in each inverter. This sharing effort is performed according to the residual power capacity of each inverter.

In this section is assumed that the unbalanced load located at the PCC (see Fig. 2) is fed using "n" inverters. In this case, the unbalanced powers defined in (29) and (30) can be generalised as shown in (33). From it, the unbalanced power N_x (see section II) in the converter "x" is given by the multiplication between the RMS voltage E_x at the output of this inverter, the RMS value of the unbalanced current at the load I_o^u and an equivalent impedance given by the current divider when "n" converters are feeding a common load   [30].

$$N_x = 3 \cdot \left| \frac{\prod_{m=1}^n Z_{out\_m}^u}{Z_{out\_x}^u \cdot \sum_{i=1}^n \frac{\prod_{j=1}^n Z_{out\_j}^u}{Z_{out\_i}^u}} \right| \cdot E_x \cdot I_o^u \tag{33}$$

The initial $PVUR_x^*$ is obtained by minimizing the cost function of (34), subject to the restrictions shown in (34). The solutions to this problem are the PVUR set points to the inverters which minimise the difference between the unbalanced powers supplied by the 4-leg converters. It should be pointed out that (34) considers the residual power capacity of each inverter. This is realised through N_x^{res} [(34) and (35)], which correspond to the residual power capability in inverter "x". Note that N_x^{res} is given by the difference between the maximum unbalanced power that this inverter can inject to the load N_x^{max} [given by (35)]   [20]- [23] and the actual unbalanced power (N_x^{actual}) that this inverter is injecting to the load. Based on that, the imbalances on the three-phase four-leg MG studied in this work, are shared according to the residual power capacity of each inverter. Moreover, the optimisation problem shown in (34) has inequality restrictions, which characterise the voltage requirements at the output of each inverter. These requirements depend on the type of load which is connected at the output of them., If a sensitive load is connected at the output of inverter "x", the maximum PVUR allowed is set to 1% ($a_x = 1\%$) [7]. In contrast, if a non-sensitive load is connected at the output of the inverter "x", the maximum PVUR allowed is 3% ($a_x = 3\%$) [17]. Finally, based on the PVUR restrictions in each inverter, the optimization problem is solved and the optimal imbalance

sharing among the converters is achieved. Note that in (34)-(35), "n" represents the number of converters which are feeding the common load. It should be pointed out that in (35), S_x is the apparent power of inverter x, P_x, and Q_x are respectively the active and reactive powers in that inverter, which are calculated using the CPT definitions (see section II).

$$\begin{cases} Min \ J = \sum_{x=1}^n \sum_{y>x}^n \left| \frac{N_x}{N_x^{res}} - \frac{N_y}{N_y^{res}} \right| \\ \qquad s.t \\ \quad PVUR_x \le a_x \qquad x = 1, 2, \dots, n \end{cases} \tag{34}$$

$$N_x^{res} = N_x^{max} - N_x^{actual} \ , \ \ N_x^{max} = \sqrt{S_x^2 - P_x^2 - Q_x^2} \ , \tag{35}$$
$$x = 1, 2, \dots\dots n$$

In (34), the unbalanced powers in the inverters are calculated using (33). Therefore, to solve this optimisation problem it is necessary to find the explicit relation for the PVURs in each inverter. For the sake of simplicity, the PVUR index of (31) can be approximated by (36). In this case, E_n is the nominal voltage of the MG. The difference between (31) and (36) is that the average voltage $\bar{E}$ defined in (31) is replaced by the nominal system voltage E_n in (36). This assumption is based on: (i) the NEMA definition for voltage imbalance, also known as the line voltage unbalance rate (LVUR), where it is assumed that the average voltage is always equal to the rated value [31] [32] and (ii) Since the maximum imbalance at the inverters' output is regulated according to the ANSI C84.1-2006 standard, the average voltage $\bar{E}$ is close to the nominal voltage E_n of the MG.

$$PVUR = \frac{Max(|E_a| - E_n, |E_b| - E_n, |E_c| - E_n)}{E_n} \tag{36}$$

Using (36), an explicit equation for the PVUR is derived. This is realised for inverter "x" (for the rest of the converters it is the same procedure). Using Fig. 4 it can be concluded that the voltage at the output of inverter "x" ($\underline{E}_x^{ref}$) is given by (in vector format): $\underline{E}_x^{ref} = \underline{E}_x^* - \underline{E}_x^b - \underline{E}_x^u$, where $\underline{E}_x^*$ is the voltage reference given by the conventional $P - f$ and $Q - E$ droop controllers; $\underline{E}_x^b$ is the voltage drop produced by the virtual impedance loop (see Fig. 6); and $\underline{E}_x^u$ is the unbalanced voltage reference produced by the virtual resistance computation block shown in Fig 4.   Using Fig. 5 it can be concluded that $\underline{E}_x^u$ is obtained by the product of the unbalanced current vector at the output of the inverter (in this case $\underline{i}_x^u$) and the virtual resistance R_x^u programmed in the control system of that inverter. Using (36), the $PVUR_x$ of the inverter "x" is given by (37) [considering voltages and currents in phasor format].

Applying the Max function to (37) yields (38) which can be written as a function of the infinite norm and the Euclidean norm, as shown in (39).
Because these norms meet the triangular inequality, $PVUR_x$ can be bounded superiorly as shown in (40). Finally, (40) can be rewritten as (41).

In (41), the magnitude of the balanced voltage phasors $\dot{E}_{a\_x}^*$, $\dot{E}_{b\_x}^*$ and $\dot{E}_{c\_x}^*$ are equal since these values are manipulated by the reactive power droop controller. Moreover, because the voltage variation is small, these magnitudes can be

approximated to the nominal voltage of the MG E_n [13] [19]. Assuming that the voltage drop caused by the virtual impedance loop is negligible since it has been designed to drop the output voltage by less than 5% of the nominal value [29] [33], it can be assumed that $\left|\dot{E}^*_{a\_x} - \dot{E}^b_{a\_x}\right| = \left|\dot{E}^*_{b\_x} - \dot{E}^b_{b\_x}\right| = \left|\dot{E}^*_{c\_x} - \dot{E}^b_{c\_x}\right| \approx E_n$. Therefore, (41) can be rewritten as shown in (42) (a restriction of this problem). From (42) it is concluded that the $PVUR_x$ at the output of inverter "x" is bounded superiorly by an expression which is a function of (i) nominal voltage of the MG (E_n), (ii) the modulus of the

achieves cooperative imbalance sharing among the 4-leg inverters and at the same time, maintains the voltage imbalances within acceptable levels at the inverter outputs. Obviously, the unbalanced voltage requirements at the inverter outputs will determine the cooperative sharing effort of them. In this context, the unbalanced voltage requirements at the PCC is a less important concern. This is because it is assumed that non-sensitive loads are connected at this point. In addition, a secondary control scheme is proposed to regulate the unbalanced voltage at the PCC: it is shown in Fig. 7

$$PVUR_x = \frac{Max\left(\left|\dot{E}^*_{a\_x} - \dot{E}^b_{a\_x} - R^u_x \cdot i^u_{a\_x}\right| - E_n, \left|\dot{E}^*_{b\_x} - \dot{E}^b_{b\_x} - R^u_x \cdot i^u_{b\_x}\right| - E_n, \left|\dot{E}^*_{c\_x} - \dot{E}^b_{c\_x} - R^u_x \cdot i^u_{c\_x}\right| - E_n\right)}{E_n} \tag{37}$$

$$PVUR_x = \frac{Max\left(\left|\dot{E}^*_{a\_x} - \dot{E}^b_{a\_x} - R^u_x \cdot i^u_{a\_x}\right|, \left|\dot{E}^*_{b\_x} - \dot{E}^b_{b\_x} - R^u_x \cdot i^u_{b\_x}\right|, \left|\dot{E}^*_{c\_x} - \dot{E}^b_{c\_x} - R^u_x \cdot i^u_{c\_x}\right|\right)}{E_n} - 1 \tag{38}$$

$$PVUR_x = \frac{1}{E_n} \left\| \begin{pmatrix} \dot{E}^*_{a\_x} - \dot{E}^b_{a\_x} - R^u_x \cdot i^u_{a\_x} \\ \dot{E}^*_{b\_x} - \dot{E}^b_{b\_x} - R^u_x \cdot i^u_{b\_x} \\ \dot{E}^*_{c\_x} - \dot{E}^b_{c\_x} - R^u_x \cdot i^u_{c\_x} \end{pmatrix} \right\|_\infty - \frac{1}{\sqrt{3}} \left\| \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix} \right\|_2 \tag{39}$$

$$PVUR_x \le \frac{1}{E_n} \left\| \begin{pmatrix} \dot{E}^*_{a\_x} - \dot{E}^b_{a\_x} \\ \dot{E}^*_{b\_x} - \dot{E}^b_{b\_x} \\ \dot{E}^*_{c\_x} - \dot{E}^b_{c\_x} \end{pmatrix} \right\|_\infty + R^u_x \cdot \frac{1}{E_n} \left\| \begin{pmatrix} i^u_{a\_x} \\ i^u_{b\_x} \\ i^u_{c\_x} \end{pmatrix} \right\|_\infty - \frac{1}{\sqrt{3}} \left\| \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix} \right\|_2 \tag{40}$$

$$PVUR_x \le \frac{1}{E_n} Max\left(\left|\dot{E}^*_{a\_x} - \dot{E}^b_{a\_x}\right|, \left|\dot{E}^*_{b\_x} - \dot{E}^b_{b\_x}\right|, \left|\dot{E}^*_{c\_x} - \dot{E}^b_{c\_x}\right|\right) + R^u_x \cdot \frac{1}{E_n} Max\left(\left|i^u_{a\_x}\right|, \left|i^u_{b\_x}\right|, \left|i^u_{c\_x}\right|\right) - 1 \tag{41}$$

$$\begin{cases} Min\, J = 3I^u_o \sum_{x=1}^{n} \sum_{y>x}^{n} \left| \frac{\prod_{m=1}^{n} R^u_m}{R^u_x \cdot \sum_{i=1}^{n} \frac{\prod_{j=1}^{n} R^u_j}{R^u_i}} \cdot \frac{E_x}{N^{res}_x} - \frac{\prod_{m=1}^{n} R^u_m}{R^u_y \cdot \sum_{i=1}^{n} \frac{\prod_{j=1}^{n} R^u_j}{R^u_i}} \cdot \frac{E_y}{N^{res}_y} \right| \\ s.t \\ PVUR_x \le \frac{R^u_x}{E_n} \cdot Max\left(\left|i^u_{a\_x}\right|, \left|i^u_{b\_x}\right|, \left|i^u_{c\_x}\right|\right) \le a_x, \qquad x = 1,2,\dots,n \end{cases} \tag{42}$$

unbalanced current at the output of that inverter ($\left|i^u_{a\_x}\right|, \left|i^u_{b\_x}\right|, \left|i^u_{c\_x}\right|$), and (iii) the virtual output resistance of the inverter (R^u_x) . Considering that in this work the magnitude of the unbalanced output impedance ($Z^u_{out\_x}$) of inverter "x" is controlled through the virtual resistance (R^u_x) (as discussed in section IV), it can be assumed that $Z^u_{out\_x} \approx R^u_x$ [7] [34] and therefore (33) can be written as a function of virtual resistances instead of virtual impedances. Based on that, the optimisation problem introduced in (34) can be explicitly formulated as shown in (42), where the optimisation variables are the virtual resistances ($R^u_x, x = 1, \dots, n$) which are used in the controllers of each inverter. To solve this optimization problem, it is necessary to measure the current at the converters' output, the RMS value of the voltage at the output of each of them and the current in the load. This can be achieved by a simulation stage or it can be implemented in a tertiary control scheme [16].

Once (42) is solved, the PVUR set points for each converter are obtained evaluating these optimization variables in the expression of the PVUR of each converter [given by the upper bounds of the PVURs shown in (42)]. It means that the optimization problem is solved considering the worst case in the inequality restrictions.

Finally, as stated in the introduction of this work, cooperative imbalance sharing in an MG is provided at the expense of increasing voltage imbalance at the voltage buses. In this work, it is assumed that sensitive loads are located close to the inverter buses and the proposed control scheme

considering three 4-leg inverters. In this figure, the voltage at the PCC is measured, and the voltage unbalance index ($PVUR_{PCC}$) is calculated. Using the $PVUR_{PCC}$ and a desired imbalance index at the PCC ($PVUR^*_{PCC}$), a secondary control loop is implemented. The output of this secondary control is a $\Delta PVUR$ which is sent to the inverters. This $\Delta PVUR$ is subtracted from the PVUR references ($PVUR^*_1$, $PVUR^*_2$ and $PVUR^*_3$) given initially to the inverters. Fig. 7 shows that this secondary control system is simple to implement considering the previously discussed cooperative control scheme. Moreover, a relatively low communication bandwidth can be used by this centralised secondary controller [5]. In summary, in this work, a hierarchical control scheme is proposed and discussed. This hierarchical scheme consists of two control levels. In the primary level, the converters are controlled locally with the scheme shown in Fig. 3 (based on currents and voltages measured at the output of each inverter) while the secondary level corresponds to the centralised controller shown in Fig. 7 which sends $\Delta PVUR$ references signals to the inverters in order to keep the PVUR at the PCC below a given value . This secondary control topology can be easily extended to "n" converters.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

In this section, both the primary and secondary controllers depicted in Fig. 3 and Fig. 7 respectively are verified and validated. The system shown in Fig. 7 was simulated using

Plexim PLECS software and it was assumed that the converters were connected to the load through inductive line impedances of 2 mH. The three 4-leg converters are controlled considering the control scheme described in Fig. 3, which is implemented locally in each device. For the implementation of the controllers depicted in Fig. 3, no measurement of the voltage and currents at the PCC are required. However, when the secondary control system is considered, the PVUR at the PCC has to be measured.

In the simulation work it was assumed that the converters have different power ratings and they are droop-controlled systems with the following droop coefficients (32): $m_1 = m$ and $n_1 = n$ for inverter 1, $m_2 = 2m$ and $n_2 = 2n$ for inverter

Fig. 8 shows both the active power (P) and the unbalanced power (N) measured at the output of each inverter for the four steps considered. From Fig. 8(b), it is shown that in step 1, the unbalanced power supplied by the three converters to the load are equal because the line impedances are identical (2mH). Then, in step 2, when the proposed imbalance sharing algorithm is enabled (see Fig. 3) in each of the converters, the unbalanced power is supplied by the inverters to the load according to their residual power capacity. An interesting characteristic of the proposed control method is that it does not affect the performance of the $P - f$ droop controller [see Fig. 8(a)].
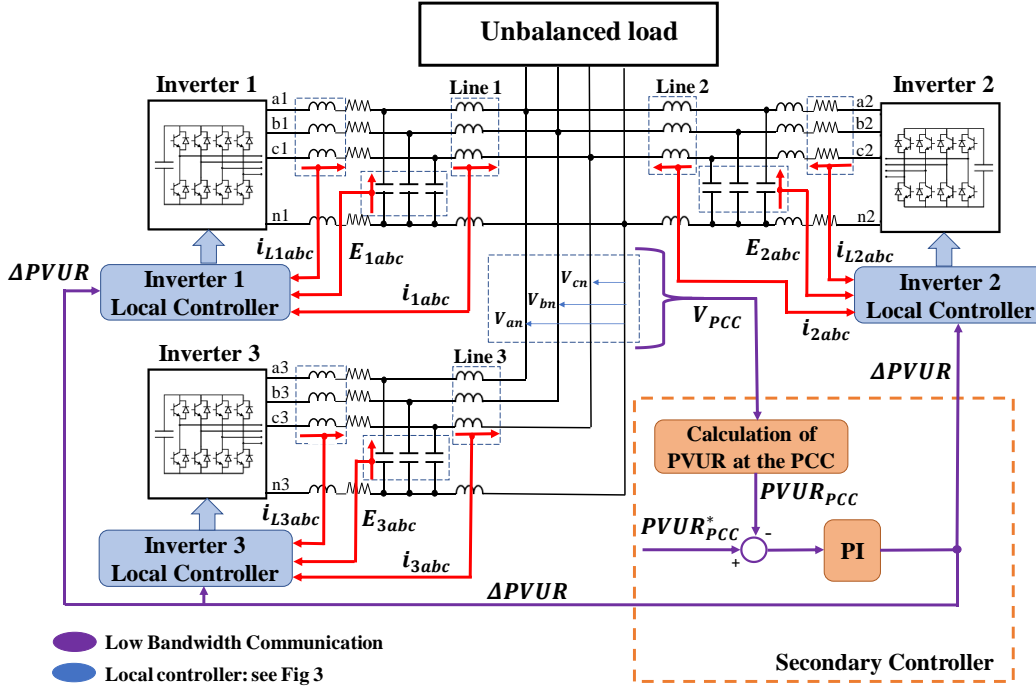

Fig. 7. Proposed secondary control scheme to regulate the voltage unbalance rate (PVUR) at the PCC

2,

and $n_3 = 3n$ for inverter 3. The value of m and n are shown in Table 1. The PVUR set points for each inverter are calculated using the methodology proposed in section IV-C as 1% for inverter 1, 2% for inverter 2 and 3% for inverter 3. These results were obtained using a genetic algorithm to solve the optimisation problem (42). At the PCC an unbalanced RL load is connected and the following power ratings for each inverter are assumed: 5000VA (inverter 1), 2500VA (inverter 2) and 1666VA (inverter 3).

Four simulation steps are considered in this work: i.e. step 1 ($0 \leq t < 3s$) in which the converters operate with the proposed control scheme shown in Fig. 3 but with the virtual unbalanced impedance loop disabled; step 2 ($3s \leq t < 6s$) in which the virtual unbalanced impedance loop in each converter is enabled; step 3 ($6s \leq t < 9s$) where the secondary control described in Fig. 7 is activated to regulate the PVUR in the PCC at 3% ; and finally step 4 ($9s \leq t \leq 12s$), where converter 1 trips at t=9s. This latter case is to evaluate the performance of the control system during a critical situation.
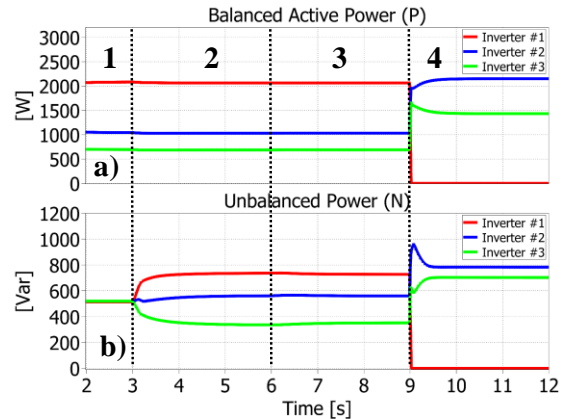

Fig. 8 (a) Active Power in the converters for the four steps studied, (b) Unbalanced Power in the converters for the four steps studied

Fig. 9 shows both the three-phase unbalanced currents and the neutral current at the output of each inverter for the steps 1 and 2. It is worth remembering that the unbalance current defined in this work contain both negative and zero sequences (see section III-A and III-B). From Fig. 9 it is concluded that

in step 1, the unbalanced currents injected by the converters (including neutral currents) to the load are identical because the line impedances are identical. In step 2, after the proposed control scheme is enabled, both three-phase and neutral currents are supplied to the load by the converters according to their residual power capacity.

Fig. 10 shows the PVURs at the output of the converters and at the PCC in the four steps studied. From this figure is can be seen that in step 1, the PVUR at the converters' output is close to zero which means that the virtual unbalanced impedance loop in each converter is not activated (see Fig. 3). In addition, the PVUR at the PCC is near to 1.7% because the load is unbalanced. From Fig. 10, can be seen that in step 2, the three
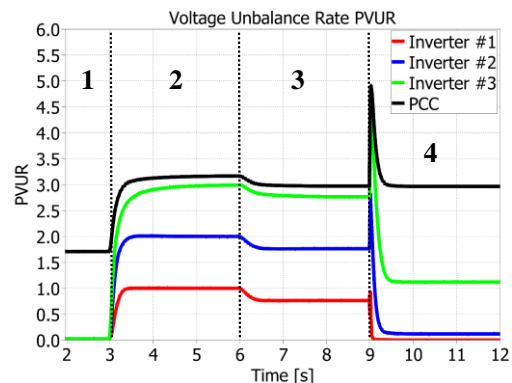

Fig. 10. PVURs in the converters and at the PCC for the four steps studied.
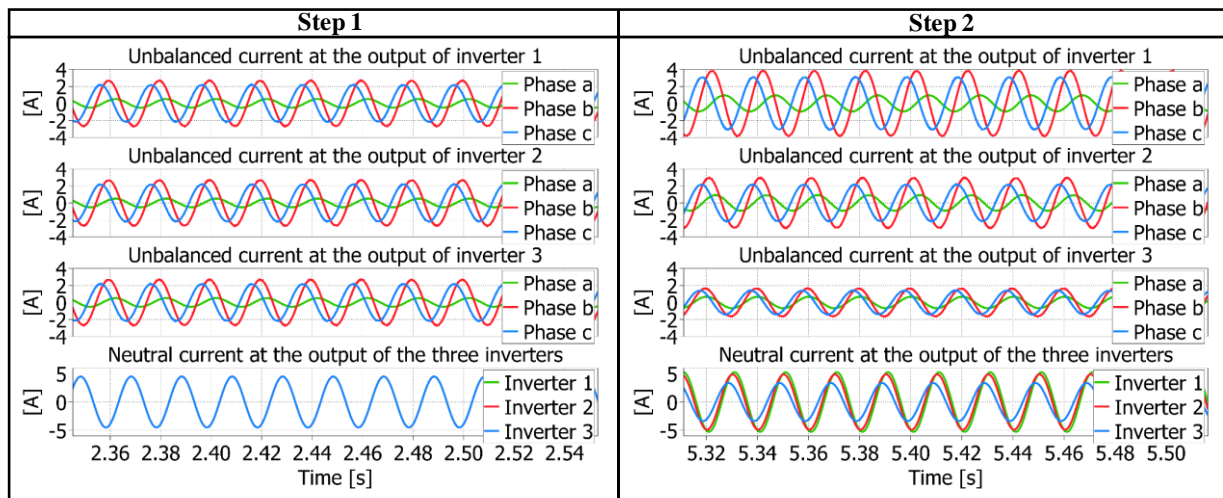

Fig. 9. Inverters' unbalanced output current waveforms at different simulation steps

PVUR set points in each converter are achieved. In this step, the PVUR at the PCC increases to around 3.3% with respect to step 1. To manage this issue, in step 3, the secondary control scheme shown in Fig. 7 is activated to regulate the PVUR at the PCC to 3%. From Fig. 10, can be seen that the proposed secondary controller effectively regulates the PVUR at the PCC to 3%. This secondary control does not interfere with the unbalanced power sharing (see step 3 in Fig. 8). Finally, in Fig. 8 and Fig. 10 step 4, is shown where inverter 1 trips at t=9s. In this case, the trip occurs when both the primary and secondary control schemes are working. From Fig. 10, it is possible to conclude that after the trip, the PVUR reference set points for inverter 2 and inverter 3 are automatically changed by the secondary control to ensure a 3% of imbalance at the PCC. These new PVUR set points are approximately 0.2% for inverter 2 and 1.2% for inverter 3.

B. Experimental Results

In this section, the performance of the control algorithm shown in Fig. 3 is experimentally validated. The system of Fig. 2 has been implemented on the experimental system shown in Fig. 11. Two Triphase units [need a ref] are used as 4-leg inverters. Inverter 1 is a Triphase PM15F120 unit (operated as a 5kW converter in this work) while inverter 2 is a Triphase PM5F42R (5kW) unit. The load at the PCC is emulated by an Ametek (9kW) programmable load. The proposed control systems are implemented in the real-time target computers controlling each of the 4-leg inverters of Fig. 11 . The inner control loops are based on self-tuning voltage and current PR controllers [9]. The parameters of the experimental system and control loops are given in Table 1.
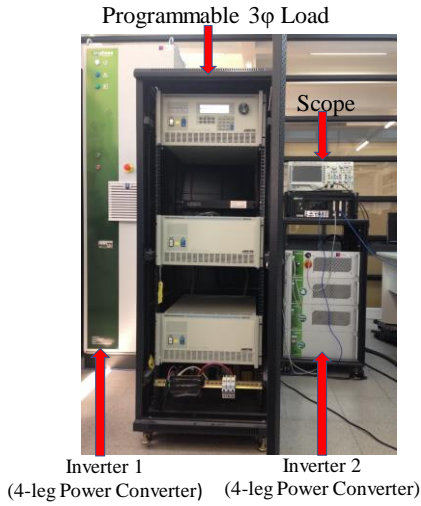
Fig. 11. Experimental system

Table 1. System Parameters in unit PM15F120* and unit PM5F42R**

Parameters	Symbol	Value

analysis, to currents that could be handled by the experimental prototype shown in Fig. 11. The pattern of the unbalanced load connected at the PCC is shown in Fig. 12.
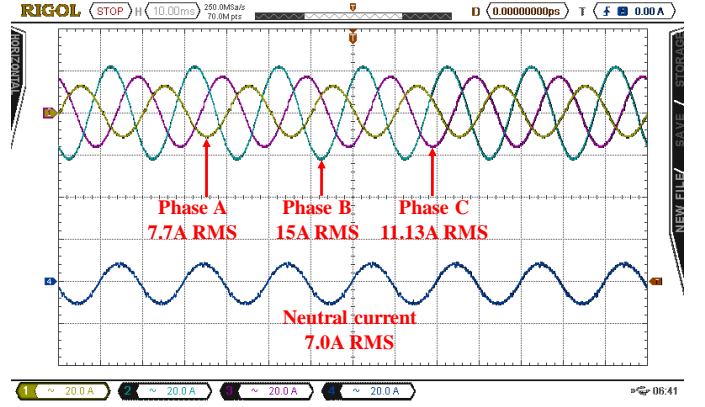

Fig. 12. Unbalanced current in the common load (20A/div)

For the experimental tests, inverter 1 is connected to the unbalanced load using an inductive line with L= 1.25mH and inverter 2 with a line inductance of 2.5mH. As both inverters
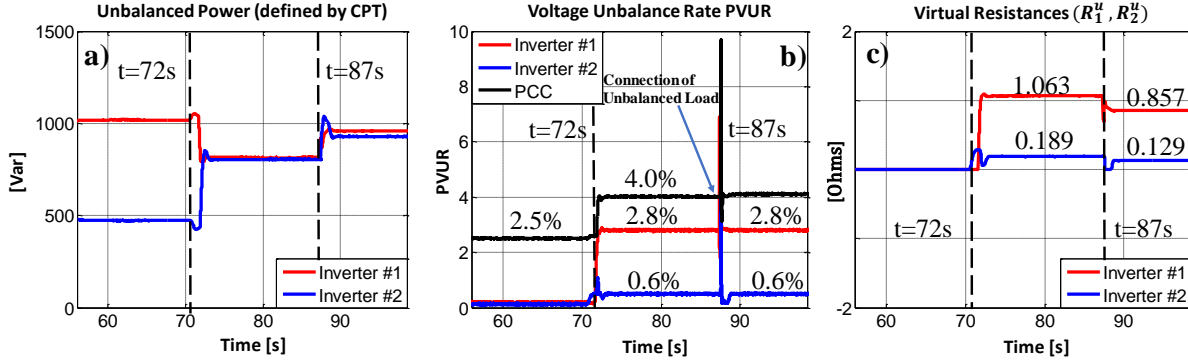

Fig. 13. (a) Unbalanced power, (b) PVUR index in both inverters and load, (c) unbalanced impedances evolution - Matlab data logging of the experimental waveforms.

Parameters	Symbol	Value
Nominal output voltage	E^*	$180V_{peak}$
Nominal angular frequency	ω^*	$2\pi\cdot50$ rad/s
Switching frequency	f_m	16kHz
DC-Link voltage	V_{DC}	720*V/520**V
Filter inductances	L	0.85*mH/0.80**mH
Filter capacitances	C	70*μF /20** μF
Voltage closed-loop	k_p	0.4*/0.12**
	k_r	20*/30**
	ω_c	0.5rad/s
Current closed-loop	k_p	0.8*/0.24**
	k_r	1000*/1000**
	ω_c	0.5rad/s
Droop coefficients	m	$1\cdot10^{-4}$rad/(W·s)
	n	$1\cdot10^{-3}$V/(Var)
Balanced virtual impedance	R^b	1Ω
	L^b	$4mH$
Unbalanced virtual impedance control loop	PI	$(0.055s+5)/s$
	LPF	$1/(1+0.031831927s)$

To validate the performance of the proposed controller, the unbalanced conditions of an MG located in Canada have been emulated at the PCC [9]. For the experimental work, the unbalanced currents reported in [9] were scaled, using per unit

have the same power rating it would be desirable that both inverters inject the same unbalanced power. Using the methodology discussed in section IV-C the references values $PVUR_1^*$ and $PVUR_2^*$ are obtained: 2.8% for inverter 1 and 0.6% for inverter 2 (both values are permitted by ANSI C84.1-2006). The first PVUR set point means that a load less sensitive to unbalance could be placed at the output of inverter 1 while the second means that a sensitive load could be connected at the output of inverter 2.

The performance of the proposed control is shown in Fig. 13. Before enabling the control system (t <72 s) the unbalanced powers are different because of the line impedances. After activating the control system, the unbalanced powers in both inverters are equal as shown in Fig. 13(a), meaning that the power imbalance sharing effort among the inverters is equal since they have the same power rating. This shows the effectiveness of the proposed control scheme.

Fig. 13(b) shows that the PVUR references are correctly achieved by each inverter. Notice that, in the experimental test shown in Fig. 13 an additional unbalanced load is connected to the PCC, at t=87 (increasing the level of current imbalance in the system). Therefore, after t=87s [see Fig. 13(a)], the

unbalanced powers in both inverters are increased. However, the PVUR set points in each inverter are successfully regulated by the proposed control scheme, even though the unbalanced currents are increased in both inverters after the load connection. This is achieved because each inverter reduces dynamically its respective unbalanced impedance to keep its respective voltage imbalance requirements, as shown in Fig. 13(c). Obviously, there is a trade-off between unbalanced power sharing and fulfilling the voltage imbalance requirements, which is shown in Fig. 13(a) after t=87s, where the unbalanced power is not shared in the same proportion.

Finally, Fig. 14 shows how active and reactive powers are not affected by the activation of the proposed controller, confirming the expected decoupling feature, i.e. conventional $P - f$ and $Q - E$ droop controllers are not influenced by the imbalance sharing control. This means also that there is a decoupling between the virtual balanced impedance loop and the virtual unbalanced impedance loop shown in Fig. 3.
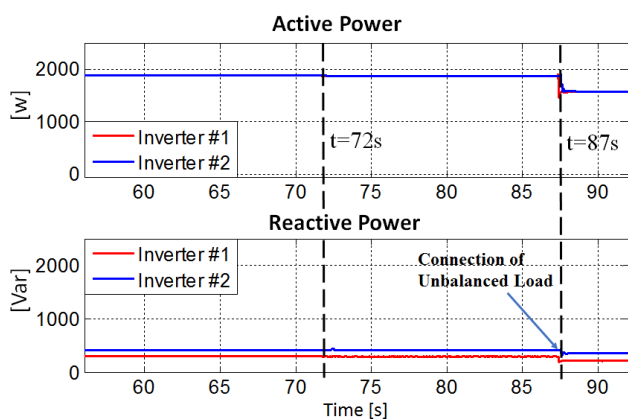

Fig. 14. Active and Reactive Powers in both inverters before and after the activation of the proposed control – Matlab data logging of the experimental waveforms.

the unbalanced voltage in the inverters is increased, to achieve a cooperative current imbalance sharing among the inverters. After 72s, it is possible to see that transient response of the proposed scheme is less than 3s. The same is seen after t=87s, when an additional unbalanced load is connected to phase "A" at the PCC.

C. Extension to Harmonics Sharing

The proposed imbalance sharing control scheme can be used to share harmonics if the common load is non-linear. Therefore, the proposed control scheme shown in Fig. 3 can be implemented using the void current, (7), instead of the unbalanced current. Moreover, the unbalance index PVUR can be replaced by the Total Harmonic Distortion of the voltage at the inverter output. This THD is calculated in real-time by the real-time computer used to control the inverters shown in Fig. 11.

To validate the control system proposed for harmonic sharing, the line impedances from the experimental test discussed in the previous section are maintained and a programmable load is connected at the PCC of the experimental system. This load is controlled to operate as a 3ϕ nonlinear load without neutral, absorbing the distorted currents shown in Fig. 16. Results are depicted only for the 5th harmonic component of the current because this is the main contributor to the THD for the current shown in Fig. 16. In Fig. 17, void powers (see section II) – including the effect of all the harmonics – and 5th harmonic currents are shown before and after the activation of the proposed control at t=83s. Before enabling the control system, noting that the inverters have different line impedances with line impedance of inverter 1 being smaller than that of inverter 2, the void power and the fifth harmonic current supplied by inverter 1 to the load is higher than inverter 2. After activating the sharing control with an output voltage THD set point of 3.0% for inverter 1 and a THD of 2.8% for the output voltage in inverter 2, the sharing profile is changed and now, inverter 2
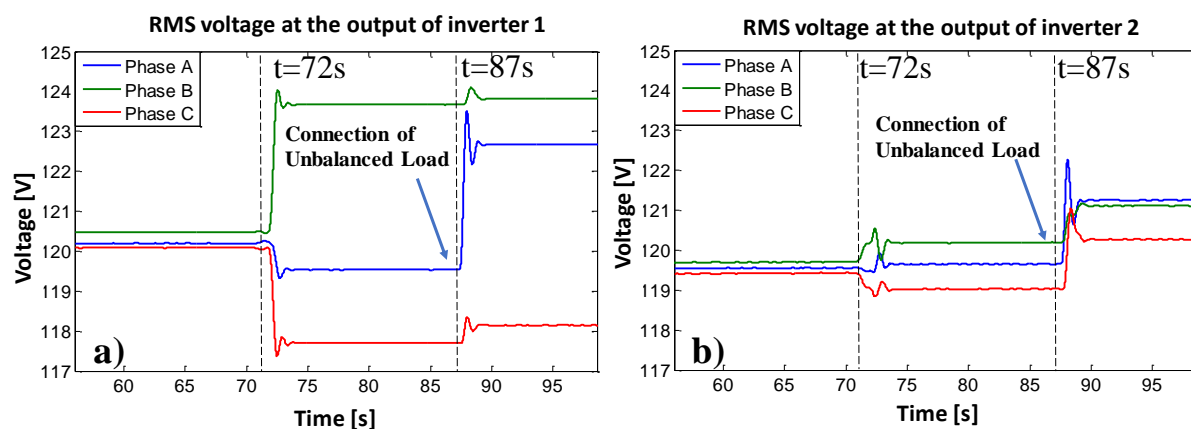

Fig. 15. (a) RMS voltages at the output of inverter 1, (b) RMS voltages at the output of inverter 2, (the load impact is applied to phase A) - Matlab data logging of the experimental waveforms.

Fig. 15 shows the effective (RMS) voltages at the output of the inverters during this test, where it is possible to see the dynamic performance of the proposed cooperative imbalance sharing method. The control is enabled at t=72s and after that,

injects most of the harmonic current content of the load. Fig. 17(c) shows that these THD set points are achieved by the local controllers of the inverters. To analyse the THD of the 5th harmonic current in both inverters before and after the activation of the proposed control, a Hioki 3196 Power

Analyser has been used. Before t=83s, the 5th harmonic current THD is 14.67% in inverter 1 and 7.45% in inverter 2. Following control activation, this index changes to 7.74% for inverter 1 and 15.43% for inverter 2. This result shows that the sharing of the 5th harmonic power and current can be effectively modified using the proposed control scheme. These results match with the results shown in Fig. 17(b). Note that the objective here is not to reduce the THD of the voltage at the PCC, but to modify how the harmonic components of the load current are shared between the two inverters. This is achieved by controlling the THD in the voltage at the output of the inverters. Whether the nonlinear load has neutral, third harmonic current will flow through the neutral wire. In this case, the implementation of the proposed control scheme discussed in this section is the same, but now the 5th harmonic is replaced by the 3rd harmonic. In this case, the proposed control scheme achieves a sharing of the 3rd harmonic between the phases of the inverters and also between their neutrals. It is worth remembering that the void current defined by the CPT (7) contains the harmonics present in the current [20]- [23] and therefore a specific harmonic can be selected from this current using a suitable filter and based on it, the proposed control scheme of Fig. 3 can be implemented. Alternatively if the whole void current is utilised in the control system of Fig. 3, then the sharing of all the current harmonics could be regulated.
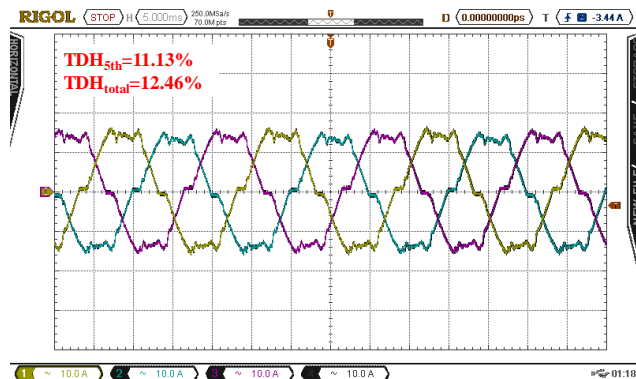

Fig. 16. Characteristics of the harmonic load (10A/div)

VI. Conclusions

In this paper, a new control algorithm for sharing load imbalance between inverters in a droop controlled MG has been presented. The proposed control scheme is based on the conservative power theory (CPT) to achieve the sharing objective in the *abc* reference frame, decoupled from the other control loops. The operating principle is based on decomposing the inverter current into balanced and unbalanced components according to the CPT, and on the concept of unbalanced virtual output impedance, implemented in the inverters' control loops. These unbalanced impedances are only seen by the unbalanced components of the inverter currents, and the impedance can be actively controlled to modify the sharing of the unbalanced components of the load current between the two inverters. Experimental results obtained from a laboratory scale microgrid confirmed the effectiveness of the sharing strategy, as well as the absence of any interference or cross coupling with the droop controller. The extension of the proposed control scheme for sharing harmonics is discussed and an experimental validation of this extension is provided. The proposed control scheme can work effectively when there are load transients in the MG. The main differences of the proposed imbalance sharing algorithm with those previously reported in the literature can be summarized
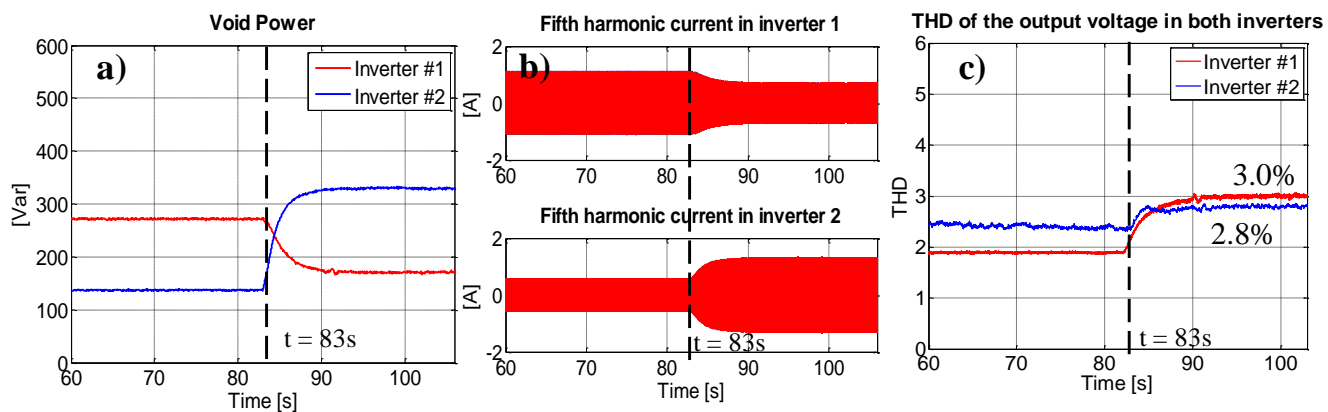

Fig. 17. (a) Void powers in both inverters, b) 5th harmonic current at the output of the inverters before and after the activation of the proposed control, and c) THD of the voltage at the output of the inverters – Matlab data logging of the experimental waveforms.

as: (i) The proposed scheme does not require sequence separation algorithms, (ii) a new method to define the preliminary unbalanced voltage set points is proposed, and

(iii) contrary to the only paper where a control scheme for cooperative imbalance sharing in 4-wire MGs [7], the proposed control scheme can be easily extended to harmonics as it does not require sequence separation algorithms. The extension of it to a harmonic load was discussed and experimental results of its performance were provided.

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