Effect of indium doping on the electrical and structural properties of TiO_2 thin films used in MOS devices

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Abstract

We investigated the effect of Indium (In) doping on the structural and electrical properties of Ti/Au/ TiO_2:In/n-Si metal-oxide-semiconductor (MOS) devices. Sputtering grown TiO_2 thin films on Si substrate were doped using two In-films with 15 nm and 50 nm thicknesses leading to two structures named Low Indium Doped (LID) sample and High Indium Doped (HID) sample, respectively. XRD analysis shows no diffraction pattern related to Indium indicating that In has been incorporated into the TiO_2 lattice. Current-Voltage (I-V) characteristics show that rectification ratio at 2V is higher for HID sample than for LID sample. Evaluated barrier height, ϕ_{B0}, decreased while the ideality factor, n, increased with decreasing temperature. Such behavior is ascribed to barrier inhomogeneity that was assumed to have a Gaussian Distribution (GD) of barrier heights at interface. Evidence of such GD was confirmed by plotting ϕ_{B0} versus n. High value of mean barrier $\overline{\phi}_{B0}$ and lower value of standard deviation (σ) of HID structure are due to indium doping which increases the barrier homogeneities. Finally, estimated Richardson constants A* are in good agreement with theoretic values (112 A/cm^2K^2), particularly, for the HID structure.

keywords

Indium doped TiO_2, Thermionic emission, Schottky barrier height, Electrical characterization, Temperature effect.

1. Introduction

Titanium dioxide (TiO_2) is an abundantly accessible semiconductor material with high thermic and oxidative potential, high refractive index, chemically/thermally stable and low leakage current density [1,2]. With its wide bandgap energy (3.20 eV for anatase and 3.02 eV for rutile phase), it has been utilized in numerous applications such as photo-catalysis [3], sensors [4], solar cells [5], memory devices [6], self-cleaning surfaces [7], water and air purification [8], Schottky barrier diodes (SBDs) [9] and photoactive uses under UV light illuminations [10]. Various types of metals and non-metals materials have been added to TiO_2 to enhance its properties and make it suitable for new device applications [11]. Incorporating some metals into TiO_2 could inhibit formation of donor/acceptor centers, resulting a change in electronic charge carriers concentration and related semiconducting properties in a controlled manner [12]. So far, such doping effect has been successful with In, Ag, Cr, Fe, Co, Au, Mn, Ni and Zr metals [13]. Among these transition metals, indium (In) is capable to enhance TiO_2 properties because of its specific characteristics such as various oxidation states (In^0, In^{+1}, In^{+3}), higher electron production due to its vacant d-orbits, trapping and mobility [14,15].

In recent years, experimental studies on TiO_2 based SBDs have shown the importance of an insulator layer at the metal-semiconductor (M/S) interface [16,17]. Such an interfacial insulating layer impacts the device characteristics such as interface state density, ideality factor and Schottky barrier height

(SBH) [18–21]. To understand the current-conduction mechanisms or formation of the barrier at M/S interface, I–V characteristics are investigated over a wide range of temperatures. Altuntaş et al. [22] examined Au/TiO_2/n-Si SBDs and observed non-ideal current–voltage–temperature (I–V–T) characteristics in the temperature range 80–400K. TiO_2 was deposited on n-Si substrates by reactive magnetron sputtering. This temperature behavior has been explained on the basis of thermionic emission (TE) theory with double Gaussian Distribution (GD) of barrier heights (BHs) due to BH inhomogeneities at M/S interface. Whereas, metal-doped TiO_2 with an interfacial layer in Schottky structures may lead to different transport phenomena. Sönmezoğlu et al. [23,24] investigated the electrical characteristics of Au/TiO_2:Sb/n-Si metal-oxide-semiconductor (MOS) device, and concluded that Fowler–Nordheim tunneling is the dominant current-conduction mechanism due to a large defect density at the interface. Taşdemir et al. [13] investigated the ideality factor (n), barrier height (ϕ_{B0}), series resistance (R_s), shunt resistance (R_{sh}) and interface states density (N_{ss}) of Al/TiO_2/p-Si and Al/TiO_2:Zr /p-Si structures at room temperature, and found that Zirconium as a dopant improves the rectifying ratio and increases the barrier height. Al Saqri et al. [25] examined defects in indium doped TiO_2 thin films grown on n-Si by e-beam evaporation using current-voltage (I-V), capacitance-voltage (C-V) and Deep Level Transient Spectroscopy (DLTS). They reported that both the reverse-bias leakage current and free carrier concentration increase with increasing indium doping. To further expand Al Saqri et al. [25] work, a thorough study of the same Schottky structures Ti/Au/15nm In/TiO_2 TFs/n-Si named Low Indium Doped sample (LID) and Ti/Au/50nm In/TiO_2 TFs/n-Si called High Indium Doped sample (HID) is undertaken using forward and reverse-bias I–V characteristics over the temperature range 80 K–400 K. The impact of temperature and Indium as dopant on TiO_2 on electrical Schottky parameters (n, ϕ_{B0}, R_s), on forward and reverse current transport mechanism, on barrier inhomogeneity and on interface state density are obtained.

2. Sample structure

RF magnetron sputtering technique was used to deposit 100 nm thin films of TiO_2 on (100) n-type silicon substrates. The samples were deposited using a 2-inch TiO_2 target at a temperature of 500 ˚C in pure Argon ambient without addition of oxygen. The chamber was evacuated to a high vacuum of less than 1×10^{-8} Torr. The substrate was rotated during the deposition at a low speed to enhance the thickness uniformity of the films. Substrates were mounted on 300 mm stainless steel rotating disk where the distance between target and substrate was 150 mm. High purity argon gas (99.999%) was introduced at a rate of 22 sccm as an inert gas for plasma. Before deposition, the samples were pre-sputtered in argon plasma for 10 mins to remove any contaminants. The working pressure was set to 10^{-3} Torr and RF power was fixed at 150 W. Then, 15 and 50 nm thick In-metal films were deposited by thermal evaporation of 99.999% pure In upon TiO_2 film to change its doping concentration. In order to incorporate the indium into the TiO_2 lattice, structures were annealed for 30 minutes at 500 °C with a 15 °C/min heating and cooling ramp. Ohmic contact was formed using thermal evaporation of Al on the back-side of Si substrates. 500 µm diameter circular Schottky contacts were obtained by thermal evaporation of Titanium (Ti)-gold (Au) over TiO_2 doped films. The schematic diagram of the fabricated Ti/Au/TiO_2:In/n-Si devices is shown in **Fig.1**.

The crystal structure of In-doped TiO_2 films was examined with an ALTIMA IV X-ray diffractometer using Cu Kα radiation (λ = 1.5405 A), operating at 40 kV and 30 mA. I-V-T characteristics in the temperature range 80-400 K are performed in a Leybold-Heraeus closed-cycle helium cryostat using a Lakeshore 340 temperature controller having a 0.001 K sensitivity. Concentration of free charge carriers was determined using reverse-bias C-V characteristics at 1 MHz with an Agilent LCR meter (4980A) and a DC signal of 30mV.

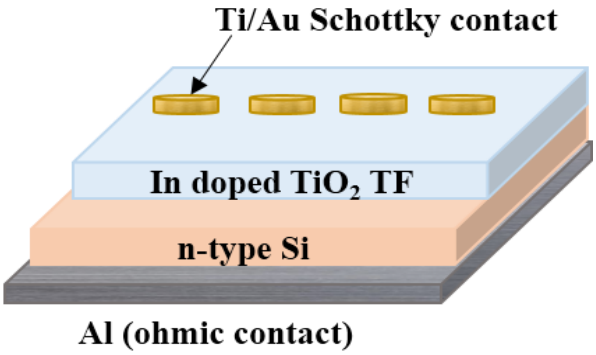

Fig.1. Schematic diagram of Ti/Au/TiO_2:In/n-Si structure.

3. Results and discussion

3.1 XRD studies of Indium doped TiO_2 thin films

The crystal quality of both LID and HID structures was examined using X-ray diffraction (XRD). Results are shown in **Fig.2.a** and **Fig.2.b**, respectively. All peaks in the XRD pattern have been identified using ASTM data. In **Fig.2.a**, peaks at 38.1° and 38.7° (2θ scale) arise from (004) and (112) reflections of TiO_2 anatase phase, respectively. Peaks at 30.5°, 43.7°, and 45.6° correspond to (222), (422) and (134) orientations arising from In_2O_3 resulting from Oxygen atoms and Indium doping atoms bounding. As illustrated in **Fig.2.b**, three main peaks are observed in the samples with 50 nm Indium film thickness, namely, (112) for TiO_2 anatase phase and (222)-(134) for In_2O_3. It is worth pointing out that (004) TiO_2 and (422) In_2O_3 peaks identified in sample LID are not present in sample HID. All prepared devices demonstrated sharp and intense peak for (112) TiO_2 orientation indicating that synthesized In-doped TiO_2 films have good crystallinity. Moreover, the favored film orientation is (112). The absence of diffraction pattern related to Indium indicates that In has been incorporated in the TiO_2 lattice.

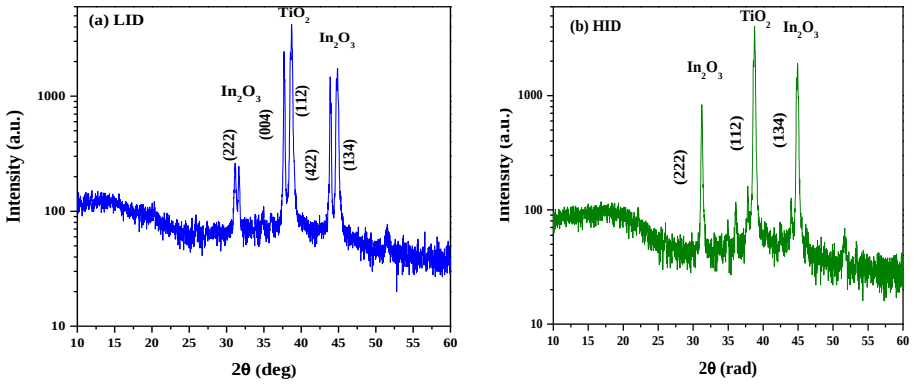

Fig. 2. X-ray diffraction patterns of (a) LID and (b) HID structures.

3.2 I-V characteristics

TE theory predicts that electrons, with energy higher than the top of the barrier, will be capable of crossing the barrier. For a M/S structure with an interfacial insulator/oxide layer native or deposited, the TE current ($V \geq 3kT/q$) relationship is given as [18,26,27]

$$I = I_0 \left[exp\left(\frac{qV - IR_S}{nkT}\right) - 1 \right] \qquad \textbf{(1)}$$

where q is electronic charge, R_s is series resistance, n is ideality factor, IR_s is the voltage drop across series resistance and I_0 is saturation current. I_0 is given as:

$$I_0 = A^* A T^2 \, exp\ \left(-\frac{q\,\phi_{B0}}{kT}\right) \qquad \textbf{(2)}$$

where k, T, A^*, A and ϕ_{B0} are Boltzmann constant, temperature in Kelvin, effective Richardson constant (112 A.cm^{-2}K^{-2} for n-type Si [26,27]), area of rectifier contact and zero bias barrier height, respectively. ϕ_{B0} is given from Eq. (2) as:

$$\phi_{B0} = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_0}\right) \qquad \textbf{(3)}$$

The ideality factor is a measure of diode conformity to pure thermionic model and is given by:

$$n = \frac{kT}{q}\ ln\left(\frac{d(V-IR_s)}{d\ ln\ I}\right) \qquad \textbf{(4)}$$

Electrical I–V measurements were performed in the temperature range 80–400 K with 20 K steps. **Fig.3** illustrates the semi-logarithmic forward and reverse I-V characteristics for LID and HID structures. For the two samples, it is found that forward bias LnI–V plots are not exactly linear and display a downward concave curvature at high voltage due to R_s rather than interface states continuum [9,28,29]. Furthermore, in the reverse bias condition, HID sample shows saturation ‘’soft’’ behavior as a function of bias, which can be assigned to the existence of a native oxide or deposited interlayer between the metal and n-Si and image force lowering of barrier height [30,31]. At room temperature, the rectifying ratio between reverse and forward bias current RR = (I_F/I_R) at 2V is estimated to be 9 for LID and 36 for HID. It is important to note that RR value is highest in HID sample. This is one of the indications that the interface charges between In-doped TiO_2 and n-Si are the lowest in HID sample.

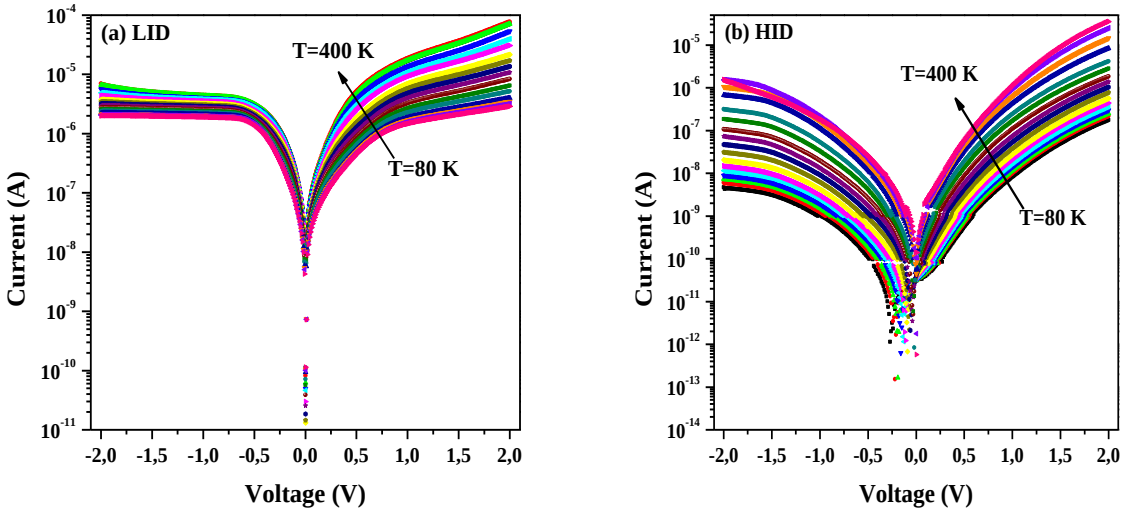

Fig. 3. Semi-logarithmic I–V plots of (a) **LID** and (b) **HID** devices in the temperature range of 80-400 K at 20 K intervals.

As determined from experimental forward I-V analysis, R_s values ranged from 482.65 kΩ to 23.84 kΩ and from 2.82 MΩ to 27.49 kΩ when the temperature was raised from 80 to 400 K for LID and HID, respectively. Sample with higher In-doping has higher R_s values. Series resistance values are higher because of the insulator effect that become more visible at low temperature [19]. Among possible sources insulator thickness, defects, and non-uniform interface distribution [32,33]**.** Experimental values of barrier height ϕ_{B0} and ideality factor n at various temperatures are calculated using **Eq.3** and **Eq.4**, respectively. They are shown in **Fig. 4**.

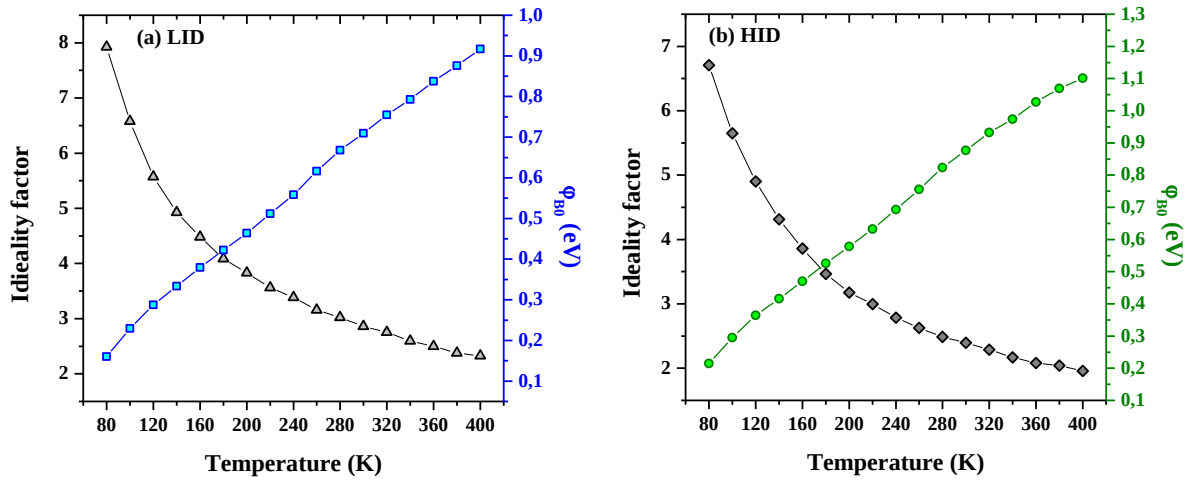

Fig. 4. Temperature evolution of Ideality factor and Zero-bias barrier height of (a) **LID** and (b) **HID**.

Fig.4 shows that the ideality factor exhibits an exponential-like increasing trend with decreasing temperature. Such behavior has been reported previously [9,22,34]. ϕ_{B0} decreases with decreasing temperature for both devices at almost the same rate. ϕ_{B0} and n changed from 0.16 eV and 7.92 (at 80 K) to 0.91 eV and 2.32 (at 400 K) for LID. These values changed from 0.21 eV and 6.70 (at 80 K) to 1.10 eV and 1.95 (at 400 K) for HID. Variation of ϕ_{B0} and n with temperature shows that current transport is temperature dependent and is far away from simple thermionic emission over the barrier at low temperatures. As temperature increases, an ever-increasing number of electrons have sufficient thermal energy to surmount higher barriers and thermionic emission dominates [35,36]. n values far bigger than unity are attributed to In-doped TiO_2 interfacial layer and specific density distribution of surface states (N_{ss}) [9,19,28,37]. At room temperature, ϕ_{B0} is 0.70 eV for LID and 0.87 eV for HID. The difference is due to effective bandgap dropping in the In-Ti-O material due to the incorporation of Indium. This value is bigger than those achieved with conventional metal/semiconductor contacts such as Al/p-Si structure, where ϕ_{B0}=0.50 eV [38]. The case may be ascribed to an oxide interlayer modifying the effective barrier height by influencing the space charge region of the substrate [39]. According to Tung's theory [40], there is a straight correlation between experimental ϕ_{B0} and n as shown in **Fig.5.**

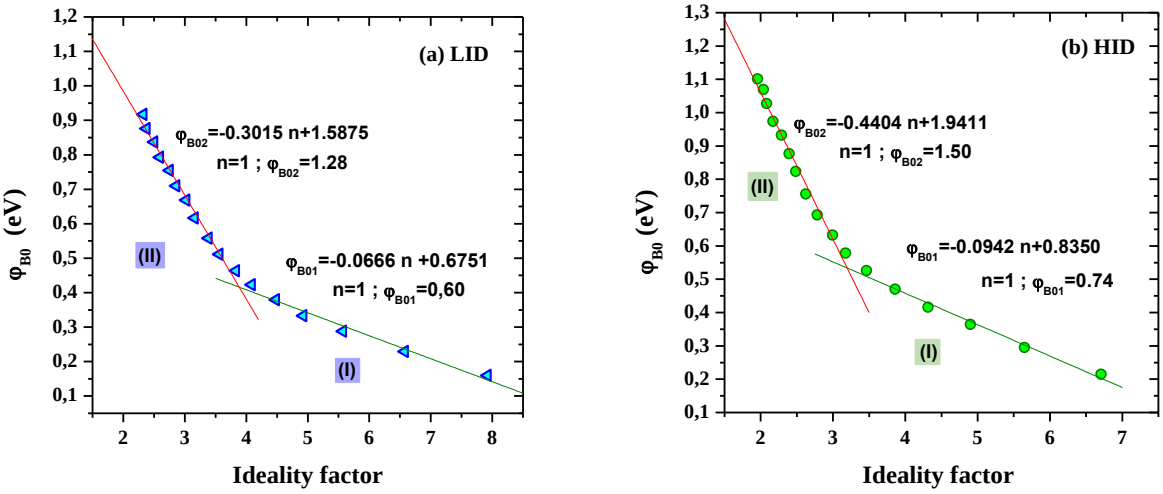

Fig.5. ϕ_{B0}versus n for (a) LID and (b) HID structures at different temperatures.

Fig.5 shows two linear regions indicating lateral inhomogeneities in barrier heights [22,41,42] and are attributed to the non-uniformity of interfacial charges, grain boundaries, a mixture of various phases, facets, defects, etc. [16,37,43–45]. One of such interface atomic structures may become dominant at a specific temperature and voltage region. The ϕ_{B0} versus n plot demonstrates two linear regions called Region (I) (from 80K to 180K) and Region (II) (from 200 K to 400 K). In Region (I), extrapolation of experimental $\phi_{B0}(n)$ line to n = 1 gives ϕ_{B0} = 0.60 eV for LID and ϕ_{B0}=0.74 eV for HID. In region (II), extrapolation of experimental $\phi_{B0}(n)$ line to n = 1 gives 1.28 eV for LID and 1.50 eV for HID, respectively. Additionally, it is observed that ϕ_{B0} value of Region (I) and (II) increase as indium doping is increased. This result proves that indium doping plays a significant role in enhancing the electrical properties and barrier homogeneity of devices. Sellai et al. [46] pointed out that barrier height found by extrapolation to n=1 may be considered as a reasonably good estimate for the homogeneous barrier height. Thus, the barrier of HID sample is more homogeneous, because the ϕ_{B0} value at n = 1 for both regions are higher than those of LID sample.

Inhomogeneities in SBHs can also be shown through ideality factor "T_0 effect or anomaly" [47]. When the temperature is lowered, the current is dominated by fewer low-SBH regions with lower effective SBHs and larger ideality factors [47,48]. The origin of T_0 effect is also attributed to interface state density distribution, quantum mechanical tunneling and image force lowering [49]. The ideality factor of diodes showing this anomaly varies linearly with temperature as:

$$n(T) = n_0 + \frac{T_0}{T} \qquad \textbf{(5)}$$

where n_0 and T_0 are constants that are independent of temperature and voltage over a wide temperature range [50,51]. In order to investigate temperature dependence of ideality factor, n versus 1000/T is plotted and shown in **Fig.6**. This figure illustrates that at higher temperatures, n is nearer to ideal case (n=1), whereas at low temperatures it increases with decreasing temperature. n exhibits a linearly change with reverse temperature. n_0 and T_0 values obtained from **Fig.6** for LID are 0.99 and 555 K, respectively. These values are higher than those obtained for HID, namely n_0 =0.77 and T_0= 484 K. The high value of T_0 might be ascribed to an interfacial native oxide layer. Without interfacial oxide, Sharma et al. [52] found a value of 205 K for Au/n-Si Schottky diode prepared by ion beam sputtering. The origin of T_0 effect is explained by the existence of a native or deposited interfacial layer, image force lowering, interface state density distribution, and barrier inhomogeneity at the M/S interface [27,40,44,53].

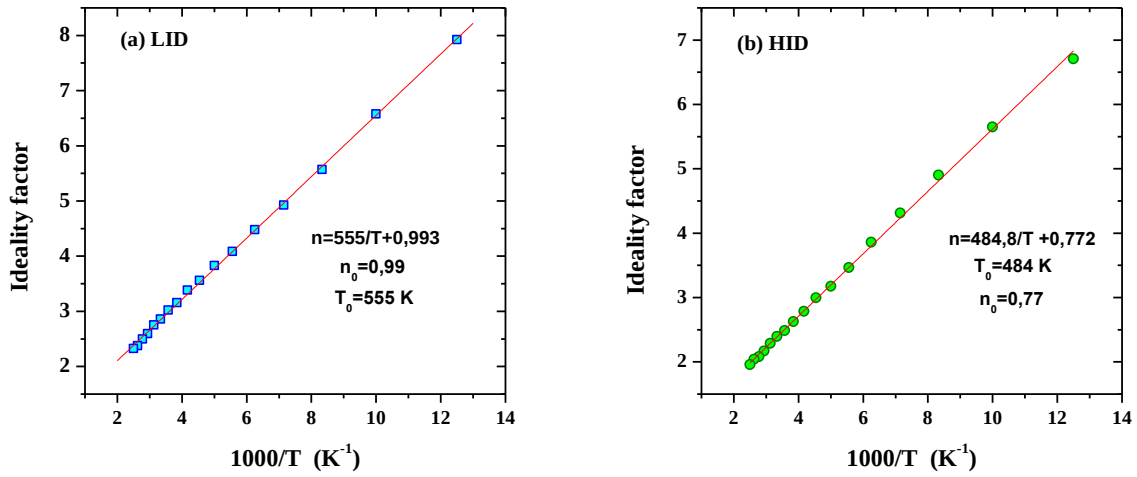

Fig.6. Linear behavior of n versus 1000/T of (a) LID and (b) HID structures.

The increase of ϕ_{B0} and decrease of n with increasing temperature may also originate from a deviation from the TE theory. Proposing that thermionic field emission (TFE) and field emission (FE) tunneling mechanisms exist at low temperatures, tunneling ideality factor n_{tun} is given as [27]:

$$n_{tun} = \frac{q\,E_{00}}{kT}\coth\left(\frac{qE_{00}}{kT}\right) = \frac{qE_0}{kT} \qquad \textbf{(6)}$$

Where E_{00} is the characteristic energy and is given by:

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_D}{m_e^*\varepsilon_s}\right)^{\frac{1}{2}} \qquad \textbf{(7)}$$

where $m_e^* = 0.19\ m_0$ is effective mass of electrons, ε_s is permittivity of Si (=11.8 ε_0) and N_D is free charge carrier concentration (calculated from reverse-bias C-V characteristics at 1 MHz as 1.89×10^{16} cm^{-3} and 5.43×10^{15} cm^{-3} for LID and HID, respectively) [26]**.** Usually, field emission (FE) is expected when $kT \ll qE_{00}$, and thermionic field emission (TFE) is expected when $kT \approx qE_{00}$ and pure thermionic emission (TE) occurs when $kT \gg qE_{00}$. Theoretical values of E_{00}were derived from **Eq. (7)** and found to be 1.70 meV and 0.91 meV for LID and HID, respectively. According to these values, the conduction mechanism at all temperatures should be governed by TE mechanism. However, the experimental values of E_{00} are generally higher because of the electric field enhancement at the semiconductor surface [54] or increasing of density of states at MS interface [55]. **Fig.7** displays n_{tun} versus temperature at different E_{00} estimated values. Filled circles represent n values calculated experimentally from I-V for LID and HID samples, respectively. These values match n_{tun} values and are found to be between 50 to 80 meV for LID and 50 to 60 meV for HID samples, respectively. Both samples have a tunneling parameter value higher than kT/q at all temperature ranges. This indicates that FE is a more effective current transport mechanism rather than TE in the Ti/Au/TiO_2:In/n-Si structure. This can be one reason of the non-ideal behavior of the structure.

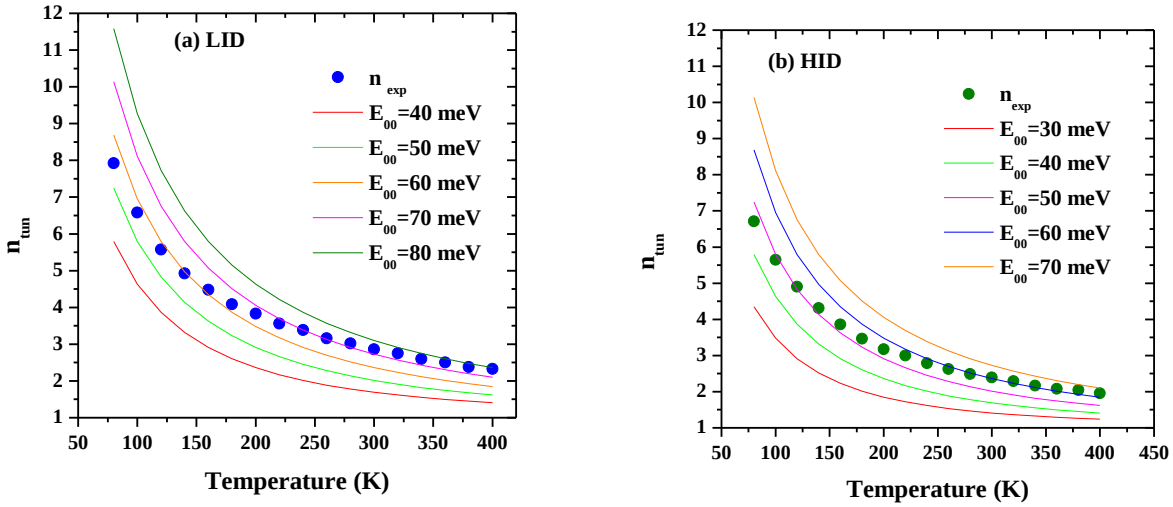

Fig.7. Temperature dependent tunneling ideality factor for various E_{00} values for (a) LID and (b) HID structures.

3.3 Current mechanisms in reverse bias

To investigate current transport mechanisms dominating reverse leakage current (I_R) through the structures, Poole-Frenkel emission (PFE) and Schottky emission (SE) models are considered [56–58]. Poole-Frenkel barrier lowering leads to the reverse leakage current given by:

$$I_R \propto E\exp\left(\frac{1}{kT}\sqrt{\frac{qE}{\pi\varepsilon_i}}\right) \qquad \textbf{(8)}$$

and the contribution to reverse current by Schottky lowering is given by:

$$I_R \propto T^2 \exp\left(\frac{1}{2kT}\sqrt{\frac{qE}{\pi\varepsilon_i}}\right) \qquad \textbf{(9)}$$

where E is maximum electric field in the junction. The plot of derived $\ln(I_R/E)$ and $\ln(I_R/T^2)$ versus $E^{1/2}$ for various temperature (80 K-400 K) for both LID and HID samples are shown in **Fig.8** and **Fig.9**, respectively. Plots give a linear behavior for Poole-Frenkel and Schottky emission and the slope can be expressed as [58]:

$$S = \frac{q}{nkT}\sqrt{\frac{q}{\pi\varepsilon_i}} \qquad \textbf{(10)}$$

where n = 1 for PFE and n = 2 for SE. Theoretically calculated slopes and slopes obtained from the fits for both PFE and SE for each temperature are tabulated in **Tab.1**.

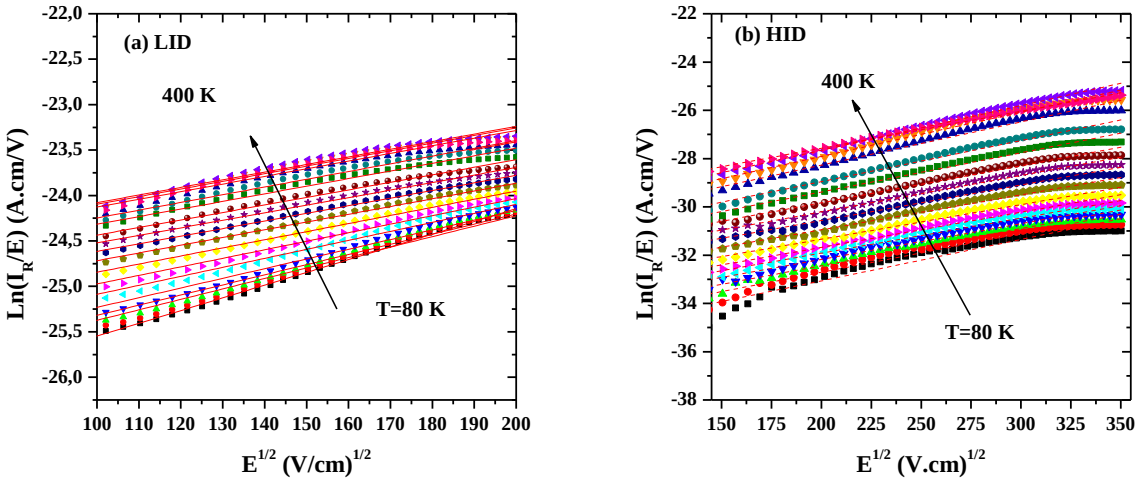

Fig.8. $\ln(I_R/E)$ versus $E^{1/2}$ for PFE mechanism of (a) LID and (b) HID sample in reverse bias region.

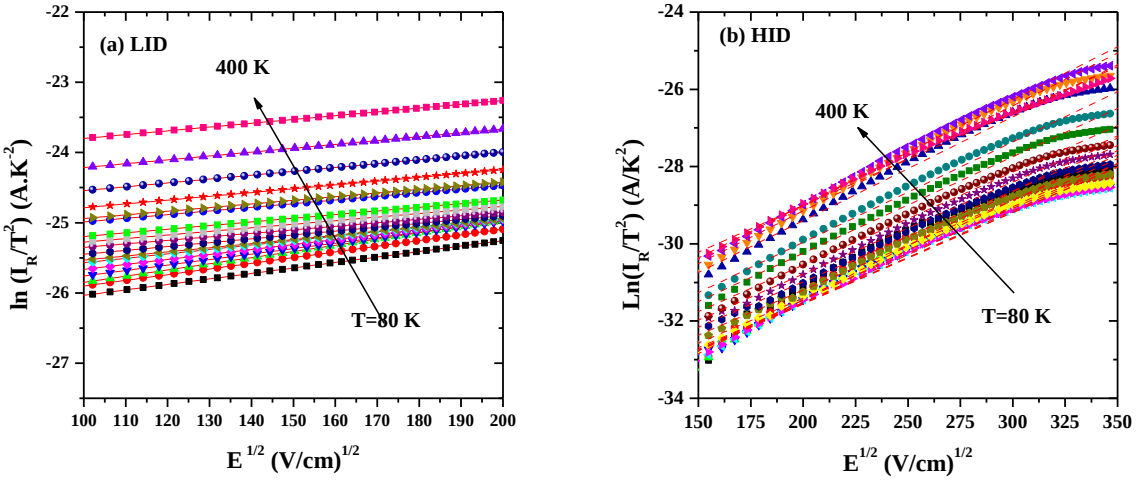

Fig.9. $\ln(I_R/T^2)$ versus $E^{1/2}$ for SE mechanism of (a) LID and (b) HID samples in reverse-bias region.

Tab.1. Calculated and experimental slopes for PFE and SE mechanisms at different temperatures in the range 80-400 K for LID and HID structures.

	LID sample		**HID sample**	
T(K)	FPE $(V/cm)^{-1/2}$	SE $(V/cm)^{-1/2}$	FPE $(V/cm)^{-1/2}$	SE $(V/cm)^{-1/2}$

	Calculated	Experimental	Calculated	Experimental	Calculated	Experimental	Calculated	Experimental
80	0.0159	0,0140	0.0100	0.0078	0.0159	0.0158	0.0079	0.0242
100	0.0127	0.0115	0.0063	0.0081	0.0127	0.0148	0.0063	0.0231
120	0.0106	0.0111	0.0053	0.0088	0.0106	0.0143	0.0053	0.0225
140	0.0091	0.0106	0.0045	0.0078	0.0091	0.0138	0.0045	0.0220
160	0.0079	0.0099	0.0040	0.0071	0.0079	0.0135	0.0040	0.0217
180	0.0071	0.0093	0.0035	0.0063	0.0071	0.0136	0.0035	0.0217
200	0.0063	0.0089	0.0032	0.0059	0.0063	0.0134	0.0032	0.0215
220	0.0058	0.0085	0.0029	0.0055	0.0058	0.0135	0.0029	0.0217
240	0.0053	0.0083	0.0026	0.0050	0.0053	0.0138	0.0026	0.0219
260	0.0049	0.0083	0.0024	0.0051	0.0049	0.0142	0.0024	0.0223
280	0.0045	0.0082	0.0023	0,0052	0.0045	0.0144	0.0023	0.0225
300	0.0042	0.0083	0.0021	0,0052	0.0042	0.0152	0.0021	0.0233
320	0.0040	0.0085	0.0020	0.0052	0.0040	0.0159	0.0020	0.0241
340	0.0037	0.0084	0.0019	0,0054	0.0037	0.0167	0.0019	0.0248
360	0.0035	0.0084	0.0018	0,0055	0.0035	0.0172	0.0018	0.0253
380	0.0033	0.0083	0.0017	0,0055	0.0033	0.0175	0.0017	0.0256
400	0.0032	0.0084	0.0016	0,0056	0.0032	0.0150	0.0016	0.0231

Based on the values in **Tab.1**, experimental slopes of LID structure are consistent with PFE in temperature range 80-200 K and SE in temperature range of 220-400 K. This suggests that in lower temperature region (T<220 K) the leakage current is observed to be dominated by PFE with a donor-like trap and thermal carrier detrapping from bulk oxide into conduction band. Therefore, this is a bulk-limited conduction process [26,29]. In this mechanism, conduction occurs due to defect states and a very small amount of carriers pass over barrier. Whereas in higher temperature region (T>220 K) Schottky emission is dominant. In this mechanism, carriers absorb thermal energy and are then emitted over the potential barrier at the interface [59], while a few carriers tunnel through the interface barrier. On the other hand, slopes of HID sample determined from the fit in all temperature range are near theoretical PFE value. Hence, reverse current in this sample in all temperature range is dominated by PFE. The wide distribution of traps in band gap may be ascribed to structural defects and/or impurities that lead to the enhancement in trapping/detrapping of charge carriers. Obviously, HID has more defect than LID sample, that made it more sensitive to temperature in the reverse bias. The origin of these defects has been reported by Setviń et al. to be donor-like traps within the TiO_2:In layer, most likely oxygen vacancies [60].

3.4 Interface barrier analysis

For BH evaluation, one may also make use of Richardson plot of saturation current. I_0 expression can be re-organized by rewriting **Eq. (2)** as:

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{q\phi_{B0}}{kT} \qquad \textbf{(11)}$$

Plots of $\ln(I_o/T^2)$ versus 1000/T for LID and HID devices are depicted in **Fig. 10.**

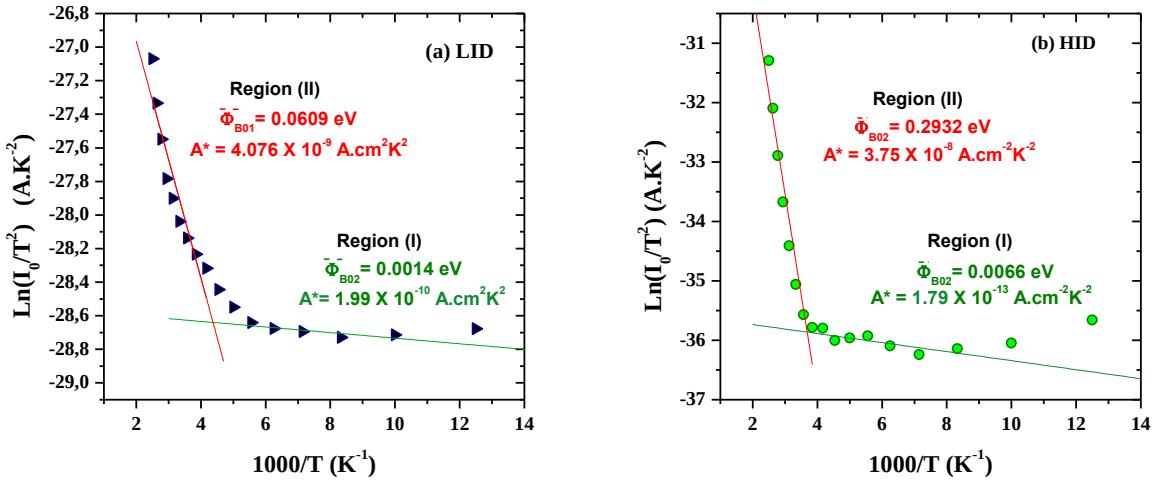

Fig.10. Richardson plots of ln(I_0/T^2) versus 1000/T for **(a) LID** and (b) **HID** Schottky diodes.

As can be seen in **Fig.10** the curves are non-linear over the experimental temperature range but display two linear regions (I) and (II) with various slopes and intercepts. Similar behaviors have been reported by several authors [22,34,42,45,48]. They were attributed to spatial inhomogeneous barrier heights and potential fluctuations at the interface that comprise low and higher barrier areas. When the temperature is lowered, the current will flow preferentially through the lower barriers in the potential distribution [22,23]. As shown in **Fig.10**, linear fitting of experimental data at low temperature region (I) (80-180K) gives Φ_{B0} and A* values from the slope and intercept. These values are 0.0014 eV and 1.99×10^{-10} A/cm^2 K^2 for LID and 0.0066 eV and 1.79×10^{-13}A/cm^2 K^2 for HID, respectively. While at high temperature region (II) (200-400K) these values were obtained as 0.0609 eV and 4.07×10^{-9} A/cm^2 K^2 for LID, and as 0.2932 eV and 3.75×10^{-8}A/cm^2 K^2 for HID, respectively. On the other hand, the values of Richardson constants are much lower than the well-established value of 112 Acm^{-2}K^{-2} for n-type Si and this can be explained by the lateral inhomogeneity of the barrier [61]. To further investigate barrier inhomogeneity, the model of Werner and Güttler [44] was used. This model introduces a GD in the BH with a mean value $\overline{\Phi}_{B0}$ and a standard deviation σ. This GD of BHs and the ideality factor can be expressed as a function of temperature and are given by following equations [62,63]:

$$\phi_{B0} = \overline{\phi_{B0}} - \frac{q\sigma^2}{2kT} \qquad \textbf{(12)}$$

$$\left(\frac{1}{n} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \qquad \textbf{(13)}$$

where ρ_2 is voltage coefficient of mean barrier height, and ρ_3 is voltage coefficient of standard deviation. It is assumed that $\bar{\phi}_{B0}$ as well as σ^2 are linearly bias dependent on Gaussian parameters, such as $\bar{\phi}_b(V) = \bar{\phi}_{B0} + \rho_2 V$ and standard deviation $\sigma^2(V) = \sigma_0^2 + \rho_3 V$ [16,44,64]. Usually the temperature reliance of σ is small and can be neglected. The plots of ϕ_{B0} and $(n^{-1} - 1)$ as a function of q/2kT are shown in **Fig.11** for LID and HID samples, respectively.

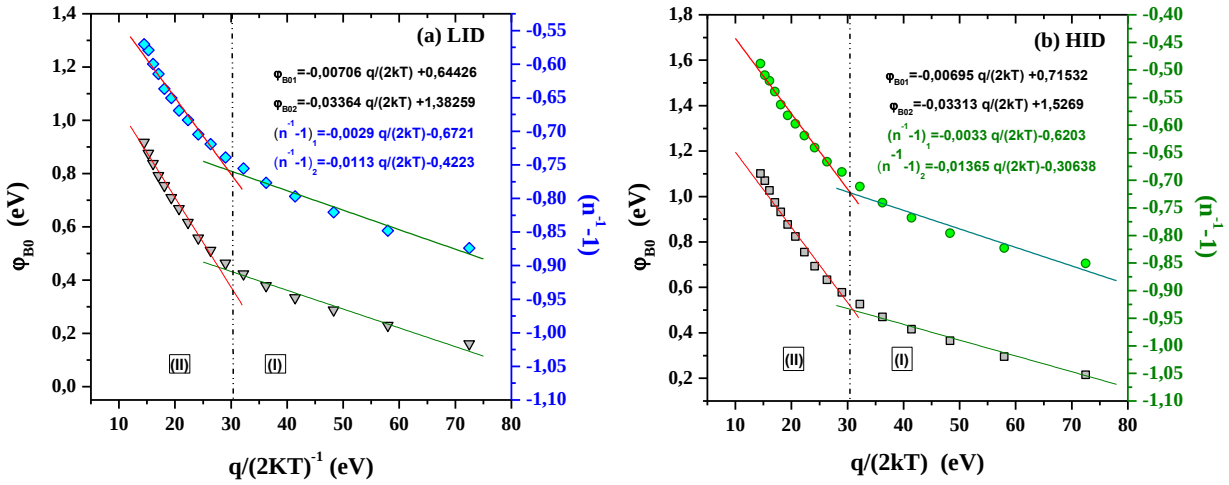

Fig.11. Zero-bias barrier height and ideality factor vs q/2kT curves of (a) **LID**, (b) **HID** devices.

Fitting experimental I–V data to Eqs **(3)** and **(4)** gives ϕ_{B0} and n, respectively, which should obey **Eqs. (12) and (13)**. Thus, experimental ϕ_{B0} versus q/2kT plot should be a straight-line with intercept at the ordinate determining $\bar{\phi}_{B0}$and slope giving σ. In our case, two straight lines rather than a single one, with a transition occurring at 180 K, are found. Intercepts and slopes gave two sets of $\bar{\phi}_{B0}$ and σ values with 0.64 eV and 0.0840 V in Region (I) and 1.38 eV and 0.1834 V in Region (II) for LID sample. For HID structures these values are 0.71 eV and 0.0834 V in Region (I) and 1.52 eV and 0.1820 V in Region (II). The standard deviation σ is a measure of barrier homogeneity; a lower σ value corresponds to a more homogenous barrier height. Accordingly, HID samples have better homogeneity and excellent electrical properties when contrasted with LID samples. Chand and Kumar [65] argued that the decrease of standard deviation leads to an increase in barrier height and a decrease in ideality factor; the same behavior has been observed here.

This study demonstrates that Au/TiO_2:In/n-Si structures have Double-Gaussian distribution. The presence of a Double-Gaussian can be credited to the nature of the inhomogeneities themselves in the two cases. This may include variation in the interface composition/phase, interface quality, electrical charges, non-stoichiometry, etc. They are important enough to electrically impact the current–voltage (I–V) characteristics of the Schottky diodes, at especially low temperatures [66]. Thus, I–V measurements at very low temperatures are capable of revealing the nature of barrier inhomogeneities present in the contact area. That is, the presence of a second Gaussian distribution at very low temperatures may conceivably arise due to some phase change taking place on cooling below a certain temperature. Furthermore, the temperature range covered by each straight-line endorses the regime where corresponding distribution is effective. In the same way, $(n^{-1}-1)$ versus q/2kT plots show for both temperature ranges two barrier height distributions. Voltage coefficients ρ_2 and ρ_3 values are acquired from intercepts and slopes of $(n^{-1}-1)$ versus q/2kT plots shown in **Fig.11**. Values for LID are 0.6721 and -0.0029 in Region (I), whereas these values are 0.4223 and -0.0113 in Region (II), respectively. For HID these coefficients change to 0.6203 and -0.0033 in Region (I), and 0.3063 and -0.0136 in Region (II), respectively. All these values are shown in **Tab.2** for comparison purposes.

Tab.2. Mean barrier height $\bar{\phi}_{B0}$, standard deviation σ and voltage deformation coefficients (ρ_2 and ρ_3) for LID and HID samples.

$\bar{\phi}_{B0}$ (eV)		σ (V)		σ^2 (V^2)		ρ_2 (V)		ρ_3 (V)	
Region (I)	Region (II)	Region (I)	Region (II)	Region (I)	Region (II)	Region (I)	Region (II)	Region (I)	Region (II)

LID	0.64	1.38	0.0840	0.1834	0.0070	0.0336	0.6721	0.4223	-0.0029	-0.0113
HID	0.71	1.52	0.0834	0.1820	0.0069	0.0331	0.6203	0.3063	-0.0033	-0.0136

As illustrated in **Tab.2**, the negative values of ρ_3 in Region (II) are greater than those of Region (I) for both samples, suggesting that Region (II) is wider and has a relatively higher BH with smaller ρ_2 and larger $-\rho_3$. Thus, it could be argued that Region (I) at very low temperatures may possibly arise due to some phase change taking place on cooling below a certain temperature. Furthermore, it is found that values of σ^2, ρ_2 and ρ_3 decreased by increasing indium doping. Thus, $\bar{\Phi}_{B0}$ value increases as the indium doping is increased. However, σ^2 value of HID sample decreased with decreasing ρ_3 leading to an increase in barrier height. This confirms that HID samples have better barrier homogeneity and electrical properties than LID samples.

As mentioned above, the conventional Richardson $\ln(I_o/T^2)$ versus 1000/T plot has demonstrated two linear regions. According to Gaussian distribution of the BH, **Eq. (11)** changes to:

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\,\sigma^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\phi}_{B0}}{kT} \qquad \textbf{(14)}$$

Fig.12 shows modified $\ln(I_0/T^2) - q^2\sigma^2/2k^2T^2$ versus q/kT plots of LID and HID structures. This figure shows two straight lines, and according to **Eq.(14)**, the slope of these straight lines yields the mean BHs $\bar{\Phi}_{B0}$ and intercepts $\ln(AA^*)$ at ordinate and thus A^* for a given rectifier contact area A. The $\ln(I_0/T^2) - ((q^2\,\sigma^2)/(2k^2T^2))$ values were calculated for both σ values obtained in Region (I) and Region (II). For LID samples, $\bar{\Phi}_{B0}$ and A^* were found to be 0.63 eV and 198.11 A/cm^2 K^2 in the temperature range 80-180 K, and 1.35 eV and 124.91 A/cm^2 K^2 in the range 200-400 K, respectively. For HID samples, $\bar{\Phi}_{B0}$ and A^* values are 0.72 eV and 141.89 A/cm^2 K^2 in 80–180 K range, and 1.50 eV and 111.68 A/cm^{2}K^2 in 200-400 K range, respectively. It is clear that zero-bias mean BH values are very close to mean BHs obtained from φ_{B0}versus q/2kT plots in **Fig.11**. The obtained Richardson constant values are close to theoretical value of 112 A/cm^2 K^2 for n-Si especially in Region (II) for HID samples.

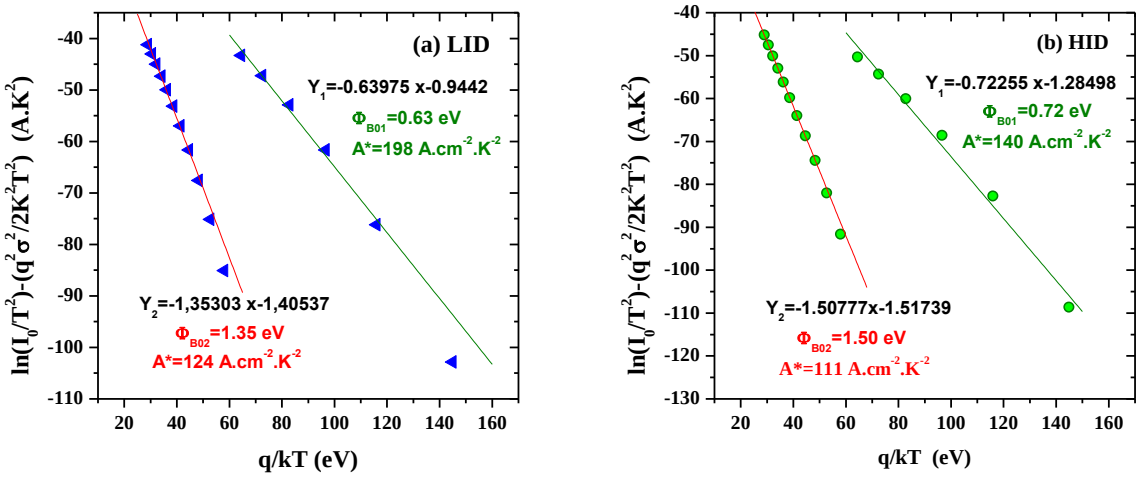

Fig.12. Modified Richardson $\ln(I_0/T^2) - q^2\sigma_0^2/2(k^2T^2)$ vs q/kT plots for (a) LID and (b) HID structures.

3.5 Effect of interface state density and series resistance

Energy density distribution profiles of interface states (N_{ss}) for Ti/Au/TiO_2:In/n-Si structures were obtained by taking into account voltage dependent BH and ideality factor, are given in **Fig.13.** According to Card and Rhoderick [18], for M/S type SBD with a native or deposited interfacial layer, N_{ss} can be simplified and is given by:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \qquad \textbf{(15)}$$

where δ is the thickness of interfacial oxide layer, W_D is space charge width, ε_s ($= 11.8\ \varepsilon_0$) and ε_i($= 48\ \varepsilon_0$ TiO_2 [18]) are permittivity of semiconductor and interfacial layer, respectively. W_D values of LID and HID structures were calculated from C^{-2} vs reverse bias V at 1 MHz, and are found to be 2.87×10^{-5} cm and 6.40×10^{-5} cm, respectively. δ values were found from the interfacial layer capacitance at 1 MHz ($C_i = \varepsilon_i\varepsilon_0 A/\delta$) as 93 nm and 234 nm for LID and HID, respectively. n(V) is the voltage-dependent ideality factor and is given by [18,26,27,29]:

$$n(V) = \frac{q}{kT}\left(\frac{d(V-IR_s)}{d\ln\left(\frac{I}{I_0}\right)}\right) \qquad \textbf{(16)}$$

In n-type semiconductors, the energy of the interface states E_{ss} with respect to the top of the valence band at the surface of the semiconductor is given by [18] [29] :

$$E_c - E_{ss} = q(\phi_e - V) \qquad \textbf{(17)}$$

where V is the voltage drop across the depletion layer and ϕ_e is the effective barrier height. The voltage dependence of ϕ_e is contained in the ideality factor n through the relation [18,26,27,29]:

$$\frac{d\phi_e}{dv} = \beta = 1 - \frac{1}{n(V)} \qquad \textbf{(18.a)}$$

where β is the voltage coefficient of ϕ_e. The effective barrier height ϕ_e is given by:

$$\phi_e = \phi_b + \beta(V) \qquad \textbf{(18.b)}$$

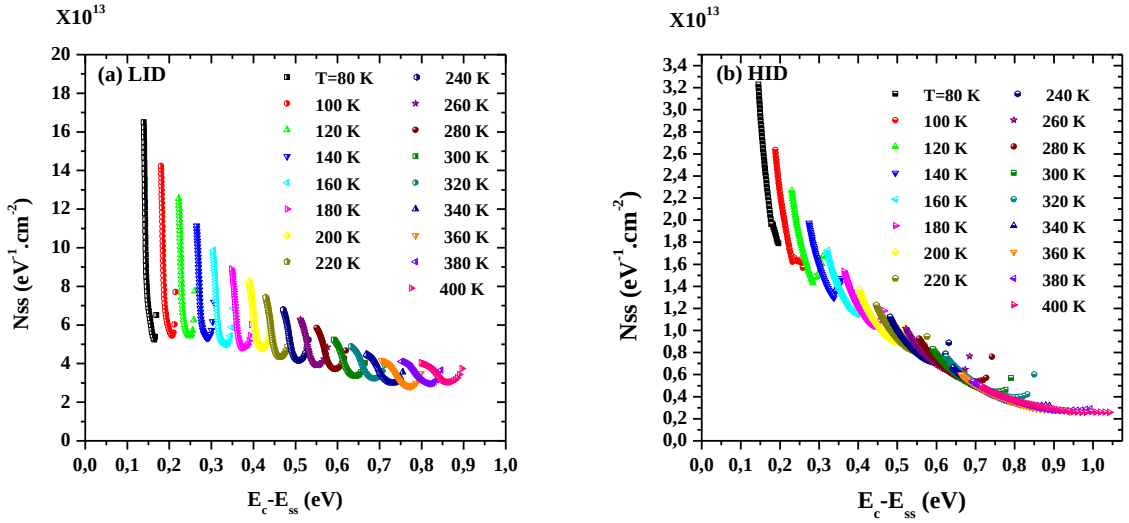

Fig.13 A plot of N_{ss} versus $E_c - E_{ss}$ for (a) **LID** and (b) **HID** Schottky diode with temperatures ranging from 80 to 400 K.

Fig.13 shows N_{ss} versus $E_c - E_{ss}$ plots at various temperatures for LID and HID samples. As can be seen from these plots, N_{ss} value decreases with increasing $E_c - E_{ss}$ as a function of temperature. Moreover, for LID structure, N_{ss} shifts from 1.66×10^{14} $eV^{-1}cm^{-2}$ (Ec-0.13) to 6.51×10^{13} $eV^{-1}cm^{-2}$ (Ec-0.16) at 80 K, whereas N_{ss} magnitude varied from 4.04×10^{13} $eV^{-1}cm^{-2}$ (Ec-0.79) to 3.74×10^{13} $eV^{-1}cm^{-2}$ (Ec-0.89) at 400 K. For HID samples these values changed from 3.22×10^{13} $eV^{-1}cm^{-2}$ (Ec-0.14) to

1.79×10^{13} $eV^{-1}cm^{-2}$ (Ec-0.19) at 80 K and from 4.98×10^{12} $eV^{-1}cm^{-2}$ (Ec-0.71) to 2.56×10^{12} $eV^{-1}cm^{-2}$ (Ec-1.04) at 400 K. Such behavior follows ideality factor variation with temperature and is due to lateral inhomogeneities of barrier height at MS interface [67]. Akkal et al. [68] explained this behavior by molecular restructuring and reordering of MS interface due to the effect of the temperature. Clearly, N_{ss} values of HID are lower than those of LID samples, indicating that n-Si surface is efficiently passivated by the 50nm In/TiO2 TF interlayer, which leads to a saturation of dangling bonds on the surface of Si. Saturation current is reduced by increasing indium doping and barrier height increases as indium doping increases. Therefore, it can be concluded that indium doping influences N_{SS} values.

Furthermore, both R_s and shunt resistance (R_{sh}) are also important parameters that govern the electrical properties and influence the performance of Schottky barrier junction. In an ideal case, R_s value is as low as possible, whereas R_{sh} is as high as possible. R_s and R_{sh} values of LID and HID structures were determined from structure resistance (R_i) versus applied bias voltage (V) plots that are shown in **Fig.14** It has been observed that, for all temperatures and at sufficiently high forward and reverse bias voltages, R_i reaches constant values, which corresponds to R_s and R_{sh} values, respectively. Thus, LID R_s values varied from 703.31 kΩ to 25.40 kΩ from 80 K to 400 K. while in HID sample R_s values varied from 9180.46 kΩ to 56.66 kΩ in the same temperature range. A low value of R_s in LID can be accomplished by either having low SBH at M/S interface or by enhanced tunneling through the BH as in heavy doped n-type Si [69], or by transportation of charge carriers through inversion layer. On the other hand, R_{sh} can originate from a leaky oxide and leakage current. R_{sh} values are found to be about 10^5 to 10^6 Ω for LID structures and about 10^8 to 10^9 Ω for HID devices.

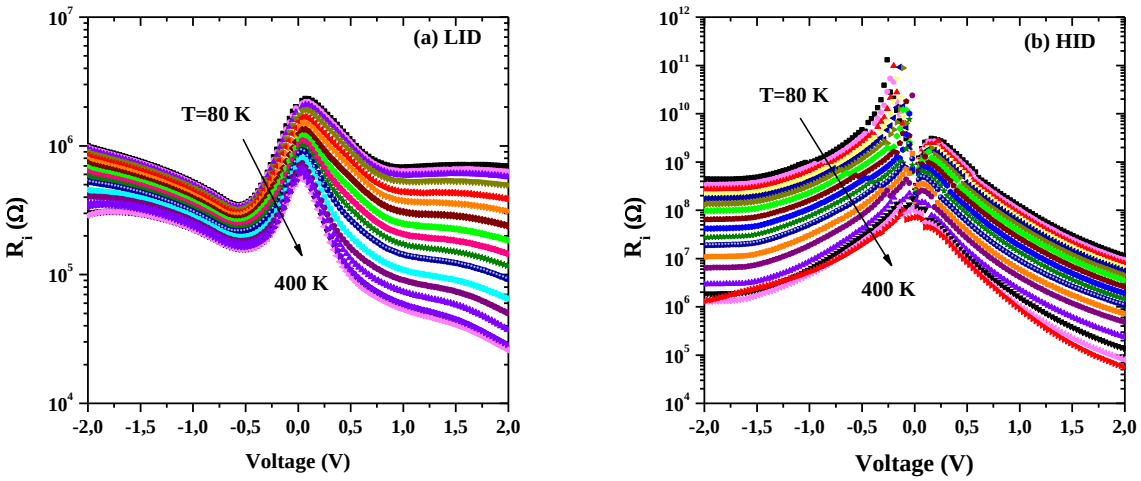

Fig. 14. Structure resistance (R_i) vs V plots of (a) LID and (b) HID SBDs.

4. Conclusions

In this investigation, Ti/Au/TiO_2:In/n-Si structures with two different indium doping were studied using XRD and I-V measurements performed in the temperature range 80K-400K. XRD diffraction patterns show only TiO_2 peaks and some peaks of In_2O_3 resulting from bounding between Oxygen and Indium atoms. Current-voltage characteristics show that HID samples have higher rectification ratio value at 2V and lower saturation current compared to LID samples. Evaluated experimental ϕ_{B0}, n, N_{ss}, Rs and Rsh assuming TE mechanism indicate strong temperature and applied bias voltage dependence. Results show that n decreases while ϕ_{B0} increases with increasing temperature. To explain such behavior, both ϕ_{B0} versus n and (n^{-1}- 1) versus q/2kT characteristics were analysed in order to provide evidence of a Gaussian distribution (GD) of BHs. Corresponding $\bar{\phi}_{B0}$ and σ values show that lower value of σ corresponds to a more homogenous barrier height. Hence, HID structures have better homogeneity and excellent electrical properties compared to LID ones. Furthermore, the modified $\ln(I_0/T^2) -$

$q^2\sigma_0^2/2(k^2T^2)$ versus q/kT plots gave consistent $\bar{\phi}_{B0}$ values, and experimental value of A* for HID are very close to the theoretical value of 112 A/(cm K)^2 for n-Si. The analysis of reverse conduction mechanism indicates that for LID structure, the leakage current flow in lower temperature region (T<220K) is due to FPE, whereas SE is dominant in higher Temperature range (T>220K). On the other hand, reverse current in HID sample in all temperature range is dominated by PFE. Obviously, HID has more defect than LID sample, that made it more sensitive to temperature in the reverse bias. Calculated interface states N_{ss} density for both sample is ~ 10^{13} $eV^{-1}cm^{-2}$ and can be considered suitable for semiconductor devices. Saturation current is reduced and barrier height increases as indium doping increases. These results influence N_{ss} values. It is found that indium doping plays a role in enhancing electrical properties of devices by improving interface barrier homogeneity.

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