Investigation of Electrically Active Defects in InGaAs Quantum Wires Intermediate-Band Solar Cells Using Deep Level Transient Spectroscopy (DLTS) Technique

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Abstract

InGaAs Quantum Wires (QWr) Intermediate-Band Solar Cells based nanostructures grown by molecular beam epitaxy (MBE) are studied. The electrical and interface properties of these solar cell devices as determined by current–voltage (I–V) and capacitance – voltage (C-V) techniques were found to change with temperature over a wide range of 20–340 K. The electron and hole traps present in these devices have been investigated using deep level transient spectroscopy (DLTS). The DLTS results showed that the traps detected in the QWr doped devices are directly or indirectly related to the insertion of the Si δ-layer used to dope the wires. In addition, in the QWr doped devices, the decrease of the solar conversion efficiencies at low temperatures and the associated decrease of the integrated external quantum efficiency EQE through InGaAs could be attributed to detected traps $E1_{QWR\_D}$, $E2_{QWR\_D}$ and $E3_{QWR\_D}$ with activation energies of 0.0037 eV, 0.0053 eV, and 0.041 eV, respectively.

Keywords: Quantum Wires Intermediate-Band Solar Cells, I–V, C-V, DLTS, defects

1. Introduction

In a photovoltaic semiconductor device, the inability to absorb light with energy less than the bandgap and the loss of photons with energies exceeding the bandgap as heat are considered to be the main fundamental effects that limit its efficiency [1]. Recently, the social interest in exploiting the solar energy using the photovoltaic effect has led to a tremendous increase in the demand of solar cells. Therefore, it is essential to develop new technologies and concepts of producing solar cells in order to increase their efficiency. In 1961, William Shockley and Hans Queisser calculated the maximum theoretical efficiency limit of p-n junction based photovoltaic solar cells to be 30% for an optimized semiconductor bandgap of 1.1 eV. This limit is known as Shockley–Queisser limit or the detailed balance limit of efficiency [2]. This formalism has been used by many authors to model solar cells [1]. Consequently, different approaches have been proposed and attempted in order to exceed the efficiency of solar cells above that limit. Tandem solar cells, multiband solar cells, hot carriers solar cells, intermediate level solar cells, impurity level solar cells, and quantum well solar cells are good examples of these approaches [3].

In 1997, Luque *et al.* [4] theoretically predicted the intermediate band solar cells (IBSC) to increase the efficiency of solar cells up to 63.1% under maximum concentrated sunlight. The main principle of these cells is to introduce one or more electronic bands (called intermediate bands or levels) inside the main bandgap of a conventional semiconductor [6, 7]. Hence, the intermediate band solar cells are expected to have an increase in photocurrent [5] without voltage degradation [6].

The fabrication and investigation of IBSC-based devices have received considerable interest worldwide because of their relevance in enhanced efficiency solar cells [7]. Specifically, the three main approaches adopted to fabricate an IBSC are: (i) use of quantum dot technology as a way of engineering the IB material; (ii) direct synthesis

of the IB material; and (iii) formation of a localized absorber layer within a highly porous large bandgap semiconductor [8]. However, amongst these three methods, the quantum dot (QD) technology is the most promising technique to realise the IB idea and to study its principle of operation [6]. In this technique, a QD structure is inserted between the bandgap of the conventional semiconductor so that charge carriers are quantum confined in three directions. Consequently, this allows QDs, which have a discrete delta-like density of states, to create the required intermediate band that has a separate quasi-Fermi level from the conduction and valence band of the semiconductor [9]. However, the incorporation of QDs leads to a reduction of the photoelectrical conversion efficiency (PCE) of QD IBSC due to the formation of strain and resulting dislocations which lead to the deterioration of the open-circuit voltage, V_{oc} [10-12]. To increase the PCE of QD IBSC, insertion of δ- dopants into the QDs was proposed [13, 14]. By using n-type δ-dopants, the electron intersubband quantum dot transitions will be increased, the recombination losses through QDs will be decreased as a result of the reduction of electron capture processes, and the deterioration of V_{oc} will be inhibited. Hence, this will enhance the infrared (IR) absorption and the photocurrent in QD IBSC [13, 14].

Kunets *et al.* [7, 15] used the above principle to fabricate an IBSC device consisting of one dimensional InGaAs quantum wires (QWRs) structure instead of using zero-dimensional quantum dots (QDs) or two-dimensional quantum wells (QWs). The QWRs were inserted into a GaAs p-i-n junction. The QWRs structure has a good configuration that allow the device to have more efficient light absorption compared to zero-dimensional systems [14]. Moreover, photocurrent can be generated in the plane of the QWRs [16, 17]. In addition, QWRs are expected to have applicable life-time of photo-generated carriers [17]. Kunets *et al.* [7, 15] also studied the effects of n-type Si delta doping on the external efficiency of this QWRs-based IB solar cell structure. They

observed that at room temperature the solar energy conversion efficiencies of the reference p-n junction and p-i-n solar cell samples were 4.1 and 4.5%, respectively, whereas samples with incorporated QWRs and delta doping showed an increase of the efficiency up to 5.1% and 5%, respectively. However, they reported that the short circuit current increases and causes a comparatively lower open circuit voltage, V_{oc} (20-50 mV) which results in a severe degradation of the performance of the solar cell.

In this work, a detailed investigation is carried out on electrically active defects in a set of (311)A GaAs solar cell structures gown by molecular beam epitaxy (MBE) [7, 15]. The devices investigated are p-n (labelled PN, first reference sample), p-i-n (labelled PIN, second reference sample), undoped p-i-n with InGaAs quantum wires (labelled QWR undoped) and Si δ- doped p-i-n with InGaAs quantum wires (labelled QWR doped). This study will help to get a better understanding of the physical phenomena that affect the efficiency of the above solar cell structures using current-voltage (I-V), capacitance-voltage (C-V), conventional DLTS and Laplace DLTS characterisation techniques.

1. Sample Details

The detail of samples growth is given somewhere else [7]. In summary, a solid source MBE 32P Riber system was used to grow the devices on semi-insulating (311)A GaAs substrates. It is well known that the high index (311)A plane is a good template for the growth of QWRs. Also, in this plane a strong built-in piezoelectric field can be generated in the presence of strain [18]. The first GaAs p-n reference device (PN device, SE159) consisted of a 400 nm GaAs buffer layer grown at a growth temperature of 580 ºC. Then the growth temperature was decreased to 540 ºC and a 1 µm thick GaAs layer doped with Si was grown with high V/III flux ratio (V/III=20). This low growth temperature and high V/III flux ratio make the GaAs layer achieve a high n-type doping efficiency on the

(311)A surface. This was followed by a 1 μm thick p-type GaAs layer doped with Si grown at a higher growth temperature (580 ºC) and low V/III flux ratio (V/III=7) to achieve p-type conductivity. The second reference device (PIN device, SE164), which was grown using the same growth conditions and consisted of the same layers as the PN device, has an additional 330 nm thick GaAs intrinsic region grown at 540 ºC and sandwiched between the p and n layers. The third device (QWR undoped device, SE160) which was grown by incorporating an intermediate band in the GaAs i-region without any intentional doping. The i-region consisted of 10 periods of 11 monolayers of $In_{0.4}Ga_{0.6}As$ QWRs separated by a 30 nm GaAs barriers. The InGaAs quantum wires were grown at 540 º C. Finally, the fourth device is similar to the third device structure, but in the middle of each 30 nm thick GaAs barrier, a Si n-type δ- doping with a sheet concentration $N_{2D}=1x10^{11}$ cm^{-2} (QWR doped, SE162) was inserted. In all the above structures, the doping concentration of n-type and p-type GaAs layers was $5x\ 10^{17}$ $cm^{-3}$and $1x\ 10^{17}$ cm^{-3}, respectively. The samples were processed in circular mesas having diameters of 900 μm, 400 μm, 549 μm and 400 μm for PN, PIN, QWR undoped and Doped QWR devices, respectively. These mesas were formed by wet chemical etching down to the n-type GaAs contact layer and 75nm AuGe/15nm Ni/200nm Au was deposited to form an O-ring shaped n-type contact. The top circular mesa p-type contact consisted of 100nm AuZn/200nm Au. The n and p contacts were annealed at 420 ºC for 2 minutes and 350 ºC for 30 seconds, respectively, using Rapid Thermal Annealing (RTA) technique. The schematic diagrams of the solar cell devices investigated in this study are shown in figure 1.

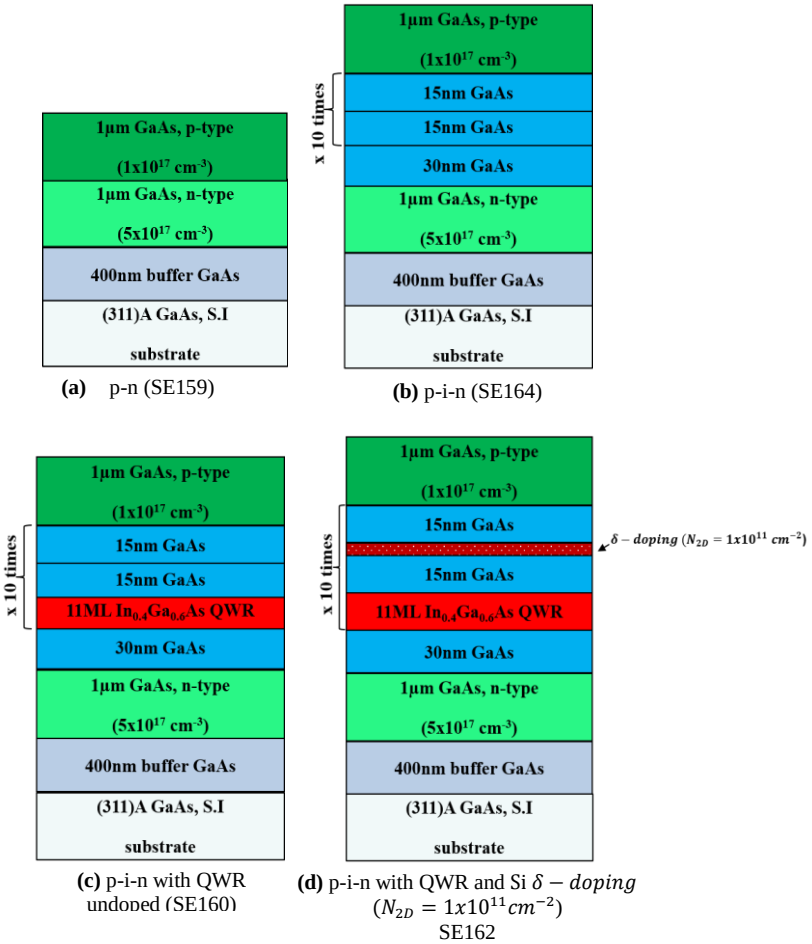

Figure 1. Schematic diagram of the solar cell structures (a) Reference p-n device (PN); (b) p-i-n device (PIN); (c) undoped p-i-n with QWR device (QWR); (d) n-type Si δ-doped p-i-n with QWR (QWR Doped).

3. RESULTS AND DISCUSSIONS

3.1 Investigation of the Current Density (J) – Voltage (V) Characteristics as Function of Temperature

Figures 2(a) and (b) show the room temperature semi-logarithmic and linear *J-V* plots of all devices, respectively. From the room temperature *J-V* characteristics it is clear that the inclusion of an i- region (PIN) and undoped InGaAs wires (QWR undoped) enhance the performance of the devices as compared to the reference PN devices. On the other hand, introducing n-type Si δ–doping (QWR doped) leads to a deterioration of the

performance of the devices. As shown in figure 2(a), at a reverse bias of -4 V, there is one order magnitude reduction in the leakage current density in the QWR undoped devices compared to the PIN devices and two orders of magnitude when compared to the reference PN devices. However, the QWR doped samples have the highest dark current density at all reverse bias voltages amongst all devices. The decrease or increase in the leakage current, which could be attributed to a decrease or increase of the number of defects and their concentrations, will be further investigated using DLTS experiments. Furthermore, the QWR undoped devices have the lowest forward current density as compared to all the other devices. However, Hao Feng Lu *et al.* [19] reported an increase of the forward current density at 310 K when incorporating $In_{0.5}Ga_{0.5}As$ quantum dots to GaAs p-i-n solar cells grown on n^+ GaAs (001) substrates by metal organic chemical vapour deposition. They related this behaviour to the creation of additional recombination paths via QD states as a result of the presence of QDs in the depletion region. Moreover, it can be seen from figure 2(b), the QWR undoped devices have a turn-on voltage (V_{on}) of 0.77 V, which is higher than the V_{on} of the PIN devices (V_{on} ~ 0.68 V). This behaviour can be explained by the creation of new defects states in the undoped i-region where the QWRs are incorporated. However, the QWR doped samples have the lowest V_{on} at around 0.51 V, while the reference PN devices have V_{on} around 0.57 V.

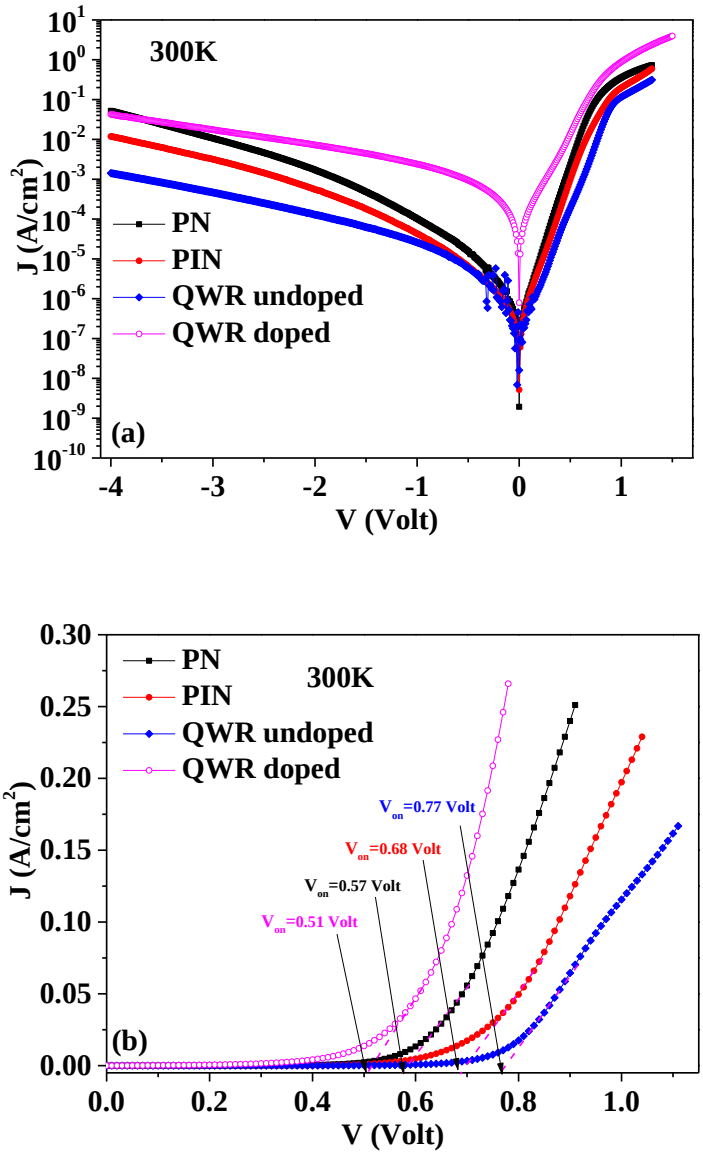

Figure 2. (a) Semi-log plots of dark J-V characteristics at T=300 K for PN, PIN, QWR undoped and QWR doped devices, (b) the corresponding linear plots.

In order to get more insight in the functioning of the p-i-n devices, the dark J-V measurements as a function of temperature (20K-340K at 20 K intervals) were carried out for all devices, however, for clarity purposes, only selected presentative curves (20–320 K at 40 K intervals) are shown in figure 3. The steady increase in the forward dark current with temperature for PIN devices (see figure 3(b)) is normally attributed to the

exponential change of the concentration of the intrinsic carrier, n_i, in the depletion region with temperature [20]. The forward-biased dark current density transport characteristics of the QWR undoped devices have more pronounced temperature dependence as compared to the reference devices, i.e., PN and PIN. While the forward dark current density for the QWR doped devices have less noticeable temperature dependence as compared to the PIN and QWR undoped devices.

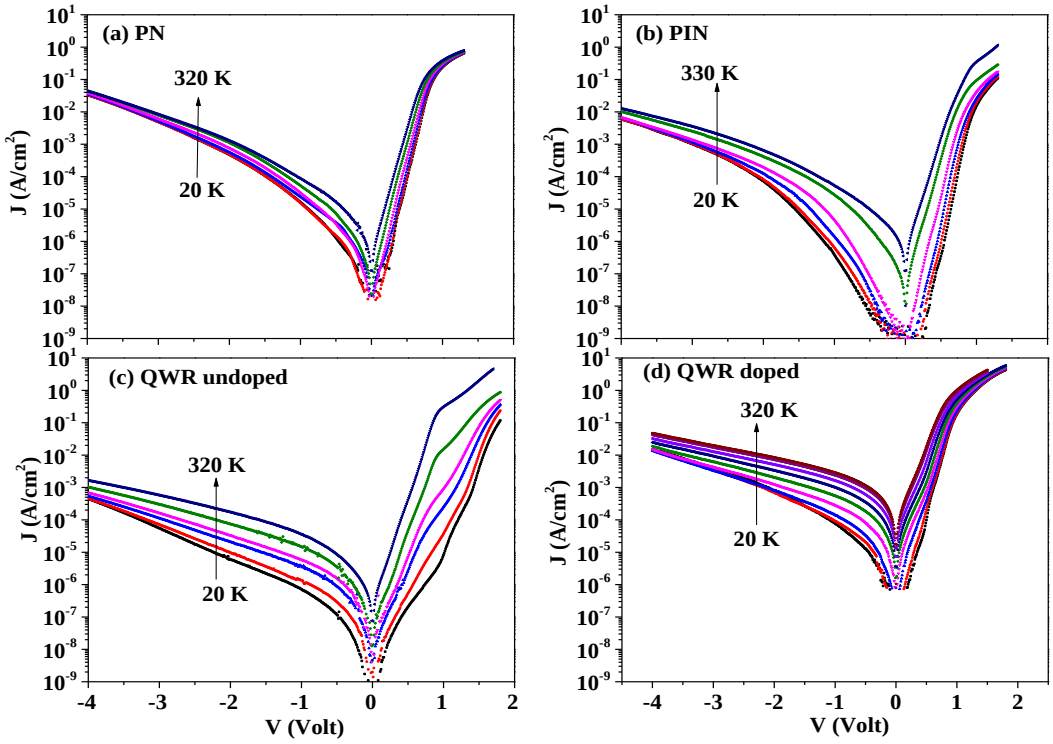

Figure 3. Semi-logarithmic plots of dark I–V characteristics (a) PN; (b) PIN; (c) QWR undoped and (d) QWR doped devices in the temperature range of 20–340 K.

Additionally, at low temperatures the QWR undoped devices exhibit an oscillation in the forward dark currents (see figure 4 for a temperature of 20K). The same behaviour was also observed at low temperatures (T<70 K) by Hao Feng Lu *et al.* [19] in QDs based solar cell devices. They suggested that these complicated dark current behaviours need to be interpreted by developing a new physical model for QDs solar cells

rather than using the conventional diode model. In contrast, the forward dark current of the QWR doped devices follows a trend similar to that of the reference PN device.

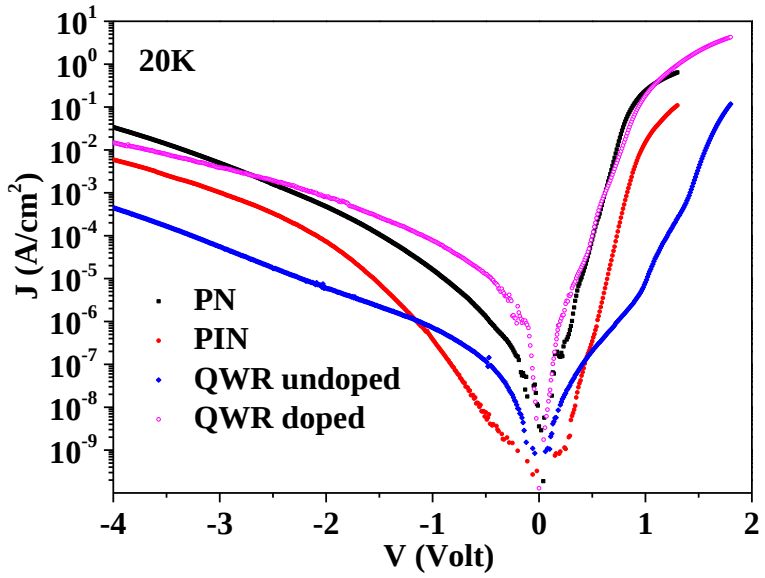

Figure 4. Semi-log plots of dark J-V characteristics at T=20 K for PN, PIN, Undoped QWR and Doped QWR devices.

Normally, the forward bias dark current is produced in a standard p-i-n solar cell via two mechanisms, namely, recombination current in the space charge region (SCR) and diffusion current through the SCR. Moreover, the change in the shape of the dark J-V curves as a function of temperature depends on the temperature dependence of the concentration and carrier capture cross-sections of different types of defects, as well as tunneling effects [21]. Besides, for the QWR devices there are additional recombination paths that are created via QWRs states and subsequently they will contribute to the dark current. The carrier capture and recombination processes under different voltage biases and temperatures are the main parameters that control the amount of additional dark current.

The J-V characteristics for all devices are analysed further to understand their properties by calculating the local ideality factor, *n(V)*, using the following approximated equation [19, 22],

$$n(V) = \frac{d(V/V_t)}{d[ln(I)]} \qquad (1)$$

where V_t is the thermal voltage.

V_t is given by $V_t = k_B T/q$. The local ideality factors for all devices are calculated at room temperature and their values change with voltage as shown in figure 5. Three different regions generally appear around 0.2V, 0.4V and 0.5V indicating the currents transition between different dominating mechanisms [19, 22] in the devices. The n(V) behaviour over certain voltage ranges is similar for all devices. However, the QWR devices have unique trends at other voltage ranges. This suggests that some mechanisms are presumably enhanced or suppressed after adding QWRs, and some of the mechanisms are possibly unique to the QWR devices. It is worth pointing out that these results are in good agreement with the previous study carried out by Kunets *et al.* [7] for the same devices.

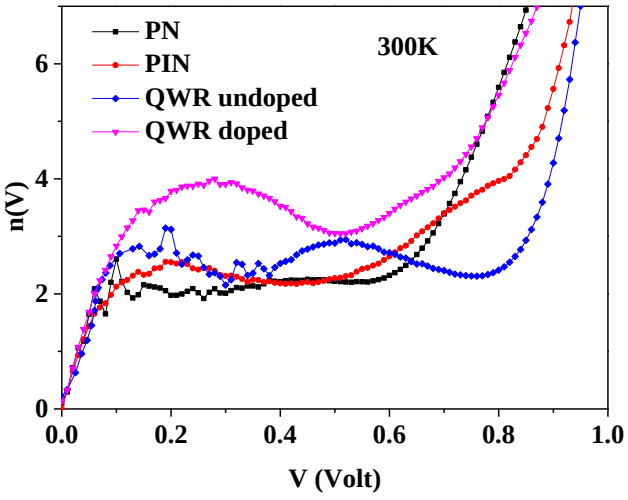

Figure 5. Voltage dependence of the local ideality factor for PN, PIN, QWR undoped and QWR doped devices at 300 K.

To gain better understanding about the different conduction mechanisms occurring in the investigated devices, the local ideality factor versus voltage at different temperatures were determined for all devices as illustrated in figure S1 (see

supplementary information). As can be seen, for each device there are two noticeable behaviours observed at low voltage and high voltage regions. In particular, at low voltages all devices exhibit a clear peak. However, for the QWRs devices, this peak becomes more significant ($n>>1$) as the temperature decreases and it shifts to higher voltages. Conversely, for PN and PIN devices this low voltage peak is almost temperature independent and has a very small amplitude as compared to the QWRs devices where n is much greater than unity. It is well-known that tunnelling or generation/ recombination processes can account for large ideality factors ($n>1$) [23]. These processes could also explain the large ideality factors observed in samples that incorporate QWRs in the intrinsic region and which create an additional current component that contributes to the total current of the devices. Thus the trend of the ideality factor at low voltages provides evidence of enhanced recombination via QWRs in these devices. A similar behaviour has been reported in QDs based solar cell devices [14]. Furthermore, for QWR doped samples, as a result of n-type Si δ–doping, the electrons will easily occupy the QWRs, and this leads to a strong local potential barrier around the QWRs. Thus, the electron mobility in the conduction band can be reduced as a result of variations of the local potential around the QWRs [11]. As a result, the J-V characteristics of these devices are worsened as evidenced by their larger ideality factors. It is worth pointing out that, a similar behaviour of the local ideality factor at low voltage biases was observed by Gu Tingyi *et al.* [22] in InAs/InGaAs quantum dots-in-a-well (DWELL) solar cells and by H. Kim *et al.* [24] in InAs quantum dots solar cells. As can be seen in figure S1 (see supplementary information), at higher voltages the local ideality factor increases approximatively linearly with bias for all devices. These large values normally reflect that the series resistance effect becomes predominant [19, 22]. According to the obtained data, the local ideality factor of the PIN and QWR undoped devices is temperature dependent

but the rate of change with the temperature is faster for the undoped QWR devices. However, for the PN and Doped QWR devices, the local ideality factor is practically temperature independent.

Figure 6 displays the first derivative of the J-V characteristics of all devices at temperatures ≥ 200 K. For clarity purposes, the first derivative of the J-V characteristics of all devices are replotted at 260 K as shown in the inset of figure 6(d). A negative differential resistance (NDR) region is only noticeable in PIN and QWR undoped devices at temperatures above 200 K and under higher forward bias regime. The appearance of the NDR is presumably due to the resonant tunnelling of electrons (or holes) through the quasi-bound levels in the QWR region [24, 25]. Clearly, figure 6(c) shows the increase of the peak-to-valley ratio as the temperature increases. While when the temperature was reduced no NDR region was observed. Houng *et al.* [26] attributed the NDR behaviour at room temperature to the resonant interband tunnelling (RIT) effect. The disappearance of the NDR at low temperatures is suggested to be due to the effect of band-gap widening at low temperatures [26]. Thus in PIN and QWR undoped devices, the carriers are thermally activated to the allowed bands from which they can tunnel. Therefore, at low temperatures a few carriers are available in the band hindering the observation of resonant tunnelling, as shown in figure 6(b) and (c). Additionally, the thickness of the delta-doped layer is an important parameter of device design, having a direct influence on whether RIT occurs or not [26]. Indeed, as can be seen in figure 6(d), when the delta-doped layer is incorporated in the QWR devices, the NDR behaviour disappears.

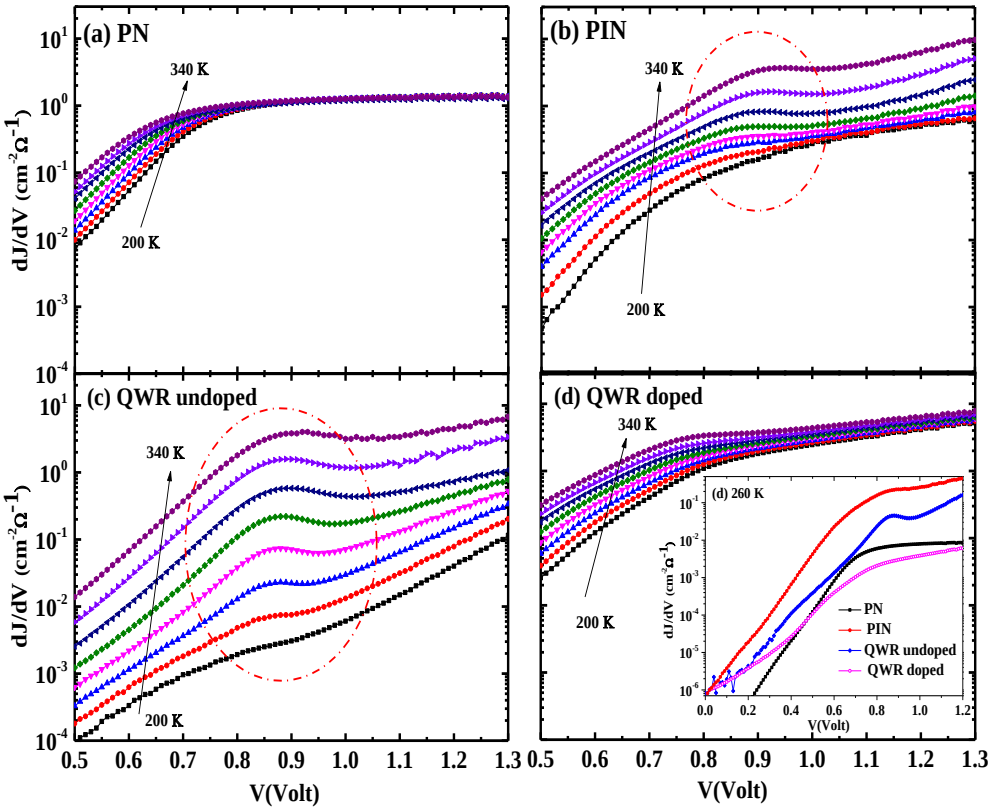

Figure 6. Semi-log plots of dJ/dV versus V for (a) PN, (b) PIN, (c) QWR and (d) Doped QWR devices at temperatures ≥ 200 K. The inset in (d) shows Semi-log plots of dJ/dV versus V of all devices at 260 K.

3.2 C-V Characteristics

In order to determine the apparent free carrier concentrations and to have specific understanding of the junction structure of these devices, capacitance-voltage (C-V) measurements have been performed at a frequency of 1MHz.

Figure 7 depicts the dependence of the capacitance/area (C/A) as a function of bias voltage recorded at temperatures 300 K and 20 K for all devices. In the p-n devices investigated in this work a maximum room temperature capacitance, C_{max}, is observed in forward biases as shown in figure 7(a). C_{max} increases in the following sequence: C_{max1} (PN) < C_{max2} (PIN) < C_{max3} (QWR undoped) < C_{max4} (QWR doped). The same behaviours were also observed by Gunawan *at al.* [27] in p-n wire-array solar cells with different microsphere diameters fabricated by lithography technique. They observed an increase of C_{max} as the wire diameter increased. They suggested that this increase of C_{max} is due to the extra cylindrical sheath surface of the wires. It is worth pointing out that in the devices investigated by Gunawan *at al.* [27] the wires were vertical, while in this study the devices incorporated lateral wires (QWRs).

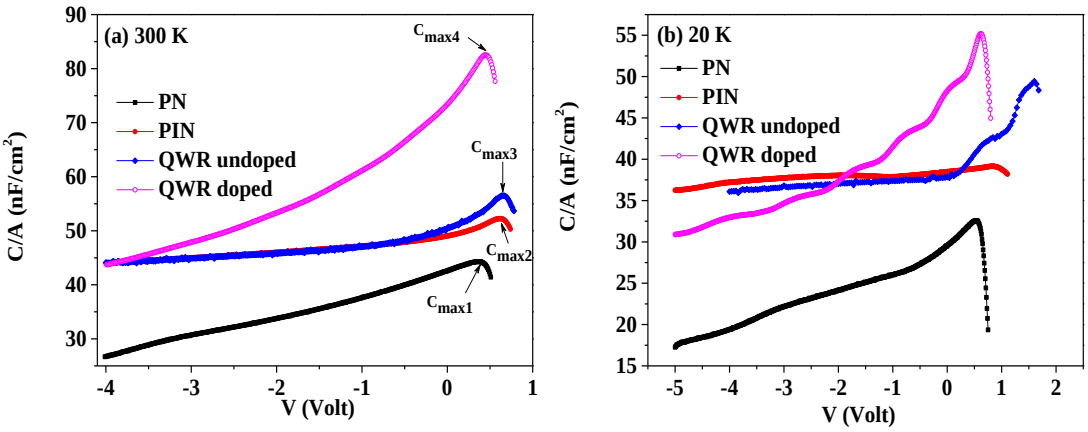

Figure 7. Variation of capacitance/area with voltage for PN, PIN, Undoped QWR and Doped QWR devices at (a) 300 K and (b) 20K.

As the structure of the devices investigated are p-i-n junctions the capacitance is expressed by the following equation:

$$\frac{1}{C} = \frac{d}{\varepsilon_s \varepsilon_0 A} + \frac{x_n}{\varepsilon_s \varepsilon_0 A} + \frac{x_p}{\varepsilon_s \varepsilon_0 A} \qquad (2)$$

where d represents the thickness of the intrinsic region (cm), $x_{n,p}$ the depletion regions in both n and p sides (cm), respectively, and ε_s is the permittivity ($F \cdot cm^{-1}$) of GaAs (12.9 ε_0

[23]) . As the doping levels of the n and p layers are fairly high, it is very likely that the intrinsic region dominates the overall capacitance because d is considered to be >> $x_{n,p}$. Consequently, the capacitance should vary only slightly with bias in reverse conditions. As shown in figure 7, the capacitance change as function of reverse bias in PIN and QWR Undoped devices is very slow as expected by equation 1. However, for the QWR Doped samples this behaviour deviates considerably from the one described by equation 1 and it follows the same trend as the PN devices. The reason is very likely due to the effect of introducing n-type Si δ–doping which makes the QWR doped junction behaving as a PN junction.

Figure 7(b) shows that the capacitance/area (C/A) at T = 20 K decreases with increasing reverse bias, a behaviour which is frequently observed in this kind of device due to the increase of the depletion layer width. However, the most interesting features observed in the C-V characteristics are the plateaux or multiple steps detected in the QWR samples. For the QWR undoped devices the plateau appears only in the forward biased (0.24 – 1.0 V), while the steps are present in the QWR doped devices over the whole bias range. The distinct behaviours of the capacitance in QWR undoped devices can be related to a two dimensional electron gas (2DEG) formation as a result of electron localization in InGaAs wetting layer (WL). Chiquito *et al.* [28] observed a plateau like dependence in their C-V measurements at the bias range 0.5 to 1.5 V in InAs/GaAs self-assembled quantum dots system. They related this behaviour to the formation of 2DEG at the $(GaAs)_4/(AlAs)_{11}$/GaAs top interface rather than at the WL because their PL and Raman scattering measurements proved that there is no contribution of the WL. In fact, the capacitance increase and the plateau features that are observed in the capacitance measurements for a bias range of 0.24 -1.0 V as shown in figure 7(b) for QWR undoped samples could be attributed to the confinement of electrons at the InGaAs WL. Recent

photoluminescence (PL) measurements performed by Kunets *et al.* [7] provided a strong evidence of the contribution of the WL in QWR devices. Therefore, one could conclude that a 2DEG is created in the InGaAs WL when a forward bias is applied in the QWR undoped devices investigated here and would account for the plateaux observed in the C-V characteristics. When a sufficiently high forward voltage is applied the capacitance decreases, as shown in figure 7(b) because the 2DEG layer is fully depleted of electrons. Babinski *et al.* [29] reported a similar behaviour at V= 0.7 V in $In_{0.6}Ga_{0.4}As$/GaAs QDs grown by metalorganic vapour phase epitaxy. They explained the plateaux formation in the forward bias voltage by the QDs excited states filled by electrons or a DEG formed in InGaAs WL. It is, however, worthwhile mentioning that Kim et *al.* [30] observed a hump shape at a forward voltage near 0.4 V in InAs/GaAs QDs Schottky diodes grown by MBE. They related this hump to the carrier accumulation in the QDs layer.

In order to investigate further the behaviour of C-V characteristics, C-V measurements were performed at low frequencies for both doped and undoped QWR devices. The apparent carrier concentration profile as function of depth is also calculated by using the following relations [31]:

$$N_{CV}(W) = \frac{2}{A^2 q \varepsilon_s \varepsilon_0}\left[\frac{d}{dV}\left(\frac{1}{C^2}\right)\right]^{-1} \text{ and } W = A\frac{\varepsilon_s \varepsilon_0}{C} \qquad (3)$$

where W is the length of the depletion region and $N_{CV}(W)$ is the apparent carrier concentration for semiconductors with quantum confinement [32]. Figure S2 (see supplementary information) shows the C-V and N_{CV} of doped and undoped QWR devices at 100 K at low and high frequency. It can be seen from the C-V plots that there is no significant capacitance difference between the C-V measurements at low and high frequency. Similarly, the N_{CV} plot at both frequencies in undoped and doped samples is unchanged. The C-V and N_{CV} have no frequency dependence, which confirms that the emission of electrons from quantum wires is very fast.

In order to determine the distance between the steps observed in figure 7(b) for the QWR devices the derivative of capacitance (dC/dV) were calculated, as shown in figure 8. One could approximate the number of charge carriers accumulated in the QWR doped layers by using $Q=C_p \Delta V$, where C_p represents the capacitance at the plateau and ΔV represent the width of the plateau region [33]. The accumulation charge in the first, second, third, fourth and fifth QWRs layers of the QWR doped samples are calculated to be $Q_1= 4.02 \times 10^{-11}$ C, $Q_2= 4.72 \times 10^{-11}$ C, $Q_3= 4.73 \times 10^{-11}$ C, $Q_4= 4.94 \times 10^{-11}$ C and $Q_5= 5.43 \times 10^{-11}$ C, respectively. These values are associated with the fact that as the step is wider, the carrier concentration confined in the QWRs layer is higher [34, 35]. For the undoped QWR devices there is only one accumulation layer with a charge $Q= 8.56 \times 10^{-11}$ C. As shown in figure 8, for the QWR doped samples the width of the steps (ΔV) increases as the reverse bias increases. This increase could be attributed to the increase of the electrical field in the space charge region [36, 37]. Because of this, for small reverse biases the first QWR layer is depleted of electrons while all the other QWRs layers in the device remain electrically neutral. When the reverse voltage is increased further the conduction electrons are depleted to the second QWR layer, and therefore the boundary of the space charge region moves to the second QWR. This process will carry on until all the QWR are depleted. Thus, the number of steps in the capacitance curve is related to the number of depleted QWR layers in the device.

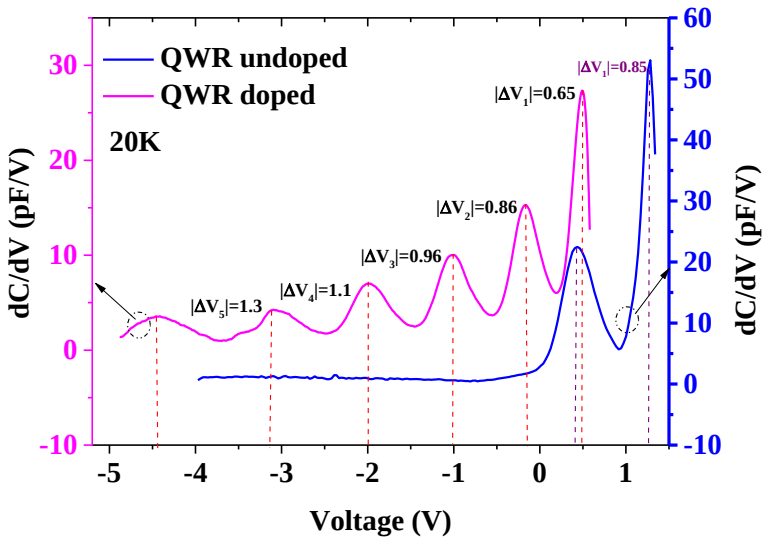

Figure 8. dC/dV characteristics of the undoped and doped QWR devices measured at a frequency of 1MHz and temperature of 20K.

The free carrier concentration profile shown in figure S2 (see supplementary information) reflects clearly the charge carriers accumulated in the QWR layers. The estimated free carrier sheet densities [29, 37] for the first, second, third, fourth and fifth QWRs layers in Doped QWR devices are 7.96 x 10^{11} cm^{-2}, 1.00 x 10^{11} cm^{-2}, 1.00 x 10^{11} cm^{-2}, 8.66x 10^{10} cm^{-2}, 1.13 x 10^{11} cm^{-2}, respectively. While the free carrier sheet density for the QWRs layer in QWR undoped devices is 9.29 x 10^{10} cm^{-2}. Additionally, the distances between the N_{CV} peaks shown in figure S2 (see supplementary information) for QWRs layers was approximately 28 nm, which is nearly consistent with the designed QWR doped device structure (30 nm).

3.3 DLTS and Laplace DLTS Characteristics

In order to explore the effect of the electrically active defects on the solar cell efficiency in GaAs (311)A solar cell devices, DLTS experiments [38] were carried out at basing conditions of a reverse bias V_R = -0.25 V with filling pulse height V_P= 0 V, and a filling

pulse duration, t_p =1 msec. The samples temperature was scanned from 10 K up to 450 K. Figure 9 shows normalized DLTS spectra for all devices. DLTS measurements reveal a distinct broad minority electron trap peak (negative peak) over a wide range of temperatures in all devices which can be resolved by Laplace DLTS measurements [39]. In PN devices, in addition to the broad electron peak, a hole trap is also detected (positive peak).

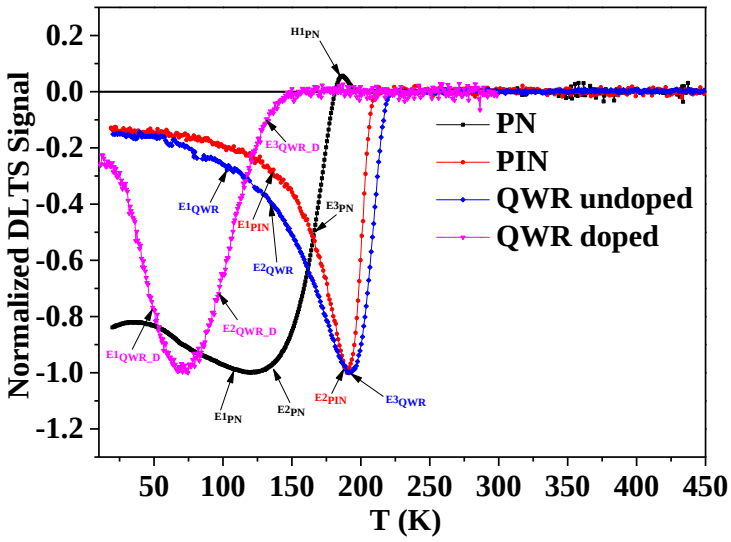

Figure 9. Normalized DLTS spectra of PN, PIN, QWR undoped and QWR doped devices obtained with the following conditions: reverse bias V_R= -0.25 V, filling pulse V_p = 0 V and pulse duration t_p= 1 msec at rate window of 500 s^{-1}.

Laplace DLTS was used in order to resolve the broad electron trap peak detected in all samples. Figure 10 shows that the broad DLTS peak observed for QWR doped devices over the temperature range ~14-144 K (see figure 9) splits in three clear peaks as detected by the high resolution Laplace DLTS at T = 53 K. In summary, the Laplace DLTS revealed the presence of the following traps: (i) PN: three electron traps ($E1_{PN}$ to $E3_{PN}$) and one hole trap ($H1_{PN}$); (ii) PIN: two electron traps ($E1_{PIN}$ & $E2_{PIN}$); (iii) QWR undoped:

three electron traps ($E1_{QWR}$ to $E3_{QWR}$); (iv) QWR doped: three electron traps ($E1_{QWR\_D}$ to $E3_{QWR\_D}$).

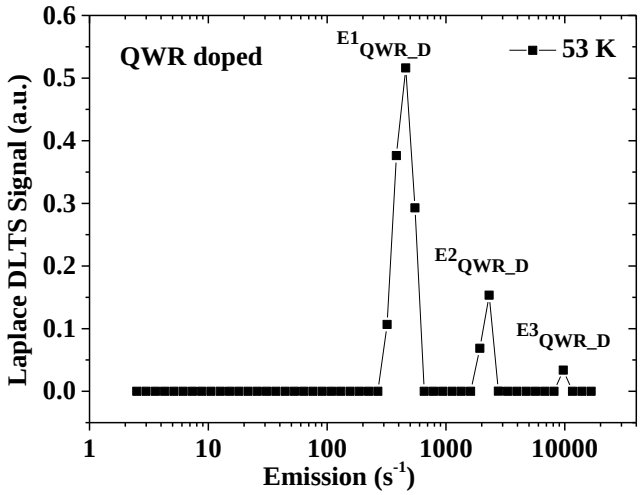

Figure 10. Laplace DLTS of QWR doped devices at 53 K under biasing condition V_R=-0.25V, V_p= 0 V and t_p= 1 msec.

The Arrhenius plots of the emission rates as a function of temperature (ln (e_n /T^2) versus (1000/T)) for each defect level detected by Laplace DLTS are shown in figure S3 (see supplementary information). The traps activation energies and capture cross-sections are calculated from the slope and the intercept of the above plots, respectively. These are summarized in table 1 with the concentrations of each trap. It is worth to mention that the traps concentrations are calculated from the peaks of Laplace DLTS signal and C-V measurements.

Table 1: Summary of traps activation energies, capture cross-sections and concentrations for PN, PIN, QWR undoped and QWR doped devices.

Device	Trap Label	Activation energy (eV)	Apparent capture cross-section (cm^2)	Trap concentration (cm^{-3})
PN	$H1_{PN}$	(0.157±0.004)	$1.96x10^{-18}$	$6.16x10^{15}$
	$E1_{PN}$	(0.018±0.002)	$1.01x10^{-21}$	$6.55x10^{14}$
	$E2_{PN}$	(0.039±0.002)	$5.68x10^{-21}$	$2.20x10^{13}$
	$E3_{PN}$	(0.095±0.003)	$3.54x10^{-19}$	$7.04x10^{15}$
PIN	$E1_{PIN}$	(0.070±0.004)	$2.81x10^{-20}$	$1.86x10^{14}$
	$E2_{PIN}$	(0.14±0.01)	$3.58x10^{-18}$	$2.93x10^{15}$
QWR undoped	$E1_{QWR}$	(0.010±0.001)	$1.93x10^{-22}$	$2.09x10^{15}$
	$E2_{QWR}$	(0.074±0.003)	$8.64x10^{-20}$	$4.03x10^{13}$
	$E3_{QWR}$	(0.145±0.008)	$1.63x10^{-17}$	$1.62x10^{15}$
QWR doped	$E1_{QWR\_D}$	(0.0037±0.0009)	$2.06x10^{-21}$	$3.93x10^{15}$
	$E2_{QWR\_D}$	(0.0053±0.0001)	$2.22x10^{-21}$	$5.99x10^{14}$
	$E3_{QWR\_D}$	(0.041±0.004)	$5.38x10^{-20}$	$6.96x10^{13}$

As seen in table 1 only one hole trap, $H1_{PN}$, is detected in PN devices. It has an energy close to the one measured from Laplace DLTS by Boumaraf *et al.* [40] in p-type Si-doped GaAs Schottky diode. Although the origin of this defect is not yet clear, they suggested that it could be related to complexes involving silicon atoms, background impurities, and defects originating from the growth conditions used. $E1_{PN}$ has an activation energy comparable to the trap reported in GaAs [41]. However, the origin of $E1_{PN}$ is still not known.

It can be seen from table 1 that the shallow trap, $E2_{PN}$ in PN reference device has approximately the same activation energy as trap, $E3_{QWR\_D}$ detected in the QWR doped devices, and could possibly originate from the same defect. This trap might be assigned to an arsenic vacancy v_{As} introduced in electron-irradiated GaAs (labelled E_1) and whose activation energy was found to be 32–45 meV [42-45] below the conduction band. It is worth pointing out that this is the only trap which is common in the QWR doped and PN devices. In the earlier analysis of the C-V characteristics it was concluded that the QWR doped junction acts as PN junction as a result of introducing n-type Si δ–doping. This common shallow trap might justify this assumption in C-V. However, the capture cross-section and concentration of this trap in QWR doped devices are higher than those of the PN devices. According to the previous study [7] for this QWR doped device, the fitting of PL spectra at a high excitation intensity of 3000 W/cm^2 shows an energy difference between the wires and the 2D wetting layer transition to be 46 meV. This energy difference is nearly equal to the trap $E3_{QWR\_D}$ activation energy. Thus another possibility that $E3_{QWR\_D}$ could be related to the inter-band energy transition between the InGaAs wire and the 2 D WL where tunnelling to the conduction band could occur. $E3_{PN}$ trap with an activation energy of ~ 0.095 eV can be related to the well-known electron trap in GaAs

grown by MBE, M0 (E_c-0.10 eV), that originated from chemical impurities during growth[46].

It can be seen from table 1 that the electron traps $E1_{PIN}$ and $E2_{PIN}$ in the PIN devices have similar activation energies as the electron traps $E2_{QWR}$ and $E3_{QWR}$ in the QWR undoped devices, respectively. These traps in both PIN and QWR undoped devices may originate from the intrinsic GaAs region since these were not observed in PN devices. One can therefore infer that by introducing n-type Si δ–doping in QWR doped samples, $E2_{QWR}$ and $E3_{QWR}$ traps were annihilated. Additionally, it is found that the trap densities and apparent capture cross-sections of $E1_{PIN}$ and $E2_{PIN}$ are affected by the introduction of the InGaAs QWRs intermediate band. From DLTS measurements Lee *et al.* [47] detected an electron trap with activation energy of 0.14 eV in InAs/GaAs δ–doped QD solar cell structures grown by MBE and they identified this trap to M1 defect which is commonly observed in GaAs layers grown by MBE [46]. Furthermore, $E2_{PIN}$ and $E3_{QWR}$ have comparable activation energies as trap F (0.14 eV) reported by Asano *et al.* [48] in GaAs (001) /InAs/InGaAs/GaAs self-assembled QD structures. In their study, they inferred that the increase of the density of this trap and others traps around the QDs is due to the growth conditions of InGaAs/GaAs QD structures. In particular, the density of these defects were reduced by a factor of 20 when they used migration enhanced epitaxy (MEE) to grow the GaAs capping layer at 400 or 500 °C as compared to using MBE for a growth temperature of 500 °C. Also Fang *et al.* [35] detected the M1 defect in $In_{0.5}Ga_{0.5}As$/GaAs QDs structures grown by MBE and they attributed this defect to point defects instead of defect-impurity complexes. Moreover, Kunets *et al.* [49] observed the M1 trap in $In_{0.35}Ga_{0.65}As$/GaAs QDs structures grown by MBE using noise spectroscopy measurements, and they related the increase of its density in the vicinity of $In_{0.35}Ga_{0.65}As$

QDs to strain. Thus there is a consensus that $E2_{PIN}$ and $E3_{QWR}$ are related to M1 defect which could be assigned to defect-impurity complexes or/and point defects [35, 46, 49, 50]. The shallow trap $E1_{QWR}$ with energy of ~10 meV is only observed in QWR undoped devices. Thus, in this work it is believed that the $E1_{QWR}$ level is created due to the incorporation of InGaAs QWRs. From a rectangular potential well calculation using the Nextnano software, Vakulenko *et al.* [51] found that the quantum energy of the ground state in InGaAs/GaAs QD structures is approximately about 10 meV. This finding provides further evidence that $E1_{QWR}$ trap could be related to the incorporation of the QWRs.

For QWR doped devices the traps $E1_{QWR\_D}$ to $E3_{QWR\_D}$ are directly or indirectly related to the introduction of the n-type Si δ–doping since these traps were not observed in PIN and QWR undoped devices. The shallow trap $E2_{QWR\_D}$ has an activation energy of ~5.3 meV which is comparable to the ionization energy of silicon donors in GaAs (5.8 meV) [52]. Furthermore, Teh *et al.* [53] found a similar trap level with concentration ~ 10^{15} cm^{-3} using the temperature dependence of the double exponential decay measurements. They assigned this trap to silicon substituting for a gallium centre, Si_{Ga},with binding energy of 5.85 meV. It is relevant to note that some of the traps detected in the devices investigated in this work are reported here for the first time. Their origins are not clear and further investigations are needed.

These DLTS measurements for PIN, QWR undoped and QWR doped devices are correlated with the earlier solar conversion efficiency measurements done by Kunets *et al.* [15] at different temperatures (83 K-300 K). In their measurements, they found that the efficiency increases as the temperature decreases in all devices until the temperature reached down to between 180 and 160 K, then the trend changed. In particular, in the PIN

devices, the efficiency showed very small increments as the temperature decreased. While for the QWR undoped samples the efficiency increased considerably as the temperature decreased down ~120 K, then the efficiency decreased for lower temperatures. For the QWR doped devices, the efficiency tended to decrease as the temperature decreased. The dramatic changes in the efficiency in the temperature range below 160-180 K can be correlated to the peaks observed in the DLTS spectra over the same temperature ranges (see figure 9). Moreover, the above analysis of the DLTS and Laplace DLTS spectra demonstrates as well a reasonable correlation with the external quantum efficiency (EQE) study done by Kunets *et al.* [15] on these devices at different temperatures. In their work, they correlated the lower solar conversion efficiency values in the QWR undoped devices compared to the PIN and QWR doped samples in the temperature range 160-240 K to their lower integrated EQE over the same temperature. This behaviour has been explained by measuring the GaAs EQE. The integrated GaAs EQE measurements showed an obvious U-shape trend as a function of temperature for QWR undoped devices, however, for the reference PIN devices the GaAs EQE characteristics were almost temperature independent. In this study [15], this behaviour can be associated to the electrically active traps $E2_{QWR}$ and $E3_{QWR}$ since they were detected within the temperature ranges where the solar conversion efficiencies were low. Although the PIN and QWR undoped devices have similar defects in terms of activation energy, the capture cross-sections of the QWR undoped devices are higher. Therefore, these higher cross-sections of these defects could have more influence on the solar conversion efficiencies. However, a rapid increase of solar conversion efficiency and associated increase of the integrated EQE signal at low temperatures (T<~120K) observed in InGaAs QWR undoped devices could be attributed to the incorporation of QWRs which introduce an intermediate energy band for enhanced energy harvesting and therefore enhanced efficiency. This level/band, $E1_{QWR}$, was indeed

detected by DLTS in the InGaAs QWR undoped samples. In the QWR doped devices, however, it was reported that the solar conversion efficiencies and integrated InGaAs EQE decrease at low temperatures (T<~120K). This behaviour could be attributed to the three traps $E1_{QWR\_D}$ to $E3_{QWR\_D}$ detected by DLTS. $E2_{QWR\_D}$ has an energy comparable to the ionisation energy of Si as discussed above. $E1_{QWR\_D}$ and $E3_{QWR\_D}$, which were not observed in the PIN or QWR undoped samples, could be also assigned to complexes involving Si atoms via delta-doping.

4. Conclusion

I-V, C-V, DLTS and Laplace DLTS techniques were used to investigate the existence of defects in GaAs p-i-n solar cells incorporating undoped and doped intermediate band QWRs in the intrinsic region of the device junction.

Analysis of the J-V dependence showed that the QWRs-containing devices exhibited a clear peak of the local ideality factor at small forward biases at all temperature conditions, which might be caused by the charges captured at the QD-induced defect states. While under large forward biases, the temperature dependence of the ideality factor for all devices was well related to the effect of the series resistance. In addition, the C-V measurements at T=20 K revealed plateaux in QWR undoped devices which were related to 2DEG or/and the carrier accumulation in the QD layer, and for the QWR doped devices the i^{th} steps observed in the C-V plots were related to the depletion of the i^{th} QWR in the devices. The efficiency and EQE characteristics obtained by Kunets *et al.* [15] at different temperatures correlated with the appearance of trap peaks observed in the DLTS and Laplace DLTS spectra at almost the same temperature ranges. An IB level/band with energy of ~10meV detected by Laplace DLTS in QWR undoped devices was related to the ground state energy of InGaAs QWRs. From these results, it is concluded that the observed defects play an important role in the efficiency of QWRs IBSC. They also

provide an essential understanding of the properties of these solar cell structures in order to enhance further their efficiencies.

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REFRENCES

[1] Conibeer G 2007 Third-generation photovoltaics *Materials Today* **10** 42-50

[2] Shockley W and Queisser H J 1961 Detailed balance limit of efficiency of p-n junction solar cells *Journal of Applied Physics* **32** 510-9

[3] Nozik A 2002 Quantum dot solar cells *Physica E: Low-dimensional Systems and Nanostructures* **14** 115-20

[4] Luque A and Martí A 1997 Increasing the efficiency of ideal solar cells by photon induced transitions at intermediate levels *Physical Review Letters* **78** 5014

[5] Luque A, Martí A and Stanley C 2012 Understanding intermediate-band solar cells *Nature Photonics* **6** 146-52

[6] Marti A, Lopez N, Antolin E, Canovas E, Luque A, Stanley C, Farmer C and Diaz P 2007 Emitter degradation in quantum dot intermediate band solar cells *Applied Physics Letters* **90** 233510--3

[7] Kunets V, Furrow C, Morgan T A, Hirono Y, Ware M, Dorogan V, Mazur Y I, Kunets V and Salamo G 2012 InGaAs quantum wire intermediate band solar cell *Applied Physics Letters* **101** 041106--5

[8] Luque A, Martí A, Wahnón P, Cuadra L, Tablero C, Stanley C, McKee A, Zhou D, Konenkamp R and Bayón R 2002 Progress towards the practical implementation of the intermediate band solar cell: IEEE) p 1190-3

[9] Linares P, Marti A, Antolin E and Luque A 2011 III-V compound semiconductor screening for implementing quantum dot intermediate band solar cells *Journal of Applied Physics* **109** 014313

[10] Luque A and Martí A 2010 The intermediate band solar cell: progress toward the realization of an attractive concept *Advanced Materials* **22** 160-74

[11] Shang X, He J, Wang H, Li M, Zhu Y, Niu Z and Fu Y 2011 Effect of built-in electric field in photovoltaic InAs quantum dot embedded GaAs solar cell *Applied Physics A* **103** 335-41

[12] Marti A, Lopez N, Antolin E, Canovas E, Luque A, Stanley C, Farmer C and Diaz P 2007 Emitter degradation in quantum dot intermediate band solar cells *Applied Physics Letters* **90** 233510

[13] Sablon K A, Little J W, Mitin V, Sergeev A, Vagidov N and Reinhardt K 2011 Strong enhancement of solar cell efficiency due to quantum dots with built-in charge *Nano letters* **11** 2311-7

[14] Sablon K A, Little J W, Sergeev A, Vagidov N and Mitin V 2012 Solar cell with built-in charge: Experimental studies of diode model parameters *Journal of Vacuum Science & Technology A* **30** 04D104

[15] Kunets V P, Furrow C, Ware M, de Souza L, Benamara M, Mortazavi M and Salamo G 2014 Band filling effects on temperature performance of intermediate band quantum wire solar cells *Journal of Applied Physics* **116** 083102

[16] Kunets V P, Teodoro M, Dorogan V, Lytvyn P, Tarasov G, Sleezer R, Ware M, Mazur Y I, Krasinski J and Salamo G 2010 Interface roughness scattering in laterally coupled InGaAs quantum wires *Applied Physics Letters* **97** 262103

[17] Kunets V P, Prosandeev S, Mazur Y I, Ware M, Teodoro M, Dorogan V, Lytvyn P and Salamo G 2011 Isotropic Hall effect and “freeze-in” of carriers in the InGaAs self-assembled quantum wires *Journal of Applied Physics* **110** 083714

[18] Vaccaro P, Hosoda M, Fujita K and Watanabe T 1996 Growth and Characterization of Vertical-Cavity Surface-Emitting Lasers Grown on (311) A-Oriented GaAs Substrates by Molecular Beam Epitaxy *Jpn. J. Appl. Phys. Part* **1** 1292

[19] Lu H F, Fu L, Jolley G, Tan H H, Tatavarti S R and Jagadish C 2011 Temperature dependence of dark current properties of InGaAs/GaAs quantum dot solar cells *Applied Physics Letters* **98** 183509

[20] Radziemska E 2006 Effect of temperature on dark current characteristics of silicon solar cells and diodes *International Journal of Energy Research* **30** 127-34

[21] Kachare R, Anspaugh B and Garlick G 1988 Tunneling effects in the current-voltage characteristics of high-efficiency GaAs solar cells *Solid-state electronics* **31** 159-66

[22] Gu T, El-Emawy M A, Yang K, Stintz A and Lester L F 2009 Resistance to edge recombination in GaAs-based dots-in-a-well solar cells *Applied Physics Letters* **95** 261106

[23] Sze S M and Ng K K 2006 *Physics of semiconductor devices*: John Wiley & Sons)

[24] Kim H, Park M H, Park S J, Kim H-S, Song J D, Kim S-H, Kim H, Choi W J and Kim D-W 2014 Influence of InAs quantum dots on the transport properties of GaAs-based solar cell devices *Current Applied Physics* **14** 192-5

[25] Sellai A, Henini M and Ouennoughi Z 2011 Temperature dependence of dark current in a p–i–n photodiode incorporating a resonant tunneling structure *physica status solidi (a)* **208** 210-4

[26] Houng M, Wang Y, Chen H, Wei H and Lee Y 1992 The negative differential resistance behavior in delta-doped GaAs structure due to resonant interband tunneling *Journal of Applied Physics* **71** 780-2

[27] Gunawan O, Wang K, Fallahazad B, Zhang Y, Tutuc E and Guha S 2011 High performance wire-array silicon solar cells *Progress in Photovoltaics: Research and Applications* **19** 307-12

[28] Chiquito A, Pusep Y A, Mergulhão S and Galzerani J 2002 Capacitance-voltage characteristics of InAs dots: a simple model *Brazilian Journal of Physics* **32** 784-9

[29] Babiński A, Wysmołek A, Tomaszewicz T, Baranowski J, Leon R, Lobo C and Jagadish C 1998 Electrically modulated photoluminescence in self-organized InGaAs/GaAs quantum dots *Applied Physics Letters* **73** 2811-3

[30] Kim J S, Kim E K, Kim J O, Lee S J and Noh S K 2009 Study on carrier trapping and emission processes in InAs/GaAs self-assembled quantum dots by varying filling pulse width during DLTS measurements *Superlattices and Microstructures* **46** 312-7

[31] Kaniewska M and Engström O 2007 Deep traps at GaAs/GaAs interface grown by MBE-interruption growth technique *Materials Science and Engineering: C* **27** 1069-73

[32] Schubert E F 2005 *Doping in III-V semiconductors* vol 1: Cambridge University Press)

[33] Geller M, Stock E, Kapteyn C, Sellin R and Bimberg D 2006 Tunneling emission from self-organized In (Ga) As⁄GaAs quantum dots observed via time-resolved capacitance measurements *Physical Review B* **73** 205331

[34] Park Y M, Park Y J, Kim K M, Shin J C, Song J D, Lee J I and Yoo K-H 2004 Electrical and optical characterizations of self-assembled quantum dots formed by the atomic layer epitaxy technique *Journal of Applied Physics* **95** 123-7

[35] Fang Z, Xie Q, Look D C, Ehret J and Van Nostrand J 1999 Electrical characterization of self-assembled In 0.5 Ga 0.5 As/GaAs quantum dots by deep level transient spectroscopy *Journal of electronic materials* **28** L13-L6

[36] Ershov M, Ryzhii V and Saito K 1995 Capacitance-voltage characteristics of multiple-quantum-well semiconductor heterostructures *Journal of Physics D: Applied Physics* **28** 2118

[37] Moon C, Choe B-D, Kwon S, Shin H and Lim H 1998 Electron distribution and capacitance–voltage characteristics of n-doped quantum wells *Journal of Applied Physics* **84** 2673-83

[38] Lang D 1974 Deep-level transient spectroscopy: A new method to characterize traps in semiconductors *Journal of Applied Physics* **45** 3023-32

[39] Dobaczewski L, Peaker A and Bonde Nielsen K 2004 Laplace-transform deep-level spectroscopy: The technique and its applications to the study of point defects in semiconductors *Journal of applied physics* **96** 4689-728

[40] Boumaraf R, Sengouga N, Mari R, Meftah A, Aziz M, Jameel D, Al Saqri N, Taylor D and Henini M 2014 Deep traps and temperature effects on the capacitance of p-type Si-doped GaAs Schottky diodes on (211) and (311) oriented GaAs substrates *Superlattices and Microstructures* **65** 319-31

[41] Aziz M, Ferrandis P, Mesli A, Mari R H, Felix J F, Sellai A, Jameel D, Al Saqri N, Khatab A and Taylor D 2013 Deep-level transient spectroscopy of interfacial states in “buffer-free” pin GaSb/GaAs devices *Journal of Applied Physics* **114** 134507

[42] Pons D and Bourgoin J 1985 Irradiation-induced defects in GaAs *Journal of Physics C: Solid State Physics* **18** 3839

[43] Corbel C, Stucky M, Hautojärvi P, Saarinen K and Moser P 1988 Positron-annihilation spectroscopy of native vacancies in as-grown GaAs *Physical Review B* **38** 8192

[44] Loualiche S, Nouailhat A, Guillot G and Lannoo M 1984 Interpretation of deep-level optical spectroscopy and deep-level transient spectroscopy data: application to irradiation defects in GaAs *Physical Review B* **30** 5822

[45] Lai S and Nener B 1994 Annealing behavior of deep-level defects in 1 MeV electron irradiated GaAs *Journal of Applied Physics* **75** 2354-7

[46] Lang D V, Cho A Y, Gossard A, Ilegems M and Wiegmann W 1976 Study of electron traps in n-GaAs grown by molecular beam epitaxy *Journal of Applied Physics* **47** 2558-64

[47] Lee K S, Lee D U, Kim E K and Choi W J 2015 Effect of space layer doping on photoelectric conversion efficiency of InAs/GaAs quantum dot solar cells *Applied Physics Letters* **107** 203503

[48] Asano T, Fang Z and Madhukar A 2010 Deep levels in GaAs (001)/InAs/InGaAs/GaAs self-assembled quantum dot structures and their effect on quantum dot devices *Journal of Applied Physics* **107** 073111

[49] Kunets V P, Morgan T A, Mazur Y I, Dorogan V, Lytvyn P, Ware M, Guzun D, Shultz J and Salamo G 2008 Deep traps in GaAs/InGaAs quantum wells and quantum dots, studied by noise spectroscopy *Journal of Applied Physics* **104** 103709

[50] Lin S, Balocco C, Missous M, Peaker A and Song A 2005 Coexistence of deep levels with optically active InAs quantum dots *Physical Review B* **72** 165302

[51] Vakulenko O, Golovynskyi S and Kondratenko S 2011 Effect of carrier capture by deep levels on lateral photoconductivity of InGaAs/GaAs quantum dot structures *Journal of Applied Physics* **110** 043717

[52] Krishnamurthy S, Van Schilfgaarde M and Newman N 2003 Spin lifetimes of electrons injected into GaAs and GaN *Applied Physics Letters* **83** 1761-3

[53] Teh C, Tuszyński J and Weichman F 1990 The decay of carbon, luminescence in liquid-encapsulated Czochralski-grown semi-insulating GaAs *Journal of Materials Research* **5** 365-71