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A Method for the Suppression of Fluctuations in the Neutral-Point Potential of a Three-Level NPC Inverter with a Capacitor-Voltage Loop

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***Abstract*: This paper investigates the problem of fluctuation of the neutral-point potential (NPP) in a three-level NPC inverter with a capacitor-voltage loop. The phase pulse width duty cycle disturbance PWM method is proposed to suppress the NPP fluctuation efficiently. Based on the basic carrier-based Phase Disposition (PD) PWM method, the average pulse neutral-point current model is established. Then the frequency, amplitude and equivalent initial phase of the NPP fluctuation are analyzed based on the current model. According to the alternating error of the DC-link capacitor voltages, a capacitor-voltage loop with a quasi PR (proportional resonant) controller is presented. The control variable, which varies with the modulation index, phase current, load power factor, etc, can be obtained from the quasi PR controller. Finally, an experimental three-level NPC inverter is described and the validity and feasibility of the proposed method are verified by experimental results.**

***Keywords*: Three-level NPC inverter, neutral-point potential, capacitor-voltage loop, fluctuation-suppression.**

I. Introduction

In order to step down d*v*/d*t*, improve the harmonic performance of the output voltage and current, and also reduce the voltage stress of power switches of inverters used in medium-voltage and high power applications, the three-level neutral-point clamped (NPC) inverter was proposed [1]. However a particular problem with the NPC compared to traditional two-level inverters, is the fluctuation of the capacitor midpoint voltage or neutral-point potential (NPP) due to influences from the modulation index and the load power factor [2]. Capacitor voltage imbalance may cause failure of the power switches and the series connected DC-link capacitors. In addition low-order harmonics will be created in the output voltage and current, due to low-frequency ripple of the NPP [3]. Therefore, a great deal of research on the NPP fluctuation problem of three-level NPC inverters has been carried out [4]. In medium-voltage induction motor drive systems, the three-level NPC inverter can eliminate NPP fluctuation by using two isolated voltage sources instead of capacitors in series [5, 6]. In addition, the NPP fluctuation could also be removed through using a front-end converter such as a three-level boost converter or a back to back topology [7, 8]. These additional converters can be used to inject or extract current into or from the neutral point if necessary [9]. However, with the additional hardware circuits, the volume and cost of the system are increased while the efficiency and the reliability of the system are reduced. Therefore, improving the modulation performance is a better way to restrain the NPP fluctuation as this removes the need for extra converters [10-13].

There are two main modulation strategies for the three-level NPC inverter, namely space vector pulse width modulation (SVPWM) and carrier-based PWM [14, 15]. The nearest three vectors (NTV) modulation is one of the common SVPWM methods [16]. It conforms to the principle in which the reference vector is synthesized by the nearest three vectors and can prevent overlapping of the level layers in the line to line voltages (analyzed in [17]), as well as reducing the total harmonic distortion (THD). However, the essence of the NTV modulation method is that a third-order harmonic is injected into the three-phase sinusoidal modulation waves, and its fluctuation-suppression for NPP is limited (this is analyzed in detail in Section III. A). Therefore, the nearest three virtual vectors (NTV^2) method was proposed to enhance the capability for fluctuation-suppression [18, 19]. Compared to the NTV method, the NTV^2 method goes against the principle of the synthesized reference vector, and produces overlapping of level layers and as much as 25% more switching actions in every fundamental period. Naturally, the hybridization of the NTV and the NTV^2 methods is a tradeoff between the fluctuation-suppression and the fundamental switching number. The proportional index p_m, such as p_m=0.5, was used to determine the extent of the alternate action in a fundamental period [20], but the overlapping of level layers still exists in this proportional hybrid SVPWM strategy in line to line voltages.

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The three-level NPC inverter is suitable for electric power plants, municipal water supply systems, etc. It is mainly used in medium-voltage and high power variable voltage variable frequency (VVVF) induction motor drive systems [21, 22]. Therefore, according to the designed voltage-frequency curve, the required speed adjustment of the fan or pump results in the induction motor's variable voltage and power factor, as well as its phase currents [23]. However, the combinations of the variable voltage, power factor and phase current due to the changed speed of the induction motor may affect the neutral-point current (namely the neutral-point potential) of the NPC inverter. A basic carrier-based PD PWM method with a capacitor-voltage loop is proposed in this paper, in order to solve the problem of the NPP fluctuation, and avoid the disadvantages (more switching actions and overlapping levels of the line to line voltages) of the NTV[2], the hybridization of the NTV and the NTV[2] methods mentioned above. This proposed method can also reduce the impact of the practical imbalance capacitance of the series connected DC-link capacitors.

Moreover, the VVVF control is adopted for the inverter to supply a three-phase *RL* load (for the convenience of exactly obtaining the combinations of the variable voltage, power factor and phase current) in this paper. It thus begins with the theoretical analysis of the NPP fluctuation frequency, amplitude, and equivalent initial phase, based on the basic carrier-based PD PWM method. Then, the NPP fluctuation method with injected 3rd harmonic PWM is introduced with its limited ability to suppress the NPP fluctuation, due to the constant initial phase of the injected 3rd harmonic component. The capacitor-voltage loop with the quasi PR controller that is presented here can create a variable zero sequence component, i.e. a variable equivalent initial phase, according to the load power factor. Furthermore, the proposed phase pulse width duty cycle disturbance PWM method changes the modulation waves in the presence of NPP, resulting in an efficient suppression of NPP fluctuation, as well as less switching actions, non-overlapping levels of the line to line voltages, and tolerance to the imbalance capacitance of the series connected DC-link capacitors.

II. Basic Analysis of NPP Fluctuation

A. Frequency of NPP Fluctuation

The topology of the three-level NPC inverter is shown in Fig. 1. The capacitance of the DC-link capacitors C_{cap1}, C_{cap2} are equal (C_1=C_2), and the DC-link voltage U_{dc} is divided into U_{cap1}=U_{cap2}=U_{dc}/2. Point "o" is the neutral point. The basic carrier-based PD PWM method is adopted to control the power switches Q_{x1}~Q_{x4}, where x stands for Phases a, b, and c.

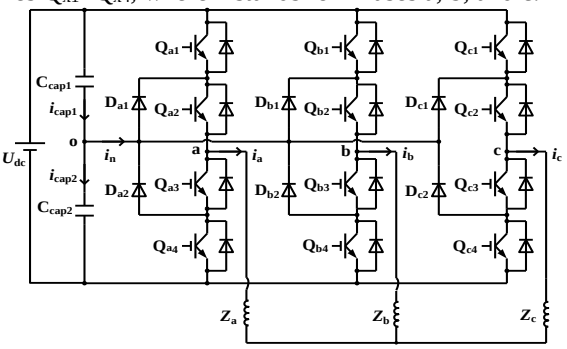


Fig. 1. Topology of three-level NPC inverter.

The neutral-point potential U_o can be regarded as the voltage across C_{cap2} as follows

$$U_o = U_{cap2} \tag{1}$$

Given that medium or small vectors cause corresponding NP current during the action time, so C_{cap1} is charged or discharged, and C_{cap2} is discharged or charged, under the condition of U_{cap1}+ $U_{cap2} \equiv U_{dc}$. The voltage ripple of C_{cap2} is determined by i_n and the action time dt (dt << T , T is the fundamental period), by virtue of the corresponding vector. From Fig. 1, it can be seen that the voltage ripple Δu_2 of C_{cap2} is the difference between U_{cap2} and U_{dc}/2, namely the NPP fluctuation Δu_o is written as

$$\Delta u_o = \Delta u_2 = U_{cap2} - U_{dc}/2 = \frac{1}{C_2}\int_0^{t_{ecp}} i_{cap2}\mathrm{d}t \tag{2}$$

where i_{cap2} is the instantaneous current flowing into or out of C_{cap2}, during the vector action time dt; t_{ecp} is defined as the effective charging or discharging time when U_{cap2} goes from U_{dc}/2 to the peak value. According to Fig. 1, when medium or small vectors act, the current equation concerning the neutral point "o" can be obtained as follows

$$i_{cap1} = i_{cap2} + i_n \tag{3}$$

The charging or discharging state of C_{cap2} is shown in Fig. 2. This results from the NP current i_n when using the basic carrier-based PD PWM method over a fundamental period. In fact, i_n is the pulsed NP current, as shown in Fig. 2(e). Its pulse amplitude corresponds to the instantaneous phase current. In addition, the three-phase sinusoidal modulation waves are divided into six regions I~VI, as depicted in Fig. 2(a). The phase pulse width duty cycle is defined as the ratio of the positive or negative phase voltage pulse width to the carrier period, as denoted in Fig. 2(b~d). The phase pulse width duty cycle d_x can also be defined as the ratio of the modulation wave instantaneous value (-1~1) to the corresponding carrier amplitude (1 or -1), i.e. it can be expressed as

$$d_x = \left| u_{ref\_x} \right| \tag{4}$$

where d_x=0~1. According to Fig. 2(e), it is noted that the pulse NP current i_n varies with both the duty cycles and the phase currents. As a result, the average current flowing into the neutral point can be described as

$$\bar{i}_n = -(d_a \times i_a + d_b \times i_b + d_c \times i_c) \tag{5}$$

where $\bar{i}_n$ is the average pulse NP current; d_a, d_b and d_c are phase pulse width duty cycles; i_a, i_b, and i_c are three-phase instantaneous currents.

The three-phase sinusoidal modulation waves are defined as

$$\begin{cases} u_{ref\_a} = m\sin\omega t \\ u_{ref\_b} = m\sin(\omega t - 2\pi/3) \\ u_{ref\_c} = m\sin(\omega t - 4\pi/3) \end{cases} \tag{6}$$

where m is the modulation index, and $0 \le m \le 1$; ω is the fundamental angular frequency. When the carrier frequency is much greater than the fundamental frequency and the three-level NPC inverter supplies a three-phase symmetrical *RL* load, the phase currents can be considered as sinusoidal

$$\begin{cases} i_a = I\sin(\omega t-\varphi) \\ i_b = I\sin(\omega t-2\pi/3-\varphi) \\ i_c = I\sin(\omega t-4\pi/3-\varphi) \end{cases} \quad (7)$$

where " I " is the phase current amplitude, and φ is the load power factor angle. Therefore, in terms of (4), each phase pulse width duty cycle in Region I ($\omega t\in[0,\pi/3)$) as shown in Fig. 2(a), can be written as follows

$$\begin{cases} d_{aI} = u_{ref\_a} = m\sin\omega t \\ d_{bI} = -u_{ref\_b} = -m\sin(\omega t-2\pi/3) \\ d_{cI} = u_{ref\_c} = m\sin(\omega t-4\pi/3) \end{cases} \quad (8)$$

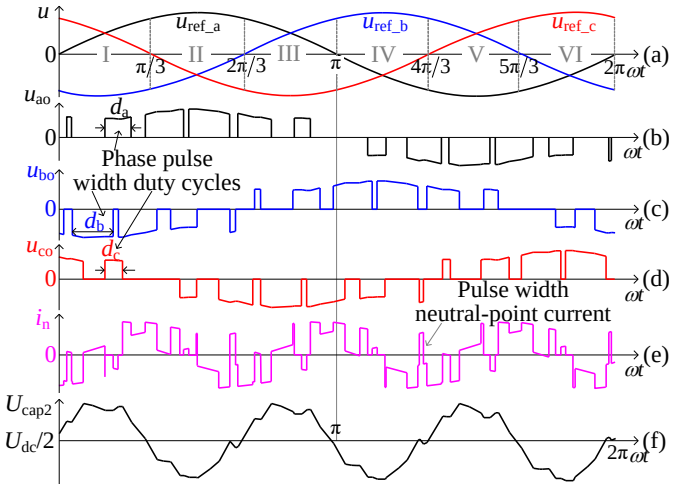


Fig. 2 Charging or discharging state of C_{cap2} by NP current i_n under basic carrier-based PD PWM method during a fundamental period.

According to (5), (7) and (8), the average pulse NP current $\bar{i}_{nI}$ in Region I can be obtained as

$$\begin{aligned} \bar{i}_{nI} &= -m\sin(\omega t)\times I\sin(\omega t-\varphi) \\ &\quad -[-m\sin(\omega t-2\pi/3)]\times I\sin(\omega t-2\pi/3-\varphi) \\ &\quad -m\sin(\omega t-4\pi/3)\times I\sin(\omega t-4\pi/3-\varphi) \\ &= -0.5mI[\cos\varphi+2\cos(2\omega t-4\pi/3-\varphi)] \end{aligned} \quad (9)$$

Likewise, the average pulse NP current in the other five regions can also be deduced, and the current model $\bar{i}_n$ can be established in a fundamental period $\omega t\in[0,2\pi)$ as follows

$$\bar{i}_n = \begin{cases} 0.5mI[-\cos\varphi-2\cos(2\omega t-4\pi/3-\varphi)], \omega t\in[0,\pi/3) \\ 0.5mI[\cos\varphi+2\cos(2\omega t-\varphi)], \omega t\in[\pi/3,2\pi/3) \\ 0.5mI[-\cos\varphi-2\cos(2\omega t-2\pi/3-\varphi)], \omega t\in[2\pi/3,\pi) \\ 0.5mI[\cos\varphi+2\cos(2\omega t-4\pi/3-\varphi)], \omega t\in[\pi,4\pi/3) \\ 0.5mI[-\cos\varphi-2\cos(2\omega t-\varphi)], \omega t\in[4\pi/3,5\pi/3) \\ 0.5mI[\cos\varphi+2\cos(2\omega t-2\pi/3-\varphi)], \omega t\in[5\pi/3,2\pi) \end{cases} \quad (10)$$

From (10), each of the expressions shows the frequency of " $\bar{i}_n$ " is twice the fundamental frequency during $\omega t\in[0,2\pi)$. In fact, the actual $\bar{i}_n$ is synthesized by the corresponding part of every expression in terms of the exact range of ωt shown in (10). As a result, there exists the unique time t_I when $\bar{i}_n=0$ during $\omega t\in[0,\pi/3)$. Thus ωt_I can be written as

$$\omega t_I = 0.5\times\mathrm{mod}\{[4\pi/3+\varphi+\arccos(-0.5\cos\varphi)],2\pi\} \quad (11)$$

where "mod" is the remainder function. Similarly, the other five expressions $\omega t_{II}\sim\omega t_{VI}$ can also be obtained in the other five regions. Consequently, there are six zero crossing points of $\bar{i}_n$ in a fundamental period according to (10) i.e. (ωt_I ,0), (ωt_{II} ,0), (ωt_{III} ,0), (ωt_{IV} ,0), (ωt_V ,0) and (ωt_{VI} ,0) and the frequency of $\bar{i}_n$ is three times the fundamental one. The DC-link capacitor voltages also fluctuate at three times the fundamental frequency. The simulation results of the neutral-point current and the fluctuating state of the capacitor voltage U_{cap2} are shown in Fig. 3, from a Matlab/Simulink simulation with the simulation condition of m=1, and $\cos\varphi=0.886$.

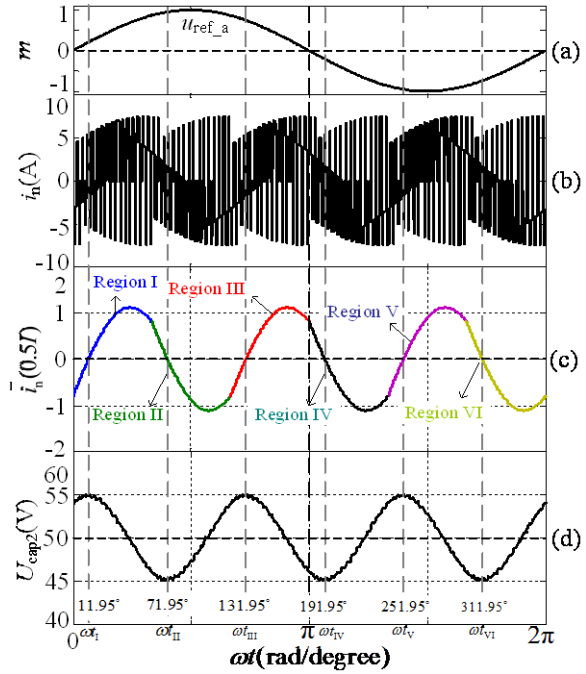


Fig. 3 Simulation results of neutral-point current and fluctuating state of capacitor voltage from Matlab/Simulink (simulation parameters: m=1, fundamental frequency f=50Hz, switching frequency f_c=4.67kHz, C_1=C_2=470 μF , U_{dc}=100V, load R=6 Ω , L=10mH, and $\cos\varphi=0.886$). (a) Sinusoidal modulation wave. (b) Pulse NP current. (c) Average pulse NP current. (d) Fluctuating voltage of C_{cap2}.

The "Phase-a" sinusoidal modulation wave u_{ref_a} is shown in Fig. 3(a), and the pulse NP current i_n is depictured in Fig. 3(b). In terms of (10), the average pulse NP current is shown in Fig. 3(c), and its amplitude is determined by m, I, and φ. Its frequency is three times the fundamental as analyzed above. Moreover, the charging and discharging characteristics for DC-link capacitors can be explained more clearly by $\bar{i}_n$: In Region I, $\bar{i}_n$ (blue curve) is from negative to positive with the zero crossing point (ωt_I, 0), where $\omega t_I=11.95^\circ$ is calculated by (11) with $\cos\varphi=0.886$; when $\bar{i}_n<0$, C_{cap1} is being discharged, and C_{cap2} is being charged; when $\bar{i}_n=0$, C_{cap1} is discharged down to the minimum voltage, and C_{cap2} is charged

up to the maximum; when $\bar{i}_n > 0$, C_{cap1} is being charged, and C_{cap2} is being discharged. When $\bar{i}_n$ (green curve) is in Region II, another zero crossing point occurs (ωt_{II}, 0) at $\omega t_{II} = 71.95^\circ$. At this time, C_{cap1} is charged up to the maximum voltage, and C_{cap2} is discharged down to the minimum as shown in Fig. 3(d). The fluctuation frequency of U_{cap2} is three times the fundamental as shown above.

B. Amplitude of NPP Fluctuation

According to (2), (10) and the conclusions for the NPP fluctuation frequency analyzed above, then by examining $U_{dc}/2$, the neutral-point potential U_o is at its maximum or minimum voltage during $T/12$. Therefore, the amplitude of the NPP fluctuation is directly determined by i_{cap1}, i_{cap2}, C_1, C_2, t_{ecp} in $T/12$, m, I, and φ. It is clear that the NPP fluctuation is inversely proportional to C_1 and C_2.

It should be noted that the charging or discharging states of C_{cap1} and C_{cap2} are opposite from each other, with the condition that $U_{cap1} + U_{cap2} \equiv U_{dc}$. When C_1, C_2, ω, m, and φ remain unchanged, i_{cap1} and i_{cap2} are proportional to i_n according to (3). i_{cap2} is proportional to I, as well as the amplitude of the NPP fluctuation by virtue of (2); when the fundamental angular frequency ω is decreased from ω_1 to ω_2, the period of $\bar{i}_n$ increases, leading to a longer distance between adjacent zero crossing points. Therefore the effective time t_{ecp}, which is the equivalent time for charging or discharging capacitors from $U_{dc}/2$ to the maximum or minimum voltage, increases proportionally from t_{ecp1} to $t_{ecp1} \times \omega_1 / \omega_2$. t_{ecp1} is the equivalent charging or discharging time when the fundamental angular frequency is ω_1. In addition, the amplitude of phase currents remains unchanged. Consequently the amplitude of the NPP fluctuation is ω_1 / ω_2 times that of the original one, as shown in Fig. 4, i.e. it is inversely proportional to the fundamental frequency.

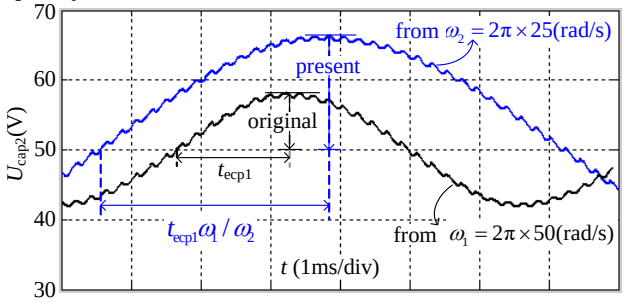
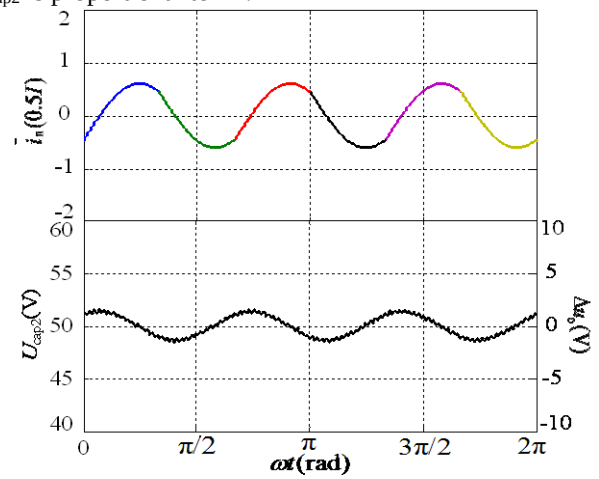
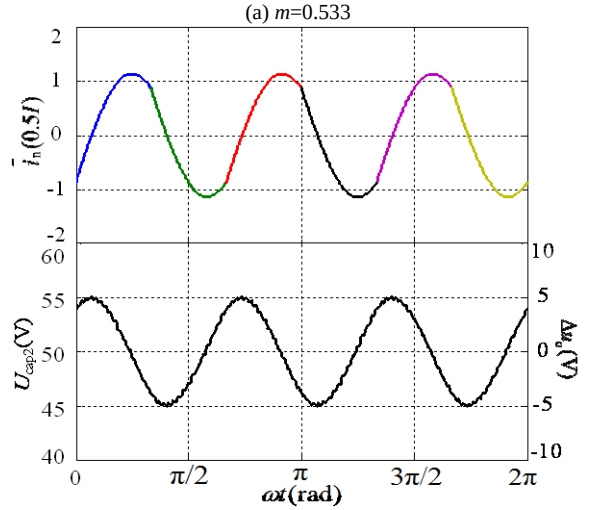


Fig. 4 Comparative amplitudes of NPP fluctuation between conditions of $\omega_1 = 2\pi \times 50$ (rad/s), L=10mH and $\omega_2 = 2\pi \times 25$ (rad/s), L=20mH (R=6 Ω).

In order to clarify the impacts of the modulation index and load power factor on the NPP fluctuation, an analysis of the three-level NPC inverter supplying a three-phase symmetrical *RL* load is made here. It is assumed that the load power factor is constant $\cos\varphi = 0.866$ ($R = 5.89\Omega$, L=10.8mH, fundamental frequency f=50Hz), while m is set to two conditions namely "0.533" and "1". The other simulation parameters are the same with those used for Fig. 3. The comparison of fluctuation amplitudes of the capacitor voltages with different modulation indexes is shown in Fig. 5. The amplitudes of $\bar{i}_n$ in Fig. 5 (a, b) are $0.6 \times 0.5I$ and $1.13 \times 0.5I$, respectively; and the fluctuation amplitude ΔU_2 of U_{cap2} is 1.4V and 5V. As shown in (10), with a constant φ, the amplitude of $\bar{i}_n$ is determined by m and I. The fluctuation amplitudes of the capacitor voltages are nearly proportional to the amplitude of $\bar{i}_n$. For an identical *RL* load and fundamental frequency, I is proportional to m. Therefore $\bar{i}_n$ is proportional to mI, i.e. the fluctuation amplitude ΔU_2 of U_{cap2} is proportional to m^2.



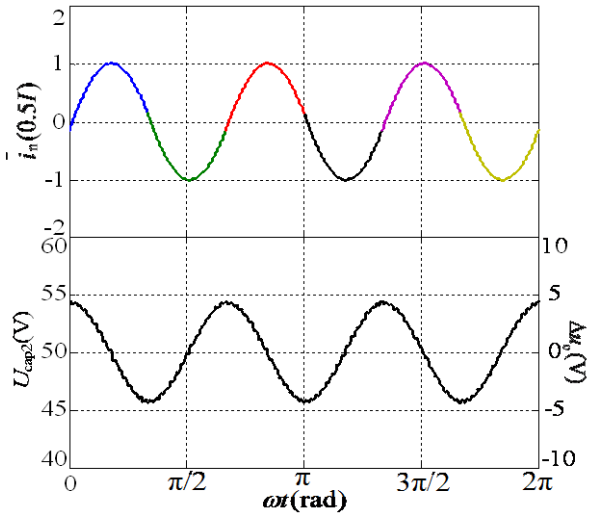
(a) m=0.533



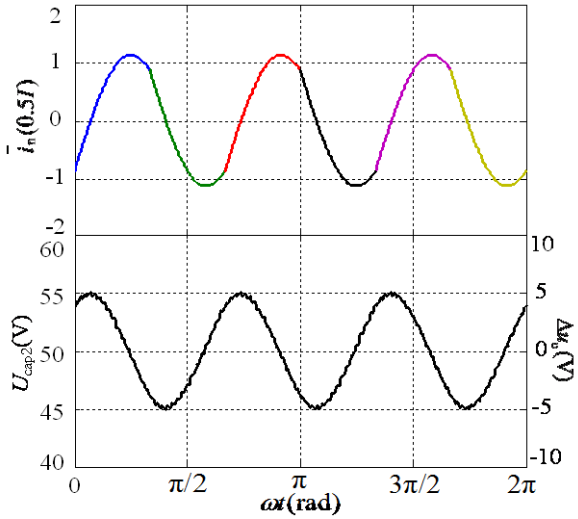
(b) m=1

Fig. 5 Comparison of fluctuation amplitudes of capacitor voltages with different modulation indexes (R=5.89 Ω, L=10.8mH, f=50Hz, and $\cos\varphi = 0.866$).

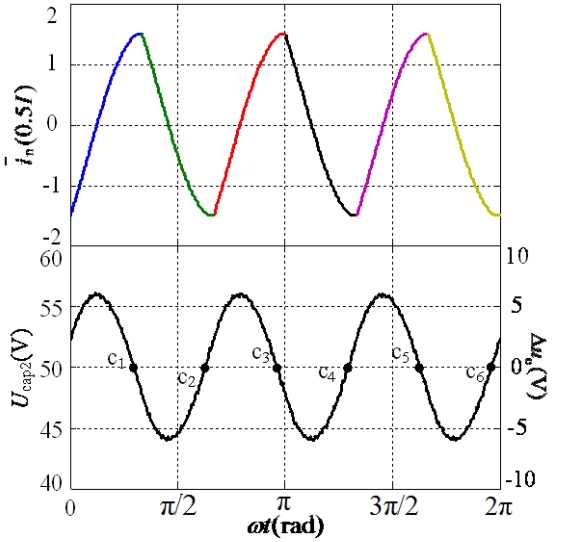
Regarding the impact of the load power factor, it is assumed that m=1, the phase impedance $Z_{phase} = 6.8\Omega$, and f=50Hz. With the same phase impedance, different load power factors can be obtained by adjusting the phase resistors and inductors, e.g. 0.996 ($\varphi = 5^\circ$), 0.866 ($\varphi = 30^\circ$), 0.5 ($\varphi = 60^\circ$) and 0.087 ($\varphi = 85^\circ$). The other simulation parameters remain the same as those in Fig. 3. The comparison of the fluctuation amplitudes of the capacitor voltages under different load power factors is shown in Fig. 6.



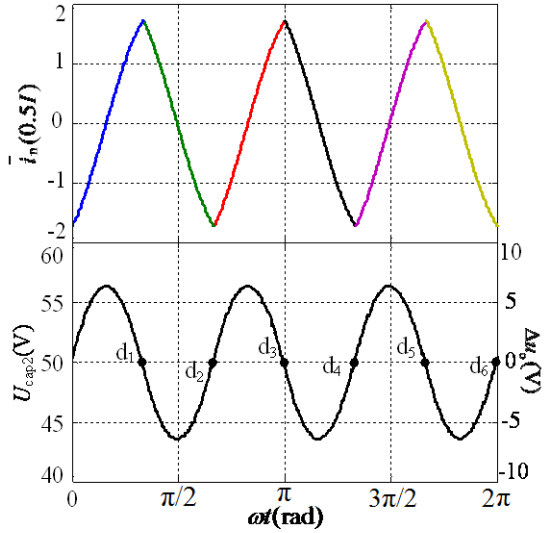
(a) R=6.77 Ω , L=1.89mH, $\varphi = 5^\circ$



(b) R=5.89 Ω , L=10.8mH, $\varphi = 30^\circ$



(c) R=3.4 Ω , L=18.75mH, $\varphi = 60^\circ$



(d) R=0.59 Ω , L=21.57mH, $\varphi = 85^\circ$

Fig. 6 Comparison of fluctuation amplitudes of capacitor voltages with different load power factors (m=1, Z_{phase} = 6.8Ω , and f=50Hz).

In terms of (11) and Fig. 3, there is a peak of $\bar{i}_n$ when the phase lags ωt_I is $\pi/6$. Combining this with (10), the amplitude function $\bar{I}_n(\varphi)$ of $\bar{i}_n$ can be obtained as follows

$$\begin{cases} \omega t_I = 0.5 \times \mathrm{mod}\{[4\pi/3 + \varphi + \arccos(-0.5\cos\varphi)], 2\pi\} \\ \bar{I}_n(\varphi) = 0.5I\{-\cos\varphi - 2\cos[2(\omega t_I + \pi/6) - 4\pi/3 - \varphi]\} \end{cases} \quad (12)$$

where $\varphi \in [0, \pi/2]$. According to (12), the relationship between $\bar{I}_n$ and φ is shown in Fig. 7. It should be noted that the linear relationship between $\bar{I}_n$ and φ is the "cb" line segment, and the nonlinear relationship takes place on the "ba" curve. Moreover, the nonlinear segment "ba" shows that the higher the load power factor is, the lower the influence on $\bar{i}_n$ from φ , as shown in Fig. 6. As a result, the NPP fluctuation amplitude ΔU_o is proportional to $\bar{I}_n = f(\varphi)$ as shown in Fig. 7, according to the charging or discharging characteristic of C_{cap1} and C_{cap2} as stated above.

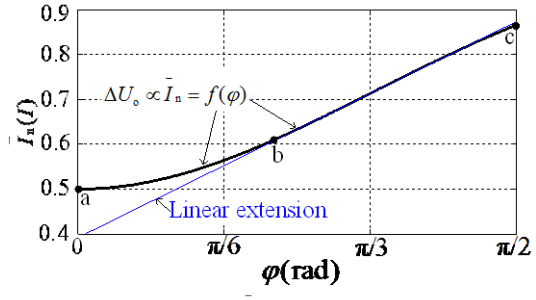


Fig. 7 Relationship between $\bar{I}_n$ and φ (m=1, and Z_{phase}=Constant).

C. Equivalent Initial Phase of NPP Fluctuation

The NPP fluctuation Δu_o alternates at triple fundamental frequency and its equivalent initial phase can be considered as $3(\omega t + \theta)$, referring to the phase ωt of the sinusoidal modulation wave $u_{ref\_a} = m\sin\omega t$. The phase of Δu_o is

determined by the load power factor angle φ in terms of Fig. 3 and (11), then the initial phase angle θ can be written as

$$\begin{aligned}\theta &= \pi/6\text{-}\omega t_{\mathrm{I}} \\ &= \pi/6 - 0.5\times \mathrm{mod}\left\{[4\pi/3+\varphi+\arccos(-0.5\cos\varphi)], 2\pi\right\}\end{aligned} \tag{13}$$

The relationship between θ and φ is shown in Fig. 8. It is noted that θ decreases from $\pi/6$ to zero, according to the increase of $\varphi\in[0,\pi/2]$. As a result, six zero crossing points of Δu_{o} all cause a right shift from points c_1~c_6 as shown in Fig. 6(c) to the corresponding ones d_1~d_6 in Fig. 6(d). It reveals the substantial change of the initial phase due to the impact of the load power factor.

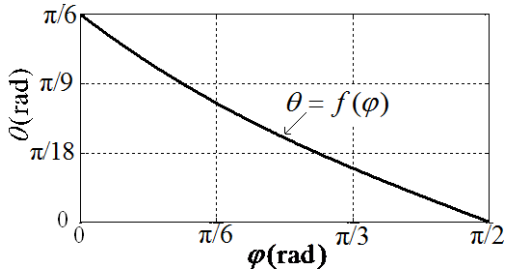


Fig. 8 Relationship between θ and φ.

III. Fluctuation-Suppression Method of NPP

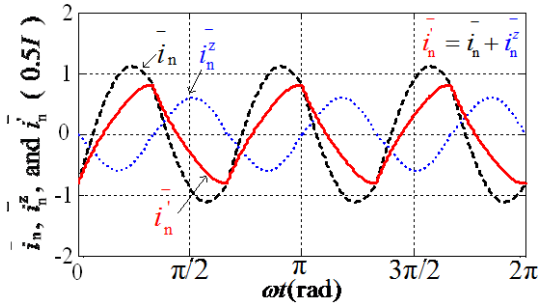
A. NPP Fluctuation with Injected 3rd Harmonic PWM

It is known that the injected 3rd harmonic ($m\sin 3\omega t/6$) PWM method not only can improve the utilization of the DC-link voltage of the three-phase inverter, but does not change the characteristics of line to line voltages [24]. According to (5), (7), (8), and (10), the injected 3rd harmonic can also cause a corresponding average pulse NP current $\bar{i}_{\mathrm{n}}^{z}$ shown in (14)

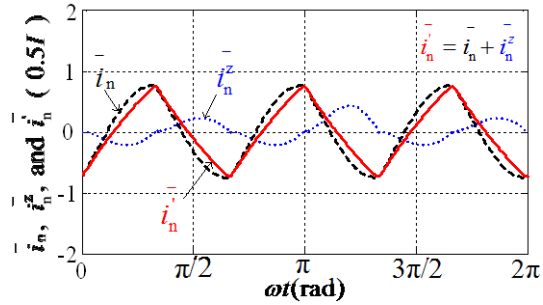
$$\bar{i}_{\mathrm{n}}^{z}=\begin{cases} mI[-\cos(4\omega t-2\pi/3-\varphi)+\cos(2\omega t+2\pi/3+\varphi)]/6, \omega t\in[0,\pi/3) \\ mI[\cos(4\omega t-\varphi)-\cos(2\omega t+\varphi)]/6, \omega t\in[\pi/3,2\pi/3) \\ mI[-\cos(4\omega t-4\pi/3-\varphi)+\cos(2\omega t+4\pi/3+\varphi)]/6, \omega t\in[2\pi/3,\pi) \\ mI[\cos(4\omega t-2\pi/3-\varphi)-\cos(2\omega t+2\pi/3+\varphi)]/6, \omega t\in[\pi,4\pi/3) \\ mI[-\cos(4\omega t-\varphi)+\cos(2\omega t+\varphi)]/6, \omega t\in[4\pi/3,5\pi/3) \\ mI[\cos(4\omega t-4\pi/3-\varphi)-\cos(2\omega t+4\pi/3+\varphi)]/6, \omega t\in[5\pi/3,2\pi) \end{cases} \tag{14}$$

As a result, the actual synthesized average pulse NP current $\bar{i}_{\mathrm{n}}^{'}=\bar{i}_{\mathrm{n}}+\bar{i}_{\mathrm{n}}^{z}$ can be obtained. The injected modulation wave of "Phase-a" is $u_{\mathrm{ref\_a}}^{'}=m\sin\omega t+(m\sin 3\omega t)/6$, and the injected $u_{\mathrm{ref\_b}}^{'}$, $u_{\mathrm{ref\_c}}^{'}$ lag $u_{\mathrm{ref\_a}}^{'}$ 120° and 240° respectively.

According to (10) and (14), the average pulse NP currents with injected 3rd harmonic PWM method under the VVVF control mode are shown in Fig. 9. When m=1, f=50Hz, and $\cos\varphi=0.886$, the injected average pulse NP current $\bar{i}_{\mathrm{n}}^{z}$ can offset the amplitude of the average pulse NP current $\bar{i}_{\mathrm{n}}$ by a significant amount. The amplitude of the synthesized average pulse NP current $\bar{i}_{\mathrm{n}}^{'}$ is reduced further as shown in Fig. 9(a). Nevertheless, the injected average pulse NP current $\bar{i}_{\mathrm{n}}^{z}$ cannot counteract $\bar{i}_{\mathrm{n}}$ enough when m=0.533, f=25Hz, and $\cos\varphi=0.59$, the amplitude of $\bar{i}_{\mathrm{n}}^{'}$ is virtually unchanged as shown in Fig. 9(b). Therefore, it is concluded that the injected 3rd harmonic component, whose initial phase is constant (i.e. does not change with the modulation index, load current and power factor), cannot suppress the amplitude of the synthesized average pulse NP current $\bar{i}_{\mathrm{n}}^{'}$ efficiently under VVVF control.



(a) m=1, f=50Hz, R=6 Ω, L=10mH, $\cos\varphi=0.886$



(b) m=0.533, f=25Hz, R=4.54 Ω, L=40mH, $\cos\varphi=0.59$

Fig. 9 Average pulse NP currents with injected 3rd harmonic PWM method under VVVF control mode.

B. Phase Pulse Width Duty Cycle Disturbance PWM Method

In terms of (10) and (14), factors m, I, φ etc, can be considered as disturbance sources in the capacitor-voltage loop (in Section III. C). These factors are directly associated with the *RL* loads, and their combined effect would influence the amplitude of the synthesized average pulse NP current. Based on the referred basic carrier-based PD PWM method with saddle modulation waves, the phase pulse width duty cycle disturbance PWM method (in "Phase-a") is demonstrated in Fig. 10. When m=0.533, I=3.4A, $\cos\varphi=0.59$ and f=25Hz, the second zero sequence component u_{pr}=u_3 can be obtained through the quasi PR controller, according to the capacitor voltage error Δu_{12}. Then, u_3 can be injected into the referred saddle modulation wave $u_{\mathrm{ref\_a}}^{'}$. Therefore, the original phase pulse width duty cycle $d_{\mathrm{a}}^{'}$ is modified to be $d_{\mathrm{a}}^{''}$ according to the final modulation wave $u_{\mathrm{ref\_a}}^{''}$, as shown in Fig. 10(a). Because the disturbance information is transferred to modulation waves by u_3 in real time, samples and calculations for phase currents and load power factors can be omitted completely.

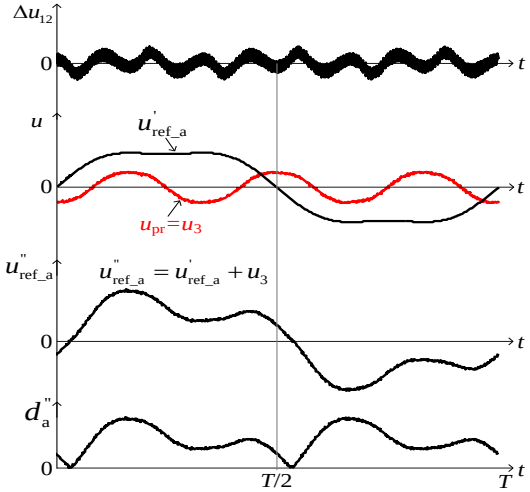
If the VVVF operation condition is below m=1, I=7.4A, $\cos\varphi=0.886$ and f=50Hz, the output u_{pr} of the quasi PR controller (in Section III. C) may suffer from over modulation (in certain parts) according to the capacitor voltage error Δu_{12}, which is different from the case in Fig. 10(a). In order to avoid

load current distortion, it is necessary to limit the amplitude of u_{pr} in terms of $\left|u_{pr}+u'_{ref\_x}\right|\le 1$ [25], where x stands for Phases a, b, and c. It is also noted that the $\max(u'_{ref\_a},u'_{ref\_b},u'_{ref\_c})$ and $\min(u'_{ref\_a},u'_{ref\_b},u'_{ref\_c})$ stand for the maximum and minimum instantaneous saddle waves in every fundamental period, so u_{pr} can be limited as follows

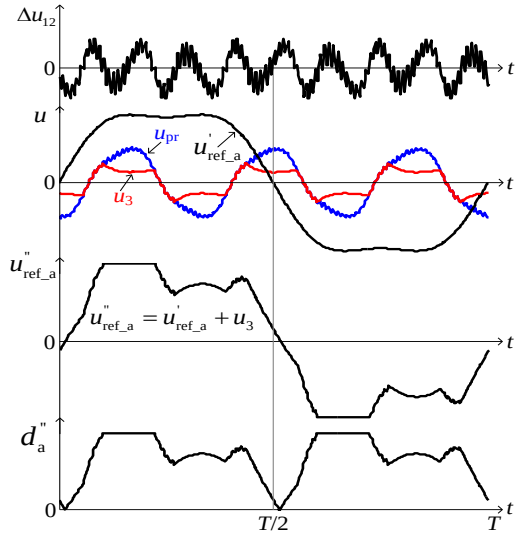
$$-1-\min(u'_{ref\_a},u'_{ref\_b},u'_{ref\_c})\le u_{pr}\le 1-\max(u'_{ref\_a},u'_{ref\_b},u'_{ref\_c}) \quad (15)$$

According to (15), the second zero sequence component u_3 can be obtained from u_{pr} as shown in Fig. 10(b). Then the original phase pulse width duty cycle d'_a is also modified to be d''_a due to the final modulation wave u''_{ref_a}. Furthermore, u''_{ref_a} is clamped at "1" to prevent over modulation and this is beneficial to reduce the switching number in each fundamental period, lowering the switching loss of the inverter.

From Fig. 10, it can be concluded that the disturbance PWM method optimizes the charging and discharging balanced states between C_{cap1} and C_{cap2} in terms of the asymmetric modulation wave obtained.



(a) m=0.533, and f=25Hz



(b) m=1, and f=50H

Fig. 10 Phase pulse width duty cycle disturbance PWM method in capacitor-voltage loop (in "Phase-a").

C. Capacitor-Voltage Loop Control with Quasi PR Controller

If a different injected harmonic could cause the proper average pulse NP current to make the final actual synthesized average pulse NP current closer to zero, the NPP fluctuation Δu_o would be suppressed close to zero. In fact, the voltage difference $\Delta u_{12} = U_{cap1} - U_{cap2}$ directly reflects the essence of Δu_o. In terms of the basic analysis of the NPP fluctuation in Section II (A~C), Δu_{12} is the alternating component with the triple fundamental frequency, especially as it contains information on the load current amplitude, power factor etc. Its amplitude, frequency and equivalent initial phase change with loading.

Therefore, Δu_{12} could be a second injected zero sequence component, which can suppress the final synthesized average pulse NP current efficiently. To achieve this, a capacitor-voltage loop control method with a quasi PR controller is proposed for the suppression of the fluctuation of the NPP as shown in Fig. 11. In terms of $U_{cap1}+U_{cap2}\equiv U_{dc}$, the capacitor voltages fluctuate in opposite directions, and therefore U_{cap2} would follow U_{cap1} infinitely according to the feedback mechanism.

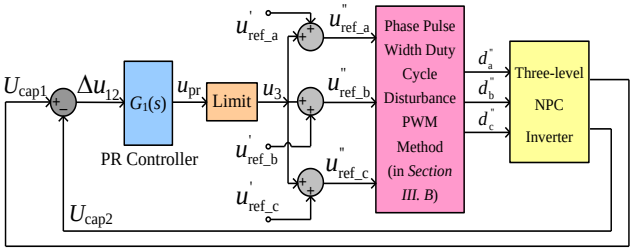


Fig. 11 Capacitor-voltage loop control method with quasi PR controller for fluctuation-suppression of NPP.

The actual second zero sequence component u_3 can be obtained after Δu_{12} is imported into the controller. The transfer function is $G_1(s)$:

$$u_{pr} = \Delta u_{12}\cdot G_1(s) \quad (16)$$

where Δu_{12} is also the input error to this controller, and this alternating input error can be constrained effectively by the nonlinear quasi PR controller [26]. Its transfer function is written as

$$G_1(s) = G_{PR}(s) = k_p + k_r\frac{2\omega_c s}{s^2+2\omega_c s+\omega_0^2} \quad (17)$$

where k_p is the proportional coefficient; k_r is the resonant coefficient; ω_0 is the resonant angular frequency; ω_c is the cutoff angular frequency, and $\omega_c << \omega_0$. The controller parameters have been derived from the model parameters [26] as k_p=0.05, k_r=2, $\omega_c = 2\pi\times(0.02f)$, and $\omega_0 = 2\pi\times(3f)$, where f is the fundamental frequency.

IV. Experimental Verification and Analysis

The proposed fluctuation-suppression method of the NPP for the three-level NPC inverter is verified using the experiment platform shown in Fig. 12. The digital controller is composed of DSP (TMS320F28335) and FPGA (Cyclone EP1C6Q240C8N);

the power switches are IGBTs (FGA40N120D) used to form the main circuit of the inverter. The DC-link voltage is supplied by two DC voltage sources in series for U_{dc}=100V. A three-phase adjustable resistor and inductor (*RL*) were chosen as the load for the inverter. Voltages across DC-link capacitors are measured by voltage sensors. Phase-a modulation wave can be displayed from a DA converter (0.175/V). Finally, the inverter with the three-phase adjustable *RL* load operates under VVVF control mode, and experimental parameters are listed in TABLE I.

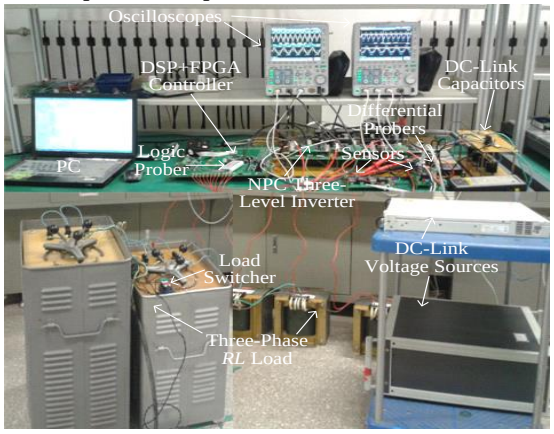
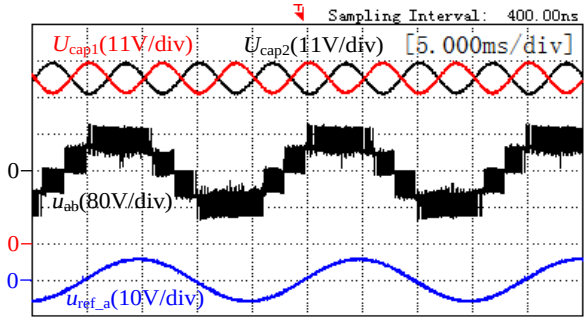


Fig. 12 Experiment platform for the three-level NPC inverter.

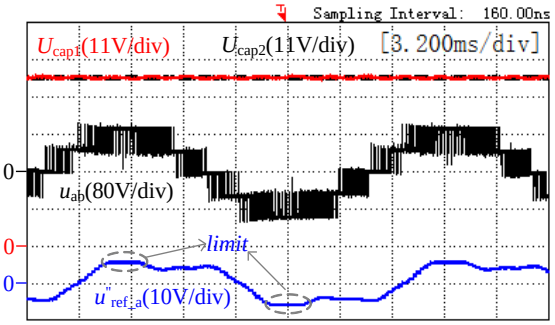
TABLE I Experimental parameters

Parameter	Value
DC-Link voltage U_{dc}	100V
DC-Link capacitance C_1=C_2	470 μF
Resistor and inductor of *RL* load	R=0~15 Ω , L=5~40mH
Switching frequency f_c	4.67kHz
Variable modulation index variable frequency of VVVF control mode	m=1/f=50Hz, m=0.733/f=40Hz, m=0.533/f=25Hz
Variable load power factor under VVVF control	0.886 (m=1), 0.59 (m=0.533)

The experimental results using the basic and proposed control methods are shown in Fig. 13. The amplitudes of the capacitor voltages U_{cap1} and U_{cap2} for the basic control are approximately 10% of U_{dc}/2 as shown in Fig. 13(a). Under the same conditions, the amplitudes of U_{cap1} and U_{cap2} decrease significantly with the proposed control as shown in Fig. 13(b). Moreover, the proposed method reduces the switching number in a fundamental period by limiting the maximum value of the final modulation wave u''_{ref_a} as shown in Fig. 13(b), and there is no overlapping of level layers in the line to line voltage with both methods, comparing with the NTV[2], the hybridization of the NTV and the NTV[2] methods.



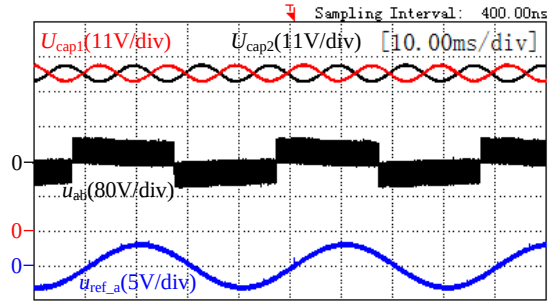
(a) Sinusoidal modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using basic carrier-based PD PWM method



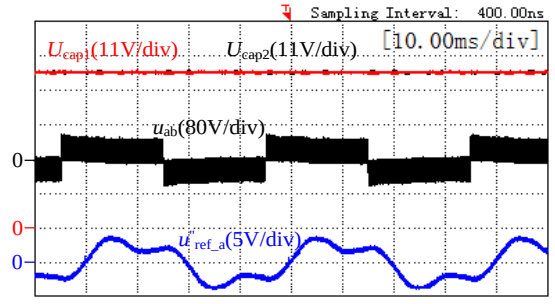
(b) Final modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using proposed PWM method

Fig. 13 Experimental results using basic and proposed methods (m=1, f=50Hz, $\cos\varphi = 0.886$, $R = 6\Omega$, L=10mH and C_1=C_2= 470μF).

When the variable modulation index, fundamental frequency and load power factor decrease following a change in operating setpoint, both m and I decrease. However, the fundamental period increases, and the fluctuation of U_{cap1} and U_{cap2} is still larger with the basic carrier-based PD PWM method, approximately 5% of U_{dc}/2 as shown in Fig. 14(a). Under the same conditions, comparing u_{ref_a} with u''_{ref_a} in Fig. 14(a, b), the final modulation wave u''_{ref_a} controlled by the proposed method is modified with the reduced modulation index, fundamental frequency and load power factor. As a result, the fluctuation of U_{cap1} and U_{cap2} is further reduced as shown in Fig. 14(b).



(a) Sinusoidal modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using basic carrier-based PD PWM method



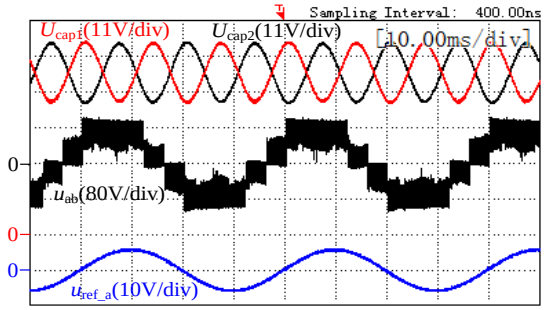
(b) Final modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using proposed PWM method

Fig. 14 Experimental results using basic and proposed methods (m=0.533, f=25Hz, $\cos\varphi = 0.59$, $R = 4.5\Omega$, L=40mH and C_1=C_2= 470μF).

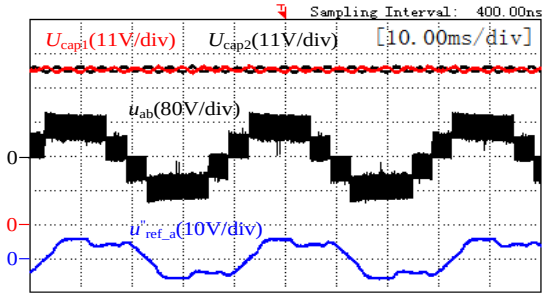
In order to verify the fundamental period effect on the fluctuation, the fundamental frequency is changed from 50Hz to a half (25Hz), and the inductor is also changed from 10mH to 20mH: m=1 and the other parameters are kept the same as those used for Fig. 13. The phase current amplitude and the load power factor remain unchanged. As a result, with the basic carrier-based PD PWM method, U_{cap1} and U_{cap2} fluctuate by about 20% of U_{dc}/2 shown in Fig. 15(a), i.e. twice those in Fig.

13 (a). It is consistent with the analytic result depicted in Fig. 4. However, the fluctuation of U_{cap1} and U_{cap2} is suppressed efficiently as shown in Fig. 15(b), to about 2% of $U_{dc}/2$ using the proposed PWM method. Therefore, the NPP fluctuation is almost eliminated by the proposed PWM method.

It is also noted that although the capacitance of the DC-link capacitors is reduced by half, and the other parameters are the same as those used in Fig. 13, the fluctuation of U_{cap1} and U_{cap2} is still suppressed well using the proposed PWM method as shown in Fig. 16, to about one fifth of that shown in Fig. 13(b). Thus, it is concluded that the proposed PWM method is beneficial for reducing the capacitance of the DC-link capacitors.



(a) Sinusoidal modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using basic carrier-based PD PWM method



(b) Final modulation wave (bottom), line to line voltage (middle) and capacitor voltages (upper) using proposed PWM method

Fig. 15 Experimental results using basic and proposed PWM methods when fundamental frequency is reduced by half (m=1, f=25Hz, $\cos\varphi = 0.886$, $R = 6\Omega$, L=20mH and C_1=C_2= 470μF).

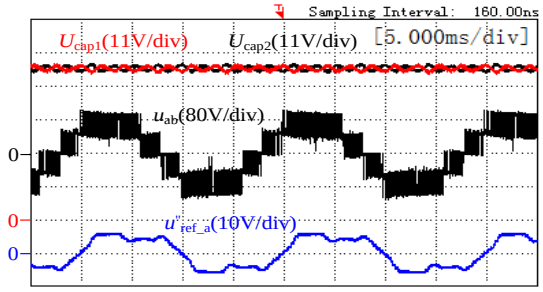


Fig. 16 Experimental results using proposed PWM method when capacitance of DC-link capacitors is reduced by half (m=1, f=50Hz, $\cos\varphi = 0.886$, $R = 6\Omega$, L=10mH and C_1=C_2= 235μF).

Because conventional charge pumps may suffer from current mismatch, a 10% mismatch in one phase of the *RL* load (R_b=R_c= 6Ω, L_b=L_c=10mH, and R_a= 6.6Ω, L_a=11mH) has also been considered in this paper. Experimental results under this condition are shown using the proposed PWM method in Fig. 17. Comparing i_a with i_b, (although the amplitude of i_a decreases because of 10% mismatch in Phase-a *RL* load), the final actual synthesized average pulse NP current is still suppressed well through the capacitor-voltage loop. U_{cap1} and U_{cap2} have very little difference to those under the symmetrical three-phase *RL* load as shown in Fig. 13(b).

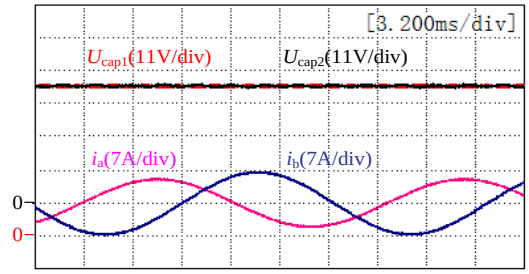


Fig. 17 Experimental results of mismatch 10% in Phase-a *RL* load using proposed PWM method (m=1, f=50Hz, R_b=R_c= 6Ω, L_b=L_c=10mH, R_a= 6.6Ω, L_a=11mH, and C_1=C_2= 470μF)

Another mismatch that may happen in the three-level NPC inverter is the capacitance imbalance between the DC-link capacitors, and it may result in the failure of the power switches due to the serious unbalanced voltage stress, as well as the distortion of the line to line voltages. In order to demonstrate the ability of fluctuation-suppression of the proposed PWM method, the equivalent C_2 is changed from 470μF (paralleled by two capacitors with capacitance 235μF) to 235μF (removing one of the two capacitors). By adjusting the final modulation wave at each switching period, the capacitor voltages U_{cap1} and U_{cap2} fluctuate only a little more as shown in Fig. 18, and the line to line voltage u_{ab} is not influenced significantly. Therefore, the proposed method can tolerate the imbalance capacitance (at least 50%) of the series connected DC-link capacitors, due to the capacitor-voltage loop.

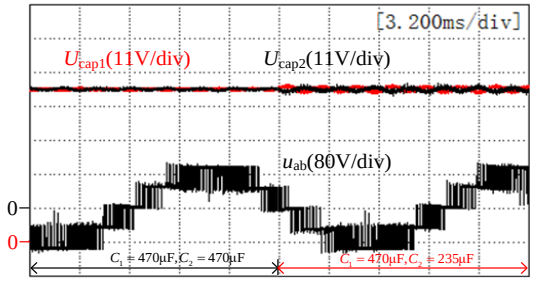
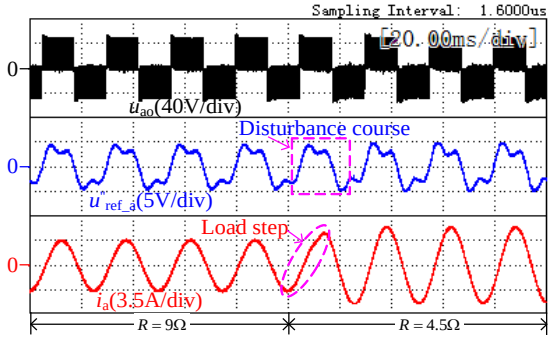


Fig. 18 Experimental results of capacitance imbalance between DC-link capacitors using proposed PWM method (m=1, f=50Hz, $\cos\varphi = 0.886$, $R = 6\Omega$, L=10mH, C_1= 470μF, and equivalent C_2 is changed from 470μF to 235μF).

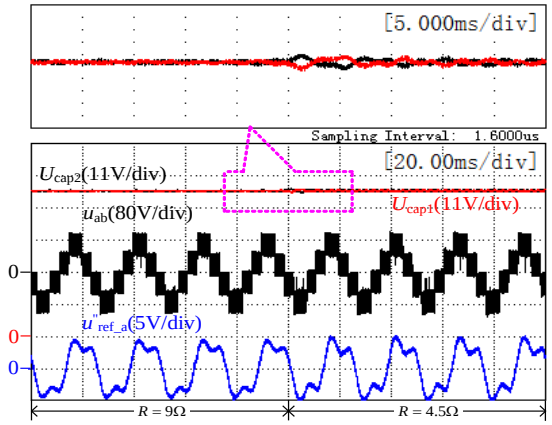
When a symmetric three-phase load step change happens from $R = 9\Omega$ to 4.5Ω, the experiment results are shown in Fig. 19. With the proposed method, i_a and the fluctuation of U_{cap1} and U_{cap2} increase, as shown in Fig. 19(a, b) respectively. However, the final modulation wave u''_{ref_a} is modified through the capacitor-voltage loop with the quasi PR controller, and its amplitude also increases properly as shown in Fig. 19(a) and therefore the fluctuation of U_{cap1} and U_{cap2} can also be controlled well as shown in Fig. 19(b).

Under the same conditions, Fig. 19(c) shows the load step change experiment results with the basic carrier-based PD PWM method. It is seen that the fluctuation of U_{cap1} and U_{cap2} is still much larger than the one in Fig. 19(b). After the step change in load resistance, the phase current increases and the load power factor reduces. Comparing Fig. 19(b) with Fig. 19(c), the

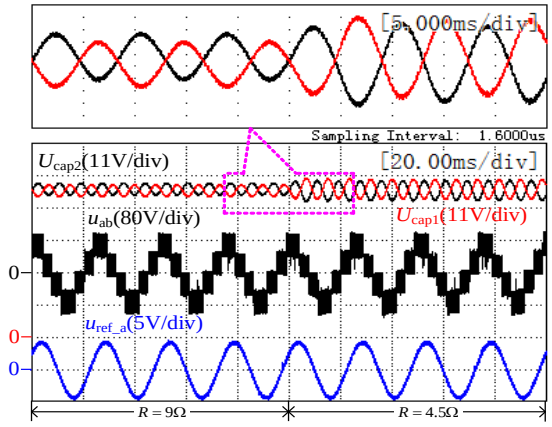
fluctuation using the proposed method is virtually immune to the disturbance factors, but the basic method is very oscillatory.



(a) Phase current (bottom), final modulation wave (middle), and phase voltage (upper) in Phase-a using proposed PWM method



(b) Final modulation wave in Phase-a (bottom), line to line voltage (middle) and capacitor voltages (upper) using proposed PWM method



(c) Final modulation wave in Phase-a (bottom), line to line voltage (middle) and capacitor voltages (upper) using basic PWM method

Fig. 19 Experimental results of symmetric three-phase load step change from $R = 9\Omega$ to 4.5Ω (m=0.733, f=40Hz, L=20mH and C_1=C_2= 470μF).

V. Conclusion

This paper introduces a new method for the suppression of fluctuations in the NPP of a three-level NPC inverter using the capacitor-voltage loop. Due to the constant initial phase of the injected zero sequence, the saddle wave modulation method has limited capability to suppress the fluctuation of the NPP. The essence of the NPP fluctuation can be revealed by the average pulse NP current: the fluctuation frequency is three times the fundamental; the fluctuation amplitude is mainly determined by the modulation index, the phase current and load power factor; the equivalent initial phase of the NPP fluctuation is related to the load power factor.

Reducing the amplitude of the average pulse NP current is an efficient way to suppress the NPP fluctuation. Under VVVF control mode, the controlled variable, which varies with the disturbance factors, (i.e. modulation index, phase current, load power factor, etc) can be produced properly by a quasi PR controller in the capacitor-voltage loop. The final three-phase modulation waves are obtained by virtue of the controlled variable. The reduction in amplitude of the average pulse NP current is carried out through the proposed phase pulse width duty cycle disturbance PWM. Experimental results demonstrate that under the VVVF control mode, the proposed method not only suppresses the NPP fluctuation efficiently, but also avoids the overlapping of the level layers in the line to line voltages, reduces the switching actions (in high modulation indices), and tolerates the imbalance capacitance (at least 50%) of the series connected DC-link capacitors. It is suitable for fan and pump applications with the induction motor.

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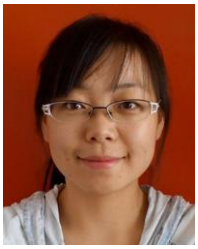

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