Open-End Winding Induction Machine Fed by a Dual-Output Indirect Matrix Converter

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***Abstract*—Open-ended winding induction machines fed from standard two-level Voltage Source Inverters (VSI) provide an attractive arrangement for AC drives. An alternative approach is to use a dual output Indirect Matrix Converter (IMC). It is well known that the IMC provides fully bidirectional power flow operation, with small input size filter requirements. Whilst a standard IMC consists of an AC-DC matrix converter input stage followed by a single VSI output stage, it is possible to replicate the VSI to produce multiple outputs. In this paper an open-end winding induction machine fed by an IMC with two output stages is presented. The IMC modulation strategy aims to reduce the common-mode voltage whilst compensating any zero sequence voltage fed to the machine. The system is modeled using a PSIM and MATLAB/Simulink platform. Experimental results demonstrating the viability of the method are presented using a 7.5 kW prototype.**

***Index Terms*—Matrix converters, Space vector pulse width modulation, Variable speed drives.**

I. Introduction

An open-end winding induction machine fed by two 2-level VSIs, offers several advantages when compared to a standard wye or delta connected induction machine drive. The main features of an open-winding induction machine drive can be summarized as [1]-[2]:

(1) Equal power input from both sides of each winding, thus each VSI is rated at half the machine power rating.
(2) Each phase stator current can be controlled independently; possibility to have twice the effective switching frequency (depending on the modulation strategy).
(3) Extensibility to more phases, therefore multiphase induction machines can be considered if current reduction is required; possibility of reducing common-mode voltage (CMV).
(4) Certain degree of fault tolerance, as there is voltage space vector redundancy.

However, an open-ended winding induction machine drive can have some drawbacks, such as [1]: possibility of zero sequence current flowing in the machine, because of the occurrence of zero sequence voltage, and more complex power converter requirements, i.e. more power devices, circuit gate drives, etc.

In addition, the open-ended winding approach can be used in other applications such as power transformers [3] or synchronous machine drives in wind power generation systems [4].

In the recent decades, a significant research effort has been focused on direct frequency changing power converters, such as the Matrix Converter (MC) [5] or the Indirect Matrix Converter [6]. It is known that these power converter topologies offer a suitable solution for direct AC-AC conversion, achieving sinusoidal input and output currents, bidirectional power flow capability and controllable input power factor, without using bulky energy storage elements [6].

Several works have been focused on investigating the open-end winding topology based on direct matrix converters. This topology requires a total of 18 bidirectional switches (i.e. 36 IGBTs and diodes) and achieves a maximum output voltage of 1.5 times the input phase voltage as reported in [7], where the dual-matrix converter scheme is described and a modulation strategy is proposed intended to reduce the common-mode voltage at the load terminals. Experimental results are shown using open-loop V/f control strategy for an induction motor. In [8]-[9] a detailed mathematical analysis of this topology is presented. Additionally a modulation strategy aiming to reduce the CMV is studied and experimental results are shown for a passive resistive-inductive load. Moreover, the dual-matrix converter scheme has been widely studied for applications in multiphase open-end winding AC drives. For instance, in [10] a three-to-five dual matrix converter topology is studied; in this case a total of 60 power devices are required and a switching

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strategy to reduce the CMV is proposed. The system is experimentally verified with a 5kW, 5-phase induction machine. The same authors propose in [11] a similar approach for a three-to-seven dual matrix converter system (96 IGBTs and diodes required) where the modulation strategy proposed aims to eliminates the CMV and simulation results for an induction machine load are presented.

On the other hand, relatively few publications concerning the open-end winding topology based on the indirect matrix converter can be found [12]-[14]. In [13] a modulation strategy intended to reduce the CMV is presented and preliminary experimental results are shown for an R-L load. In [12] two modulation strategies are proposed for the system: a Space Vector Modulation (SVM) strategy intended to reduce the zero sequence voltage and a carrier-based modulation (SPWM) strategy that produces only high frequency zero sequence voltage components. Simulations results for a passive load are presented. In [14] a five-leg open-end winding topology based on the IMC is proposed. In this case as one leg of the output inverters must be shared by two phase windings of the load, additional constraints arise regarding the modulation strategy. Simulation results for a passive load are shown.

In this paper an experimental investigation into the application of an IMC with two output stages to supply energy to an open-ended winding induction machine is presented. The topology is depicted in Fig. 1, where the input stage, consisting of an AC-DC matrix converter, provides the DC link voltage for the two VSI output stages. The modulation strategy for the input converter is standard [15] and aims to provide the DC voltage for the output stages. The modulation strategy for the output stages uses only voltage space vectors which do not produce common-mode voltage at the machine terminals [16]. Moreover, the zero sequence voltage at the machine terminals is reduced by decreasing the average zero sequence volt-seconds within each sampling period [17]. Preliminary results with the application of this topology to an open-ended winding machine were presented in [13] and the concept is further developed and verified in this paper. The proposed approach is modeled using a PSIM/MATLAB platform and experimentally verified in a 7.5 kW rig. Simulation and experimental results are presented and discussed.

II. Dual-Output Stage Indirect Matrix Converter

Regarding the topology in Fig. 1, the modulation strategy for the rectifier aims to obtain the maximum positive DC link voltage in each sampling period. Usually, the Pulse Width Modulation (PWM) reference signal is chosen to operate the converter with unity displacement power factor at the input. The output stage of the IMC consists of two VSI. Each inverter can produce eight space voltage vector locations independent of the other, resulting in a total of 64 voltage vector combinations. The six-terminal open-end winding induction machine is connected between the VSI outputs. Considering the six bidirectional switches of the input stage and the two output stages, a total of 24 discrete IGBTs and diodes are needed in this topology.

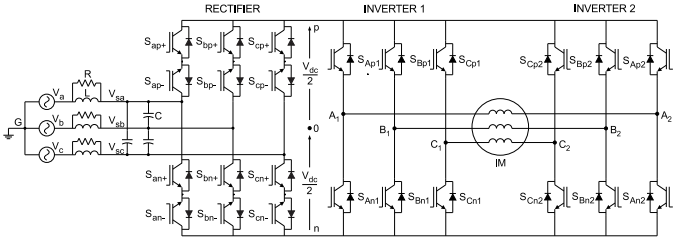


Fig. 1. IMC with two output stages feeding an open-ended winding induction machine.

III. Common-Mode Voltage

Conventional PWM inverters generate alternating common-mode voltages relative to ground which generate currents through the motor parasitic capacitances to the rotor iron [18]. These currents find their way via the motor bearings back to the grounded stator case. The so-called bearing currents have been found to be a major cause of premature bearing failure in PWM inverter motor drives [19]. One of the main advantages of the open-end winding topology is the possibility of reducing the common-mode voltage at the machine terminals and this has been the research topic of several investigators [7]-[11], [13], [20]-[24]. For the topology depicted in Fig. 1, the common-mode voltage is given by [16]:

$$v_{cm} = \frac{1}{6}(v_{A1G} + v_{B1G} + v_{C1G} + v_{A2G} + v_{B2G} + v_{C2G}) \quad (1)$$

where v_{AiG}, v_{BiG}, v_{CiG}, with $i = 1,2$, are the pole voltages of each inverter with respect to the grounded neutral point of the source (Fig. 1). These voltages can be also expressed as:

$$\begin{aligned} v_{AiG} &= S_{Api}v_{pG} + S_{Ani}v_{nG} \\ v_{BiG} &= S_{Bpi}v_{pG} + S_{Bni}v_{nG} \\ v_{CiG} &= S_{Cpi}v_{pG} + S_{Cni}v_{nG} \end{aligned} \quad (2)$$

where v_{pG} and v_{nG} are the voltages of the positive and negative rail of the DC link with respect to the grounded neutral point of the source, respectively; $S_{xpi}, S_{xni} \in \{0,1\}$ with $x = A, B, C$, $i = 1,2$ are the switching functions of the inverter devices (0: switch opened, 1: switch closed) and $S_{xni} = 1 - S_{xpi}$ (because of the complementary operation of the upper and lower switches of each inverter leg). Therefore,

$$\begin{aligned} v_{cm} = \frac{1}{6}[&(S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2})v_{pG} \\ &+(S_{An1} + S_{Bn1} + S_{Cn1} + S_{An2} + S_{Bn2} + S_{Cn2})v_{nG}] \end{aligned} \quad (3)$$

Let $N_{sw} = S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}$, thus

$$v_{cm} = \frac{1}{6}\left[N_{sw}v_{pG} + (6 - N_{sw})v_{nG}\right] \quad (4)$$

Where N_{sw} is the number of upper inverter switches closed. The squared RMS value of the common-mode voltage is:

$$v_{cm_{RMS}}^2 = \frac{1}{36T}\int_0^T \left[N_{sw}v_{pG} + (6 - N_{sw})v_{nG}\right]^2 dt \quad (5)$$

where T is the period of v_{pG} (equals the period of v_{nG}). Further expansion yields:

$$\begin{aligned} 36v_{cm_{RMS}}^2 = {} & N_{sw}^2 \frac{1}{T}\int_0^T v_{pG}^2 dt \\ & + 2N_{sw}(6 - N_{sw})\frac{1}{T}\int_0^T v_{pG}v_{nG}dt \\ & + (6 - N_{sw})^2 \frac{1}{T}\int_0^T v_{nG}^2 dt \end{aligned} \quad (6)$$

The voltages of the DC link rails are given by:

$$\begin{aligned} v_{pG} &= S_{ap}v_{ra} + S_{bp}v_{rb} + S_{cp}v_{rc} \\ v_{nG} &= S_{an}v_{ra} + S_{bn}v_{rb} + S_{cn}v_{rc} \end{aligned} \quad (7)$$

where v_{ra}, v_{rb} and v_{rc} are the converter input phase voltages and S_{xp}, S_{xn} with $x = a, b, c$ are the switching functions of the rectifier (see section IV-A). Accordingly v_{pG} and v_{nG} will always be segments of different input phase voltages and

$$\left|v_{pG}(t)\right| = \left|v_{nG}(t - t_o)\right| \ , t_o \in \mathbb{R} \quad (8)$$

thus

$$\int_0^T v_{pG}^2 dt = \int_0^T v_{nG}^2 dt \quad (9)$$

Differentiating (6) with respect to N_{sw} and equating to zero, it can be found that $v_{cm_{RMS}}^2$ (and implicitly $v_{cm_{RMS}}$) achieves a minimum value at $N_{sw} = 3$, which means that in order to reduce the RMS common-mode voltage at the machine terminals, only three upper inverter switches should be closed at each switching period.

This can be further investigated by considering a virtual midpoint of the DC link as a reference point (see point 0 in Fig. 1). Then, (1) can be rewritten as:

$$\begin{aligned} v_{cm} = {} & \frac{1}{6}(v_{A10} + v_{B10} + v_{C10} + v_{A20} + v_{B20} \\ & + v_{C20}) + v_{0G} \\ = {} & v_{cm0} + v_{0G} \end{aligned} \quad (10)$$

where the contributions of the input and output stages to the overall common-mode voltage have been separated (v_{0G} and v_{cm0}, respectively). The voltage v_{0G} is the voltage between the reference point 0 and the grounded neutral point of the source. This voltage can be calculated as:

$$\begin{aligned} v_{0G} = {} & \frac{1}{2}\left[(S_{ap} + S_{an})v_{ra} + (S_{bp} + S_{bn})v_{rb}\right. \\ & \left. + (S_{cp} + S_{cn})v_{rc}\right] \end{aligned} \quad (11)$$

It can be seen in (11) that v_{0G} depends on the modulation of the input stage, which in this work is totally defined by the duty cycles of the rectifier stage (see IV-A). Thus, v_{0G} will have a predictable and bounded value. On the other hand, the voltage v_{cm0} can be rewritten as:

$$\begin{aligned} v_{cm0} &= \frac{1}{6}\left[N_{sw}\frac{v_{DC}}{2} + (6 - N_{sw})\left(-\frac{v_{DC}}{2}\right)\right] \\ &= \frac{1}{6}[N_{sw}v_{DC} - 3v_{DC}] \end{aligned} \quad (12)$$

Therefore, it can be seen in (12) that by using $N_{sw} = 3$, the contribution of the output inverters to the common-mode voltage is eliminated [16].

IV. Modulation for the IMC with two output Stages

A. Modulation of the input (rectifier) stage

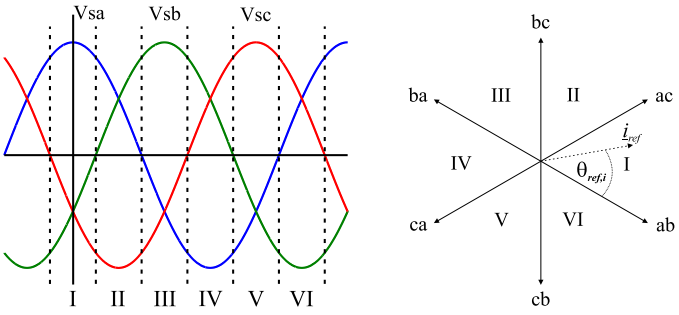
The input (rectifier) stage of the converter is modulated, using Space Vector Modulation (SVM). To obtain a maximum positive DC link voltage, commutation between the largest and second largest positive line input voltages is carried out [15]. For the modulation algorithm, a current reference vector is used and six sectors are considered as shown in Fig. 2a and 2b. The reference current vector is chosen with zero phase shift angle respect to the converter input phase voltage vector (see Fig. 2a). In this way, unity displacement power factor operation is achieved at the converter input. Fig. 2b also shows the current reference vector in the first sector with $\theta_{ref,i}$ the angle of the current vector referred to the sector.

The $\gamma - \delta$ duty cycles for the rectifier SVM are given by [15]:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \ , \ d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \quad (13)$$

with

$$d_\gamma = \sin(\pi/3 - \theta_{ref,i}) \ , \ d_\delta = \sin(\theta_{ref,i}) \quad (14)$$



(a) (b)

Fig. 2. a) Sector definition for the input rectifier and b) current vectors.

The modulation of the rectifier results in, depending on the sextant, an upper (or lower) switch closed (corresponding to the highest absolute value of the input phase voltage) and two lower (upper) switches modulated according to (13).

B. Modulation for the IMC Output Stages

For the topology depicted in Fig, 1, the aim of the modulation strategy for the output stages is to reduce v_{cm}, whilst providing the desired machine phase voltages. The voltage vectors for

inverter 1 are shown in Table I; the same space vectors are valid for inverter 2 but with superscript 2.

TABLE I. SWITCHING STATES OF THE INDIVIDUAL INVERTERS

States of inverter 1 $[S_{Ap1}\ S_{Bp1}\ S_{Cp1}]$		
$V_1^1 = [1\ 0\ 0]$	$V_2^1 = [1\ 1\ 0]$	$V_3^1 = [0\ 1\ 0]$
$V_4^1 = [0\ 1\ 1]$	$V_5^1 = [0\ 0\ 1]$	$V_6^1 = [1\ 0\ 1]$
$V_7^1 = [1\ 1\ 1]$	$V_8^1 = [0\ 0\ 0]$	

Let $V_{ij} = [V_i^1 V_j^2]$ with $i, j = 1 \dots 8$, be the phase voltage vector combination of the dual-inverter output. A representation of the vector locations is shown in Fig. 3 [16].

According to Section III, a voltage vector producing null common-mode voltage v_{cm0} should have only three upper switches closed ($N_{sw} = 3$). Considering, for instance, the dual-inverter space vector $V_{14} = [1\ 0\ 0\ 0\ 1\ 1]$, the common-mode voltage v_{cm0} generated by the output stages of the IMC is given by (10), where in this case:

$$v_{A10} = v_{B20} = v_{C20} = \frac{V_{DC}}{2} \tag{15}$$

and

$$v_{B10} = v_{C10} = v_{A20} = -\frac{V_{DC}}{2} \tag{16}$$

Therefore

$$v_{cm0} = \frac{1}{6}\left(\frac{V_{DC}}{2} - \frac{V_{DC}}{2} - \frac{V_{DC}}{2} - \frac{V_{DC}}{2} + \frac{V_{DC}}{2} + \frac{V_{DC}}{2}\right) = 0 \tag{17}$$

The same procedure can be used to verify that voltage vectors given in Table II generate zero v_{cm0} [16].

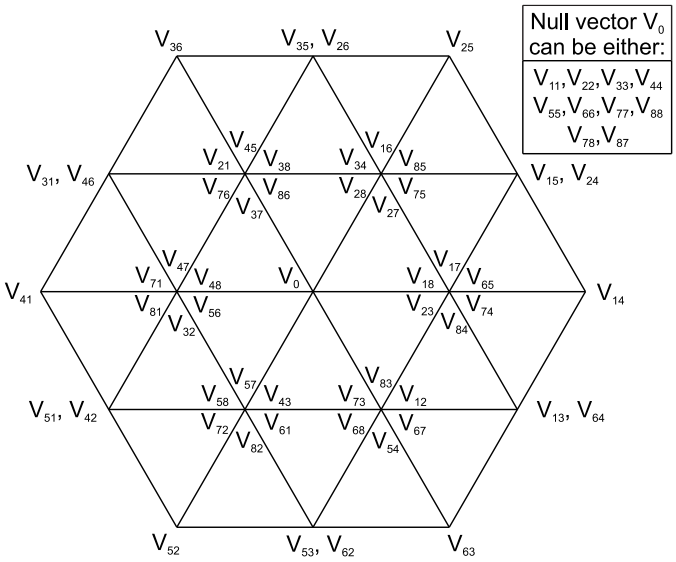


Fig. 3. Space vector locations of the dual-inverter scheme.

Hence, to eliminate v_{cm0} and maximize the output load voltage, the modulation strategy for the output inverters considers the zero voltage vectors $\{V_{78}, V_{87}\}$ and the largest active voltage vectors $\{V_{14}, V_{25}, V_{36}, V_{41}, V_{52}, V_{63}\}$ (see Fig. 3). Note that it is possible to use all of the active vectors given in Table II (rather than just the largest ones), but this complicates the algorithm and the benefits in terms of current/voltage Total Harmonic Distortion (THD) are not significant (less than 2% according to simulations).

TABLE II. SPACE VECTORS WITH ZERO COMMON-MODE VOLTAGE CONTRIBUTION

Space vector combinations $[S_{Ap1}\ S_{Bp1}\ S_{Cp1}\ S_{Ap2}\ S_{Bp2}\ S_{Cp2}]$	
$V_{14} = [1\ 0\ 0\ 0\ 1\ 1]$	$V_{56} = [0\ 0\ 1\ 1\ 0\ 1]$
$V_{25} = [1\ 1\ 0\ 0\ 0\ 1]$	$V_{61} = [1\ 0\ 1\ 1\ 0\ 0]$
$V_{36} = [0\ 1\ 0\ 1\ 0\ 1]$	$V_{43} = [0\ 1\ 1\ 0\ 1\ 0]$
$V_{41} = [0\ 1\ 1\ 1\ 0\ 0]$	$V_{12} = [1\ 0\ 0\ 1\ 1\ 0]$
$V_{52} = [0\ 0\ 1\ 1\ 1\ 0]$	$V_{16} = [1\ 0\ 0\ 1\ 0\ 1]$
$V_{63} = [1\ 0\ 1\ 0\ 1\ 0]$	$V_{65} = [1\ 0\ 1\ 0\ 0\ 1]$
$V_{23} = [1\ 1\ 0\ 0\ 1\ 0]$	$V_{54} = [0\ 0\ 1\ 0\ 1\ 1]$
$V_{34} = [0\ 1\ 0\ 0\ 1\ 1]$	$V_{32} = [0\ 1\ 0\ 1\ 1\ 0]$
$V_{45} = [0\ 1\ 1\ 0\ 0\ 1]$	$V_{21} = [1\ 1\ 0\ 1\ 0\ 0]$
$V_{78} = [1\ 1\ 1\ 0\ 0\ 0]$	$V_{87} = [0\ 0\ 0\ 1\ 1\ 1]$

It can be noted that the zero vectors V_{78} and V_{87} produce an output phase voltage, which is the same in each machine winding (V_{DC} for vector V_{78} and $-V_{DC}$ for vector V_{87}). Since $\underline{V_{ij}}$ is a space vector combination of the dual-inverter, it can be represented by:

$$\underline{V_{ij}} = v_{A1A2} + v_{B1B2} e^{-j\frac{2\pi}{3}} + v_{C1C2} e^{j\frac{2\pi}{3}} \tag{18}$$

where v_{A1A2}, v_{B1B2} and v_{C1C2} are the machine phase voltages. Therefore, for vectors V_{78} and V_{87} (19) is obtained:

$$\begin{aligned} \underline{V_{78}} &= -\underline{V_{87}} = V_{DC} + V_{DC} e^{j\frac{2\pi}{3}} + V_{DC} e^{-j\frac{2\pi}{3}} \\ \underline{V_{78}} &= V_{DC}\left(1 + e^{j\frac{2\pi}{3}} + e^{-j\frac{2\pi}{3}}\right) = 0 \end{aligned} \tag{19}$$

It is verified that the magnitude of these voltage vectors is zero, hence they are effectively zero vectors of the dual-inverter system.The duty cycles for each of the output stages are calculated as:

$$d_\alpha = m(t)\sin\left({}^{\pi}/_{3} - \theta_{ref,o}\right) \tag{20}$$

$$d_\beta = m(t)\sin\left(\theta_{ref,o}\right) \tag{21}$$

$$d_0 = 1 - d_\alpha - d_\beta \tag{22}$$

where $m(t)$ is a variable modulation index given by $m(t) = m_o\left(d_\gamma + d_\delta\right)$. The factor $\left(d_\gamma + d_\delta\right)$ is included to compensate the fluctuations of the DC link voltage; m_o is the standard modulation index ($0 \le m_o \le 1$) and $\theta_{ref,o}$ is the angle of the output reference voltage space vector.

To obtain a correct balance of the input currents and the output voltages in a switching period, the modulation pattern should produce all combinations of the rectification and the

inversion switching states [15], resulting in the following duty cycles for the active vectors:

$$d_{\alpha\gamma} = d_\alpha d_\gamma^R \ , \ d_{\beta\gamma} = d_\beta d_\gamma^R$$
$$d_{\alpha\delta} = d_\alpha d_\delta^R \ , \ d_{\beta\delta} = d_\beta d_\delta^R \quad (23)$$

The total zero vector duty cycle is:

$$d_0 = 1 - d_\alpha - d_\beta \quad (24)$$

and the combined zero vector duty cycles are:

$$d_{0\gamma} = d_0 d_\gamma^R \ , \ d_{0\delta} = d_0 d_\delta^R \quad (25)$$

C. Voltage gain of the converter

It has been shown that the input rectifier uses an SVM strategy to maximize the DC link voltage. However, the average value of the DC link voltage, in every switching period, varies between a minimum $V_{pn,min} = \frac{\sqrt{3}}{2}\hat{V}_{s,l-l}$ and a maximum $V_{pn,max} = \hat{V}_{s,l-l}$, where $\hat{V}_{s,l-l}$ is the peak value of the input line voltage. The output voltage vector locus considering the average DC link voltage is shown in Fig. 4.
Therefore, the voltage produced by the output stages is limited by the minimum average DC link voltage (red circle in Fig. 4). As each machine phase winding can be considered to be supplied by an H-bridge, the amplitude of the fundamental output phase voltage is given by [25]:

$$\hat{V}_{o,ph} = m_o V_{pn,min} = m_o \frac{\sqrt{3}}{2}\hat{V}_{s,l-l} \quad (26)$$

where m_o is a modulation index for the output inverters ($0 \leq m_o \leq 1$). Since the input phase voltage equals $\sqrt{3}$ times the input line voltage, eq. (26) can be rewritten as:

$$\hat{V}_{o,ph} = m_o \frac{\sqrt{3}}{2}\sqrt{3}\hat{V}_{s,ph} = 1.5 m_o \hat{V}_{s,ph} \quad (27)$$

Hence, with the proposed topology (see Fig. 1), the maximum output phase voltage without over-modulation is 1.5 times the input phase voltage.

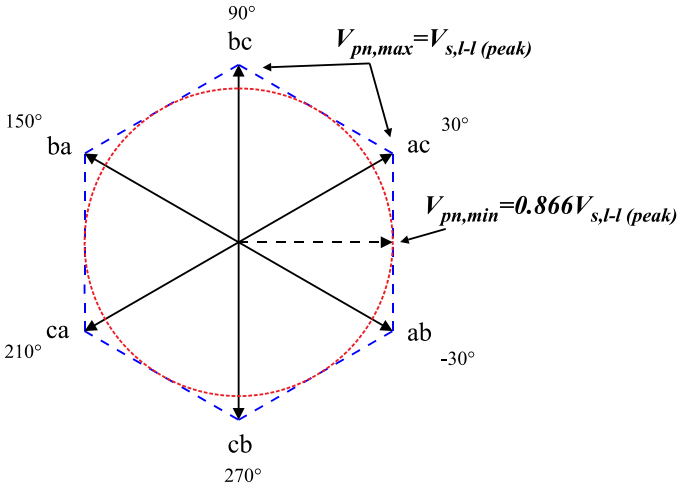


Fig. 4. Output voltage vector locus for the average DC link voltage.

V. Zero Sequence Voltage

As mentioned before, the dual-inverter fed open-ended winding induction motor drive may suffer from zero sequence current caused by zero sequence voltage. This zero sequence voltage is produced because of the asymmetry of the instantaneous phase voltages applied to the machine windings (due to the voltage space vectors used). In general, zero sequence currents may give rise to increased RMS phase current, thus increasing the system losses; high current/voltage THD and machine over-heating and vibrations. The zero sequence voltage is given by [17]:

$$v_{zs} = \frac{v_{A1A2} + v_{B1B2} + v_{C1C2}}{3} \quad (28)$$

The zero sequence voltage contributions from the 64 space vector combinations are shown in Table III. As can be noted from Table II and Table III, the vectors that do not produce common-mode voltage are not the same vectors that do not produce zero sequence voltage. Hence, as the vectors used to modulate the converter output stages will eliminate common-mode voltage (section IV-B), compensation must be performed to avoid the circulation of zero sequence current in the machine.

The average zero sequence voltage within a sampling interval can be eliminated by forcing the zero sequence volt-seconds to zero [17] by applying the null voltage vectors with unequal times. Accordingly, the standard switching sequence used in the IMC [15] is modified (see Fig. 5) in order to reduce/eliminate the average zero sequence voltage within a sampling period. For the modulation strategy presented, the duty cycles for both output VSIs are the same, which can be noted in Fig. 5.

TABLE III. Zero Sequence Voltage Contributions from Different Space Vector Combinations

V_{zs}	Voltage vector combinations
$-V_{DC}/2$	V_{87}
$-V_{DC}/3$	$V_{84}, V_{86}, V_{82}, V_{57}, V_{37}, V_{17}$
$-V_{DC}/6$	$V_{85}, V_{83}, V_{54}, V_{34}, V_{81}, V_{56}, V_{52}, V_{36}$ $V_{32}, V_{47}, V_{14}, V_{16}, V_{12}, V_{67}, V_{27}$
0	$V_{88}, V_{55}, V_{53}, V_{35}, V_{33}, V_{44}, V_{51}, V_{31}, V_{46}, V_{42}$ $V_{15}, V_{13}, V_{64}, V_{24}, V_{11}, V_{66}, V_{62}, V_{26}, V_{22}, V_{77}$
$+V_{DC}/6$	$V_{58}, V_{38}, V_{45}, V_{43}, V_{18}, V_{65}, V_{25}, V_{63}$ $V_{23}, V_{74}, V_{41}, V_{61}, V_{21}, V_{76}, V_{72}$
$+V_{DC}/3$	$V_{48}, V_{68}, V_{82}, V_{75}, V_{73}, V_{71}$
$+V_{DC}/2$	V_{78}

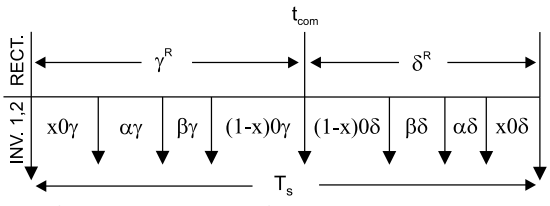


Fig. 5. Modified switching sequence for the IMC with two outputs.

Taking into account that the same space vector sequence applied in the γ^R interval is applied in the δ^R interval but in reverse order, then the value of x, which causes the cancellation

of the zero sequence volt-seconds, is calculated at every sampling period to satisfy [17]:

$$v_{zs1}x(0\gamma+0\delta)+v_{zs2}(\alpha\gamma+\alpha\delta)+v_{zs3}(\beta\gamma+\beta\delta)+v_{zs4}(1-x)(0\gamma+0\delta)=0 \quad (29)$$

where v_{zsk} with $k=1,2,3,4$, is the zero sequence voltage value at intervals $x0\gamma$, $\alpha\gamma$, $\beta\gamma$ and $(1-x)0\gamma$, respectively.

Solving (29) (considering the space vectors used), it can be found that x is given by:

$$x=\frac{1}{2}+\frac{d_{\beta\gamma}+d_{\beta\delta}-d_{\alpha\gamma}-d_{\alpha\delta}}{6\left(d_{0\gamma}+d_{0\delta}\right)} \quad (30)$$

VI. Simulation Results

The system has been modeled and simulated using PSIM. The results obtained in PSIM are then plotted and analyzed in the MATLAB environment. The simulation data (which is the practically the same as the experimental rig), is given in Table IV. A 20Hz digital synchronous filter is used for filtering the capacitor voltages signal [26]. An open loop *V/f* strategy was used to control the machine. For simulation purposes, the load used is a constant torque, set to 35 Nm. As the machine rated phase voltage is 220 V and the converter voltage gain is 1.5, see (27), the input phase voltage was set to 130 V, in order to not exceed the machine ratings ($V_{o,ph\,max}=1.5\cdot 130\sim 200\,V$ without overmodulation). Further information about the machine parameters can be found in the Appendix.

TABLE IV. Simulation/Experimental Parameters

Variable	Description	Value
P_m	Machine power	7.5 kW
$V_{m,ph}$	Machine phase voltage	220 V
V_s	Input phase voltage	130 V
L_s	Supply inductance	0.1 mH
f	Input voltage frequency	50 Hz
f_s	Switching frequency	12 kHz
C	Input filter capacitance	2 µF
L	Input filter inductance	0.5 mH
R	Input filter resistance	100 Ω

The DC link voltage and phase-a machine voltage are shown in Fig. 6, top and bottom, respectively. The reference output voltage and frequency were set to 150 V and 50 Hz respectively.

The machine currents for 25 Hz operation are shown in Fig. 7 (top), while Fig. 7 (bottom) shows machine currents for 50 Hz operation.

Small disturbances, occurring every 60°, can be noted in the motor currents shown in Fig. 7. These current disturbances are due to the application of zero voltage vectors to machine windings, see PWM pattern in Fig. 5, aiming to reduce the zero sequence voltage.

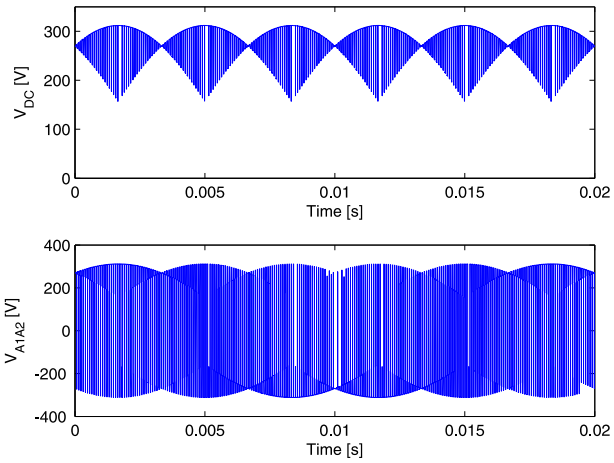


Fig. 6. DC link voltage (top) and output phase voltage (bottom).

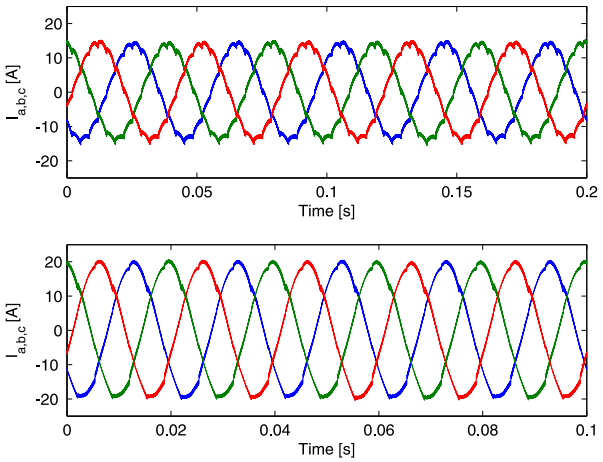


Fig. 7. Machine currents for 25 Hz output (top) and 50 Hz output (bottom).

During the application of zero voltage vectors each machine phase winding is supplied with a voltage of $-V_{DC}$ or $+V_{DC}$. When $-V_{DC}$ voltage is applied to the machine windings the current decreases according to the zero vector duty cycle. Fig. 8 shows the current disturbance along with the corresponding DC link voltage and output phase voltage.

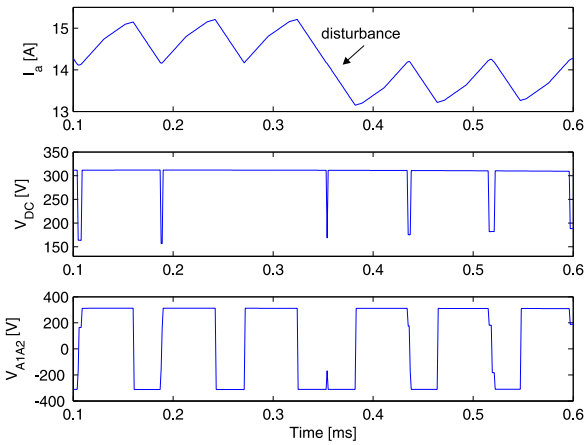


Fig. 8. Phase a machine current (top), DC link voltage (middle) and machine phase-a voltage (bottom).

The low order harmonics of the machine currents are presented in Table V.

TABLE V. HARMONIC CONTENT OF THE MACHINE CURRENTS

	25 Hz	50 Hz
Harmonic	**RMS Value [A]**	**RMS Value [A]**
Fundamental	10.5	14.490
2nd	0.011	0.130
3rd	0.107	0.105
4th	0.008	0.037
5th	0.005	0.034
6th	0.022	0.217

The input (supply) currents are shown in Fig. 9 (top) while Fig. 9 (bottom) shows the converter input phase voltage (blue) and current (green) for an output reference of 150 V and 50 Hz. Operation at unity displacement factor is evident in Fig. 9 (bottom). The notches present in the voltage and current waveforms, occurring every 60°, are due to the output current disturbances reflected on the input converter voltage and current, further attenuated because of the input filter.

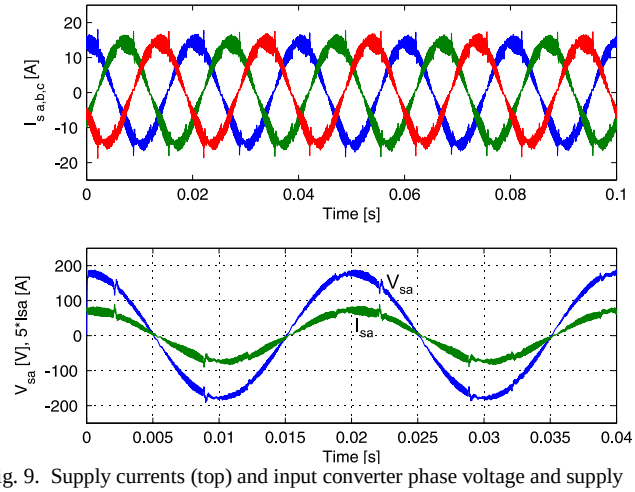


Fig. 9. Supply currents (top) and input converter phase voltage and supply current (bottom).

Fig. 10 shows the common-mode voltage separated into v_{0G} and v_{cm0} as defined in (10). Due to absence of the reference point 0 in the real (and also simulated) converter, the common-mode voltages v_{0G} and v_{cm0} shown in Fig. 10 top and bottom, respectively, are obtained as:

$$v_{0G} = v_{nG} + \frac{v_{DC}}{2}$$
$$v_{cm0} = \frac{1}{6}(v_{A1n} + v_{B1n} + v_{C1n} + v_{A2n} + v_{B2n} + v_{C2n}) - \frac{v_{DC}}{2} \quad (31)$$

where n is the negative rail of the DC link. It can be seen in the simulation results that the contribution of the output inverters to the common-mode voltage is completely eliminated due to the modulation strategy used.

Fig. 11 shows the zero sequence voltage (top) and its frequency spectrum (bottom). This voltage has been obtained measuring all the three machine phase voltages and then applying (28). It can be noted that the low order zero sequence harmonics are reduced because of the asymmetry of the null vector duty cycles used in the switching sequence for each output stage.

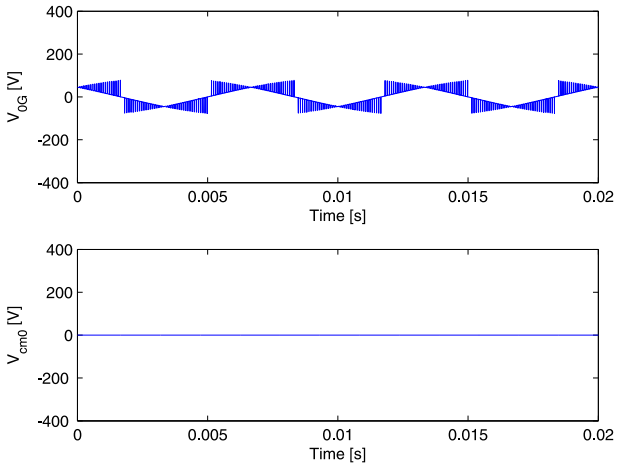


Fig. 10. Common-mode voltages v_{0G} (top) and v_{cm0} (bottom).

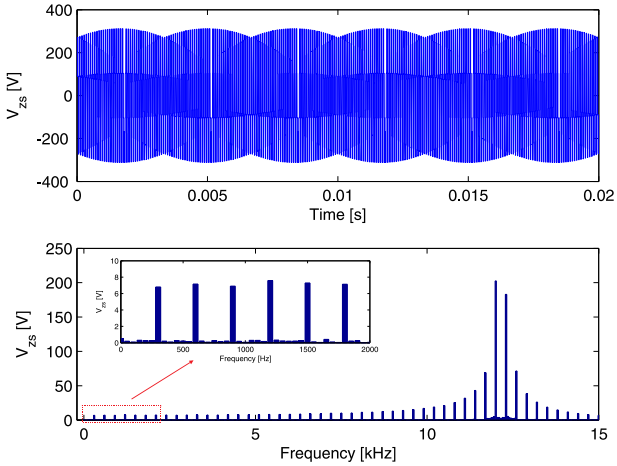


Fig. 11. Zero sequence voltage (top) and its frequency spectrum (bottom).

VII. EXPERIMENTAL RESULTS

The proposed strategy has been tested using the experimental system shown in Fig. 12. The IMC has been designed and built at the University of Nottingham Power Electronics, Machines and Control lab facilities. A six-pole induction machine rated at 7.5 kW is used. A DSP board, based on the TMS320C6713 processor, is used as the control platform. The calculation of duty cycles is carried out on the DSP among several other tasks. An FPGA interface board, designed at Nottingham University, is used to implement the modulation strategies and data acquisition. Communication between the DSP and a PC is achieved using a DSK6713HPI (Host Port Interface) daughter card. The converter input stage uses SK60GM123 modules and the output stages use SK35GD126 modules. The switching frequency is 12 kHz and voltages and currents are also sampled

at 12 kHz. A four-step commutation strategy is used based on the input converter voltage sign [27].

The voltages and currents have been measured using the Yokowaga DL850 ScopeCorder, using four two channel, 12 bit, high speed 100Ms/s modules for voltage measurements and two 12 bit, two channel, 10Ms/s modules for current measurements. The load used in the experimental system is a DC generator, coupled to the induction motor shaft, supplying a resistive load.

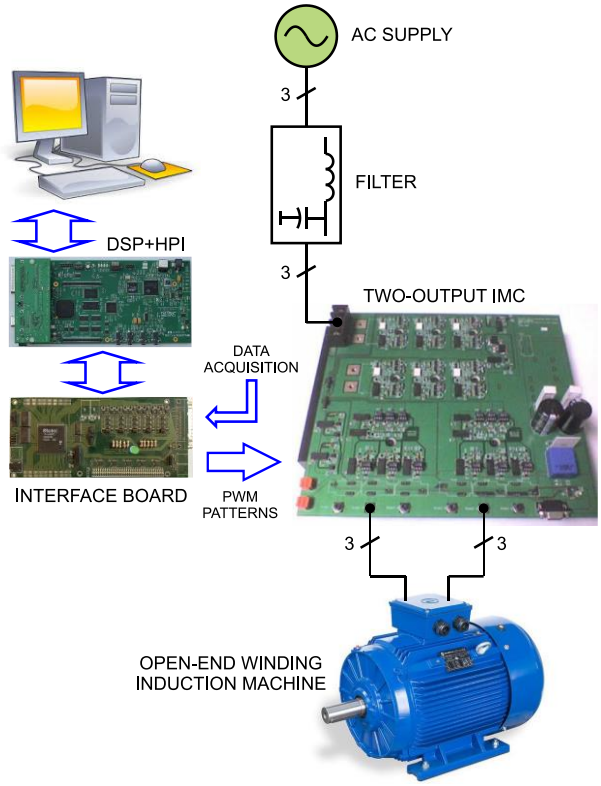


Fig. 12. Experimental setup.

Fig. 13 (top) shows the DC link voltage while Fig. 13 (bottom) shows the voltage across the machine phase-a winding. The output phase voltage presents a fundamental component of 141 V, 50 Hz, slightly less than the voltage reference (150 V). This voltage difference is attributed to the voltage drops of the power devices. According to the datasheets of the power modules used in the converter, the voltage drop in the IGBTs and the diodes can be modeled as:

$$V_{drop} = rI + V_{th}$$

where r is the slope of the device voltage-current curve, I is the circulating current in the device and V_{th} is the device voltage drop for almost zero current. A summary of the V_{th} values (extracted from the corresponding datasheets) is shown in Table VI. Further details about the power modules of the converter can be found in the Appendix.

TABLE VI. THRESHOLD VOLTAGES OF THE POWER DEVICES

	$V_{th,IGBT}$	$V_{th,diode}$
Rectifier	1.5 V	1.0 V
Inverter	0.8 V	1.0 V

Therefore, as in each conduction period there are two IGBTs plus two diodes of the rectifier conducting and two IGBTs or two diodes of the inverter conducting, the overall voltage drop will be at least (for almost zero current):

$$V_{drop,tot} \approx 2\left(V_{th,IGBT_{rect}} + V_{th,diode_{rect}}\right) + 2V_{th,IGBT_{inv}}$$
$$= 2(1.5 + 1) + 2 \cdot 0.8 = 6.6\ V$$

As can be seen the modulation strategy used results in a bipolar pulse width modulated voltage at the converter output. Good correspondence between the simulation and experimental result can be observed.

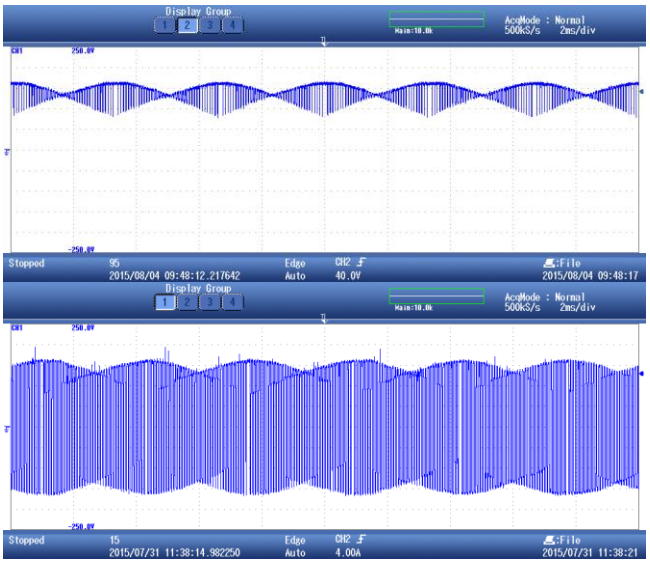


Fig. 13. DC link voltage (top) and output phase voltage (bottom). Scale 100V/div.

The machine currents for 25 Hz and 50 Hz operation are shown in Fig. 14 top and bottom, respectively. The reference output voltages are set to 75 V and 150 V, respectively.

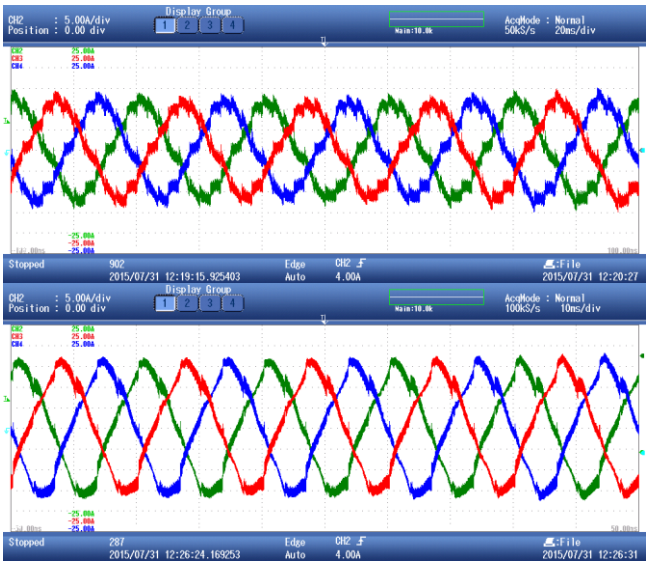


Fig. 14. Machine currents for 25 Hz output (top) and 50 Hz output (bottom). Scale 5A/div.

In Fig. 14, the effect of the zero voltage vectors in the PWM pattern shown in Fig. 5 is also observed. The supply currents

are shown in Fig. 15 (top), again with good correspondence with the simulation study. Fig. 15 (bottom) shows the input phase voltage and current.

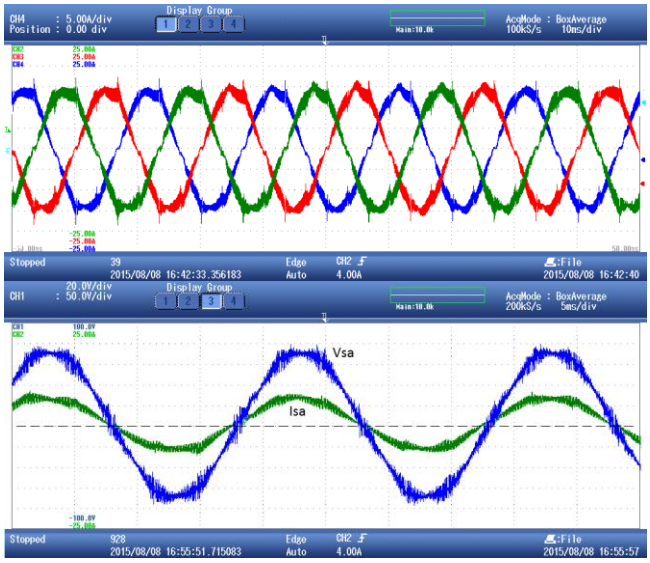


Fig. 15. Supply currents (top – Scale: 5A/div) and converter input phase voltage and supply current (bottom – Scales: 50V/div for voltage and 15A/div for current).

Fig. 16 shows the common-mode voltages v_{0G} (top) and v_{cm0} (bottom). The voltages v_{0G} and v_{cm0} are very close the simulation results shown in Fig. 10. Simultaneous measurements of six PWM machine terminal voltages and the DC link voltages, with respect to the negative pole, are needed to determine v_{0G} and v_{cm0}, hence some voltage spikes in those signal occur because not all channels are sampled exactly at the same time and because in Fig. 10 the input switches are ideal.

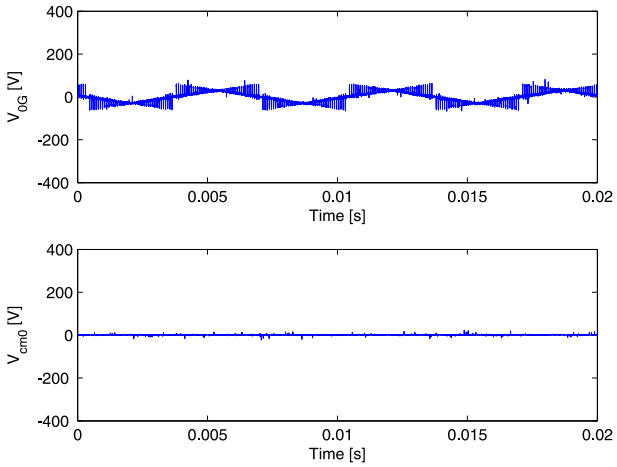


Fig. 16. Common-mode voltages v_{0G} (top) and v_{cm0} (bottom).

Finally, Fig. 17 shows the zero sequence voltage (top) and its frequency spectrum (bottom), agreeing closely with the simulation results.

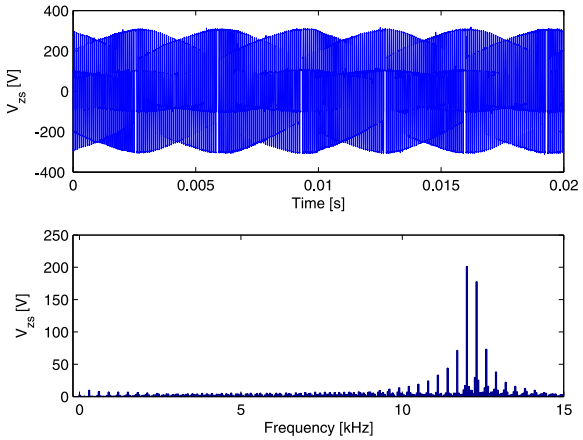


Fig. 17. Zero sequence voltage (top) and its frequency spectrum (bottom).

VIII. Converter Loss Calculations

In order to give a primary evaluation of the converter losses for the topology presented in this work and also an initial comparison with a standard IMC losses, the power losses in the converters are evaluated using the standard approach presented in [28] and applied in [29]. This method considers simulated waveform data together with power devices manufacturer's datasheet information (see the Appendix) to calculate conduction and switching losses.

The losses comparison between a standard IMC (one output stage) and the two-output IMC presented in this paper, is carried out considering a 330V, 7.5kW load with power factor equal 0.81. The converter output current for the two-output IMC is 9.3A whereas the converter output current for the standard IMC is 16.2A. The results are summarized in Table VII.

As can be noted, for the considered conditions, the dual-inverter output IMC presents similar losses to that of the standard IMC, resulting in a suitable alternative in terms of efficiency for this type of applications.

TABLE VII. Power Losses Calculation

	Two-output IMC		Standard IMC
INPUT RECTIFIER	**112.7 W**		**103.6 W**
OUTPUT INVERTERS	**INV1**	**INV2**	**191.9 W**
	95.8 W	**101.8 W**	
TOTAL LOSSES	**309.9 W**		**295.5 W**

IX. Conclusion

A modulation strategy for a two-output IMC feeding an open-ended winding induction machine has been shown. The strategy has been modeled and experimentally verified in a prototype rig. The strategy reduces the common-mode voltage and dynamically compensates the load zero sequence voltage in order to avoid the occurrence of low frequency zero sequence current in the load. For the proposed topology, the maximum output phase voltage it is possible to obtain without overmodulation is 1.5 times the input phase voltage. A preliminary converter power loss evaluation has shown that the topology has similar efficiency compared with standard Indirect Matrix Converter.

APPENDIX

Machine parameters (referred to stator): $R_s = 0.45\ \Omega$, $R_r = 0.54\ \Omega$, $L_o = 0.0818\ H$, $L_s = 0.0854\ H$, $L_r = 0.0860\ H$, six poles, stator phase voltage 220 V.

Rectifier power module: SK60GM123

Parameters: $E_{on} = 7.0\ mJ$, $E_{off} = 5.2\ mJ$, $E_{rr} = 2.4\ mJ$, $r_{IGBT} = 0.0313\ \Omega$, $r_{diode} = 0.0150\ \Omega$.

Inverters power module: SK35GD126

Parameters: $E_{on} = 4.6\ mJ$, $E_{off} = 4.3\ mJ$, $E_{rr} = 2.9\ mJ$, $r_{IGBT} = 0.0320\ \Omega$, $r_{diode} = 0.0163\ \Omega$.

Junction temperature considered for both the rectifier and the inverter: 125°C. Gate-emitter voltage considered for the IGBTs: 15V

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