SiC power MOSFETs performance, robustness and technology maturity

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Abstract: Relatively recently, SiC power MOSFETs have transitioned from being a research exercise to becoming an industrial reality. The potential benefits that can be drawn from this technology in the electrical energy conversion domain have been amply discussed and partly demonstrated. Before their widespread use in the field, the transistors need to be thoroughly investigated and later validated for robustness and longer term stability and reliability. This paper proposes a review of commercial SiC power MOSFETs state-of-the-art characteristics and discusses trends and needs for further technology improvements, as well as device design and engineering advancements to meet the increasing demands of power electronics.

List of symbols

d	device thickness [cm]	R_θ	thermal resistance [K W^{-1}]
$D_{n,p}$	diffusion coefficients [cm$_2$ s^{-1}]	V	electrostatic potential [V]
$\vec{E}$	electric field [V cm^{-1}]	V_{BR}	breakdown voltage [V]
Ec	critical electric field value [V cm^{-1}]	V_{DS}	drain-source voltage [V]
E_g	energy bandgap [eV]	V_{GS}	gate-source voltage [V]
H	heat dissipation rate [W cm^{-3}]	T_{CASE}	case temperature [ºC]
$\vec{J}$	current density [A cm^{-2}]		
J_{LEAK}	leakage current amplitude [A cm^{-2}]	α_T	current temperature coefficient [A K^{-1}]
n,p	electron, hole density [cm^{-3}]	ε_r	relative dielectric constant [-]
n_i	intrinsic carrier concentration [cm^{-3}]	λ_θ	thermal conductivity [W cm^{-1} K^{-1}]
P_D	power density [W cm^{-3}]	$\mu_{n,p}$	electron, hole mobility [cm^2 V^{-1} s^{-1}]
q	electronic charge [C]	Z_θ	thermal impedance [K W^{-1}]
R_S	specific resistance [Ω]		

1. Solid-state devices in power electronics

Switches used in electrical energy conversion are primarily expected to enable transfer of energy between a source and a load, allowing for conversion of the electrical characteristics (e.g., voltage and current levels), with minimum energy losses in the process. Ideally, one would want devices featuring infinite current conduction capability with zero on-state voltage (i.e., conductor-like behaviour), infinite blocking voltage capability with zero off-state current flow (i.e., isolator-like behaviour) and instantaneous non-dissipative transitions between the on and off states. Semiconductor components enable approximating these behavioural features to a reasonable extent and with a considerable degree of design flexibility. However, in practice, the design of solid-state devices is necessarily characterised by trade-offs between on-state, switching and blocking performance. How closely a power device approximates an ideal switch is a very important figure of merit, key in the competition among manufacturers: indeed, the ability to conjunctly improve the above

mentioned characteristics yields not only better efficiency and reduced stresses, but also, and probably more importantly, it enables to significantly decrease the size and weight of power converters by reducing electro-magnetic filters and heat-sink sizes, which is of paramount strategic value in a broad range of application domains.

1.1 Design for nominal function

Eq. (1) is most commonly used to describe the on-state behaviour of a semiconductor device (see [1-3], for example). A more detailed description also accounts for current components associated with temperature gradients (*Seebeck* effect) [4], but it is beyond scope in this context.

$$\vec{J} = q\mu_n n \cdot \vec{\nabla}V + qD_n \cdot \vec{\nabla}n + q\mu_p p \cdot \vec{\nabla}V - qD_p \cdot \vec{\nabla}p \quad (1)$$

The on-state current is the sum of drift and diffusion components, due to flow of both electron and holes, driven by gradients within the semiconductor crystal of the electro-static potential and the charge-carriers' density, respectively. More typically, devices are designed to make primarily use of drift current components of one charge carrier type and diffusion of the other type. So, for simplicity, in the following, reference is made to electron (n) drift currents and hole (p) diffusion currents. In a first approximation [4], the density of power dissipated during the on-state conduction (i.e., the heat generation rate) can be described as

$$\vec{J} \cdot \vec{E} = H = P_D \quad (2)$$

and is thus essentially related to the drift current components, the factors multiplying the voltage gradient in (1) being equivalent to a specific electrical resistance

$$\frac{1}{q\mu_n n} \cdot d = R_S \quad (3)$$

So, to optimise on-state performance, relatively high doping levels and relatively large diffusion current components are desirable, with as thin as possible devices.

However, for a given material, the maximum doping level is typically dictated by the concurrent requirement for voltage withstand capability, the device breakdown voltage being inversely proportional to the carriers' concentration as

$$V_{BD} \propto \frac{\varepsilon_r}{2qn} \cdot E_C \quad (4)$$

Minimum crystal thickness is in general limited by the need to contain the depletion region extension, which increases with blocking voltage capability as

$$W_D \propto \sqrt{\frac{2\varepsilon_r}{qn} V_{BD}} \quad (5)$$

Also, the leakage current in a power device increases with both reverse bias voltage and intrinsic carrier concentration, the latter being a function of both temperature and energy band-gap [2, 3], as

$$J_{LEAK} \propto \sqrt{V_{RB}} \cdot n_i \quad (6)$$

Finally, diffusion currents require charge accumulation within the semiconductor crystal, which typically impairs the device switching performance.

Table I: selected material properties of Si and SiC

	E_C [MV/cm]	n_i (300 K) [cm^{-3}]	Eg [eV]	λ_θ [W/cm K]
Si	0.3	$1.45 \cdot 10^{10}$	1.12	1.5
SiC	2.0	$8.2 \cdot 10^{-9}$	3.26	4.5

1.2 Temperature considerations

Power devices operation is intrinsically characterised by heat generation and self-heating phenomena (see Eq. (2)). In the steady-state, the resulting change in device operational temperature is related to the power dissipation by

$$\Delta T = P_D \cdot R_\theta \quad (7)$$

with

$$R_\theta \propto \frac{1}{\lambda_\theta} \cdot d \quad (8)$$

Temperature plays a major role in a number of considerations related to both the design and the theoretical performance of the devices [1-3, 5]. Indeed, the design features of a semiconductor device are conditional to its doping levels always being much higher than the intrinsic carrier concentration: when this condition is no longer met, the device loses its intended characteristics. This poses a clear limit to the device maximum operational temperature capability. Over the allowed range, the actual temperature value affects on-state (e.g., decrease of carriers' mobility), off-state (e.g., increase of leakage current) and switching performance. Finally, the value of ΔT is central in determining the device reliability and operational lifetime.

1.3 SiC versus Si

Table I summarises the values of four selected material properties for Si and SiC. The critical electrical field of SiC is about seven times higher than that of Si. In view of the preceding discussion, it is clear how this characteristic alone has the important implication of enabling a significant increase of the doping level for a given target blocking voltage capability. This, in turn, leads straightforward to a reduction of the required minimum nominal thickness for a given voltage blocking capability. The result is that SiC devices can theoretically be designed with greatly improved on-state performance than their Si

counterparts, or, conversely, devices with much smaller cross-section and higher blocking voltage than Si can be realistically designed, still with suitable on-state performance: this, notwithstanding a lower value of the carriers' mobility in SiC as compared with Si [3]. A reduction of the die cross–section goes in favour of switching performance, as it reduces the built-in capacitance. Also, with high enough doping and reduced thickness, reliance on large diffusion currents to achieve satisfactory on-state performance is less of a need and charge storage effects can be significantly reduced, with great advantages from a switching performance point of view.

Still after the values listed in Table I, the intrinsic carrier concentration in SiC is about 20 orders of magnitude lower than in Si at room temperature. This has the twofold consequence of enabling the design of devices able to operate at temperatures well in excess of the typical maximum values found in Si, as well as designing devices with much higher voltage withstand capability than in Si for a given target performance. A nearly three-fold value of energy band-gap of SiC as compared to Si contributes to the design of devices with high temperature capability, thermally stable characteristics and intrinsically robust against a number of overload conditions. For reference, the energy bandgap in Si reduces from nearly 1.1 eV at 300 K to nearly 0.9 eV at 1000 K, whereas the change is from about 3.26 eV at 300 K to 3 eV at 1000 K for SiC [3].

Finally, the higher thermal conductivity value enables a reduction of the thermal resistance of the semiconductor die, which, in principle, can be taken advantage of by increasing the achievable power density for a given ΔT (i.e., device size for given current rating, see Eq. (7)) or by reducing ΔT for a given power density value. To which extent the reduced R_θ value of the die can be taken advantage of clearly depends on its relative importance in the overall thermal resistance value of the packaged device.

To date, the main practical outcome of the above considerations has been the commercialisation of power MOSFET technology with voltage ratings of 400, 650, 900, 1200 and 1700 V, in both discrete and multi-chip module housings [6-8] and Schottky diodes with ratings of as much as 3.3 and 8 kV [9], as well as the production of bipolar device types (e.g., p-i-n diodes, thyristors) with voltage ratings well in excess of 6.5 kV commercially. At a research level, much higher voltage levels have been demonstrated for both bipolar and unipolar device technologies [10, 11] and SiC trench gate technology MOSFETs are being developed [12, 13]. In this paper, the focus is on commercial discrete transistors.

1.4 SiC power MOSFETs

Historically, the MOSFET has been one of the latest SiC transistor technologies to be distributed. Up to only a few years ago, SiC BJTs and JFETs, both normally on and normally off, were also being produced and distributed at 1200 V. However, the appearance and distribution of the MOSFET by CREE and ROHM seems to have resulted in this technology receiving most of the attention and interest of the specialist community and quickly coming to dominate the marketplace. Presently, SiC MOSFETs are being produced and partly distributed by a number of additional manufacturers, including ABB, Mitsubishi, ST Microelectronics, MicroSemi, Sumitomo, GE, Monolith Semiconductor. Bipolar devices are still being produced by GeneSiC, while JFETs can still be obtained from Infineon Technologies.

The main reasons why MOSFET technology is generally favoured for use in power conversion applications are:

- gated, non-dissipative control, which enables high switching frequencies and is potentially compatible with established IGBT gate-driver designs;

- availability of a built-in diode, which does not strictly require the use of an external component for freewheeling of inductive load currents;

- symmetrical bi-directional current conduction capability, which enables the implementation of advanced converter architectures with a lower number of devices;

- low off-state drain leakage current, with very good temperature stability;

- avalanche robustness capability, which enables the design of snubber-less converters and allows a reduction of the voltage de-rating margin in application.

A comparison between the on-state characteristics of 1200 V SiC MOSFET, BJT and normally-off JFET, shown in Fig. 1, also highlighted that, even if the MOSFET does not necessarily offer the best on-state resistance at all bias and temperature conditions, it does feature however very stable performance over temperature, in the sense that its on-state voltage drop at given current does not change significantly, in relative terms, with temperature. This aspect is very interesting since it removes, to a large extent, the distinction between nominal and worst case conditions in the design of power converters, with clear benefits

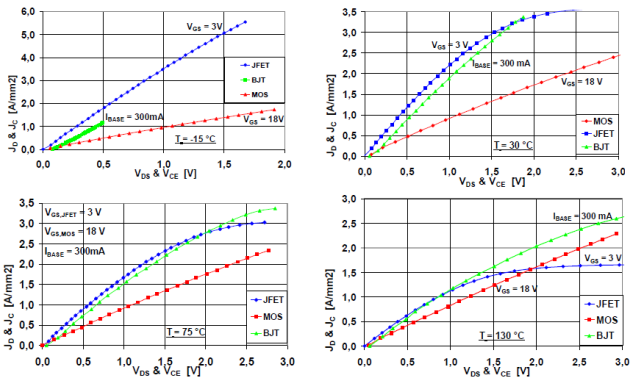
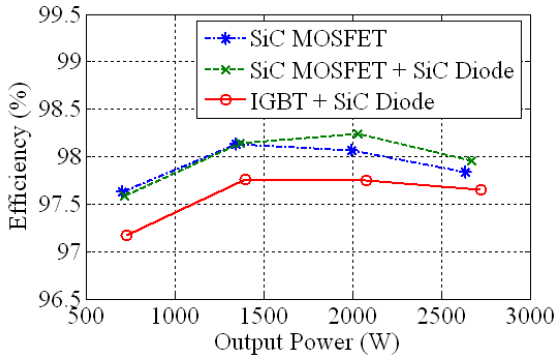


Fig. 1. Output characteristics of first generation 1200 V SiC MOSFETs, BJTs and JFETs (normally off) at four different value of ambient temperature, ranging from -15 to +130 ºC.

on the device reliability and operational lifetime, too.

2. Performance in application

Literature production on the use of SiC power MOSFETs in application is already abundant. As a case study, here the focus is on the use of both 650 V and 1200 V rated devices within a 3-level inverter topology, of common use in a range of applications including photo-voltaic, avionics, automotive, industrial. The investigations in [14] have pointed out the superior performance of SiC MOSFETs even as a drop-in replacement of Si, that is with devices using the same commercial type package (TO220 and TO247), in terms of efficiency, switching frequency capability, stability over temperature, circuit complexity and, to some extent, electro-magnetic signature. Fig. 2 shows a comparison of the efficiency at different loads that can be achieved with Si and SiC technology, at two different values of the switching frequency. 16 kHz is the reference value used in commercial applications for this topology at this power level; SiC MOSFETs enable to more than double such a value (with major impact on converter size), without any penalty on efficiency. Operation of the SiC inverter has been shown to be feasible and competitive up to four times the nominal switching frequency, that is, up to 64 kHz, which was, on the other hand, an impractical value for the Si transistors. Moreover, as evident from the results of Fig. 2, use of SiC MOSFETs does not necessarily require the use of additional SiC diodes for current free-wheeling, with important benefits on overall system complexity.



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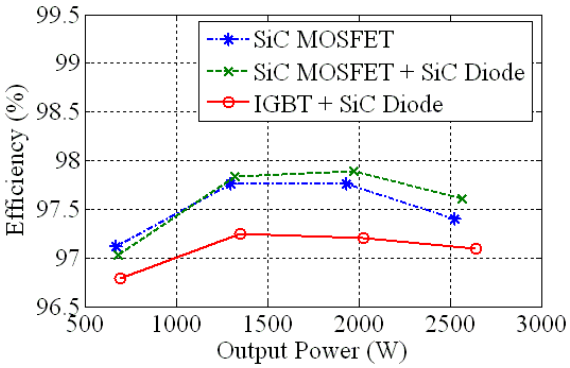
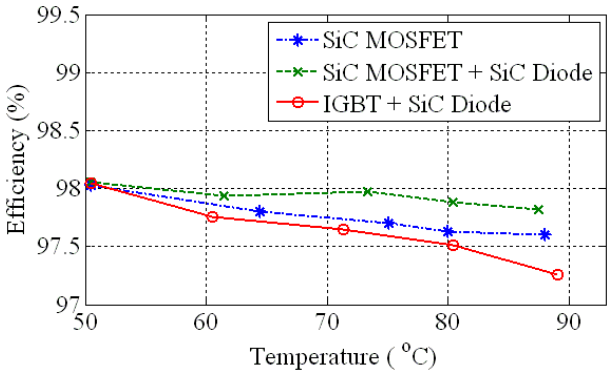


b)

Fig. 2. Comparison of Full SiC and Mixed Si/SiC inverter efficiency as a function of output load at a representative heat-sink temperature of 65°C and for two values of the switching frequency: 16 kHz (a) and 32 kHz (b).

Fig. 3 shows a comparison of the efficiency at maximum load, for different values of the heat-sink temperature, still at 16 and 32 kHz. Important to notice here is how stably SiC performs over temperature as compared with Si. This, together with the high frequency capability, is presently one of the key aspects of interest in relation to the use of such technology: extremely high temperatures (indicatively above 250 ºC) are yet limited in interest to few niche applications; however, the higher capability and stable behaviour of SiC enables for a straightforward addition to the robustness margin and to the reduction of the thermal management effort, which further contributes to higher volumetric and gravimetric power density figures.

Investigations on multi-level inverters have also pointed out the improvement in total harmonic distortion that can be derived from the faster switching of SiC MOSFETs as compared with IGBTs. Indeed, the ability to reduce the dead-time between switch commutations in a converter results in a bigger portion of the switching period being actually usable for the intended functionality, with the effect of reducing waveform distortion to the extent of making dead-time compensation techniques no longer strictly necessary in a number of applications. Fig. 4 shows a comparison of the output voltage and current waveforms of a single



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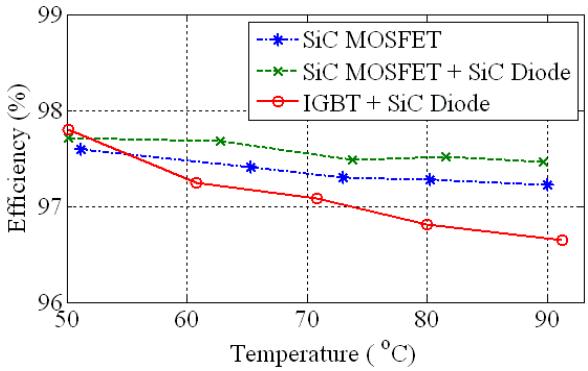

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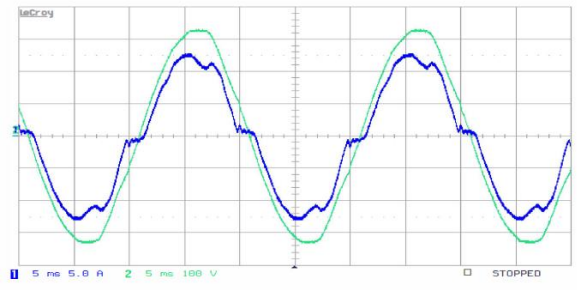
Fig. 3. Comparison of Full SiC and Mixed Si/SiC inverter efficiency as a function of temperature at a representative output power of 2.5 kW and for two different values of switching frequency: 16 kHz (a) and 32 kHz (b).



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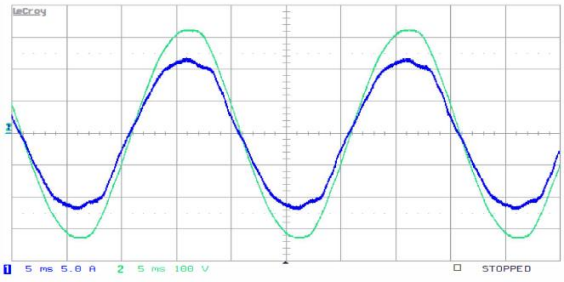

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Fig. 4. Grid voltage and current waveforms with Si IGBTs (a) and SiC MOSFETs (b) at 20kHz switching frequency (CHI: Grid current 5A/div, CH2: Grid voltage 100V/div).

phase grid-connected transformer-less inverter when using IGBTs and SiC MOSFETs, respectively, switching at 20 kHz [15]. In this case too, starting from a reference switching frequency value of 10 kHz for the Si-based commercial inverter, SiC demonstrated the ability to increase a factor 4 without any penalty, but rather with gains in efficiency, electro-magnetic performance and heat-sink temperature. Similar investigations have been carried out for other power converter topologies and have confirmed the results [16].

3. Robustness

For a new technology to access commercial markets, it needs to also comply with a number of robustness requirements. Overload conditions, though clearly not intentional operational modes, are nevertheless frequent events in a number of applications (e.g., motor drives) and semiconductor switches must be able to withstand them to some extent. The main overload robustness requirements are typically:

- overcurrent turn-off: the device must be able to withstand twice its nominal steady-state current specification at maximum specified tempearture;

- overvoltage turn-off: the margin of de-rating that needs to be taken on the maximum off-state voltage peak transient is a severe penalty for the design of a power converter; presently, the established rule in many domains is a 50% de-rating (i.e., devices rated at 3.3 kV are used up to indicatively 1.8 kV nominal bus voltage) and the devices are always protected by cumbersome *snubbers*;

- short-circuit withstand capability: typically, devices are expected to survive at least 10 µs in short-circuit, to allow for the intervention of protection circuitry. Any additional length of time that the device can survive at rated temperature and voltage is an important figure of merit, upon which part of the competition among manufacturers is played.

Overcurrent tests have demonstrated an exceptional robustness of SiC MOSFETs, even at very high switching speeds, which are known to degrade Si turn-off robustness due to the higher displacement currents within the device. Short circuit and overvoltage robustness tests are discussed in the following.

3.1 Single-pulse short-circuit robustness

Results are discussed for tests carried out on 1200 V devices at different values of drain-source bias voltage and case temperature; in all experiments the gate-source voltage amplitude was kept constant at V_{GS} =18 V. The results highlighted differences in the failure mechanism depending on the test conditions. Fig. 5 shows the short-circuit current waveforms obtained for a low bias voltage, 100 V, at a case temperature of 20 ºC. In these conditions the device is able to withstand well in excess of 10 µs, the longest pulse before failure being 160 µs: the subsequent pulse, with a width of 161 µs, led to device catastrophic failure.

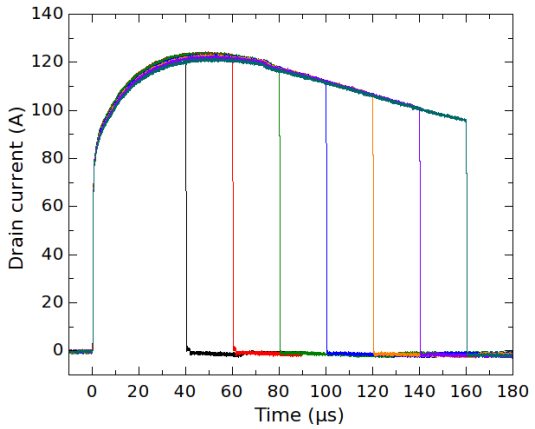


Fig. 5. Short-circuit current waveforms with V_{DS} = 100V; and T_{CASE} = 20 ºC.

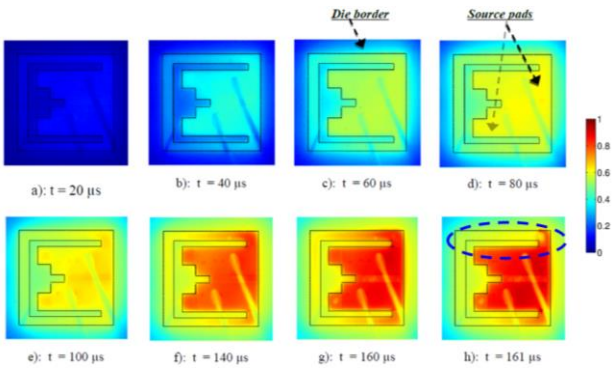


Fig. 6. Thermal maps of the chip surface corresponding to the short-circuit pulses of Fig 5. The scale is normalized to the maximum measurable temperature (ca. 500 °C).

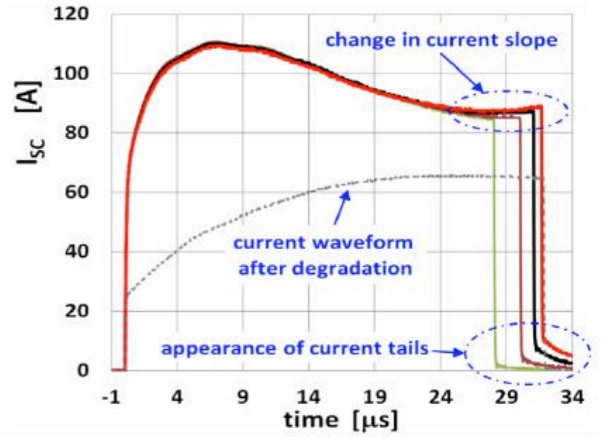


Fig. 7. Short-circuit current waveforms with V_{DS} = 400V and T_{CASE} = 90 ºC.

To assist the interpretation of the failure mechanism, advantage was taken of structural characterisation of the devices, in the form of fast transient infrared thermography of the active surface [18]. Fig. 6 shows the thermal maps corresponding to the pulsed measurements of Fig. 5. These thermal maps can be related to the current density within the device. At t = 161 µs, a portion of the device active area can be identified (circled area) which is characterised by strongly reduced current density, indicating degradation of the device integrity. This degradation was attributed to the gate-structure on the basis of the location on the chip and the estimated temperature at failure, as further discussed and referenced ahead.

The results of tests carried out at higher bias voltage (400 V) and temperature (90 ºC), reveal some interesting differences. In this case, as shown in Fig. 7, the maximum withstand capability is reduced to about 30 µs and the device features some very clear precursor of failure, in the form of a change in current slope and turn-off current tails. The last two pulses in Fig. 7 are both 32 µs long: the very last one (dashed line in Fig. 7), indicates an important reduction of the current rating of the device, compatible with the degradation mechanism put forward previously, that is, degradation of the gate structure leading to reduction of the effective active area. The temperature estimated under these power dissipation conditions was also compatible with this interpretation [19], which also found

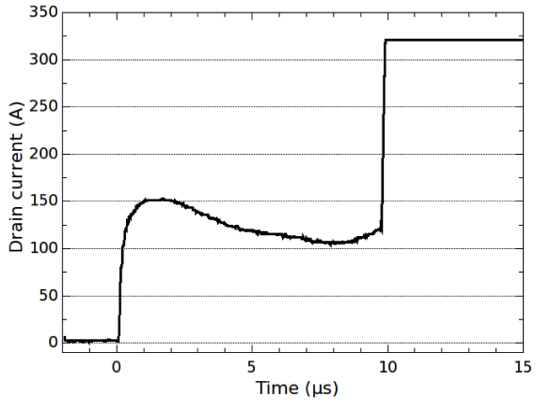
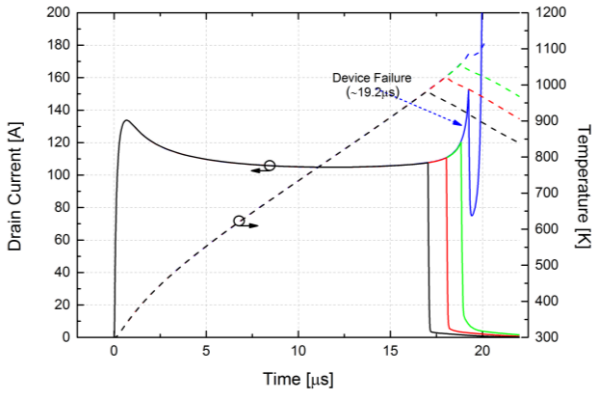


Fig. 8. Short-circuit current waveforms with V_{DS} = 800V and T_{CASE} = 150 ºC.



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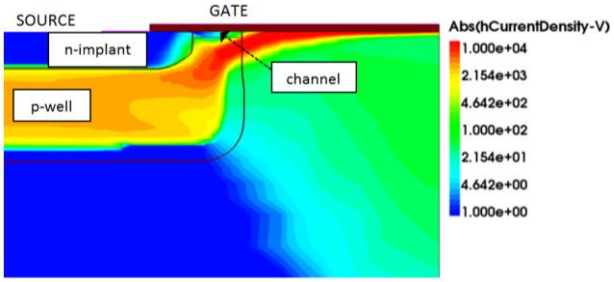

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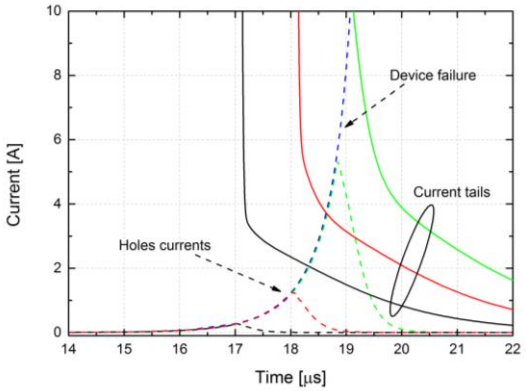

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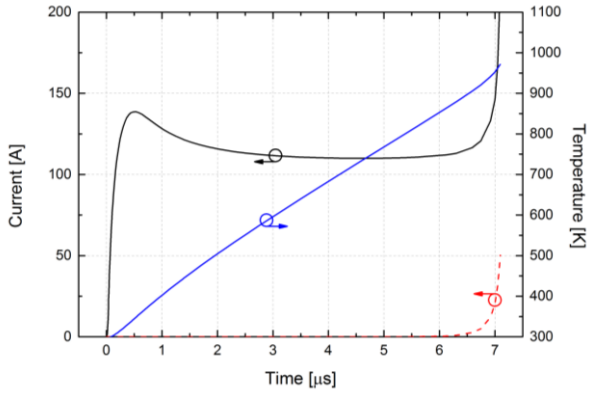
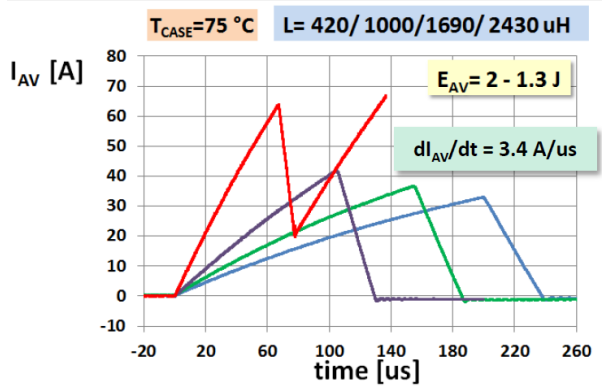


d)

Fig. 9. Simulation results: a) short-circuit current and temperature waveforms with V_{DS}=400V; b) hole current density at turn-off with t_{PULSE}=18.8µs (the scale is in A·cm-2); c) detail of current tails (solid lines) and hole currents (dashed); short-circuit drain (solid) and hole (dashed) current with V_{DS}=800V.

confirmation in other studies, which reported significant variation in the gate leakage current as a consequence of short-circuit stress [20]. Finally, as voltage and temperature are further increased, the device fails catastrophically without being able to do 10 µs, Fig. 8.

Further substantiation to the interpretation of the underlying failure mechanism comes from physical 2D device simulation. In [21], the authors have reproduced the experimental observations, including the change of slope, the current tails and the current runaway phenomenon for increasing pulse widths. Simulation results are shown in Fig. 9 a). The current change of slope and the current tails during turn-off have been attributed to thermally generated hole current flowing from the drift region and the source p-well, Fig. 9 b). Within the device structure, considerable temperature gradients can be present, with very high localised temperature values. As the pulse width and thus the device temperature increases, the tail currents amplitude also increases until the device enters a thermal runaway condition leading to catastrophic failure, Fig. 9 c). On the basis of these results, two different failure mechanisms are proposed, depending on the heat generation rate and two distinct temperature thresholds: at relatively low values of V_{DS}, power dissipation is contained and if the pulse width is increased, the device can reach and stay long enough above temperature values which can degrade the gate structure (this phenomenon is time related); on the other hand, if V_{DS} is increased, the device quickly reaches temperature values high enough to trigger hole current generation and failure is in this case determined by the electro-thermal runaway, Fig. 9 d).



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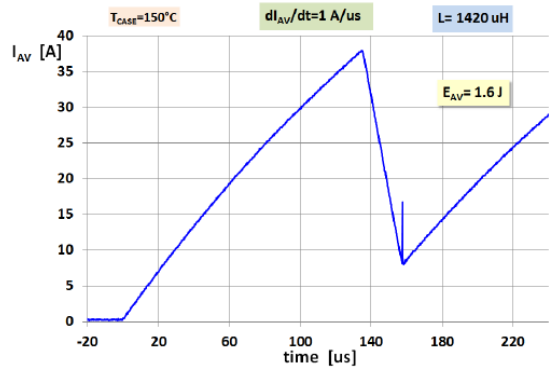
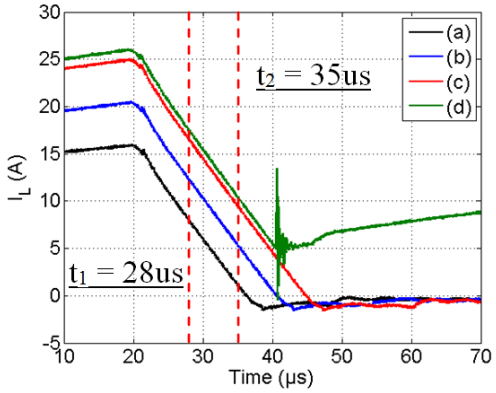


b)

Fig. 10. Avalanche current waveforms during UIS test of a 1200 V commercial SiC power MOSFET: a), T_{CASE}= 75 ºC and various energy, peak currents and dissipation rates are investigated until failure is reached; b) results in case of device failure with T_{CASE}= 150 ºC.



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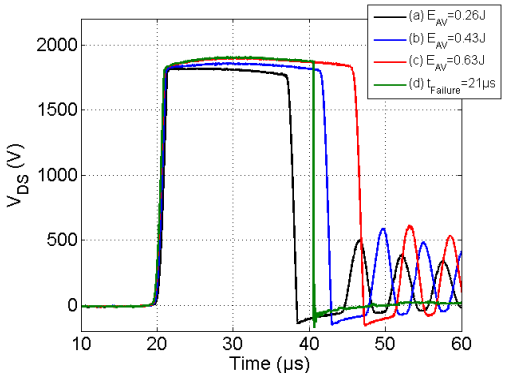

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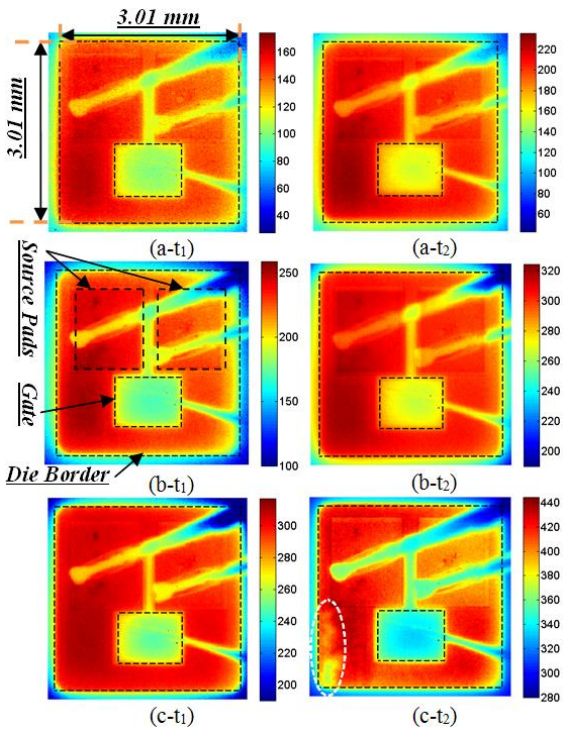


c)

Fig. 11. Avalanche current, a), and voltage waveforms, b), and corresponding device infrared thermal maps, c).

3.2 Single-pulse avalanche ruggedness

MOSFETs avalanche ruggedness is typically assessed with Unclamped Inductive Switching (UIS) tests [19, 22]. The typical robustness limit in Si is related to the activation of the parasitic BJT structure, which becomes more likely as temperature increases due to the significant reduction of the *p-n* junction forward bias voltage. However, due to their significantly higher energy bandgap value, SiC MOSFETs typically offer a high level of robustness against energy dissipation in the avalanche breakdown regime. Indeed, tests on voltage classes of 650, 1200 and 1700 V have confirmed the excellent robustness for most commercially available devices. Fig. 10 shows the drain current during UIS of commercially available 1200 V devices: the waveforms correspond to different energies and different energy dissipation rates. As can be seen in Fig. 10 a), for a case temperature T_{CASE} = 75 ºC, the devices can withstand energy values well in excess of 1 J. In this case, both the peak current values and the power dissipation are relatively high. However, as the temperature is increased to T_{CASE}= 150 ºC, Fig. 10 b), the maximum energy and dissipation rate, though still very good in absolute terms, are significantly reduced.

In this case too, tests aimed at assisting the interpretation of the failure mechanism by means of structural infrared characterisation have pointed out localised weak spots with final failure attributed to the achievement of an excessive temperature leading to degradation of some structural feature of the device [22]. Fig. 11 shows test current waveforms and the corresponding thermal maps: for each UIS event, two thermal maps were acquired during the time in avalanche of the device, at the time instants indicated by the dashed lines in Fig. 11 a), located at 28 and 35 µs from the time origin, respectively. Each pair of thermal maps is indicated with a), b) and c). These results give a clear idea of the temperature evolution within the device under this stress condition; also, thermal map c-t2 clearly shows the occurrence of some damage in the bottom left hand side corner of the device. Indeed, an additional UIS event with nearly identical stress characteristics, indicated as d) in Fig. 11 a), led to catastrophic failure of the device.

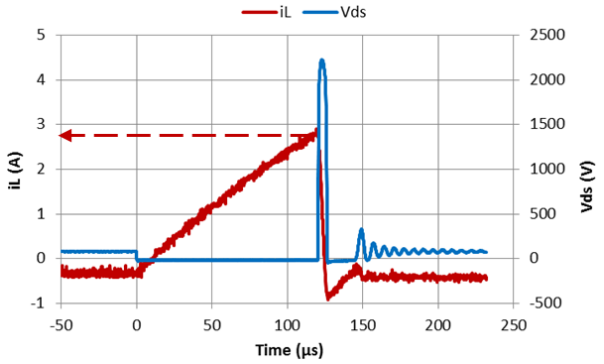
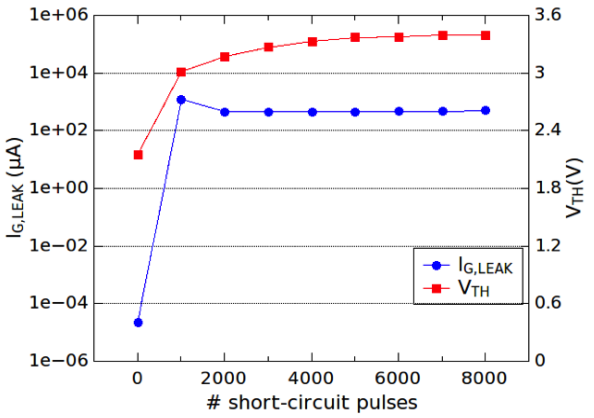


Fig. 12 UIS test on a commercially available 1200 V SiC MOSFET featuring actual breakdown voltage well in excess of 2000 V.

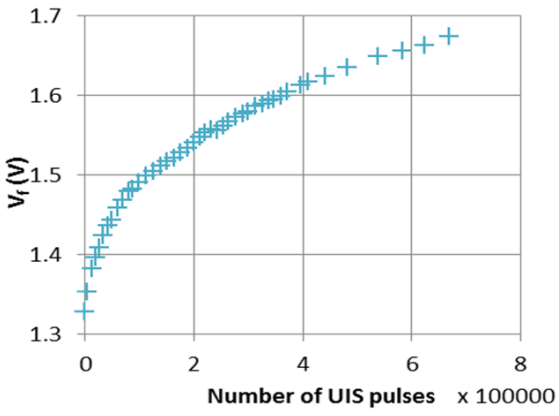
Finally, it is worth pointing out the presence on the market of 1200 V 80 mΩ devices designed with such high breakdown voltage that avalanche robustness is lost. Fig. 12 shows the current and voltage waveforms during an UIS test for such a device: in these results, although V_{DS} reaches well beyond 2000 V, the device does not actually enter avalanche breakdown; if the current is increased slightly and avalanche breakdown is entered, then catastrophic failure intervenes immediately, with no breakdown withstand capability evidence, even at these very low currents, due probably to electrical failures in some regions of the device (e.g., gate or terminations). In the understanding of the authors, such design feature is intentional and has the benefit of reducing the electric field intensity in the gate oxide during the off-state, thus enabling improved stability of its characteristics.

3.3 Aging after repetitive stress

Short-circuit and UIS being both very stressful events for the device and their occurrence during system operation being in some application domain a rather frequent event, information on device ageing as a result of repetitive exposure to such events is key to the validation for widespread acceptance of this



a)



b)

Fig. 13. Results of repetitive short-circuit and UIS tests: a) evolution of MOSFET threshold voltage (V_{TH}) and leakage current ($I_{G,LEAK}$) with number of pulses; b) evolution of body diode forward voltage (Vf) with number of pulses.

technology. The investigations in [18] and in [22] have shown that as a result of both, commercially available SiC power MOSFETs do exhibit a pronounced variation of some of their electro-thermal parameters. If the energies involved in the stress process are sufficiently lower than the maximum values the devices can withstand, then aging does not imply loss of functionality, but rather decreased performance only. On the basis of the results available, it is to be concluded that SiC MOSFETs show very good robustness characteristics towards these overload conditions, still prior to any specific device design and engineering having been specifically targeted to ensure as much. For illustration, Figs. 13 a) and b) show the variation of threshold voltage and gate leakage current and the variation of body-diode forward voltage for 1200 V commercially available devices subjected to repetitive short-circuit and UIS events, respectively.

4. Technology maturity

Traditionally, particularly challenging aspects of SiC MOSFET reliable technology development have been gate-oxide growth and interface traps, quality of the crystal (i.e., density of defects) and basal plane dislocation with stacking faults [3, 5]. Gate-oxide reliability is typically investigated, among others, by means of a standard test called High Temperature Gate Bias (HTGB), in which the device is statically biased between gate and source at a given positive and negative static stress voltage level for 1000 hours and variations in critical electro-thermal parameters (typically, threshold voltage and gate leakage current) are monitored. The quality of the crystal, junctions and device terminations can be checked by means of a High Temperature Reverse Bias (HTRB) test, in which the device is biased between drain and source at usually 80% of its maximum rated voltage withstand capability for 1000 hours, measuring variations in drain leakage current and, for the case of the MOSFET, body-diode forward bias voltage; since this stress to some extent also affects the gate-oxide, monitoring this parameter value also yield insight into technology maturity and stability. Both the HTGB and HTRB tests are usually carried out at the device maximum specified temperature.

In the following, results for HTGB and HTRB stability of commercially available 1200 V SiC MOSFETs are presented and discussed. Moreover, results of an additional test are presented, in which the gate-source voltage is pulsed as opposed to static, and the device is biased at the same time with a static drain-source bias voltage of 50% its maximum nominal rating: this test was devised in collaboration with industrial partners to be more representative of the actual stress conditions encountered in real applications.

4.1 HTGB Test

Fig. 14 summarises the results of tests conducted at bias voltage values of +20, -5 and -10 V, respectively, at a constant device case temperature of 150 ºC [23]. The graphs report the threshold voltage value, defined as the gate-source bias voltage at which the drain current is I_D = 5 mA, with the drain-terminal connected

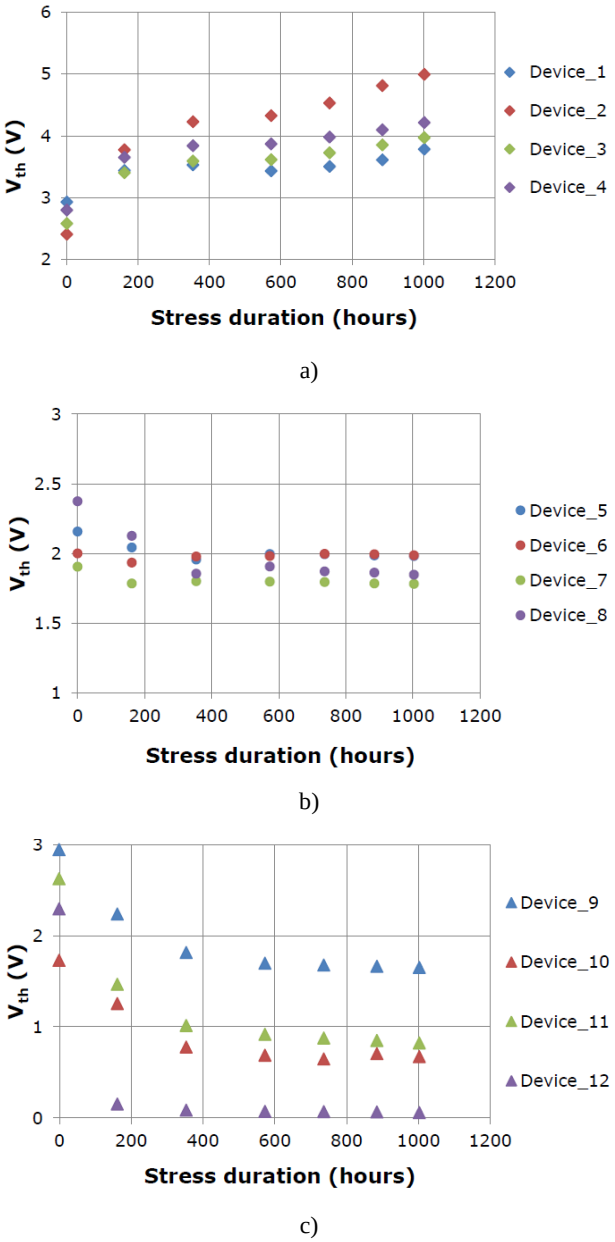


Fig. 14.Threshold voltage variation as a result of HTGB stress on commercially available 1200 V SiC power MOSFETs: a), V_{GS}= +20 V; b), V_{GS} = -5 V; c) V_{GS} = - 10 V. In all tests it is T_{CASE}=150 ºC.

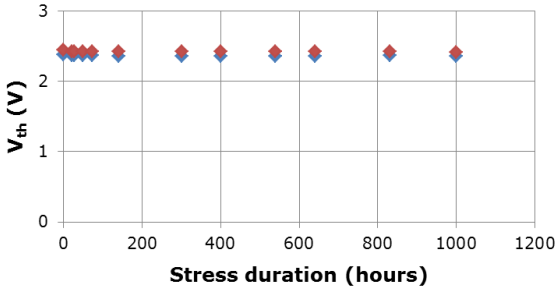


Fig. 15. Threshold voltage variation during HTGB stress for a commercial part designed with higher breakdown voltage (see Fig. 12).

to the gate. Clearly, these results highlight the need to still invest in research and design effort to further improve the stability of the gate characteristics. It is interesting to note that -10 V is in this case specified as the maximum permissible bias value in the device data-sheet, which however also indicates a recommended value of not less than -5 V; also, the maximum specified device temperature is 175 ºC. From an application point of view, such a pronounced drift would be unacceptable and there is a strong wish to be able to operate with lower turn-off bias voltages to safely cope with electro-magnetic noise generated during the transitions.

It is also worth mentioning the better gate stability of a second commercial device with formally identical ratings as the one used for the results of Fig. 14: this was a device designed with higher breakdown voltage, as discussed in Section 3.4, at the price of a penalty on its avalanche breakdown robustness. Fig. 15 shows the variation of threshold voltage during the HTGB test at a bias voltage of – 5 V and a device case temperature of 150 ºC. For this device, the specified maximum negative bias voltage is -6 V; the maximum specified temperature is however 175 ºC.

4.2 HTRB Test

The investigations in [23] have also reported on the drain leakage stability under HTRB stress with V_{DS} = 960 V and T_{CASE} = 150 ºC. Fig. 16 summarises the outcome. Here, the results are such that a larger sample population would be strictly required to conclude on the maturity of this particular aspect of the technology: indeed, two device show reasonable stability; one device shows a non-negligible percentage increase, but with absolute values which are still very good in comparison to Si; one device fails shortly after start of the test. Further testing is required on this aspect; in general, however, the issue is in general regarded as less critical than the pronounced variation of the threshold voltage, which has much more important impact on power system development.

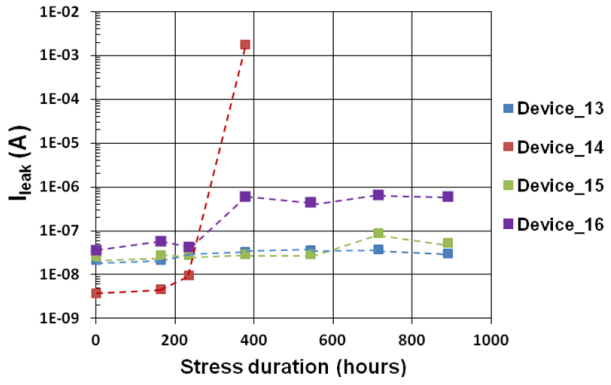


Fig. 16. . Evolution of drain leakage current under HTRB stress for a commercial 1200 V SiC power MOSFET.

4.3 Pulsed gate and drain bias test

To complement the information about device reliability, tests with pulsed gate bias and applied drain-source bias voltage, but no drain current flow, deliver useful insight, mainly from an application point

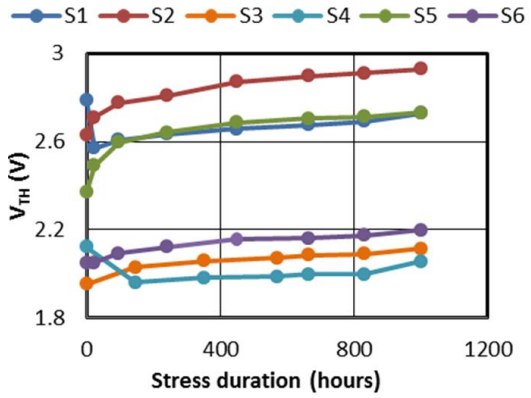


Fig. 17. Threshold voltage evolution during pulsed gate stress with applied drain-source bias. S1-S6 indicate the tested switch number.

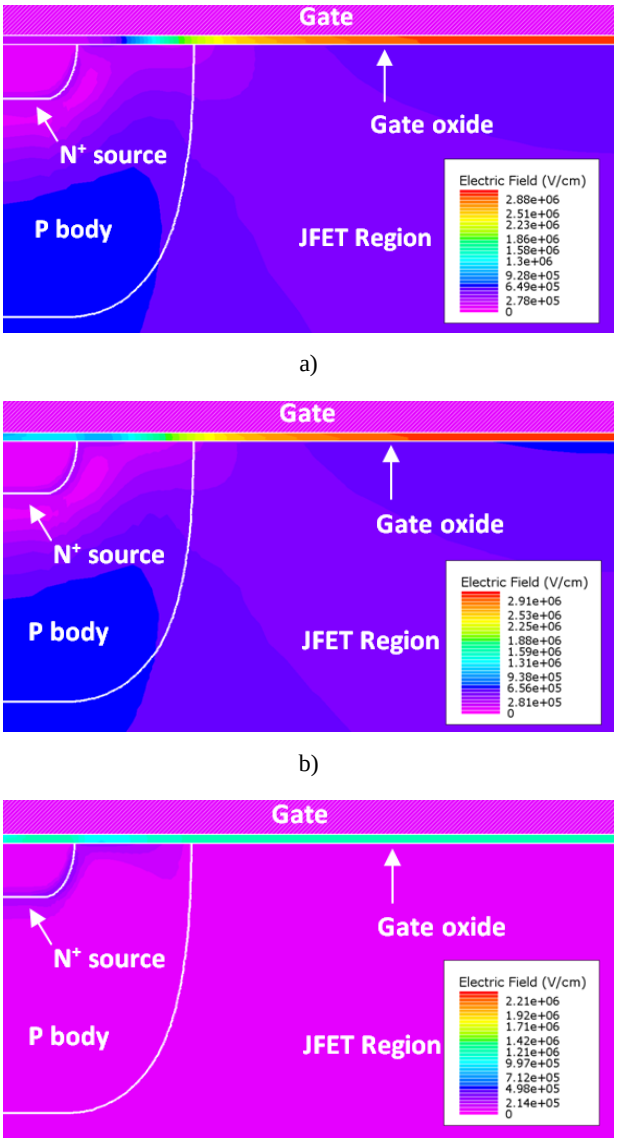
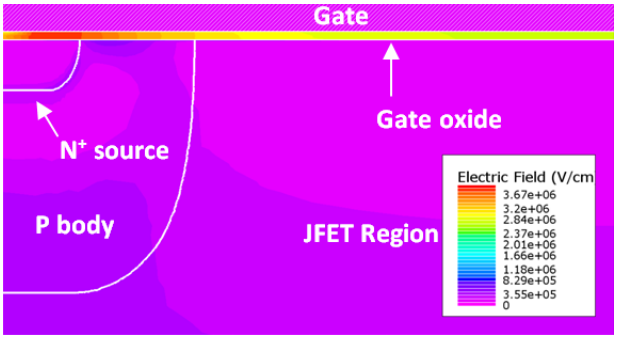


Fig. 18. Cross section of simulated device structure with detail of electric field in the gate oxide under various bias conditions: a) V_{GS} = 0 and V_{DS} = 600 V; b) V_{GS} = - 5 and V_{DS} = 600 V; c) V_{GS} = - 5 and V_{DS} = 0 V.

of view. In fact, under these bias conditions, the stress in the gate oxide is quite different than in the case of the HTGB and HTRB tests and in any case more representative of what the device actually experiences during operation in a real power converter.

The investigations in [24] have clearly pointed out that under a pulsed gate stress test with V_{DS} = +20/-5 V, V_{DS} = 600 V and T_{CASE} = 150 ºC, the variation of the threshold voltage is less pronounced than in the case of the static tests, Fig. 17.

This result is attributed on the one hand simply to the fact that the average voltage applied on the gate is lower in amplitude both when positive and when negative, with a decrease in absolute value which depends on the duty-cycle or pulse width modulation scheme during the test. Additionally, however, computer aided physical 2D device simulation has been used to show that the electric field in the gate oxide above the MOSFET channel region is to some extent reduced by the concurrent application of a drain-source bias voltage, for all values of the gate-source voltage. This is evident in the results of Figs. 18 and 19, which show the electric field distribution in the gate oxide under various bias conditions. Fig. 18 refers to V_{GS} = -5 V, whereas Fig, 19 is for V_{GS} = + 20 V.



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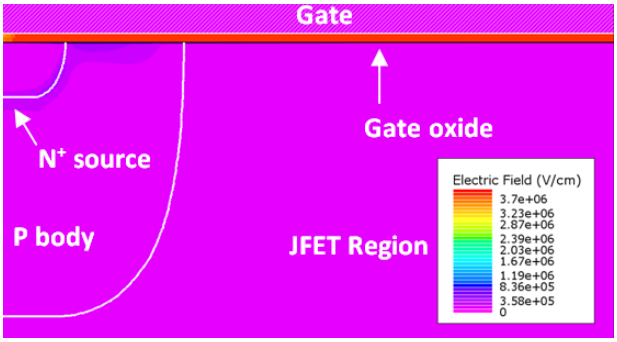


b)

Fig. 19. Cross section of simulated device structure with detail of electric field in the gate oxide under various bias conditions: a) V_{GS} = +20 and V_{DS} = 600 V; b) V_{GS} = + 20 and V_{DS} = 0 V.

5. Use as solid-state circuit breakers

Using solid-state devices as current limiter, regulators or breakers in place of electro-mechanical components has also been gaining in interest and attention over the past few years. For this application, the faster switching speeds and better handling of higher operational temperatures makes SiC a very interesting alternative to Si. Most SiC power MOSFETs, however, exhibit positive drain current temperature coefficient

$$\alpha_T = \frac{\partial I_T}{\partial T} \tag{9}$$

for a broad range of the gate-source bias voltage and temperature [25, 26]. A positive α_T is associated with thermally unstable behaviour, characterised by the device drawing more and more current as its temperature increases for given values of V_{GS} and V_{DS}. Thermally stable or unstable behaviour is determined by two concurrent effects: the increase with temperature of the on-state resistance, $R_{DS,ON}$, on the one hand, and the decrease with temperature of the threshold-voltage, *Vth*, on the other. Due to material physics (e.g., charge carriers mobility), technological and manufacturing issues, the decrease of *Vth* is presently the dominating effect in SiC and transfer characteristics with a broad range of positive α_T are a common feature.

Actually, $\alpha_T > 0$ is only a necessary condition for instability. If the parameter

$$S = \alpha_T \cdot V_{DS} \cdot Z_{\theta,JA}(t) \tag{10}$$

is defined, where $Z_{Th,JA}(t)$ is the transistor chip thermal impedance, then the actual criticality is represented by $S \geq 1$, that is,

$$\alpha_T \geq \frac{1}{V_{DS} \cdot Z_{\theta,JA}(t)} \quad (11)$$

Fig. 20 a) shows a plot of α_T as a function of I_D, for a given temperature value. For a given transistor chip, identified by a given thermal impedance $Z_{Th,JA}(t)$, the condition in (9) identifies two regions of operation, which vary with the value of V_{DS}: indeed, when the condition in (9) is satisfied, the device does exhibit thermally unstable behaviour within a range of values of I_D (I_1 to I_2), which becomes larger as V_{DS} is increased; however, as I_D increases beyond a given value (I_2 in Fig. 20 a)), the condition for thermal instability is removed and thermal stability can be re-gained. For even higher values of I_D, α_T becomes negative, removing the necessary condition for thermal instability. However, during pulsed operation, for a given V_{DS} value, the device temperature changes with the current and the device fails if the temperature at some location within the device exceeds the technologically allowed maximum before $I_D=I_2$. The time required for the onset of thermally unstable behaviour depend on the specific bias conditions and the chip thermal impedance This scenario changes drastically the Safe Operating Area (SOA) of Power MOSFETs: as illustrated in Fig. 20 b), in which the region of electro-thermal instability is highlighted, for higher values of $V_{DS,}$ the time required for the onset of thermal instability decreases. If instability does take place, then transient waveforms as shown in Fig. 21 a) are typical, with the current profile indicating current focusing phenomena within the chip, with experimentally demonstrated localised hot-spot formation and device failure under nominal operational conditions apparently still contained within the nominal SOA, Fig. 21 b) [27].

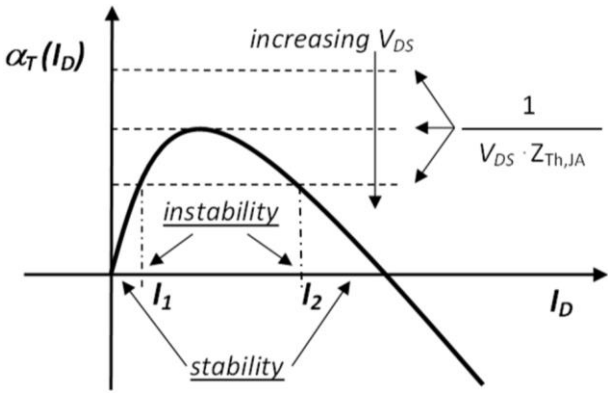
6. Discussion

The results presented indicate that SiC MOSFETs can be very competitive even as a drop-in replacement of Si transistors. In some application areas, they clearly have the potential to deliver revolutionary impact. SiC material is excellent for the design of very robust transistors, able to cope with very stressful operational conditions more reliably than Si: significant avalanche robustness comes nearly "for free"; short circuit robustness is presently limited to a great extent by structural features and it is expected that tailored device design and engineering can result in a relatively short-time in devices with good short-circuit robustness even at higher voltages and temperatures; overcurrent turn-off and over-temperature robustness are very good and presently mainly limited by packaging; reliability can in principle deliver much longer operational lifetimes, trading off with enhancements in power density. Still to assess is the long-term stability of the body-diode over time and under various operational conditions.

For SiC MOSFETs to be more easily accepted by end users, they have been thus far distributed mainly in established packages, common for Si devices. This represents an important limitation to the exploitation of the full potential of this technology, particularly in terms of power density, thermal management, parasitic inductance and common mode electro-magnetic noise at the higher switching frequencies: the development and use of bespoke packaging solutions will enable dramatic improvements in this respect and will contribute to improve reliability. Additionally, the development of bespoke circuit topologies can further enable optimum exploitation of the device characteristics.

7. Conclusion

Power electronics is being increasingly acknowledged worldwide as a key discipline for infrastructural development and societal progress. Advancements in this field are sure to have a deep impact onto a number of established and upcoming strategic areas, such as energy generation, transmission and distribution, electrification of rural areas, transportation, refrigeration and heating, cooking, telecommunications. Shift from Si to SiC technology has the potential not only to deliver more efficient



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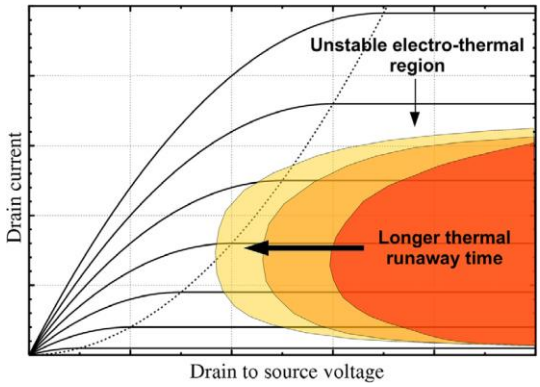
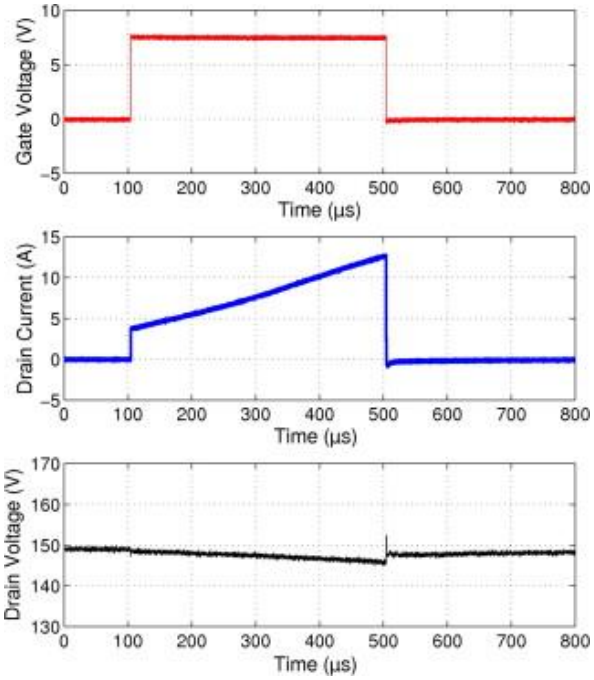


b)

Fig. 20. Illustration of thermal stability aspects of SiC power MOSFETs: a) current temperature coefficient qualitative dependence on current; b) effect of thermal instability on the -runaway on the SOA of Power MOSFETs.



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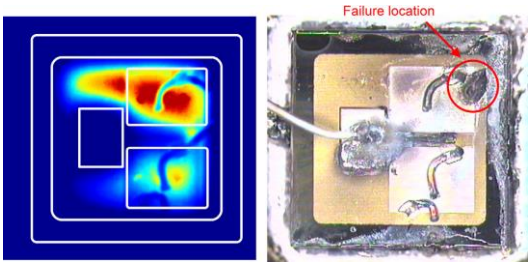

b)

Fig. 21. Experimental characterization of SiC power MOSFETs operated under thermally unstable bias conditions: a) representative electrical waveforms; b) device thermal map characterized by hot spot formation and eventually failed device.

systems (due to both reduced losses and reduced size and weight of on-board power systems), with improved functionality, robustness and reliability, but also to enable newer application domains for solid-state devices.

SiC power MOSFETs are still indicatively a factor ten more expensive than their Si counterparts. Presently, it is unclear if the unit price can be further reduced, due to higher manufacturing costs. However, in the assessment of the benefits of transitioning from Si to SiC, it is important to also consider: system level price reduction due to reduced filter and heat-sink sizes; simplified circuit topologies, with reduced component number and thus cheaper manufacturing, assembly and testing costs; running cost of the equipment, including energy savings over time and maintenance; added functionality, availability and reliability.

Based on the results produced thus far in specialist literature, the authors' judgement is that SiC will probably not be competitive with Si in all power conversion applications. It does however have a very strong potential for revolutionary impact in some highly strategic application domains, including transportation and energy generation, conversion, transmission and distribution. Still in the authors' opinion, whereas SiC devices at lower voltage ratings (indicatively, below 900 V) may be of interest in some specific applications, it is expected that GaN HEMTs will be the preferred choice in this voltage class due to competitive performance and price [28]: SiC MOSFETs are expected to dominate wide-band-gap power conversion for voltage ratings up to indicatively 3.3-4.5 kV. Above that, bipolar devices are likely to be a competitive alternative.

Acknowledgment

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