Low Voltage Power Conversion

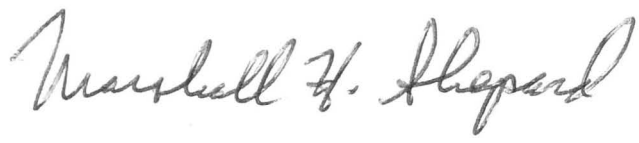
Marshall Howard Shepard

A thesis submitted for the degree of Master of Philosophy
of The Australian National University.

July, 2003

Declaration

I certify that, except where otherwise acknowledged in the text, this thesis is entirely my own work. I further certify that it contains no material previously submitted for a degree of The Australian National University, or of any other university or tertiary institution.



Marshall H. Shepard

March, 2004

Abstract

This thesis describes the design, construction and evaluation of a DC-DC converter intended for use with very low input voltages, such as would be obtained from a single solar cell or a parallel solar array. Although the low voltage power converter discussed here has been optimised for inputs from 0.5 to 0.6VDC, operation down to 0.3V or less is practical.

Particular importance is placed on the design of magnetic components. A new, semi-passive technique for the control of staircase saturation in transformer cores is presented. Unfortunately, the technique has proven to be unsuitable for low voltage applications. The reasons for this are explained.

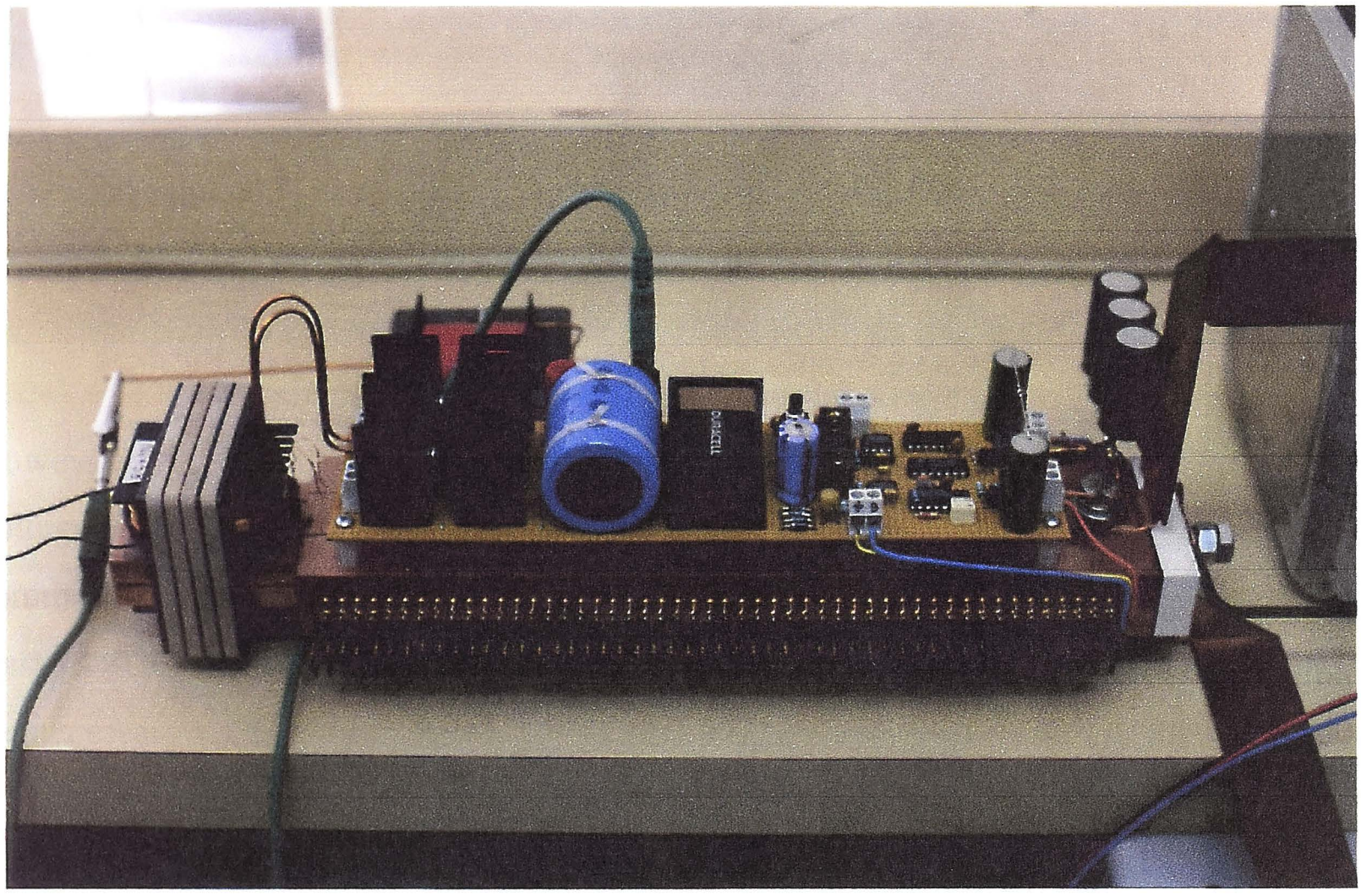
A circuit model for the converter is developed, and used to predict circuit operation. A core flux displacement hypothesis is presented, which addresses a discrepancy in voltage transformation between measured data and the model. To test the hypothesis, a specially constructed nickel steel transformer core was installed and evaluated.

The electrical and thermal design of a low voltage, 500A adjustable DC power supply is also discussed. This supply was required as a test input for the DC-DC converter, as parallel solar arrays would not have been convenient for developmental work.

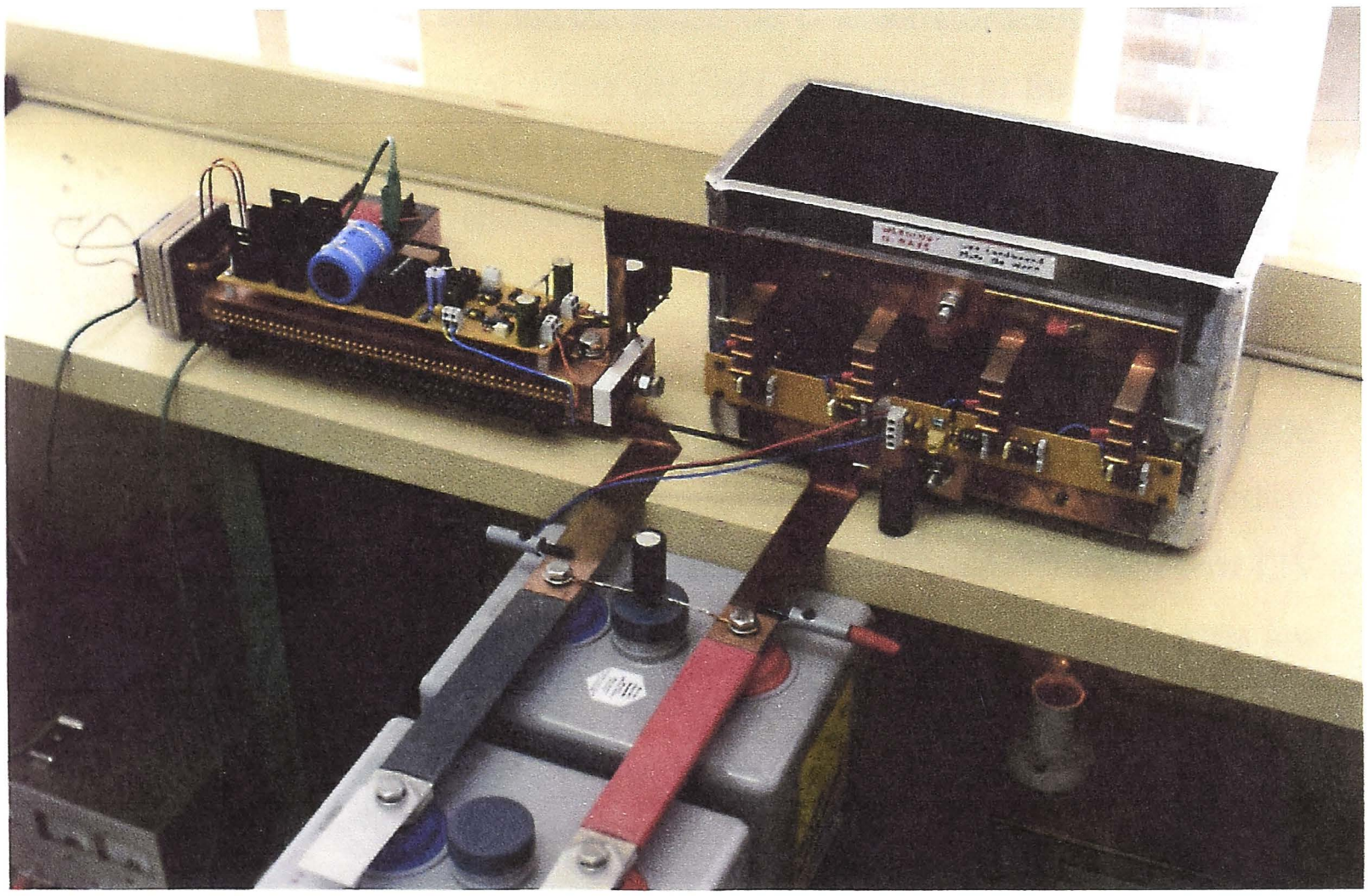
Table of Contents

Acronyms

AC	Alternating Current
ANU	Australian National University
CGS	Centimetre Gram Second
CSES	Centre for Sustainable Energy Systems
DC	Direct Current
DCPS	Direct Current Power Supply
DMM	Digital Multimeter
EMF	Electromotive Force
ESR	Equivalent Series Resistance
FEIT	Faculty of Engineering and Information Technology
FET	Field Effect Transistor
GBWP	Gain Bandwidth Product
LCR	Inductance (L) Capacitance (C) Resistance (R)
LED	Light Emitting Diode
LVPC	Low Voltage Power Converter
MKS	Metre Kilogram Second
MOSFET	Metal Oxide Silicon Field Effect Transistor
NiFe	Nickel Steel
PCB	Printed Circuit Board
PV	Photovoltaic
RMS	Root of the Mean of the Squares
SS	Stainless Steel
TTL	Transistor Transistor Logic



Low Voltage Power Converter



LVPC and 500A DC Power Supply

1 Introduction

1.1 Obtaining useful power from a photovoltaic array

Silicon solar cells produce DC electric power most efficiently when their output is approximately 0.6V per cell. Because this voltage is relatively low, cells are usually connected in series to form an array. For some applications (charging batteries, operating remote bore pumps) the power from DC solar arrays may be used directly. However, it is often desirable to convert the DC output to AC at some convenient voltage (e.g. 240Vrms). Electronic devices ("inverters") which convert DC to AC are commonly available and can take many forms. Most inverters require an input of at least 12VDC, and therefore at least 20 solar cells must be connected in series to obtain the necessary voltage. In stand-alone systems where power may be required in the absence of sunlight, solar cells charge batteries which in turn supply DC-DC converters or DC-AC inverters.

1.2 Low voltage power conversion

High efficiency solar cells and sun tracking solar concentrator arrays have been the subject of intense research interest within the FEIT Department of Engineering for many years. Significant progress has been made, both in the efficiency of photovoltaic cells and in the performance of the optical concentration systems in which they are used.

Although much progress has been made in improving cells and concentrators, the electrical power conversion techniques used to transform the output from these arrays have heretofore relied on DC converter or inverter circuits designed for inputs of 12V to 48V or more. Off-the-shelf power conversion products for use with low and extra low input voltages have not been available. This restriction has led to the necessity of interconnecting cells in series to achieve the required voltage. However, because current from a series array is limited by the weakest or least illuminated cell, care must be taken to match cells and ensure they are evenly illuminated. This requires extra testing, precise paraboloids, and accurate, two axis solar tracking. The effect of blocked or

defective cells can be reduced through the use of bypass diodes, but they dissipate power and can be difficult to install. Because cell anodes must be electrically isolated from each other, series arrays also impose limitations on thermal resistance between the cells and the heatsink.

Parallel arrays offer advantages in that all anodes can be bonded to a common heatsink, which can also serve as the positive output connection. Cell matching, solar tracking and uniformity of illumination become less critical; even a totally blocked cell has little overall effect. The disadvantage of parallel arrays is that output current will be one or two orders of magnitude greater than that which exists in a series array of equivalent output. As most electrical power conversion techniques rely on current switching, the ability to produce an economical low resistance switch is crucial to the success of low input voltage converters. (Shepard and Williamson [12]).

Previous work in the area of low voltage power conversion appears to be limited. Meyer and Schmidt [10] describe a 10W DC-DC converter operating from a 0.7V input and a 250W converter for use at 1.4V. The first was designed for fuel cell applications while the second was developed for three-junction amorphous silicon solar cells. Efficiencies of 80 to 95% were reported, but few details of the design were given.

The DC-DC converter discussed in this thesis is designed to operate from a parallel solar concentrator array with an output of about 0.55VDC at 450A. The circuit should convert this to 25VDC at 8A, suitable for charging batteries or operating a conventional mains output inverter. The 200W power level was selected because it is high enough to give a true feeling for the problems involved, yet low enough to be achieved within a limited (~$5,000) budget.

Extracting useful power from 500ADC at ½V potential is analogous to extracting the same power (250W) from a 500 litre/second flow of water at 5cm head. Both are mathematically easy, but both are technically challenging. The energy density of these sources is quite low (½ J/C and ½ J/l, respectively), therefore large flows must be accommodated to produce the required power. This leads to physically large (and therefore expensive) structures. The problem is essentially one of impedance matching:

A low impedance source demands a low impedance transducer, if reasonable efficiency is to be achieved.

There are also control problems associated with such high flow rates. Imagine instantly closing a valve in a length of pipe carrying a flow of 500 l/s. Not only would it be difficult to close a large valve "instantly", but unless they were very strong, the inertia of the water could cause the valve or pipe to rupture. Continuing with the analogy, if the commutation transistors in the ½V converter turn off in 0.5μs, even the inductance of 10cm of wire could convert the "inertia" of 500A (through ~0.1μH) into a 100V spike.

Identifying and analysing problems of particular relevance to low energy density electrical power conversion was a primary objective of this project. The second main goal was the construction of an efficient working prototype.

1.3 The 500A DC Power Supply

It is not convenient to use a solar concentrator array as a power source for developing prototype DC-DC converters. There are several reasons for this: It is sometimes necessary to work on cloudy days. A parallel concentrator array is not currently available and, even if one was, no physically realisable cable could carry the necessary current from the array to the laboratory without incurring an unacceptable voltage loss. (In practice, it would almost certainly be necessary to locate a low voltage converter very close to the solar array.) Therefore, a power supply is required which is capable of simulating the output of a 250W parallel solar array.

Because the efficiency of the power supply itself was not an issue, a linear regulator operating from a large battery was seen to offer the least costly alternative. Such a power supply was designed and constructed.

1.4 Thesis overview

This thesis begins (Section 2) with a discussion of the technologies relevant to the production of "useful" DC voltages (e.g. 24V) from the output of a parallel array of solar cells. Topics include the characterisation of the photovoltaic effect in silicon, the relative merits of various DC-DC converter configurations, and the magnetics of transformer design.

The next two sections (3 and 4) reveal the steps involved in the design and construction of a Low Voltage Power Converter (LVPC) and a 500A DC Power Supply. At each stage, design decisions are highlighted and justified. Particular attention is paid to the design of magnetic components – the LVPC transformer and output inductor. The operation of both circuits is discussed in some detail. These two pieces of equipment formed the basis of the experimental part of the project.

Results gained from performance testing of the LVPC and DC Power Supply are presented in Section 5. LVPC circuit losses are analysed in (excruciating) detail, and a complete model of its transformer is developed. Performance specifications are presented for both the LVPC and DC Power Supply, together with an analysis of their operating limitations and potential failure modes.

A circuit model for the LVPC is developed in Section 6. Simplifying assumptions are made, permitting the adoption of a DC equivalent circuit. The contribution of each element or functional block within the circuit is analysed, and the effects are incorporated in the model. Predictions based on this model are then compared with actual results, and similarities and discrepancies are noted.

Lessons learned from both the LVPC and the circuit model are addressed in Section 7. Measurement techniques are analysed, and design improvements suggested. One possible source of improvement involves the substitution of a nickel steel transformer core for the ferrite core used in the initial design. Implementation of this modification forms the basis of the next section.

Section 8 describes the design and characterisation of the LVPC transformer utilising a replacement core of laminated nickel steel. Revised performance figures are provided, conclusions are drawn, and some remaining questions are discussed. The section concludes with a discussion of an as-yet unresolved question concerning a voltage loss observed at the transformer secondary during all stages of the project. In this context, a moderately non-linear dependence of voltage loss on input current is explored.

Following is a summary of the principal findings, concepts and contributions resulting from this project:

- Notwithstanding the inherent difficulties, the output of a parallel photovoltaic array *can* be efficiently and reliably converted to a more useful voltage.
- Stray inductance and transformer leakage inductance are principal limiting factors in the design of efficient low voltage DC-DC converters.
- Stray inductance and the commutation of large currents dictate that snubber circuits be used on high power switching supplies – even when the source voltage is low.
- An inductive output filter can significantly improve the performance of forward converters, particularly when leakage inductance is present.
- Contact resistance and skin effect can be significant sources of loss in high current low voltage AC circuits, even at relatively low frequencies.
- Constructing a 0.1mΩ switch capable of changing state in 0.5μs is electrically simple, aesthetically pleasing, mechanically difficult, and financially painful.
- Power ferrites can be used to advantage at frequencies as low as 1kHz, particularly in circumstances where the higher flux density and permeability of steel alloys cannot be fully utilised due to other constraints.
- It should be possible to control staircase saturation in a transformer core by briefly interrupting primary drive at the point where the nominal flux zero crossing occurs.

2 Theory

2.1 The PV cell to DC converter interface

A silicon solar cell is simply a p-n junction designed to maximise electrical output power when exposed to sunlight. As a first order approximation, it may be represented as a diode in parallel with an ideal current source. The current source results from the separation of hole/electron pairs at the junction in response to the absorption of photons. The resulting current/voltage characteristics are therefore those of an ideal diode forward biased by a light dependent current source. For the purposes of this discussion, the series resistance introduced by metallic contacts and bulk silicon must also be considered.

The expression governing the I/V characteristics of a silicon diode is

$$V_f = (nkT/q) \ln(I_f/I_o) \qquad [2-1]$$

where V_f is the forward junction voltage, n is a current dependent factor of about 1 at higher current densities (Grove [6], pp. 186-190), k is Boltzmann's constant, T is absolute temperature, q is the charge of an electron, I_f is the forward junction current, and I_o is the junction reverse saturation current.

Solar cells produced by the ANU Centre for Sustainable Energy Systems are designed to operate at 20 suns, or an incident solar flux of about 2.0 W/cm^2. Even with active liquid cooling, junction temperatures of around 60°C can be expected (Andrew Blakers, pers. comm.). Under these conditions, cells typically have an open circuit voltage of 680mV and produce a short circuit current of 700mA/cm^2 (Andrew Blakers, Andres Cuevas and William Keogh, pers. comm.).

Because a cell is equivalent to a diode in parallel with a current source, an open circuited 1cm^2 cell with 2.0 W/cm^2 solar spectrum illumination will have 680mV forward bias and 700mA forward junction current. Solving the diode equation at this operating point gives

$$0.680 = 0.0287 \ln(0.700/I_o), \text{ or } I_o = 3.591\times10^{-11}\text{A}. \qquad [2\text{–}2]$$

Therefore, for the cells in question,

$$V_f = 0.0287 \ln(I_f/3.591\times10^{-11}), \text{ or } I_f = 3.591\times10^{-11}\exp(34.84V_f). \qquad [2\text{–}3]$$

If I_f is the junction current, then $0.700 - I_f$ will be the cell output current, I_{out}.

V_f is the voltage at the p-n junction, not the cell output voltage. Thin metal fingers on the upper surface of each cell are used to make electrical contact with the n-type silicon cathode. Junction current must also pass through the relatively thick p-type silicon substrate which forms the anode. The combined resistance associated with the fingers and substrate would be about 0.003Ω for a typical 18A cell (Keogh, pers. comm.). Normalising this figure on a per-square-centimetre basis gives $0.003 \times 18/0.7 = 0.077\Omega$. This resistance, R_s, is in series with I_f, and will produce voltage drop V_s. The actual cell output voltage, V_{out}, will be reduced by this amount. Cell output power, $P_{out} = V_{out} \times I_{out}$, and efficiency can be computed from $P_{out}/2.0$. Figure 2.1 summarises these results. The full set of calculated data from which this figure was derived appears in Table 2.1.

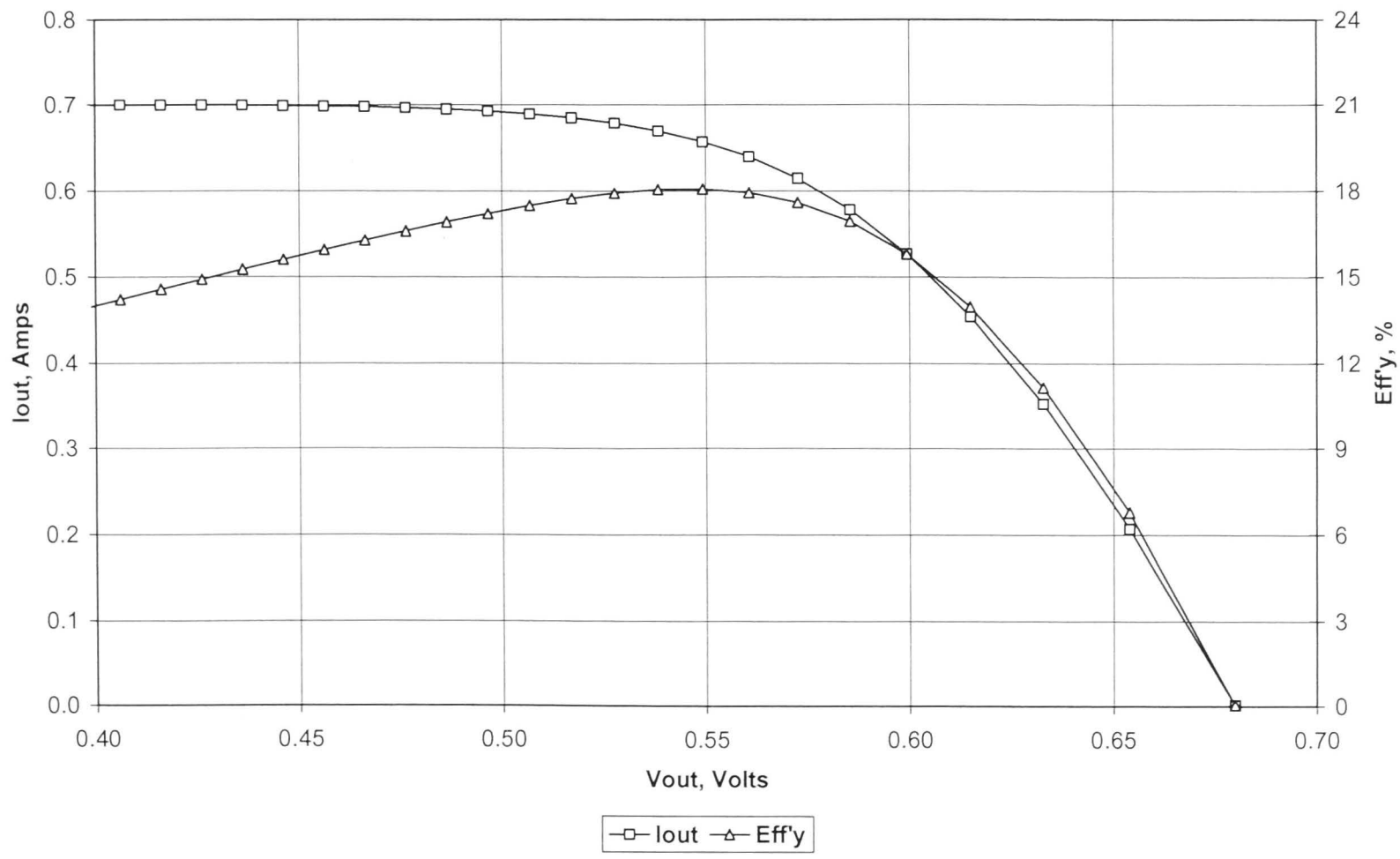


Figure 2.1 Characteristics of ANU CSES Solar Cells at 20 Suns.

Table 2.1 Characteristics of ANU CSES Solar Cells at 20 Suns ($2.0W/cm^2$).

Vf	If	Iout	Rs	Vs	Vout	Pout	Eff'y
0.45	0.000	0.700	0.077	0.054	0.396	0.277	13.86
0.46	0.000	0.700	0.077	0.054	0.406	0.284	14.21
0.47	0.000	0.700	0.077	0.054	0.416	0.291	14.56
0.48	0.001	0.699	0.077	0.054	0.426	0.298	14.90
0.49	0.001	0.699	0.077	0.054	0.436	0.305	15.25
0.50	0.001	0.699	0.077	0.054	0.446	0.312	15.59
0.51	0.002	0.698	0.077	0.054	0.456	0.319	15.93
0.52	0.003	0.697	0.077	0.054	0.466	0.325	16.26
0.53	0.004	0.696	0.077	0.054	0.476	0.332	16.58
0.54	0.005	0.695	0.077	0.053	0.487	0.338	16.90
0.55	0.008	0.692	0.077	0.053	0.497	0.344	17.20
0.56	0.011	0.689	0.077	0.053	0.507	0.349	17.47
0.57	0.015	0.685	0.077	0.053	0.517	0.354	17.71
0.58	0.021	0.679	0.077	0.052	0.528	0.358	17.91
0.59	0.030	0.670	0.077	0.052	0.538	0.361	18.03
0.60	0.043	0.657	0.077	0.051	0.549	0.361	18.05
0.61	0.061	0.639	0.077	0.049	0.561	0.358	17.92
0.62	0.086	0.614	0.077	0.047	0.573	0.351	17.57
0.63	0.122	0.578	0.077	0.044	0.586	0.338	16.91
0.64	0.173	0.527	0.077	0.041	0.599	0.316	15.78
0.65	0.246	0.454	0.077	0.035	0.615	0.279	13.97
0.66	0.348	0.352	0.077	0.027	0.633	0.223	11.14
0.67	0.493	0.207	0.077	0.016	0.654	0.135	6.77
0.68	0.699	0.001	0.077	0.000	0.680	0.001	0.05

V_f = Cell forward bias junction voltage. $V_f = 0.0287 \ln(I_f/3.591\times10^{-11})$.
I_f = Cell forward bias junction current, in Amperes. $I_f = 3.591\times10^{-11}\exp(34.84V_f)$.
I_{out} = Cell output current, in Amperes. $I_{out} = 0.700 - I_f$.
R_s = Cell contact finger plus substrate resistance, in Ohms.
V_s = Voltage drop across R_s. $V_s = I_{out} \times R_s$.
V_{out} = Cell output voltage. $Vout = V_f - V_s$.
P_{out} = Cell output power, in Watts. $P_{out} = V_{out} \times I_{out}$.
Eff'y = Cell efficiency, in percent. $Eff'y = 100P_{out}/2.0$.

Cell efficiency is highest (18%) when $V_{out} = 0.55V$, but remains above 17% from about 0.49 to 0.58V. To achieve maximum overall efficiency, the power converter should be designed to operate with an input voltage within this range (or, in the case of a series array, a multiple of it). This window of optimum efficiency will change somewhat due to temperature and illumination. Some converters automatically adjust their operating point to maximise output power, however the window is broad enough to

accommodate a ±10% change in operating voltage without reducing overall efficiency by more than 6% of its maximum value.

It should be noted that at voltages below the optimum power point the cell tends to look like a current source, while above this point it looks like a voltage source. Because of this, the converter designer must ensure current draw is relatively steady, otherwise cell voltage, and therefore efficiency, will vary. On the other hand, design is simplified to some extent because cells can produce neither excessive current under short circuit conditions, nor excessive voltage under no-load conditions.

2.2 Overview of competing converter technologies

Electrical power conversion can be defined as the process by which one form of electrical energy is transformed into another. The start and end points can be AC, DC, or a combination of both, and the conversion process can be either electrical or electromechanical. As this project is concerned primarily with the conversion of DC power from silicon solar cells, only DC input converters will be considered.

Electromechanical conversion is usually implemented with some form of motor/generator or motor/alternator combination, although these may share a single mechanical structure. DC input motor/alternators can convert the output of solar cell arrays directly into mains power with reasonable efficiency (70-80%). Their principal disadvantages of size, weight and maintenance requirements are partially offset by their chief advantage: robustness. (Iron withstands lightning better than electronic circuitry.)

The homopolar motor (e.g. the Faraday Disc) is of particular interest because its design is inherently suited to low voltage operation (Gottlieb [5], p.24). A homopolar motor driven alternator would be an excellent choice for low voltage power conversion, and significant progress towards a working design was made during the early stages of this project. However, high prototype fabrication cost estimates (approaching $10,000) ultimately precluded its use.

Almost all forms of DC electrical power conversion require some form of commutation. Therefore, an alternating voltage or current is always present within the device. The reason for this is simple: The magnetic components which function as energy storage and transfer elements depend upon changing magnetic fields for their operation, and DC can only produce a constant magnetic field. (The homopolar motor/generator is an exception. It sidesteps the commutation requirement by using sliding DC contacts and a fixed magnetic field.)

Electronic power converters can be designed to produce either AC or DC outputs. However, if a sinusoidal mains voltage output is desired, the conversion is usually accomplished in two stages. The input DC voltage is initially converted to another (usually higher) DC level, which then feeds a DC to AC inverter. Mains output DC-AC inverters with inputs from 12 to 96V are commonly available. For this reason, it was decided that a low input voltage DC-DC converter stage would be the primary focus of this investigation.

Most electrical DC-DC converters fall into one of two broad categories. The first is the *flyback* converter (figure 2.2), in which energy at one voltage or current is temporarily stored in an inductive circuit element, to be subsequently retrieved at a second voltage or current. In the flyback converter, energy storage takes place while the commutating device is conducting. This energy is then transferred to the load while the commutating device is switched off. Stored magnetic energy is fundamental to device operation, while turns ratio (in those cases where a transformer forms the energy storage element) is of lesser importance, as it does not determine the voltage transfer ratio of the converter. If a transformer is used, its principal function is to provide galvanic (DC) isolation between input and output, although turns ratio derived voltage transformation can reduce the voltage transient seen by the switching devices. The voltage or current transfer ratio is primarily controlled by adjusting the commutation duty cycle. Flyback converters are sometimes referred to as *boost* converters, especially if they are used in voltage step-up applications. This term can be confusing, as it is sometimes applied to other step-up designs as well. Flyback converters are typically used at power levels up to about 150W (Krein [9], p.156).

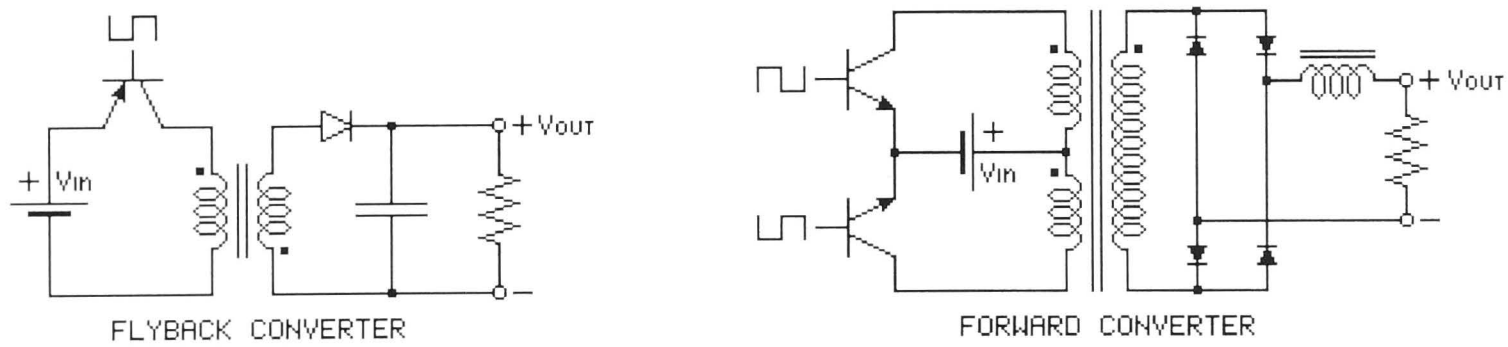


Figure 2.2 DC-DC converter types.

The second basic type is the *forward* converter (figure 2.2), in which the principal energy transfer from supply to load takes place while the commutating device is conducting. A transformer is frequently used to step the input voltage or current up or down by a desired amount, and to provide galvanic isolation. The turns ratio is very important, as it determines the approximate step-up or step-down ratio for the converter. Energy stored in the transformer's magnetic field is not central to the operation of the design, although changing magnetic flux must be present for the transformer to function. In contrast to the flyback converter, the duty cycle of forward converter commutation is usually maintained at or near 50%. Forward converters are sometimes called *buck* converters, particularly when a switched series inductor is used to step voltage down. However, the term can be misleading as it is used somewhat inconsistently in the literature. Forward converters employing bridge or push-pull primary drive are appropriate for high power applications up to 5,000W (Bird, King and Pedder [2], p.210).

A fundamental difference between flyback and forward converters can be found in their input current waveforms. Flyback converters draw input current in linear ramps. This is because a constant voltage will cause inductor current to change linearly with time. An important consequence of this is that the RMS input current can never be less than 1.15 times the average current. (The RMS value of a $2.00A_{peak}$ triangle wave is $1.15A_{rms}$.) Forward converters draw nearly constant current, so the average and RMS values will be similar. Because of this, I^2R losses will be at least $(1.15)^2$, or 33% higher in a flyback converter than in a forward converter of similar power rating. (This advantage will be reduced or lost in forward converters employing split primary windings because the effective primary resistance doubles while the half-winding RMS

current is 70.7% of the total.) In addition, current (and therefore magnetic flux) in the inductive component of the flyback converter is always unidirectional, whereas the transformer coupled forward converter exploits the full (four quadrant) B-H curve. This means a forward converter will require a core cross sectional area roughly half that of a flyback converter of similar rating.

The bottom line is this: The output voltage of flyback converters is easily controlled by adjusting the commutation duty cycle, making them quite versatile. However, forward converters are inherently more efficient, and are therefore better suited to high power applications.

Somewhere between electromechanical and all-electronic converters lies the (hypothetical) "homopolar switch" converter. This is a forward converter in which commutation is provided by one or more homopolar motor/generators connected in series with the primary winding of a transformer. With the homopolar motor field coil energised, the applied DC voltage will cause the (unloaded) rotor to spin. This in turn generates a back EMF in opposition to the applied DC source voltage, preventing significant current from flowing in the primary. After the non-conducting interval, the homopolar motor field coil is turned off. With no core flux there is no back EMF, the rotor acts as a short circuit, and the DC source is applied to the transformer primary.

Following the drive pulse, the homopolar motor field is re-energised, and the "switch" returns to its non-conducting state. While in the conducting state (with no field applied) the rotor will remain in motion. The only retarding torque is friction, and assuming this is kept small in relation to switching frequency, the rotor speed should remain fairly constant. Note that in this design the homopolar machine is employed as a four terminal device functionally equivalent to a relay.

The principal advantage of the homopolar switch lies in its ability to achieve commutation "contact" resistances of a few micro Ohms – far lower than is possible with any known individual semiconductor device. It should be noted that the writer is unaware of a homopolar machine ever having been used as a switch. Problems such as residual magnetism in the core would have to be overcome. However, the design was

excluded from further consideration primarily because prototyping costs could exceed those estimated for the previously mentioned homopolar motor/alternator.

2.3 Transformer magnetics, detailed model

An "ideal" transformer transfers electrical energy from one wire to another by means of a magnetic field which encircles both. In operation, one wire – the primary winding – supplies energy to the magnetic field, while one or more other wires – the secondary windings – remove energy from it. Energy removal may be concurrent, subsequent, or both, depending on the mode of operation. Ideal transformers are lossless, have infinite inductance, handle DC with ease, and do not exist. However, if they did exist, they would demonstrate the familiar transformer relationship:

$$N_p/N_s = V_p/V_s = I_s/I_p, \qquad [2-4]$$

where N_p and N_s are the number of primary and secondary turns. Real transformers routinely come within a few percent of achieving this relationship.

The following "imperfections" distinguish real transformers from their ideal counterparts:

* Winding resistance – The DC resistance of each transformer winding is usually modelled as a single resistor in series with a resistanceless winding. Its I^2R heating results in what is called "copper" loss.

* Eddy current loss – The I^2R loss associated with circulating currents induced in an electrically conductive core. These circulating currents are, in effect, resistively loaded single turn secondary windings, and can be represented as a single resistance referred to (and in parallel with) the primary.

* Hysteresis loss – Energy lost as heat in the process of reversing magnetic domains within the core. It is dependent upon both core flux density and excitation frequency. Under defined operating conditions it can be modelled as a fixed resistor in parallel with

the primary. The combined effects of eddy current and hysteresis losses are termed core or "iron" loss.

* Inter-winding capacitance – The distributed capacitance which exists between all the windings of a transformer. They are usually treated as single capacitors linking one terminal of each winding with one terminal of every other winding.

* Intra-winding capacitance – The distributed capacitance which exists between each turn of a winding and all the other turns on the same winding. It is usually modelled as a single capacitor in parallel with the winding.

* Magnetising inductance – The self inductance of that portion of the primary winding which is magnetically coupled (flux linked) with other windings. It is usual to represent this as a separate inductor in parallel with the primary winding of an ideal transformer. Total primary inductance is the sum of magnetising inductance and primary leakage inductance.

* Magnetising current – Current which flows in the primary magnetising inductance as the time integral of applied voltage. It is not related to any load component of primary current (transferred from a secondary) which may also be present. It is responsible for iron loss and contributes marginally to copper loss, but is essential for transformer operation.

* Leakage inductance – A distributed inductance which is not magnetically coupled with any other winding, as measured at the terminals of the winding. It is usually considered as a single inductor in series with each winding.

* Core saturation – The condition that exists in a ferromagnetic material when all domains have become aligned with the applied magnetomotive force (ampere turns), resulting in a permeability approaching that of free space. A saturated core effectively ceases to exist.

Taken together, these attributes suggest a model for the real, single secondary transformer as shown in figure 2.3. (See also: Duffin [3], pp. 261-268; Flanagan [4]; and Section 5.2.) The following notation is used:

R_p, R_s	Primary and secondary winding resistance
R_{fe}	Resistor representing the combined effects of eddy current and hysteresis loss
C_p, C_s	Primary and secondary intra-winding capacitance
C_{ps}	Primary to secondary inter-winding capacitance
L_{mag}	Magnetising inductance
I_{mag}	Magnetising current
I_p, I_s	Primary and secondary current
L_{lp}, L_{ls}	Primary and secondary leakage inductance
N_p, N_s	Primary and secondary winding turns
V_p, V_s	Primary and secondary voltage

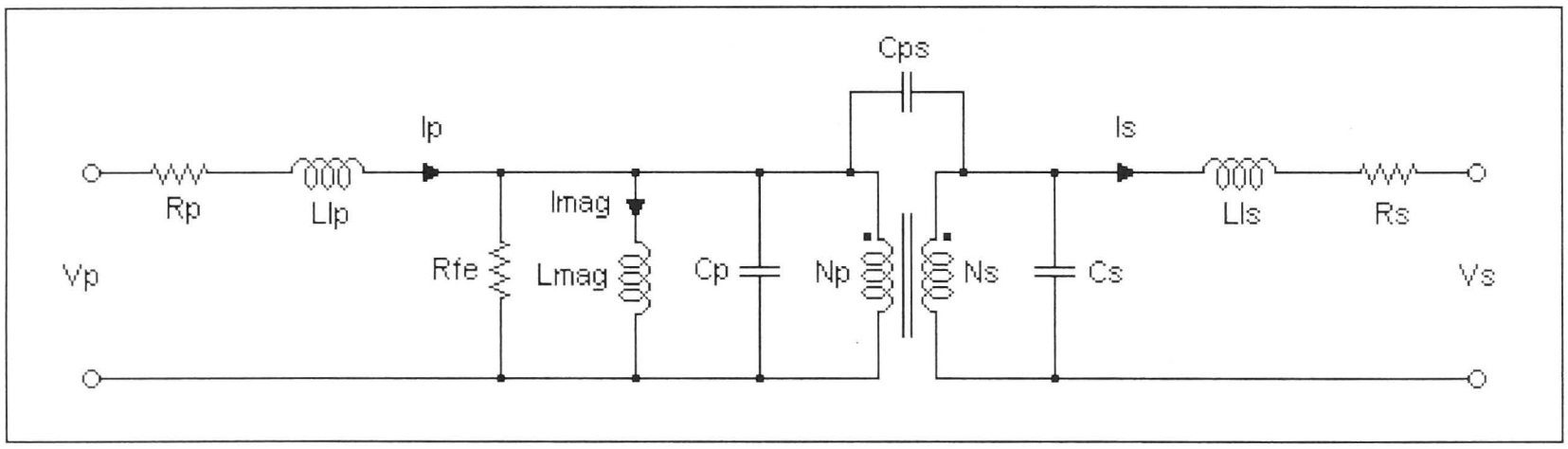


Figure 2.3 Transformer equivalent circuit.

Total primary winding inductance, as seen from the input terminals (with the secondary disconnected), is the sum of magnetising plus primary leakage inductance:

$$L_p = L_{mag} + L_{lp}. \qquad [2\text{–}5]$$

Any flux generated by the primary which does not pass through all turns of the secondary contributes to primary leakage inductance. The coupling coefficient, k, indicates the extent to which flux links the primary and secondary windings: $k = L_{mag}/L_p$, and therefore

$$L_{lp} = (1-k)L_p. \qquad [2-6]$$

By the same reasoning, any secondary turns which are not linked by primary flux contribute to secondary leakage inductance,

$$L_{ls} = (1-k)L_s, \qquad [2-7]$$

where L_s is the total secondary inductance as measured at its terminals (with the primary disconnected).

Many magnetics texts model the transformer as a "T" network composed of three inductors (Duffin [3], Hayt and Kemmerly [8]). In this model, the vertical leg is called *mutual inductance*, M, where $M = k\sqrt{(L_pL_s)}$. While mathematically expedient, this model has problems: M does not physically exist. Also, the inductances in the horizontal legs can assume negative values (a physical impossibility) to accommodate turns ratios other than unity. The model is mentioned here for completeness, but will not be used.

Switch mode power supplies generally employ ferrite cores because they can operate at much higher frequencies than steel or nickel alloys. Higher frequencies permit smaller, cheaper cores because flux density is inversely proportional to both frequency and core cross sectional area. For square wave drive,

$$B_{max} = e_{max}/4fN_pA_m, \qquad [2-8]$$

where B_{max} is the maximum flux density, e_{max} is the primary voltage, f is the drive frequency, and A_m is the magnetic cross sectional area. Therefore, for a given flux density, increased frequency permits a reduction in core cross section. Because transformer families have scaled standard shapes with fixed relative dimensions, this translates into a reduction in size.

But reduced size also implies a proportional increase in winding resistance, so primary turns must be reduced as the square root of the linear dimension (e.g. halving the size implies $1/\sqrt{2}$ turns) if copper loss is not to increase. Core loss is proportional to frequency, core volume, and flux density:

$$P_{fe} \propto f A_m l_m B_{max} = l_m e_{max}/4N_p, \qquad [2\text{–}9]$$

where P_{fe} is the core loss and l_m is the magnetic path length. Therefore, for a given primary voltage, core loss is proportional to l_m/N_p. If N_p is proportional to $\sqrt{l_m}$, then P_{fe} is also proportional to $\sqrt{l_m}$. Clearly, a net reduction in core size is possible.

However, with both N_p and A_m decreasing, f must increase (as $l_m^{-2.5}$) to maintain a given flux density and prevent the core from being driven into saturation. The bandwidth of the core material therefore becomes a limiting factor in size reduction. Power ferrites are available with bandwidths up to about 1 MHz, permitting the use of drive frequencies as high as 100 kHz. Above this speed, reduced μ and B_{max} present additional trade-offs.

Skin effect (see Billings[1]) has been ignored in the preceding discussion. If the current penetration depth is greater than the conductor radius, skin effect will be minimal. However, when the conductor is large and/or the frequency is high, skin effect can reduce the effective conduction cross section, thereby causing resistance to increase. Although wire diameter will tend to decrease with a reduction in core size (as $l_m^{0.75}$), the frequency required to prevent saturation will increase at a much greater rate. At some point, skin effect will begin to increase the copper loss and become an additional factor limiting transformer size reduction.

Skin effect is significant in the primary winding and input conductors of the LVPC. However, it does not contribute appreciably to losses in the secondary winding or output circuitry. Refer to Section 5.1 for details.

2.4 Core saturation, cause and prevention

All ferromagnetic materials used in electromagnetic devices (including inductors, transformers, and motors) will saturate if flux density exceeds a critical value. The transition from the unsaturated to saturated states ranges from gradual to abrupt, depending upon the material. In power ferrites and steel alloys intended for power applications, the transition tends to be smooth but fairly rapid, with full saturation being approached gradually beyond a pronounced knee in the graph of flux density (B) vs. field intensity (H). Above the knee, increases in magnetomotive force will produce small corresponding increases in field strength, ultimately approaching those which would result if the core was replaced by air. At this point, the core becomes magnetically useless.

The magnetising current in an inductor (including transformer and motor windings) is proportional to the applied voltage and time. That is,

$$i_L(t) = (1/L) \int v_L(t)dt + i_L(0) \qquad [2-10]$$

where L is the inductance, v(t) is the voltage waveform, and $i_L(0)$ is the initial current. Flux density, B, is proportional to magnetising current (and several other physical parameters), so it will increase with the product of voltage and time. Flux density will reach the saturation limit whenever the corresponding volt-second product is exceeded. This can occur if an applied AC voltage is too high, or its frequency too low, resulting in excessive area under successive positive and negative half-cycles of the waveform. It can also occur if DC (or an AC voltage with DC offset) is applied for too long.

Saturation has a number of undesirable effects. The worst is possibly the sharp rise in current associated with falling inductance. Inductance is proportional to permeability, μ, which is defined as the ratio of flux density to field intensity, B/H. ($H = NI/l_m$, where l_m is the effective magnetic path length.) As saturation approaches, B increases at a much slower rate than H, with the result that μ and L decrease rapidly. From the expression for $i_L(t)$ given above, it can be seen that rapidly decreasing inductance implies rapidly increasing magnetising current, significantly higher than that which would result from

the volt-time product alone. The resulting current spike increases copper loss and adds to the voltage drop across commutation devices, both of which contribute to a reduction in secondary voltage.

There is also a rough correlation between core permeability and coupling coefficient. As permeability falls, less flux is confined to the core, so primary to secondary flux linkage is reduced. For the same reason, primary and secondary leakage inductances (and their associated voltage drops) tend to increase (Krein [9], pp. 422 and 431). This effect also acts to reduce the secondary output voltage.

"Staircase" saturation in transformers is a gradual drift towards core saturation resulting from unequal positive or negative ampere seconds in the magnetising current. It is usually caused by unequal push-pull primary drive, but can also result from differing positive or negative ampere seconds in any component of secondary current not reflected back (magnetically coupled) to the primary supply. Differing positive and negative conduction intervals, unequal turns in split-primary windings, mismatched rectifier diode forward drops, and variations in winding resistance can all contribute to the problem. As one or more of these conditions exists in every real transformer circuit employing switched primary drive, the effect is always present to some degree. It can be a major design problem. Traditional solutions include (Billings [1]):

* Inclusion of an air gap in the magnetic path to increase the ability of the core to handle a DC flux component.

* Addition of series resistance in the primary drive circuit to decrease the applied volt seconds at the onset of core saturation.

* Inclusion of a capacitor in series with the drive circuit to eliminate any DC component in the primary.

* Active feedback derived from primary current or voltage sensors may be used to control ampere seconds by adjusting the ratio of positive to negative primary drive.

None of these solutions are completely effective; all involve significant drawbacks.

It should be possible to improve upon the active feedback technique by continuously measuring core flux with a Hall Effect sensor located in the magnetic path. Such transducers have the advantage of being able to detect DC flux, and knowledge of this would permit continuous adjustment of the primary drive so as to actively prevent a DC flux imbalance.

Another (and potentially simpler) alternative would be to introduce a brief mid-cycle interruption to primary drive at the nominal core flux zero-crossing to enable any flux imbalance to dissipate into primary or secondary circuitry through flyback action. With push-pull primary drive there exists a point (nominally half way through each drive pulse) when core flux should be zero. However, any inequality in primary or secondary ampere seconds will shift this zero crossing in time. After many cycles, core saturation results (unless some limiting process intervenes). If the drive transistor is momentarily switched off mid-cycle (at or near the flux zero crossing), any magnetic field present will collapse, generating a current into the supply or load circuitry presenting the lowest impedance. This discharge of magnetic energy will always act in the direction required to re-zero the core flux excursion. The process repeats twice each drive cycle.

This last technique was implemented in the initial design of the Low Voltage Power Converter (see Section 3.7), but was subsequently abandoned due to complications relating to the presence of high levels of leakage inductance.

The flux zero-crossing flyback antisaturation technique described above is believed to be new. No reference to it has been seen in any of the literature consulted to date. Although not yet evaluated in a transformer drive circuit where the additional switch-off interval could be tolerated, this novel concept should be of substantial benefit to designers of drive circuits for magnetic components where staircase saturation is a problem. The only limitation to its successful implementation appears to be related to leakage inductance. The time required to reverse the load component of primary current in the leakage inductance depends upon the ratio of the product of that current and inductance to the primary drive voltage (see Section 5.2). If the current reversal time is

small in comparison to the drive interval (the usual case), then the zero-crossing flyback technique should be successful.

3 LVPC Design

3.1 Introduction

In most designs, the DC-DC conversion process involves three basic steps. The first is commutation; the DC input must be converted to AC. Next, the AC is transformed to AC at a different voltage level, with or without galvanic isolation. Finally, the transformed AC is rectified and filtered to produce the desired DC output. As discussed in Section 2.2, the two principal types of AC transformation are flyback and forward. A forward conversion design was chosen for the low voltage power converter because it offers the best possible efficiency in high power applications.

3.2 The push-pull converter

Forward converters fall into three main sub-types: Full (or "H") bridge, half bridge, and push-pull. The full bridge type utilises four switching devices for commutation, the half bridge uses two switching devices plus a series capacitor, and the push-pull uses two switches and a split (centre tapped) primary transformer winding. (Krein [9], pp. 146-148.) The terminology is often blurred, with the two bridge types sometimes being given the push-pull designation also. (Push-pull refers to transformer drive in which primary current is actively driven in alternate directions, which is the case with all three types described here.) Figure 3.1 illustrates the basic structure of the full and half bridge designs. The push-pull forward converter is shown on the right hand side of figure 2.2.

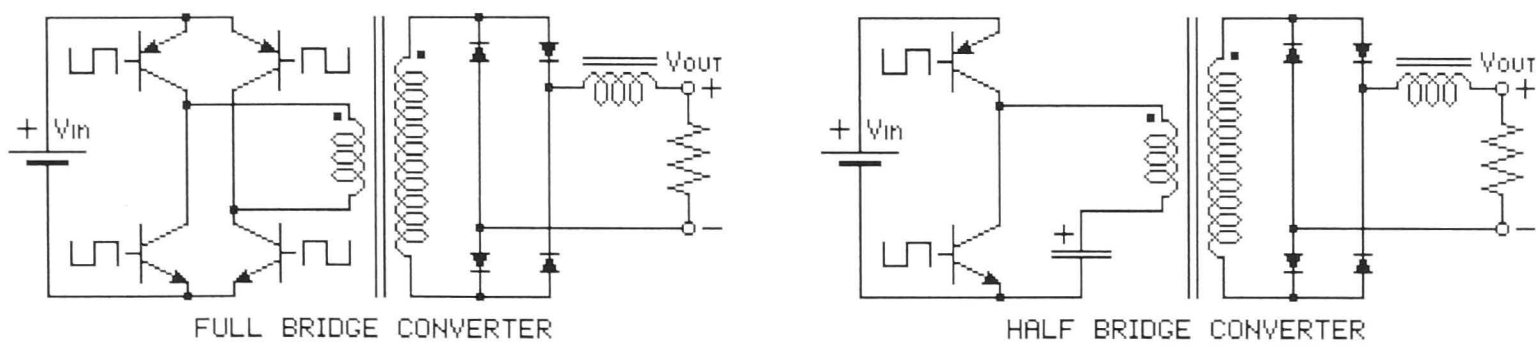


Figure 3.1 Full bridge and half bridge forward DC-DC converters

For applications involving low input voltages, commutation losses assume critical importance. In the full bridge design, input current must pass through two switching devices in series with the primary. Both switches incur a voltage loss. While presenting only one series switch, the half bridge design adds a series capacitor which also inserts a voltage loss. In this application, such a capacitor would need to possess humorous specifications (e.g. C = 10F, ESR = 20μΩ) to keep its associated voltage drop comparable to that across the switch. The push-pull design uses only one switch in series with each half primary. The trade-off is less a than optimal utilisation of primary core window area. However, in this case the transformer cost is about one tenth that of the switching transistors, so a slight increase in core dimensions is a relatively small price to pay in relation to the cost of halving the combined switch resistance.

The push-pull split primary forward DC-DC converter topology appears to offer the most promise in low voltage, high power applications. With some modification, it forms the basis of the design implemented.

3.3 MOSFET drive circuit and snubber

The following circuit descriptions refer to the Low Voltage Power Converter schematic diagram which appears at the end of this section. A List of Materials for the LVPC is given in Appendix I.

The first step in the conversion process is commutation. Given a target output power of 200W, an assumed converter efficiency of 80% at full power, and a 0.55V input from a parallel solar cell array, an input current of 455A is to be anticipated. If this is to be switched with less than 10% of the input voltage lost across the switching devices, their combined "on" resistance must be less than 120μΩ. An extensive search of available switching devices revealed that the Philips PHP130N03T MOSFET yielded the lowest resistance × dollar product available at that time (27 mΩ$ in 1999). With an R_{ds}(on) of 5mΩ (typical), 42 transistors in parallel should suffice. A contact resistance of 1mΩ per transistor was then assumed, leading to the conclusion that 50 MOSFETs would be required to drive each half-primary.

It was later considered prudent to install the transistors so as to facilitate replacement. Individual gold plated pin sockets were used, which increased the average contact resistance to about 5mΩ per transistor. This resulted in a total $R_{ds}(on)$ plus $R_{contact}$ of about 200μΩ per bank. However, the copper bus bar source/drain assembly had already been machined, so the number of MOSFETs per bank remained at 50.

With $0 > V_{ds} > 1V$, PHP130N03T MOSFETs have a typical input capacitance (C_{iss}) of 5500pF. Of this, about 2000pF is reverse transfer capacitance (C_{rss}), and 3500pF is gate-source capacitance (C_{gs}). Gate-source threshold voltage (V_{th}) is about 3V, but a V_{gs} of 10V is needed to ensure minimum $R_{ds}(on)$. Because in this application the voltage to be switched is so small, the Miller charge is only $C_{rss} \times \Delta V_{ds} = 2nC$ per FET. However, the gate charge is $C_{iss} \times \Delta V_{gs} = 55nC$, giving a total of $57nC \times 50 = 2.85\mu C$ per bank. This charge must be supplied by the gate drive circuit. A combined gate current of 10A could be expected to switch a transistor bank in $2.85\mu C/10A = 285ns$. This seemed a reasonable target.

TelCom TC4422 MOSFET driver ICs should be able to supply about 7A into 0V with a 12V supply, but their 1.5Ω typical output resistance would limit average 0-10V drive current to about 3.7A. A complementary emitter follower (Philips BDT81 and BDT82 power BJTs) was used to buffer the TC4422 outputs, thereby ensuring adequate current throughout the gate charge/discharge interval. A 0.47Ω series gate resistance was added to limit peak current to the transistors' $I_c(max)$ of 20A. Gate rise and fall times of 500ns (for a 10V swing) were achieved in the actual circuit, indicating an average gate drive current of $2.85\mu C/0.5\mu s = 5.7A$ during the switching interval. Averaged over one full cycle, gate drive current is only $2.85\mu C \times 4$ transitions $\times$ 1 kHz = 11.4 mA.

The gate drive waveforms are generated by hard-wired TTL. A 74LS123 dual retriggerable multivibrator produces an asymmetrical 2 kHz clock with a 0.1% duty cycle at "A" and "B" (figure 3.2). Flip-flop 2 of the 74LS74 divides this down to 1kHz, and outputs a square wave and its complement at "C" and "D". Although clocked, LS74 flip-flop 1 is not used in the present drive circuit configuration. However, it is used when antisaturation drive is desired (Section 3.7). The square waves are then ANDed

with the clock (and inverted clock) to produce 0.5μs break-before-make gaps in the complementary drive waveforms at "E" and "F". These gaps are necessary to prevent simultaneous conduction in both halves of the primary, a condition which would effectively present a short circuit to the input.

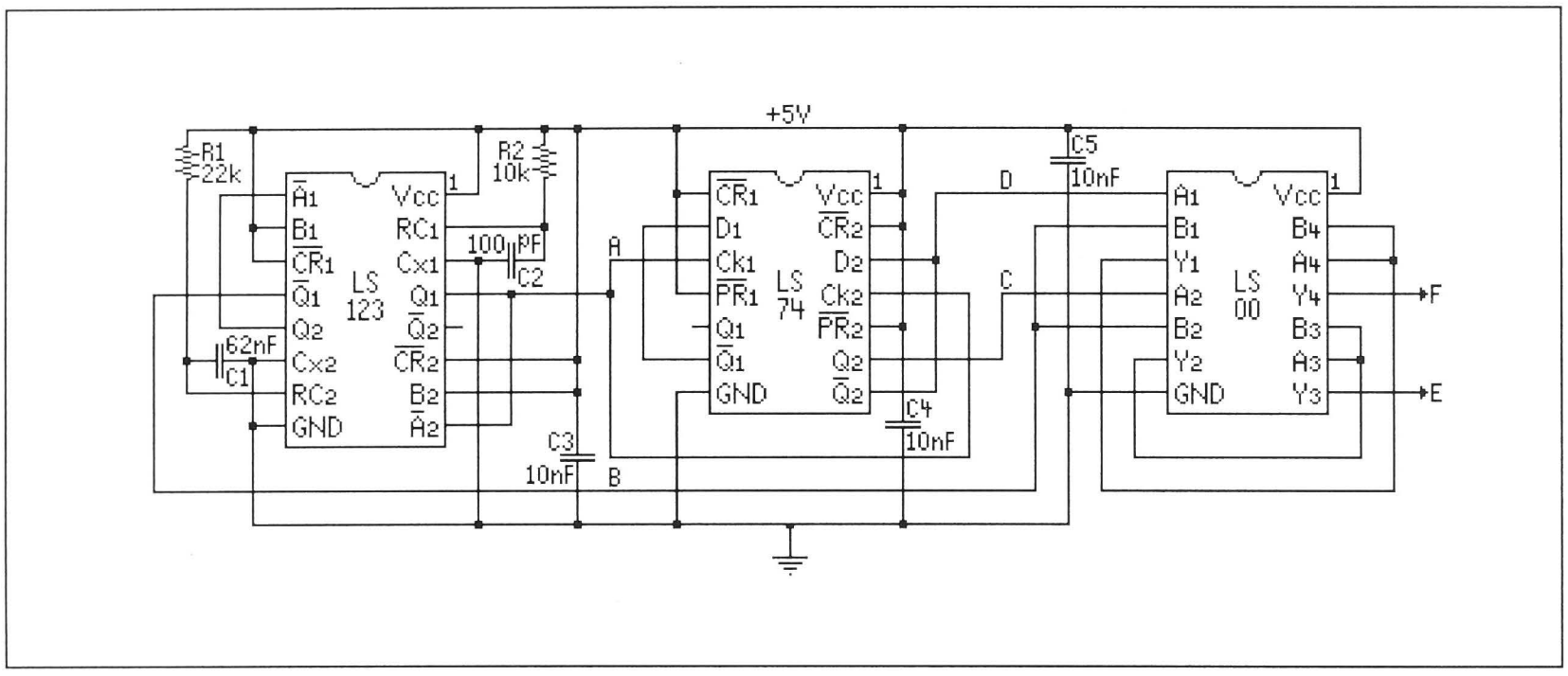


Figure 3.2 Drive waveform generator.

The drive circuit and core flux waveforms are given in figure 3.3. Note that the time axis is discontinuous, permitting details of the transition points to be shown.

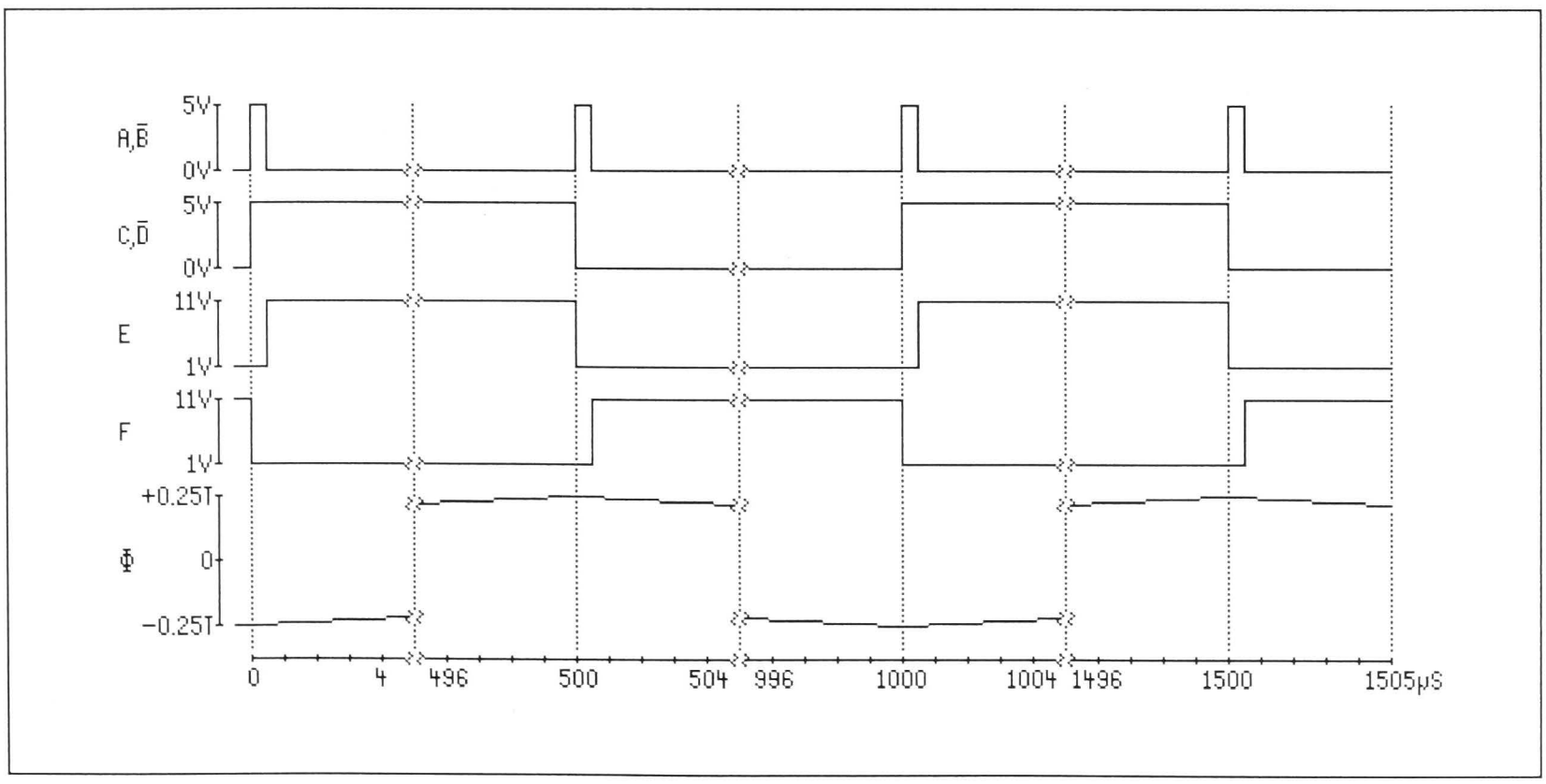


Figure 3.3 Drive circuit and core flux waveforms.

Magnetic energy – predominantly that component stored in transformer primary leakage inductance – is released following each drive interval. This energy produces an Ldi/dt voltage spike across the switching device unless it is diverted to some other component. A snubber circuit is used in which fast recovery diodes D1 and D2 divert switching transients to capacitors C15 and C16, where they are temporarily stored until being returned into the +0.55V input through resistors R7 and R8.

In this device, transformer leakage inductance referred to the primary is about 140nH (see Section 5.2). With an input current of 155A, stored energy is $\frac{1}{2}LI^2$, or 1.68mJ. At 1 kHz, 1000 × 1.68mJ × 2 off-transitions, or 3.36W could be released. Each 1.68mJ spike would charge the (2 × 10μF) snubber capacitors to about 13.0V ($W = \frac{1}{2}CV^2$), if the switching interval is long enough. However, $\tau = \sqrt{(LC)} = 1.67\mu s$, so the capacitor voltage can only rise by a maximum of about 3.9V during each 0.5μs t_{off} interval. (It actually rises by 5.2V, probably because charging continues beyond the t_{off} interval. See Section 6.2 for further discussion.) Most of the remaining leakage current will continue to circulate in the primary where it will act in opposition to the next drive pulse. Except at very low current levels, the voltage across the snubber resistors will be greater than the input supply voltage. Therefore, only a portion of the stored energy will be returned to the +0.55V input. Most will be dissipated in the snubber resistors.

In the absence of a snubber circuit, switching transient power would be dissipated in those few MOSFETs in each bank which happened to have the lowest drain to source breakdown voltages. While repetitive drain-source breakdown is not necessarily damaging to FETs, such operation is not recommended.

3.4 Drive circuit power supply

The following circuit descriptions refer to the Low Voltage Power Converter schematic diagram which appears at the end of this section.

Power to operate the logic and MOSFET driver circuits is derived from an auxiliary transformer winding of 28 turns. During operation, this winding delivers a nominal 14

VAC square wave, which is rectified and filtered to produce unregulated 12 VDC for the FET drive stage. A 78L05 linear regulator is then used to establish the 5.0 VDC rail for the TTL waveform generator. Total power consumed by the drive circuit and its associated power supply is about 0.6W. Drive circuit power is linearly dependent upon LVPC input voltage, but independent of output load.

Because the auxiliary winding delivers power only after operation commences, a start-up circuit is required. For this purpose, a small 9V battery is momentarily connected to the 12V supply rail to enable FET drive to commence. The supply becomes self-sustaining after the first few cycles, so the momentary contact battery switch (S1) can be released. In view of the low input voltage to the LVPC, any automatic start-up circuit would probably need to employ either battery power or germanium transistors ($V_{be} \approx 0.3V$). However, it was not considered necessary to incorporate an auto-start feature at this time.

An "interesting" start-up problem was observed during initial prototype testing. When the start button was pushed, the first drive pulse would be generated as soon as the LS123 commenced oscillation, which occurred when the logic supply reached about 3.5V. The gate current associated with the first drive pulse would depress the raw supply voltage (then about 5.0V) which, in turn, permitted the logic rail to fall below 3.5V. This caused the LS123 to reset briefly until its supply again reached the minimum operating level. The resulting power supply oscillation caused excessive drive current to flow into the combined gate capacitance, which effectively clamped the 12V drive circuit supply rail to 5V, thereby preventing normal start-up.

A start-up inhibit circuit was added to correct this problem. In operation, this circuit disconnects the 5V rail until the 12V rail filter capacitor (C17) has charged to at least 7.5V. Zener diode D12 sets this voltage in conjunction with R10 and R13. These two resistors also provide hysteresis, which is required to prevent the start-up inhibit circuit from oscillating. With 2.5V headroom, the linear regulator can comfortably maintain the 5V rail until normal operation of the auxiliary secondary is established (within several cycles). The circuit also serves to inhibit driver operation if the 12V rail falls below about 6.5V for any reason. This feature prevents drive circuit supply oscillation in the

event of reduced input voltage (<0.3V). It will also shut down the LVPC under severe overload conditions.

3.5 Transformer design

In an ideal transformer only the turns ratio is important. The actual number of turns is irrelevant. This is true because primary inductance is infinite, so there is no magnetising current. In a real transformer primary inductance increases, and magnetising current decreases, as the square of primary turns:

$$L_p = \mu N_p^2 A_m / l_m, \qquad [3-1]$$

where μ is the permeability of the core material. Core flux density (and therefore core loss) increases linearly with the volts per turn ratio ($B_{max} = e_{max}/4fN_pA_m$) so, for a given primary voltage and frequency, increasing primary turns will cause core loss to fall proportionately. For most core materials the area enclosed by the magnetisation curve, and therefore core loss, tends to increase rapidly as saturation approaches. For this reason the knee of the magnetisation curve – not the actual saturation limit – is used to establish the maximum permissible volts per turn ratio.

Unfortunately, primary resistance (and therefore copper loss) increases with the square of the number of primary turns. This is because, for a given core, winding length increases in proportion to turns while the window space available for each turn (i.e. the wire cross sectional area) decreases. The transformer will be most efficient when the sum of copper and core losses is minimised, and this condition often occurs when these losses are nearly equal.

Transformer design is usually an iterative process. There are so many interdependent yet differently weighted variables that an optimal design based on their simultaneous solution is often impractical. Therefore, the first step is to reduce the number of variables by making a few assumptions.

Assumption 1: Each half of the split primary winding will consist of a single turn.

This assumption is dictated by the fact that any primary designed to carry 450A is going to have a large cross section, and will very likely have to be machined from solid copper. Also, while fractional turns (e.g. 2.5) are technically possible (with an EI or EE core), they are significantly longer than their closest integral counterparts because turns are applied to the outside legs. They will therefore present significantly more resistance.

Assumption 2: A standard, off-the-shelf EE core in power ferrite will be used.

As the LVPC is a switch-mode power supply, it was assumed the general rule that "faster is better" would apply (see below), and that power ferrite was therefore an appropriate choice for the core material. This assumption later proved to be partly incorrect, but because the prototype design was based upon a ferrite core, this will be considered first.

For a given power level, larger cores tend to be more efficient than smaller ones. This is because windings can be thicker and flux levels lower, so both copper and core losses reduce as size increases. Of course, larger cores are more expensive. But in this design the cost of the largest readily available core set and winding bobbin (about $15.00) was negligible compared with the cost of MOSFETS ($547.00) and other components. An E65/32/27 core set was selected. Samples were ordered in Philips 3C90 and Neosid F5 materials, both of which have similar specifications.

Assumption 3: A nominal output of 25VDC at 8ADC (200W) is appropriate.

Choice of output voltage is relatively unimportant. The intent of the design is to establish the practicality of constructing an efficient DC-DC converter for use at very low input voltages. Except at very high voltages (where thick insulation displaces copper cross section in the window), transformer efficiency is almost independent of voltage. 25V is a good compromise between electrical safety and convenience, and many DC/AC inverters operate with this voltage as a nominal input. Also, fixed losses associated with rectifier diode forward drops are less significant at 25VDC than they would be at a lower voltage.

With these three assumptions made, transformer design is straightforward. It should be noted that magnetics calculations may be carried out in either the mks system, in which B, H and Φ carry the units Tesla, Ampere turns/metre and Weber, or in the cgs system, where the same parameters are measured in Gauss, Oersteds and Maxwells. The mks system is gradually displacing cgs in the literature, and will be used here (with the exception of small linear dimensions, where metres can be cumbersome). In the discussion which follows, reference will be made to the core's mechanical and magnetic parameters as set forth below.

E65/27/32 core set design parameters:

Magnetic path length (effective)	l_e	14.7 cm
Magnetic cross section (effective)	A_e	5.35 cm^2
Permeability (effective)	μ_e	2.0 mH/m
Bobbin winding window area	A_w	3.92 cm^2
Length of turn (mean)	l_T	15.1 cm

Because primary and secondary windings carry equal ampere turns, core losses are usually minimised by assigning half the winding window area to the primary, and half to all the secondaries. (This is not strictly true when a split primary is combined with an un-split secondary, but the difference is negligible. The proof is tedious and uninformative.) The coil former (bobbin) window comprises two sections separated by a partition, each measuring 1.92 cm wide by 1.0 cm deep. Allowing for 0.06 cm insulation (air and epoxy) between them, both split primary turns should be able to have rectangular cross sections of 0.93 × 1.0 cm, and a length of 15.1 cm. Each half-primary will have a DC resistance of $\rho l_T/A = (1.73 \times 10^{-6})(15.1)/(0.93) = 28.1\ \mu\Omega$. Skin effect (see Section 5.1) will cause the effective resistance to be somewhat higher, but it still compares favourably with the as-designed switch resistance of 120μΩ.

If the LVPC is to operate with a nominal input of 0.55 VDC, and if 455A × 120μΩ = 0.055 V will be lost in switching, the primary should see about 0.495 VDC. However, with 455A × 28.1 μΩ = 0.013 V lost across the primary resistance, the effective primary voltage is only 0.482 V. The secondary must supply enough voltage to forward bias the

MBR6045 Schottky diode bridge rectifier ($V_f = 0.50 \times 2$ at $I_f = 8A$) plus its own winding resistance, and still supply a nominal 25VDC at full load.

Primary I_pR_p drop is about 2.6% of the applied voltage. If it is assumed that the secondary will experience the same percentage voltage drop as the primary (a reasonable first-pass approximation), then about $(25.00 + 1.00) \times 2.6\% = 0.68$ V will be lost. Therefore, the secondary should have sufficient turns to produce 26.68V, or $N_s = 26.68/0.482 = 55.4$ turns. As fractional turns are impractical, N_s should be 56 turns.

The window area available for the secondary also measures 1.92×1.00 cm. To achieve maximum fill factor, layer winding should be employed. Consideration of the available dimensions leads to the conclusion that 6×11 turn layers results in the largest possible wire diameter consistent with the requirement for 56 turns. The resulting optimum wire diameter is 1.66 mm; the closest standard wire size is 1.5 mm. Even with 1.5 mm wire, insulation thickness, layering imperfections, and the fact that the last turn on each layer is also the first turn on the next combine to limit the actual number of turns per layer achievable in practice to 10. Although the design called for 56 turns, 58 turns were actually applied because space was available. This was done under the assumption that removing unwanted turns would be much easier then adding them later if modification proved necessary.

The secondary will have a DC resistance of $\rho l_T N_s/A = (1.73\times10^{-6})(15.1)(58)/(0.0177) = 85.6m\Omega$. Skin effect should not be significant with wire of this diameter. Note that $8A \times 85.6m\Omega = 0.68V$, or about 2.4% of the nominal full load secondary voltage of $0.482 \times 58 = 27.96V$. The assumption concerning voltage drops of similar percentages in the primary and secondary was justified. The fill factor is $(0.0177 \times 58)/1.92 = 53.5\%$, which is normal for layer winding.

Converter performance can be estimated by substituting values for R_p, N_p, N_s, and R_s into the transformer model given in Section 2.3. AC parameters and core loss may be ignored at this stage. Considering only DC losses, $(V_{in} - I_pR_{ds} - I_pR_{contact} - I_pR_p)(N_s/N_p) = V_{out} + 2V_f + I_sR_s$, and $I_p = (N_s/N_p)I_s$.

If $V_{in} = 0.55V$, $R_{ds}(on) = 100\mu\Omega$, $R_{contact} = 20\mu\Omega$ (the pre-socket value), and R_p, N_s, N_p, V_f and R_s are as stated above, then $V_{out} = 30.9 - 0.5838I_s$. For $P_{out} = V_{out}I_s = 200W$, $V_{out} = 26.49V$ and $I_s = I_{out} = 7.55A$. $I_{in} = I_p = 58I_s = 437.9A$, so $P_{in} = 240.8W$. Therefore converter efficiency, $\eta = 83.0\%$. Transformer copper losses will be $I_p^2R_p + I_s^2R_s = 5.39W + 4.88W$, or about 5% of output power, giving a transformer efficiency (discounting core losses) of about 95%.

As mentioned above, the addition of MOSFET sockets caused $R_{contact}$ to increase to $100\mu\Omega$. The result of this change is that $V_{out} = 23.70V$, $I_{out} = 8.44A$, and $\eta = 74.3\%$ if a 200W output is to be maintained. A more accurate AC evaluation using the full circuit model will give somewhat more pessimistic results (see Section 6.2), however the turns ratio and copper loss appear to be satisfactory.

Operating frequency must be determined by evaluating conflicting trade-offs. Higher frequencies involve higher switching losses. Because a fixed interval is required to reverse current in the leakage inductance, higher frequencies also reduce the effective drive duty cycle, thereby increasing RMS current (and copper losses) in the windings. Core loss is proportional to both drive frequency and B_{max}, but as B_{max} is proportional to 1/f, drive frequency does not significantly affect core loss unless B_{max} is pushed beyond the knee of the magnetisation curve. For the ferrites considered here, the magnetisation curve begins to bend noticeably at about 350mT, and inputs up to 0.67V are possible (see Section 2.1). With $B_{max} = e_{max}/4fN_pA_e = 0.67/4f(5.35 \times 10^{-4})$, $f_{min} = 895Hz$.

A preconception that a good starting point for ferrite core drive is a frequency just above the audible range gave 25kHz as the initial selection. However, dismal preliminary test results quickly led to this being reduced, first to 2.5kHz, and then to 1.0kHz. Incipient core saturation due to drive pulse imbalance or unequal primary coupling has fixed 1.0kHz as the lower practical limit with this core (see Section 5.3). At this frequency, and with $V_p = 0.50V$, B_{max} is nominally 234mT.

The data sheet for the Philips E65/32/27 in 3C90 material lists core loss as 9.1W at 25kHz and 200mT. The data sheet for the Siemens E65/32/27 in N27 material (a power ferrite similar to Neosid F5) gives a value of 14.6W under the same conditions. With

core loss proportional to drive frequency and flux density, at 1kHz and 234mT it should be about 426mW for 3C90 and 683mW for N27/F5. Therefore, if $V_p = 0.5V$, then R_{fe} will be 587mΩ and 366mΩ for the two materials, or 477mΩ average. However, at about 0.3% of maximum output power, core loss is nearly 20 times less than copper loss, and therefore practically insignificant.

Transformer primary magnetising inductance, $L_{mag} = \mu_e N_p^2 A_e / l_e$, or 7.28μH for the transformer as wound. Measurements made on the Neosid core using a Marconi TF1313A impedance bridge confirmed primary inductance as 7.3μH (Q = 0.80) at 1kHz and 7.2μH (Q = 0.70) at 10kHz. Secondary inductance measured 28.5mH (Q = 34) at 1kHz, which is reasonably close to the expected $58^2 L_p$. Core bandwidth was measured with $N_p = N_s = 9$, $V_p = 2.50V_{peak}$ (sinusoid), $R_{source} = 33\Omega$, and $R_{load} = 100\Omega$. Under these conditions $f_c = 1.2MHz$, where $V_s = 2.5/\sqrt{2}\ V_{peak}$ at an angle of −50°. V_s rolled off smoothly with increasing frequency.

3.6 Leakage inductance minimisation

As stated previously, transformer leakage inductance is a distributed inductance in a winding which is not magnetically coupled with any other winding. Although not part of the transformer, any uncoupled inductance in series with a transformer winding adds to the effective leakage inductance. For this reason, inductance associated with the wiring to and from a transformer should also be minimised.

Leakage inductance is a problem for several reasons. First, the $L_l di/dt$ voltage developed across it always acts to oppose the voltage applied to or developed by a winding, thereby reducing the effective turns ratio. Also, a finite amount of time is required twice per cycle for load current to reverse in the leakage inductance. To maintain the same average current, the RMS current must increase as the reciprocal of the square root of the duty cycle. (e.g. For the same I_{avg}, $D = 0.9 \Rightarrow I'_{rms} = I_{rms} / \sqrt{0.9}$.) Finally, energy stored in primary leakage inductance is released into the drive circuit at switch-off, where it is dissipated as heat unless energy recovery measures are in place.

Because of the high di/dt's associated with switching large currents, the LVPC is particularly vulnerable to the adverse effects of leakage inductance. This fact was only vaguely appreciated during the early design stages, but it has become by far the most troublesome obstacle to attaining the desired performance.

Current is supplied to each half-primary through copper bars machined from the same piece of copper as the winding itself. These bars are parallel and closely spaced, so that flux generated by each will partially link with and, because the currents are equal and opposite, partially cancel the flux from the other. One bar carries input current from the positive supply to the transformer. The other connects to the drains of the 50 MOSFETs which drive the associated half-primary. The sources of these MOSFETs connect to a third copper bar which parallels the others and forms the negative return for the circuit. The length of the bars is about 270mm, corresponding to fifty TO-220 transistor packages mounted at 5mm spacing.

The LVPC draws discontinuous current, primarily because of the dip produced during the time required to reverse load current in the leakage inductance. Under these conditions, cable inductance produces undesirable Ldi/dt voltage spikes at the LVPC input, despite its being filtered by 3 × 4.7mF low ESR capacitors. For this reason, it was also necessary to reduce the inductance associated with the cables supplying current to the converter. Parallel cabling was impractical, so shortening the battery/regulator/ LVPC loop to around 850mm was the best that could be achieved.

3.7 Antisaturation feature

The LVPC design initially incorporated a feature intended to prevent core saturation (see Section 2.4). With the fundamental drive frequency set at 2.5kHz, the MOSFETs were switched off midway through each 195μs on-interval to permit any flux imbalance to dissipate into primary and/or secondary circuitry through flyback action. This was achieved by running the 74LS123 multivibrator at 10 kHz, with a 4.5% duty cycle at "A" and "B" (figure 3.4).

Two cascaded 74LS74 flip-flops were used to divide this down to 2.5kHz, outputting a square wave and its inverse at "C" and "D". The square waves were then ANDed with the clock (and inverted clock) to produce 4.5μs break-before-make gaps and 4.5μs mid-pulse gaps in the complementary drive waveforms at "E" and "F". These waveforms are shown in figure 3.5, together with the plot of expected core flux vs. time.

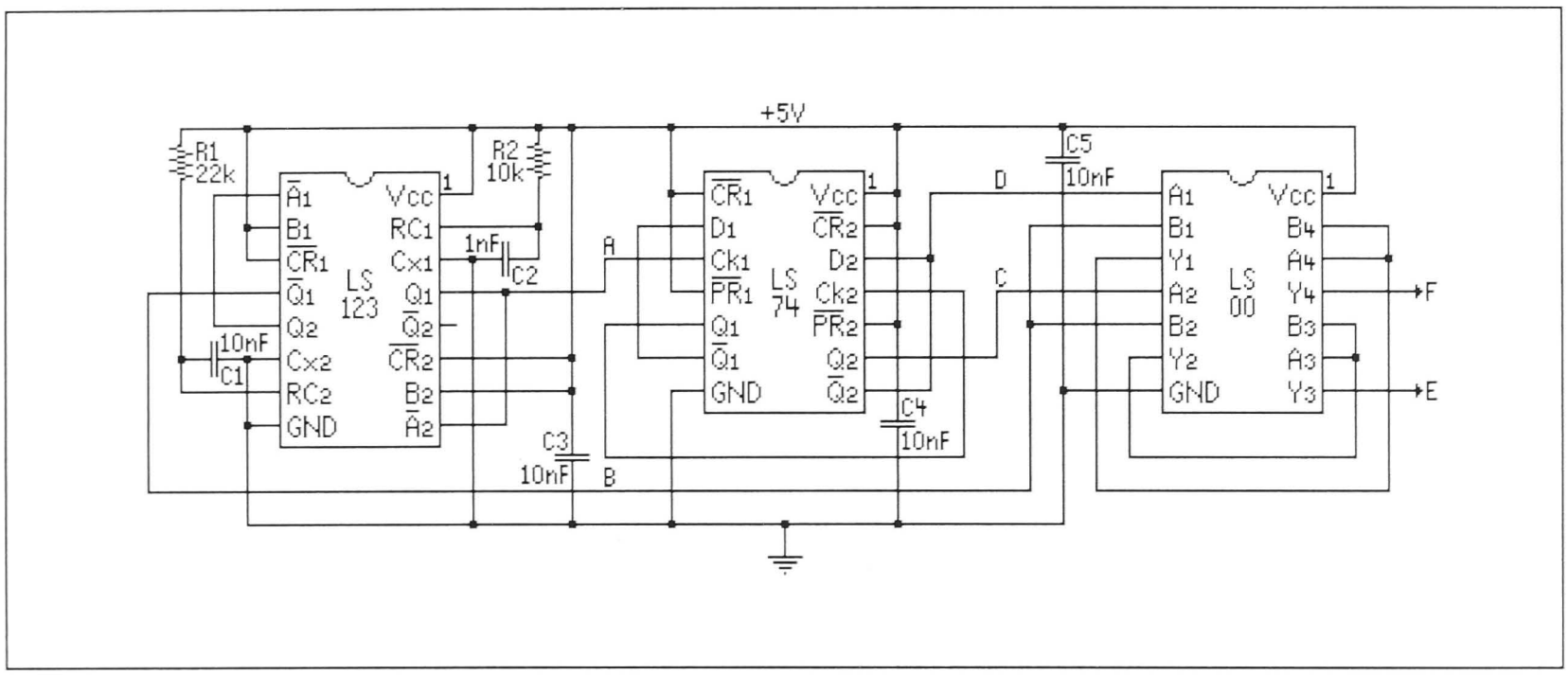


Figure 3.4 Antisaturation drive waveform generator.

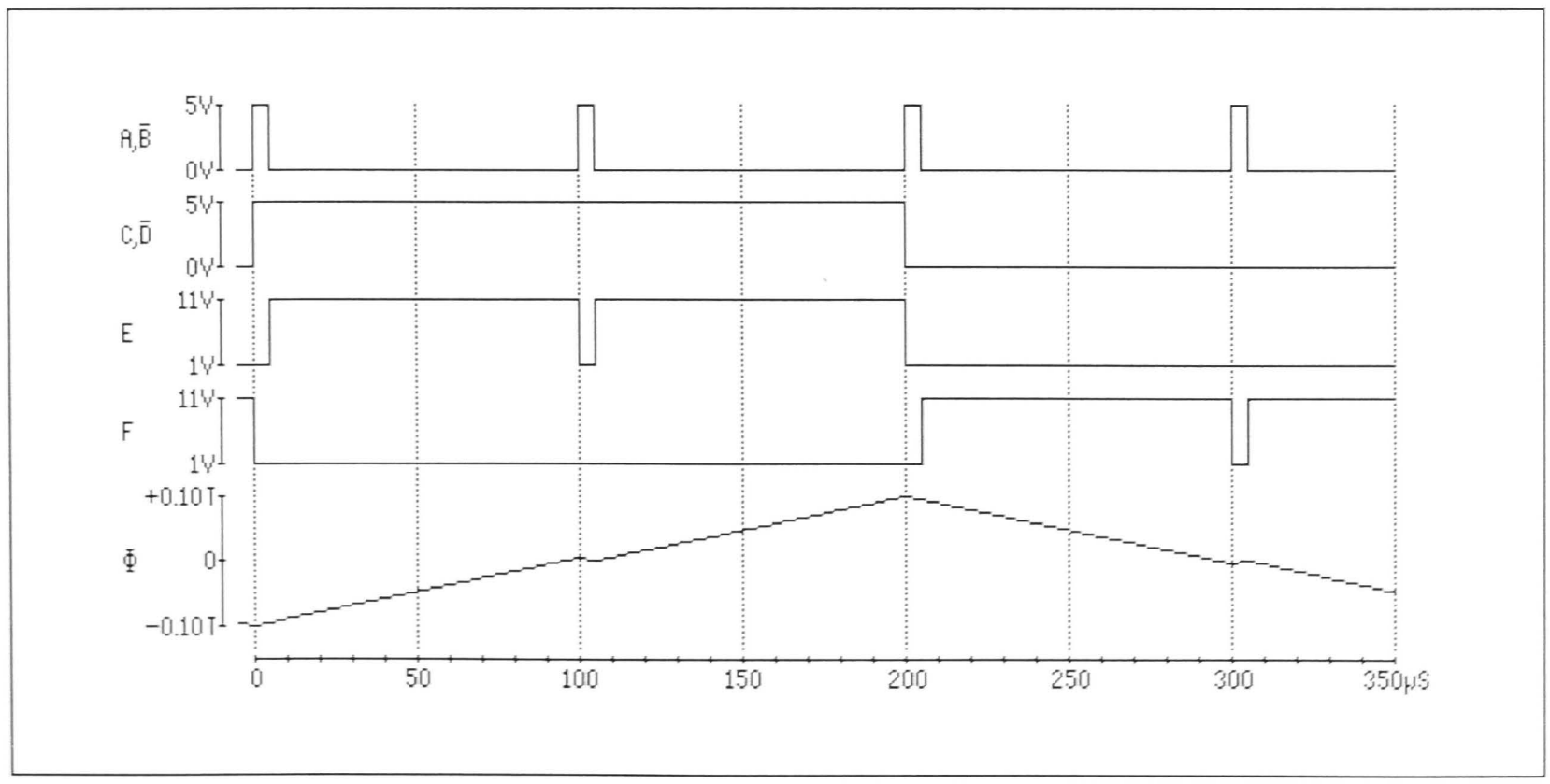


Figure 3.5 Antisaturation drive circuit and core flux waveforms.

Apart from the extra divide-by-two stage and the change in timing capacitors, the antisaturation drive circuit is otherwise identical to the waveform generator currently in use (Section 3.3).

Except at very low input current levels, leakage inductance prevents load current from resuming its former value until well after the mid-pulse gap. This gives rise to the same reduced drive duty cycle that would have resulted from switching at 5kHz without the gaps. As the leakage inductance induced load current re-start time approaches the effective 95μs drive pulse width, output voltage falls away dramatically, limiting output power to about 25W. This process was exacerbated by the capacitor output filter in use at the time (see Section 3.8). However, it should be noted that no evidence of core saturation (e.g. trailing edge droop on alternate drive pulses) was observed. Following these initial tests, the antisaturation drive gap was removed.

3.8 Inductive output clamp and filter

The LVPC was originally intended to operate into a capacitive output filter. This arrangement is quite common in DC–DC converters generally, but inappropriate in this case. The reason is leakage inductance.

In the absence of leakage inductance, the secondary output circuit is effectively a diode bridge in series with the parallel combination of a resistor (representing the output load) and a 4,700μF filter capacitor. Under "steady state" (mid drive pulse) conditions, the resistor determines the secondary current, and therefore the load component of primary current (that portion exclusive of I_{mag}). The load voltage is held nearly constant by the filter capacitor, which appears to the primary (with $N_s/N_p = 58$) as $0.0047 \times 58^2 = 15.8$F charged to 0.5V in series with an ideal diode. In effect, the diode bridge and filter capacitor look like back-to-back ideal 0.5V zener diodes, as viewed from the primary. If the filter capacitor discharges slightly – as it does during drive reversal – large primary current flows until the capacitor recharges to $58V_p$ volts, after which the primary current returns to $58I_{load}$ amps. When primary drive reverses, reflected load current simply transfers to the other half-primary, and all is well.

However, with primary and secondary leakage inductance present, all is not well. This inductance is effectively inserted between the input and the output, so that when primary drive reverses, primary and secondary current cannot change unless a voltage is developed across both leakage inductances. But this cannot occur as long as the filter capacitor remains charged to $58V_p$, because this appears as 0.5V at the primary. The filter capacitor alone must then supply the load, and as it does its voltage falls, creating the drop needed to reverse current in the leakage inductance. The higher the load current, the more the capacitor must discharge to reverse bias the leakage inductance sufficiently to bring about current reversal, and the longer the process takes. Average output voltage falls, and efficiency suffers.

Removing the output filter capacitor helps. This allows current to reverse in the leakage inductance with a time constant approximated by $(58^2L_{lp} + L_{ls})/R_{load}$. The price for this is excessive output ripple.

A better solution is to use an inductive output filter in place of the capacitor. With this arrangement, the filter inductor keeps load current circulating through the diode bridge whenever secondary current is insufficient, such as during drive reversal. Under these conditions, all four bridge diodes become forward biased, which clamps the voltage at the bridge input (and therefore V_s) to zero. With V_s effectively shorted, the full input voltage is applied across the leakage inductance, so current can reverse and return to steady state levels in the minimum possible time. In fact, measuring the resulting clamp interval, t_{clamp}, is a convenient means of estimating total leakage inductance (see Section 5.2). As soon as secondary current reaches the level flowing in the inductor, the bridge unclamps (normal two diode operation resumes), and the secondary begins to support the load current.

The output filter inductor should be large enough to maintain load current during the longest foreseeable reversal interval – about 100μs. It must also be able to handle 8ADC load current without saturating. If V_{out} is to drop by no more than 10% (e.g. from 25.0 to 22.5V) into a 3Ω load, then $22.5 = 25\ \exp(-100 \times 10^{-6} \times 3/L)$, and L = 2.85mH. A spare E65/32/27 core just happened to be available, so it was used. B_{max} was taken as (a probably rather conservative) 300mT.

At this point a slight digression is required. During the clamp interval, the output filter indictor supports the load current, and V_{out} falls (if the load is resistive). After the clamp interval, the transformer secondary both supports the load and restores current to the output inductor. V_{out} rises during this part of the cycle. Because the average voltage across an (ideal) inductor must be zero, V_{out} must be the average voltage at the output of the bridge rectifier: $V_s \times (0.5\text{ms} - t_{clamp})/0.5\text{ms}$. The output filter inductor behaves like a transformer with an effective turns ratio determined by the clamp interval. (See also Section 6.2.) It should be noted that the voltage drop across the inductor does not imply a power loss, apart from that imposed by the non-ideal factors of copper and core loss.

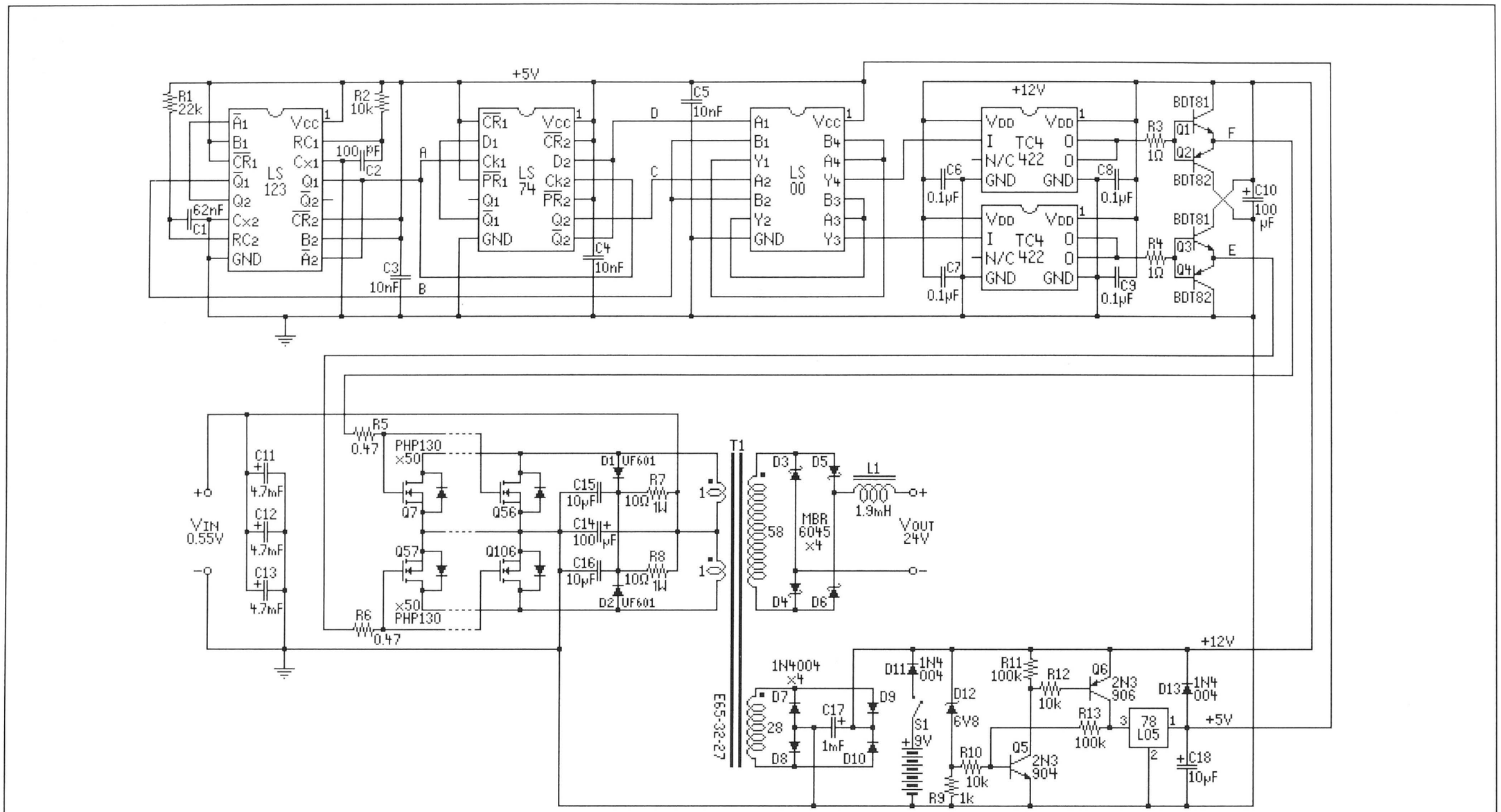
For this core, $L = \mu_e N^2 A_e/l_e = \mu_e N^2(5.35 \times 10^{-4})/0.147 = 2.85\text{mH}$. Also, $B_{max} = \mu_e NI/l_e = \mu_e N \times 8/0.147 = 300\text{mT}$. Simultaneous solution gives $N = 142$ and $\mu_e = 3.88 \times 10^{-5}$. Because the material permeability, $\mu_i = 2.0$ mH/m, an air (or plastic) gap between the core halves will be required. The magnetic circuit can be expressed as

$$l_e/\mu_e = l_m/\mu_i + l_g/\mu_0, \qquad [3\text{–}2]$$

where l_e is the total effective magnetic path length, μ_e is the effective (overall) permeability, l_m is length of the magnetic path in the ferrite, μ_i is permeability of the ferrite, l_g is the (total) length of the air gap, and μ_0 is the permeability in the gap. Assuming l_g will be relatively small, $l_e \approx l_m$, and $0.147/(3.88 \times 10^{-5}) = 0.147/0.002 + l_g/(4\pi \times 10^{-7})$. Therefore, $l_g = 4.67\text{mm}$. Because the EE core sections are to be spaced apart, each line of flux must pass through two gaps, so a non-ferromagnetic spacer of 2.33mm thickness would be required.

With 142 turns, the largest wire which will fit the bobbin is 1.25mm. The resistance of 142 turns of 1.25mm diameter wire would be $(1.73 \times 10^{-6})(142)(15.1)/(0.0123) = 302\text{m}\Omega$, which would drop 2.42V and dissipate 19.33W at 8A. As this represents an additional 9.7% power loss, it was decided that fewer turns should be used. If the above calculations are repeated with the assumption that a 20% voltage drop in V_{out} can be tolerated, $L = 1.34\text{mH}$, $N = 67$, and $l_g = 2.15\text{mm}$. The resistance of 67 turns of 1.5mm wire should be $99\text{m}\Omega$, giving a more reasonable power loss of 6.34W.

Upon winding the coil, it was discovered that 68 turns in three layers was a good, tight fit. This is an advantage mechanically, as it helps to hold the turns in place. The increase to 68 turns called for an l_g of 2.19mm, requiring a 1.09mm spacer. Two thicknesses of plastic were used. As wound, the coil specifications are L = 1.91mH, Q = 97, and R = 124mΩ. The increase in inductance probably indicates that μ_i is actually higher than 2.0mH/m (the expected variation would be about ±25%), or that the spacers may have compressed somewhat after assembly. However, the extra inductance is welcome in this application.



EXCEPT AS NOTED:

1. ALL RESISTORS 1/4W 5%
2. ALL CAPACITORS 10%
3. VOLTAGES ARE NOMINAL

TITLE: LOW VOLTAGE POWER CONVERTER
DRAWN: M. SHEPARD
DATE: 04-03-03

4 DC Power Supply Design

4.1 Introduction

The LVPC is designed to operate from a parallel array of silicon photovoltaic cells with a combined output of about 450A at 0.5 to 0.6VDC. However, because such an array would be of no practical use without a suitable power converter, none exists (at least not within the FEIT Department of Engineering). A power source with the above specifications would therefore be required during the development of the LVPC. A commercial DC power supply, if available, would have been prohibitively expensive, so a 500A, low voltage regulated DC power supply was designed and constructed as part of this project.

4.2 Fast settling, high current linear regulator

The following circuit descriptions refer to the 500A DC Power Supply schematic diagram which appears at the end of this section. A complete List of Materials for this power supply is given in Appendix II.

Because this DC supply was intended for a single purpose of limited duration, cost rather than electrical efficiency was considered the primary concern. For this reason, the design was based on a linear regulator operating from a pair of 2V lead-acid batteries with a parallel capacity of 1200 ampere hours. (As a point of interest, 2.4 kWhr of lead weighs 70kg.)

The design incorporates a series-pass regulator comprising four 250A SGS-Thomson STE250N06 power MOSFETs (Q1 – 4) in semi-parallel source follower configuration. Each FET operates within its own moderate gain, high bandwidth local feedback loop. The four FET outputs are then summed to form a common supply bus, the voltage of which is regulated by means of an outer control loop which provides a reference voltage to the individual FET drivers. In this way, recovery from short duration transients can be very rapid, without the need for high gain bandwidth product (with its attendant stability problems) in the main voltage feedback loop.

Battery voltage is applied directly to the common drains of the power MOSFETs, while the remainder of the control circuitry operates from separate ±12VDC supplies. The source voltage of each MOSFET is compared with reference level V_{ref}. The difference is then amplified by a Harris HA-2842 high bandwidth, high current op-amp and applied to the associated FET gate. In this way, the source voltages of all four FETs remain nearly equal, despite variations in their individual gate-source voltage requirements. The output currents from the four sources are then combined by means of 0.5mΩ source resistors (R1 – R4). These are constructed from 0.9 × 12.5 × 326mm folded copper ribbon and are designed to dissipate up to 10W each. The 100Ω gate resistors (R13 – R16) act in combination with C_{rss} to preserve stability by rolling off loop gain above 1.6 MHz, while the 22nF gate-source shunt capacitors (C1 – C4) limit control loop overshoot which can result from positive voltage spikes on the output.

Current from the source resistors is summed at the common output point, V_{out}. Output voltage is used to establish the FET controller reference level, V_{ref}, through feedback provided by an LM-741 op-amp. Bandwidth of this outer control loop is limited to about 16kHz by a 1nF capacitor (C24) in parallel with the 10kΩ feedback resistor (R19) at the LM-741 output. Output voltage can be adjusted over a range of about 0 to 1V by means of a potentiometer (R23) connected to the non-inverting input of the LM-741.

The output impedance of the individual MOSFET stages will be the sum of source impedance plus source series resistance. Effective source impedance is $1/(g_{fs} \times$ gate feedback gain), or about 0.5mΩ. Therefore, each FET stage appears as 1.0mΩ with respect to V_{ref}. The overall output impedance of the power supply should be the parallel impedance of the four MOSFET stages (250μΩ) divided by the gain of the outer control loop (10), or about 25μΩ. However, the effective output impedance will be much greater due to conductor and connection resistance.

Response time of the completed power supply was tested by injecting a ±50mA, 7ns rise time current square wave at the output. With V_{out} set at 0.50VDC, output deflections of ±500mV were induced. Settling times were: within ±50mV (10%) in

70ns, within ±25mV (5%) in 200ns, and within ±10mV (2%) in 300ns. With the substitution of a ±50mA sinusoidal current, the output remained within ±25mV at 600kHz.

4.3 Parasitic inductance

The physical dimensions of the battery, power supply and converter require that significant lengths of copper be used to interconnect them. Flat copper strips of $27mm^2$ cross section are used for most conductors. The total length of the shortest achievable current loop is about 850mm which, if perfectly circular, would be expected contribute an inductance of about 450nH.

Power supply conductor loop inductance resists rapid changes in power supply current, giving rise to voltage transients similar to those produced by transformer leakage inductance, but larger. Paralleling conductors carrying opposing currents would have helped, but was not practical given the distributed arrangement and large physical size of the components. The best solution was to place three large, low ESR capacitors (4,700μF, 15mΩ) across the LVPC input. These act to absorb transient energy spikes during LVPC off intervals, thereby keeping the supply voltage relatively constant. However, short duration (0.5μs) voltage transients of up to +13V are observed across these input capacitors. Other arrangements were tested (additional capacitors, Schottky diode clamps, balancing inductors, etc.), but any possible improvements were negated by the additional inductance present in the interconnecting wires. Longitudinal potential gradients of 1V/cm were routinely observed along conductors, consistent with a di/dt of 100A/μs in 10nH/cm wire inductance.

4.4 Thermal management

At maximum design output, the regulator will drop about 1.4V at 500A. Therefore 700W must be removed, principally from the MOSFETS. $R_{ds}(on)$ is about 16.7μΩ/°K at the junctions of each of the four FETs, or effectively 4.2μΩ/°K for the parallel combination. Regulation will be lost if $I_{ds}R_{ds}(on)$ exceeds about 1V, but this should not occur if junction temperature remains below a conservative 125°C. With a parallel

junction-to-case thermal resistance of 0.08°C/W, the case temperature should not be permitted to exceed 69°C. Room air temperatures of up to 35°C are not uncommon, so a case to ambient thermal resistance of 0.05°C/W would have been required. Such a low thermal resistance is impractical in air. However, at the C/2.4 rate the battery can only remain above 1.8V for about 20 minutes, so a total of about 700W × 1200s = 840kJ must be removed. This can be accomplished by melting 2.5kg of ice. An open topped box of 6 litre capacity was constructed using 10mm aluminium plate, with the four power MOSFETs mounted directly to one side. While a mix of 3kg crushed ice and 2 litres of water should maintain the box temperature near 0°C for 20 minutes, cold water alone was used successfully for most test runs.

The completed power supply has been in operation for two years, routinely delivering currents of up to 300A. On one occasion the output was inadvertently short circuited, with an estimated 2000A flowing for about 10 seconds. No damage resulted, although the magnetic field created was observed to deflect the beam off screen on a nearby oscilloscope.

4.5 Photovoltaic array equivalence

Below about 1.6kHz, the 500A DCPS can be approximated by an ideal voltage source in series with a resistor. This supply has a theoretical output impedance of 25μΩ (see Section 4.2), but 850mm of 27mm^2 copper is required to connect it to the LVPC. Of this, about 300mm is outside the voltage-sense feedback loop. Therefore, an interconnection resistance of 192μΩ must be added to the output impedance, giving a 0.217mΩ total. While this means the supply will be a bit "spongy" at 500A, the resistive voltage drop at 131A (where the LVPC output is 54W) is only 28mV, or 5% of 0.55V.

A parallel solar array can be modelled as a current source in parallel with a forward biased diode junction, so at first glance it may seem that the wrong design was chosen for the power supply. However, inspection of Table 2.1 reveals that V_{out} remains between 0.68V and 0.50V as I_{out} is increased from zero to 0.69A/cm^2, or 98.6% of the short circuit output current. If I_{out} is increased from 0.69 to 0.70A/cm^2 the voltage

collapses towards zero and the cell begins to approximate a current source, but for most of the region of interest a voltage source is the better approximation.

From Section 2.1, the expression for the V/I curve of a $1cm^2$ solar cell operating under 20 suns is

$$V_f = (nkT/q)\ln(I_f/I_o) = 0.0287\ln(I_f/3.591 \times 10^{-11}). \qquad [4-1]$$

About $730cm^2$ would be required for a 250W parallel solar array, so its V/I curve would be described by $V_f = 0.0287\ln(I_f/2.621 \times 10^{-8})$. However, the slope of the V/I curve is $0.0287/I_f$, irrespective of cell area. For best efficiency, $V_{out} = 0.55V$, which places V_f at about 0.60V (Table 2.1). At this voltage, $I_f = 0.043A/cm^2$, or 31.4A for a $730cm^2$ parallel array. Therefore, cell output impedance, dV_f/dI_f, will be 0.0287/31.4, or 0.914 mΩ at this operating point. Of course, the impedance will change as one moves along the V/I curve, becoming 0.226mΩ at $V_f = 0.64V$ and 3.676mΩ at $V_f = 0.56V$, corresponding with array outputs of about 0.60V and 0.50V, respectively. Finger resistance would be expected to contribute an additional 0.1 mΩ to these impedance values. Estimated performance curves for a $730cm^2$ cell are given in figure 4.1.

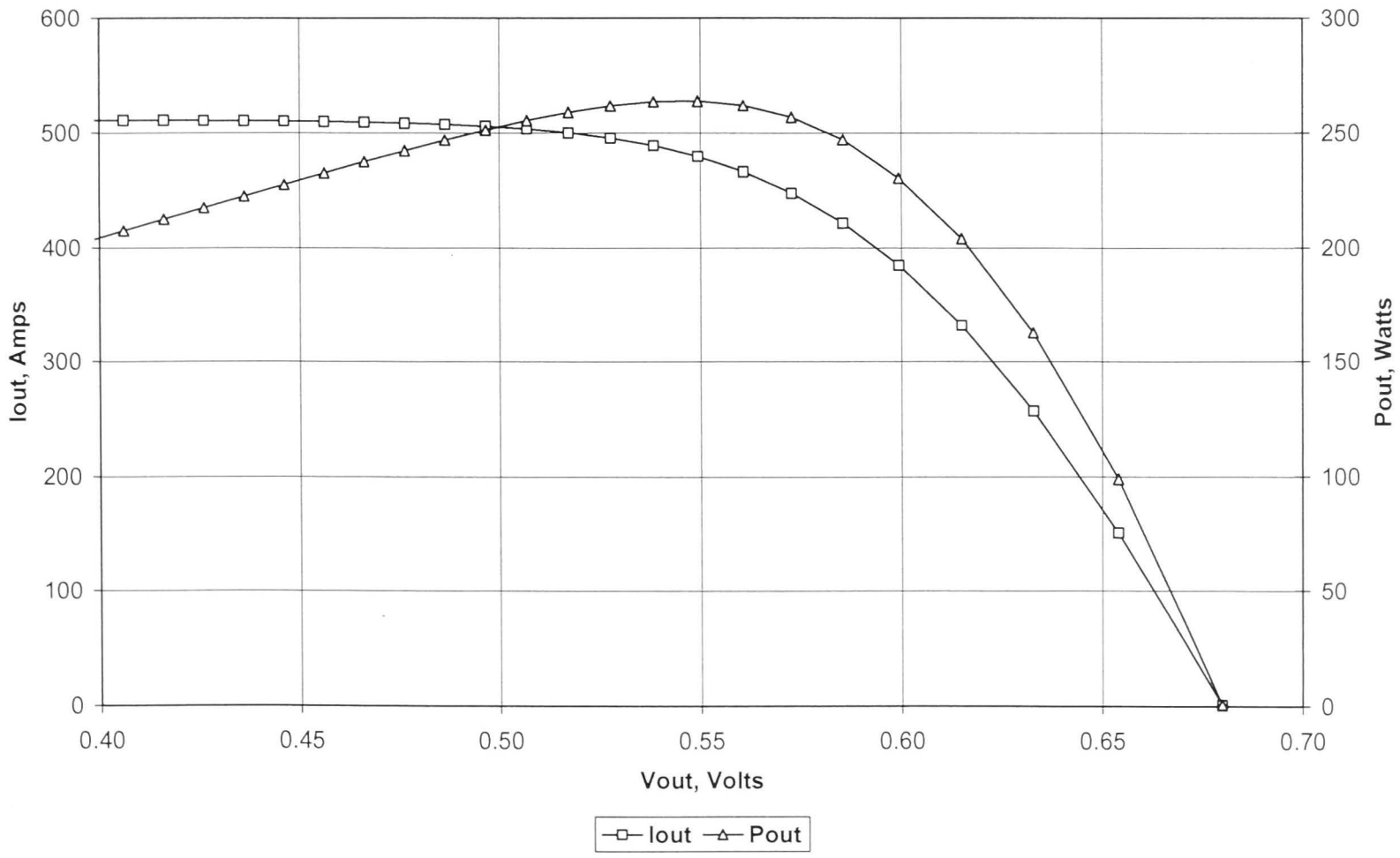
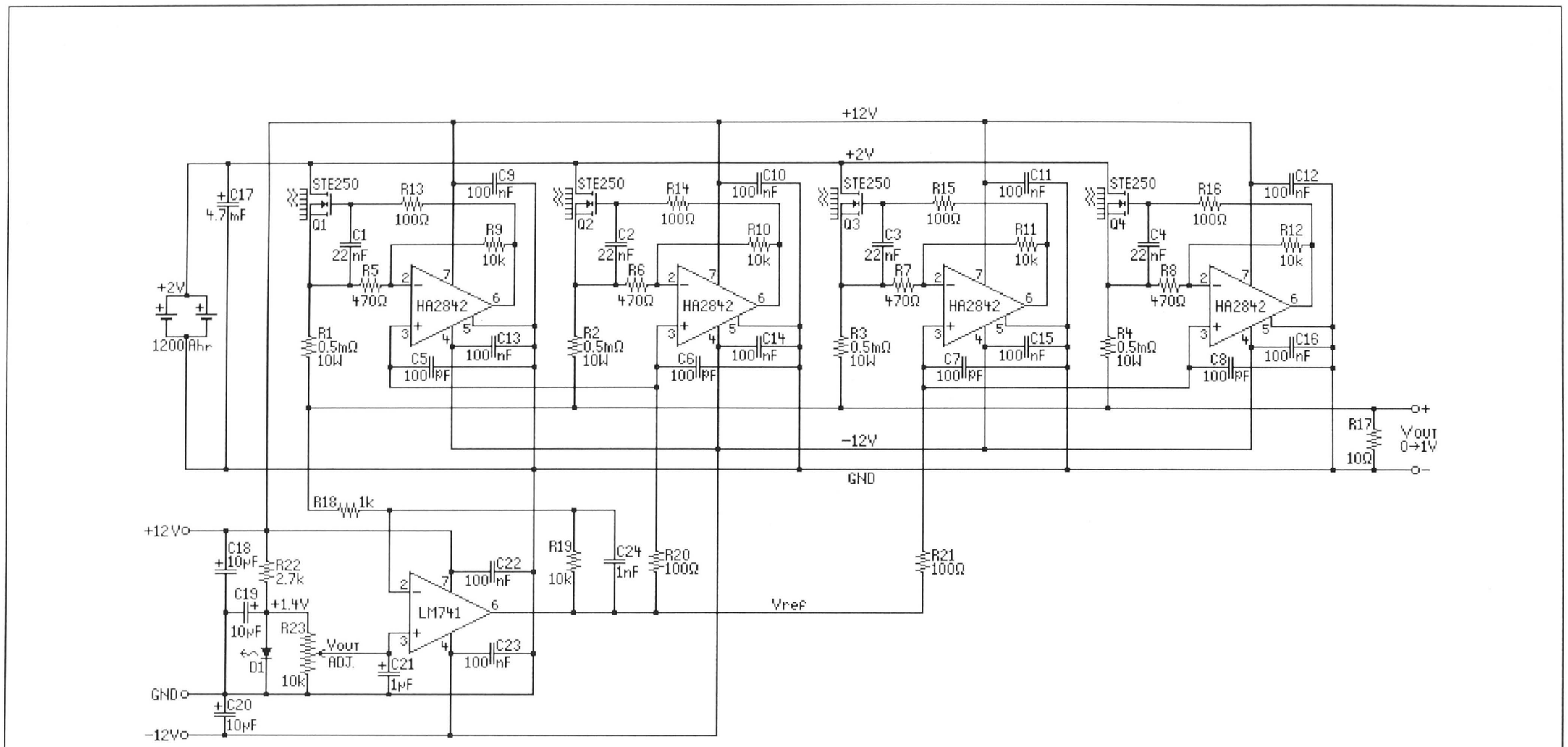


Figure 4.1 Characteristics of a $730cm^2$ cell at 20 suns.

Because of its relatively high output impedance, the solar array is a poor voltage source. This is particularly true on the constant current side of the power curve. The LVPC output is unregulated, so its output V/I curve will have the same basic shape as that of the solar array, but scaled by the effective turns ratio. If the converter is loaded too far beyond the knee of the V/I curve (i.e. $V_{in} \leq 0.3V$), primary drive circuit voltage will fall to the point where operation ceases. Circuitry could be added to delay this by reducing converter output voltage by the amount required to keep V_{in} from falling below 0.50V.

It would also be relatively simple to regulate the LVPC output by means of primary drive duty cycle control, but regulation would only serve to accelerate the collapse of V_{out} as V_{in} slid down the current source side of the array power curve. (Any form of switching regulation would also decrease efficiency by increasing RMS current. Linear regulation would be even worse.) In the end, no amount of clever circuitry can change the fact that the array cannot deliver more than its maximum power.



EXCEPT AS NOTED:

1. ALL RESISTORS 1/4W 5%
2. ALL CAPACITORS 10%
3. VOLTAGES ARE NOMINAL

TITLE: 500A DC POWER SUPPLY
DRAWN: M. SHEPARD
DATE: 05-03-03

5 Results

5.1 LVPC operating characteristics

The LVPC was originally intended to operate at an output power of 200W with an efficiency of 80%. This was not achieved. There are many reasons for this, the most important being a failure to anticipate the detrimental effects of stray and leakage inductance, and the consequent inappropriate selection of transformer core material (see Sections 3.5 and 7.3). However, respectable efficiency (≈75%) was achieved at output power levels up to about 50W, and a peak efficiency of 88% was recorded at 20W. Although the converter was not specifically designed to operate with inputs below about 0.5V, the device continues to function at voltages as low as 0.3V. Still lower inputs would probably be practical if the auxiliary transformer winding was provided with the extra turns needed to maintain the drive circuit power supply.

Table 5.1 summarizes the test results for the Low Voltage Power Converter, while figure 5.1 shows how output power, efficiency and output voltage vary with input power at a fixed input of 0.55V. Test conditions were as follows:

Transformer core	Philips 3C90
Output inductor core	Neosid F5
Load resistance	Iskra 2.5A potentiometer ($105\Omega \geq R_{out} \geq 30.0\Omega$)
	Fixed 100W power resistors ($20.0\Omega \geq R_{out} \geq 3.9\Omega$)
Power source	500A DC power supply (2V battery with water cooled adjustable linear regulator)
Interconnections	Battery to LVPC and Battery to DCPS freshly cleaned
Test equipment	Fluke 87 DMM (voltage and resistance measurements)
	Good Will GW037 current clamp (current measurements)
	Tektronix 2232 oscilloscope (time measurements)

Table 5.1 LVPC Test results.

Vin, V	Iin, A	Pin, W	Vout, V	Rout, Ω	Iout, A	Pout, W	Eff'y, %	tc1, µs	tc2, µs	(Ii-2)/Io
0.50	16.9	8.5	27.5	105	0.26	7.2	84.7	4.0	4.5	57.2
0.55	18.6	10.2	30.4	105	0.29	8.8	85.4	4.0	4.5	57.6
0.60	20.3	12.2	33.1	105	0.31	10.4	85.4	4.0	4.5	58.2
0.50	32.3	16.2	26.6	49.9	0.53	14.2	87.5	8.5	9.0	56.9
0.55	35.7	19.7	29.3	49.8	0.59	17.3	87.9	8.5	9.0	57.2
0.60	39.0	23.5	32.1	49.8	0.64	20.7	88.2	8.0	8.5	57.4
0.50	50.0	25.1	25.6	30.1	0.85	21.8	86.7	13.0	14.0	56.4
0.55	55.1	30.3	28.1	30.0	0.94	26.4	87.0	13.0	14.0	56.6
0.60	59.9	35.9	30.7	30.0	1.02	31.5	87.5	13.0	14.0	56.5
0.50	70.2	35.2	24.3	20.2	1.20	29.2	83.1	19.0	20.5	56.7
0.55	77.6	42.8	26.8	20.2	1.33	35.6	83.3	18.5	20.5	56.9
0.60	84.6	50.8	29.2	20.2	1.45	42.3	83.4	18.5	20.5	57.1
0.50	95	47.4	22.7	14.0	1.62	36.7	77.4	26.0	29.0	57.4
0.55	105	57.6	25.0	14.0	1.79	44.8	77.6	26.0	29.0	57.6
0.60	114	68.5	27.3	14.0	1.95	53.3	77.8	25.5	29.0	57.6
0.50	118	59.0	21.1	10.1	2.09	44.2	74.9	33.0	37.0	55.6
0.55	131	72.1	23.4	10.1	2.31	54.1	75.1	33.0	37.0	55.8
0.60	143	86.0	25.5	10.1	2.53	64.5	75.1	33.0	37.0	55.9
0.50	153	76.8	19.1	7.0	2.72	51.8	67.5	45.0	50.0	55.6
0.55	169	93.1	21.0	7.0	3.00	62.9	67.5	45.0	50.0	55.7
0.60	185	111.0	22.9	7.0	3.27	75.0	67.6	45.0	50.0	55.9
0.50	181	90.6	17.1	5.3	3.23	55.4	61.1	56.0	64.0	55.4
0.55	200	109.9	18.9	5.3	3.57	67.4	61.3	56.0	64.0	55.4
0.60	219	131.1	20.6	5.3	3.89	80.2	61.2	57.0	64.0	55.6
0.50	201	100.7	15.7	4.4	3.57	55.9	55.6	68.0	78.0	55.8
0.55	222	122.1	17.3	4.4	3.93	67.9	55.6	68.0	78.0	56.0
0.60	242	145.2	18.9	4.4	4.29	81.1	55.9	70.0	78.0	55.9
0.50	218	109.2	14.5	3.9	3.73	54.1	49.6	82.0	92.0	58.0
0.55	241	132.3	16.0	3.9	4.10	65.6	49.6	82.0	92.0	58.3
0.60	265	159.3	17.5	3.9	4.48	78.4	49.2	83.0	92.0	58.6

Notes

1. V_{in}, I_{in}, V_{out}, R_{out}, t_c1 and t_c2 are measured values. All other values are calculated from these.
2. DMM probe resistance of 0.2Ω has been subtracted from all R_{out} values. (e.g. 10.1Ω indicates an initial reading of 10.3Ω.)
3. t_c1 and t_c2 (t_{clamp1} and t_{clamp2}) are the intervals during which the output bridge clamps the transformer secondary to zero volts.
4. (I_i-2) is I_{in} minus the approximate load-independent current used by the transformer core and FET drive circuit. (I_i-2)/I_o therefore approximates the effective input to output current transfer ratio of the LVPC.

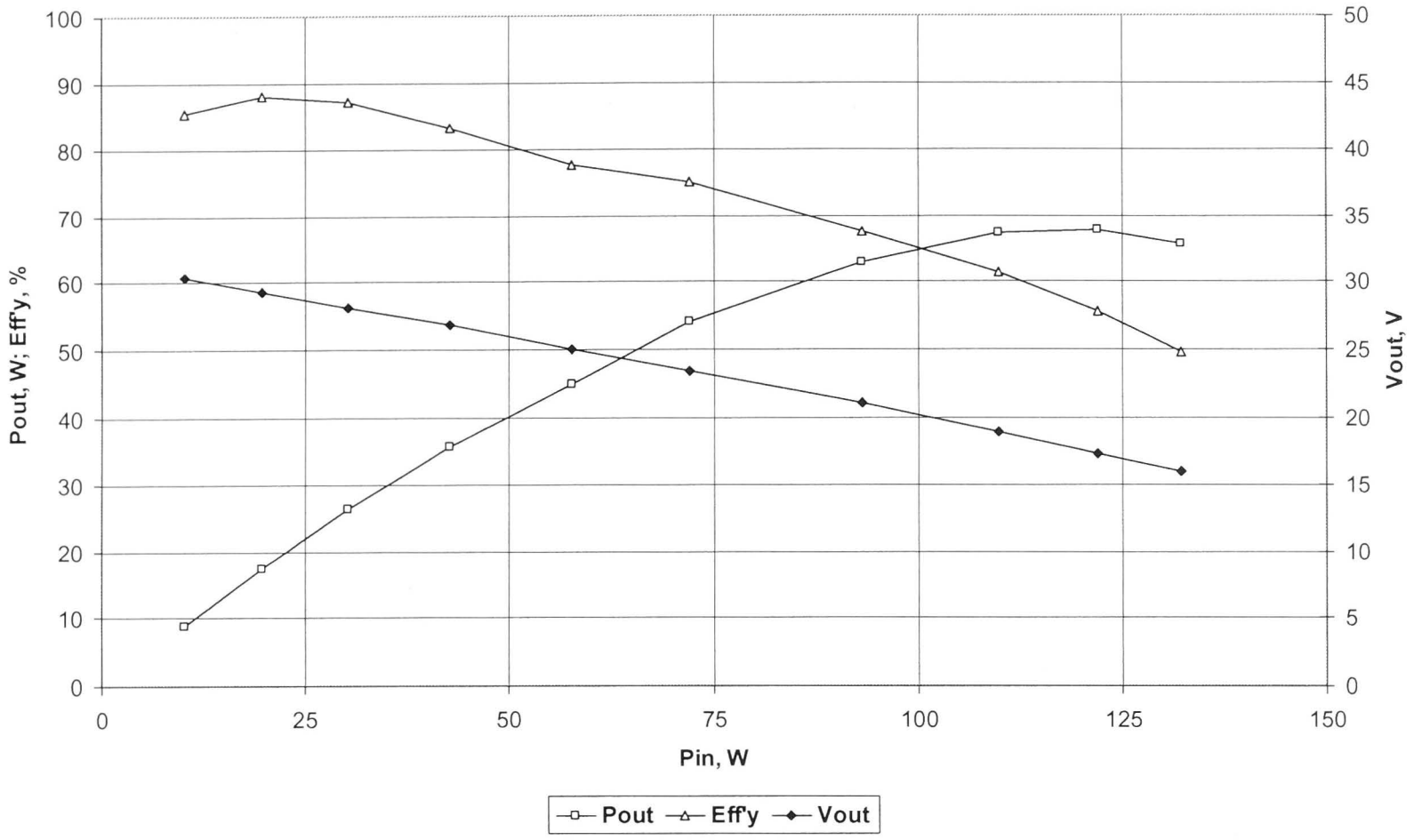


Figure 5.1 Variation of LVPC output power, efficiency and voltage with input power.

Inspection of Table 5.1 and figure 5.1 suggests that an output of 60 or 65W may be the practical upper limit for the LVPC. Beyond this point, output power does not increase significantly with increasing load. An even lower limit would apply at an input of 0.5V. Because this is well below the design limit of 200W, all sources of loss were carefully examined to determine the cause of the unexpected result. Operating conditions of P_{out} = 54.07W with V_{in} = 0.550V were selected for this evaluation. At this operating point, P_{in} = 72.05W, so 17.98W is lost within the converter. Identifiable losses are determined below.

Input filter capacitors – 3.71W (5.1% of P_{in})

Current, and therefore power, in the input capacitors can be inferred from the AC component of input voltage. The actual waveform is a complex curve, but a reasonable approximation can be made by representing it as three triangles. As the MOSFETs switch, V_{in} rises rapidly by 0.21V, then returns to 0.55V in about 40μs. Next, V_{in} falls by an additional 0.06V in another 40μs. Finally, V_{in} returns to 0.55V during the next 100μs. The slopes of $V_{in}(t)$ during these three intervals are 5250, 1500, and 600V/s, respectively.

There are three 4,700μF input filter capacitors connected in parallel, giving a total of 14.1mF. Capacitor current will be Cdv/dt, or 74.0, 21.2, and 8.5A during the three intervals, giving an RMS ripple current of: $\sqrt{[(40/500)(74.0^2) + (40/500)(21.2^2) + (100/500)(8.5^2)]} = 22.1A_{rms}$. The filter capacitors have a specified effective series resistance of 15mΩ each, or 5mΩ for the parallel combination, and they are connected to the input terminals with wire which contributes an additional 2.6mΩ. The input filter capacitors should therefore dissipate $22.1^2 \times 7.6 \times 10^{-3} = 3.71W$.

Drain and source bars – 1.37W (1.9% of P_{in})

The transformer primary is supplied by machined copper bars of $2.72cm^2$ cross sectional area and 27.0cm length. Neglecting skin effect, their combined resistance would be 34.3μΩ. However, with conductors of this size skin effect will be noticeable. Penetration depth in millimetres, $\Delta = k_m/\sqrt{f}$, where $k_m = 66$ at 25°C (Billings [1]). At f = 1kHz, $\Delta = 2.1mm$. For the 12.7 × 21.4mm bars, the effective cross sectional area is $1.26cm^2$, so their actual combined resistance should be 74.1μΩ.

Average input current is 131.0A. However, current ramps up during the ≈35μs clamp intervals, so the RMS current will be higher. The assumption that I_{in} rises from 0.0 to 135.8A in 35μs, then remains at 135.8A for 465μs, is consistent with $I_{in} = 131.0A_{avg}$.

It will later be shown (see Section 5.2) that magnetising current, I_{mag}, is a 19.1A triangle wave, with an average value of zero. This waveform is superimposed on I_{in}, producing a current waveform which rises from −19.1A at t = 0μs to +119.4A at t = 35μs, and then to +154.9A at t = 500μs. However, the single section approximation $i(t) \approx \pm[116.7 + 38.2t/(500 \times 10^{-6})]A$ is accurate enough for loss estimation. The RMS value of this waveform is $\sqrt{[(1/500\mu s)\int i(t)^2 dt]} = 136.2A_{rms}$. With $I_{in} = 136.2A_{rms}$, power loss in the drain and source bars should be $136.2^2 \times 74.1 \times 10^{-6} = 1.37W$.

Input connections – 0.71W (1.0% of P_{in})

The input connections consist of copper bars bolted together. The negative input also passes through an additional connection made by a heel-plate which is screwed to the source return bars. All are dry joints between bare copper surfaces, the area and resistance of which are difficult to determine. At $I_{in} = 131.0A$ there appears to be a

small drop across each connection, but it is very sensitive to probe position, and therefore difficult to measure with confidence. If 5mV is taken as the combined voltage drop across all three connections, then $R_{con} = 0.005/131.0 = 38.2\mu\Omega$, giving a power loss of $136.2^2 \times 38.2 \times 10^{-6} = 0.71$W.

MOSFET R_{ds}(on) – 1.86W (2.6% of P_{in})

The MOSFETs have a specified R_{ds}(on) of 5mΩ, giving a parallel combination of 100μΩ for each bank of 50. With $I_{in} = 136.2A_{rms}$, resistive power loss in the FETs should be $136.2^2 \times 100 \times 10^{-6} = 1.86$W.

MOSFET switching – 2.79W (3.9% of P_{in})

During the 0.5μs t_{off} switching interval, the MOSFETs experience a leakage inductance driven V_{ds} transient of about 36V. Assuming a linearly falling I_{ds} current ramp, switching energy, $W_{sw} = V_{ds}I_{ds}(max)t_{off}/2 = (36)(154.9)(0.5 \times 10^{-6})/2 = 1.394$mJ. With two t_{off} transitions per cycle and a drive frequency of 1kHz, MOSFET switching consumes $2000 \times 1.394 \times 10^{-3} = 2.79$W.

MOSFET reverse diodes – 0.08W (0.1% of P_{in})

During the 0.5μs t_{on} switching interval, reverse diodes on the MOSFET substrates become forward biased to about 1V and conduct the 154.9A leakage inductance driven primary current. This current should decrease linearly to nearly zero as leakage inductance discharges (see Section 5.2), so reverse diode energy, $W_{rd} = V_f I_{ds}(max)t_{on}/2 = 38.7\mu$J. With two t_{on} transitions per cycle, the reverse diodes dissipate $2000 \times 38.7 \times 10^{-6} = 0.08$W.

MOSFET sockets – 2.23W (3.1% of P_{in})

Sockets on the MOSFET source and drain connections were initially thought to contribute about 5mΩ per transistor. Measurements at $I_{in} = 132$A and $I_{in} = 202$A revealed drops between the drain and source bars of 27mV and 40mV respectively, giving a parallel combination of 200μΩ for each bank of 50. Subtracting 100μΩ for R_{ds}(on) gives 100μΩ for the connectors (or 5mΩ per transistor). However, subsequent tests gave $V_{ds} = 35$mV (bar to bar) at $I_{ds} = 139$A, implying 7.6mΩ contact resistance per

transistor. Taking an average value of 6mΩ gives 120μΩ for each bank. With I_{in} = $136.2A_{rms}$, power loss in the sockets should be $136.2^2 \times 120 \times 10^{-6} = 2.23W$.

Snubber circuit – 0.55W (0.8% of P_{in})

Ideally, during t_{off} the snubber diodes should divert most of the leakage inductance driven primary current into the two 10μF holding capacitors (see Section 3.3), keeping V_{ds} at a safe level. However, because the snubber was added after initial LVPC construction, it is physically located near the input terminals. These are up 250mm from the switching FETs at the transformer end of the connection bars. Also, the 0.8mm pin sockets limit snubber drain connections to small diameter wire of high resistance and inductance. As a result of these deficiencies, V_{ds} transients reach 36V while the holding capacitors charge to only 5.8V. They then discharge to 0.6V through the two parallel 10Ω snubber resistors. The capacitors are therefore charged by 5.2V during each t_{off} transient. Snubber energy, $W_{sn} = ½C(V_2^2 - V_1^2) = 0.5(20 \times 10^{-6})(5.8^2 - 0.6^2) = 333\mu J$. With two t_{off} transitions per cycle, the snubber capacitors should transfer $2000 \times 333 \times 10^{-6} = 0.67W$ to the snubber resistors and 0.55V input.

Voltage on the holding capacitors decays exponentially through the snubber resistors with an average current of $20\mu F \times 5.2V \times 2000Hz = 0.21A$. Therefore, power returned to the 0.55V input through these resistors is only $0.21A \times 0.55V = 0.12W$, giving a net power loss of 0.55W.

Transformer primary – 0.77W (1.1% of P_{in})

With a cross sectional area of $0.93cm^2$ and a length of 15.1cm, the DC resistance of each half-primary would be 28.1 μΩ without skin effect. But with a penetration depth of 2.1mm (see "Drain and source bars" above), the effective cross sectional area of the $10.0 \times 9.3mm$ windings is only $0.63cm^2$. The resistance of each half primary will be 41.5μΩ. At I_{in} of $136.2A_{rms}$, power loss in the primaries should be $136.2^2 \times 41.5 \times 10^{-6}$ = 0.77W. That is, each half-primary will dissipate 0.38W.

Transformer core – 0.44W (0.6% of P_{in})

Philips E65/32/27 core sets in 3C90 material are specified as dissipating ≤9.1W at 25kHz when B_{max} = 200mT and T = 100°C. However, actual core conditions are f =

1kHz, B_{max} = 241mT, and T = 25°C. Neglecting the effect of temperature, and assuming power will vary linearly with frequency and flux density, $P_{fe} \leq 1/25 \times 241/200 \times 9.1 =$ 0.44W. Core loss should be somewhat lower at 25°C. However, incipient saturation effects evident in the secondary voltage waveform imply a DC bias, and therefore higher B_{max}, so 0.44W will be assumed.

FET drive circuit – 0.61W (0.8% of P_{in})

Gate charge is about 2.85μC per bank (see Section 3.3). With four transitions per cycle, $4000 \times 2.85 \times 10^{-6} = 11.4$mA will be required for switching. This current is supplied to the MOTFET gates through the BDT81 power BJTs. Other drive circuit components have the following current requirements:

TC4422:	$0.2 \times 2 = 0.4$mA
78L05:	3.0mA
74LS00:	1.6mA
74LS74:	4.0mA
74LS123:	12.4mA
Inhibit circuit:	7.0mA

A total of 39.8mA must therefore be supplied by the 28 turn auxiliary transformer winding, which is transformed to 1.11A on the primary. Power for the FET drive circuit is therefore $1.11 \times 0.55 = 0.61$W.

Transformer secondary – 0.47W (0.7% of P_{in})

With a cross sectional area of 0.0177cm^2, and a length of 876cm, the DC resistance of the secondary winding should be 85.6mΩ. Average output current is 2.314A. As in the case of the drain and source bars, secondary current can be assumed to ramp from 0.0 to 2.398A in 35μs, then remain at that level for 465μs. However, unlike the drain and source bars, I_{mag} will have no effect. RMS current will be 2.341A_{rms}, giving a secondary power loss of $2.341^2 \times 85.6 \times 10^{-3} = 0.47$W.

Diode bridge – 1.39W (1.9% of P_{in})

The MBR6045 Schottky diodes carry the average output current of 2.314A. At this current they have a forward voltage drop of 0.30V, so they will collectively dissipate $2 \times 0.30 \times 2.314 = 1.39$W.

Output inductor core – 0.07W (0.1% of P_{in})

The average output voltage is 23.37V. With a resistive load, output voltage will be a falling exponential during the clamp intervals, but negligible accuracy will be lost by assuming a linear change. Therefore, if L = 1.91mH, average di/dt during the ≈35μs clamp intervals should be $V_{out}/L = 23.37/0.00191 = 12{,}236$A/s. This gives a change of 0.428A in 35μs, or ±0.214A around the average output current of 2.314A.

For the output inductor, $L = \mu_e N^2 A_e / l_e = \mu_e 68^2 (5.35 \times 10^{-4})/0.147 = 1.91$mH, so $\mu_e = 113.5\mu$H/m. $B = \mu_e NI/l_e$, therefore B will be 121.5 ± 11.2mT. With the core under DC bias, extrapolation from data sheets is risky at best. However, the flux excursion is low enough such that even a large percentage error will have a very small overall effect. Using the same procedure as was used for the transformer core, but with f = 2kHz due to full wave rectification, and 14.6W for Neosid F5 material, $P_{fe} \leq 2/25 \times 11.2/200 \times 14.6 = 0.07$W.

Output inductor winding – 0.67W (0.9% of P_{in})

As explained above, output current can be approximated as a ±0.214A triangle wave centred at 2.314A. The winding will carry an RMS current of about 2.317A through a resistance of 124mΩ. Therefore, the winding should dissipate $2.317^2 \times 0.124 = 0.67$W.

The total power loss from all identified causes is 17.72W (24.6% of P_{in}), leaving only 0.26W unaccounted for. This discrepancy represents 0.4% of input power, well within the limits of measurement error. Results of the LVPC loss calculations are summarised in Table 5.2. In Section 6 it will be shown that most circuit losses are proportional to the square of input current (and therefore to the square of input power). This causes the significant drop in efficiency seen above about 65W output. An additional consideration is the progressive reduction in output voltage observed at the higher load levels. Part of this loss is associated with simple IR drops throughout the

circuit, while part is due to the fact that the voltage drops across the output filter inductor (Section 6.2) and leakage inductance (Section 6.4) increase with load. The result is a flattening of the output power curve seen in figure 5.1 at about 65W. It therefore appears that an output of 60 or 65W is the upper limit for the converter as designed.

Table 5.2 LVPC Losses at 72W input power.

Source	Loss, W	% of Pin
Input filter capacitors	3.71	5.1
Drain and source bars	1.37	1.9
Input connections	0.71	1.0
MOSFET R_{ds}(on)	1.86	2.6
MOSFET switching	2.79	3.9
MOSFET reverse diodes	0.08	0.1
MOSFET sockets	2.23	3.1
Snubber circuit	0.55	0.8
Transformer primary	0.77	1.1
Transformer core	0.44	0.6
FET drive circuit	0.61	0.8
Transformer secondary	0.47	0.7
Diode bridge	1.39	1.9
Output inductor core	0.07	0.1
Output inductor winding	0.67	0.9

None of these components becomes noticeably warm to the touch following short (<5 min.) periods of operation. Extended (15-20 min.) operation at ~50W output power produces a slight temperature rise in the power MOSFETs and Schottky bridge diodes, while the input filter capacitors become quite warm. The effect of this temperature rise appears to be small, however some reduction in output (~0.1V) was noted following lengthy test runs. A quantitative analysis of the effect of temperature on efficiency was not attempted, although this may become significant at higher power levels.

Table 5.3 lists the resulting performance specifications for the Low Voltage Power Converter. Unless otherwise stated, V_{in} = 0.55VDC and T_a = 25°C. Absolute maximum input voltage, V_{in}(max) = 0.70V.

Table 5.3 LVPC specifications.

Parameter	Desig	Min	Typ	Max	Unit
Input voltage range	V_{in}	0.50	0.55	0.60	V
Output voltage	V_{out}	24.0		31.5	V
Output ripple, P_{out} = 50W	V_{rip}		3.9		V_{p-p}
Ripple frequency			2.0		kHz
Output regulation, 0 to 50W			24		%
Efficiency, P_{out} = 25W			87		%
Efficiency, P_{out} = 50W			76		%
Operating temp. range	T_a	0		40	°C

5.2 Transformer characterisation

In this section, the LVPC transformer will be modelled by the equivalent circuit introduced in Section 2.3. This circuit is reproduced below (figure 5.2) to aid in the discussion which follows. The model will permit the transformer's effect on circuit operation to be characterised in detail in Section 6.2. Some of the variables relating to the LVPC transformer have already been determined, while those remaining will be dealt with now. The results are given in Table 5.4 at the end of this section.

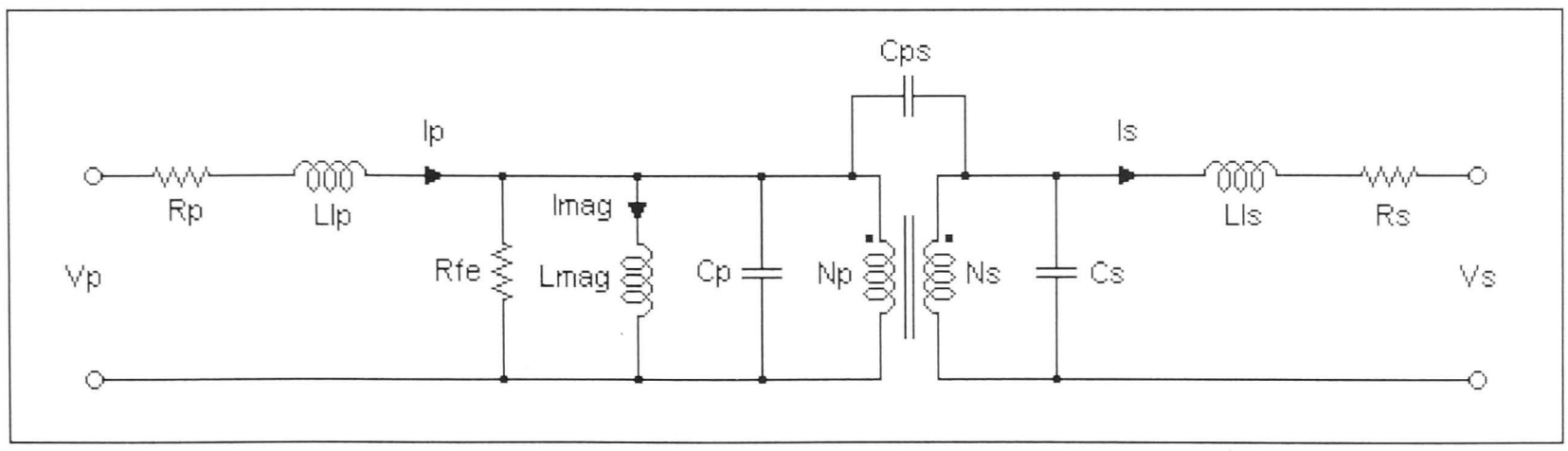


Figure 5.2 Transformer equivalent circuit.

The inter-winding capacitance, C_{ps}, was found to be below the measurement capability of the LCR meter, and will be assumed to be less than 1pF. This result is reasonable because the primary and secondary are separated by about 2mm at their closest point. However, even if the value was much higher, C_{ps} would have no effect on circuit operation because primary and secondary circuits do not share a common reference.

Secondary intra-winding capacitance, C_s, can be determined directly from the resonant frequency of the winding: $f_o = 1/2\pi\sqrt{(L_sC_s)}$. For this test to be effective, the primary winding must be removed from the core to eliminate the effects inter-winding magnetic coupling. No resonance was detected at frequencies up to 10MHz, so the core was removed. The air-cored secondary was then measured with a Topward 5030 LCR meter, and found to have $L_s = 105.0\mu H$ and $Q = 15$ at 10kHz. The secondary was then placed in series with a 50Ω resistor and driven with a 1V sinusoid at frequencies up to 50MHz. The first resonance was observed at 10.6MHz, with others detected at about 19, 29, and 42MHz. Dips in impedance (characteristic of series resonance) were noted, with the impedance at resonance inversely proportional to frequency. Even at the lowest resonant frequency of 10.6MHz, the corresponding value of C_s is only 2.2pF. This value is too small to be significant, particularly as it caused no detectible effects within the bandwidth of the core.

A similar test could not be performed on the primary. The drain-source capacitance of 50 MOSFETs ($\approx$225nF at $V_{ds} = 1V$) is effectively in parallel with C_p, and it would have been impractical to disconnect. However, primary self capacitance would have to be greater than 3.5nF in order for the resonance with L_p to fall within the 1MHz bandwidth of the core material. A smaller C_p would have minimal effect upon transformer operation, while a larger value is highly unlikely, given the mechanical dimensions of the single turn half-primary windings. Therefore, C_p can be neglected.

This transformer model shows only one primary winding, whereas the LVPC transformer has two. However, as only one is conducting at any given time, with each carrying current of opposite polarity (with respect to core flux) on alternate drive cycles,

they may be treated as a single winding carrying currents of opposite polarity on alternate cycles. Each half of the split primary winding does have its own leakage inductance, but these also charge and discharge alternately. It is probable that the difference seen in alternate clamp intervals is due to differences in leakage inductance between the two half primaries.

In the following discussion, it will be assumed that R_p, R_s and all capacitances are small enough, and R_{fe} is large enough, that their effect on inductance computations can be neglected. This simplifying assumption permits the model to be reduced to four elements: Three inductors linked by an ideal transformer. A further simplification can be made by reflecting secondary leakage inductance, L_{ls}, to the primary circuit. This is achieved by dividing it by $(N_s/N_p)^2$, giving an effective inductance of $L_{ls}' = L_{ls}/58^2$ in series with primary leakage inductance, L_{lp}.

L_p and L_s have been measured (at 1kHz) as 7.3μH and 28.5mH, respectively. Similar values were also obtained at 10kHz. It will be shown below that $k = L_{mag}/L_p = 0.99$. Therefore $L_{mag} = 7.2\mu H$. At the end of each drive cycle, the active primary is carrying $I_p = 135.8 + I_{mag}$. (135.8A was determined previously, based upon $I_{in} = 131.0A_{avg}$ and $t_{clamp} = 35\mu s$.) I_{mag} will be approximately $V_p\Delta t/2L_{mag}$, where Δt is the drive pulse width, and $L_{mag} = 7.2\mu H$. (The factor of ½ is required because $\Delta I_{mag} = 2I_{mag}$.) With $I_{mag} \approx 0.55(500 \times 10^{-6})/2(7.2 \times 10^{-6}) = 19.1A$, I_p should be 154.9A.

At this point (the end of each drive cycle), the drive FETs switch off for about 0.5μs, during which time two things happen. Because current in the leakage and magnetising inductances cannot cease instantaneously, some of their energy is dissipated in the MOSFETs and snubber circuit at about 36V. At the same time, the secondary can no longer supply the full load current, so the output inductor forces the diode bridge into the clamped state, driving V_s to zero. This short circuit is transferred to the primary side of the ideal transformer, effectively removing this component from the model. All that remains is L_{lp} in series with the parallel combination of L_{mag} and L_{ls}'. This combination has a total inductance, $L_{tot} = L_{lp} + L_{mag}L_{ls}'/(L_{mag} + L_{ls}')$.

Consideration must now be given to the effects of L_{mag}. Tests conducted without the output filter inductor show that V_s increases with a time constant of about 12μs into a purely resistive output load of 20Ω. This is only a rough estimate because careful examination of the curve reveals a second order response, with $\tau = 12\mu s$ corresponding to the faster exponential. Time constant was observed to increase with decreasing load resistance, suggesting that leakage inductance is the cause. From this data, total series inductance, $L_{lp} + L_{ls}'$, can be estimated as $20 \times 12 \times 10^{-6} = 240\mu H$, referred to the secondary. This becomes $240 \times 10^{-6} \times 58^{-2} = 71nH$ if reflected back to the primary. But $L_{mag} = 7.2\mu H$, so clearly $L_{mag} >> (L_{lp} + L_{ls}') > L_{ls}'$. Therefore, $L_{tot} \approx L_{lp} + L_{ls}'$.

The combined leakage inductance of $L_l = L_{lp} + L_{ls}'$ discharges at 36V for 0.5μs. As the other MOSFET bank switches on, drive polarity reverses. However, leakage inductance may still be driving I_p and I_s in the "wrong" direction, keeping the MOSFET reverse diodes forward biased until gate threshold voltage is reached. These currents must first reverse, and then rise sufficiently to support the full load current, before the output bridge can revert to the unclamped state. Because of the relatively large value of L_{mag}, I_{mag} changes little during the clamp interval. Therefore, at the end of the clamp interval, load current plus I_{mag} (which is now supporting I_p) will have been re-established in the primary. Immediately following t_{clamp}, $I_p \approx -135.8 + I_{mag} = -116.7A$. The total change in I_p is $154.9 - (-116.7) = 271.6A$, part of which ($\Delta I_{p1}$) is brought about at 36V, and part of which (ΔI_{p2}) at 0.55V. During the first 0.5μs: $36 = L_l \Delta I_{p1}/(0.5 \times 10^{-6})$. Then, taking 35μs as the average clamp interval, during t_{clamp}: $0.55 = L_l \Delta I_{p2}/(35 \times 10^{-6})$. With $\Delta I_{p1} + \Delta I_{p2} = 271.6A$, $L_l = L_{lp} + L_{ls}' = 137.2nH$.

Leakage inductance results when a winding generates unlinked flux. The amount of unlinked flux is dependent upon core permeability and the mechanical distribution of turns. Two windings of equivalent mechanical placement on the same core can be expected to have similar amounts of leakage inductance, expressed as a percentage of winding inductance. This ratio is 1 − k, where k is the coupling coefficient. Because primary and secondary windings on the LVPC transformer are similarly sized and symmetrically positioned on the core, it is reasonable to assume that $L_{lp} = L_{ls}' = 68.6nH$. Therefore, $L_{ls} = 58^2 \times 68.6nH = 230.8\mu H$. Also, if $L_p = 7.3\mu H$ and $L_{lp} = 68.6nH$, then $k = 1 - L_{lp}/L_p = 0.99$ and $L_{mag} = kL_p = 7.2\mu H$, as asserted above.

Values for leakage inductance will change somewhat if the actual clamp intervals of 33 and 37μs are taken into consideration. Average drive current should be nearly the same for both drive pulses, or staircase saturation could result. (See Section 5.3.) Therefore the total change in I_p at drive reversal should be 271.6A, as before. Repeating the previous calculations for t_{clamp} = 33μs gives L_l = 133.1μH. Similarly, t_{clamp} = 37μs gives L_l = 141.2nH. It is unlikely that L_{ls}' would change significantly from one half-cycle to the next, so its value should remain as 68.6nH. This leaves L_{lp33} = 64.5nH and L_{lp37} = 72.6nH as the leakage inductances of the two half primaries. The 12% difference between the two L_{lp} values is reasonable, given the non-symmetrical placement of the half primary windings on the core.

Damped oscillation of ≈1.2Mhz appears on the primary at the beginning of each clamp interval. The secondary is effectively shorted at this time, but 1.2MHz is above the core bandwidth, so the short will not transfer completely to the primary. Secondary leakage inductance will be largely decoupled from the primary for the same reason. The oscillation is probably the result of the step input applied to MOSFET drain-source capacitance, $C_{ds,}$ and primary leakage inductance, L_{lp}. If these are 225nF and 68.6nH, a resonant frequency of 1.28MHz would be expected. This corresponds well with the observed oscillation. Similarly, ≈300kHz ringing appears on the secondary immediately following the clamp intervals. However, its cause has not been determined.

Data for the full LVPC transformer model is given in Table 5.4. An input of 0.55V at a drive frequency of 1kHz is assumed. Values apply to a Philips E65/27/32 core in 3C90 material, but no significant differences would be expected if an equivalent ferrite was substituted (Neosid F5; Siemens N27). The section where the each variable was determined is shown for reference. Variables which are primarily load dependent have been identified by "LD".

Table 5.4 Transformer model parameters

Variable	Value	Section	Description
R_p, R_s	41.5μΩ*, 85.6mΩ	3.5, 5.1	Primary and secondary winding resistance
R_{fe}	587mΩ	3.5	Resistor representing core losses
C_p, C_s	0pF, 2.2pF	5.2	Primary and sec. intra-winding capacitance
C_{ps}	<1pF	5.2	Primary to sec. inter-winding capacitance
L_{mag}	7.2μH	3.5	Magnetising inductance
I_{mag}	19.1A	5.2	Magnetising current
I_p, I_s	LD	3.5	Primary and secondary current
L_{lp}, L_{ls}	68.6nH, 230.8μH	5.2	Primary and secondary leakage inductance
N_p, N_s	1, 58	3.5	Primary and secondary winding turns
V_p, V_s	0.55V, 25(LD)	2.1, 3.5	Primary and secondary voltage

*Includes skin effect.

5.3 Core saturation

Evidence of DC bias in the core was detected at power levels exceeding about 20W. As load current was increased beyond this point, a small voltage droop was observed in the last 50 to 100μs of alternate drive cycles. Input current, as measured with a Hall Effect current transducer, displayed an increase in the slope of the current ramp coincident with the secondary voltage droop. The input current waveform also showed that the drive pulse with the steeply sloping tail was delivering more average current than the alternate pulse. As load current was increased, both effects became more pronounced. At power levels above 60W the effect became severe.

The voltage droop and current cusp resulting from asymmetrical drive are typical of staircase saturation, but the load dependence is unexpected. Staircase saturation is usually assumed to depend solely upon magnetising current, which should be independent of load. No sign of DC bias was visible under no-load conditions, when I_{mag} contributes most of the primary current. With no load present, the Hall Effect probe revealed a perfectly symmetrical input current waveform of approximately $2.5A_{avg}$. Therefore, a second order effect must be in operation.

In an attempt to gain more information, a DC bias was deliberately injected into the core by means of an additional four turn winding. By connecting an external DC power supply, up to 12 ampere turns could be applied in either polarity. At an output power of 54W, it was found that a DC bias of 8 ampere turns was required to fully balance the average input current pulses as seen with the Hall Effect device, but this caused the saturation effects to worsen. It was also discovered that exactly the opposite bias (−8 ampere turns) was required to completely eliminate the saturation effects. However, in this case the current imbalance between successive input drive pulses became worse that it had been with no bias applied. With +8 Ampere turns of external bias the converter efficiency fell by 2% from its normal (no bias) value, while −8 Ampere turns produced a 1% fall. The positive bias also caused the core to emit a louder, harsher sound than usual. The core normally emits a seemingly pure 1kHz tone. The harsher tone probably indicates the presence of electrically or mechanically generated odd-order harmonics.

Evidently, positive external bias was driving the core further towards saturation, even though the input current pulse areas appeared more equal. However, equal load currents in successive pulses do not imply equal magnetising currents. Differences could arise if one drive path (transistors, contact resistance, leakage inductance, etc.) presents less impedance than the other. In this case, equal currents would produce different voltage drops, and therefore different volt-seconds would be applied to each half primary. This could explain the load dependence of the saturation effects. Higher load currents would increase the differential voltage drop between the half primaries, resulting in a progressively larger volt-second imbalance.

As saturation approaches, inductance falls and magnetising current rises. The increased current produces a voltage drop which tends to reduce the applied volt-seconds. The process is therefore self-limiting to some extent, but saturation still appears to be one of the factors limiting LVPC operation at higher powers.

5.4 Antisaturation feature

The LVPC design originally incorporated an antisaturation feature intended to release any DC component of transformer core flux during brief interruptions to the primary drive interval (see Section 3.7). As stated previously, this feature was removed when it became clear that significant time was required to reverse current in the transformer leakage inductance, with the mid-pulse antisaturation gaps effectively doubling the time lost to current recovery. With primary plus reflected secondary leakage inductance totalling 140nH, it takes about 28μs for 0.5V to re-establish a 100A input current. At 200A the time required increases to 60μs. To reduce this overhead to a more acceptable 5% of cycle time, the drive frequency would have to be reduced to 400Hz, or even less at higher currents. This is much too slow for the ferrite cores selected. However, given their higher permeability and saturation flux density, silicon or nickel steel cores may permit the antisaturation feature to be re-evaluated in future. If so, it might also be necessary to increase the output filter inductance in order to support the load current during the antisaturation gaps. (See Sections 7.3 and 8.7.)

5.5 Operating limitations and fault/overload tolerance

As LVPC output current increases, efficiency falls, and progressively more power is dissipated within the device. The principal locations of power loss are the input filter capacitors, power MOSFETs, transformer, diode bridge, and output filter inductor. At an output of 4A, for example, efficiency is only 50%, so about 60W will be dissipated as heat within the converter. Without extensive (and possibly destructive) tests, it would be difficult to determine the maximum permissible heat that could be dissipated safely, but 60W is probably very near that limit. At higher loads, overheating and circuit damage would be inevitable.

However, at or near short circuit conditions the auxiliary transformer winding would not be able to maintain sufficient output to sustain the drive circuit, so operation would cease before overheating could occur. Even with an ideal 0.6V source at the input, current through the MOSFETs and primary could not exceed 0.6V/230μΩ = 2600A, or 52A per transistor. This is well within their specified I_{ds}(max) of 75A. In the intended

application, with input provided by a 250W parallel solar cell array, current would be limited (by the array) to about 500A. A current of ten amps per transistor is not much higher than their normal design operating level. A failure in the MOSFET drive circuit will have exactly the same effect as a short circuit at the output. This is because normal drive ceases, leaving one bank of MOSFETs conducting (for about 20 seconds) until gate voltage falls below V_{th}. This has happened, with no apparent damage.

A production version of the LVPC should include some type of overload protection. This would probably take the form of active primary drive duty cycle control based upon input or output current sensing.

5.6 DCPS operating characteristics

The DC power supply developed as part of this project was designed to supply currents up to 500ADC at regulated output voltages from 0 to 1V. Although currents above 300A have yet to be required, the design objectives appear to have been met. Table 5.5 lists the performance specifications for this device. Unless otherwise stated, $V_{bat} = 2.0V$, $V+ = 12V$, $V- = -12V$, and $V_{out} = 0.5V$.

Note: Specifications for V_{bat}, $V+$, $V-$, V_{out}, I_{out} (up to 300A), and response times have been verified by test. All other specifications are either calculated or inherent to the design.

Table 5.5 500A DC power supply specifications

Parameter	Desig	Min	Typ	Max	Unit
Battery voltage	V_{bat}	1.8	2.0	2.4	V
Battery capacity			1.2		kAhr
Positive supply voltage	V+	10	12	15	V
Positive supply current	I–		65		mA
Negative supply voltage	V–	–10	–12	–15	V
Negative supply current	I–		–57		mA
Output voltage	V_{out}	0.0		1.0	V
Output current	I_{out}	0.0		500	A
Operating time at 500A				20	min.
DC output impedance	R_{out}			0.25	mΩ
Response time, ±10mV*			300		ns
Response time, ±25mV*			200		ns
Response time, ±50mV*			70		ns
Cooling bath temperature		0		50	°C

*Time to settle within the stated limits following a ±0.5V step applied at V_{out}.

6 Modelling

6.1 Introduction

In the preceding section, circuit losses were identified and a complete model of the transformer was developed. It should now be possible to predict how the circuit will operate under various input and load conditions.

Although many of the losses are the result of AC phenomena, it will be shown that they are all proportional – or nearly proportional – to the second power of input current. This means they can be related to I_{in}^2 by proportionality constants: $P_{loss} = kI_{in}^2$. Also, $P_{loss} = V_{in}I_{eq}$, where I_{eq} is the equivalent DC current which would produce the same power if supplied at V_{in}. In all cases, P_{loss} was determined for an input voltage of 0.55V, so $I_{eq} = (k/0.55)I_{in}^2$. Therefore, a DC equivalent circuit should prove satisfactory.

Figure 6.1 shows the resulting LVPC equivalent circuit. An explanation of each element follows. See Section 5.1 for details concerning the parameters and losses referred to below.

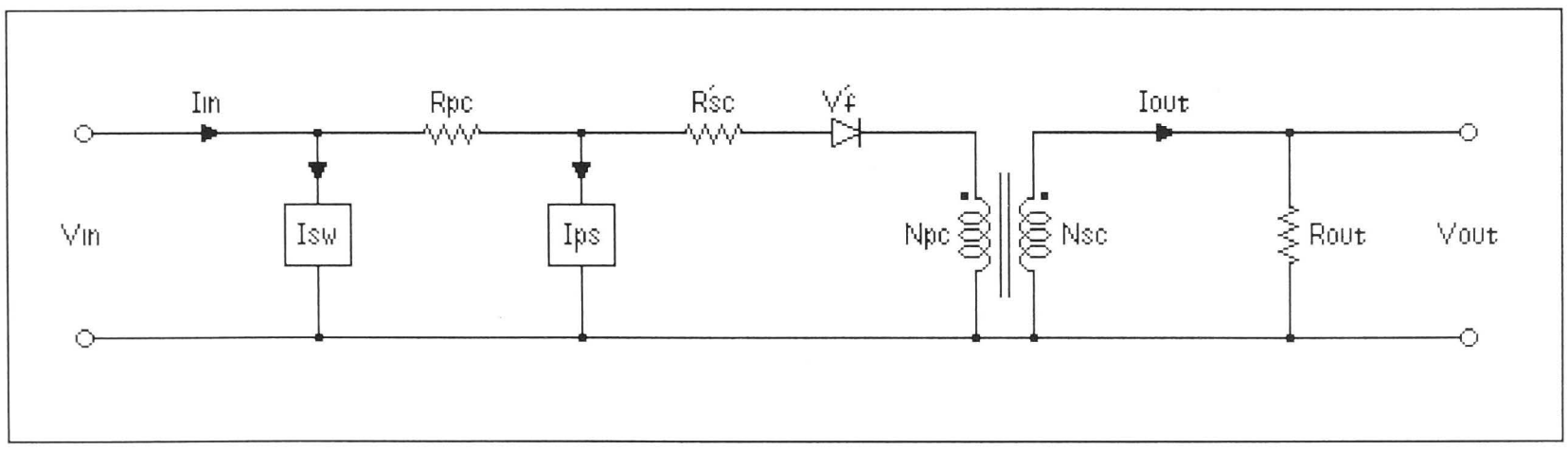


Figure 6.1 LVPC Circuit Model

6.2 Circuit elements

A model will be developed which consists of seven circuit elements. Most of these are composed of several sub-elements which act in series or parallel and can therefore be summed. In the discussion which follows, sub-elements are treated first, followed by

a description of how they combine to form model elements. The main circuit elements corresponding with those shown in figure 6.1 are preceded by a black dot (●) to facilitate identification.

Input filter capacitor equivalent current – I_{Cin}

Power dissipated in input filter capacitor effective series resistance is proportional to the square of input ripple voltage. Ripple voltage is proportional to I_{in}, so power is proportional to I_{in}^2. If $P_{Cin} = 3.71W$ at $I_{in} = 131.0A$, then $P_{Cin} = (216.2 \times 10^{-6})I_{in}^2 = 0.55 I_{Cin}$. Therefore, $I_{Cin} = (393 \times 10^{-6})I_{in}^2$.

MOSFET switching equivalent current – I_{fs}

Power dissipated in the MOSFETs while switching is proportional to V_{ds}, $I_{ds}(max)$ and t_{off}. However, because most of the energy to be dissipated is stored in leakage inductance, it is proportional to I_{in}^2. This means that as I_{in} decreases, the effective value of t_{off} will also decrease because I_{ds} will reach zero sooner. This argument does not quite hold for input currents above about 130A because t_{off} cannot extend beyond the point where FET drive resumes (0.5µs). In this case, additional power can be dissipated because I_{ds} does not return to zero during t_{off}.

If FET switching loss, $P_{fs} = 2.79W$ when $I_{in} = 131.0A$, then $P_{fs} = (162.6 \times 10^{-6})I_{in}^2$. Division by $V_{in} = 0.55V$ to convert to an equivalent current gives $I_{fs} = (296 \times 10^{-6})I_{in}^2$.

MOSFET reverse diode equivalent current – I_{rd}

Power dissipated in the MOSFET reverse diodes while switching is proportional to V_f, $I_{ds}(max)$ and t_{on}. By a similar argument to that given above, power to the MOSFET reverse diodes will also be proportional to I_{in}^2. If $P_{rd} = 0.08W$ at $I_{in} = 131.0A$, then $P_{rd} = (4.662 \times 10^{-6})I_{in}^2 = 0.55I_{rd}$, and $I_{rd} = (8.48 \times 10^{-6})I_{in}^2$.

Snubber circuit equivalent current – I_{sn}

At FET turn-off, the snubber circuit acts to minimise the V_{ds} voltage spike by diverting some of the leakage inductance driven primary current into the holding capacitors. Because t_{off} is significantly shorter than the $\sqrt{(L_l C_{sn})}$ time constant, snubber voltage should increase almost linearly by $I_p t_{off}/C_{sn} = 154.9(0.5 \times 10^{-6})/(20 \times 10^{-6}) =$

3.9V. However, it actually increases by 5.2V. The reason for this is uncertain, but the fact that the 36V spike at V_{ds} is not seen at the holding capacitors gives a strong clue: Spike energy may be stored temporarily in series inductance associated with the snubber circuit wiring. It could then continue to be transferred on to the holding capacitors after the 0.5μs switching interval, effectively lengthening the C_{sn} charge time.

Such an inductance would form a crude integrator which would cause the snubber input current to be approximately proportional to the area of the $V_{ds}t_{off}$ spike. V_{ds} is only weakly dependent upon I_{in}, while t_{off} should be roughly proportional to it (as described above), making spike area proportional to I_{in}. Because most snubber energy is dissipated in resistors, power is proportional to the square of snubber current. Therefore, snubber circuit *equivalent* current is proportional to the square of *actual* snubber current. If $P_{sn} = ½(20 \times 10^{-6})(5.2^2)(2000) = 0.54W$ at $I_{in} = 131.0A$, then $P_{sn} = (31.47 \times 10^{-6})I_{in}^2 = 0.55I_{sn}$, and $I_{sn} = (57.21 \times 10^{-6})I_{in}^2$.

- Combined switching loss equivalent current – I_{sw}

  Because I_{Cin}, I_{fs}, I_{rd} and I_{sn} act in parallel, they may be replaced by a combined switching loss equivalent current, $I_{sw} = (754.7 \times 10^{-6})\ I_{in}^2$.

Input connection resistance – R_{con}

The input connection resistance, $R_{con} = 38.2\mu\Omega$.

Drain and source bar resistance – R_{bar}

The combined effective resistance of the drain and source bars, $R_{bar} = 74.1\mu\Omega$.

MOSFET channel resistance – R_{ds}

The MOSFETs have a specified $R_{ds}(on)$ of 5mΩ, giving a parallel combination of $R_{ds} = 100\mu\Omega$ for each bank of 50.

MOSFET socket resistance – R_{soc}

The parallel resistance of MOSFET sockets, $R_{soc} = 120\mu\Omega$ for each bank.

Transformer primary resistance – R_p

The effective DC resistance of each half-primary, $R_p = 41.5\mu\Omega$.

- Combined primary equivalent series resistance – R_{pc}

Because R_{con}, R_{bar}, R_{ds}, R_{soc} and R_p, act in series, they can be replaced with a combined primary equivalent series resistance, $R_{pc} = 373.8\mu\Omega$.

Transformer core equivalent current – I_{fep}

If the transformer core dissipates 0.44W at $V_p \approx 0.50V$, the effective equivalent resistance, $R_{fep} = 0.50^2/0.44 = 0.57\Omega$. Transforming this into an equivalent current makes the model much easier to use (fewer loops), with negligible loss in accuracy. $I_{fep} = 0.44/0.50 = 0.88A$.

FET drive circuit current – I_{fd}

The drive circuitry uses 39.8mA at 12V, 70% of which is independent of input voltage. As the input voltage only varies by ±9%, the effect of voltage on the remaining 12mA is negligible. The auxiliary winding current is transformed to about $I_{fd} = 1.11A$ on the primary.

- Combined primary equivalent shunt current – I_{ps}

Transformer core equivalent current and FET drive circuit current act in parallel. They can be replaced by a primary equivalent shunt current, $I_{ps} = 1.99A$.

Transformer secondary resistance – R_s

The DC resistance of the secondary winding, $R_s = 85.6m\Omega$.

Output inductor core equivalent resistance – R_{feL}

Because the inductor is in series with the load, an equivalent series resistance will be used to model the core loss. If the core dissipates 0.07W when $I_{out} = 2.314A$, then $R_{feL} = 0.07/2.314^2 = 13.1m\Omega$.

Output inductor winding resistance – R_L

The DC resistance of the inductor, $R_L = 124m\Omega$.

• Combined secondary equivalent series resistance – R_{sc}'

Because R_s, R_{feL} and R_L, act in series, they can be replaced with a combined secondary equivalent series resistance, $R_{sc} = 222.7m\Omega$. To simplify computation, R_{sc} will be referenced to the primary. $R_{sc}' = (222.7 \times 10^{-3})/(58^2) = 66.2\mu\Omega$.

• Diode bridge forward voltage – V_f'

For most currents within the operating range of the LVPC, the forward drop of the diode bridge, $V_f = 2 \times 0.30 = 0.60V$. To simplify computation, V_f can be referenced to the primary side of the transformer. $V_f' = 0.60/58 = 0.0103V$.

Ideal transformer – N_s/N_p

The ideal transformer will have the same turns ratio as the real one: 58:1.
(This assumption may be incorrect. See Sections 6.4 and 7.3 for discussions concerning an unexplained voltage loss associated with the transformer.)

Output inductor voltage/current transformation – N_{sL}/N_{pL}

Apart from voltage drops associated with resistive and core losses, the average voltage across the inductor, V_L, must be zero. The output end of the inductor is, of course, at V_{out}. The diode bridge holds the input end at zero volts during t_{clamp} (or t_c), and the secondary drives it to $V_s - V_f = V_{s-f} = v_{out}(t) + v_L(t)$ for the remainder of the cycle. If $V_L(avg) = 0$, then $V_{out}t_c = (V_{s-f} - V_{out})(500\mu s - t_c)$. Therefore the average output voltage, $V_{out} = V_{s-f} \times (500\mu s - t_c)/500\mu s$, or $V_{out}/V_{s-f} = (500\mu s - t_c)/(500\mu s)$.

During t_{clamp}, I_{out} flows in the inductor but not the secondary, whereas for the remainder of the cycle I_{out} flows in both. Therefore, the average current through the inductor, $I_{out} = I_s(500\mu s)/(500\mu s - t_c)$, or $I_{out}/I_s = (500\mu s)/(500\mu s - t_c)$. These expressions for inductor voltage and current show that it functions like a transformer with $N_s/N_p = (500\mu s - t_c)/(500\mu s)$.

Clamp interval is proportional to input current and leakage inductance, and inversely proportional to input voltage and V_{ds} transient voltage. With leakage inductance fixed, it is reasonable to expect that t_{clamp} will be roughly proportional to I_{in}/V_{in}. Inspection of

Table 5.1 bears this out, with the ratio of t_{clamp} to I_{in}/V_{in} averaging 0.144×10^{-6} volt seconds per ampere over a wide range of currents. Substituting $t_{clamp} \approx (0.144 \times 10^{-6})I_{in}/V_{in}$ into the expression for effective inductor turns ratio gives $N_{sL}/N_{pL} = 1 - 0.000288I_{in}/V_{in}$.

- Combined equivalent output transformer – N_{sc}/N_{pc}

The ideal 58:1 transformer can be combined with the output inductor/transformer of $N_{sL}:N_{pL}$ to form a combined equivalent output transformer, $N_{sc}/N_{pc} = 58(1 - 0.000288I_{in}/V_{in}) = 58 - 0.0167I_{in}/V_{in}$.

- Load resistor – R_{out}

Load resistance values will be the same as those used for the LVPC circuit evaluation: 3.9 through 105Ω.

6.3 Equivalent circuit equation

The LVPC equivalent circuit can be used to predict the operating point which should result from various input and load conditions. The following expression relating V_{in}, R_{out} and I_{in} was derived (with some effort) from the circuit model given above. To reduce complexity, μ has been substituted for 10^{-6}, and μμ for 10^{-12}.

$$92.609\mu\mu I_{in}^4/V_{in}^2 - 0.12271\mu I_{in}^3/V_{in}^2 - 0.64328\mu I_{in}^3/V_{in} - 2.8359\mu I_{in}^2/V_{in}^2 + 1{,}131.3\mu I_{in}^2/V_{in} + 1117.1\mu I_{in}^2 + 754.7\mu R_{out}I_{in}^2 - 3.4174I_{in} + 19{,}698\mu I_{in}/V_{in} - R_{out}I_{in} + 1.99R_{out} + 3364V_{in} - 34.206 = 0. \quad [6\text{–}1]$$

This expression was used to predict circuit behaviour at the same operating points as those selected for the LVPC tests. Actual circuit data is given in Table 5.1. Parameters predicted by the model are shown below in Table 6.1, while figure 6.2 shows how output power, efficiency and output voltage are expected to vary with input power, at an input of 0.55V.

Table 6.1 LVPC circuit model results

Vin, V	Iin, A	Pin, W	Vout, V	Rout, Ω	Iout, A	Pout, W	Eff'y, %	tc, µs	Vo/Vin	(Ii-2)/Io
0.50	17.3	8.7	27.7	105	0.26	7.3	84.0	5.0	55.3	58.2
0.55	18.9	10.4	30.5	105	0.29	8.8	85.1	4.9	55.5	58.3
0.60	20.5	12.3	33.4	105	0.32	10.6	85.9	4.9	55.6	58.4
0.50	33.7	16.9	27.0	49.8	0.54	14.7	87.0	9.7	54.0	58.4
0.55	37.1	20.4	29.8	49.8	0.60	17.9	87.6	9.7	54.2	58.6
0.60	40.4	24.2	32.6	49.8	0.65	21.3	87.8	9.7	54.3	58.7
0.50	53.4	26.7	26.3	30.0	0.88	23.0	86.3	15.4	52.6	58.7
0.55	58.9	32.4	29.0	30.0	0.97	28.0	86.4	15.4	52.7	58.9
0.60	64.4	38.6	31.6	30.0	1.05	33.4	86.4	15.5	52.7	59.2
0.50	76.1	38.1	25.4	20.2	1.26	31.9	83.9	21.9	50.8	58.9
0.55	84.2	46.3	28.0	20.2	1.39	38.8	83.8	22.0	50.9	59.3
0.60	92.4	55.4	30.6	20.2	1.51	46.4	83.6	22.2	51.0	59.7
0.50	105	52.6	24.4	14.0	1.74	42.4	80.7	30.3	48.7	59.3
0.55	117	64.2	26.8	14.0	1.92	51.5	80.2	30.6	48.8	59.8
0.60	128	77.0	29.3	14.0	2.09	61.4	79.7	30.8	48.9	60.4
0.50	139	69.6	23.2	10.1	2.30	53.3	76.6	40.1	46.4	59.7
0.55	155	85.3	25.6	10.1	2.53	64.7	75.9	40.6	46.5	60.5
0.60	171	102.7	27.9	10.1	2.76	77.1	75.1	41.1	46.5	61.2
0.50	189	94.4	21.6	7.0	3.09	66.9	70.9	54.3	43.3	60.4
0.55	211	116.2	23.8	7.0	3.40	81.1	69.8	55.3	43.3	61.5
0.60	235	140.8	26.0	7.0	3.71	96.5	68.5	56.3	43.3	62.7
0.50	236	117.9	20.3	5.3	3.83	77.6	65.8	67.9	40.6	61.1
0.55	265	145.9	22.3	5.3	4.21	93.8	64.3	69.4	40.5	62.6
0.60	297	177.9	24.3	5.3	4.59	111.5	62.7	71.2	40.5	64.2
0.50	273	136.3	19.3	4.4	4.39	84.6	62.1	78.5	38.6	61.7
0.55	308	169.4	21.2	4.4	4.82	102.2	60.3	80.6	38.5	63.5
0.60	346	207.7	23.1	4.4	5.25	121.1	58.3	83.1	38.5	65.6
0.50	299	149.4	18.6	3.9	4.78	89.0	59.6	86.1	37.3	62.1
0.55	339	186.5	20.5	3.9	5.25	107.3	57.6	88.8	37.2	64.2
0.60	383	229.6	22.3	3.9	5.71	127.0	55.3	91.8	37.1	66.7

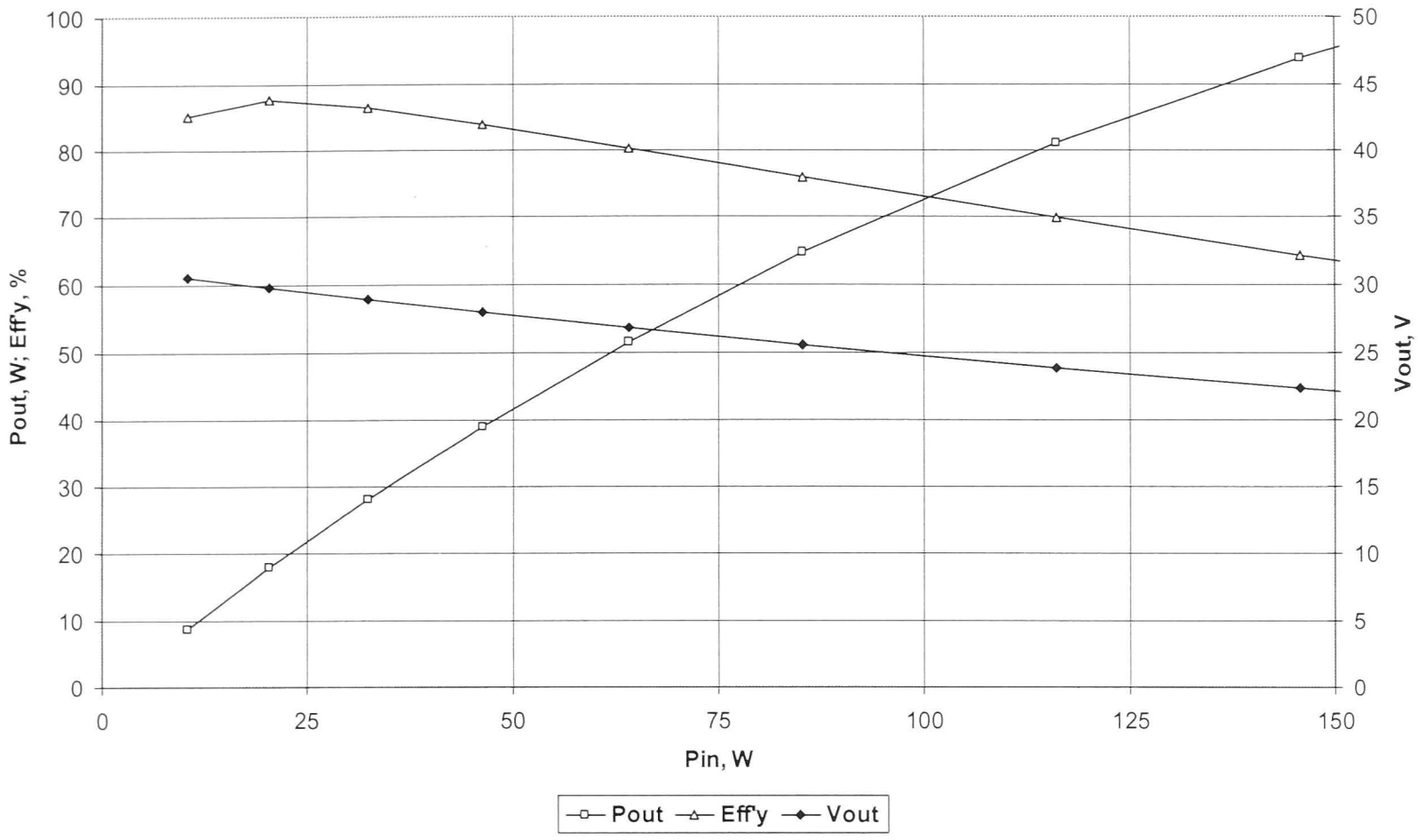


Figure 6.2 Predicted variation of LVPC output power, efficiency and output voltage with input power.

6.4 Model evaluation

Comparison of actual LVPC results (Table 5.1 and figure 5.1) with those predicted by the model (Table 6.1 and figure 6.2) reveals that as input power increases, output voltage falls off more rapidly in the actual circuit than it does in the model. Because of this, the actual circuit is restricted to somewhat lower power levels than would be expected from the model. Predicted efficiency agrees well with measured results at similar power levels (up to about 75W input), so circuit losses appear to be accurately represented. It would seem that the LVPC output voltage is being reduced by some mechanism that does not involve significant power loss.

Examination of the LVPC circuit confirms that voltage is being lost in the transformer. Under light load, primary and secondary volts per turn are nearly equal, but as current increases, the secondary experiences a voltage drop in excess of that which can be explained by the combined winding resistance. The transformer behaves as though its turns ratio was inversely proportional to current. At an output power level of 56W, the mid-pulse primary voltage was found to be 0.515V per turn, while the

secondary measured 27.6V, or 0.476V per turn. The 7.6% voltage loss is consistent with the 54W data given in Table 5.1 (after allowing for the other known losses). At this power level, primary plus secondary winding resistance only accounts for 0.009V/turn, or a 1.7% voltage drop.

Part of the remaining voltage loss can be explained by leakage inductance. At P_{out} = 54W, load current falls by 0.428A during the 35µs clamp interval. (See Section 5.1, "Output inductor core".) Therefore, load current must increase by an equal amount over the next 465µs, during which the secondary supplies current to the output filter inductor and load resistor. The transformer converts this to a 24.82A increase in primary current, with a resulting di/dt of 53.38A/ms. (With a resistive load, current rise will be exponential, but the linear approximation is very close.) This di/dt could be expected to produce a voltage of 7.32mV across a 137.2nH leakage inductance, as reflected to the primary.

Magnetisation current also ramps up by 38.2A during the 500µs drive interval, with a slope of 76.40A/ms. Because magnetisation current acts only on the primary, this di/dt should produce a voltage drop of 5.24mV across the 68.6nH primary leakage inductance. The combined loss of 12.6mV per turn on the primary is equivalent to a 729mV fall on the secondary, which should lead to a drop of 679mV on the output side of the filter inductor. (With comparable output and magnetising currents, the output voltage predicted by the model is about 2.2V too high. The inclusion of the above loss would reduce this error to about 1.5V.)

An $L_l di/dt$ factor could have been included in the circuit model as a pair of current related voltage losses associated with the transformer: An input voltage dependent ΔI_{mag} component, plus a load and input voltage dependent ΔI_{out} component. However, 0.515 − 0.476 − 0.009 = 0.030 volts per turn. Of this, leakage inductance and changing load and magnetising current can only account for 12.6mV/turn, leaving 17.4mV/turn (or 1.009V on the secondary) still "missing".

It is possible that a progressive loss of flux linkage between primary and secondary is occurring as load current increases. It is also possible that such a loss of coupling acts to

modulate the value of leakage inductance, thereby introducing an additional IdL_l/dt term. While such a process could be responsible for an additional 17.4mV/turn loss, there is as yet no experimental proof of its existence (see Section 7.3).

The model also fails to predict the effects of incipient core saturation, which are seen in the real circuit above about 60W. However, these effects would be extremely difficult to model due to the random and varied nature of their causes. The omission is not seen as serious flaw.

7 Discussion

7.1 Interpretation of results

The principal objective of this project was to prove the feasibility of converting 0.5-0.6V DC into usable power. This was achieved. As a means to this end, the original specification for the Low Voltage Power Converter called for a 200W output to be produced from a 0.55V input at an efficiency of 80%. This was not achieved, although these voltage and efficiency goals were met at lower power levels.

There are a number of reasons power did not reach the desired value. Most have already been discussed quantitatively in Section 5.1 but, to summarise, the principal causes are:

Input filter capacitors – ESR too high.
Drain and source bars – Skin effect.
MOSFET sockets – Contact resistance too high.
MOSFETs – Switching losses too high.
Transformer – Leakage inductance; Voltage loss.

None of these were considered significant during the design phase, yet the first four causes contribute more than half the power loss above the 50W output level, while the last two limit the usefulness of the converter beyond this wattage. But the news is not all bad. Most of these factors are correctable, at least in principle. By substituting a different core material, it may even be possible to overcome the transformer voltage loss problem (see Section 7.3 below).

7.2 Measurement error analysis

The same test equipment was used to evaluate both the LVPC and the 500A DCPS. A Fluke 87 digital multimeter was used for most voltage and resistance measurements. It has a specified accuracy of 0.1% of reading ±1 count for DC volts, and 0.2% of reading ±1 count for Ohms. Measurements of LVPC output voltage and load resistance

were made directly with this meter. Output current was calculated from these readings to avoid the voltage burden of the meter's current sense resistor. Values so obtained are assumed to be reliable.

LVPC input (and 500A DCPS output) voltages taken with this meter may have been affected by the short, high amplitude switching transients which were present at all load levels. However, such readings were in reasonably close agreement (±5%) with voltages observed simultaneously on an oscilloscope.

LVPC input current measurements were made using a Good Will Instruments GWM-037 current clamp. This is a Hall Effect device with a specified accuracy of 1% ±5 counts for DC current. The instrument has a specified accuracy of 2.5% ±10 counts for RMS AC current, within a range of 47 to 400Hz. High speed switching transients with frequency spectra lying well above this range should not have had a significant effect on accuracy.

Input current waveforms were also observed on an oscilloscope coupled to an LEM type HT200-SB Hall Effect current transducer. The specified accuracy of this device is: offset, ±0.4% of range; gain, ±1% of range ±0.05% of reading per degree Celsius. These would total ±3% for a half scale reading with $\Delta T = 4°C$. The specified small signal frequency range is DC to 25 kHz, which may imply a reduction in gain of up to 4% at 1 kHz.

At a power level of 54W, the GWM-037 read 133.5A, while careful visual averaging of the HT200-SB transducer output on the oscilloscope display gave 125A. The 6.4% discrepancy is reasonable, considering that it includes the combined inaccuracies of three instruments plus interpolation error.

A Tektronix 2232 oscilloscope was used for all time measurements. It was also used to measure the amplitudes of non-DC voltages such as drive circuit, switching transient and transformer waveforms. Its specified time base accuracy is ±2%, while vertical amplifier DC accuracy is also stated to be ±2%. Vertical gain linearity, defined as the change in amplitude of a two-division test signal as it is moved around the screen, is

specified as ±5%. This would appear to imply that the 2% DC accuracy is with respect to full-screen deflection.

Great difficulties were encountered while attempting to obtain meaningful voltage data with the oscilloscope. Large currents and high di/dt's made the concept of "ground" almost meaningless. Transient voltages varied significantly when either the probe tip or ground clip was moved a few centimetres. Even varying the BNC contact resistance (by wiggling) at the oscilloscope front panel made tens of millivolts difference in the apparent amplitudes of some transients. Effective measurement would have required RF construction techniques such as impedance-controlled conductors and a tightly coupled ground plane. This would not have been practical, given the size and distribution of many critical components.

Many attempts were made to reduce these effects. A battery powered (floating) oscilloscope was tried. The probe was shielded with a length of grounded steel pipe. Readings were taken differentially using a pair of probes with their cables twisted together. A coaxial probe tip connector was soldered directly to the LVPC input conductors. However, none of these techniques elicited so much as a placebo effect.

Although questions concerning the reliability of oscilloscope data frustrated much diagnostic work, they had minimal impact on the key measurements used in determining basic circuit performance. One possible exception to this is the measurement of MOSFET drain to source voltage, V_{ds}. This is a low level, ground referenced voltage which contains high level, high frequency transients. MOSFET R_{ds}(on), MOSFET socket resistance and V_{ds} switching transient waveforms are critical factors governing efficiency. Their contribution was determined directly from oscilloscope measurements of drain-source voltage. The accuracy of such measurements would be difficult to establish, but 5-10% might be a reasonable estimate.

7.3 Design improvements

The performance of the LVPC could be substantially improved by reducing the losses identified in Section 7.1.

The input filter capacitors were called upon to carry much more ripple current than was originally expected. This is partly because the current and voltage transients associated with transformer leakage inductance and distributed conductor inductance are higher than anticipated, and partly because the 500A DCPS does not recover from these transients quickly enough. More input capacitance with lower effective series resistance would help, but physical constraints limit this to about 30mF and 3mΩ. Redesigning the 500A DCPS amplifier circuit board for improved bandwidth would probably reduce the demands placed on the input capacitors, thereby improving efficiency.

The situation may or may not be improved by replacing the DCPS with an actual parallel solar array. A rapid transient recovery time could be expected to improve performance, while the increased output impedance of heavily loaded solar cells would have the opposite effect. The LVPC will undoubtedly perform at its best when the array is operating at or above the array's maximum power point, but experimental data will be required to quantify details of the interaction.

The LVPC and DCPS circuit boards were constructed using point-to-point hand wiring on perforated phenolic prototyping board because PCB design software and fabrication facilities were not readily available. Both circuits would probably benefit from high quality circuit boards incorporating guard tracks and ground planes.

Skin effect was not considered in the design of the drain and source bars. These should have been made thinner and wider to minimise this effect. A radial design utilising a toroidal transformer might also prove advantageous. (A circuit photograph indicates this technique may have been employed by Meyer and Schmidt [10].)

MOSFET sockets were not part of the original design. They were added as an "insurance policy" to protect against having to replace melted MOSFETs by the handful. In fact, despite the occasional static discharge from an inquisitive visitor, none were lost. The square cross section transistor pins should have been pressed into slightly undersized round holes in the drain and source bars as originally planned. (Soldering is

impractical because of the large thermal mass of the drain and source bars, and because epoxy adhesives are used in their assembly.)

MOSFET switching losses were greatly underestimated. This is another consequence of failing to foresee the problems associated with parasitic inductance. An effective snubber circuit should be able to keep V_{ds} transients to less than 10V, thereby reducing switching losses by a factor of four. Unfortunately the snubber in the LVPC was added later as a "fix". Consequently, it is located too far away from the transistors to be of much benefit. To be effective, each MOSFET should have its own spike diversion diode. These would feed holding capacitors distributed along the FET banks, each serving a group of about five transistors. In addition, snubber wiring should be of large cross section to reduce resistance and stray inductance.

Further reduction in switching losses could be achieved by operating the converter at lower drive frequencies. A core material with higher saturation flux density, B_{sat}, would be required, as the number of primary turns is fixed by mechanical and electrical constraints. Alternatively, a larger core (with greater cross sectional area) could be used.

The last major factor which limits maximum achievable output power is voltage loss across the transformer. Part of the loss is due to combined primary and secondary IR drop, and part appears to be the result of interaction between leakage inductance and the current ramps produced by both the primary magnetising inductance and the output filter inductor (see Section 6.4).

However, there remains a significant voltage loss which cannot be explained by these two mechanisms. This component amounts to about 17.4mV/turn at the 54W power level. It may be that leakage inductance is being modulated by magnetising current, producing an additional IdL_l/dt voltage term (see below). Alternatively, the additional loss may be an indirect consequence of a progressive reduction in flux linkage between primary and secondary, corresponding with increased load current.

Normally, such an association should not occur. Magnetising and load current should be independent, so the latter should not affect core flux levels. However, portions of the

core may be magnetically linked to only one winding (or part winding), and so contribute to leakage inductance. High load currents may cause these areas to expand relative to the remainder of the core, with possible secondary effects.

Such a displacement would produce an increase in leakage inductance and a corresponding decrease in magnetising inductance. Increased leakage inductance could be expected to be accompanied by an increase in the ratio of clamp interval to load current. Inspection of Table 5.1 reveals that this is the case, especially at output power levels above about 50W.

The only direct effect of a decrease in magnetising inductance would be an increase in magnetising current (accompanied by slight increases in copper and core loss). The voltage and current transfer ratio should not change, but an increase in magnetising current will cause flux density to increase proportionately. If this increase drives the core too close to saturation near the ends of successive drive pulses, secondary voltage will fall, accompanied by a simultaneous rise in magnetising current (in addition to the increase just described). These effects have been observed in the secondary voltage and input current waveforms at the higher power levels. However, they only affect the last 100μs of alternate drive intervals, not the mid-pulse voltage. If the flux displacement hypothesis is also responsible for mid-cycle voltage loss, the connection must be lie elsewhere.

For an inductor, $V_L = Nd\Phi/dt$, where core flux, $\Phi = LI_L/N$. (This is consistent with $\Phi = \mu_e N I_L A_e/l_e$ and $L = \mu_e N^2 A_e/l_e$.) If current is changing while inductance is constant (the usual case), $V_L = LdI_L/dt$. However, if current and inductance are both functions of time, then

$$V_L = LdI_L/dt + I_L dL/dt. \qquad [7.1]$$

This situation could arise if load current induced flux displacement is modulating leakage inductance directly. This can happen because load current varies during each cycle due to the effects of the output inductor. It is also possible that I_{mag} is solely responsible for the time dependence of L_l, with the effect only becoming apparent as the

dL_l/dt term becomes multiplied by progressively higher load currents. But it is more likely to be a combination of the two, with flux displacement forcing a rise in flux density, which in turn causes leakage inductance to become progressively more dependent upon the instantaneous value of I_{mag}. In this case, the dL_l/dt term would become a function of both load current and I_{mag}.

From Section 6.4, I_{mag} and I_{out} current ramps combine to produce an $L_l di/dt$ term of 12.6mV/turn. The remaining "unexplained" voltage loss is therefore $0.515 - 0.476 - 0.009 - 0.0126 = 0.0174$V/turn. If changing leakage inductance is responsible for this loss, then $I_p dL_l/dt = 0.0174$V. With $I_p = 135.8$A at mid-pulse (where $I_{mag} = 0$), $dL_l/dt = 128.1\mu$H/s. If it is assumed that most of the change in leakage inductance takes place in the 465μs interval during which I_{out} is ramping up in the output filter inductor, then $\Delta L_l = (128.1 \times 10^{-6})(465 \times 10^{-6}) = 59.6$nH.

Taking I_p' as secondary current referred to the primary, the complete expression for primary-referenced voltage loss across the transformer leakage inductance becomes: $V_{Ll} = L_l dI_p'/dt + L_{lp} dI_{mag}/dt + I_p dL_l/dt = 0.00732 + 0.00524 + 0.0174 = 0.030$V. Therefore, a change in leakage inductance from 107nH to 167nH (centred around the average value of 137nH) during the course of the drive interval would fully explain the missing secondary voltage. This change seems plausible.

Confirmation of this hypothesis could be achieved directly by measuring changes in L_l during the conduction interval. Or, it could be verified indirectly by establishing whether a reduction in the average value of L_l, as measured at a given load, corresponds with the expected increase in secondary voltage at that load. The first approach would be difficult to achieve in practice, while the second has a distinct advantage in that it has the potential to both confirm and solve the problem in a single step.

By confining more flux to the core, higher permeability, μ_e, should reduce the percentage of flux which fails to link all turns (leakage flux). Although the relationship between μ_e and L_l may be nonlinear, leakage inductance should be reduced and coupling coefficient improved by increasing permeability. The ferrite cores used in the LVPC have $\mu_e \approx 2$mH/m and $B_{sat} \approx 420$mT. Silicon steel and nickel steel core materials

are available with $\mu_e \approx 38$mH/m and $B_{sat} \approx 1300$mT, so it may be possible to reduce leakage inductance and related circuit losses by a significant amount. The trade-off associated with these materials is bandwidth. Nickel steel is usable to about 20kHz, while silicon steel is somewhat slower. However, the 1 MHz bandwidths typical of power ferrites are not necessary in this application.

A prototype core constructed from 75 stacked 0.014 inch EI lamination sets in 49% nickel steel ("SuperPerm 49") was ordered from Magnetic Metals. It was hoped that a significant reduction in leakage inductance would be achieved, permitting operation at higher power levels than are currently possible. Performance of the LVPC using this core is reviewed in Section 8.

7.4 Commercial potential

A complete List of Materials for the LVPC is given in Appendix I. The total parts cost of the converter is $969.54 (in 1999 dollars). Assembly and test would add at least $250 to this figure, putting the selling price well over $2,000. With an as-constructed output of 50W and 75% efficiency, the commercial applications of this converter (at this price) would probably be nonexistent at best. However, as discussed above, the original design goal of 200W may yet be reached. If this is successful, it may be possible to exploit niche markets where the long term maintenance benefits of parallel solar arrays outweigh the relatively high initial cost of the LVPC.

The principal advantage of the parallel solar cell array/LVPC combination is its superior tolerance of uneven illumination and unequal cell output. Cell matching, positioning, bypassing, cleaning and sun tracking all become less important as compared to a series array. For low power levels, only a single cell may be required. (One 127mm diameter cell can produce 40W at 20 suns.) However, a single cell 30W output converter probably could not compete with a converterless 24 or 48 cell series equivalent, at least not on the basis of price alone.

The principal cost-drivers are the MOSFET switches (~$550), the drain/source/primary assembly (~$190), and the fitting of the MOSFETs to this

assembly (~$70). The cost of the remaining components, assembly and test (~$390) would not be much more than normal for a DC/DC converter of 200W output.

The price of high current MOSFETs has been declining steadily over the past 20 years. Consequently, a 5mΩ device probably costs less today (allowing for inflation) than a 1Ω device did in 1980. This trend might well continue but for the fact that 5mΩ is close to the resistance limit imposed by the 3-pin plastic packages (TO-220 or similar) in which they are sold. Putting a 5μΩ FET in such a package would be pointless. More appropriate packages exist, but they are expensive because production quantities are relatively low.

A better approach would be to wire-bond the least expensive FET dice available (in terms of minimum Ω$ product) directly to the drain and source bars of the converter, then protect the bonded FETs with a suitable cap or coating. Parts, assembly and machining costs, as well as contact and thermal resistance, inductance and size would all be reduced.

The cost of the copper drain/source/primary assembly could probably be lowered by casting or stamping the two halves, followed by machining only the critical surfaces. It may also be practical to substitute aluminium for copper in this assembly, although contact resistance could become a significant problem.

It is extremely difficult to extrapolate production costs of a complex electromechanical assembly based upon a single hand made prototype. Nevertheless, the fact that a not-too-expensive device has been functioning reliably for more than three years is a convincing argument for its practicality. A quantitative cost/benefit analysis of series vs. parallel solar arrays is beyond the scope of this paper, but there would seem to be ample justification for further work in this direction. Certainly there is no technical reason not to proceed.

8 Nickel Steel Core

8.1 Introduction

In Section 7.3 it was proposed that a nickel steel transformer core be trialled in an attempt to improve converter performance by reducing leakage inductance. It was also hoped that this change would confirm that the "missing" output voltage was a consequence of an IdL/dt term in the expression for primary voltage.

A custom made, laser cut core consisting of 75 "EI" laminations was obtained from Magnetic Metals Corp. of Camden, New Jersey, USA. The laminations were fabricated from "Superperm 49", a magnetic alloy containing 50% nickel and 50% iron. This material is available in 0.006 and 0.014 inch thicknesses. The 0.014 inch material was selected for reasons of cost and convenience in handling. External dimensions of the new core are identical to the 65/32/27 ferrite core set used previously, except that its effective thickness is reduced very slightly (to about 26.3mm) by small air gaps between the laminations. Parameters for the assembled NiFe core are as follows:

Superperm 49 EI lamination set design parameters:

Magnetic path length (effective)	l_e	14.7 cm
Magnetic cross section (effective)	A_e	5.18 cm^2
Permeability (effective)*	μ_e	16.5 mH/m
Bobbin winding window area	A_w	3.92 cm^2
Length of turn (mean)	l_T	15.1 cm

* This parameter is determined in Section 8.4, below.

8.2 Eddy current reduction

Following core replacement, initial tests indicated that the Low Voltage Power Converter no-load input current had increased from 2.6A (with the Philips 3C90 ferrite core) to 4.3A. An ohmmeter check across the lamination stack indicated about 1Ω; the

laminations were not insulated from each other. Large eddy currents were therefore presumed to be the cause of the additional no-load input current.

The core was disassembled and each lamination was cleaned and painted on one side. Excess paint was carefully removed to ensure maximum stacking factor (i.e. minimum spacing), and the pieces re-cleaned. Upon reassembly, only 74 EI laminations fit into the winding bobbin, indicating that the paint film on each was about 5 microns thick. Stack resistance was measured as roughly 50Ω. It is not known why this figure isn't significantly higher. However, given that eddy current loops can only develop a maximum of 0.5V, 50Ω should be sufficient to reduce these stray currents to negligible levels.

Following this labour-intensive procedure, it was most disappointing to learn that no-load input current remained completely unchanged at 4.3A! Obviously eddy currents weren't the problem. Hysteresis loss must therefore be significant, as will be shown below.

8.3 L_s and L_p measurement

Unlike ferrite core materials, the permeability of nickel steel is strongly dependent upon magnetic field strength. For this reason, winding inductance should be measured with magnetisation levels approximating those experienced during normal operation.

One way to achieve this would be to place a current transducer in series with the primary with the LVPC operating under no-load conditions. This is impractical due to physical constraints. (The probe won't fit.) However, the same level of magnetisation can be achieved by driving the secondary. This method has an advantage in that $1/58^{th}$ the current (at 58 times the voltage) is needed to produce the required field, making a much better impedance match to a conventional 50Ω signal generator.

During normal 1kHz operation, about 0.5V is applied to the primary for 0.5ms. For square wave drive, $B_{max} = V_p/(4fN_pA_e) = V_s/(4fN_sA_e)$, so V_pN_s/N_p applied to the secondary should produce the same B_{max}. Unfortunately, typical function generators

cannot deliver $0.5 \times 58 = 29V$, so it was necessary to reduce the drive frequency to 200Hz at 5.8V to achieve the $29 \times 0.5 \times 10^{-3} = 14.5$ mVsec required.

Inductance is most easily computed from impedance, so the 5.8V square wave was replaced with a $9.1V_{peak}$, 200Hz sinusoid having the same area per half-cycle. ($\pi^{-1}\int_0^{\pi}\sin\theta d\theta = 2/\pi$, $2/\pi \times 9.1 = 5.8$.) Under these conditions, secondary current was measured as $26.10mA_{rms}$, giving an reactance, $X_{Ls} = 9.1/(0.0261\sqrt{2}) = 246.5\Omega$. Therefore $L_s = X_{Ls}/2\pi f = 246.5/400\pi = 196.2$mH and $L_p = (1/58^2)L_s = 58.3\mu H$. These values are approximately eight times higher than those measured for the ferrite cores.

8.4 I_{mag}, B_{max} and μ_r

With a primary inductance of 58.3μH, LVPC no-load magnetising current, I_{mag}, should be $(V_p\Delta t)/(2L_p) = (0.55 \times 0.5 \times 10^{-3})/(2 \times 58.3 \times 10^{-6}) = 2.36A_{peak}$. This value is insignificant when compared with full-load input currents exceeding 100A, particularly as it acts in quadrature.

Maximum core flux density, $B_{max} = V_p/(4fN_pA_e) = 0.55/(4000 \times 5.18 \times 10^{-4}) =$ 265mT = 2650 gauss. Because core material properties do not affect B_{max}, this value is comparable to the flux density predicted for the ferrite core. The Magnetic Metals Superperm 49 material data sheet gives maximum usable flux densities of about 6 to 8 kilogauss.

Secondary inductance, $L_s = 196mH = \mu N_s^2 A_e/l_e$, so $\mu = (0.196 \times 0.147)/(58^2 \times 5.18 \times 10^{-4}) = 16.5$ mH/m. Relative permeability, $\mu_r = \mu/(0.4\pi \times 10^{-6}) = 13158$, representing a factor of eight improvement over the ferrite core. The Superperm 49 data sheet shows relative permeabilities exceeding 30000 are achievable at higher levels of induction.

The data sheet also shows that permeability is an exponential function of flux density. At 60Hz, B = 20, 200 and 2000 gauss correspond with $\mu_r \approx 6000$, 12000 and 24000, or $\mu_r \approx 2500B^{0.3}$. Another graph suggests that $\mu_{60Hz} \approx 1.7\mu_{1000Hz}$ (average) for inductions ranging from 10 to 4000 gauss, but that $\mu_{60Hz} \approx 2.0\mu_{1000Hz}$ at the higher inductions (2000 to 4000 gauss). Therefore at 1000Hz, and with B = 2000 to 4000

gauss, $\mu_r \approx 1250B^{0.3}$. For the LVPC transformer B = 2650, and $1250 \times 2650^{0.3} = 13300$. This value is in (remarkably!) close agreement with the $\mu_r = 13158$ calculated from measured inductance.

8.5 Core losses

The Superperm 49 data sheet gives the core loss of 0.014 inch laminations as 0.8W/lb when B = 2650 gauss and f = 1000Hz. With a volume of 80.9 cm^3 and a specific gravity of 8.38g/cm^3, the core should weigh 678g (1.50 lb) and dissipate $1.50 \times 0.8 = 1.20$W. The ferrite core was assumed to dissipate 0.44W (Section 5.1), so an increase of 0.76W is expected. At $V_{in} = 0.55$V, the additional loss should produce an increase of about 1.4A in no-load input current. The actual increase is 1.7A, or about 0.94W.

Insulating the laminations can only affect eddy current loss. However, doing so did not change the no-load current, so hysteresis may well be the principal core loss mechanism. Of course, eddy currents will still circulate – and dissipate power – because the laminations are conductive and of finite thickness. The ratio of these losses would be difficult (and probably pointless) to determine.

8.6 Test results

Table 8.1 and figure 8.1 summarize the test results for the Low Voltage Power Converter with a Superperm 49 core substituted for the Philips 3C90 core in the transformer assembly. Test conditions were as follows:

Transformer core	Magnetic Metals Superperm 49; 74 EI laminations.
Output inductor core	Neosid F5
Load resistance	Iskra 2.5A potentiometer ($104\Omega \geq R_{out} \geq 29.8\Omega$)
	Fixed 100W power resistors ($20.3\Omega \geq R_{out} \geq 3.6\Omega$)
Power source	500A DC power supply (2V battery with water cooled adjustable linear regulator)
Interconnections	Battery to LVPC and Battery to DCPS freshly cleaned

Test equipment — Fluke 87 DMM (voltage and resistance measurements)
Good Will GW037 current clamp (current measurements)
Tektronix 2232 oscilloscope (time measurements)

Table 8.1 LVPC Test results with Superperm 49 core.

Vin, V	Iin, A	Pin, W	Vout, V	Rout, Ω	Iout, A	Pout, W	Eff'y, %	tc1, µs	tc2, µs	(Ii-4)/Io
0.55	4.3	2.37	34.3	∞	0	0	0	0	0	
0.55	20.6	11.4	30.2	104	0.29	8.8	77.2	3.0	4.0	57.2
0.55	37.5	20.7	29.1	49.8	0.59	17.1	82.5	7.0	8.5	57.3
0.55	57.2	31.5	27.8	29.8	0.93	25.9	82.3	11.0	14.0	57.1
0.55	78.8	43.4	26.5	20.3	1.30	34.5	79.5	16.0	20.0	57.4
0.55	106	58.2	24.7	13.9	1.78	43.9	75.5	23.0	28.0	57.3
0.55	131	72.2	23.0	10.1	2.28	52.4	72.6	31.0	37.0	55.8
0.55	167	91.6	20.5	7.2	2.84	58.3	63.6	42.0	50.0	57.2
0.55	197	108.5	18.5	5.3	3.50	64.8	59.7	50.0	63.0	55.2
0.55	219	120.2	16.9	4.4	3.84	65.0	54.1	62.5	77.0	55.8
0.55	238	130.9	15.7	3.6	4.36	68.6	52.4	72.0	90.0	53.6

Notes

1. V_{in}, I_{in}, V_{out}, R_{out}, t_c1 and t_c2 are measured values. All other values are calculated from these.
2. DMM probe resistance of 0.2Ω has been subtracted from all R_{out} values. (e.g. 10.1Ω indicates an initial reading of 10.3Ω.)
3. t_c1 and t_c2 (t_{clamp1} and t_{clamp2}) are the intervals during which the output bridge clamps the transformer secondary to zero volts.
4. (I_i-4) is I_{in} minus the approximate load-independent current used by the transformer core and FET drive circuit. $(I_i-4)/I_o$ therefore approximates the effective input to output current transfer ratio of the LVPC.

Comparison of Table 8.1 with LVPC test results using a ferrite core transformer (Table 5.1) reveals three significant changes:

- Efficiencies at the lower power levels have fallen appreciably, primarily because the ~1W increase in core loss forms a significant fraction of output power.

- Output voltage has fallen by about 0.35V at most power levels, resulting in output power reductions of up to 5% at equivalent loads. However, reduced input currents at the heavier loads (above $P_{out} \approx 55W$) partially compensate for the lower output powers, producing efficiencies which average about 2% lower than their ferrite core counterparts.

• Falls in clamp interval t_c1 average nearly 13%, while the average drop in t_c2 is less than 3%. These reductions average about 8%, and imply a similar (and therefore small) reduction in transformer leakage inductance. As discussed in Section 5.2, differences in alternate clamp intervals may be a consequence of the non-symmetrical placement of the half-primary windings on the core. However, this does not fully explain why variations in core parameters would produce asymmetrical changes in clamp interval.

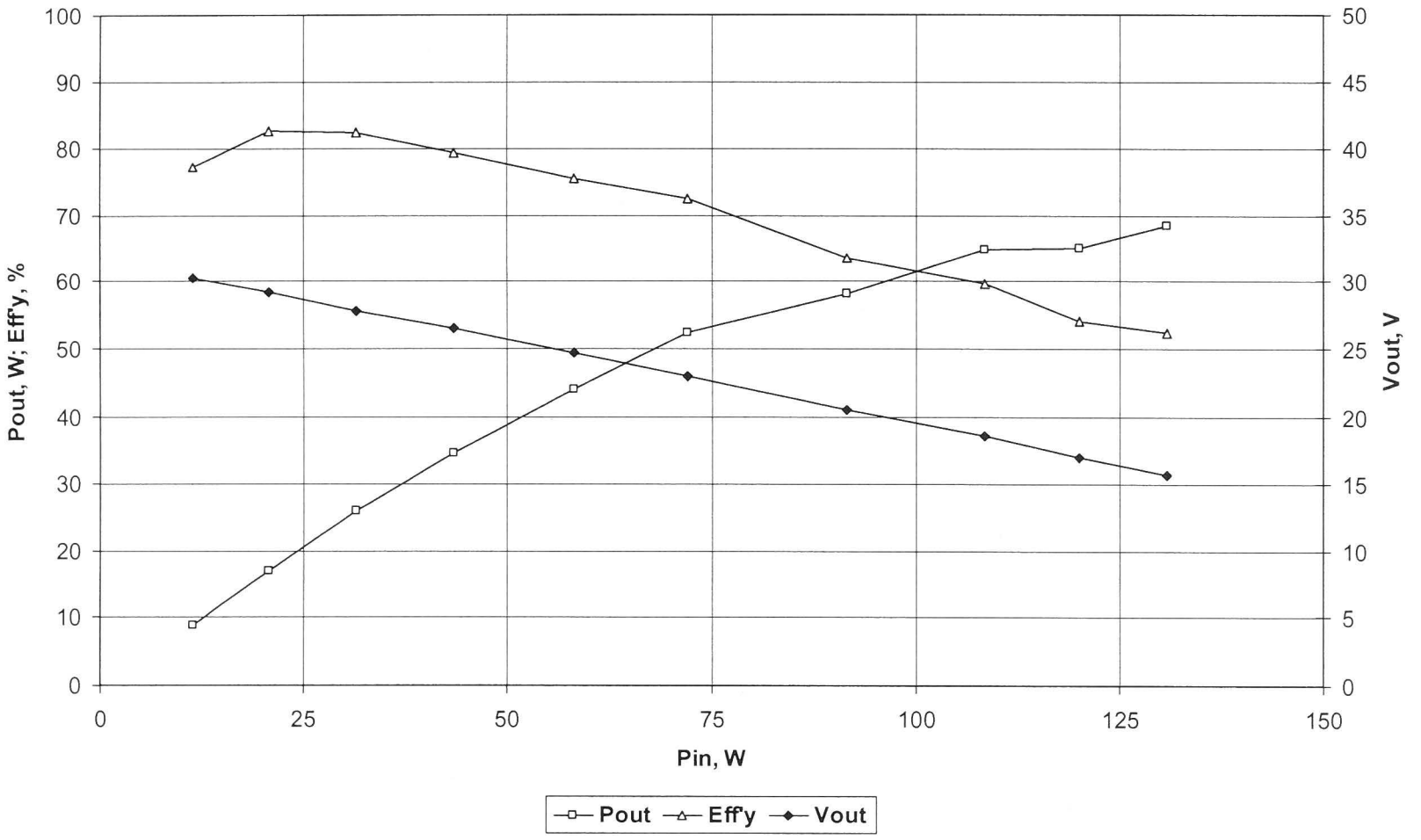


Figure 8.1 Output power, efficiency and voltage with the NiFe core.

Perhaps the most noticeable result is the *lack* of change. If the effects of increased core loss are removed (by reducing P_{in} by 1W), the most significant difference between the ferrite core and the nickel steel core is a 1.5% drop in efficiency at the 50W level. This contrasts sharply with the significant gains in power and efficiency which a reduced leakage inductance was expected to deliver. Unfortunately, the reduction in leakage inductance was nowhere near the hoped-for order of magnitude improvement.

8.7 Drive frequency reduction

The 1kHz drive frequency used for the ferrite core was retained for the NiFe core. This was done so that the effects of the core change could be evaluated in the absence of

other variables. Given that flux density is well below saturation, and magnetising current is also extremely low, it would seem that switching and possibly core losses might be reduced by lowering the drive frequency. But there are a few trade-offs.

Any reduction in frequency will bring about a corresponding increase in both magnetising current and flux density. According to the Superperm 49 data sheet, core loss (P_{fe}) is nearly proportional to the square of the induction at a given frequency, and also to the 1.65th power of frequency at a given flux density: $P_{fe} \propto (B_{max}^{2} \times f^{1.65})$. But B_{max} is inversely proportional to frequency, so core loss should be proportional to $f^{-2} \times f^{1.65} = f^{-0.35}$. Halving the frequency will therefore increase core loss by 27.5% (about 0.3W).

From Sections 5.1 and 6.2, at the 50W output power level switching losses total about 7W. This figure should decrease linearly with drive rate, so halving the frequency should save about 3.5 − 0.3 = 3.2W, a significant gain. However, rising magnetising current, core losses and saturation effects would ultimately impose a lower limit on frequency. This would probably occur when B_{max} exceeded 8 kilogauss, corresponding to a drive frequency of about 330Hz. Experimentation would be needed to determine the optimum drive frequency under a range of load conditions.

Lower drive frequency does not imply higher output power. Even if the NiFe cored transformer was capable of delivering higher currents (which it apparently isn't), a reduction in drive frequency would not result in increased output power handling capability unless output filtering was improved. The 1.9mH output inductor already produces $4V_{p\text{-}p}$ ripple at the 50W output level. At higher currents the ripple becomes excessive. If ripple is to be controlled at higher powers, either output filter inductance must be increased, or an LC filter section employed. Increasing the inductance without increasing losses would require a new, larger core (see Section 3.8). Decreasing the drive frequency would not increase ripple, as it is determined by the inductor's capacity to deliver current during the clamp interval. Clamp interval is governed by leakage inductance, which has not changed significantly.

8.8 "Missing" voltage

As discussed in Sections 6.4 and 7.3, a discrepancy exists between the measured and expected values of secondary voltage. This difference cannot be fully explained by the combined effects of IR and Ldi/dt drops, so an additional IdL/dt drop was postulated. This term relies upon a current (and therefore time) dependant leakage inductance, which was presumed to exist as a result of flux displacement within the ferrite core. It was hoped that increasing the core's permeability would reduce leakage inductance and, with it, the undesirable IdL/dt voltage loss.

In short, this didn't happen. With the NiFe core, permeability has increased by nearly an order of magnitude, while leakage inductance and voltage loss remain essentially unchanged.

New data pertaining to these affects is given in Table 8.2. I_{in} = 130.7A_{avg}, and P_{out} = 52W. Voltages were measured with a Tektronix 2232 oscilloscope at the mid point of successive drive pulses (250μs after each transition). Values of the form "nnnn/nnnn" reflect measurements made during alternate drive pulses.

Table 8.2 Circuit voltages with Superperm 49 cored transformer.

Parameter	Volts	Volts/Turn	Comments
V_{in}	0.540/0.535		Measured at input terminal bolt.
V_{ds}	0.025/0.020		MOSFET V_{ds} measured at leads.
$V_{sockets}$	0.014/0.014		Drop for drain + source pin sockets.
$V_{contact}$	0.006/0.006		Ground terminal connection loss.
V_p(driven)	0.495/0.495	0.495/0.495	Energised half-primary winding.
V_p(off)	0.470/0.475	0.470/0.475	De-energised half-primary winding.
V_{sense}	1.800/1.820	0.450/0.455	Unloaded dΦ/dt sense winding, N = 4
V_s	26.20/26.50	0.452/0.457	Secondary voltage.

Note that V_p(driven) − V_s(/turn) = 0.495/0.495 − 0.452/0.457 = 0.043/0.038, or 0.040V average. This is the same result as was previously obtained for the ferrite core

transformer. There has been no improvement. The IR component will remain unchanged, as will that portion of the Ldi/dt component associated with load current ramps (see Section 6.4). However, the reduction in I_{mag} should have resulted in a corresponding decrease in the Ldi/dt term associated with it. This is not seen, although the effect would be quite small (less than 5mV).

8.9 Dependence of V_{loss} upon I_{in}

Several loss mechanisms affecting the primary to secondary per-turn voltage drop can be readily identified. As discussed, these include IR drops in the primary and secondary, a magnetising current induced $L_{lp}dI_{mag}/dt$ loss in the primary, and an L_ldI_{out}/dt loss resulting from current ramps generated by the output filter inductor. Although these effects may not account for all the "missing" voltage, their relationship to it may shed some light on the problem. It is also worth noting that the difference between input power and output power almost exactly equals the sum of the individual losses from all identified causes (see Section 5.1). Apparently the missing voltage is not affecting the efficiency of the LVPC, and must therefore be the result of reactive circuit elements (e.g. leakage inductance).

It was proposed that load current dependent leakage inductance might be producing an additional IdL/dt component. It was also proposed that by substituting a core of higher permeability, leakage inductance could be reduced and, with it, the IdL/dt loss (Section 7.3). It was then established that a substantial increase in core permeability had negligible effect on voltage loss. However, it may be that leakage inductance, and its relationship to current, are not as dependent upon core permeability as was previously thought.

A non-linear inductance (leakage inductance in this case) can be modelled as

$$L = L_0(1 + \alpha I^n) \qquad [8-1]$$

where L_0 is the zero-current inductance, α is a constant, and I is the inductor current (Jeffrey Harris, pers. comm.). In general, inductor voltage is given by

$$V_L = LdI/dt + IdL/dt. \qquad [8-2]$$

Combining [8−1] with [8−2] yields

$$V_L = [1 + (n+1)\alpha I^n]L_0 dI/dt. \qquad [8-3]$$

The dI/dt term will normally differ between primary and secondary. This is because magnetising current dI_{mag}/dt interacts only with primary leakage inductance, whereas secondary dI_s/dt also transfers to the primary, and will therefore develop a voltage across both primary and secondary leakage inductances. Calculations are greatly simplified if the secondary is treated as a single turn, carrying half the total transformer leakage inductance. In this case, $L_{ltot} = L_{lp} + L_{ls}' = 2L_{lp} = 2L_{ls}'$, where $L_{ls}' = L_{ls}/58^2$ (see Section 5.2). If V_L is taken at mid-cycle, $i_{mag}(t) \approx 0$ because the current ramp is crossing zero. Also, at mid-cycle $I_s' \approx I_{in}$, where I_s' is the secondary current referred to the primary ($I_s' = 58I_s$).

For the LVPC transformer, these "simplifications" yield:

$$V_{Ltot} = [1 + (n+1)\alpha I_{in}^n][L_{lp0}dI_{mag}/dt + 2L_{lp0}dI_s'/dt]. \qquad [8-4]$$

At a given input voltage and drive frequency, dI_{mag}/dt is constant. For the ferrite core transformer, $I_{mag} = 19.1A_p$. Therefore, $dI_{mag}/dt = 38.2A/500\mu s = 76{,}400A/s$. Also, $V_{out}t_c/L_{out} = \Delta I_s$, and $\Delta I_s/500\mu s \approx dI_s/dt$ during the conduction interval. If V_{out} is taken as 26.0V and L_{out} as 1.91mH, $dI_s/dt = (27.2\times10^6)t_c$. For the ferrite core at $V_{in} = 0.55V$ and $18.6 \le I_{in} \le 169A$, Table 5.1 indicates that the $t_c \approx (0.165\times10^{-6})I_{in}^{1.1}$. This slight non-linearity is probably a consequence of the dependence of L_l upon I_{in}. Consequently, $dI_s/dt = 4.49I_{in}^{1.1}$, and $dI_s'/dt = 58dI_s/dt = 260I_{in}^{1.1}$. With these assumptions, $V_{Ltot} = [1 + (n+1)\alpha I_{in}^n][76{,}400L_{lp0} + 520I_{in}^{1.1}L_{lp0}]$, or

$$V_{Ltot} = L_{lp0}[1 + (n+1)\alpha I_{in}^n][76{,}400 + 520I_{in}^{1.1}]. \qquad [8-5]$$

For the NiFe core, $dI_{mag}/dt = 4.72A/500\mu s = 9{,}440A/s$. If V_{out} is again taken as 26.0V and L_{out} as 1.91mH, $dI_s/dt = (27.2\times10^6)t_c$. For the NiFe core operating at $V_{in} = 0.55V$ and $20.6 \leq I_{in} \leq 167A$, Table 8.1 shows that $t_c \approx (0.097\times10^{-6})I_{in}^{1.2}$. Therefore, $dI_s/dt = 2.64I_{in}^{1.2}$ and $dI_s'/dt = 58dI_s/dt = 153I_{in}^{1.2}$. As before, $V_{Ltot} = [1 + (n+1)\alpha I_{in}^{n}][9{,}440L_{lp0} + 306I_{in}^{1.2}L_{lp0}]$, or

$$V_{Ltot} = L_{lp0}[1 + (n+1)\alpha I_{in}^{n}][9{,}440 + 306I_{in}^{1.2}]. \qquad [8\text{–}6]$$

Transformer voltage loss is assumed to consist of two components: an IR drop and a voltage produced by the interaction of leakage inductance with changing primary and secondary current. The IR losses are easy to estimate. If these are subtracted from the total loss, only the inductive losses should remain. A comparison of inductive losses with input current proved instructive. The results are given in Tables 8.3 and 8.4 for both the ferrite and NiFe cores.

An estimation of primary voltage was obtained by subtracting the total resistive losses in the primary drive circuit from the input voltage (see Section 6.2). This value, $V_p(est)$, is $V_{in} - I_{in}(R_{con} + R_{bar} + R_{ds} + R_{soc}) = V_{in} - (I_{in} \times 332\mu\Omega)$. The secondary voltage can be estimated from the average (mid-cycle) output voltage and clamp interval. From Section 6.2, the average output voltage, $V_{out} = V_{s-f} \times (500\mu s - t_c)/500\mu s$, where $(500\mu s - t_c)/500\mu s$ is the conduction duty cycle of the output filter inductor (DutCyc in Tables 8.3 and 8.4). Therefore, secondary voltage can be estimated as $(V_{out}/DutCyc) + V_f$. A better estimation should result if resistive losses in the output inductor are included. The resistances are R_L (124mΩ), R_{feL} (13.1mΩ), and an assumed circuit board track and contact resistance of 100mΩ, giving a total of 0.24Ω. Therefore, a mid-cycle secondary voltage of $V_s(est) = (V_{out}/DutCyc) + 0.6 + 0.24I_{out}$ is assumed. For a more useful comparison with primary voltage, $V_s(est)$ was divided by the turns ratio (58:1) to yield secondary volts per turn, V_s/N.

The difference between $V_p(est)$ and V_s/N is the total transformer voltage loss. Figures so obtained are in reasonably close agreement with measured values (54mV vs. 40mV for ferrite at $I_{in} = 131A$). However, some of this loss is caused by primary and secondary resistance, R_p (41.5μΩ) and R_s (85.6mΩ). By reflecting R_s to the primary, a

single value governing resistive loss per turn is obtained: $R_p + 58^{-2}R_s = R_{p+s} = 66.9\mu\Omega$. This combined resistance will produce a per-turn voltage loss, $V_s(IR) = I_{in} \times 66.9\mu\Omega$, which must then be subtracted from $V_p(est) - V_s/N$ to give the inductive loss per turn, V_{sL}/N. That is, $V_{sL}/N = V_p(est) - V_s/N - V_s(IR)$. This figure was then compared with I_{in} to determine the nature of the dependence.

Table 8.3 Estimated transformer voltage loss with Ferrite Core.

Vin	Iin	Vout	Iout	tc(avg)	DutCyc	Vp(est)	Vs(est)	Vs/N	VsIR	VsL/N	αI^1.25
0.551	18.6	30.36	0.29	4.25	0.992	0.545	31.29	0.539	0.001	0.004	0.004
0.551	35.7	29.34	0.59	8.75	0.983	0.539	30.60	0.528	0.002	0.009	0.009
0.550	55.1	28.13	0.94	13.5	0.973	0.532	29.74	0.513	0.004	0.015	0.015
0.551	77.6	26.83	1.33	19.5	0.961	0.525	28.84	0.497	0.005	0.023	0.023
0.549	105	25.03	1.79	27.5	0.945	0.514	27.52	0.474	0.007	0.033	0.034
0.550	131	23.37	2.31	35.0	0.930	0.507	26.28	0.453	0.009	0.045	0.044
0.551	169	20.98	3.00	47.5	0.905	0.495	24.50	0.422	0.011	0.061	0.061
0.551	200	18.90	3.57	60.0	0.880	0.485	22.93	0.395	0.013	0.076	0.075
0.550	222	17.28	3.93	73.0	0.854	0.476	21.78	0.375	0.015	0.086	0.086
0.549	241	16.00	4.10	87.0	0.826	0.469	20.96	0.361	0.016	0.092	0.095

Table 8.4 Estimated transformer voltage loss with NiFe Core.

Vin	Iin	Vout	Iout	tc(avg)	DutCyc	Vp(est)	Vs(est)	Vs/N	VsIR	VsL/N	αI^1.15
0.551	20.6	30.2	0.29	3.5	0.993	0.544	31.09	0.536	0.001	0.007	0.006
0.551	37.5	29.1	0.59	7.8	0.985	0.539	30.34	0.523	0.003	0.013	0.013
0.550	57.2	27.8	0.93	12.5	0.975	0.531	29.32	0.505	0.004	0.022	0.021
0.551	78.8	26.5	1.30	18.0	0.964	0.525	28.37	0.489	0.005	0.030	0.030
0.550	106	24.7	1.78	25.5	0.949	0.515	27.06	0.467	0.007	0.041	0.043
0.551	131	23.0	2.28	34.0	0.932	0.508	25.82	0.445	0.009	0.053	0.054
0.550	167	20.5	2.84	46.0	0.908	0.495	23.84	0.411	0.011	0.073	0.072
0.551	197	18.5	3.50	56.5	0.887	0.486	22.33	0.385	0.013	0.087	0.087
0.550	219	16.9	3.84	69.8	0.861	0.477	21.17	0.365	0.015	0.098	0.098
0.550	238	15.7	4.36	81.0	0.838	0.471	20.39	0.352	0.016	0.103	0.108

Tables 8.3 and 8.4 show that an extremely good approximation for inductive voltage loss per turn, V_{sL}/N, is given by αI_{in}^{n}. For the ferrite core $V_{sL}/N \approx 0.0001 I_{in}^{1.25}$, whereas $V_{sL}/N \approx 0.0002 I_{in}^{1.15}$ for the NiFe core. These expressions confirm the non-linearities described by equations [8−5] and [8−6].

It should be possible to estimate variables L_{lp0}, n and α in [8−5] and [8−6] by solving these expressions at three points. By assuming $I_{in} = 0$ at no load, L_{lp0} will be determined solely by V_{Ltot} (represented as V_{sL}/N in Tables 8.3 and 8.4). Then, with L_{lp0} known, the expressions can be recomputed at $I_{in} = 131A$ (heavy load) and some other intermediate value. Values for n and α may then be found by simultaneous solution. Unfortunately, V_{Ltot} must be measured as a difference between the predicted secondary volts/turn and the actual value. This difference (the I_{mag} contribution to V_{Ltot}) is only a few millivolts at no-load, and cannot be reliably measured as a change in the ~500mV/turn on the secondary.

An alternative method of estimating L_{lp0}, n and α is by solving these expressions at three different currents. This would involve a tedious iterative approach, as n appears as both factor and exponent. A more expedient (albeit slightly dodgy) approach is to assume a value for n, based upon the empirical formulas for V_{sL}/N given in Tables 8.3 and 8.4. With n "known", only two currents are required to obtain a solution. For the ferrite core transformer, these will be taken as $I_{in} = 18.6A$ and 131A. In the first case, $V_{Ltot} = V_{sL}/N = 0.004 = L_{lp0}[1 + (n+1)\alpha 18.6^{n}][76{,}400 + 520(18.6)^{1.1}]$. Because $V_{sL}/N \approx 0.0001 I_{in}^{1.25}$, n = 1.25 will be assumed. Therefore,

$0.004 = L_{lp0}[1 + (1.25+1)\alpha 18.6^{1.25}][76{,}400 + 520(18.6)^{1.1}] = L_{lp0}[89{,}356 + 7{,}764{,}590\alpha]$, and

$0.045 = L_{lp0}[1 + (1.25+1)\alpha 131^{1.25}][76{,}400 + 520(131)^{1.1}] = L_{lp0}[187{,}318 + 186{,}793{,}443\alpha]$.

Simultaneous solution gives $\alpha = 0.00823$ and $L_{lp0} = 26.1nH$. The expression for V_{Ltot} becomes:

$$V_{Ltot} = 26.1\times10^{-9}[1 + 0.0185 I_{in}^{1.25}][76{,}400 + 520 I_{in}^{1.1}]. \qquad [8-7]$$

This seems plausible, as it gives fairly good agreement at intermediate points. At $I_{in} = 55.1A$, $V_{Ltot} = 0.012V$. ($V_{sL}/N = 0.015V$ at the same current.) Although [8−7] includes a value for L_{lp0} which is on the low side, it is still "believable". If n = 1.25, $\alpha = 0.00823$, and $L_{lp0} = 26.1nH$ are applied to expression [8−1] at $I_{in} = 131A$, $L_{lp131} = 26.1\times10^{-9}(1 + 0.00823(131)^{1.25}) = 121nH$. ($L_{lp}$ was estimated as 68.6nH at $I_{in} = 131A$ in Section 5.2.)

For the NiFe core transformer, I_{in} = 20.6A and 131A will be used. $V_{Ltot} = V_{sL}/N$ = $0.007 = L_{lp0}[1 + (n+1)\alpha 20.6^{n}][9{,}440 + 306(20.6)^{1.2}]$. Because $V_{sL}/N \approx 0.0002I_{in}^{1.15}$, n = 1.15 will be assumed. Therefore,

$0.007 = L_{lp0}[1 + (1.15+1)\alpha 20.6^{1.15}][9{,}440 + 306(20.6)^{1.2}] = L_{lp0}[20{,}984 + 1{,}463{,}015\alpha]$, and

$0.053 = L_{lp0}[1 + (1.15+1)\alpha 131^{1.15}][9{,}440 + 306(131)^{1.2}] = L_{lp0}[115{,}719 + 67{,}718{,}690\alpha]$.

Simultaneous solution gives $\alpha = 0.000762$ and L_{lp0} = 317nH. The expression for V_{Ltot} becomes:

$$V_{Ltot} = 317\times10^{-9}[1 + 0.00164I_{in}^{1.15}][9{,}440 + 306I_{in}^{1.2}]. \qquad [8\text{–}8]$$

At first glance, this too seems reasonable, as it also gives fairly good agreement at intermediate points. At I_{in} = 57.2A, V_{Ltot} = 0.018V. (V_{sL}/N = 0.022V at I_{in} = 57.2A.) However, if n = 1.15, α = 0.000762, and L_{lp0} = 317nH are applied to expression [8–1] at I_{in} = 131A, $L_{lp131} = 317\times10^{-9}(1 + 0.000762(131)^{1.15})$ = 383nH. This value for L_{lp131} is far from that predicted by input current and clamp interval ($L_{lp} \approx 0.55t_c/2I_{in}$ = 71nH). While it is possible that a higher but more stable leakage inductance is forcing the LdI/dt term to dominate, it is more likely that the n = 1.15 assumption is incorrect.

Leakage inductance (as determined from clamp interval) has not been significantly reduced by the exchange of core materials, even though permeability has increased by a factor of eight. However, it is clear that voltage loss is a non-linear function of input current. Although the nonlinearity of this dependence is fairly weak, the relationship appears to support the proposition that transformer leakage inductance is changing with load and/or magnetising current. It may also be possible that the inductance being measured is not within the transformer, but external to and in series with it. In this case it should more properly be called stray inductance.

Empirical first order approximations for loss voltage vs. input current fit very well, while variables associated with the theoretically derived current dependence have only been loosely identified. Attempts at a more convincing three-point iterative solution have proved extremely difficult. Because of the uncertainties, a precise explanation of the contributing effects must await further data relating to transformer input and output

voltages under a range or load conditions. With existing data, it may be impractical to determine the unknown constants in expressions [8−5] and [8−6] with sufficient accuracy.

9 Conclusions

A DC-DC converter optimised for operation from the 0.5 to 0.6V output of a single photovoltaic cell or parallel solar array has been designed and built. Converter efficiencies of 75% at 50W and 87% at 25W have been achieved. The device has operated reliably for several years with inputs ranging from 0.3 to 0.8V and from 2 to 300ADC, and with outputs which include both open and short circuits.

The design of the DC-DC converter was analysed, and the function of all major components and sub-circuits was described. The design and analysis of magnetic components was given particular attention.

Operation was characterised for outputs from 7 to 81W, and circuit losses were identified and quantified. Models were developed for the transformer and for the circuit as a whole. These models were then used to predict operation with reasonable success. Discrepancies between predicted and measured results led to the development of an hypothesis identifying flux displacement in the transformer core as a possible source of variable leakage inductance. It was hoped this effect might explain an observed loss in secondary voltage. Subsequent tests using a nickel steel core showed that an eight-fold increase in permeability had little effect. However, further analysis of the data revealed that the inductive component of transformer voltage loss is a weak non-linear function of input current. This implies that leakage inductance variation is at least a contributing factor.

Inductance, both stray and leakage, was found to play a significant and detrimental role in the operation of the LVPC. Stored magnetic energy contributed to switching losses and caused increased power to be dissipated in the input filter capacitors. Inductance was found to be responsible for an excessive primary current reversal time, which lowered efficiency by reducing the primary drive duty cycle. Leakage inductance also acted to reduce the output voltage of the transformer, and it prevented the implementation of a promising antisaturation technique.

A new flux zero-crossing flyback technique for the prevention of staircase saturation in transformer cores was developed and presented.

A low voltage, high current adjustable regulated DC power supply was designed and constructed as a source of power for the low voltage DC-DC converter. This supply was designed to provide an output of 0 to 1VDC at currents up to 500A with a response time of 200ns. This device has also been in operation for three years, delivering currents up to 300A. It has survived a short circuit current estimated to be 2000ADC.

The electrical and thermal aspects of the 500A DC power supply design were discussed, and performance specifications were provided.

Finally, a brief analysis of the commercial possibilities of the low voltage power converter was given. Several design changes were proposed which could ultimately reduce the cost of production.

References

1. Billings, K. H.: *Switchmode Power Supply Handbook*, McGraw-Hill Publishing Co., New York, 1989.

2. Bird, B. M.; King, K. G.; Pedder, D. A. G.: *An Introduction to Power Electronics*, John Wiley & Sons, Chichester, Second Edition, 1983.

3. Duffin, W. J.: *Electricity and Magnetism*, McGraw-Hill Publishing Co. Ltd., London, 1965.

4. Flanagan, W. M.: *Handbook of Transformer Applications*, McGraw-Hill Book Co., New York, 1986.

5. Gottlieb, I. M.: *Electric Motors and Control Techniques*, TAB Books, Division of McGraw-Hill, Inc., New York, Second Edition, 1994.

6. Grove, A. S.: *Physics and Technology of Semiconductor Devices*, John Wiley and Sons, New York, 1967.

7. Hayt, W. H.: *Engineering Electromagnetics*, McGraw-Hill Book Co., Inc., New York, Second Edition, 1967.

8. Hayt, W. H.; Kemmerly, J. E.: *Engineering Circuit Analysis*, McGraw-Hill Book Co., Inc., New York, 1962.

9. Krein, P. T.: *Elements of Power Electronics*, Oxford University Press, Inc., New York, 1998.

10. Meyer, T.; Schmidt, H.: "New Low-Voltage DC-DC Converter", Fraunhofer ISE, Press and Public Relations web page: http://www.ise.fhg.de/press s_Info/pi199.html.

11. *Reference Data for Radio Engineers*, Howard W. Sams & Co., Inc., Indianapolis, Fifth Edition, 1968.

12. Shepard, M. H.; Williamson, R. C.: "Very Low Voltage Power Conversion," *IEEE ISCAS Proceedings*, 2001.

13. Williams, B.W.: *Power Electronics*, McGraw-Hill Inc., Second Edition, 1992.

Acknowledgments

I would like to thank (in ascending order of name length):

Will Keogh, for providing information about solar cells, for listening to my numerous "theories", and for not being too upset that I appropriated his parallel cell DC-DC converter idea in the first place.

Jeff Harris, for his interest in the project and helpful suggestions concerning the current dependence of leakage inductance, and for alerting me to the possibility of weird things such as phase-change-like effects in transformer core materials.

Bruce Mascord, for enthusiastically fabricating the LVPC primary/drain/source bars and DCPS heatsink/water tank.

Bob Williamson, for technical and editorial assistance throughout the project, notwithstanding his strange penchant for LaTeX, which nearly finished me.

Andrew Blakers, for advising me on various aspects of PV technology, for providing guidance on the draft thesis, and for believing in the project enough to give me $300 towards a 240V alternator I never used.

Boyd Blackwell, for bringing various leakage inductance minimisation techniques to my attention (at just the right time), and for his sound advice concerning improvements to the circuit model and directions for further investigation.

Darius Krivanek, for his advice and assistance on many aspects of material properties and fabrication techniques.

Mick Cardew-Hall, for his support, and for allowing me to take time away from an already under-staffed department to work on this project.

Zbigniew Stachurski, for helping me to keep focussed on the project at times when "real" work threatened to get in the way.

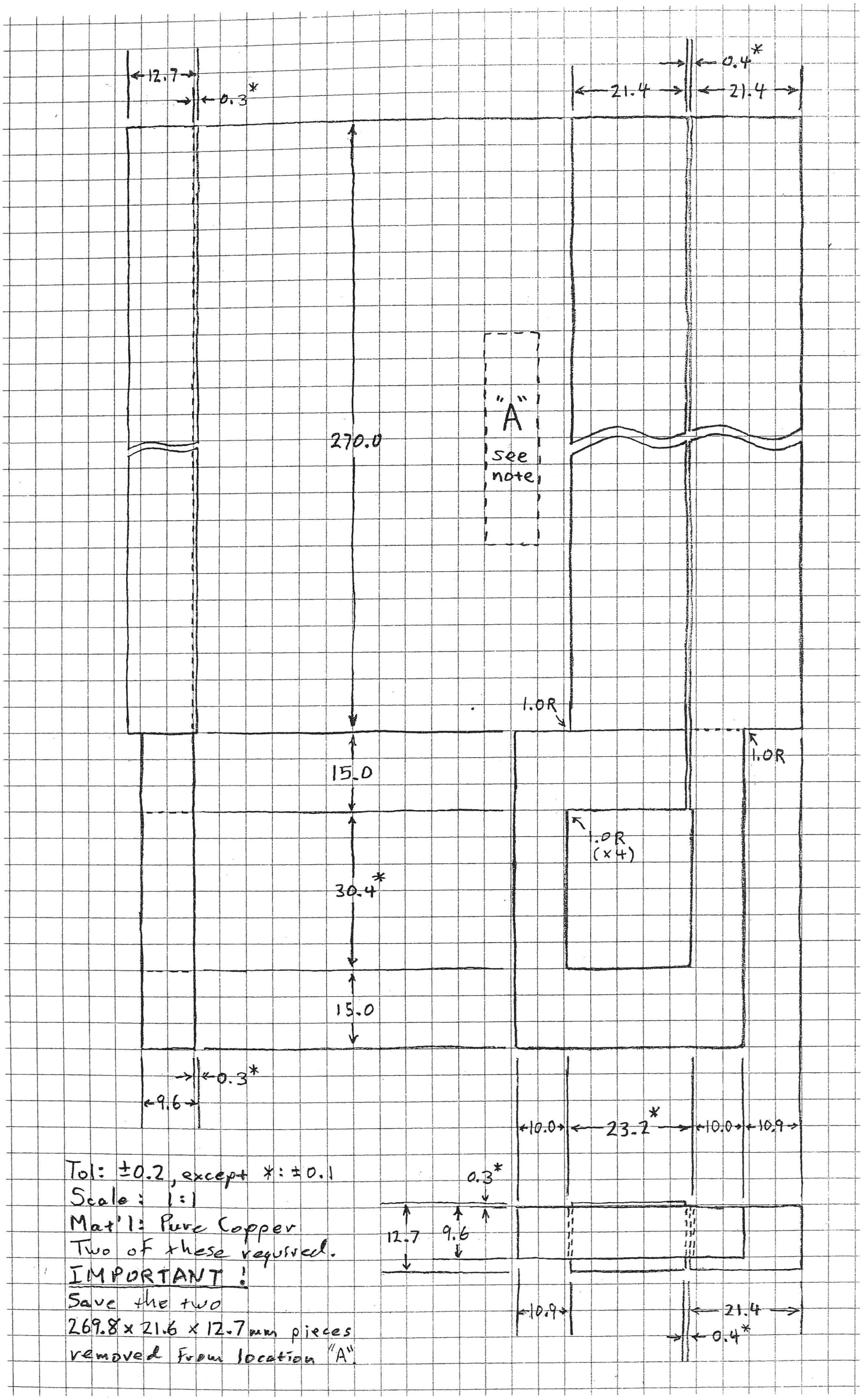
Appendix I Low Voltage Power Converter – List of Materials

Description	Part Number	Mfgr/Vendor	Qty.	Price Ea.	Comments
E65/32/27 core half	020 55481	Philips	4	6.00	3C90 mat'l
E65/32/27 coil former	021 28732	Philips	2	1.00	
Primary, machined		ANU	2	35.00	Estimate
Magnet wire, 1.5mm	146-533	Farnell	19m	0.72/m	
Magnet wire, 0.25mm	146-524	Farnell	4.3m	0.03/m	
Schottky diode, 60A/45V	MBR6045	Motorola	4	8.54	
Ult Fast diode, 6A/100V	UF601	Farnell	2	3.01	
Rectifier diode, 1A/400V	1N4004		6	0.10	
Zener diode, 6.8V, 5mA	BZX79C6V8	Philips	1	0.07	
Power MOSFET, 6mΩ	PHP130N03T	Philips	100	5.47	
Power BJT, NPN	BDT81	Philips	2	6.46	
Power BJT, PNP	BDT82	Philips	2	8.47	
Switching BJT, NPN	2N3904	RS	1	0.46	
Switching BJT, PNP	2N3906	RS	1	0.40	
FET driver IC	TC4422	TelCom	2	13.65	
Quad NAND gate	74LS00		1	0.67	
Dual D flip flop	74LS74		1	0.88	
Dual multivibrator	74LS123		1	1.61	
Positive regulator, 5V	78L05		1	1.35	
Res, 0.47Ω, ¼W, 5%	R47		2	0.10	
Res, 1.0Ω, ¼W, 5%	1R0		2	0.05	
Res, 10Ω, 1W, 5%	131-716	RS	2	0.20	
Res, 1KΩ, ¼W, 5%	1K0		1	0.05	
Res, 10KΩ, ¼W, 5%	10K		3	0.05	
Res, 22KΩ, ¼W, 5%	22K		1	0.05	
Res, 100KΩ, ¼W, 5%	100K		2	0.05	
Cap, 4.7mF, 25V, Alum	315-0669	RS	3	5.41	Low ESR
Cap, 1.0mF, 25V, Alum	108-837	Farnell	1	4.48	
Cap, 100μF, 25V, Tant			2	4.89	
Cap, 10μF, 16V, Tant	966-721	Farnell	1	0.56	
Cap, 10μF, 63V, Poly	303-8051	Farnell	2	9.45	
Cap, 0.1μF, 50V Cer	146-227	Farnell	4	0.96	
Cap, 68nF, 63V Poly	115-017	RS	1	0.67	
Cap, 10nF, 63V, Cer	237-279	Farnell	3	0.41	
Cap, 100pF, 100V, Cer	126-922	RS	1	0.60	
Switch, SPSTMC	219-344	Farnell	1	7.25	
Battery holder, 9V	301-103	Farnell	1	2.97	
Battery, 9V, alkaline	PP9	RS	1	4.73	
Binding post, red/black	148-250/251	Farnell	2	4.38	
PCB standoff, 7x13mm	627-150	Farnell	5	4.34	
Heatsink, 10°C/W	595-834	Farnell	4	2.06	TO-3P type
Insulating pads, TO-3P	681-090	Farnell	4	0.64	
Circuit board			1	20.00	Estimate
Misc. hardware			-	10.00	Estimate
Enclosure	129-640	RS	1	65.80	
Total materials cost				$969.54	

Appendix II 500A DC Power Supply – List of Materials

Description	Part Number	Mfgr/Vendor	Qty.	Price Ea.	Comments
Battery, 2V, 600Ahr		Sonnenschein	2	407.50	35kg each
Power MOSFET, 250A	STE250N06	SGSThomson	4	115.00	R_{ds} = 3mΩ
High GBWP op-amp	HA3-2842-5	Harris	4	15.00	Hard to get
Op-amp	LM-741		1		
LED, red			1		
Cap, 4.7mF, 25V, Alum	315-0669	RS	1	5.41	Low ESR
Cap, 10μF, 16V, Tant	966-721	Farnell	3	0.56	
Cap, 1μF, 25V, Tant			1		
Cap, 100nF, 63V, Poly			10		
Cap, 22nF, 63V, Poly			4		
Cap, 1nF, 63V, Poly	114-929	RS	1	0.47	
Cap, 100pF, 100V, Cer	126-922	RS	1	0.60	
Res, 0.5mΩ, 10W, 5%		ANU	4		0.9mm copper
Res, 10Ω, ¼W, 5%	10R		1	0.05	
Res, 100Ω, ¼W, 5%	100R		6	0.05	
Res, 470Ω, ¼W, 5%	470R		4	0.05	
Res, 1KΩ, ¼W, 5%	1K0		1	0.05	
Res, 2.7KΩ, ¼W, 5%	2K7		1	0.05	
Res, 10KΩ, ¼W, 5%	10K		5	0.05	
Pot, 1T, 10KΩ, ½W			1		
IC socket, 14 pin			5		
PCB terminal block			2		2-way
PCB pin sockets		Harwin	16		
Hook up wire, 0.5mm			15cm		
Crimp connector, ring			1		
Circuit board		ANU	1		
Drain connector bar		ANU	1		0.9mm copper
Output connector bar		ANU	1		0.9mm copper
Heatsink/water tank		ANU	1		10mm alumin.
Insulating support plate		ANU	2		10mm acrylic
SS bolt, 10mm x 25mm			2		
SS nut, 10mm			2		
SS washer, 10mm			2		
Misc. hardware			-		

Appendix III Transformer Primary and Supply/Drain Bars



Tol: ±0.2, except *: ±0.1
Scale: 1:1
Mat'l: Pure Copper
Two of these required.

IMPORTANT !

Save the two
269.8 x 21.6 x 12.7 mm pieces
removed From location "A".