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Dynamic Load Modulation Scheme for Digital Transmitters

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FOR JURY EVALUATION

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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July 31, 2018

Resumo

A crescente necessidade de se obter um maior desempenho energético e de se atingir um valor de débito de dados cada vez mais elevado motivou o desenvolvimento de soluções capazes de satisfazer essas necessidades. Além disso, tendo em conta o congestionamento do espetro que se observa atualmente, os standards de ligações de redes sem fios RF tendem a utilizar modulações complexas. Estes sinais tendem a possuir um valor de razão entre potência de pico e a potencia media muito alto, o que por si só é uma propriedade problemática, já que, quando há um desvio do pico de potência do sinal, existe uma degradação de eficiência no transmissior. Esta é causada pelo elemento responsável pelo maior consumo de potência na cadeia de transmissão: o amplificador de potência (PA). Desta forma, surge a necessidade e a motivação para desenvolver técnicas capazes de aumentar a eficiência do PA quando este se desvia da potência de pico. Assim, ao longo desta dissertação, umas dessas técnicas, mais concretamete a técnica de modulação dinâmica de carga discreta, será abordada e desenvolvida.

Nesta dissertação, é, então, proposto o dimensionamento de uma rede dinâmica de carga utilizando o algoritmo Particle Swam Optimization (PSO). A rede resultante deverá apresentar três níveis de impedância diferentes (10Ω, 20Ω e 30Ω), a mesma fase da corrente na antena, e uma eficiência intrínseca elevada. Os resultados preliminares foram testados e validados utilizando o ambiente de simulação Cadence Virtuoso com modelos BSIM. De forma a melhor a fiabilidade das soluções obtidas, foram feitas alterações ao algoritmo de optimização, no sentido de se permitir que este faça a optimização das variáveis diretamente num ambiente de simulação. Isto permite obter soluções que usam modelos reais de componentes, tais como PCB traces e modelos de bondwires. Quando se obteve a solução final, foi realizada uma implementação física em tecnologia CMOS 180nm e esta foi depois enviada para fabrico. Surgiu, assim, a necessidade de desenvolver um ambiente de teste para posterior avaliação do circuito integrado, que teve por base o desenvolvimento de um algoritmo de de-embedding. Para os níveis de impedância de 10Ω e de 20Ω, os valores de impedância de entrada alvo foram atingidos com um erro inferior a 5%. No entanto, para o nível de 30Ω esse valor de erro já ronda os 15%. Ambos os níveis de impedância mostram uma eficiência intrínseca superior a 86% e uma diferença de fase na corrente de saída inferior a 1.2°.

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Abstract

New solutions to solve the demand for increasing user data rate transfer and throughput are required. Thus, in order to attain a best use of the frequency spectrum, strict wireless standards must be employed. These signals tend to have a high peak-to-average power ratio (PAPR), which is a troublesome property since as soon as signal deviates from its peak power, a efficiency degradation on the transmitter chain can be noted. This efficiency degradation on the transmission chain is caused by its most power hungry element, the power amplifier. This in turn has a critical impact on the battery duration of mobile devices. Hence, the motivation for the development of techniques capable of improving the power back-off (PBO) efficiency of the PAs arises. Thus, one of such techniques, discrete dynamic load modulation, was studied and developed during this dissertation.

In this dissertation it is proposed the design of a discrete dynamic matching network topology, suitable for CMOS integration. The resulting matching network (MNT) should have three distinct impedance values (10Ω, 20Ω and 30Ω), the same current phase in the antenna between these levels and an high intrinsic efficiency. This will be attained using the particle swarm optimimzation algorithm (PSO). Preliminary results were tested and validated on the Cadence Virtuoso simulator with BSIM models. In order to improve the quality of the computed solutions, the original algorithm was modified to use computer aided design environment (ADS) to account for circuit parasitics. This allows the usage of real components, PCB traces and bond-wire models. With the final computed solution, a physical implementation was carried out in a 180nm CMOS technology, sent to tape-out. This in turn motivated the development of a setup capable of testing the fabricated IC. Therefore, a de-embedding strategy was developed in order to measure the input impedance, efficiency and phase distortion using a vector network analyzer (VNA). In terms of final results, for the 10Ω and 20Ω the target input impedance was achieved with an error smaller than 5%, while for 30Ω the error was around 15%. All the three different impedance levels were able to attain and intrinsic efficiency higher than 86% and an current phase difference lower than $1.2°$.

Acknowledgments

I would like to thank to my supervisor Cândido Duarte, for supporting me although this dissertation and for creating opportunities that allowed me to develop this work. Also, I would like to thank my co-supervisor Rui Gomes, for his guidance, knowledge and friendship whom were essential to achieve the presented results. I would also like to thank my family, pretty much for everything.

Rafael Santos

'Events may appear to us to be random, but this could be attributed to human ignorance about the details of the processes involved."

Brian S. Everitt

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Abreviaturas e Símbolos

ac	Alternating current
ADS	Advanced design system
CMOS	Complementary metal-oxide-semiconductor
DAC	Digital to analog converter
dc	Direct current
DDLM	Discrete dynamic load modulation
DDMNT	Discrete dynamic matching network
DLM	Dynamic load modulation
DMNT	Dynamic matching network
DPA	Digital power amplifier
DUT	Device under test
ET	Envelop tracking
IC	Integrated circuit
IoT	Internet of things
MNT	Matching network
OFDM	Orthogonal-frequency-division-multiplexing
PA	Power amplifier
PAPR	Peak-to-average power ratio
PBO	Power back-off
PCB	Printed circuit board
PSO	Particle swarm optimization
RF	Radio frequency
SoC	System on chip

Chapter 1

Introduction

1.1 Context

The internet of things (IoT) paradigm [1] aims to provide to all sorts of consumer electronics device and home appliances internet connectivity. To realize the full potential of IoT paradigm, researchers and practitioners need to address several challenges and develop suitable conceptual and technological solutions for tackling them, like developing reconfigurable architectures. This, in turn, creates a market necessity for small, cheap and efficient transmitters. Indeed, the efficiency is a key word, since most of those "things" are low-power portable devices, thus it would be unpractical to add a extra functionality, that not only is not vital for the primary purpose of the device but also jeopardizes the overall devices system autonomy. Furthermore with the eminent deployment of the 5G communications paradigm [2], complex but spectral efficient modulations will emerge imposing linearity constraints be attained by the transmitter. The CMOS benefits from efficient area usage, low manufacturing cost and widely available signal processing capabilities. Recently, all-digital transmitters front-ends were successfully reported, allowing the integration of the power amplifier (PA) with the rest of the circuitry (baseband), hence performing the true system-on-chip (SoC) transceiver. The PA the electronic block responsible for amplifying the RF signal to adequate levels before driving the antenna, as seen in Fig. 1.1.
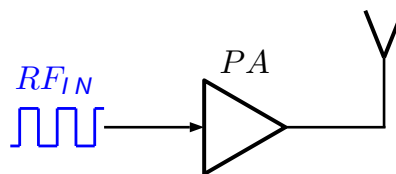
Figure 1.1: Simplified transmitter chain

Indeed this progress offered reduced area and improved energy performance by removing the necessity of a DAC, and a mixer on the transceiver path, since the digital power amplifier (DPA) can perform both operations. However, the fact that most DPAs present a class-B like efficiency-output power profile implies that when the operational power level deviates from the peak power

level, the efficiency decreases proportionally to the square root of the power, as seen in Fig.1.2, being this efficiency defined by the proportion of AC power delivered to the load and the DC power drawn from the supply by the PA. This efficiency degradation presents a major drawback since most of the wireless standards employ orthogonal-frequency-division-multiplex (OFDM), which is known to have high PAPR (peak-to-average power ratio), meaning that most of the time the PA is working in power back-off (PBO), thus degrading the overall efficiency.
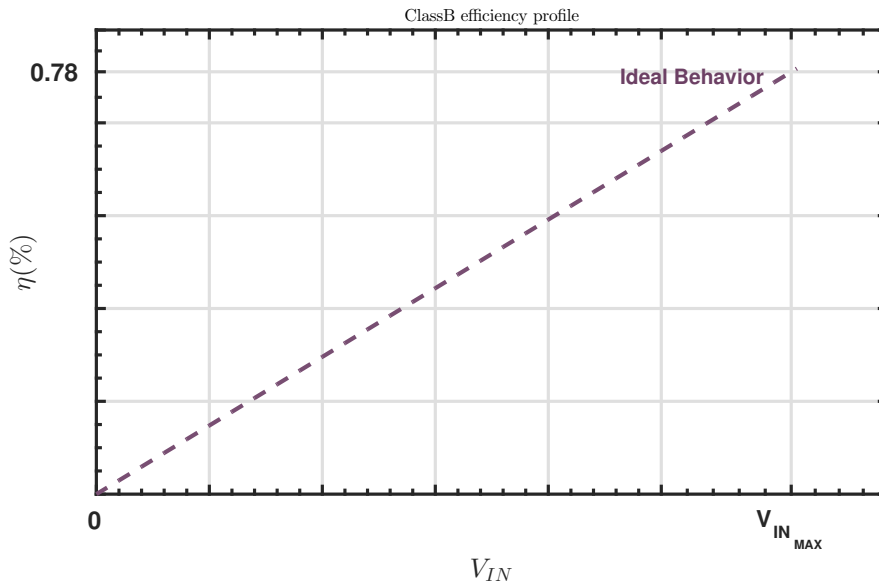
Figure 1.2: Efficiency Profile of a Class B PA

This efficiency degradation, motivated the development of techniques capable of improving the PBO efficiency such as: envelop tracking (ET), Doherty [3] , out phasing [4][5] and dynamic load modulation (DLM) [6] [7]. Dynamic load modulation is achieved by placing a dynamic matching network (DMNT) that is capable of dynamically change its input impedance between the PA and the antenna, as seen in Fig.1.3. The goal of the DMNT is to match the load value that maximizes the power delivered to the load (antenna).
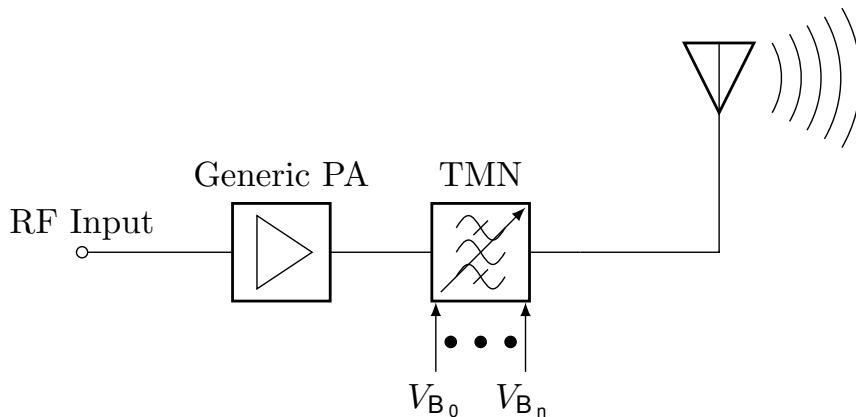
Figure 1.3: Simplified transmitter chain with tunable MNT

1.2 Motivation

The portability is not defined only by the size of the device, but also by its autonomy. The motivation for this dissertation resides on the latter given that the (PA) power consumption can make up to 50% of the total power consumed in the transceiver chain. Hence, the PA efficiency plays an important role on mobile devices effective autonomy. Due to the high complexity of the communication modulations employed in wireless technology e.g. (OFDM), the PAs are forced to sacrifice their own peak efficiency to be able to provide linear responses. On other hand, this efficiency degradation has a significant impact on the mobile device battery duration. This motivated the development of PBO efficiency improving techniques. From those techniques, Doherty [3] is the one that received the most interest from the industry, due to its simplicity. The basic Doherty setup its presented in Fig. 1.4. It has a main and a peak PA. The main PA is all ways on and is responsible for low signal levels, and the peak PA turns on for high power levels. Both PAs have the same input signal but with a 90° phase difference. When the main PA is close to saturation the peak PA turns-on and since a $\frac{\lambda}{4}$ transmission line is on the main PA path a 90° phase is added, thus on the R_L node, the signals are on phase, they add, and the voltage on R_L increases. Since there is a impedance inverter on the main PA path, what it actually sees is a impedance decrease, keeping the PA operating in high linear efficiency. This is known has active load modulation, and it is attained and controlled by the drive current of the peak PA. The need for two PAs and the necessity of transmission lines imply an area overhead and a narrow bandwidth.
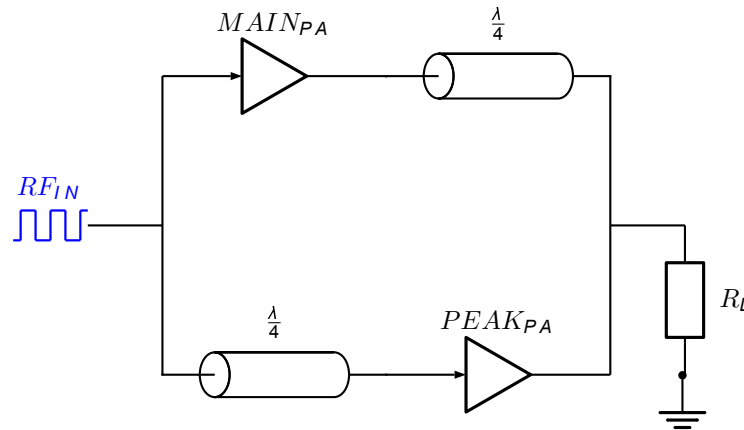
Figure 1.4: Doherty topology

Another of such techniques is the outphasing (LINC) [4]. This approach allows the PA to work in deep triode region, but still attain linear response. The overall system schematic is presented in Fig. 1.5. The out-phasing technique attains linear response by means of sums of out-of-phase waves.
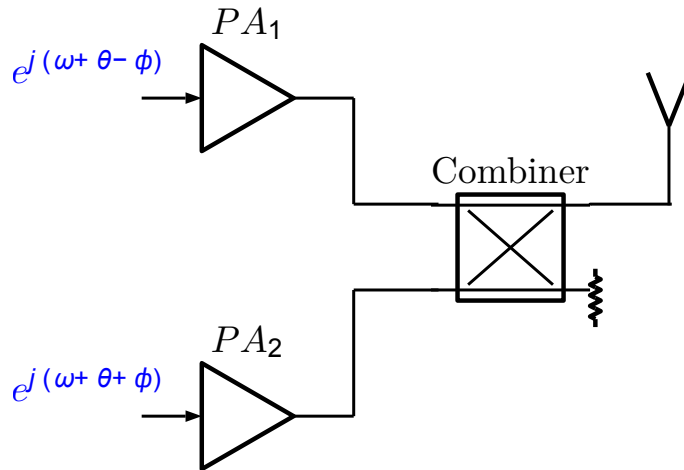
Figure 1.5: Outphasing scheme with isolater combiner.

Thus, the output wave magnitude can be modulated by the phase difference, as can be seen in the left of Fig. 1.6, while the phase information can be modulated by simply common phase off-set to both waves [8]. The Chireix topology differs from the original in the sense that the PAs are not isolated, this leads to load modulation between the two PAs. This imposes the need of adding a parallel inductance in order to compensate the reactive load component [5]. Despite being a very promising technique, it falls short when outputting small power signals, since for 0 voltage wave as shown in Fig. 1.6 on the right, it will still operate in a peak power, therefore a significant efficiency degradation is expected at low operating levels.
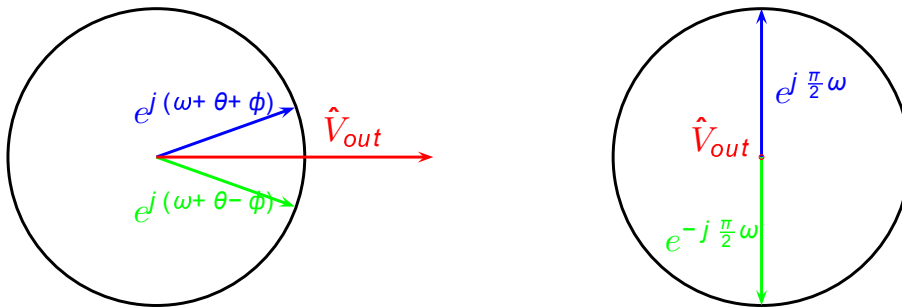
Figure 1.6: Outphasing Vectors

On the Envelope Tracking technique [9] when operating on a PBO level, the supply voltage decreases, pushing the PA operating point closer to triode, in order to improve the efficiency. To attain this, a supply modulator that is able to comprise the RF signal envelope bandwidth must be developed. Therefore, pushing the complexity from the PA itself into a supply modulator. Supply modulation is a similar technique, but instead of tracking the envelope, the supply modulates the signal amplitude, imposing the need for a supply capable of sustaining the whole signal bandwidth. As explained in the previous section, the DLM is a technique whose goal is to constantly match the impedance that maximizes the power transferred to the load. Continuous DLM is realized using tunable elements such as varactors and switched capacitors. Varactors allow a continuous control,

but fall short when it comes to linearity since the capacitance is not only controlled by the applied bias but is also affected by the RF swing. For this reason we chose to pursue a discrete dynamic load modulation (DDLM) approach, since it imposes well defined critical points, therefore allowing for reduced added nonlinearities. Thus, the correction of the gain and phase discontinuities between switching levels will preserve linearity, regardless of the load variations at the antenna [10]. Also, since it is framed on a digital scope, a DDLM approach allows a band base discrete control. This also implies a better area usage and a lower power consumption, making it ideal for low-power mobile devices that in the context of internet of things (IoT).

1.3   Problem Statement

Several approaches to DDMNT with variable inductors were developed in previous works. Several challenges arise when implementing these solutions, since they are transmission line dependent that imply an increased area usage, and a narrow bandwidth. Therefore, contrary to several other works [6][7], all the inductors will be set fixed, since tunable inductors are difficult to implement. Therefore, the only tunable element is going to be capacitors. The efficiency degradation on the PBO region presents a huge threat to the battery duration of mobile devices. Also, AM-PM distortion can make a communication link unreliable when it employs some kind of phase-using modulation. Furthermore, since the final solution is set to be used on a IC design, an effort to approximate the optimization process to the real scenario must be done. Since there are some fabrication variation, the solutions sensitivity must be somehow quantified and mitigated.

1.4   Goals

This dissertation will focus on the design of a matching network topology, using the Particle Swarm Optimization (PSO) method. The resulting matching network is set to be paired with a linear current digital power amplifier, and should have three distinct impedance values (10Ω, 20Ω and 30Ω), the same current phase in the antenna and an high intrinsic efficiency. Those three distinct impedance values where chosen so the peak efficiency of each is equally spread across the PBO region. The current phase should be similar between levels, to minimize the AM-PM distortion induced by the switching. The intrinsic efficiency should be high, to minimize the losses induced by the MNT. The results will be tested and validated on the Cadence Virtuoso simulator with BSIM models, in a first stage using ideal components, in a second stage using a second order model, and in a third stage using real models provided by the manufactures, e.g. S-Parameters, Spice Models. To improve the quality of the computed solutions, a PSO-ADS optimization loop will be defined, and with the final solution computed at this stage, an IC was designed and manufactured. For this reason, a de-embedding algorithm was developed in order to test and validate the IC. In summary, this dissertation objectives are:

- Development of a discrete DLM matching network.

- The dynamic matching network must support three different levels (10Ω, 20Ω and 30Ω)

- Must exhibit high intrinsic efficiency on the three different levels.

- Suitable frequency response to integrate with a linear DPA.

- Reduced AM-PM distortion and AM-AM distortion between different impedance levels.

- Improving the quality of the computed solutions, creating a optimization algorithm capable of optimize on top of a simulation environment.

- Development of a de-embedding algorithm, in order to obtain the true response of the IC.

1.5   Document Outline

This document is organized as follows.

Chapter 2 presents a theoretical foundation for the dynamic load technique. Also, previous work on discrete dynamic load modulation is analyzed and discussed. Each presented work has different tunable elements as foundations whose advantages and disadvantages are enumerated.

Chapter 3 establishes the work that is set to be developed in therms of DLM and optimization. First some PA metrics to motivate for the design goals. A brief introduction to particle swarm optimization algorithm (PSO). This was the algorithm used to attain the final solution. Some of the algorithm inherent trade-offs are explained and explored. Previous work proposing changes to the base algorithm are also subject of scrutiny. After this, it is described how the alignment between discrete dynamic matching network design and the PSO was made. All the changes made to the base algorithm are explained and justified until it finally presents the final algorithm.

Chapter 4 starts by explaining a new optimization paradigm that involves the optimization on top of a simulation environment.
followed by brief introduction about de-embedding. The whole proposed de-embedding process is described. Finally, explains how is possible to obtain the MNT target properties from the MNT s-parameters.

Chapter 5 presents the final conclusions, the dissertation outcomes and possible future research directions.

Chapter 2

A Review on CMOS Dynamic Load Modulation

There are several approaches to improve the PBO efficiency like envelop tracking [11], Doherty, outphasing and DLM. The ET is able to achieve good results, but moves the complexity from the PA to the supply modulator. Likewise, to achieve good efficiency results, the outphasing techniques requires heavy digital signal processing, imposing a significant power consumption, which impacts heavily the battery duration of low-power mobile devices. Also, despite receiving alot of attention from the industry due to its simplicity, Doherty suffers from narrow bandwidth, possible phase mismatch and are overhead, due to the necessity of at least two PAs and two transmission lines. Dynamic Load Modulation (DLM) is a technique that improves the PA efficiency when operating in a power back-of state. A Discrete-type DLM PA switches the load impedance from one value to another, without continuous control. Therefore it is more suitable for digitally-intensive transmitters. This chapter will provide an introduction to load modulation, followed by a state-of-the-art review on discrete DLM implementations.

2.1 Optimal Load Impedance

2.1.1 Theoretical Analysis

In class B PAs, the gate bias voltage is set equal to the threshold voltage (V_{TH}). Thus, if a sinusoid wave is applied to the gate of the PA, the current I_{DS} has the shape of a semi-rectified wave, has shown in fig. 2.1.
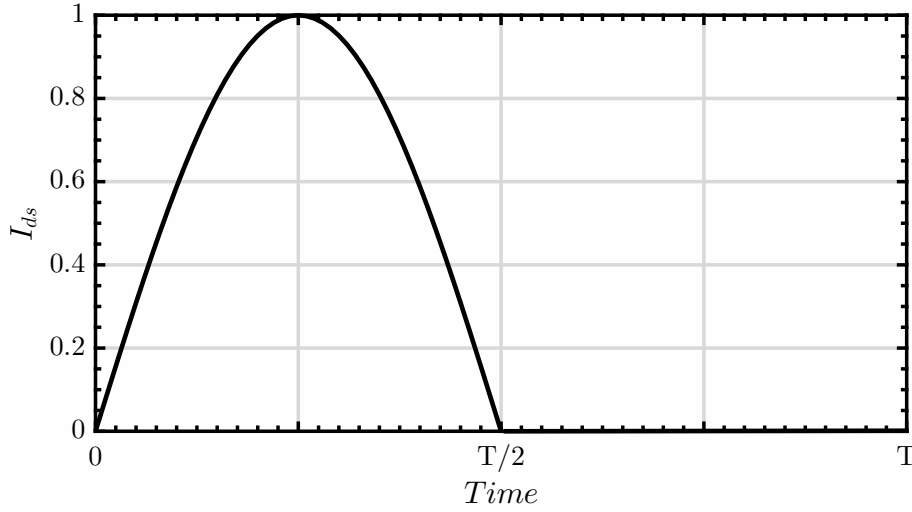
Figure 2.1: I_{DS} of Class B PA with sinusoidal V_{GS}

This in turn, induces harmonic content to the signal. Since the goal is the fundamental frequency, it can be assumed that,

$$Z_L = R_L + 0j\Omega \ : \ f = f_1$$
$$Z_L = 0\Omega \ : \ f \neq f_1$$

This implies that the voltage swing at the output of the PA has no harmonic content. Also, from now on lets assume that there's a linear dependency between V_{gs} and $_{Ids}$, when the NMOS works in saturation. Both these premises will ease the analysis done ahead. Assuming that the PA behaves like an ideal voltage controlled current source, the value of Z_L that allows the maximum allowed voltage swing can be calculated. Thus, since $Z_L = R_L$,

$$R_L = \frac{\Delta V_{AC}}{\Delta I_{AC}} = \frac{2 \cdot (V_{DD} - VDS_{SAT})}{I_p} = \frac{2 \cdot \Delta V_{MAX}}{I_p}, \tag{2.1}$$

where I_p is the maximum peak drain current and ΔV_{MAX} is the maximum output voltage swing which guarantees that the PA stays in saturation. The maximum output power can be defined as,

$$P_{out_{MAX}} = \frac{I_p \cdot \Delta V_{MAX}}{4} = \frac{R_L \cdot I_p^2}{8} \tag{2.2}$$

on the other side, the DC consumption can be quantified as,

$$P_{DC} = \frac{V_{DD} \cdot I_p}{\pi} \tag{2.3}$$

thus, the PA peak efficiency can be quantified as,

$$\eta_{peak} = \frac{P_{out_{MAX}}}{P_{DC}} = \frac{R_L \cdot I_p^2 \cdot \pi}{8 \cdot V_{DD} \cdot I_p} = \frac{\pi \cdot \Delta V_{MAX}}{4 \cdot V_{DD}} \tag{2.4}$$

From inspection of (2.4), one can state that the theoretical peak efficiency for a class B PA is $\frac{\pi}{4} = 0.78$, witch is obtained when $\Delta V_{MAX} = V_{DD}$.

Equation (2.4) only stands when the condition $V_{IN} = V_{GS_{MAX}} = V_{DD}$, but an analysis should be made for the scenario where $V_{IN} = V_{GS} < V_{DD}$, that is, when the PA is working in a power back-of state(PBO). Since it was previously stated that there is a linear relationship between I_{DS} and V_{GS}, it can be defined as follows,

$$I_{DS}(V_{GS}) = \frac{I_p \cdot V_{GS}}{V_{GS_{MAX}}} \tag{2.5}$$

where the fundamental current amplitude I_{f1} can be defined as,

$$I_{f1}(V_{GS}) = \frac{I_p \cdot V_{GS}}{2 \cdot V_{GS_{MAX}}} \tag{2.6}$$

and the dc component as,

$$I_{DC}(V_{GS}) = \frac{I_p \cdot V_{GS}}{\pi \cdot V_{GS_{MAX}}} \tag{2.7}$$

Now, the output voltage's dependency on V_{GS} is defined as,

$$\Delta V(V_{GS}) = \frac{I_p \cdot V_{GS} \cdot R_L}{2 \cdot V_{GS_{MAX}}} \tag{2.8}$$

From (2.4) and (2.8), we derive that

$$\eta(V_{GS}) = \frac{\pi \cdot \Delta V_{MAX}(V_{GS})}{4 \cdot V_{DD}} = \frac{\pi \cdot I_p \cdot V_{GS} \times R_L}{8 \cdot V_{DD} \cdot V_{GS_{MAX}}} \tag{2.9}$$

If $V_{GS} = V_{GS_{MAX}}$, the peak efficiency is obtained once again, but when $VGS < V_{GS_{MAX}}$ (power back-off), the efficiency is degraded fig. 1.2. This because, in distinction to V_{GS}, its assumed that every parameter in (2.9) is constant. If one assumes that its possible to adapt the R_L value to compensate the reduction of V_{GS} with respect to $V_{GS_{MAX}}$, it should be possible to improve the efficiency in the PBO state. From (2.1) and (2.6), the following relationship can be defined,

$$R'_L(V_{GS}) = \frac{2 \cdot \Delta V_{MAX}}{I_{f1}(V_{GS})}) = \frac{(V_{DD} - V_{DS_{SAT}}) \cdot 2 \cdot V_{GS_{MAX}}}{I_p \cdot V_{GS}} \tag{2.10}$$

the equation can be further simplified with (2.1), leading to

$$R'_L(V_{GS}) = RL \cdot \frac{V_{GS_{MAX}}}{V_{GS}} \tag{2.11}$$

where R_L is the optimum value for the particular case $V_{GS} = V_{GS_{MAX}}$. Substituting $R'_L(V_{GS})$ for R_L in (2.9),

$$\eta'(V_{GS}) = \frac{\pi \cdot I_p \cdot V_{GS} \cdot R'_L(V_{GS})}{8 \cdot V_{DD} \cdot V_{GS_{MAX}}} = \frac{\pi \cdot I_p \cdot R_L}{8 \cdot V_{DD}} = \frac{\pi \cdot \Delta V_{MAX}}{4 \cdot V_{DD}} \tag{2.12}$$

Thus, for this values of R'_L, it is possible to obtain the class B peak efficiency for all the PBO levels. Dynamic load modulation is a technique whose aim is a practical implementation of the relation in (2.11) .

2.1.2   From a Load-Line Theory Perspective

In Fig.2.2 the input peak power with peak efficiency load line is presented. As can be seen the PA is operating at the maximum voltage swing that allows him to stay in saturation. When the input power decreases, the PA starts operating in a PBO state fig. 2.3, decreasing the voltage and current swing, therefore decreasing the efficiency. Since the PA operates in saturation, the PA behaves like an current source, meaning that increasing the load will have no impact on the current, but the voltage swing will increase, and so does the output power and efficiency.
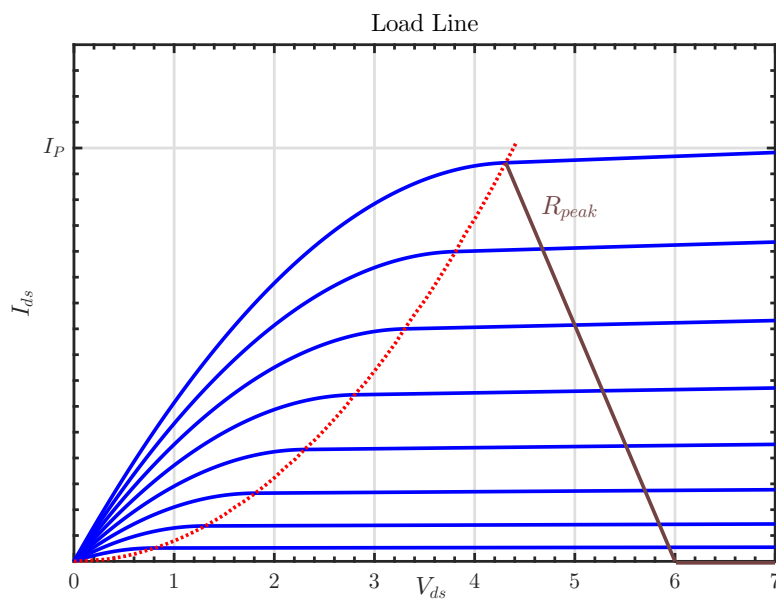
Figure 2.2: Load Line - Peak efficiency
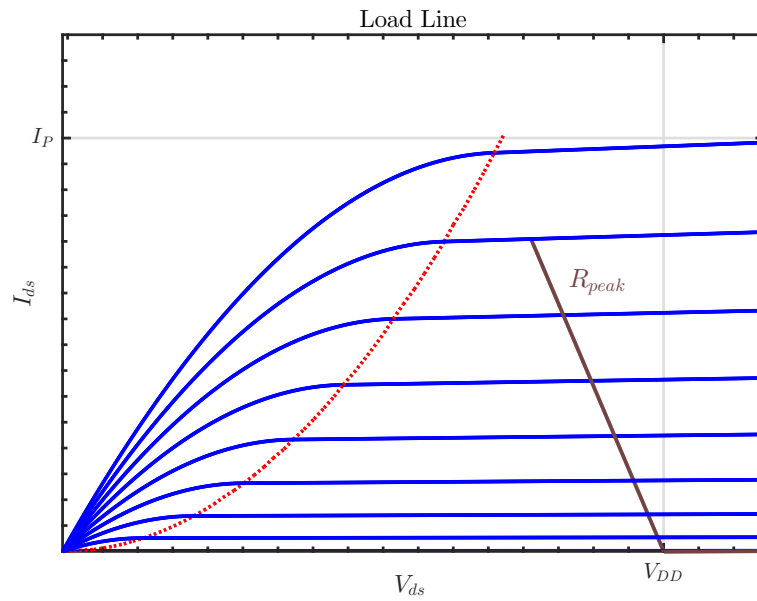
Figure 2.3: Load line PBO - No optimum load load

From Fig. 2.3 to Fig. 2.4, the load impedance was increased, and it can be seen that in practical terms, it represents a decrease, of the load line slope. Furthermore, the I_{ds} barely suffers variation, but since V_{ds} increases, an increase in efficiency is also attained. Basically the dynamic load modulation technique can be interpreted as a slope variation that maximizes the voltage swing and prevents the DPA from entering the triode region.
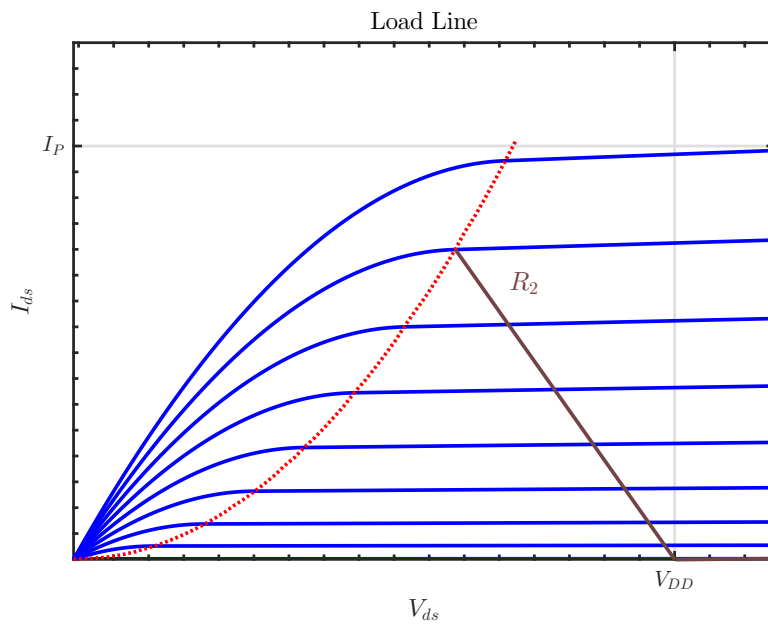
Figure 2.4: Load line PBO - Optimum load

I_{ds} / V_{ds} curve
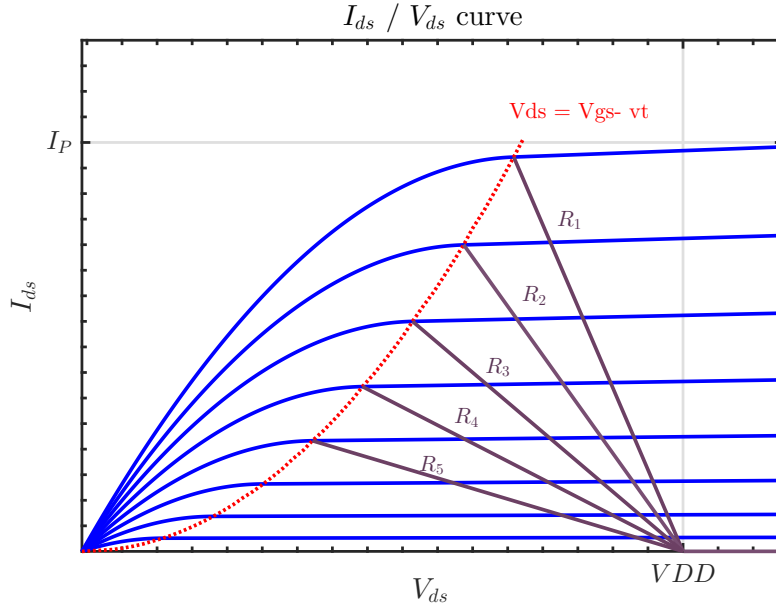
Figure 2.5: 5 level DDLM system

In fig. 2.5 a representation of a 5 levels discrete dynamic load modulation system. In this figure is possible to note that, it can not switch to a different impedance level right after operating PBO, otherwise would push the PA into triode. Nevertheless, it shows flexibility to be paired with another PBO efficiency improving technique, who would be responsible for a small-scale optimization inside each level.

2.2   Previous Work - DDLM

In the following sub-sections a review of previous work is done, and the justifications for not using them as basis for the work developed on this dissertation are enumerated for each one.

2.2.1   Pulsed Dynamic Load Modulation

A pulsed dynamic load modulation (PDLM) technique was proposed in It switches between two impedance levels using a PWM control signal. Moreover, it defines three operating states,

- *High Power State*(HP_{state}) $\rightarrow$ $P_{out} \geq P_{max}$

- *Low Power State*(LP_{state}) $\rightarrow$ $P_{out} \leq PBO$

- *PWM Power State*(PWM_{state}) $\rightarrow$ $P_{max} > P_{out} > PBO$
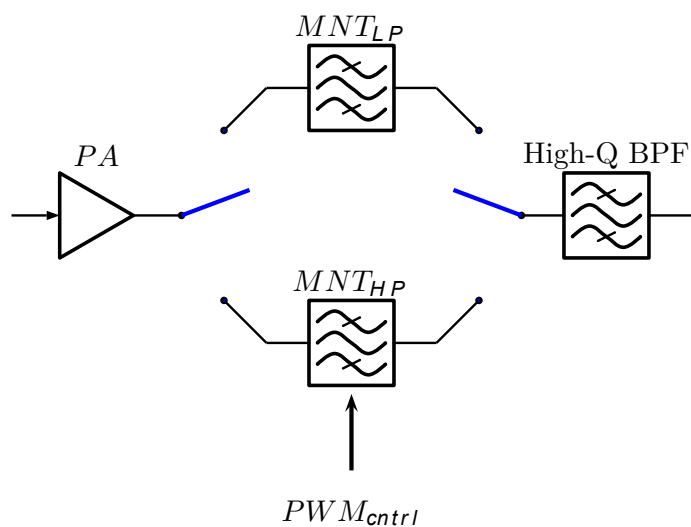
Figure 2.6: High power MNT / Low power MNT scheme.

When in HP_{state}, Z_{in} is fixed in a value defined as Zh_{in}. Likewise, when operating in LP_{state}, the Z_{in} is fixed in $Zl_{in} = m \times Zh_{in}$. However, when operation is carried on the PWM_{state} the Z_{in} value will constantly shift between Zh_{in} and Zl_{in}. This switching is controlled by a PWM signal whose duty cycle(D_{cycle}) will be defined in a way that

$$Current_{state} = PWM_{state}$$

when,

$$Current_{state} \rightarrow HP_{state}.$$

Then,

$$D_{cycle} \rightarrow 1.$$

Likewise when,

$$Current_{state} \rightarrow LP_{state},$$

then

$$D_{cycle} \rightarrow 0.$$

Thus, a continuous control is attained with discrete impedance levels. A Power-Added Efficiency (PAE) higher than 44% is attained over a 6dB PBO range. Still, due to the constant switching,high Q bandpass filter is needed to filter out the noise as well as digital pre-distortion on both the phase and magnitude paths.

2.2.2   Tunable $\frac{\lambda}{4}$ Transmission Line

In [12], the DML was implemented using $\lambda/4$ transmission lines. When a external load R_L is connected to a quarter-wave transformer with characteristic impedance Z_T, like presented in fig. 2.7, the equivalent impedance is given by,

$$Z_{eq} = \frac{Z_T^2}{R_L} \qquad (2.13)$$

Since R_L is fixed, the transmission line characteristic, Z_T, must be variable in order to obtain the variable Z_{eq}. To attain this, the author proposed a parallel combination of multiple transmission lines and RF switches like in fig. 2.8. The RF switches are responsible for the connection of each parallel transmission line. Therefore, the characteristic impedance ranges discretely as follows,

$$Z_{eq} = \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + ... + \frac{1}{Z_n}} \qquad (2.14)$$

This technique showed an overall efficiency improvement of 5.1% over all the PBO levels.
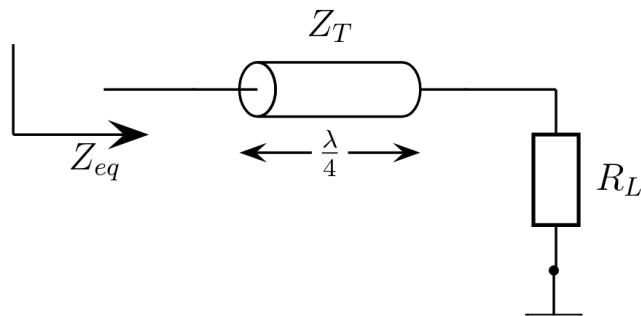
Figure 2.7: Basic $\frac{\lambda}{4}$ Scheme
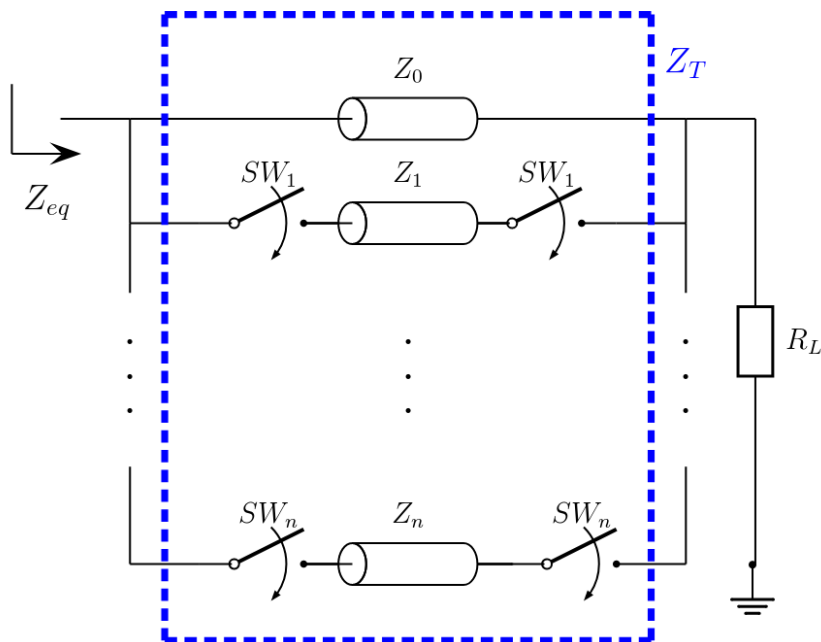
Figure 2.8: Variable Z_T scheme

2.2.3   T-Network with Constant Current Phase Difference

In [6], a tunable matching network whose phase difference between input and output port is constant was proposed. To achieve this the author proposed the circuit in the fig. 2.9 where,

$$Z_{eq} = \frac{\omega^2 \cdot L_P \cdot C_L}{Z_0 \cdot \frac{C_S}{L_P} + \frac{1 - \omega^2 \cdot L_P \cdot C_S}{j\omega \cdot L_P}} + \frac{1 - \omega^2 \cdot L_P \cdot C_S}{j\omega \cdot C_S} \tag{2.15}$$

and,

$$\Delta\phi = \angle(\frac{i_{in}}{i_{out}}) = tan^{-1}(\frac{Z_0}{\frac{1}{\omega \cdot C_S} + \omega \cdot L_P}) \tag{2.16}$$

If the circuit is set to work at

$$\omega_0 = \frac{1}{\sqrt{C_s \cdot L_P}} \tag{2.17}$$

Substituting ω from (2.15) and (2.16) by ω_0 defined in (2.17),

$$Z_{eq} = \frac{L_P}{R_L \cdot C_S} \tag{2.18}$$

and that,

$$\Delta\phi = \frac{\pi}{2} \tag{2.19}$$

Therefore, if the product of L_P and C_S stays constant, the input impedance can be varied without changing the phase difference between the input and the output signals. To implement the tunable inductor, the author proposes the configurations in Fig. 2.10. The drain efficiency has an overall improvement of 5% when compared to a fixed MNT. Notwithstanding, since the technique has a strong dependence on the relation between the frequency and both L_P and C_S (2.17), it has an extremely narrow-band operating region.
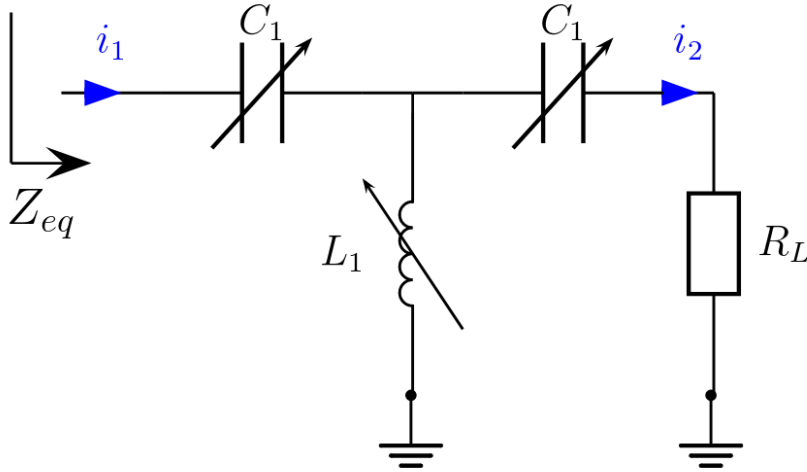
Figure 2.9: T-Matching Network

2.2.4   L-Network with Tunable L and C

In [7] the author proposes a Class-E PA for RF Polar transmitters. This PA embodies a L-type DMNT, whose L and C are both variable Fig. 2.11. To attain a variable inductor the author proposes the scheme presented in Fig. 2.10 (a). Where the equivalent inductance can be obtained as follows,

$$X_{eq} = \frac{1}{j\omega \cdot C_2} + j\omega \cdot L_1 = j\frac{(\omega^2 \cdot L_1 \cdot L_2 - 1)}{\omega \cdot C_2} \tag{2.20}$$
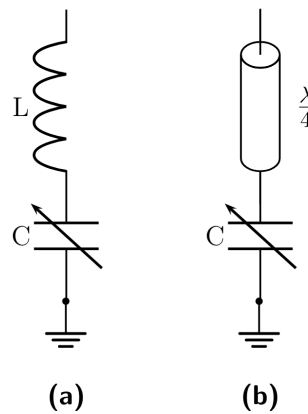
Figure 2.10: Fixed inductor (a). $\frac{\lambda}{4}$ Transmission line (b)
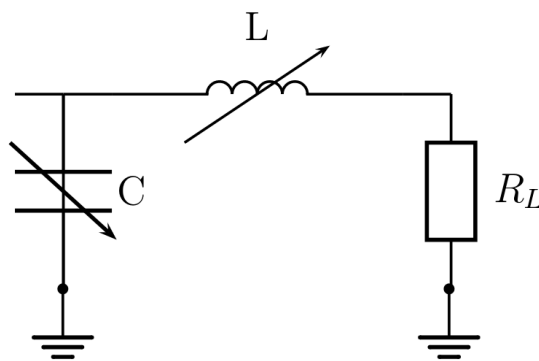
Figure 2.11: L-Network with tunable inductor.

A 48% peak efficiency was attained for a peak output power of 17 dBm and a strong rejection of the harmonic contents by the MNT.

2.2.5 Conclusions

There are several approaches to implement a DDLM, all of them implying different trade-offs. The common factor is that by definition, they all depend on a discrete tunable element. From the previous works, one can state that solutions with variable inductors are extremely narrow band, but in turn they ease the optimization process for reduced AM-PM.

Chapter 3

Proposed Discrete Dynamic load Modulation Architecture

3.1 Discrete dynamic load modulation

Discrete dynamic load modulation is a spectrum of dynamic load modulation technique, whose fundamental property lies on its discrete control. Indeed when to integrate in CMOS transmitters, discrete control has some fundamental advantages, compared with its continuous counter part, as stated in the previous chapter.

3.1.1 AM − AM and AM − PM Distortions

3.1.1.1 AM-AM Distortion

AM − AM distortion refers to the amplitude distortion of any amplifier that is driven into a nonlinear condition [13]. When applying a single tone input signal, this distortion can be observed by the amount of compression on the $V_{in} − V_{out}$ curve.
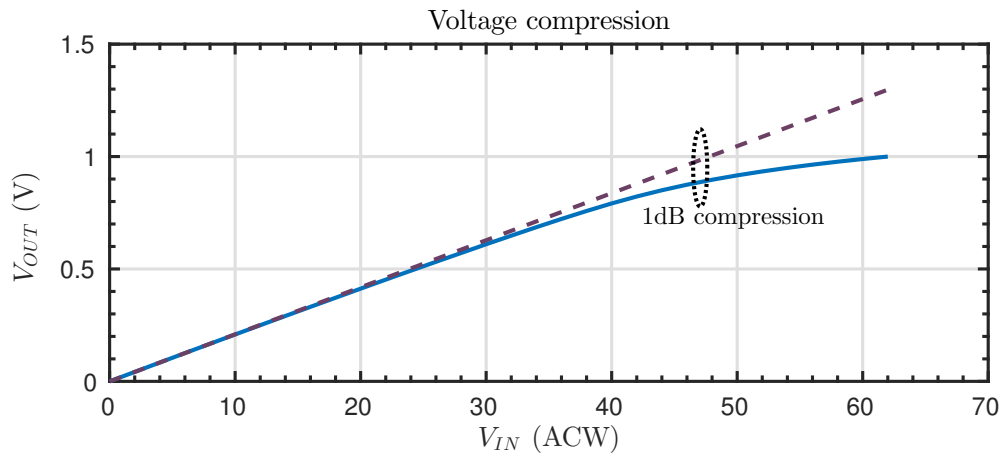
Figure 3.1: Ideal vs Real AM-AM profile

3.1.1.2 AM-PM Distortion

AM – PM distortion refers to the phase difference between the input and output signal as function of the input signal level [13], which should ideally be zero. When transmitting phase modulated signals, correcting the AM – PM distortion is crucial for standard compliance.

3.1.2 Tunable Element - Switched Capacitor Array

The chosen tunable component was the switched capacitor, as it allows a more efficient area usage, when compared with transmission line dependent solutions, while resorting only to digital control.
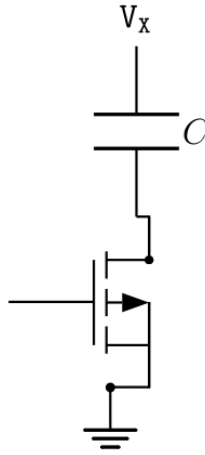
Figure 3.2: Switched capacitor

When the switch is closed (ON), the impedance seen from V_x is

$$Z_x = X_c + R_{on} \tag{3.1}$$

where X_C is the impedance from the capacitance, and R_{on} is the on resistance of the transistor. When the transistor is open (OFF), the impedance seen from V_x is.

$$Z_x = X_c + X_{c_{parasitic}} \tag{3.2}$$

$$C \gg C_{parasitic} \Rightarrow Z_x \simeq X_{c_{parasitic}} \tag{3.3}$$

Since there is no dc current going through the capacitor, there will be no dc current going through the transistor either. This implies that there is no dc drain voltage and that the transistor is

(a) Switched Cap - ON state   (b) Switched Cap - Off state
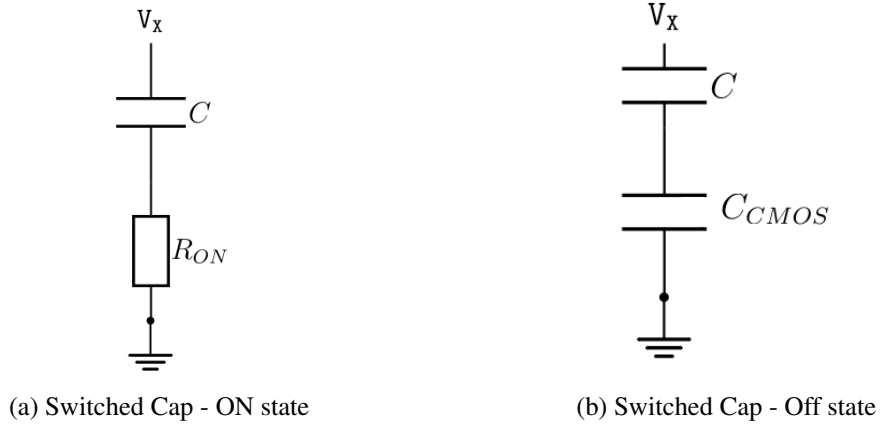
Figure 3.3: Switched Cap - Both states of operation

operating in a deep triode region. This conclusion allows us to state that,

$$R_{on} = \frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_t)} \tag{3.4}$$

where μ is the mobility, C_{ox} is the gate oxide capacitance per area, W and L are the width and length of the transistor, and V_{GS} and V_t are the gate-to-source and threshold voltage. Therefore, the On quality factor of the switched capacitor can be defined as,

$$Q_{ON} = \frac{1}{2 \times \pi \times F \times C \times R_{on}} \tag{3.5}$$

When the transistor enters saturation the relation (3.4) does not stand, therefore, one should quantify what is the margin that is being dealt with. That being said, the transistor stays in triode when,

$$v_{DS} < V_{GS} - V_t \tag{3.6}$$

and,

$$v_{DS} = \frac{R_{on}}{X_c + R_{on}} \times V_x = \frac{R_{on}}{\frac{1}{2 \times \pi \times F \times C} + R_{on}} \times V_x = \frac{1}{\frac{1}{2 \times \pi \times F \times C \times R_{on}} + 1} \times V_x \tag{3.7}$$

from (3.5) it is possible to formulate the relationship between Q_{ON} and V_{DS}

$$v_{ds} = \frac{1}{Q_{ON} + 1} \times V_x \tag{3.8}$$

then from (3.6) and (3.8), its possible to state that if the condition

$$Q_{ON} > \frac{V_x}{V_{GS} - V_t} - 1 \tag{3.9}$$

is satisfied, the transistor stays in the triode region. Assuming $V_{GS} = 3.3V$, $V_t = 0.65V$ and $V_x = 3.3V$, $Q_{ON} > 0.2692$ to ensure triode, which is a very comfortable result, since we aim to attain $Q_{ON} \gg 1$. In Fig. 3.4 its possible to see a multi-level switched capacitor. They are in parallel, so the resulting capacitance seen from V_X, is the sum of all the individual equivalent capacitances. Inspecting the expressions (3.1) and (3.2) its possible to understand that, to attain a good off-state a small capacitor needs a small width transistor, since the parasitic transistor value increases with transistor width. On other hand, from (3.4) it is possible to see that the equivalent on resistance of the transistor increases, as the transistor width decreases, this in turn motivates the necessity of transistors with high width for large capacitor values. But, when presented with the necessity of implementing a switched capacitor whose different capacitance interval show significant variance, for example from 1pF to 16pF step 1pF, one must choose to sacrifice the On quality factor (Q_{ON}) or the smallest possible capacitance values. When these values are not flexibile, one must resort to sacrifice the Q_{ON}, thus decreasing the system overall efficiency.
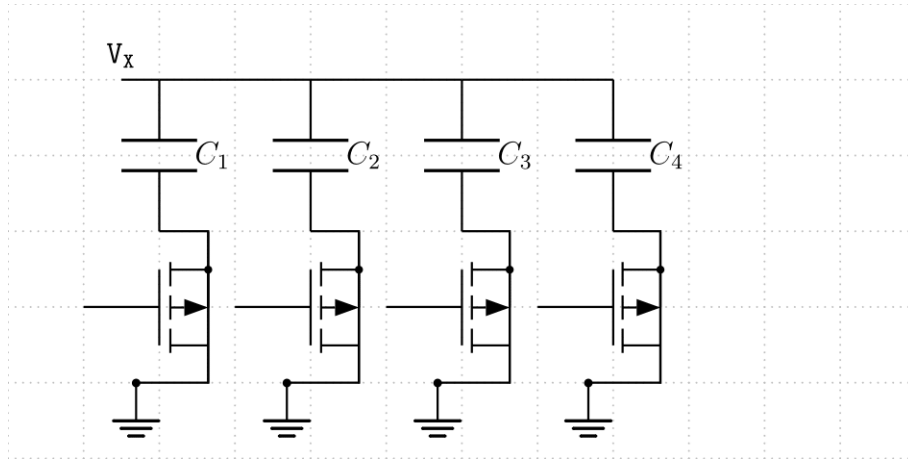
Figure 3.4: Multi-level switched capacitor

3.1.3 Design Goals

The objective of the DLM is to increase de PBO efficiency, while satisfying some standard. Most of the times, this also implies that some linear performance must also be attained. Therefore, it is necessary to define the peak output power, and divide the PBO zone in order to define the impedance values that the DDMNT must attain. In total, three different impedance levels will be defined. The AM-AM and AM-PM distortion must be minimized by preventing the PA from entering in the ohmic region and minimizing the current phase difference at the antenna between the three different impedance levels. Finally, if the DDMNT itself exhibits low power efficiency this will have implications on the system overall efficiency, so the DDMNT must be as efficient as possible, making a total of three objectives per impedance level. This in turn, motivates the necessity of a optimization algorithm capable of computing a solution that comprises all these objectives at the operational frequency 860MHz.

3.1.4 Preliminary DDMNT

Several matching network topology were experimented with the optimization algorithm described in the following section, and the double pi was the one exhibiting better convergence.
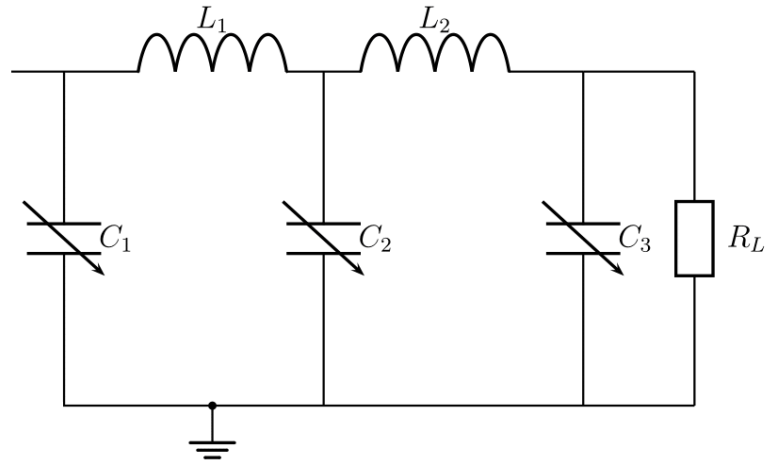
Figure 3.5: Proposed DDMNT topology

3.1.4.1 DPA

This proposed DDMNT is set to be paired with a discrete class B PA, as can bee seen in Fig. 3.6
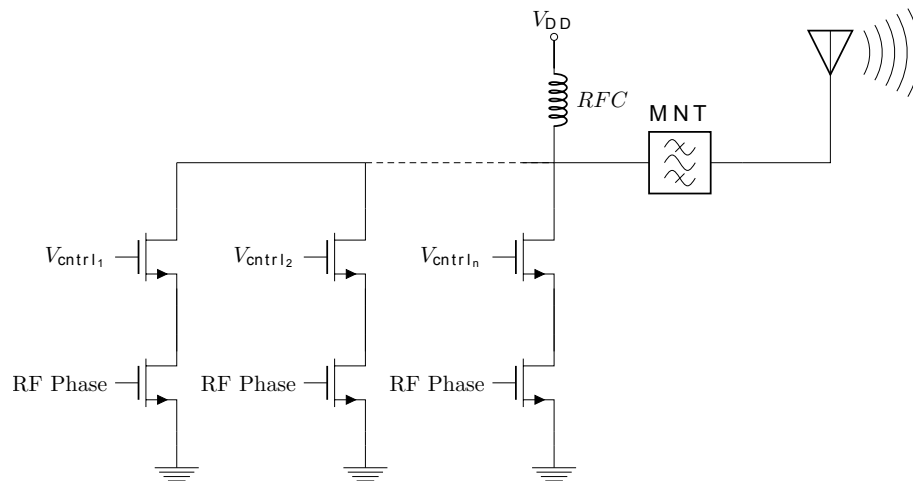
Figure 3.6: Discrete class B PA paired with DDMNT.

3.1.5 Problem – Drain Voltage Harmonic Content

3.1.5.1 Second Harmonic – Harmonic Trap

The DMNT is set to be paired with a digital class B PA whose discrete input levels are coded in amplitude code words (ACW). For the scope of this dissertation the peak is set to be ACW = 62.

When the computed solutions were tested with the DPA, a 1dB deviation from the ideal efficiency profile could be noted, still far from the target output peak power Fig. 3.7. By inspecting the drain voltage in the time and frequency domain Fig. 3.8, it is possible to note that there is a high harmonic content on the drain voltage that is pushing the DPA into the triode region, and therefore imposing undesirable efficiency degradation. Also from inspection it is possible to see that the the most troublesome is the 2nd harmonic, therefore the first improvement step is to add a harmonic trap at the 2nd harmonic frequency.

The results can be seen in Fig. 3.9 and Fig. 3.10 where a preeminent improvement can be noted on the efficiency deviation at the operating frequency.
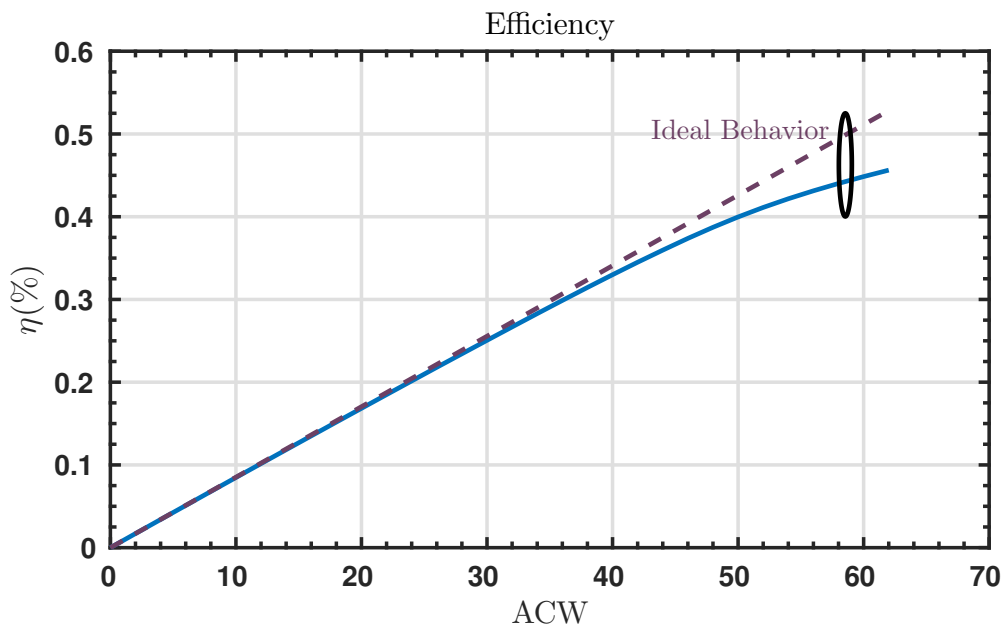
Figure 3.7: Efficiency deviation - no HT
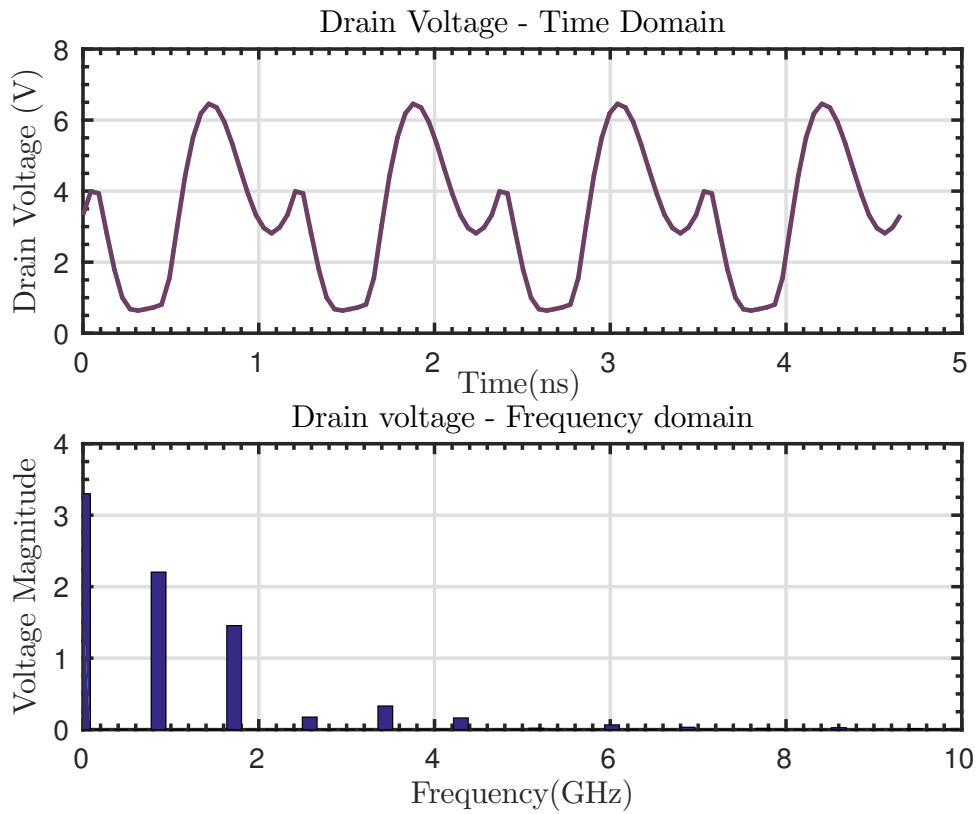
Figure 3.8: Time and frequency domain - no HT
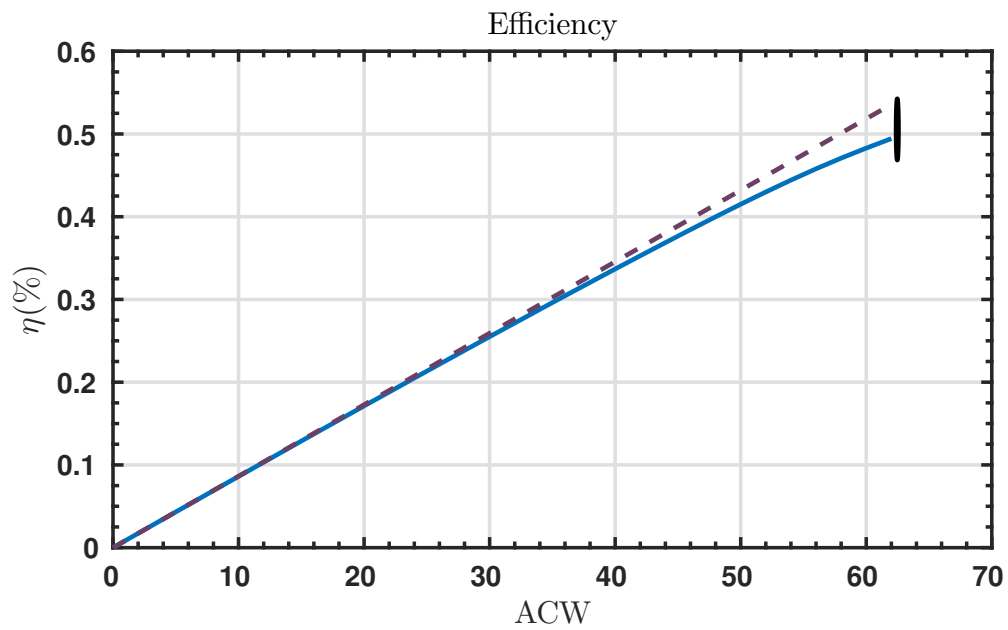
Figure 3.9: Efficiency deviation - 2nd Harmonic HT
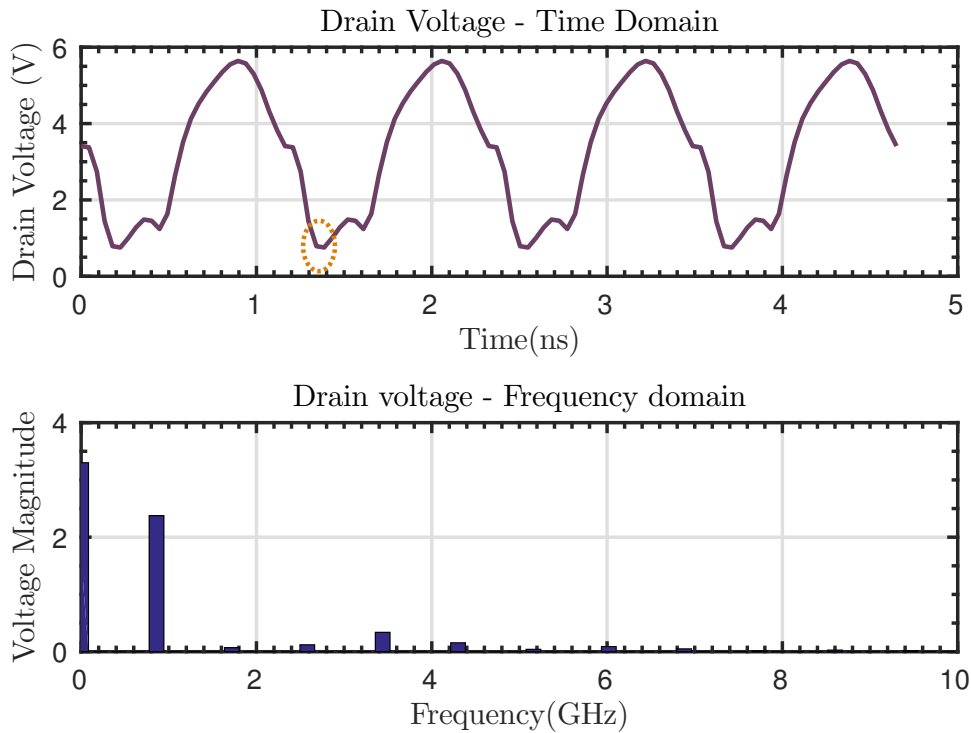
Figure 3.10: Time and frequency domain - 2nd Harmonic HT

3.1.5.2 Fourth Harmonic – Harmonic Trap

Even though the addition of the second ht showed evident improvement, there still is a small deviation. Once again, inspecting the time and frequency domain of the drain voltage for ACW=62 (Fig. 3.10), it can be noted that, although the 4th harmonic magnitude is small when compared to the fundamental, it just happens that it adds itself to the fundamental in the minimum fig. 3.10, making a small but crucial contribution that pushes the DPA momentarily into triode region, therefore an additional harmonic trap centered at the 4th harmonic frequency was experimented. In figures Fig. 3.11 and Fig. 3.12 the final results can be seen, where at peak power only a 0.23dB deviation is attained.
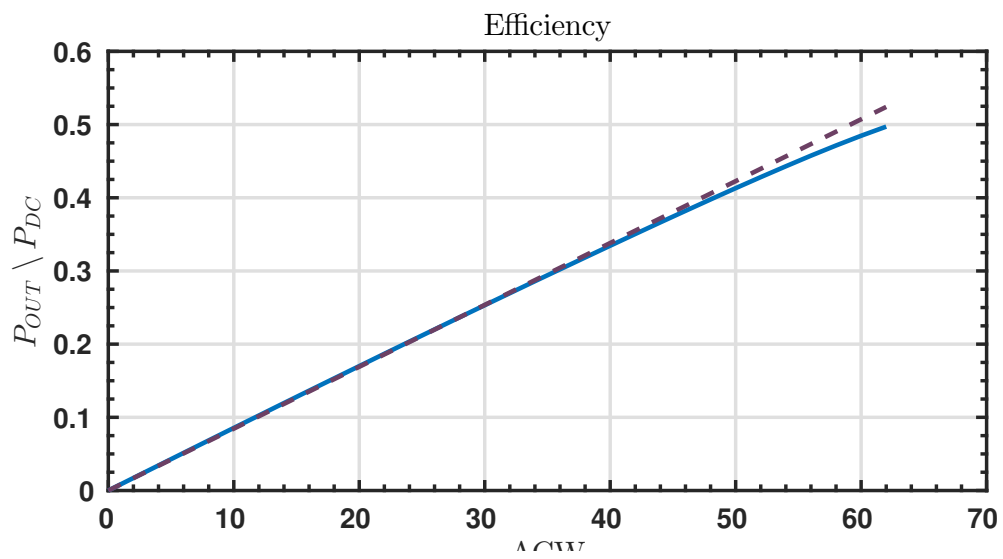
Figure 3.11: Efficiency deviation - 2nd and 4th HT
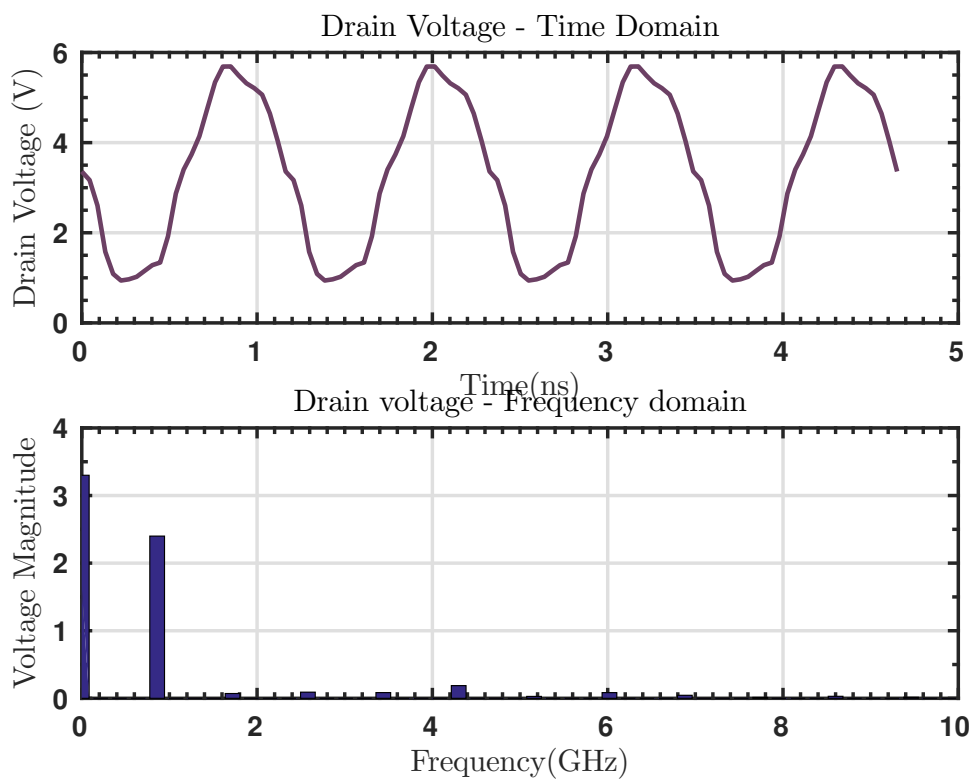
Figure 3.12: Time and Frequency domain -2nd and 4th HT

Thus, the final DDMNT topology is obtained,
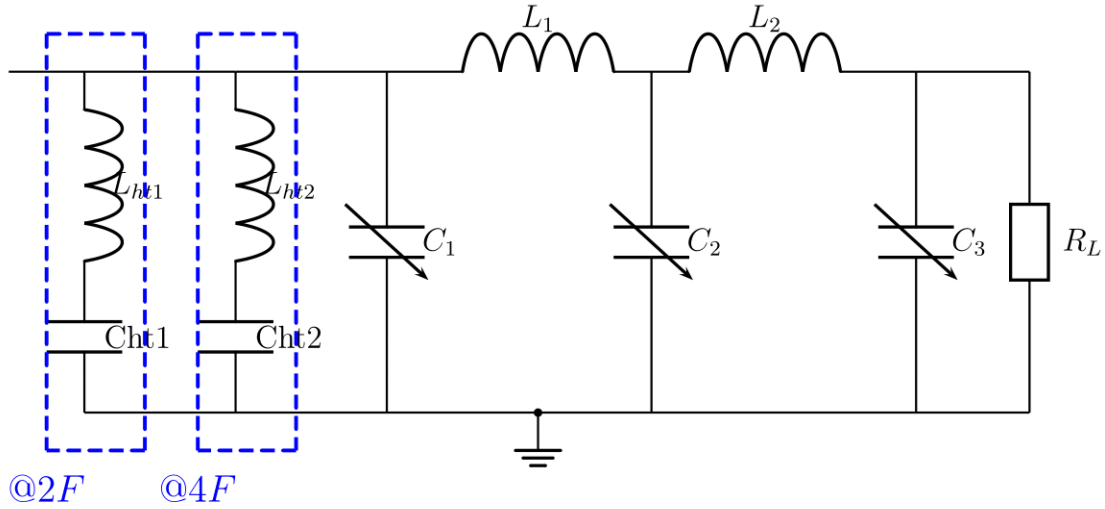
Figure 3.13: Final DMNT topology

3.2   Particle Swarm Optimization - Introduction

Similarly to evolutionary algorithms, PSO exploits a population, called a swarm, of potential solutions, called particles, which are modified stochastically at each iteration of the algorithm [14]. However, both these approaches differ in the sense that, the underlying model of the evolutionary algorithms is competitive and the PSO is cooperative. Instead of having particles competing to see who are the most fit to pass to the next generation, in PSO, the particles share experiences in an attempt to improve the whole swarm. In fact, this improves the exploration of promising regions. To do this each particle is aware of the best position it has ever been to (pbest) and the best pbest in the entire swarm (gbest). Moreover, when dealing with continuous space problems, genetic algorithms rely on a discretization of the problem space, where the resolution is a parameter to tune with relevant trade-offs. On other hand, PSO is inherently fitted to optimize continuous space problems with lower computational cost [15].

3.2.1   PSO Classic Algorithm

More formally in a n-dimensional search space $S \rightarrow \mathbb{R}$, the single objective PSO algorithm can be described as follows,

$$FullSwarm = \{X_0, X_1, ..., X_N\}$$

where FullSwarm is formed by N particles, and the i-th particle is,

$$X_i = \{x_{i_0}, x_{i_1}, ..., x_{i_n}\} \in S$$

Its personal best is

$$Pbest_i = \{x_{i_0}, x_{i_1}, ..., x_{i_n}\} \in S$$

which represents the best position ever visited by the i-th particle, while its velocity vector is

$$V_i = \{v_{i,0}, v_{i,1}, ..., v_{i,n}\}$$

All of these parameters are randomly initiated in the search space to ensure diversification. As one can state, there are little memory requirements, witch by itself is one of the attributes that makes the algorithm so attractive. As described in the original algorithm of [16], assuming a star topology implies that there can be only one global best at any given time. So the global variable

$$Gbest = \{x_0, x_1, ..., x_n\}$$

represents the global best position of any particle at any moment in time. All the particles are evaluated using the cost function f,

$$Score_i = f(X_i)$$

Considering that f is the function to minimize, the update of pbests is done by simply,

$$if(f(Pbest_i) > f(X_i))$$
$$Pbest_i = X_i$$

as for gbest,

$$if(f(Gbest) > f(X_i))$$
$$Gbest = X_i$$

Again we should note that Gbest does not have index i, because it is a global variable whose scope is the whole swarm.The particles movements are modelled according to the following equations, where t denotes the iteration counter. First, we update the velocity (3.10) of the particle and then the position (3.11)

$$V_i(t+1) = \omega \times V_i(t) + c_1 \times r_1 \times (Pbest_i(t) - X_i(t)) + c_2 \times r_2 \times (Gbest(t) - X_i(t)) \quad (3.10)$$

$$X_i(t+1) = V_i(t+1) + X_i(t) \quad (3.11)$$

where r_1 and r_2 are realizations of two random independent variables modeled by a uniform distribution of range $[0,1]$.

3.2.1.1 Cognitive and Social Parameters

The c_1 and c_2 are two positive constants, called cognitive and social parameter, respectively. These names reflect on their function, as one can state by inspection of (3.10), c_1 will determine the importance that each particle will give to his own past experience, hence cognitive parameter. On other hand the c_2 will determine the importance given to the best position found by the entire

swarm, hence the name social parameter. How the tweaking of this parameters impacts the velocity update, can be seen in Fig. 3.14. Furthermore, [16] stated that $c_1 + c_2 = 4$ is a good starting point for the definition of these constants.
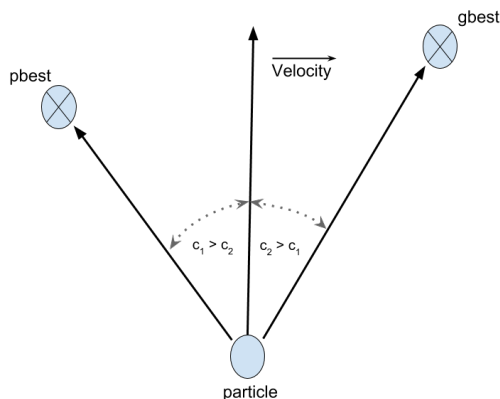
Figure 3.14: Cognitive vs social behavior

3.2.1.2   Exploration and Exploitation

The ω variable in (3.10) is called inertia weight, and it quantifies the importance of $V_i(t-1)$ in $V_i(t)$, thus modeling the particles inertia. When dealing with non-linear optimization problems, one of the biggest concerns is local minima. The optimization algorithm must ensure that it simultaneously covers an extensive area of the problem space (exploration), and also tries to refine the solution in promising regions (exploitation). One of the most common ways to deal with this trade-off is to implement a simulated annealing like approach, where the algorithm starts exploring in the early stages, and, as the iterations increase, it shifts to a more exploitation like behavior [17, 18]. Since larger values of ω promote exploration, and lower ones promote exploitation, one can implement the early exploration and late exploitation technique by starting with large values of ω and decreasing it as time goes on, instead of using a fixed ω. In [19] it was proposed the use of 0.1 as initial value of ω and gradually declining it to 0.0.

3.2.2   Multi-Objective PSO

In the previous section, it was made clear how PSO would behave when trying to optimize the cost function f, i.e., a single objective PSO. To solve the problem presented in this dissertation, a multi-objective approach must be accomplished. Therefore, several changes must be imposed to the classic PSO algorithm.

3.2.2.1 Lexicographic Ordering Approach

These approaches require the definition of priorities for all the functions to optimize $f_1, f_2 \ldots f_k$. Then, the minimization is performed from the most important to the least. Therefore, in order to quantify the best particles, we start comparing the function of highest priority (lower index). If it is a draw we compare the particles using the next higher priority function, and so on, until there is no draw or there are no more functions. If there is a draw in the last, we can save both particles as non-dominated solutions, or simply ignore one of them. The lexicographic ordering algorithm can then be defined as follows

$for(k = 0,$ **until** *number of functions do optimize* **or** *not draw*)
{
    $if(f_k(particle) == f_k(Gbest))$
        Draw
    $else \; if(f_k(particle) < f_k(Gbest))$
        $Gbest = particle$
        Not Draw
    $else$
        Not Draw
}

It can also be stated that the algorithm performance is tightly connected to how the priorities are set. In [20] it was proposed that the priorities change dynamically during optimization. This scheme aims to improve the flexibility and diversity of the fixed priorities algorithm. The proposed dynamic lexicographic ordering works as follows: first, it is assigned a probability to each function using the equation

$$p_q = \frac{1}{M} e^{-\frac{\sigma}{N} q}, \tag{3.12}$$

where N is the number of objective functions, q is the priority set to each of these functions, σ is exponential shaping constant, and M is a normalization constant, computed by

$$M = \sum_q e^{-\frac{\sigma}{N} q}, \tag{3.13}$$

therefore making

$$\sum_q p_q = 1 \tag{3.14}$$

These probabilities are used do create a number of intervals in a segment. Spanning the interval [0,1] and then applying the Roulette Wheel Selection mechanism. Figure 3.2 shows the results for $N = 5$ and $\sigma = 2.5$.
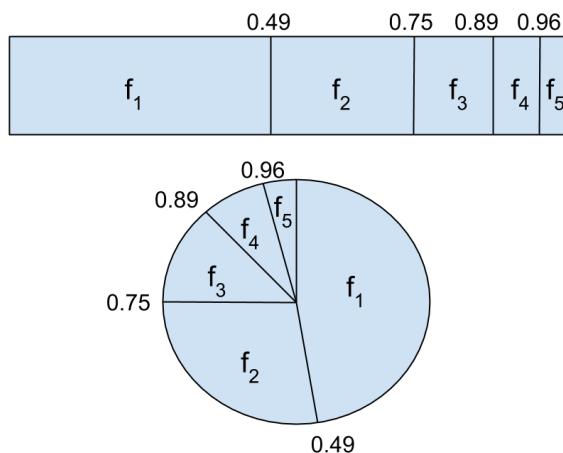
Figure 3.15: Segment top, Roulette bottom

A random value between [0,1] is generated, and the objective function whose sub-segment spans the random value is selected. The selected objective function is removed from the spanning interval, which is normalize to [0,1] again. The process repeats until a ordering is found.

3.2.2.2 Objective Function Aggregation Approaches

These approaches try to modulate a multi-objective problem into a single-objective problem, by creating a new objective function that results from a polynomial combination of all the objective functions

$$F(x) = \sum_k weight_k \times f_k(x), \tag{3.15}$$

where $weight_k$ are non-negative constants that

$$\sum_k weight_k = 1. \tag{3.16}$$

which turns a multi-objective problem into a single-objective, i.e., with one objective function $F(x)$. This approach is called Conventional Weighted Aggregation (CWA)[21]. Despite its simplicity, it shows high performance dependability in the weights selection, i.e., the optimal weights are problem dependent and require an iterative approach to be estimated. Moreover, the CWA approach is unable to detect solutions in concave regions of the Pareto front [22]. To surpass all this limitations, a dynamic weights approach was proposed in [22] for bi-objective problems. This approach is Dynamic Weighted Aggregation (DWA) and can be defined as

$$w_1(t) = \|sin(2\pi t/a\| \tag{3.17}$$

$$w_2(t) = 1 - w_2(t), \tag{3.18}$$

where t is the iteration counter and a is a user-defined constant that determines the adaptation frequency. As expected the DWA outperforms the CWA as can be seen in [19].

3.2.2.3 Conclusions

As stated before, PSO is an algorithm that focus on a cooperative approach to solve non-linear problems, being well suited for continuous space exploration. When faced with a multi-objective problem changes must be made to the original algorithm. A static Lexicographic ordering approach performance, has a strong correlation with the priorities scheme that is set. To relax this problem, a probabilistic version was defined. Objective Function aggregation allows a quantification of the importance of the some cost function. Thus, one can state that it has a larger number of degrees of freedom than the Lexicographic ordering, thus being more versatile but harder to tune.

3.3 Aligning DDMNT Design and PSO Optimization

To achieve the solutions mentioned in the previous section a multi-objective particle swarm optimization (PSO) algorithm was set to be developed. PSO intrinsically benefits from important properties that align with the problem in hands. Since the problem search space is not well behaved (has a lot of local minima), classical optimization algorithms like gradient-descent or Newton's method are not well suited since they use gradient information. Because PSO is a gradient free algorithm, local minima does not necessarily imply an erroneous convergence. Indeed, in the PSO perspective its more suited to talk about promising solution space regions instead of local minima, and one can state that the algorithm converged to a local minima when the majority of the particles reside in the same region, making the velocity updates negligible. Therefore, to attain robustness against local minima convergence, the PSO algorithm should first explore for promising regions and finally exploit those promising regions. This is known as the exploration-exploitation trade-of and it is easily tweaked in PSO. Genetic algorithms also provide a gradient-free optimization, and also has the exploration-exploitation interface embedded in the form of selection and mutations/crossovers, but it falls short since it needs a binary separation, making it not the most suitable for continuous search space problems.

3.3.1 Algorithm Objectives and Constraints

3.3.1.1 Objectives

As stated in the previous chapter, there are four mandatory properties that the final MNT should exhibit.

- Three different impedance levels:
    - $R_{10} = (10 + 0j) \times (1 \pm \varepsilon_{11})\Omega$
    - $R_{20} = (20 + 0j) \times (1 \pm \varepsilon_{12})\Omega$

– $R_{30} = (30 + 0j) \times (1 \pm \varepsilon_{13})\Omega$

– $\varepsilon_{11}, \varepsilon_{12}, \varepsilon_{11} \leq 0.1\%$

- High efficiency for all the impedance levels ($\geq 85\%$).

- Low current phase difference at the antenna, between the different impedance levels ($\leq 1°$).

- Low harmonic content on the drain voltage.

From preliminary studies, it was possible to conclude that, since the harmonic traps could be designed to achieve high Q values, its effect at the fundamental frequency could be neglected from the optimization process, leaving only three different objectives. To tackle the multi-objective challenge, a objective function aggregation approach was used. Assuming that

- $\varepsilon_1 = f_1(p)$

- $\varepsilon_2 = f_2(p)$

- $\varepsilon_3 = f_3(p)$

where $f_x(p)$ is a function that receives as argument the particle under evaluation and ε_1, ε_2, ε_3 are the errors in terms of the first, second and third aforementioned objectives, respectively. Finally, these functions can be combined to form the final objective function, $f_{final}(p)$ as

$$f_{final}(p) = a_1 \times f_1(p) + a_2 \times f_2(p) + a_3 \times f_3(p) \tag{3.19}$$

Note that despite being easy to implement, several problems arise from this approach, mainly because the different objectives work on different scales (Zin, degrees, efficiency), and some are unbounded (Zin), no normalization can be performed, thus imposing an undesired intrinsic prioritization, since high errors are more likely to be optimized first. This in turn motivates the tweaking of the a_1, a_2 and a_3 constants, in an attempt to mitigate the aforementioned problem.

3.3.1.2 Constraints

The solutions computed are set to be applied, so they must be physically feasible. Therefore, the algorithm must be constrained to search for solutions in some defined finite interval of physically feasible values, therefore,

- C $\in \left[C_{MIN} : C_{MAX} \right]$

- L $\in \left[L_{MIN} : L_{MAX} \right]$

3.3.1.3 Summary

One can summarize the objectives and goals as follows,

$$
\begin{cases}
Min\left[f_{final}(p)\right], \quad \textbf{s.t. } C \in \left[C_{MIN}:C_{MAX}\right], \ L \in \left[L_{MIN}:L_{MAX}\right] \\[2em]
f_{final}(p) = a_1 \times f_1(p) + a_2 \times f_2(p) + a_3 \times f_3(p) \\[2em]
p \in R^{11}, \ a_x \in R^1
\end{cases}
\tag{3.20}
$$

3.4 Algorithm Flow, Objectives and Constraints

3.4.1 Algorithm Flow

The fundamental blocks of the PSO algorithms are the particles. In a first stage, the particles can be defined as,

$$
Particle_{1^{st}_i} = \begin{bmatrix} c_{1_1} & c_{1_2} & c_{1_3} & c_{2_1} & c_{2_2} & c_{2_3} & c_{3_1} & c_{3_2} & c_{3_3} & l_1 & l_2 \end{bmatrix}
\tag{3.21}
$$

where c_{k_i} represents the capacitor i of the level k and l_x the x inductor, both from the circuit in figure fig. 3.13. The full swarm is the congregation of all the particles,

$$
Swarm_{1^{st}} = \begin{bmatrix} Particle_{1^{st}_1} \\ Particle_{1^{st}_2} \\ ... \\ Particle_{1^{st}_n} \end{bmatrix}
\tag{3.22}
$$

One should interpret the particles as possible solutions, and after each movement each particle is evaluated and compared with its personal best solution (P_{BEST}) and the actual global best solution (G_{BEST}). So, the basic algorithm flow is:
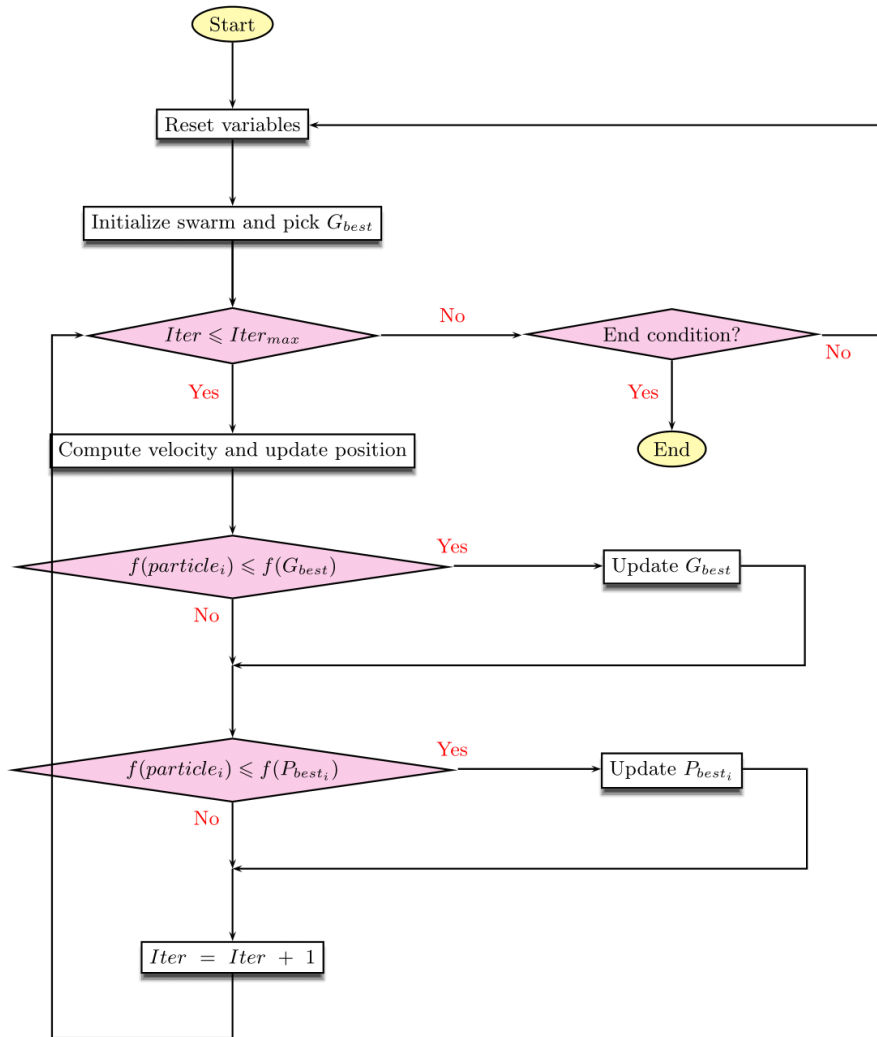
Figure 3.16: Base Algorithm flow chart

3.5   Proposed Algorithm Modifications

Several modifications were made to the base algorithm, in an attempt to improve the robustness, the flexibility and convergence. Consider the following equation, noting that it is equal to (3.10)

$$V_i(t+1) = \omega \times V_i(t) + c_1 \times r_1 \times (Pbest_i(t) - X_i(t)) + c_2 \times r_2 \times (Gbest(t) - X_i(t)) \qquad (3.23)$$

these parameters were explained before, its transcript is just to ease the lecture of the following subsections.

3.5.1 Cognitive vs Social Behavior

As stated before, the constants c_1 and c_2 from (3.23) control the importance given by the particle to their own experience and the group's experience. In [16] it was shown that the optimal values were such that $c_1 + c_2 = 4$. In simple terms, a pure cognitive behavior implies that the swarm loses its cooperative aspect, meaning that the particles would never converge. On the other hand, a pure social behavior, would mean that the particles would rapidly converge for the same place, without doing any significant individual exploration, meaning that the algorithm would most probably converge to a local minima. The first modification proposed was to use the previously stated facts to make the algorithm more robust to local minima, by enforcing a strong exploration behavior in early stages of the algorithm and gradually shifting to a exploitation behavior. To attain this, changes to (3.23) were done, such that,

$$
\begin{cases}
V_i(t+1) = \omega \times V_i(t) + c_1 \times r_1 \times (Pbest_i(t) - X_i(t)) \times \mu + c_2 \times r_2 \times (Gbest(t) - X_i(t)) \times (1-\mu) \\
\\
\mu = \frac{t}{t_{max}} \\
\\
\omega = \frac{(t_{max}-t) \times ((w_{max}-w_{min}) \times rand(1) + w_{min})}{t_{max}}
\end{cases}
$$

$$(3.24)$$

where t is the current iteration number, t_{max} is the maximum iteration number, w_{max} is the maximum value that ω can attain and w_{min} is the minimum. Inspecting the equations above, one can note that for low values of t, the swarm exhibits a strongly cognitive behavior and high dependence on the previous velocity (high inertia weight). As t approximates t_{max}, the swarm behavior starts to shift to social, and the previous velocity dependence starts to diminish.

3.5.2 Different Solutions

When t reaches t_{max} the algorithm ends, yields the solution found and restarts with randomized particles. This in the author perspective has two fundamental drawbacks. First, only one solution is returned each run of the algorithm, even if two different solutions that satisfy all the objectives were found. Second, depending on the problem in hand and how it was evaluated there could be a local minima that would not satisfy all the constraints but, because it was seemingly a very promising region, it constantly forced an erroneous convergence. To mitigate the second point, the algorithm was changed so that different runs could see all the solutions found so far, thus allowing only particles different from these solutions to become G_{best} and P_{best}. The measure of similarity chosen was the Euclidean distance. In fig. 3.17 the final of the first run is shown, where only one G_{best} is present (optimal or not), then the area around the G_{best} is marked so the algorithm is deprived of selecting other particle as G_{best} in that zone (fig. 3.18), this in turn forces the algorithm to obtain different solutions every time(optimal or not). To mitigate the first point, the algorithm was allowed to save as G_{best} all the particles that satisfied the constraints. This combined with

the change previously mentioned implies that all these obtained G_{best} would be different under the applied measure of similarity. Since a particle is attracted by the G_{best}, and since now there's the possibility of more than one G_{best} being present, the particle will be attracted by the G_{best} that is closer to him, using again the Euclidean distance as the metric. The result of the these two changes combined can be seen in fig. 3.19, where 66 all different solutions were found in only 10 runs of the algorithm.
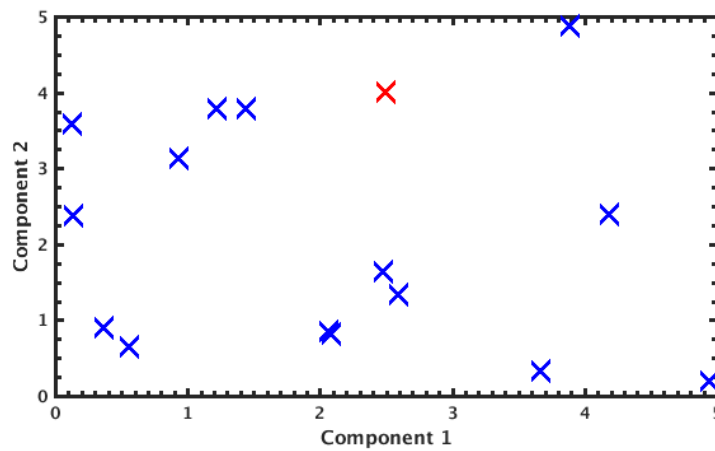
Figure 3.17: First run.*X* represent particles. The red *X* is the G_{best} particle.
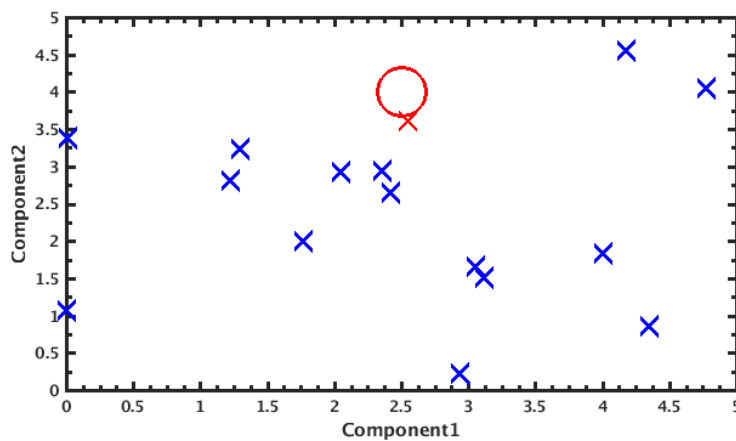
Figure 3.18: Second run. The circle represents a area where new G_{best} can't be selected.
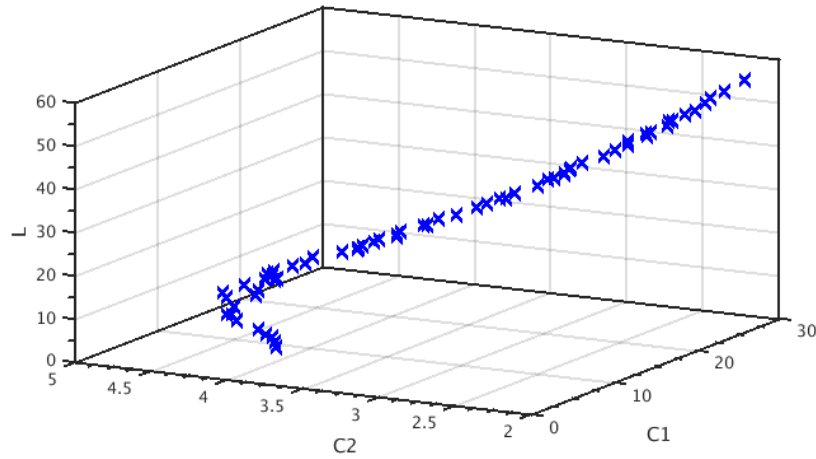
Figure 3.19: Results from Pi network circuit. 66 Solutions found in 10 runs.

3.5.3 Dynamic Weighting

From preliminary tests it could be seen that some incompatibility existed between optimizing the efficiency and the input impedance value. Most of the time the algorithm was only capable of optimizing one of these conflicting objectives. To attain a more balanced optimization a Dynamic Weighting approach, previously described was applied. In order to do this, some changes were made to (3.23), such that,

$$\begin{cases} a_1 \neq Constant \rightarrow a_1 = \left(sin\left(\frac{2\pi \times t \times 40}{t_{max}}\right) + 1\right) \times \alpha \\ a_2 \neq Constant \rightarrow a_2 = \left(1 - sin\left(\frac{2\pi \times t \times 40}{t_{max}}\right)\right) \times \alpha \\ a_3 = Constant \\ \alpha = Constant, \qquad \text{Defines weighting variation} \end{cases} \tag{3.25}$$

In summary, the final algorithm flow can be defined by,
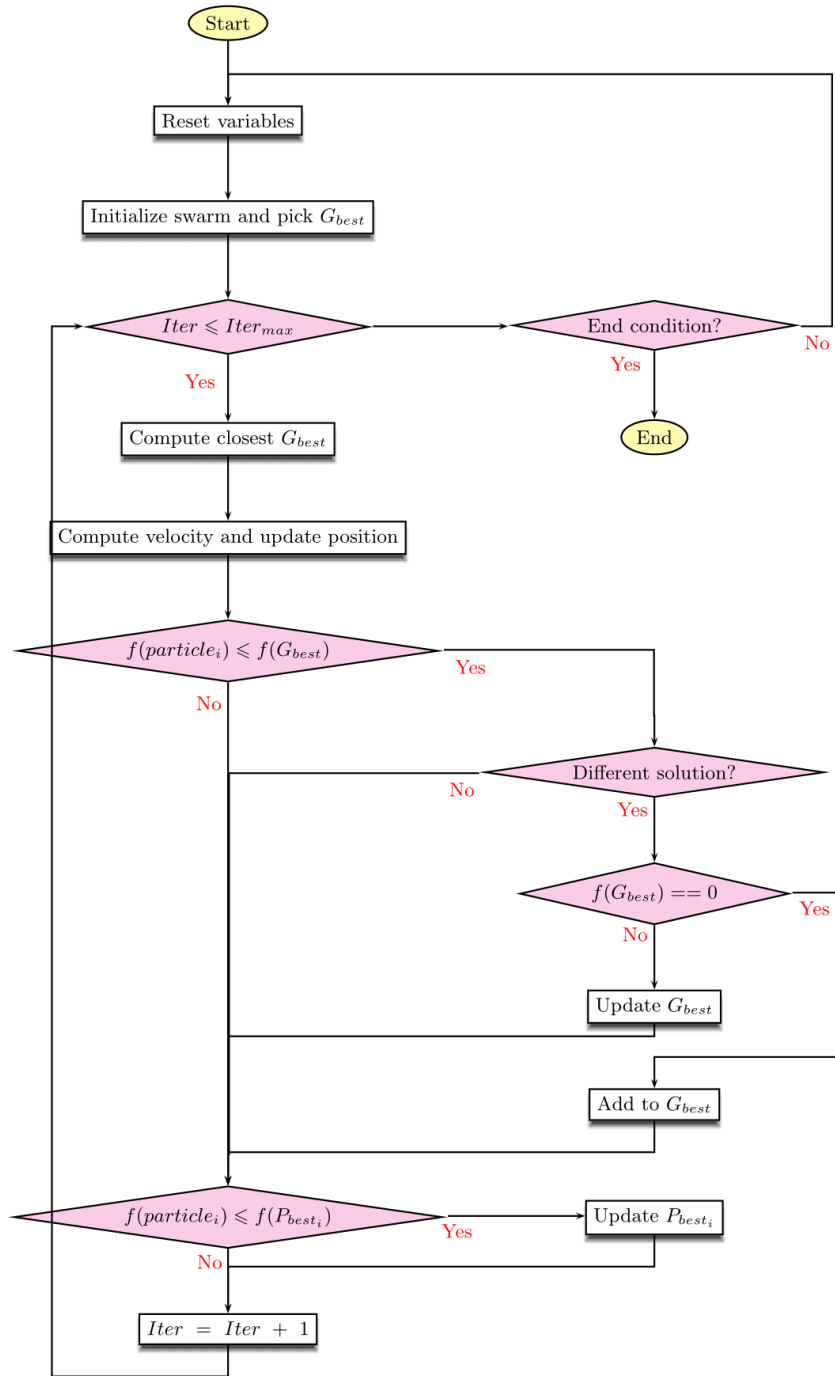
Figure 3.20: Final Algorithm flow chart

3.6 Preliminary Results

All the results obtained at this stage need validation from a simulation environment, since the optimization was made on top of matlab equations that were derived from the equivalent DDMNT

circuit. Bondwires were modeled as a 0.75nH inductor with a quality factor of 15. On chip components were modeled with capacitors with 40 quality factor. The inductor that will be used for L_{ht1} and L_{Ht2} is 0604HQ2N6 from coilcraft. The ht capacitors are set to define the resonance frequency. The only thing left to compute are the variable capacitors and both L_1 and L_2. In the next subsection the simulation values will be presented and compared with the optimization values. The results shown belong to the following computed solution,

$C_{1_{10\Omega}}$	$C_{2_{10\Omega}}$	$C_{3_{10\Omega}}$
7.78pF	11.772pF	2.3428pF

Table 3.1: 10Ω level capacitor values.

$C_{1_{20\Omega}}$	$C_{2_{20\Omega}}$	$C_{3_{20\Omega}}$
2.7376pF	9.3364pF	4.9067pF

Table 3.2: 20Ω level capacitor values.

$C_{1_{30\Omega}}$	$C_{2_{30\Omega}}$	$C_{3_{30\Omega}}$
1.6359pF	7.4673pF	6pF

Table 3.3: 30Ω level capacitor values.

L_1	L_2
2.611nH	4.5478nH

Table 3.4: L_1 and L_2 values.
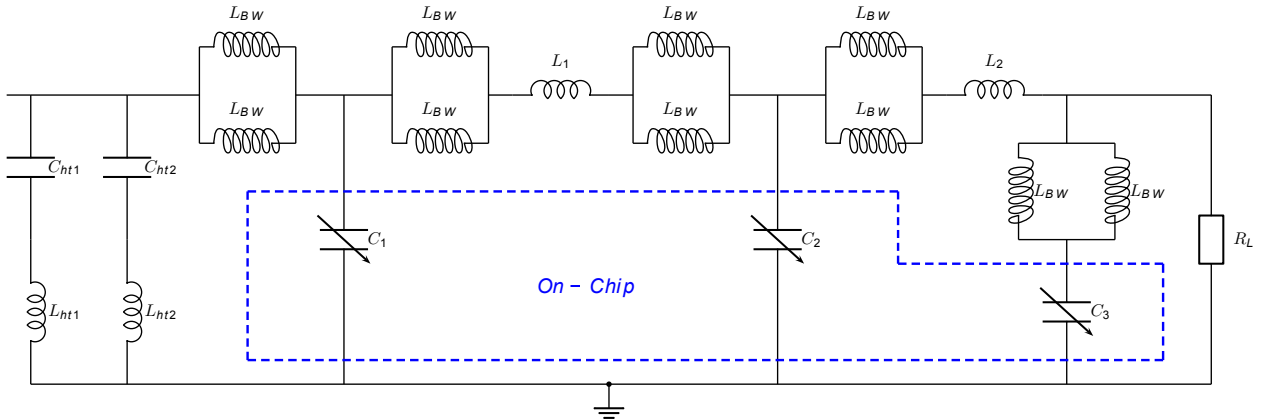
Figure 3.21: Simulation full circuit.

3.6.1 Simulation Results

3.6.1.1 10 Ω

	Optimization	Simulation
Z_{in}	10.09 - j0.01	10.12 - j0.12
Output Θ	-137.59 °	-137.602 °
Intrinsic efficiency	0.8521	0.8470

Table 3.5: 10Ω level results.
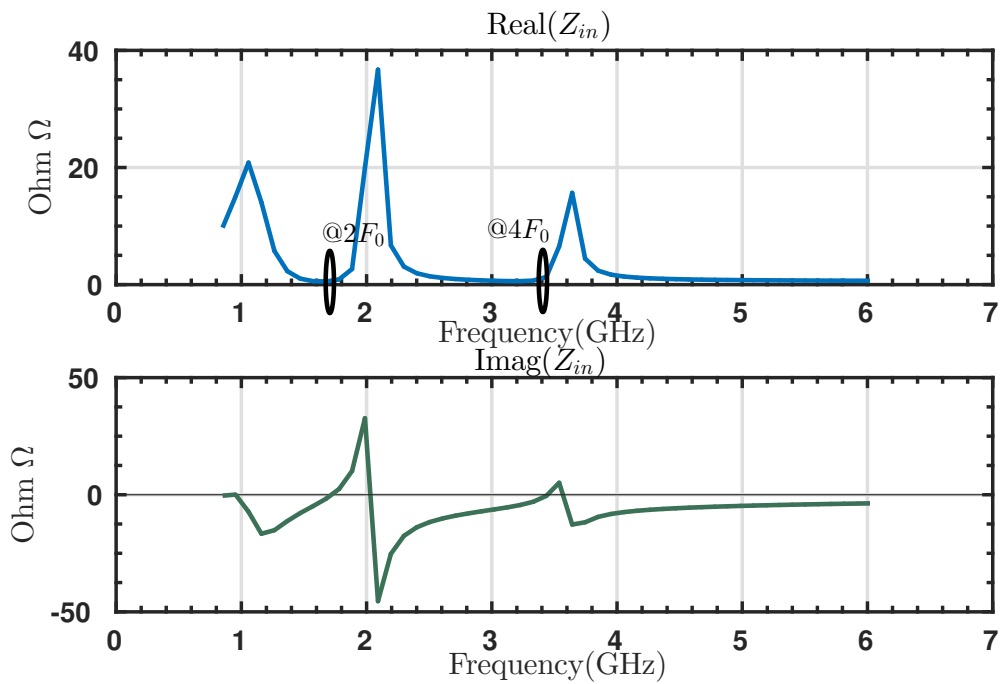
Figure 3.22: 10 Ω - Zin
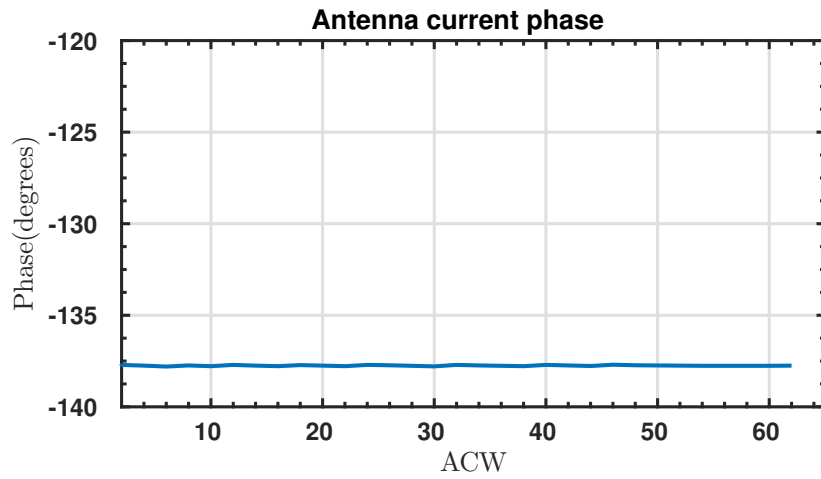
Figure 3.23: 10Ω - current phase

3.6.1.2 20 Ω

	Optimization	Simulation
Z_{in}	19.89 - j0.0075	19.65 - j0.3
Output Θ	-138.07 °	-138.0792 °
Intrinsic efficiency	0.8758	0.8992

Table 3.6: 20Ω level results.
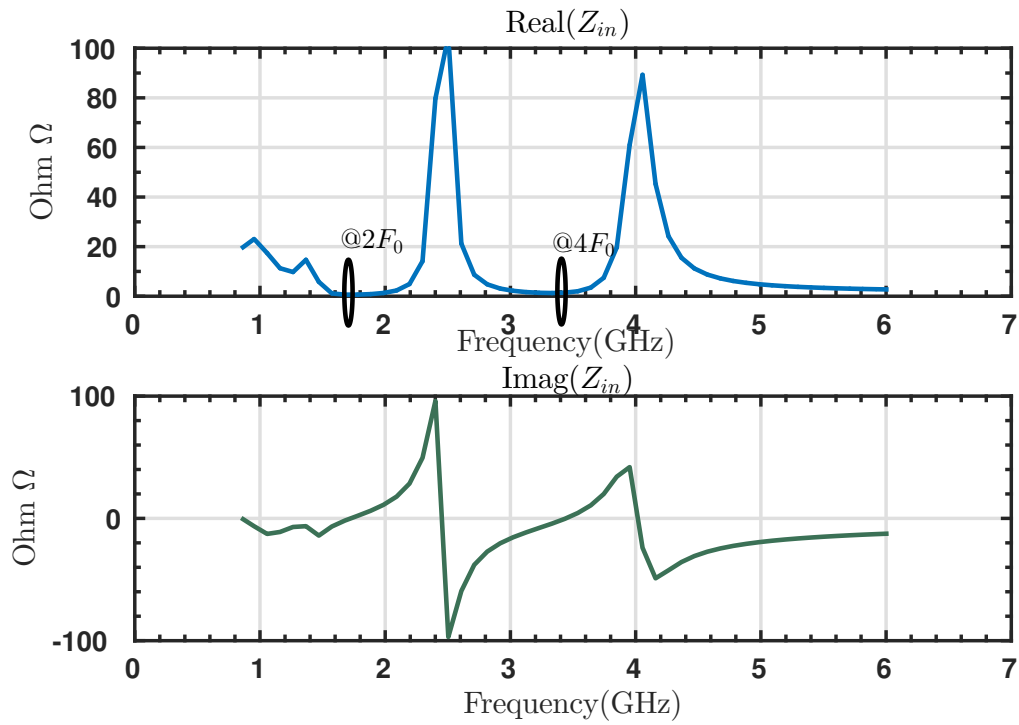
Figure 3.24: 20 Ω - Zin
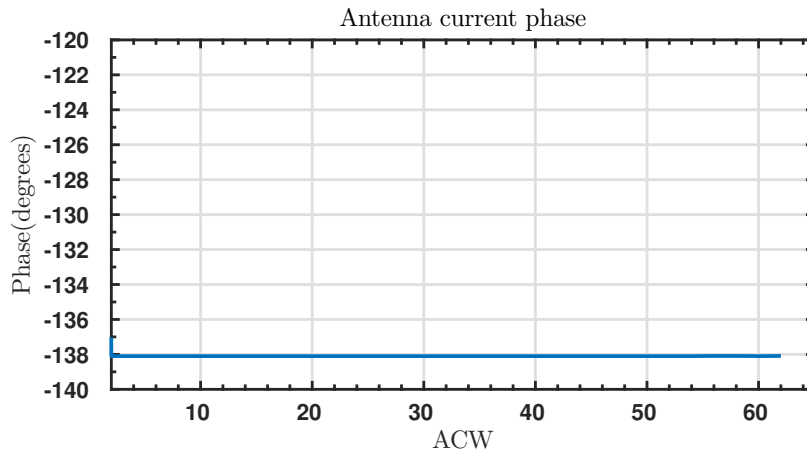
Figure 3.25: 20Ω - current phase

3.6.1.3 30 Ω

	Optimization	Simulation
Z_{in}	29.94 - j0.0025	29.45 - j0.23
Output Θ	-138.07 °	-137.078 °
Intrinsic efficiency	0.8698	0.8688

Table 3.7: 30Ω level results.
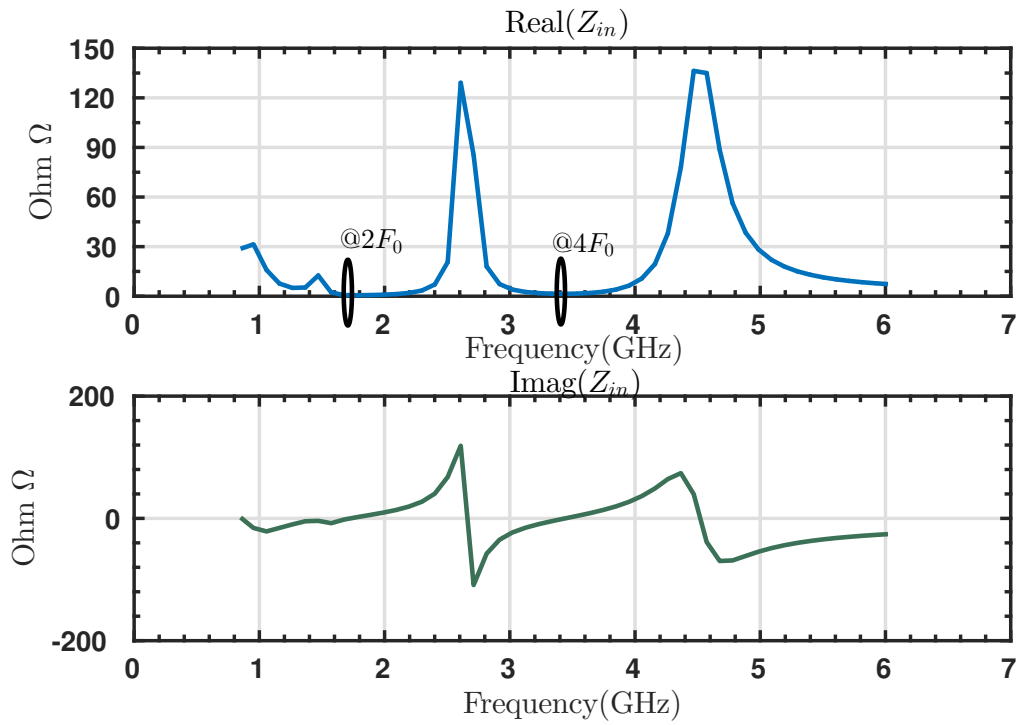
Figure 3.26: 30 Ω - Zin
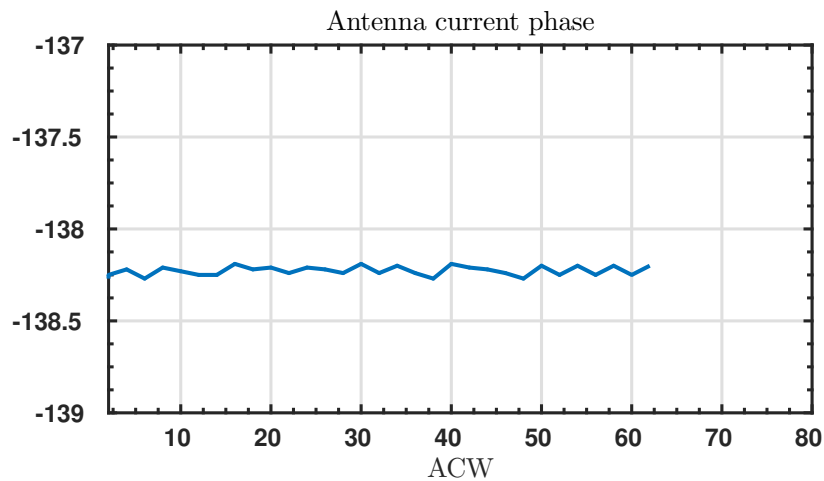
Figure 3.27: 30Ω - current phase

From the presented values, it can be seen that the optimization results are supported by the simulation environment. Small discrepancies are justified by the use of real s-parameters blocks on simulation, meaning that a 2.6nH real inductor, is in fact a 2.4nH inductor for our target frequency, inducing a miss-match on the harmonic traps, making them have some (small) impact at the fundamental frequency.

3.6.1.4 Efficiency Profiles

In fig. 3.28 it is possible to see the efficiency profile of the system DPA plus the DMNT of the different impedance levels. The 10 Ω impedance level exhibits a linear efficiency profile with almost zero deviation from the ideal behavior (max deviation = 0.23dB), this was expected since the 10 Ω level was matched to the peak power, therefore it should never enter the triode region. On other hand, as we start deviating from the peak power, the efficiency starts to decrease, which is also an expected behavior. Examining the 20 Ω impedance level it is possible to note that compression starts at lower ACW levels when compared to 10 Ω This is also expected since the DPA works in saturation, it always imposes the same current independently of the presented load. Hence, if the load increases the drain voltage increases aswell making the DPA enter the triode region faster. The compression appears roughly at half the input power level of the 10 Ω, since 20 Ω/10 Ω = 2. All these points also apply for the 30 Ω level. In fig. 3.29 it is possible to see the DMNT+DPA efficiency profile, and compare it with a 10 Ω static level, the efficiency improvement is notorious. Also in fig. 3.30 it is possible to see the phase distortion induced by the switching.
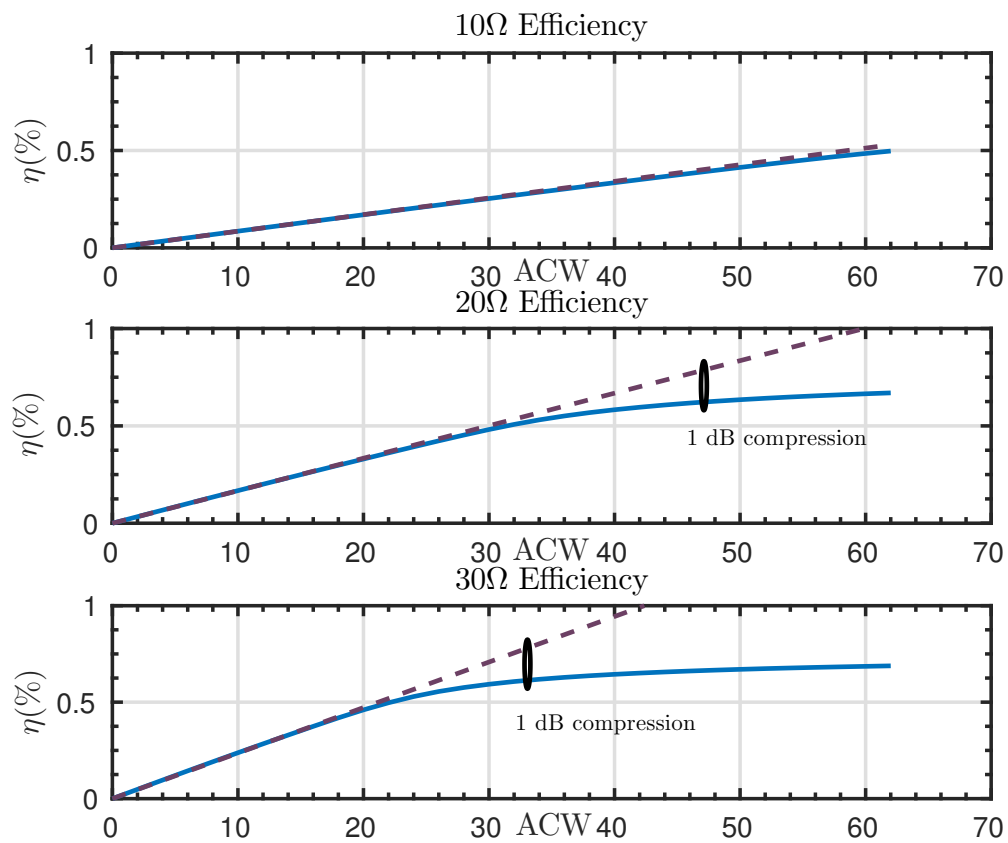
Figure 3.28: Three power profiles
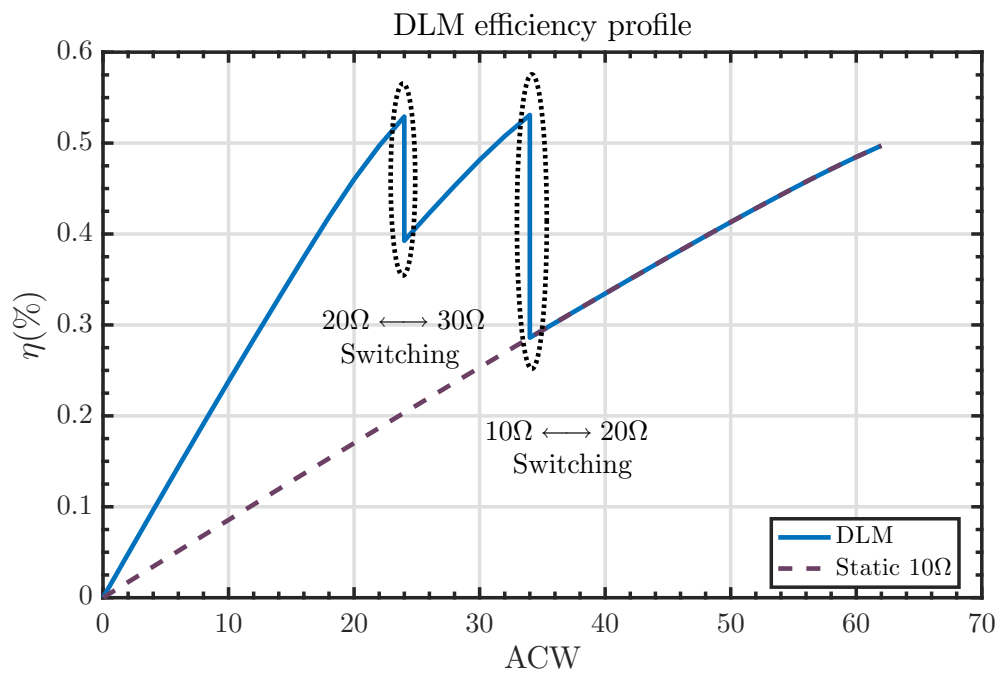
Figure 3.29: DDMMT power profile
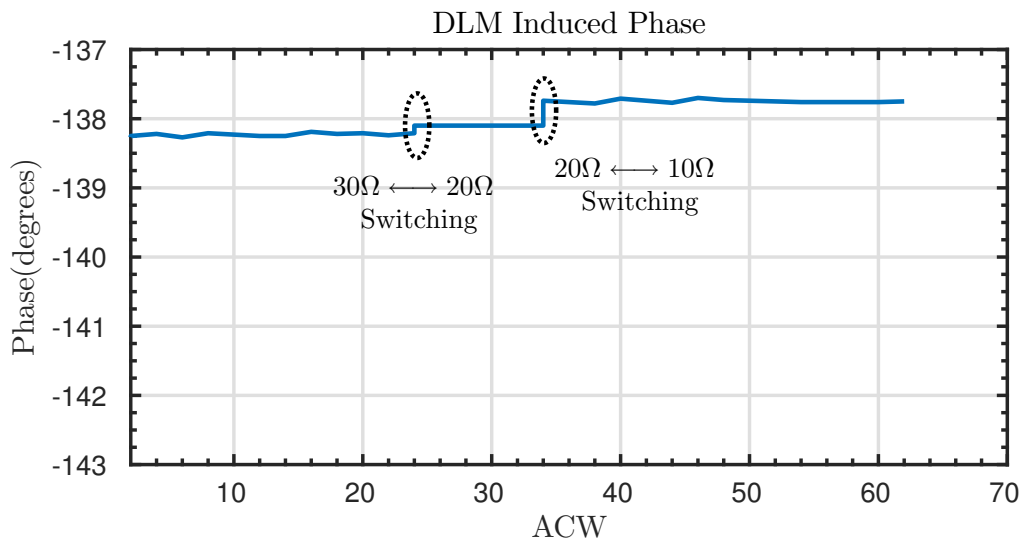
Figure 3.30: DDMNT AM–PM profile

Chapter 4

Parasitic Aware PSO Optimization

All the solutions attained so far were derived from the DDMNT equations, using some assumptions like, all the components from a given series present always the same exact behavior, linear frequency response and dismiss the effects of the integration. If one somehow, is able to consider some of these effects it would greatly improve the quality of the obtained solutions. To attain the aforementioned improvement the following methodology was developed:

- Develop an Co-Simulation between ADS and Matlab.

- In ADS the selected MNT topology was designed and the S-Param of real inductors were used.

- Also in ADS, PCB pads and bondwire models were used.

- Use manufacturer s-parameters model of real inductors for L_1 and L_2.

- The PSO-ADS loop defined.
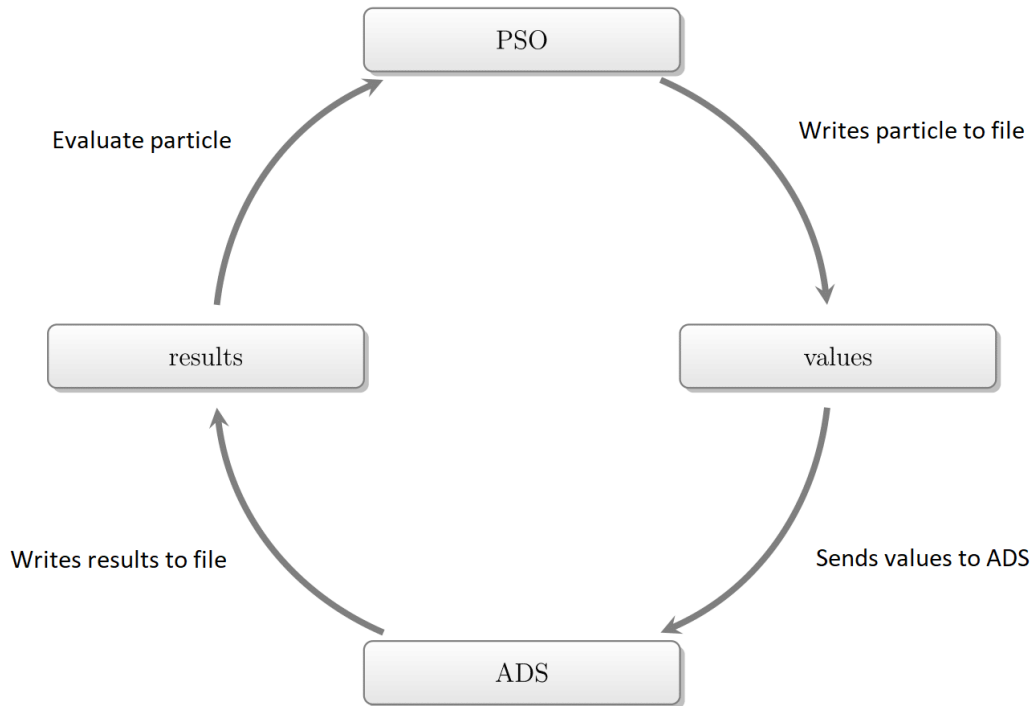
Figure 4.1: PSO-ADS optimization loop

4.0.1   PSO-ADS Optimization Loop

As stated before, as the optimization process gets closer to the real scenario improves, more robustness and reliability are added to the computed solutions. Since it is impossible to evaluate each particle in a real scenario, one must resort to a good simulation environment. The need to mitigate error caused by fabrication variation, motivated the development of a scheme capable of automatically evaluate the particles by means of simulation. In practical terms, the functions $f_1(p)$, $f_2(p)$ and $f_3(p)$ presented in (3.20), only read and evaluate the values returned by the simulation. For L_1, L_{ht1} and $Lht2$ the chosen inductor was 0604HQ2N6 and for L_2 was 0604HQ4N5 both from Coil craft. These choices are justified by the fact that the computed solutions constantly showed inductance values similar to these, and also by the fact that these models offer high Q values.

4.0.2   Solution Selection

When dealing with circuits physical implementations, one should be aware of the behavioral variations of the compounding elements of the circuit, meaning that these variations should not be able to jeopardize the circuit primary purpose. Therefore, in order to select final solution from the

several obtained solutions, the solution sensitivity in terms of the compounding fixed elements was quantified. In other words, the final solution should be the one that displayed less sensitivity to the aforementioned variations. Usually, in order to quantify some solution sensitivity, one would resort to analyze its corresponding Jacobian matrix magnitude. Since the optimization is made on top of a simulation environment, there is no direct access to the system equations, making it impossible to directly determine the Jacobian matrix. On other hand, one can make a first order approximation, and estimate the local sensitivity resorting to numerical differentiation. For example, the sensitivity of the 10Ω input impedance in terms of the L_1 inductor can be obtained as follows,

$$\frac{dZ_{10}}{dL_1} \simeq \frac{Z_{10}(L_1 + \Delta L_1) \cdot Z_{10}(L_1)}{\Delta L_1} \tag{4.1}$$

where ΔL_1 is an induced variation. The induced variation, ΔL_1 should be as small as possible in order to preserve this approximation integrity.

4.0.3 Capacitance Levels Selection

Selecting the most insensitive solution is not sufficient to guarantee that the target conditions will be met. Thus, the matching network should be designed in such a way that its dynamic on-chip components, are able to compensate possible variations on the fixed components. Therefore, the switched capacitors will be design to attain 32 different values, with a fixed step. To define the capacitance interval, the following procedure was done after obtaining the final solution,

- Add small error to a fixed component.

- Initialize the swarm G_{best} with the final solution.

- Impose a smaller search space, centered in the final solution.

- Run the optimization algorithm.

- Quantify the variation between the final solution and the one obtained in this stage.

- Repeat for all the fixed components.

- Build the final capacitance interval.

4.0.4 Final Results

Since the optimization is done on top of a simulation environment no validation is necessary. Therefore, for the central frequency 860MHz, the final results are,

10Ω

- $C_{1_{10\Omega}} = 7.767\text{pF}$

- $C_{2_{10\Omega}} = 12.2928\text{pF}$

- $C_{3_{10\Omega}} = 2.3157\text{pF}$

- $Z_{in} = 10.092 - j0.05$

- Efficiency = 0.865

- CurrentPhase = -150.24°

20Ω

- $C_{1_{20\Omega}} = 0.5012\text{pF}$

- $C_{2_{20\Omega}} = 10.7534\text{pF}$

- $C_{3_{20\Omega}} = 4.9167\text{pF}$

- $Z_{in} = 19.18 - j0.44$

- Efficiency = 0.8811

- CurrentPhase =-151.135°

30Ω

- $C_{1_{30\Omega}} = 0.5\text{pF}$

- $C_{2_{30\Omega}} = 7.9441\text{pF}$

- $C_{3_{30\Omega}} = 5.2114\text{pF}$

- $Z_{in} = 27.16 - j5.46$

- Efficiency = 0.886

- CurrentPhase = -150°

And following the aforementioned described procedure, the capaciante interval obtained was,

- $C_1 = [1.44 ; 8.03]\text{pF}$ with 0,2125pF step.

- $C_2 = [3.72; 13]\text{pF}$ with 0,2994pF step.

- $C_3 = [1.366 ; 5.737]\text{pF}$ with 0,141pF step.

A IC was designed, and fabricated using this solution, and can be seen in Fig. 4.2. This in turn motivates the development of a test setup capable of testing the IC, and validate the simulation environment. Indeed, is not a straightforward task to test an IC, since its not possible to measure its parameters directly. All this considerations are object of scrutiny in the following section.
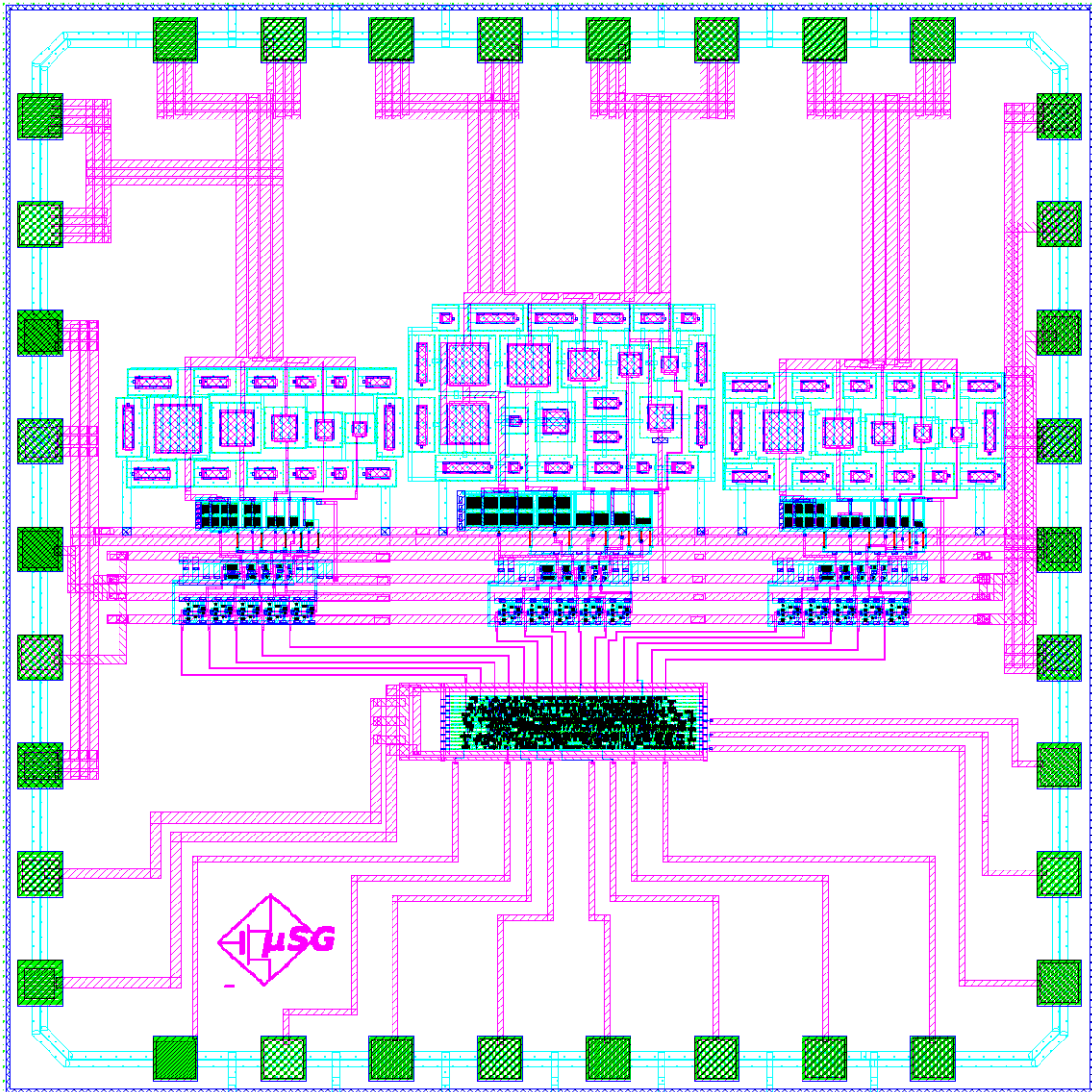

Figure 4.2: DMNT IC layout

4.1   IC Testing and De-Embedding

After the design and fabrication the integrated circuit must be tested, in order to quantify its functional constraints, functional behavior and real performance. One should note, that errors found at this stage of the project can be painfully expensive, therefore, the use of techniques to mitigate the probability of its occurrence are mandatory. The goal of some of these techniques is to approximate the simulation environment to the real scenario, as proposed in the previous chapter. For high frequency, the wavelength and the circuitry size fall in the same scale, this implies that the effects of auxiliary circuitry (connectors etc.) are not negligible, and must be taken into account. The process of eliminating effects of intervening structures of the measured parameters has been termed de-embedding [23]. Since the focus is to take the parameters of the IC, the goal of any measurement is to discern the true response of the device under test (DUT) Fig. 4.4. As stated before any measurement is never solely the response of the DUT alone, but the DUT plus the effect of the extra circuitry needed for measurement/integration. In other words, if one does not correct for the aforementioned effects, from the measurements no conclusions can be made regarding the true DUT response, since it can be heavily masked by the extra circuitry.

4.1.1   Scattering Parameters

While studying some device / component, one should resort to models that assume a black box model of the device, and is able to quantify its characteristics by means of the measurements performed at its input and output channel (for a 2 port network). One of such models is the scattering parameters model. The scattering parameters quantify different relationships between the input, reflected and transmitted wave, and some important properties are easily extracted from them, like losses, input/output impedance, introduced phase and so on. In summary the scattering parameters can be defined as follows,

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & T_{22} \end{bmatrix}$$

$$\begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \tag{4.2}$$

where a_1 is the measured wave coming from the circuit on port1, and b_1 is the measured input wave as seen in fig. 4.3. One should note that,

$$S_{11} = \frac{a_1}{b_1} \quad for \ b_2 = 0 \tag{4.3}$$

$$S_{21} = \frac{a_2}{b_1} \quad for \ b_2 = 0 \tag{4.4}$$

$$S_{22} = \frac{a_2}{b_2} \quad for \quad b_1 = 0 \tag{4.5}$$

$$S_{12} = \frac{a_1}{b_2} \quad for \quad b_1 = 0 \tag{4.6}$$

In this form the scattering parameters take a more well known meaning, being that S_{11} and S_{22} the reflection coefficients from the port1 and port2, respectively, S_{12} and S_{21} are the reverse and forward voltage gain, respectively.
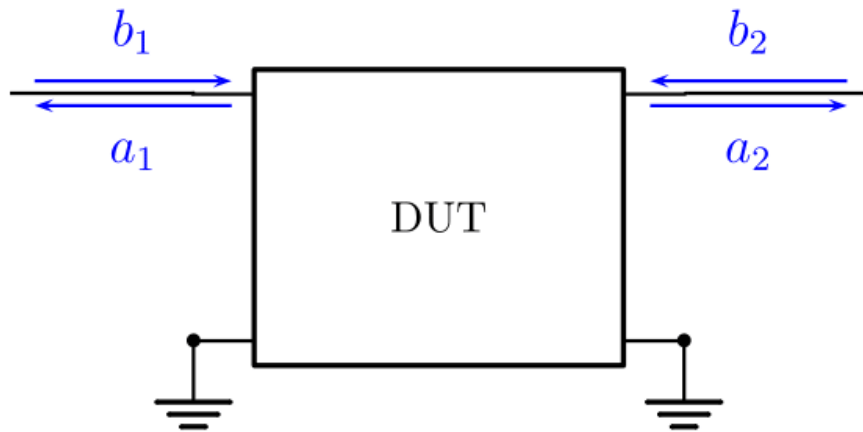
Figure 4.3: S-parameters scheme

4.1.1.1 Scattering Transfer Parameters

Since the scattering parameters assume a black box model, when dealing with a device composed with a variety of sub-devices, the measured parameters will account for all the sub-devices responses and interactions. The scattering transfer parameters (T-parameters) properties allow for the T-Parameter matrix of a cascaded network to be calculated by matrix multiplication of the compounding networks T-Parameters. Despite the fact that its direct measurement is impractical in the scope of this dissertation, the conversion S-Parameters - T-Parameters can easily be applied as follows [24],

$$T_{11} = -\frac{S_{11} \cdot S_{22} - S_{12} \cdot S_{21}}{S_{21}} \tag{4.7}$$

$$T_{12} = \frac{S_{11}}{S_{21}} \tag{4.8}$$

$$T_{21} = -\frac{S_{22}}{S_{21}} \tag{4.9}$$

$$T_{22} = \frac{1}{S_{21}} \tag{4.10}$$

4.1.2   De–Embbeding Process

Supose that T_{DUT} is the true T-Parameter matrix of the DUT, whose measurement is the main goal, the T_{AC} is the T-Parameter matrix of the auxiliary circuitry(SMA+M.line), and the T_M is the matrix that is obtained from measurement.

$$T_M = \begin{bmatrix} T_{M_{11}} & T_{M_{12}} \\ T_{M_{21}} & T_{M_{22}} \end{bmatrix} \quad T_{AC} = \begin{bmatrix} T_{AC_{11}} & T_{AC_{12}} \\ T_{AC_{21}} & T_{AC_{22}} \end{bmatrix} \quad T_{DUT} = \begin{bmatrix} T_{DUT_{11}} & T_{DUT_{12}} \\ T_{DUT_{21}} & T_{DUT_{22}} \end{bmatrix}$$

where,

$$\begin{bmatrix} T_{M_{11}} & T_{M_{12}} \\ T_{M_{21}} & T_{M_{22}} \end{bmatrix} = \begin{bmatrix} T_{AC1_{11}} & T_{AC1_{12}} \\ T_{AC1_{21}} & T_{AC1_{22}} \end{bmatrix} \cdot \begin{bmatrix} T_{DUT_{11}} & T_{DUT_{12}} \\ T_{DUT_{21}} & T_{DUT_{22}} \end{bmatrix} \cdot \begin{bmatrix} T_{AC2_{11}} & T_{AC2_{12}} \\ T_{AC2_{21}} & T_{AC2_{22}} \end{bmatrix} \tag{4.11}$$

noting that $T_{AC1} \neq T_{AC2}$ even if the circuits are the same.
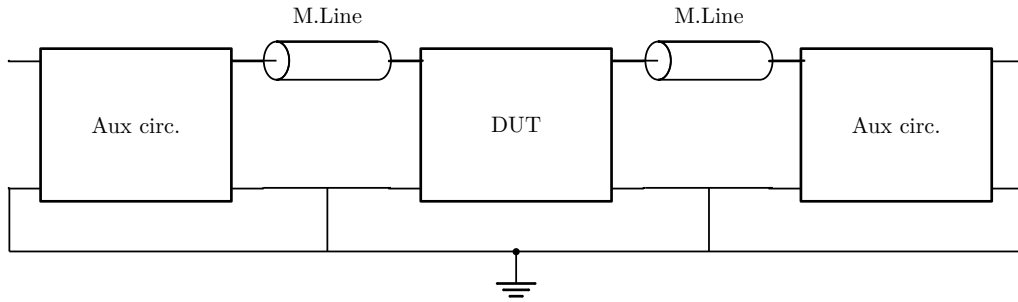
Figure 4.4: General De-Embbeding scheme. Blue dots represent the access points.

From (4.1.2), the following equation can be derived,

$$T_{DUT} = T_{AC1}^{-1} \cdot T_M \cdot T_{AC2}^{-1} \tag{4.12}$$

Thus, the goal will be to obtain T_{AC1} and T_{AC2} to finally calculate T_{DUT}. Those values will be attained by means of a incremental optimization, whose objective is to approximate the response of a given simulation environment circuit to T_{AC1} and T_{AC2}. Using the two-microstrip-line method [25], one can extract the subtract dielectric constant with an error 0.5 - 1 percent, and measure the dielectric constant as it varies with frequency. This dielectric constant can then be plugged into an ADS microstrip model. After obtaining the microstrip model, the SMA to trace transition will be modeled optimizing the circuit Fig. 4.6 [26], using a similar PSO-ADS loop defined in the previous chapter .

4.1.3 Transmission Line De–Embedding
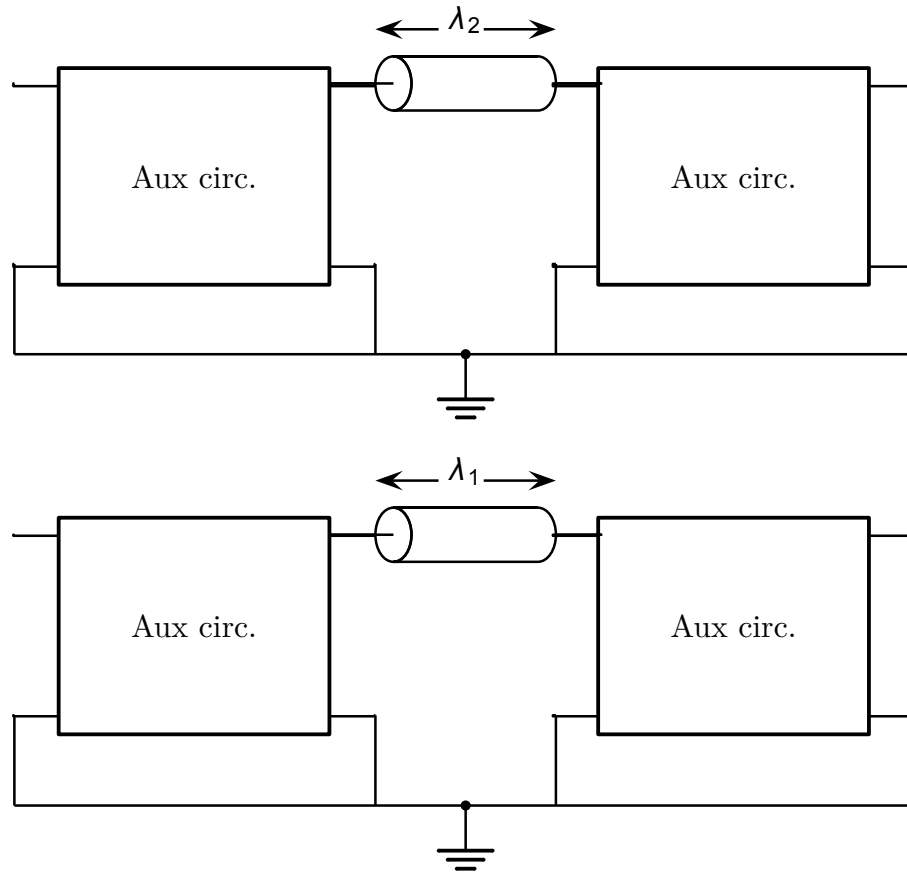
Figure 4.5: General De–Embbeding scheme. Blue dots represent the access points.

The circuit shown in the fig. 4.5 will be used to obtain the substract dielectric constant, as stated before. From [25], the following relationship can be derived,

$$\sqrt{\varepsilon_{eff}} = \frac{\Delta l_e}{\Delta l_p} \tag{4.13}$$

where Δl_p is the physical length difference between the two microstrip lines, and the Δl_e is the electrical length difference between the two microstrip lines. Because the phase is measured in degrees, and its value is confined on the interval $-\frac{\pi}{2} : \frac{\pi}{2}$, a frequency sweep from low frequency must be done, and the phase measured accumulated, in order to *unroll* the phase, and obtain the absolute value. Also it is worth to mention that, this method works under the assumption that both SMA impose the same phase difference, this is not true and can induce error. The larger the difference between λ_1 and λ_2 the sturdiest the obtained result is against this source of error. Finally, the ε_{eff} can be calculated as follows,

$$\varepsilon_{eff}(f) = \left(\frac{\Delta\, Phase(f) \cdot c}{360 \cdot f \cdot \Delta l_p}\right)^2 \tag{4.14}$$

where $\Delta\,Phase(f)$ is the absolute phase difference, in degrees, between the two lines at frequency f, and c is the speed of light.

4.1.3.1   SMA-Trace Transition Modeling

As stated before, after obtaining the substract dielectric constant, a optimization loop similar to the one used in the previous section will be developed in order to fit the measured S-Parameters. To model the SMA-trace transition the circuit[26] of figure will be used. Thus, to model the circuit of figure, the PSO-ADS loop will fit the circuit of fig. 4.6.
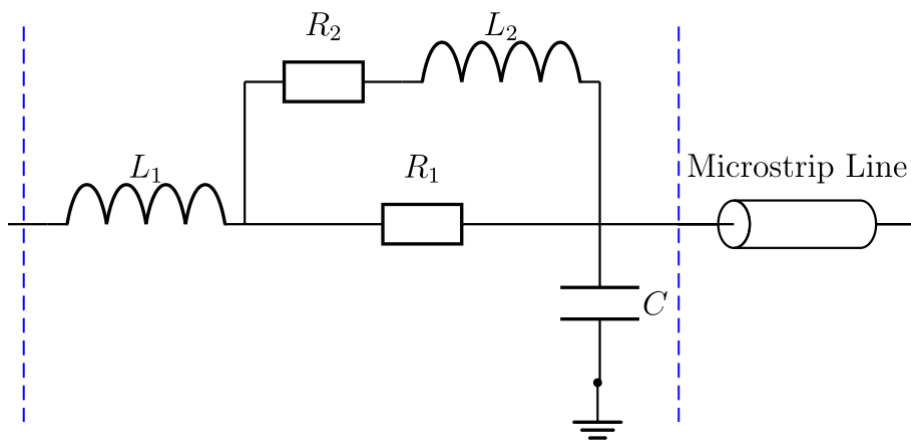
Figure 4.6: Proposed circuit for SMA-trace transition fitting

4.1.3.2   Measured Parameters De–Embedding

A test circuit like the one presented in fig. 4.5 was fabricated and can be seen in fig. 4.7, where $\lambda_1 = 40mm$ and $\lambda_2 = 10mm$. The test circuit can be defined as,

$$T_{tc} = T_{SMA1} \cdot T_{line} \cdot T_{SMA2} \tag{4.15}$$

where T_{SMA1} is the T-matrix of the leftmost sma and T_{line} is the transmission line T-matrix. After the process described in section 4.1.3, it is possible to obtain a reliable transmission line model in ADS, keeping in mind that a perfect model is never attained. With this transmission line model a fitting circuit is defined,

$$T_{fit} = T_{c.fit1} \cdot T_{ADSLine} \cdot T_{c.fit2} \tag{4.16}$$

where $T_{c.fit1}$ is the circuit presented in fig. 4.6, $T_{ADSLine}$ is a transmission line model from ADS and $T_{c.fit2}$ is the circuit presented in fig. 4.6 but flipped horizontally. The goal of the optimization is to attain $T_{fit} = T_{tc}$, but since $T_{line} \neq T_{ADSLine}$ then $T_{c.fit1} \neq T_{SMA1}$. When testing the IC, the actual de-embbeding scheme is presented in fig. 4.4, where the T_{DUT} represents the IC to be tested. This

scheme can be equally defined by,

$$T_{total} = T_{SMA1} \cdot T_{line} \cdot T_{DUT} \cdot T_{line} \cdot T_{SMA2} \tag{4.17}$$

being the goal,

$$T_{DUT} = [T_{SMA1} \cdot T_{line}]^{-1} \cdot T_{SMA1} \cdot T_{line} \cdot T_{DUT} \cdot T_{line} \cdot T_{SMA2} \cdot [T_{line} \cdot T_{SMA2}]^{-1} \tag{4.18}$$

but this is not possible to do since $T_{SMA1} \cdot T_{line}$ is an unkown matrix. But if,

$$T_{SMA1} \cdot T_{line} \simeq T_{SMA1} \cdot T_{line} \cdot T_{SMA2} \cdot T_{c.fit2}^{-1} \tag{4.19}$$

and

$$T_{line} \cdot T_{SMA2} \simeq T_{c.fit1}^{-1} \cdot T_{SMA1} \cdot T_{line} \cdot T_{SMA2} \tag{4.20}$$

then,

$$T_{DUT} \simeq T_X = [(T_{SMA1} \cdot T_{line} \cdot T_{SMA2}) \cdot T_{c.fit2}^{-1}]^{-1} \cdot T_{total} \cdot [T_{c.fit1}^{-1} \cdot (T_{SMA1} \cdot T_{line} \cdot T_{SMA2})]^{-1} \tag{4.21}$$
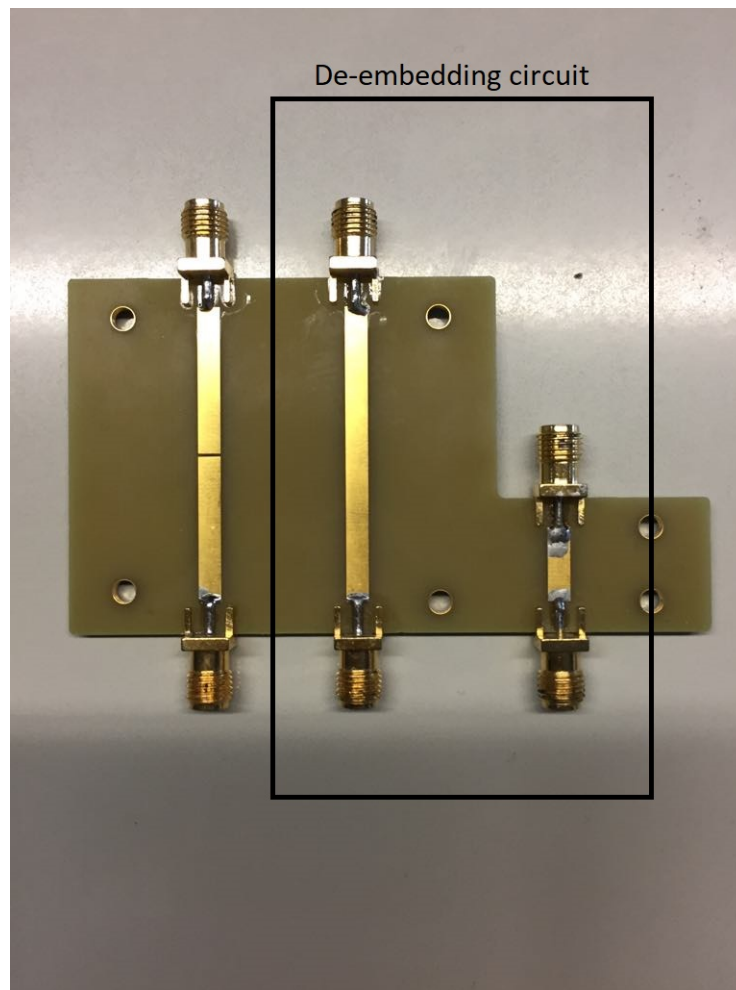
Figure 4.7: Fabricated transmission line de-embedding PCB.

Thus, the goal of this de-embedding algorithm is to attain a good SMA model in order to validate 4.19 and finally 4.18. On other hand, this also implies the necessity of a good transmission line model, that motivates the necessity of the transmission line de-embedding technique presented on Section 4.1.3.

4.1.4   Target Properties Extraction

After applying the proposed algorithm described in the previous sections, a S-parameter matrix of the IC is obtained. Even-though the S-parameters are not the goal properties used as optimization criteria, these goal properties are somehow embedded into the S-parameters model and can be extracted. In order to attain this, in the following sub-sections some formulas are derived and the thought process explained.

4.1.4.1 Zin

The S_{11} parameter can also be defined in terms of generator and load impedance as follows,

$$S_{11} = \frac{Z_{in} - Z_g}{Z_{in} + Z_g} \tag{4.22}$$

where Z_{in} is the load seen by the incoming wave, and the Z_g is the generator impedance from where the wave is coming from. Usually Z_g is well defined, and has a value of 50Ω.By rearranging the equation we can obtain,

$$Z_{in_{DUT}} = \frac{Z_g(S_{11} + 1)}{1 - S_{11}} \tag{4.23}$$

4.1.4.2 Efficiency

From the authors knowledge, there is not a straightforward way to extract the efficiency from the S-parameters, without at least one fair assumption. Efficiency can be defined as,

$$Efficiency_{DUT} = \frac{P_{out}}{P_{in}} \tag{4.24}$$

where P_{in} is the power that actually enters the DUT, and P_{out} is the power at its output. Since the DMNT has a 50Ω output, this is set to be replaced with the port2, which also is 50Ω. The power delivered by generator is

$$P_g = \frac{1}{2}Re\{V \times I^*\} = \frac{1}{2}\frac{\|b_1\|^2}{Z_g} \tag{4.25}$$

We also know that S_{11} of the incident voltage wave is reflected, so

$$P_r = \frac{1}{2}\frac{a_1 \times a_1^*}{Z_g} = \frac{1}{2}\frac{S_{11}b_1 \times (S_{11}b_1)^*}{Z_g} = \frac{1}{2}\frac{\|S_{11}b_1\|^2}{Z_g} \tag{4.26}$$

Therefore, the power that is actually delivered to the DUT is,

$$P_{in} = P_g - P_r = \frac{1}{2}\frac{\|b_1\|^2}{Z_g}(1 - \|S_{11}\|^2) \tag{4.27}$$

Since the port2 is the 50Ω load, $P_{out} = P_{port2}$,

$$P_{out} = \frac{1}{2}\frac{\|a_2\|^2}{50} = \frac{1}{2}\frac{\|S_{12}b_1\|^2}{50} \tag{4.28}$$

Note this approach is considering the power reflected back in port2 as loss of the DUT, which for small values of$\|S_{22}\|$ is a really good approximation. Nevertheless, it is a minoring approximation, meaning that any error introduced by this assumption will never improve the results. Finally, the

efficiency can be defined as,

$$Eff_{DUT} = \frac{P_{out}}{P_{in}} = \frac{\|S_{12}\|^2}{1 - \|S_{11}\|^2} \cdot \frac{Z_g}{50} \tag{4.29}$$

4.1.4.3   Current Phase

To define the current phase one must first define the reference. The reference will be b_1. Therefore, the phase at the input of the DUT is equal to,

$$\theta_{in} = angle(1 - S_{11}) \tag{4.30}$$

and once again, since port2 is the output resistor the output wave phase is,

$$\theta_{out} = angle(S_{21}) \tag{4.31}$$

and finally the DUT induced phase can be defined as,

$$\theta_{DUT} = \theta_{out} - \theta_{in} \tag{4.32}$$

4.1.5   Test Validation

The de-embedding algorithm is ready to be applied, but first it needs to be validated. In the following subsections the validation of these individual steps is attained, and the results are shown and critically described.

4.1.5.1   Test Validation – ε_{eff}

From the circuit in Fig. 4.7, the absolute phase was measured from 200MHz to 1GHz for both the tlines. Then using (4.14), the ε_{eff} for all these frequencies was attained. These results can be seen in Fig. 4.8
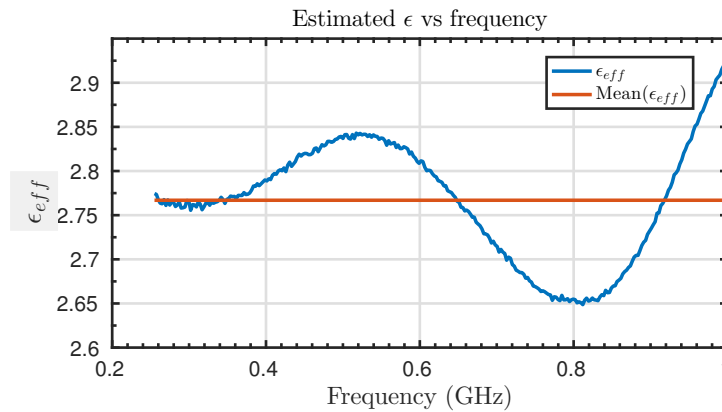

Figure 4.8: Estimated ε_{eff}

the orange line is constant because it is the mean of all the calculated ε_{eff}, and is the value that is set to be plugged into the ads mline model. $Mean(\varepsilon_{eff}) = 2.767$

4.1.5.2   Test Validation - De-Embedding

From the test circuit Fig. 4.7 the following S-Param matrix was measured,

$$S_{tc} = \begin{bmatrix} -0.0495 + j0.044 & -0.4704 - j0.8526 \\ -0.4704 - j0.8526 & -0.0495 + j0.044 \end{bmatrix}$$

from where it is possible to extract,

$$T_{tc} = \begin{bmatrix} -0.4741 - j0.8552 & -0.015 - j0.0663 \\ 0.015 + j0.0663 & -0.4961 + j0.8992 \end{bmatrix}$$

It was possible to obtain the following S-Parameters from the circuit who was subject of fitting optimization,

$$S_{fit} = \begin{bmatrix} -0.05 + j0.044 & -0.47 - j0.844 \\ -0.47 - j0.844 & -0.05 + j0.044 \end{bmatrix}$$

But for the de-embbeding purpose only the effects of the SMA followed by the transmission line are desired (or vice-versa). Thus if,

$$T_{tc} \cdot T_{c.fit2}^{-1} \simeq T_{fit} \cdot T_{fit2}^{-1} \ \Rightarrow \ T_{SMA1} \cdot T_{line} \simeq T_{SMA1} \cdot T_{line} \cdot T_{SMA2} \cdot T_{c.fit2}^{-1} \tag{4.33}$$

and

$$T_{tc} \cdot T_{c.fit2}^{-1} \simeq T_{fit} \cdot T_{fit2}^{-1} \ \Rightarrow \ T_{SMA1} \cdot T_{line} \simeq T_{SMA1} \cdot T_{line} \cdot T_{SMA2} \cdot T_{c.fit2}^{-1} \tag{4.34}$$

all the conditions described in the previous subsection are satisfied and the relation 4.21 should stand. With simple algebra manipulation,

$$S\_param[T_{tc} \cdot T_{c.fit2}^{-1}] = \begin{bmatrix} -0.0918 - j0.1592 & -0.0951 - j0.9676 \\ -0.0951 - j0.9676 & -0.091 + j0.1819 \end{bmatrix}$$

$$S\_param[T_{fit} \cdot T_{c.fit2}^{-1}] = \begin{bmatrix} -0.093 - j0.154 & -0.098 - j0.959 \\ -0.098 - j0.959 & -0.091 + j0.182 \end{bmatrix}$$

which in turn translates in following errors,

$$\varepsilon_{dB} = \begin{bmatrix} 0.11875 & 0.0745 \\ 0.0745 & 0.0031 \end{bmatrix}$$

$$\varepsilon_{phase} = \begin{bmatrix} 1.15° & 0.2245° \\ 0.2245° & 0.0024° \end{bmatrix}$$

proving that 4.33 and therefore 4.21 stands.

4.1.5.3   Additional Considerations

The aforementioned described method works under the following assumptions:

- There is no dielectric variation between the two transmission lines in the same PCB.

- All the SMAs are equal and exhibit equal parameters.

- The VNA is fully calibrated

4.1.6   IC Test setup

The fabricated IC has a SPI interface that allows to control the equivalent capacitance values. Therefore, a micro-controller will be used to control these values. Using a vector network analyzer the s-parameters from the whole integration system are going to be measured. To discern the true response of the IC, the de-embedding algorithm described in the previous sections is going to be applied. Therefore, on the integration PCB a setup similar to one presented on Fig. 4.7 needs to be present. A integration PCB with the aforementioned properties was designed and fabricated, and can be seen in Fig. 4.9.
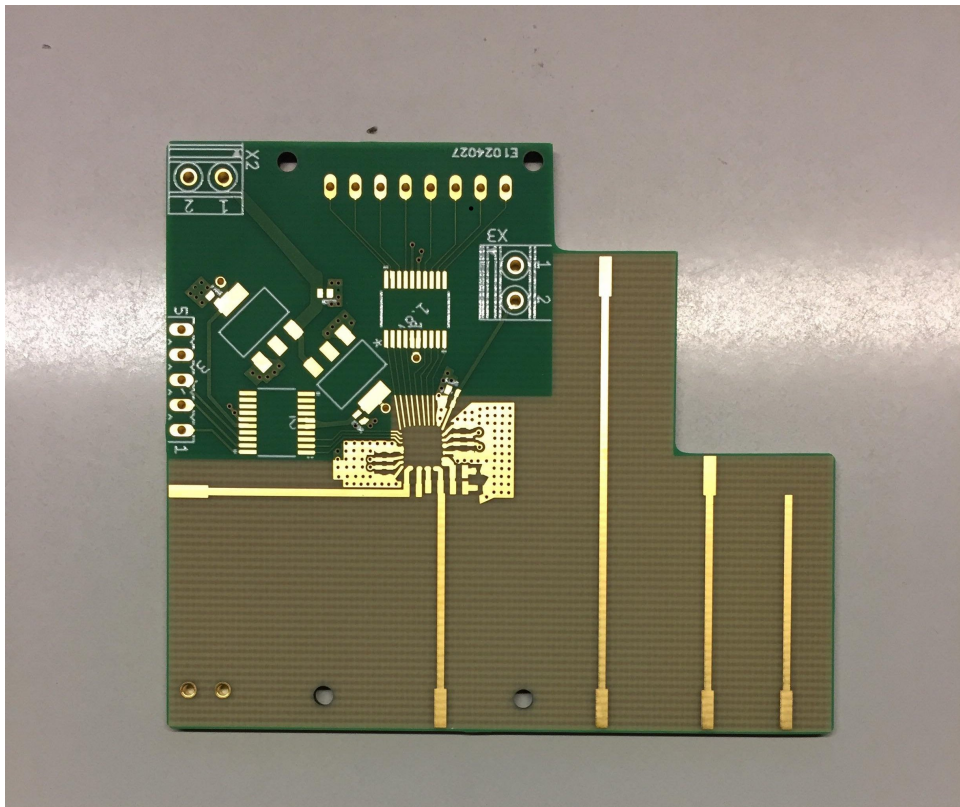

Figure 4.9: Integration PCB

Chapter 5

Conclusion

The power amplifier is a component whose optimization will be crucial, as the IoT paradigm spreads, and the 5G emerges. Thus, the development of techniques that improve this component are mandatory. The discrete dynamic load modulation is a technique that was proved capable of significantly improving the PBO efficiency without adding serious complexity to the system. The following section details the dissertation outcome, while section 6.2 enumerates several possible improvements.

5.1 Dissertation Outcomes

In this dissertation a 3 level discrete dynamic matching network was developed. In order to define the DMNT topology, a simplified optimization approach was firstly used, assuming ideal components, linear phase response etc. After selecting the DMNT topology that presented the most promising results, an optimization algorithm capable of optimizing on top of a simulation environment was developed. This allowed us to integrate the manufacturer S-parameters of the off-chip components, the ADS bond-wire models and PCB traces onto the optimization. Thus, improving the quality of the computed solutions. The results show a noteworthy improvement on the PBO efficiency, and low switching induced AM-PM distortion $< 1.2°$. In order to validate the simulation results, a physical implementation was carried out in a 180nm CMOS technology, sent to tape-out. In order to extract the properties that were target of optimization, a de-embedding technique was developed and is ready to be applied. Since S-parameters are better suited for accurate RF measurements, its study and strategy for measurement was developed.

5.2 Future Work

Despite the promising preliminary results, they must be verified by testing the DDMNT IC. Also, one should not forget that the main target of this technique is to improve the PA PBO efficiency. Therefore, the complete system DDMNT plus PA must be tested. Also, exploring

a envelope tracking technique would alleviate the efficiency degradation inside each impedance level, without adding a heavy complexity to the overall system, since the target PA is digital.

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