Interdigitated Back Contact Silicon Heterojunction Solar Cells: Towards an Industrially Applicable Structuring Method

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Abstract. We report on the investigation and comparison of two different processing approaches for interdigitated back contacted silicon heterojunction solar cells: our photolithography-based reference procedure and our newly developed shadow mask process. To this end, we analyse fill factor losses in different stages of the fabrication process. We find that although comparably high minority carrier lifetimes of about 4 ms can be observed for both concepts, the shadow masked solar cells suffer yet from poorly passivated emitter regions and significantly higher series resistance. Approaches for addressing the observed issues are outlined and first solar cell results with efficiencies of about 17 % and 23 % for shadow masked and photolithographically structured solar cells, respectively, are presented.

INTRODUCTION

The interdigitated back contacted silicon heterojunction (IBC SHJ) solar cell, introduced in 2007 [1], is currently the most successful silicon wafer-based high-efficiency approach, with record power conversion efficiencies (η) of 26.7 % [2, 3]. It combines the advantages of both IBC cells (i. e. high short-circuit currents, j_{sc}, by small optical losses due to the omission of a front grid) and SHJ cells (i. e. high open-circuit voltages, V_{oc}, by excellent interface passivation). Within the SHJ concept [4], a thick monocrystalline n-doped silicon absorber (c-Si) is bifacially passivated by thin (usually 5–10 nm [5]) hydrogenated amorphous silicon layers (a-Si:H) [6]. The passivation mechanism is understood to work mainly chemically, i. e. by saturation of dangling bonds at the c-Si surface by hydrogen atoms from the a-Si:H layer [7]. The hereby suppressed surface recombination leads to high V_{oc}s, as the potential of the lowly defective bulk material can now be utilised. For IBC solar cells [8], the electrodes for both electrons and holes are positioned on the rear side of the cell in interdigitated patterns. Thus, a front grid can be omitted and no shadow losses occur on the front side of the cell, yielding a high j_{sc}. Furthermore this opens up the opportunity to place the focus of optimisation on optical properties for the front side and on electrical properties for the rear side, respectively. However, the well-established and vastly used preparation of IBC SHJ solar cells, applying lab-based photolithographic processes, is complex, expensive, and not applicable in industrial fabrication. To support the wide distribution of this promising technology, it is hence crucial to develop simplified, damage-free, and cost-effective preparation processes, while maintaining exceptional solar cell properties. Various alternative patterning techniques for the substitution of photolithography have been presented in the past by ourselves and other groups [9–11]. Here we demonstrate the successful development of a photolithography-free patterning technique using solely *in-situ* shadow masks during plasma-enhanced chemical vapour deposition (PECVD), and show in

detail its advantages and challenges as compared to our photolithography-based preparation process. First solar cell results are presented and discussed with respect to further improvement of the passivation and minimisation of the contact resistance.

EXPERIMENTAL

All samples have been prepared using 4″ rear-side polished n-type Fz wafers with a nominal resistivity of 1–5 Ωcm and an approximate thickness of 280 µm. The front side of these wafers has been random pyramid textured, using a KOH containing solution [12]. Shadow masks have been prepared using 150 µm thick 5″ as-cut Cz wafers. An IR ps-pulse laser was used to cut the shadow masks from the Cz wafers as well as alignment holes in the sample wafers. Initially, the latter were cleaned with a standard RCA clean [13] and afterwards dipped in a 1 % diluted HF solution to remove the oxide formed on the wafer surfaces during RCA cleaning. The wafers were then immediately loaded into an AKT1600 PECVD cluster tool operating at 13.56 MHz. At the front side, a stack of 15 nm a-Si:H(i) (passivation), 70 nm SiN_x (antireflection coating, ARC), and 100 nm a-Si:H(i) (a sacrificial layer to protect the ARC during wet-chemical processes) was deposited. Subsequently the wafers were relocated to a clean PECVD carrier for rear-side passivation by a 5–10 nm a-Si:H(i) layer. Wafers and shadow masks were then attached to a specially designed sample holder. Alignment was achieved by the aforementioned laser-cut holes in the wafers and pins on the sample holder (cf. Fig. 1). Highly doped n-type nanocrystalline Si:H (nc-Si:H) [14] was deposited on the designated portions of the wafer's rear side through the slits of the mask, forming a back surface field (BSF). The procedure was repeated to form the emitter portions with highly doped p-type a-Si:H. All rear-side layers (i, n, and p) were deposited in separate chambers to prevent cross contamination of the layers. Different shadow masks with different slit widths as well as different sample holders were used for n- and p-regions. Transient photoconductance decay (TrPCD) measurements using a Sinton WCT-100 setup in transient mode [15] were carried out to verify the passivation quality of the deposited a-Si:H(i) layers. Photoluminescence (PL) measurements were carried out as well for the same purpose. Finally the rear side contact stack was formed by sputter deposition of a 150 nm thick layer of indium tin oxide (ITO) [16] in a Roth & Rau RF sputter tool, followed by thermal evaporation of 1.5 µm Ag in a Creavac Creamet 350 tool. The contact stack was then structured by photolithography to separate the n- and p-regions, followed by the removal of the sacrificial a-Si:H(i) layer on the front side. All samples were annealed for 10 min at 200 °C to cure sputter damage [17]. Illuminated one-sun current–voltage (j–V) and SunsVoc [18] measurements were carried out on the finalised cells using a class AAA solar simulator and the aforementioned Sinton WCT-100 setup, respectively. In Fig. 2, a schematic of the cell structure presented here is shown, along with a photograph of the rear side of a cell. In the following sections, we compare our shadow-mask structured cells (henceforth referred to as SMC) with our best photolithographically structured cells (henceforth referred to as PLC), developed earlier.

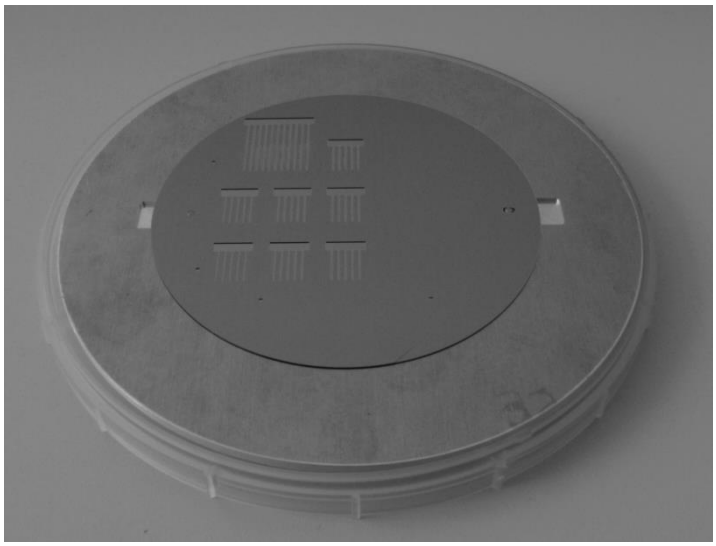

FIGURE 1. Image of a prepared sample holder with a wafer and a shadow mask attached to it. Alignment is achieved through pins (sample holder) and holes (wafer and mask).

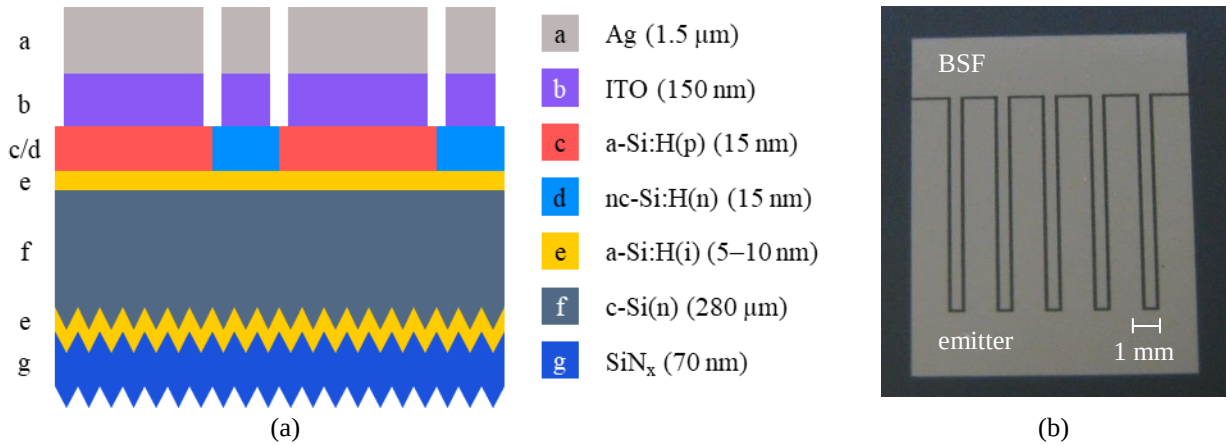

FIGURE 2. (a) Schematic of the solar cell structure presented here (not to scale, front side at the bottom), (b) Image of the rear side of a finished shadow-mask structured solar cell; emitter and BSF regions are marked; active cell area: (1 × 1) cm²

RESULTS AND DISCUSSION

Passivation Quality and Implied Fill Factors

For both PLC and SMC precursors, exceptionally high minority carrier lifetimes (τ) of about 4 ms at a minority carrier density (MCD) of 10^{15} cm^{-3} were obtained, indicating a sufficiently passivated interface. In Fig. 3a, MCD-dependent minority carrier lifetimes are shown for SMC as well as for PLC with comparable results. Minority carrier lifetime data was then used to calculate the implied fill factor (iFF), which can be understood as an upper limit for the FF, assuming an ideal, only recombination limited solar cell with infinite shunt resistance (R_{sh}) and without series resistance (R_s) [19]. Implied j–V characteristics were calculated from that data (cf. Fig. 3b). Again, results for SMC and PLC were comparable, yielding IFFs of 84.4 % for both preparation techniques; showing the high potential of our shadow-mask based process. Since TrPCD measurements display only a mean value over a large investigated area, PL measurements were carried out as well to investigate whether the passivation is spatially homogeneous. Unfortunately, PL images revealed poorly passivated emitter regions as compared to the BSF regions (cf. Fig. 4). This aspect and its impacts will be discussed in more detail in the following section.

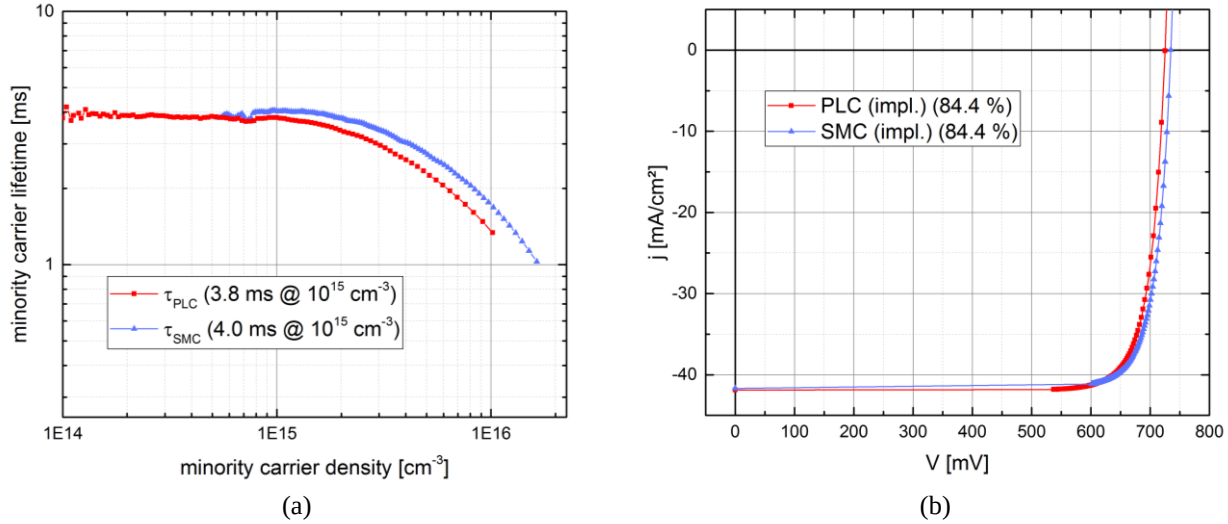

FIGURE 3. (a) Minority carrier lifetime (τ) plotted against minority carrier density, (b) Implied j–V characteristics calculated from lifetime data. Both photolithographically (PLC) and shadow-mask structured solar cells (SMC) show comparable results.

Contact Formation and Contamination Issues

As stated before, SunsVoc measurements were carried out after contact formation to determine pseudo j–V characteristics along with pseudo fill factors (pFF) of the final devices. Here, the illumination intensity is varied, while the solar cells are measured in open-circuit condition, thus neglecting R_s [18]. With the knowledge of the final device's actual j_{sc}, one can calculate the pseudo j–V characteristics. An enormous drop in V_{oc} of about 100 mV as compared to its implied j–V characteristics could be observed for SMC (cf. Fig. 5). From Fig. 4, it is apparent that the emitter regions limit the voltage of the final device. Understanding the reasons for the inferior emitter passivation and developing approaches for its circumvention is subject of current investigations. However, there is an evident assumption close at hand. The shadow masks consist of n-doped material. During the nc-Si:H(n) deposition, this mask is in contact with wafer portions that will subsequently have a-Si:H(p) deposited on them, possibly contaminating them. This can easily be verified by changing the deposition order (firstly p-regions, followed by n-regions) and, if it turns out to be correct, can be circumvented by depositing an a-Si:H(i) protection coating on those sides of the shadow masks that are in direct contact with the wafer surface. This will be examined in a future experiment.

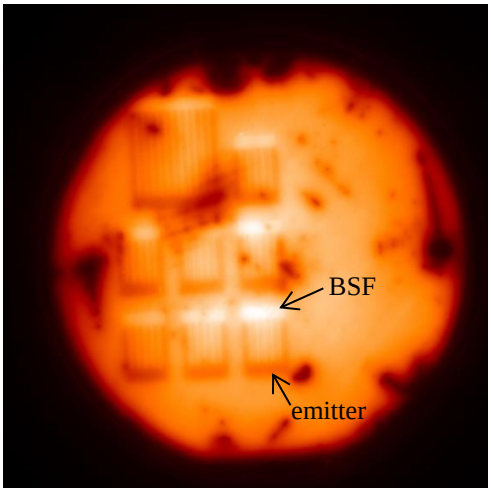

FIGURE 4. PL image of a shadow-mask structured solar cell taken before contact formation. Inferior emitter passivation as compared to the BSF regions is clearly visible.

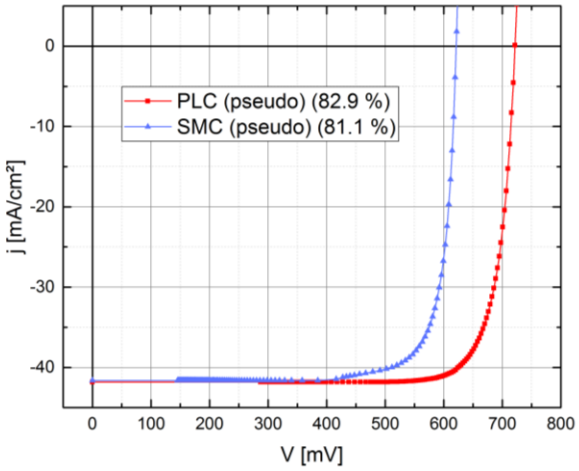

FIGURE 5. Pseudo j–V characteristics determined by SunsVoc measurements. V_{oc} of the shadow-mask structured solar cells (SMC) drops by approximately 100 mV as compared to its implied j–V characteristics, probably due to inferior emitter passivation.

Series Resistance and J–V Characteristics of Final Devices

Values for R_s were determined by two different methods, i. e. by comparing the one-sun j–V characteristics of the final devices with either dark j–V ($R_{s,dark}$) or pseudo j–V characteristics ($R_{s,SunsVoc}$) [20]. For several reasons, the dark j–V method grants more reliable results. Firstly, dark and one-sun j–V characteristics were measured with the same setup within the same session. Secondly, the V_{oc} determined by SunsVoc measurements is usually not identical to that determined by one-sun j–V measurements. Thus, the pseudo j–V graph has got to be corrected manually, which results in a larger uncertainty of the found data as compared to the dark j–V method. SMC show significantly higher R_s values than PLC (cf. Fig. 6 and Tab. 1) due to higher resistive losses in the emitter regions. The FF (and thus R_s) is further limited by the large metallisation gap between emitter and BSF regions (cf. Fig. 2b). This gap was necessary, because whilst the nc-Si:H(n) regions showed a sharp deposition edge, however, the a-Si:H(p) regions did not. They rather exhibit a fading or blurred behaviour, resulting in an overlap area (not shown here). To prevent the metallisation of this overlap area, and thus a low R_{sh}, an unfavourably large metallisation gap had to be applied. This issue will be addressed in a future experiment with a redesigned mask layout, taking the blurring of the emitter regions into account.

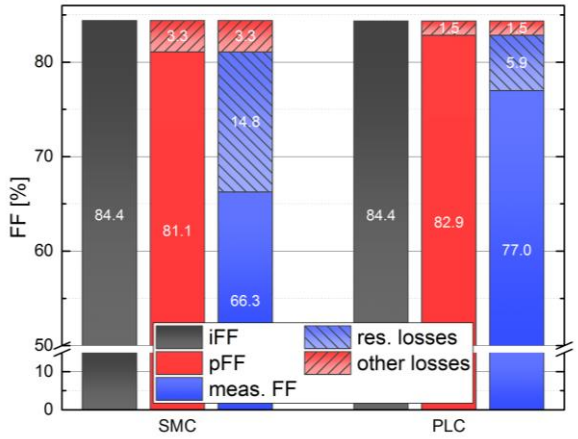

FIGURE 6. Juxtaposition of FF losses for photolithographically (PLC) and shadow-mask structured solar cells (SMC). The latter exhibit significantly higher resistive losses.

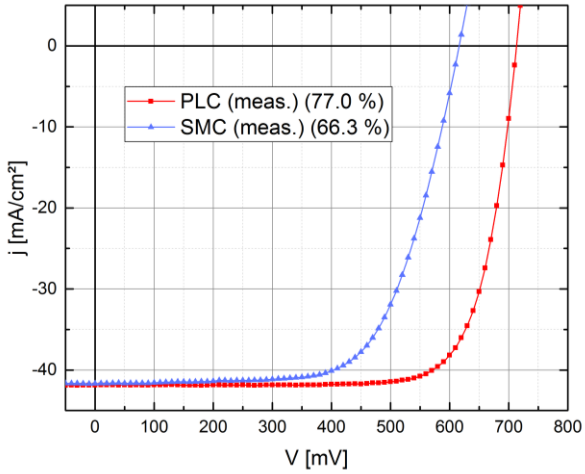

FIGURE 7. Illuminated one-sun j–V characteristics of our best IBC SHJ solar cells (photolithographically, PLC, and shadow-mask structured solar cell, SMC, in comparison).

TABLE 1. Summary of relevant parameters for our best IBC SHJ solar cells presented in this study.

Process	V_{oc} [mV]	j_{sc} [mA/cm²]	iFF [%]	pFF [%]	meas. FF [%]	η [%]	$R_{s,dark}$ [Ωcm²]	$R_{s,SunsVoc}$ [Ωcm²]
SMC	616	41.7	84.4	81.1	66.3	17.0	1.5	2.6
PLC	713	41.9	84.4	82.9	77.0	23.0	0.8	1.1

Figure 7 shows the one-sun j–V characteristics of our best SMC and PLC in comparison. The higher R_s of the SMC is clearly evident as well as the V_{oc} drop discussed above. Apart from that, a lower R_{sh} is likewise evident for SMC, probably due to the fact, that notwithstanding the large metallisation gap, a small portion of the overlap area is still metallised. Relevant parameters for our best IBC SHJ solar cells (SMC and PLC) are summarised in Tab. 1.

CONCLUSIONS

We presented the successful development of a photolithography-free patterning technique for the doped layers of IBC SHJ solar cells using *in-situ* shadow masks during PECVD. First cell results are demonstrated and compared with our best photolithographically structured cells. SMC show similarly high implied FF and minority carrier lifetimes, indicating the high potential of the concept, but still suffer from poorly passivated emitter regions and significantly higher R_s than PLC. As a further issue it was observed that the a-Si:H(p) emitter regions do not form sharp deposition edges, but were rather blurred (not shown here). This could result in a low R_{sh}, due to the possible metallisation of small portions of the overlap area. Approaches for the circumvention of all discussed issues have been outlined and will be carried out in future experiments. Lastly, to achieve a real photolithography-free and thus industrial applicable fabrication of IBC SHJ solar cells, the current metallisation technique will be eventually replaced by a yet to be developed screen-printing process. Notwithstanding the limitations that our shadow mask process currently still faces, it bears the potential to supersede photolithography as an easier and more cost-effective structuring method for highly efficient IBC SHJ solar cells, after overcoming its still apparent drawbacks.

ACKNOWLEDGMENTS

The authors would like to thank (in alphabetical order) K. Jacob, N. Preissler, H. Rhein, M. Wittig, and M. Zelt for assistance provided during processing of the devices presented here. Furthermore, we gratefully acknowledge the financial support by the European Union's Horizon 2020 Programme for research, technological development and demonstration under grant agreement no. 727523 (project NextBase). Philipp Wagner also acknowledges financial support by the HTW Berlin in the framework of the programme HTW Booster.

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