

Thermal conductivity of silicon nanowire forests

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Abstract

A large amount of parallel silicon nanowires, placed perpendicularly to a silicon substrate (silicon nanowire forests), has been contacted and assembled in order to fabricate legs of a thermoelectric generator. This paper reports the measurement of the main parameter for thermoelectric applications, which is the thermal conductivity. The reported value, which confirms the strong reduction of the thermal conductivity in nanostructures, is measured on a large amount ($> 10^7$) of parallel nanowires with a diameter variable in the range 60 - 120 nm, and takes into account eventual non uniformities which are unavoidable on surfaces of several mm^2 . As silicon nanowire forests are very thin, it has been necessary to develop a suitable measurement apparatus. The fabrication of devices based on silicon nanowire forests, the apparatus and the measurement procedure, as well as the the results, are illustrated and discussed.

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1. Introduction

Thermoelectric conversion is very attractive for energy recovery and green energy harvesting. For this reason, several research works are focusing on the development of materials with high electrical conductivity σ and low thermal conductivity k_t which, together with a high value of the Seebeck coefficient S , can exhibit a good figure of merit $ZT = S^2 \frac{\sigma}{k_t} T$. Together with a high figure of merit, which results in a good thermal to electrical conversion efficiency, issues about material availability, sustainability, technological feasibility must be considered. In this respect, the use of silicon for thermoelectric applications would be desirable for its abundance on the Earth's crust and for its worldwide pervasiveness due to the electronic market. Silicon is very good with regard to the Seebeck coefficient and electrical conductivity[1, 2, 3, 4, 5], but in the bulk state its thermal conductivity is very high, greater than 100 W/(m K). Thermal conductivity measurements have been performed on one, or very few, nanowires, and their reduced thermal conductivity, down to very few W/(m K), has been demonstrated[6, 7, 8, 9, 10]. Therefore, Si nanowires (SiNWs) and nanostructures are good candidates for the fabrication of thermoelectric generators with high conversion efficiencies, and based on a sustainable and low-cost material such as silicon.

Techniques for the fabrication of large collections of interconnected silicon nanostructures, and for the assembly of devices completed of contacts for the electrical and thermal conduction, need to be developed. Bottom-up nanowires produced by CVD[11, 12], or top-down nanostructures fabricated by high resolution lithography[13, 14], can be integrated in devices fabricated by standard silicon IC technology for the on-chip power supply of sensors and/or for Internet of Things (IoT) applications. Alternatively, low-cost maskless processes can be used for the fabrication of arrays of silicon nanowires on large areas. Metal Assisted Chemical Etching[15, 16, 17, 18, 19] (MACE) is a vertical, highly selective, etching which allows to fabricate forests of silicon nanowires perpendicular to a silicon substrate. More than 10^7 nanowires/mm², longer than 70 μm , can be

fabricated on both sides of a double polished wafer[5]. The nanowire doping, and hence the electrical conductivity, can be tailored after the fabrication by means of standard diffusion doping processes. A process for contacting the apexes of the silicon nanowires, based on copper electrodeposition, has been improved[20]: thanks to this process, vertical silicon nanowires can be connected in parallel on surfaces of several cm^2 , without using any filling material which would increase the total thermal conductance and limits the maximum operating temperature of the device. Therefore, legs of a thermoelectric module, based on forests of silicon nanowires doped both n^+ and p^+ , can be fabricated and interconnected. Silicon nanowire forests have been already characterized in the past both embedding them in a polymer[21] and using optical techniques[22, 23]. In our work, we characterize devices based on nanowire forests, completed with metal contacts for the electrical and thermal transport, so that they are legs ready to be assembled in a thermoelectric generator. We used a direct technique, imposing a heat flux across the nanowire forest and measuring the generated temperature difference. Unfortunately, conventional equipments for thermal measurements are unsuitable for nanostructures, hence suitable apparatus and techniques[24] need to be developed for their characterization. Even if thermal conductivity of single nanowires has been measured in the past, the development of innovative thermoelectric devices based on a collection of a large number of nanostructures requires suitable techniques for the exact measurement of k_t of the whole collection. This is essential in particular for nanowire forests achieved by MACE etching, made of a large number of nanostructures with a random diameter. The resulted thermal conductivity of the whole forest is an average value which takes into account the dispersion of the diameters and also eventual non-uniformities, which are unavoidable on large surfaces. The main aim of our work is to report the precise measurement of the thermal conductivity of silicon nanowire forest with areas of several mm^2 , and several tens of micrometers tall; the measured thermal conductivity will be reported and discussed. The developed measurement technique allows also to determine the contact thermal resistance, which is a key parameter in the development of thermoelectric generator devices. Af-

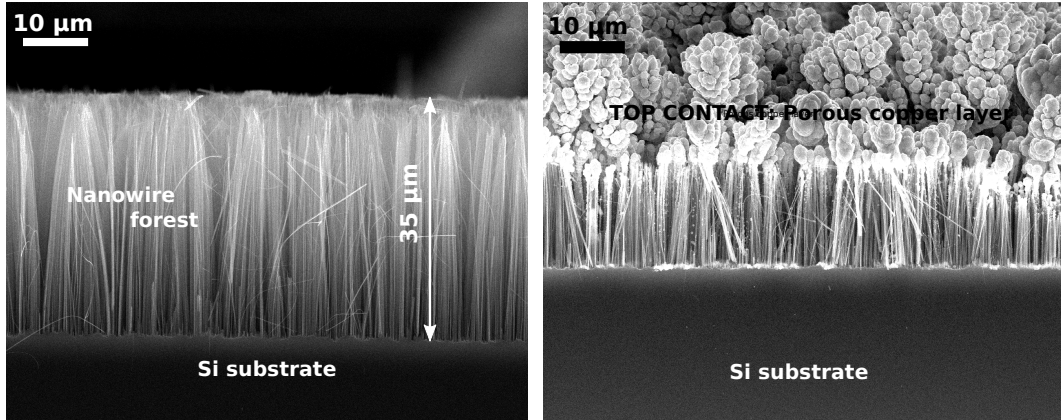


Figure 1: SEM images of silicon nanowire forests (cross sections). Left panel: silicon nanowire forest, after AgNO_3/HF metal assisted etching and cleaning in nitric acid. Right panel: a silicon nanowire forest with the top contacting layer, made of copper grown by seed evaporation and electrodeposition.

ter a resume of the fabrication process of contacted SiNW forests (see section I), we describe the measurement apparatus and technique (see section II). The measurement procedure is suitable also for other kind of very thin materials. In Section III we reports the measurement of the thermal conductivity, discussing the results: the most critical parameter to be determined, and which mostly affect the measurement, is the coverage ratio (or filling factor) of the nanowire forest.

2. Fabrication of contacted silicon nanowire forests

The metal assisted etching is a highly selective etching process that allows the definition of vertical structures (silicon nanowires) with a very high length/diameter aspect ratio. As it is a maskless technique, allowing the low-cost processing of large silicon areas, it can be proposed as a possible via for the large-scale production of forests of nanowires, perpendicular to a silicon substrate, to be used for the fabrication of thermoelectric modules. For the measurement of the thermal conductivity, we fabricated several SiNW forests with the same MACE[16, 19] conditions, apart for the etching time which de-

termines the length of the nanowires. Key conditions for the fabrication of the nanowire forests are the reagent concentrations, the temperature, which must be very stable, and the stirring condition. As a starting material, we used silicon wafers $\langle 100 \rangle$ oriented $525 \mu\text{m}$ thick, single polished, n -doped with a resistivity between $1\text{-}10 \Omega\text{cm}$. Chips of about $10 \times 10 \text{ mm}^2$ have been cleaved from the silicon wafer and cleaned in buffered HF. Nanowire forests have been produced by MACE etching in a solution 5:16:60 in volume of AgNO_3 0.1 N: HF 48%: deionized water. The etch is performed in a bath with a controlled temperature of $18 \text{ }^\circ\text{C}$, $\pm 0.2 \text{ }^\circ\text{C}$. The sample to be etched is mounted on a home-made overhead stirrer, which is rotated at random by an automatic control. The length of the nanowires is more or less proportional to the etching time, so that several nanowire forests with lengths between 6 and $38 \mu\text{m}$ have been produced. After the etching in the MACE solution, the samples resulted covered by silver, which is deposited as a result of the etching process. The deposited silver is completely removed by etching the sample in a solution 1:1 HNO_3 65%: deionized water for 1 min; the complete removal of silver has been confirmed by SEM imaging. As a result of the nitric acid etching, the nanowires are covered by a thin layer of silicon dioxide. The left panel of Figure 1 shows a SEM image of a cross section of a typical sample, obtained with a MACE etching time of 2 h. The length of the nanowires resulted $35 \mu\text{m}$, and the average diameter resulted of about 90 nm .

In order to perform the electrical and thermal characterization, a metal contact on the top of the silicon nanowire forests has been provided by copper electrodeposition, as explained in a previous publication[20]. At first, a metal seed has been deposited on the apexes of the nanowires by thermal evaporation. To this end, the samples have been etched in buffered HF for 1 min to remove the silicon dioxide, and then they have been placed in a thermal evaporator. A thin Cr layer of 20 nm for adhesion, followed by a 60 nm thick copper layer, have been evaporated on top of the nanowire forests, at a residual pressure of about $5 \times 10^{-6} \text{ mb}$. Afterward, on the bottom of the sample, 20 nm of Cr and 60 nm of Cu have been also deposited by thermal evaporation, in order to improve the

electrical and thermal contact. After the metal depositions on the top and on the bottom faces, samples are placed in an electrodeposition cell filled with a solution of copper sulfate and sulfuric acid ($[\text{CuSO}_4]:[\text{H}_2\text{SO}_4]=0.4$)[20]. A current generator has been applied between the sample (negative electrode) and a Cu plate (positive electrode). Copper has been grown, for all the samples, with the same current density of 1415 A/m^2 and the same time (2 min). Therefore, all the measured nanowire forests have a similar copper layer as a top contact. The SEM image on the right panel of Fig. 1 shows a cross section of a silicon nanowire forest after copper electrodeposition. The porous copper layer is visible on the top of the nanowires, which are anchored to the silicon substrate at the other end (at the bottom). The copper layer is about $5 \mu\text{m}$ thick and, even if it is very porous, its electrical resistivity resulted of about $10^{-5} \Omega\text{cm}$, and it is very low with respect to that of silicon.

It must be noted that the procedure for contacting the top of the nanowire forest does not require any filling polymer[25, 26] deposited between the nanowires. Therefore, at first the thermal conductivity of the nanowire forest is due only to the nanowires itself as there is not any parasitic parallel conduction of heat which would be unavoidable with the presence of a polymer. Furthermore, a polymer could upper bound the maximum operating temperature of the final device. It must be mentioned that silicon is a very stable and robust material which can withstand temperatures of several hundred of degrees, so that thermoelectric generators based on pure silicon could exploit very large temperature differences, for very high efficiencies.

3. Measurement apparatus and procedure

The thermal conductivity k_t of a material can be determined by measuring the thermal resistance $\mathfrak{R} = 1/k_t L/S$ of a piece of that material, which is related with the thermal conductivity through the geometrical parameters L and cross section surface $S = W_1 \times W_2$. In principle, the thermal resistance \mathfrak{R} can be measured imposing a known heat flux Q through the sample and measuring the temperature drop $T_{Hot} - T_{Cold} = T_H - T_C$ between its ends: $\mathfrak{R} = (T_H - T_C)/Q$.

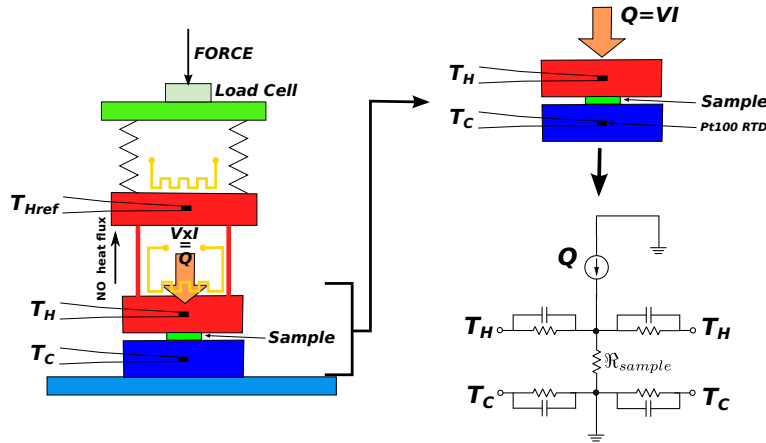


Figure 2: Sketch of the measurement apparatus, based on the guarded hot-plate concept. An overall vision of the machine is shown on the left: it includes the force, the load cell, the plate maintained at $T_{Href} = T_H$, the top plate where it is measured the temperature T_H , the sample, which is roughly 0.5 mm thick, and the bottom plate, where it is measured the temperature T_C . A sketch of the thermal circuit is shown on the right. The circuit is represented with its electrical equivalent lump parameters. The thermal resistance of the sample under measurement is \mathfrak{R}_{sample} .

Figure 2 shows a sketch of our measurement apparatus, based on the concept of the guarded hot plate technique. Samples to be measured are small chips of silicon about 0.5 mm thick, and with $S = W_1 \times W_2$ of the order of (smaller than) $5 \times 5 \text{ mm}^2$. The sample is squeezed between two blocks (plates) of aluminum $30 \times 30 \times 10 \text{ mm}^3$. The top aluminum block is maintained to a temperature T_H by an electrical (Joule) heater, which is supplied with an electrical power $P_H = V \times I$ (V and I are, respectively, the supplied voltage and current). The two blocks will be named H (Hot) and C (Cold). Their temperatures T_H and T_C are measured by means of RTD (class A Pt100) temperature sensors, applied on the lateral surfaces of the blocks, as shown in the right sketch of Fig. 2. Even if two terminal Pt100 sensors have been used, particular care has been taken for making the sensor electrical connections and cables as similar as possible (electrical cables with the same length). Therefore, their parasitic contribution to the measurement of the electrical resistance, and hence on the measured temperature, disappears in the difference $T_H - T_C$. A third aluminum block, called H_{ref} , is placed over the H block and maintained in place by 4 stainless steel

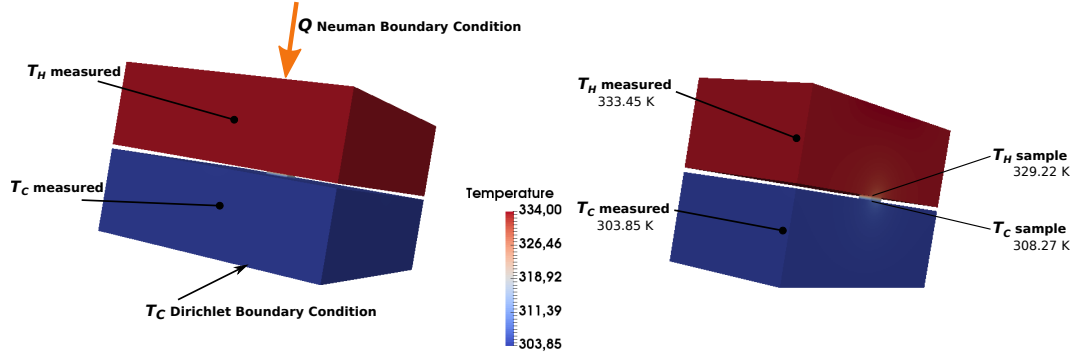


Figure 3: Numerical solution of the heat transport equation in the two main plates of the measurement system. The thermal power, equal to the electrical power $V \times I$ supplied to the heater, is used as Neumann boundary condition in the region where the heater is applied. The bottom face is maintained at T_C (Dirichlet Boundary Condition). On the right: the Finite-Element Solution allows to determine the temperature drop across the sample.

screws, whose total thermal resistance can be estimated of $\mathfrak{R} = 53 \text{ K/W}$ (assuming a stainless steel thermal conductivity of 20 W/mK). A second Joule heater is applied to this block and the applied power $P_{Href} = V \times I$ is electronically controlled in such a way that T_{Href} remains within $0.5 \text{ }^\circ\text{C}$ with respect to T_H . Therefore, the thermal power exchanged between the H and the H_{ref} blocks can be estimated to be smaller than 10 mW . Moreover, an aluminum radiation shield, maintained at the same temperature $T_{H_{ref}} \simeq T_H$, surrounds the H block, in order to minimize the radiation losses. Furthermore, all the system operates in vacuum (residual pressure of about $1.3 \times 10^{-4} \text{ atm}$), so that losses due to the air thermal conductivity and convection are minimal[27][28]. Hence, most of the electrical power $P_H = V \times I$, supplied to the heater applied to the H block, is the thermal power passing through the sample under measurement.

Given the heat power Q through the sample, the thermal resistance of the sample \mathfrak{R} can be determined knowing the temperature difference between its extremities. However, it is impossible to make a precise measurement of this temperature difference, because the sample must be tightly clamped between

the H and the C aluminum blocks, to minimize the thermal contact resistance and to allow the heat flux. It is very difficult to apply temperature sensors exactly at the ends (top surface and bottom surface) of the sample. Hence, we have implemented the following technique. The sensors for the measured of T_H and T_C are placed on the lateral surfaces of the H and C block, respectively, and they are different from the temperatures $T_{Hsample}$ and $T_{Csample}$ at the top and at the bottom of the sample. The sketch on the right of Fig. 2 shows the electrically equivalent circuit, in lump parameters, of the thermal system made of the heat generator (electrically equivalent to a current generator), the thermal resistances and capacitances of the H and C blocks and the unknown thermal resistance \mathfrak{R} of the sample. The temperature of the two blocks is not uniform, in particular in the regions closer to the sample, where the heat flux is concentrated. However, the two H and C blocks are intentionally made larger ($W = 30$ mm) than the sample to be measured, which usually is smaller than 5 mm (both W_1 and W_2 are less than 5 mm). Hence, the lateral surfaces are far away from the zone where the heat flux is concentrated, and therefore, assuming that the walls of the blocks are adiabatic, their temperature in steady state is uniform. As the temperature sensors for the measurement of T_H and T_C are placed on the lateral surface the measurement of the two temperatures is very accurate. Consequently, the results of the measurement are $Q = V \times I$, T_H and T_C . From these data, the thermal resistance of the sample \mathfrak{R} can be determined. To this end, we implemented a numerical solution of the heat transport equation:

$$\Phi = -k_t \nabla T \quad (1)$$

in the system made of the sample and of the two H and C aluminum blocks. In this equation, $\Phi = Q/S$ is the heat exchanged for surface unit (heat flux); k_t is the thermal conductivity, which is known in the two blocks (it is that of aluminum); in the sample, k_t is the unknown to be determined. The solution of the heat transport equation has been implemented with a Python code, based on the Finite Element (FE) Fenics package[29, 30]. As an example, a typical result of FE simulation for given values of \mathfrak{R} , Q , T_C and T_H is shown in the Figure 3.

The generated heat Q has been used as a Neumann boundary condition on the top of the block H , where the Joule heater (power resistor) is applied. The cold temperature T_C has been used as a Dirichlet boundary condition imposed on the bottom face of the block C . From the right sketch of Fig. 3 it is possible to see that, as anticipated, the temperatures T_H and T_C are very uniform on the lateral surfaces of the H and C blocks. This confirms that the measurement of these temperatures is very precise, and it does not depend on the position, on the lateral face, where the temperature sensors Pt100 are applied. In the right sketch of Fig. 3 a cross-section of the FE simulation result is shown. This cross-section, taken in the middle of the blocks and of the sample, shows that the temperature is not uniform at the top and at the bottom of the sample: the indicated $T_{Hsample}$ and $T_{Csample}$ are extracted from the center of the top and bottom surfaces. This concept is better shown in Figure 4, where the two graphs report both the temperature in x direction in the H block, just above the sample, and the temperature in z direction on the lateral surfaces of the H and C blocks. The temperature at the top surface of the sample is not uniform. The temperature on the lateral surfaces of the blocks is instead very uniform, hence its measurement does not depend on the position of the RTD. As the temperature drop depends on the position on the sample, it is not straightforward to determine the thermal resistance \mathfrak{R} as simply the ratio between Q and the temperature drop. Hence, we developed a Python code that, given the measured values Q , T_H and T_C , solves iteratively the heat transport equation. Imposing Q and T_C , the code looks for the thermal resistance \mathfrak{R} which gives the measured temperature T_H . Therefore \mathfrak{R} is the closest value to the thermal resistance of the sample under measurement.

4. Measurement of the thermal conductivity of silicon nanowire forests

A typical sample to be measured is made of a silicon chip 0.5 mm thick, and with a surface of few mm². The nanowire forest is perpendicular to the substrate and it has a length L of several tens of micrometers. The contacting copper layer is on the top, as seen in Fig. 1. The measured thermal resistance,

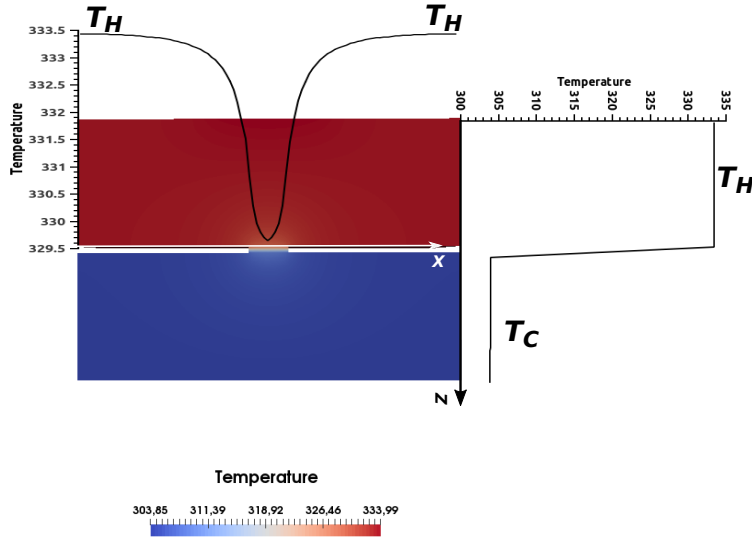


Figure 4: Temperature on the top surface of the sample, and on the sides of the two H and C blocks. The lateral surfaces of the H and C blocks have a very uniform T_H and T_C temperatures respectively.

achieved as described in Sec. III, is the series of the thermal resistance of the nanowire forest \mathfrak{R}_{NW} , the thermal resistance of the substrate, and the contact thermal resistances of the bottom and of the top faces, where there is the copper layer contacting the nanowire apices. As the contact thermal resistance is unknown, we measured several nanowire forests with different length L . To this end, we fabricated several samples with the same MACE conditions (the same etching solution 5:16:60 AgNO_3 0.1N: HF 40%: H_2O , see Sec. II), but with different etching time, which resulted in nanowire forests with different lengths L . After etching, the top copper layer has been grown on all the samples with the same electrodeposition conditions (see Sec. II). As the etching and the electrodeposition parameters are the same, apart for the etching time which determines L , we can assume that the contact thermal resistance is the same for all the measured nanowire forests. Comparing the thermal resistance \mathfrak{R} of samples with nanowires of different lengths, taking into account the geometrical

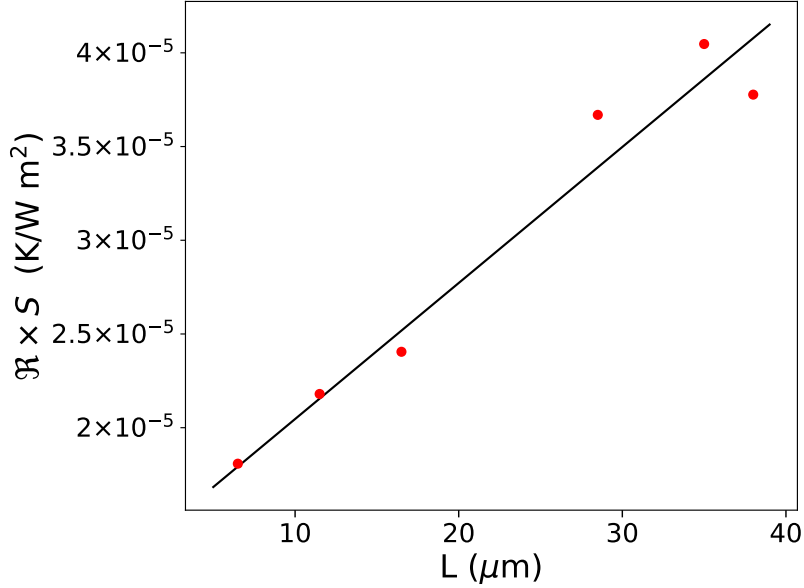


Figure 5: The measured thermal resistance, multiplied by the sample surface $\mathfrak{R} \times S$, is reported as a function of the length L of the silicon nanowire forest. Red dots: experimental measurements. Straight line: least square fitting.

parameters (surface and length), we can derive the thermal conductivity of the nanowire forest k_t , as also the contact thermal resistance for surface unit. After MACE etching and copper electrodeposition, samples have been cleaved in square, or rectangular, chips. This cleaving operation is not very precise, so samples have a similar, but slightly different, surface, between $S = W_1 \times W_2 = 2 \times 2 \text{ mm}^2$ and $S = W_1 \times W_2 = 4 \times 4 \text{ mm}^2$. W_1 and W_2 , and hence the total surface S of each sample, have been precisely measured by means of a calibrated optical microscope. For each sample, the length L of the nanowire forest has been measured by means of SEM cross-section imaging. We assumed that the total thickness of the sample is that of the original wafer, which is $525 \pm 5 \mu\text{m}$. The contact thermal resistance depends also on the compressive force for surface unit (pressure) applied to the sample during the thermal conductivity measurement. Therefore, all the measured samples have been loaded by a force corresponding to a pressure of 20 MPa, accordingly with the surface S . To this

end, we exploited the load cell provided for the measurement of the applied force (see the sketch of Fig. 2). Nanowires are electrically and thermally in parallel, so that the total thermal resistance of the nanowires can be determined knowing their length L and the total sum of their cross-sections. This total surface of the nanowire forest is only a fraction ν of that of the sample: $S_{NW} = \nu S$. We named ν the filling factor of the nanowire forest. The thermal resistance of the nanowire forest can be written as:

$$\mathfrak{R}_{NW} = \frac{1}{k_t} \frac{L}{\nu S} \quad (2)$$

and the measured thermal resistance \mathfrak{R} is:

$$\mathfrak{R} = \mathfrak{R}_C + \mathfrak{R}_{NW} = \mathfrak{R}_C + \frac{1}{k_t} \frac{L}{\nu S} \quad (3)$$

where \mathfrak{R}_C includes the contact thermal resistance and the thermal resistance of the substrate. The thermal resistance multiplied by the surface is:

$$\mathfrak{R} S = \mathfrak{R}_C S + \frac{1}{\nu k_t} L \quad (4)$$

Therefore, a linear fitting of the plot of $\mathfrak{R} S$ as a function of L allows to determine νk_t . Moreover, the linear fit allows to determine also $\mathfrak{R}_C S$, whose reciprocal $K_C = 1/\mathfrak{R}_C S$ is mainly due to the contact thermal conductance for surface unit. Figure 5 shows the measured values $\mathfrak{R} S$, as a function of the nanowire forest height, i.e. the nanowire length L . The measured values are almost on a straight line and this implies that the thermal conductivity does not depend on the nanowire length. The linear least square fitting is also shown in the figure. From the fitting, the best value of νk_t resulted of 1.38 W/(m K). From the fitting, it results also $K_C = 75.7 \times 10^4$ W/(K m²). This value is mainly due to the contact thermal conductance between the copper layer and the top aluminum block H . The filling factor ν , which is necessary in order to determine the value of k_t , is very difficult to be measured. For an estimation of ν , at first we have taken several SEM images of the surfaces of the nanowire forests (top vision), before growing the copper layer. A typical SEM top vision of the surface of a nanowire forest is shown on the left panel of Figure 6. The apexes

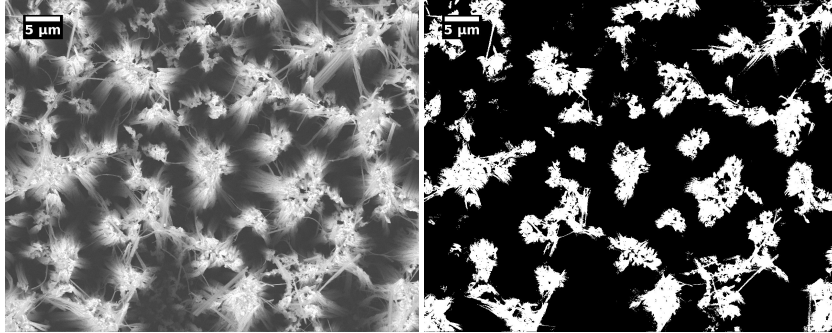


Figure 6: Left panel: SEM photo of the surface of a typical sample (4h of etch in 5:16:60 AgNO₃:HF:H₂O solution). The length of the nanowires (which are perpendicular to the SEM image) resulted of $L = 38 \mu\text{m}$, as measured from cross-section SEM images of the sample (not shown). Right panel: image reduction for a rough estimation of the filling factor ν .

of the nanowires appear to be grouped in bunches. It must be noted that the average distance of these bunches is about $5 \mu\text{m}$, meanwhile the nanowire length, measured on cross section SEM images of this sample, resulted $L = 38 \mu\text{m}$. Therefore, we can affirm that the bending of the nanowires is very small, because nanowires are bended in average of about $2.5 \mu\text{m}$ on a length of $38 \mu\text{m}$. A rough estimation of the filling factor ν can be obtained by analyzing the image, as shown in the right panel of Fig. 6 where a color threshold has been settled in order to visualize only the apices of the nanowires which are brighter than the remaining part of the nanowires. The brighter area is about the sum of the cross section surfaces of all the nanowires included in the image. Therefore, the ratio between the brighter area and the total surface of the image can be taken as an estimation of the filling factor of the nanowire forest. We repeated this procedures for all the samples. For each sample, at least 10 top vision images have been taken in random positions on the surface. Averaging on all the images, we can assume 0.3 as a reasonable value for ν . Therefore, k_t results of about $4.6 \text{ W}/(\text{m K})$. We underline that, meanwhile the measured value $k_t\nu = 1.38 \text{ W}/(\text{m K})$ is quite reliable, the final value of $k_t = 4.6 \text{ W}/(\text{m K})$ is affected by the rough estimation of the filling factor ν .

5. Conclusions

We measured the thermal conductivity of silicon nanowire forests, made of a large amount of parallel silicon nanowires placed perpendicular to a silicon substrate. The measured value is comparable to that previously achieved by several groups with devices based on a single, or on very few, silicon nanostructures[31, 32, 8, 33]. In these works, it is shown that the thermal conductivity of nanowires is strongly reduced with respect to that of bulk silicon, and this is ascribed to the reduction of phonon propagation due to the scattering on the nanowire walls. As expected, the thermal conductivity of silicon nanowire forests, made of a large collection of parallel nanostructures, follows the same trend. Our work confirms the potentialities of nanostructuring for the reduction of the thermal conductivity, which is one of the fundamental parameters to be considered for high efficient thermoelectric conversion. The MACE technique used for the fabrication of our devices, which can be used as legs of a thermoelectric generator, is simple and low-cost, and it can be applied to areas of several cm^2 , hence it can be proposed for large scale production. However, the technique gives nanowires with a non uniform diameter, whose average value is about 90 nm, but with a very large variability. Therefore, the thermal conductivity value achieved with our work is very important, because it is averaged on a large amount of long nanowires with random diameters, and on surfaces of several mm^2 where non-uniformities can be present.

Since samples are very thin (nanowires of several tens of micrometers, total thickness 0.5 mm), we developed a suitable measurement apparatus based on the guarded hot plate concept. A suitable technique for data reduction, based on finite element modeling, has been developed for a better interpretation of experimental measurements. Even if in our work we measured the thermal conductivity of silicon nanowire forests, the developed technique is very general and it can be usefully applied to the measurement of thin films and other low thickness materials.

- [1] T. H. Geballe, G. W. Hull, Seebeck effect in silicon, Phys. Rev. 98 (4)

(1955) 940.

- [2] M. E. Brinson, W. Dunstant, Thermal conductivity and thermoelectric power of heavily doped n-type silicon, *Journal of Physics C: Solid State Physics* 3 (3) (1970) 483.
URL <http://stacks.iop.org/0022-3719/3/i=3/a=001>
- [3] A. Stranz, J. Kahler, A. Waag, E. Peiner, Thermoelectric properties of high-doped silicon from room temperature to 900 k, *J. Electron. Mater.* 42 (7) (2013) 2381. doi:10.1007/s11664-013-2508-0.
- [4] N. S. Bennett, Thermoelectric performance in n-type bulk silicon: The influence of dopant concentration and dopant species, *physica status solidi (a)* 214 (7) (2017) 1700307–n/a, 1700307. doi:10.1002/pssa.201700307.
URL <http://dx.doi.org/10.1002/pssa.201700307>
- [5] E. Dimaggio, G. Pennelli, Potentialities of silicon nanowire forests for thermoelectric generation, *Nanotechnology* 29 (2018) 135401.
- [6] N. Melosh, A. Boukay, F. Diana, B. Gerardot, A. Badolato, P. Petroff, J. Heath, Ultrahigh-density nanowires lattices and circuits, *Science* 300 (2003) 112–115.
- [7] A. Boukay, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard III, J. R. Heat, Silicon nanowires as efficient thermoelectric materials, *Nature Letters* 451 (2008) 168–171.
- [8] J. Lim, K. Hippalgaonkar, S. Andrews, C., A. Majumdar, P. Yang, Quantifying surface roughness effects on phonon transport in silicon nanowires, *Nano Letters* 12 (5) (2012) 2475–2482.
- [9] J. Feser, J. Sadhu, B. Azeredo, H. Hsu, J. Ma, J. Kim, M. Seong, N. Fang, X. Li, P. Ferreira, S. Sinha, D. Cahill, Thermal conductivity of silicon nanowire arrays with controlled roughness, *J. Appl. Phys.* 112 (2012) 114306.

- [10] G. Pennelli, A. Nannini, M. Macucci, Indirect measurement of thermal conductivity in silicon nanowires, *J. Appl. Phys.* 115 (2014) 084507.
- [11] D. Davila, A. Tarancon, M. Fernandez-regulez, C. Calaza, M. Salleras, A. SanPaulo, L. Fonseca, Silicon nanowire arrays as thermoelectric material for a power microgenerator, *Journal of Micromechanics and Microengineering* 21 (2011) 104007.
- [12] D. Davila, A. Tarancon, C. Calaza, M. Salleras, M. Fernandez-Regulez, A. SanPaulo, L. Fonseca, Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices, *Nano Energy* 1 (2012) 812.
- [13] G. Pennelli, M. Totaro, M. Piotto, P. Bruschi, Seebeck coefficient of nanowires interconnected into large area networks, *Nano Lett.* 13 (2013) 2592.
- [14] G. Pennelli, M. Macucci, High-power thermoelectric generators based on nanostructured silicon, *Semicond. Sci. Technol.* 31 (2016) 054001. doi: 10.1088/0268-1242/31/5/054001.
- [15] W. Bohn, X. Li, Metal-assisted chemical etching in hf/h₂o₂ produces porous silicon, *Appl. Phys. Lett.* 77 (16) (2000) 2572.
- [16] Z. Huang, N. Geyer, P. Werner, J. de Boor, U. Gosele, Metal-assisted chemical etching of silicon: a review, *Advanced Materials* 23 (2011) 285.
- [17] J. Kim, H. Han, Y. Kim, S.-H. Choi, J.-C. Kim, W. Lee, Au/ag bilayered metal mesh as a si etching catalyst for controlled fabrication of si nanowires, *ACS nano* 5 (4) (2011) 3222.
- [18] M.-L. Zhang, K.-Q. Peng, X. Fan, J.-S. Jie, R.-Q. Zhang, S.-T. Lee, N.-B. Wong, Preparation of large-area uniform silicon nanowires arrays through metal-assisted chemical etching, *The Journal of Physical Chemistry C* 112 (12) (2008) 4444–4450.

- [19] W. To, C. Tsang, H. Li, Z. Huang, Fabrication of n-type mesoporous silicon nanowires by one-step etching, *Nano Letters* 11 (2011) 5252–5258.
- [20] E. Dimaggio, G. Pennelli, Reliable fabrication of metal contacts on silicon nanowire forests, *Nano Letters* 7 (2016) 4348. doi:10.1021/acs.nanolett.6b01440.
- [21] J. Weisse, A. Marconnet, D. Kim, P. Rao, M. Panzer, K. Goodson, X. Zheng, Thermal conductivity in porous silicon nanowire arrays, *Nanoscale Research Letters* 7 (2012) 554.
- [22] T. Zhang, S. Wu, R. Zheng, G. Cheng, Significant reduction of thermal conductivity in silicon nanowire arrays, *Nanotechnology* 24 (2013) 505718.
- [23] T. Chen, P. Yu, R. Chou, C. Pan, Phonon thermal conductivity suppression of bulk silicon nanowire composites for efficient thermoelectric conversion, *Optics Express* 18 (2010) A468.
- [24] G. Pennelli, E. Dimaggio, M. Macucci, Improvement of the 3ω thermal conductivity measurement technique for its application at the nanoscale, *Rev. of Scient. Instrum.* 89 (2018) 016104.
- [25] Y. Li, K. Buddharaju, B. Tinh, N. Singh, S. J. Lee, Improved vertical silicon nanowire based thermoelectric power generator with polyimide filling, *IEEE Electron Device Letters* 33 (5) (2012) 715.
- [26] J. Sadhu, H. Tian, J. Ma, B. Azeredo, J. Kim, K. Balasundaram, C. Zhang, X. Li, P. Ferreira, S. Sinha, Quenched phonon drag in silicon nanowires reveals significant effect in the bulk at room temperature, *Nano Letters* 15 (2015) 3159.
- [27] M. Saidi, R. Abardeh, Air pressure dependence of natural-convection heat transfer, *Proceedings of the World Congress on Engineering, WCE 2010*, June 30 - July 2, 2010, London, U.K. II.

- [28] H. Wu, S. Grabarnik, A. Emadi, G. De Graaf, R. Wolffenbuttel, Characterization of thermal cross-talk in a mems-based thermopile detector array, *J. Micromech. Microeng.* 19 (2009) 074022 (7pp) 19 (2009) 074022. doi:10.1088/0960-1317/19/7/074022.
- [29] A. Logg, K. Mardal, G. Wells, *Automated Solution of Differential Equations by the Finite Element Method*, Springer Link, 2012. doi:doi:10.1007/978-3-642-23099-8.
- [30] A. Logg, G. Wells, *Dolfin: automated finite element computing*, *ACM Transactions on Mathematical Software* 37 (2) (2010) 20. doi:doi.acm.org/10.1145/1731022.1731030.
- [31] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, A. Majumdar, Thermal conductivity of individual silicon nanowires, *Appl. Phys. Lett.* 83 (14) (2003) 2934–2936.
- [32] E. Dimaggio, G. Pennelli, , M. Macucci, Thermal conductivity reduction in rough silicon nanomembranes, *IEEE Transaction on Nanotechnologies* 17 (2018) 500.
URL DOI10.1109/TNANO.2018.2816119
- [33] Y. Zhao, L. Yang, L. Kong, M. Nai, D. Liu, J. Wu, Y. Liu, S. Chiam, W. Chim, C. Lim, B. Li, J. Thong, K. Hippalgaonkar, Ultralow thermal conductivity of single-crystalline porous silicon nanowires, *Advanced Functional Materials* 17 (2017) 1702824. doi:10.1002/adfm.201702824.