PLANAR NANOELECTRONIC DEVICES AND BIOSENSORS USING TWO-DIMENSIONAL NANOMATERIALS

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In the Name of Allah the Most Gracious, the Most Merciful

“And my guidance cannot come except from Allah, in Him I trust and to Him I repent”

Translation of the meaning of the Noble Quran [Surat Hud – Chapter 11, Verse 88]

ABSTRACT

Graphene, a monolayer of carbon atoms and the first two-dimensional (2D) material to be isolated, has sparked great excitement and vast opportunities in the global research community. Its isolation led to the discovery of a new family of materials that are completely 2D, each of which exhibits unique properties in its own right. Such a wide range of new nanomaterials in a completely unexplored 2D platform offers a potential treasure for the electronics industry, which is yet to be explored. However, after more than a decade of research, nanoelectronic devices based on 2D nanomaterials have not yet met the high expectations set for them by the electronics industry. This thesis hopes to drive these efforts forward by proposing a different approach for the conceptualization of nanoelectronic devices, in light of the new opportunities offered by 2D nanomaterials.

The proposed approach is centred on exploiting the truly unique property of two-dimensionality, which defines and distinguishes this exciting family of 2D nanomaterials, for the realization of completely 2D planar nanoelectronic devices. Less reliance is made on individual properties that are unique to individual 2D nanomaterials, however, wherever possible; such properties are exploited in enhancing the performance of the proposed devices. The proposed approach is applied to the conceptualization of a number of planar nanoelectronic devices that have a potential in a range of direct as well as long term envisioned applications, complementing conventional electronics on the short term but also having the potential to revolutionize electronics on the long term.

All of the proposed devices are planar, completely 2D and realizable within a single 2D monolayer, reducing the required number of processing steps and enabling extreme miniaturization and CMOS compatibility. For the first time, a 2D Graphene Self-Switching Diode (G-SSD) is proposed and investigated, showing promising potential as a nanoscale rectifier. By exploiting some of graphene's unique properties, the G-SSD is transformed into different types of planar devices that can achieve rectification, Negative Differential Resistance (NDR) operation and tunable biosensing. The extension of the proposed approach to other types of 2D nanomaterials is also investigated, by exploring the implementation of SSDs using MoS_2 and Silicene. Finally, new classes of graphene resonant tunneling diodes (RTDs), with completely 2D planar architectures, are proposed, showing unique transport properties and with promising performance, while requiring minimal process steps during fabrication.

DECLARATION

This is to certify that:

i. the thesis comprises only my original work towards the PhD except where indicated in the Preface,

ii. due acknowledgement has been made in the text to all other material used,

iii. the thesis is fewer than 100 000 words in length, exclusive of tables, maps, bibliographies and appendices.

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Feras Mohamad Ameer Al-Dirini, December 2015

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LIST OF ABBREVIATIONS AND ACRONYMS

2D	Two-Dimensional
2DEG	Two-Dimensional Electron Gas
3D	Three-Dimensional
ATK	Atomistix Toolkit
ab initio	From First Principles (Latin)
aGNR	Armchair Graphene Nanoribbon
CMOS	Complementary Metal-Oxide-Semiconductor
COO^-	Negatively Charged Carboxyl Group
CVD	Chemical Vapour Deposition
DB-RTD	Double-Barrier Resonant Tunnelling Diode
DDOS	Device Density of States
DFT	Density Functional Theory
DNA	Deoxyribonucleic Acid
EH	Extended Huckel
FET	Field Effect Transistor
GGA	Generalized Gradient Approximation
GHz	Gigahertz
GNR	Graphene Nanoribbon
G-SSD	Graphene Self-Switching Diode
G-SS MISFED	Graphene Self-Switching MISFED*
hBN	Hexagonal Boron Nitride
IC	Integrated Circuit
IV	Current-Voltage
MIS	Metal-Insulator-Semiconductor
***MISFED**	Metal-Insulator-Semiconductor Field-Effect Diode

MISFET	Metal-Insulator-Semiconductor Field-Effect Transistor
MoS_2	Molybdenum Disulphide
NDR	Negative Differential Resistance
NEGF	Non-Equilibrium Green's Function
NH_3^+	Positively Charged Amine Group
PBE	Perdew-Burke-Ernzerhof
PCD	Peak Current Density
PVCR	Peak-to-Valley Current Ratio
QDot	Quantum Dot
RF	Radio Frequency
RTD	Resonant Tunnelling Diode
SE	Semi-Empirical
SiO_2	Silicon Dioxide
SoC	System-on-Chip
SSD	Self-Switching Diode
TB	Tight Binding
WS_2	Tungsten (IV) Disulphide
zGNR	Zigzag Graphene Nanoribbon

1 INTRODUCTION

In this thesis a number of novel nanoelectronic devices are conceptualized and studied theoretically using rigorous quantum mechanical simulations. While being devices with a diverse range of functionalities, addressing a variant range of applications, all the proposed devices are products of a new approach to the conceptualization of electronic devices that this thesis proposes and advocates. This approach is based on using the recently discovered family of two-dimensional nanomaterials for the realization of electronic devices, through exploiting their unique property of two-dimensionality, in order to realize completely two-dimensional planar devices. This chapter gives a background to and highlights the motivation behind the work presented in this thesis, and sets the guidelines for the proposed approach, which is applied later on for the conceptualization of a range of nanoelectronic devices that are presented in subsequent chapters. A number of research objectives are set and defined and an overview of the thesis is presented. The theoretical methods used for studying and investigating the conceptualized devices are also outlined. Finally, a summary of the main contributions along with a list of derived publications from this thesis are presented.

1.1 Background

Carbon has been central to human life over the past century, whether it be through fossil fuels that fuel technology and life, or even through carbon emissions that threaten the atmosphere and lives of many living species, to the extent that some argue we may be stepping into a so-called “Carbon Age”. However, while technology has truly revolutionized life on earth within that same period of time, carbon’s contribution to it has mainly been towards providing the source of energy that drives technology, without taking an integral role within its infrastructure. With electronics being at heart of modern day ‘smart’ technology, if carbon was to ever dominate human life significantly enough for the carbon age to come into existence, it has to either find its throne within the world of electronics or look for an alternative.

The dominance of silicon within the electronics industry has kept many other materials on the bench or restricted their dominance to niche applications, even-though many of them have proven their competence through a number of superior attributes, including germanium and gallium arsenide. No other material has provided a superior comprehensive-enough package that would convince leading electronics manufacturers to invest in a new infrastructure, leaving behind their backs or at least having to refurbish their multi-billion dollar silicon-tailored investments. Nevertheless, carbon had been out of the picture for so long not because it has proven to be incompetent, but mainly because it had not attempted to play the game.

It wasn’t until the break of the year 1990, when carbon made its first debut in the form of fullerenes [1] followed by another more serious attempt in the form of carbon nanotubes [2], bringing about a lot of excitement to the global electronics community. However, soon enough, that excitement greatly cooled off mainly due to the difficulty of synthesizing these types of carbon allotropes.

Recently, carbon came back with much better shape, this time completely two-dimensional, making its most serious debut not only through a new allotrope, but more interestingly through the first two-dimensional material to ever be isolated; graphene[3]. The method with which graphene was isolated completely addressed the main problem its sister allotropes had faced, being a simple process that only requires ‘scotch tape’[3]. This involved peeling off a thin layer of a graphite block using scotch tape and then repeating the process on the peeled-off strip, until a single monolayer of carbon atoms is peeled off. This monolayer of carbon atoms became known as graphene. The scotch

tape method for peeling off graphene became later known as exfoliation and led to the isolation of a family of other two-dimensional materials [4], each having its own unique exceptional properties.

While two-dimensionality was the most unique of graphene's features at the time [3], the other extraordinary attributes that it exhibited overshadowed this fact. These included very high thermal conductivity, ultra high mechanical strength, and high flexibility [5]. However, the single attribute which captured the excitement of the electronics community was graphene's ultra-high charge carrier mobility [3], outperforming silicon in one of its weakest properties by orders of magnitude. Enabled by this property, very promising results were achieved by a number of efforts employing graphene for the realization of field effect transistors [6-9], the very same architecture that brought silicon into electronics dominance, creating for it its CMOS Empire which dominated the digital world and more recently began its invasion into the analog.

This promising start was strong enough for it to trigger serious attempts at realizing mass producible graphene integrated circuits [10], and only then did the great hype and excitement amongst the electronics community make a very sharp turn into realism very similar to the one this thesis is just about to make.

Graphene can be synthesized using the experimental exfoliation technique [3], however this technique produces patches of graphene that may only be up to millimeters in length. Graphene synthesized using this method is of high quality and exhibits exceptional properties, however, this is not the case with graphene synthesized using wafer-scale production methods, in which many of graphene's properties, including its charge carrier mobility, is not as exceptional [11].

Wafer scale production techniques include sublimation on silicon carbide wafers [12, 13] or chemical vapor deposition on metallic substrates [14, 15], which act as catalysts for graphene formation. The latter is a promising method, but requires subsequent transfer processes and gives rise to graphene monolayers with grain boundaries, disturbing its uniform crystalinity and hence some of its properties [11]. Vast efforts are currently underway in pursuit of achieving high quality wafer-scale graphene synthesis[11], which stands as one of the most important milestones towards graphene commercialization. Amongst many, a promising method is growth using CVD on other two dimensional materials such as hexagonal boron nitride (hBN) [16, 17], which

exhibits a similar hexagonal structure to graphene. It is important to note that different synthesis methods yield graphene with varying properties; however, all methods give rise to a completely two-dimensional monolayer of carbon atoms. This two-dimensionality remains to be the unique property that defines graphene.

Apart from synthesis, a major milestone towards the application of graphene in electronics is identifying a suitable electronic device for graphene. Many efforts have pursued using graphene in existing device geometries, hoping to achieve better performance due to some of graphene's superior electronic properties, such as its high charge carrier mobility. However, since many of these properties have not yet been reproduced in mass producible graphene, including the ultra-high charge carrier mobility, the high expectations set for such graphene devices have not yet been achieved.

Another reason that also led to not meeting the expectations set for graphene devices is due to the diversity of graphene's unique properties, which in most existing devices end up clashing with each other. One important example is graphene's high charge carrier mobility that gives rise to a very large mean free path for electron transport in graphene[17], a property highly favored by field effect devices with transistors in particular. This appealing property in graphene clashes with graphene's zero bandgap structure that results in its ambipolar behavior, which prevents a graphene field effect device from turning off efficiently [18]. Such a clash in properties gives rise to graphene FETs that cannot be turned off, making them impractical for switching applications, the primary application for FETs in general. However, a noteworthy attempt at reconciling between these two clashing properties was to use these ambipolar graphene FETs in new device functionalities that are useful for RF applications such as RF frequency multiplication[19], rather than restricting them to their traditional applications.

Nevertheless, the quest for an ultimate graphene device, similar to silicon's field effect transistor (FET), remains to be a highly sought-after endeavor that brings along many challenges. Such a challenging endeavor triggered the motivation behind the research presented throughout this thesis. This motivation is highlighted in the next section.

1.2 Motivation

The reasons which have hindered the discovery or conception of the ultimate graphene device are diverse and vary from application to another. However they seem to stem from two main misconceptions that start from the moment the research is initiated. These are related to the expectation, or more precisely the envisioned application, while the other is related to the strategy of device conceptualization. These two important factors are discussed individually in the following two subsections, outlining how these have been addressed in this thesis.

1.2.1 Envisioned Applications

Expectations within the device research community were raised to a very high level after the isolation of graphene in 2004, and since then graphene has been associated with taking well-established important applications to the next level, replacing current materials and devices that drive such applications, with digital electronics being at the top of this very long list. While being optimistic is regarded as positive, having an attainable expectation is important. Accordingly, this thesis follows an approach of setting a progressively increasing expectation of the impact of the conceptualized graphene devices, beginning with devices that have a strong potential in a niche application addressing a need that is not yet fulfilled nor is yet dominated by a specific device. Such an example is electronic Terahertz detection, driven by electronic rectifiers, which can provide access to a very interesting region of the electromagnetic spectrum that has been inaccessible for a long time [20]. In such an application, the need is not yet met, nor is there a single device that already dominates. This is contrary to the application of digital electronics, driven by electronic switches, in which the need is already achievable, and the application has long been dominated with a very well established class of devices; CMOS transistors.

Devices that are able to achieve rectification, do not only find applications in Terahertz detectors, but are also essential components in RF systems [21-24]. Although rectification at RF frequencies is already achievable, there is no single device that dominates such an application. Furthermore, most high frequency rectifiers are large in size in comparison with transistors, providing an unaddressed need for miniaturized nanoscale rectifiers. Moreover, with the increasing demand for RF components for flexible [25, 26], implantable [27, 28] and wearable electronics [29-32], realizing high

performance rectifiers using new types of materials that may offer flexibility and biocompatibility has become of greater importance. Based on the above, this thesis tries to explore the application of graphene, and an array of other two-dimensional materials, for the realization of high performance nanoscale rectifiers.

Another important niche application that complements electronic Terahertz detection is electronic Terahertz generation, which is achieved using Terahertz oscillators, driven mainly by resonant tunneling diodes, as well as a number of other candidate devices[20]. Once again, in such an application the need is not yet met, nor is there a single device or a single material that dominates. While resonant tunneling diodes have been very strong candidates, the material used for realizing them has varied greatly [33-36], and all have suffered from difficulty of integration with standard electronics due to their complex fabrication processes, leaving behind another need that is not yet met: Terahertz oscillators that can be integrated with standard CMOS electronics. The enabling property that makes resonant tunneling diodes promising candidates for electronic Terahertz generation is their Negative Differential Resistance (NDR) operation [37]. Accordingly, this thesis tries to also explore the application of graphene for the realization of nanoscale NDR devices that do not require complex fabrication processes.

However, the true potential of NDR devices does not stop at Terahertz generation, but rather extends to other applications with greater impact, including digital electronics. In digital electronics, NDR devices can enable multi-state logic and memory [38, 39], in which information can be stored and switched between multiple states within a single device, rather than two states only, which are usually referred to as the “0” and “1” or the “ON” and “OFF” states. Achieving this has a potential to revolutionize electronics, however, this has been out of the reach of state-of-the-art NDR devices, mainly due to their low performance, which needs to be enhanced. This is mainly due to their low peak-to-valley current ratios, which are currently suitable for oscillator applications, but not for digital switching and memory applications. Based on this, the pursuit of exploring the application of graphene for the realization of high performance NDR devices becomes much more appealing, for both direct applications, such as electronic Terahertz generation, and longer term applications of even greater impact, such as multi-state logic and memory.

Another important trend taking place in the electronics industry is the drive for complete integration between different system components in order to realize what is

referred to as a system-on-chip (SoC) [40-42]. While this can apply to a range of applications, one very promising front is biosensing systems, in which the need for integration between biosensors and electronics calls for compatible electronic biosensors [40, 42]. One application that has attracted great interest is DNA and protein sequencing [43-45], which can revolutionize medical diagnostics and genetics [43, 46, 47]. The driving process that enables sequencing is single biomolecule detection [48-50], and in such an application, the need is also not yet met, nor is there a single device that dominates. Accordingly, this thesis also tries to explore the application of graphene for the realization of single biomolecule detection devices.

In summary, this thesis investigates the use of two-dimensional nanomaterials for the realization of nanoelectronic devices that have an impact on three fronts: (1) short term applications that complement and advance the state-of-the-art in electronics, such as nanoscale rectifiers, (2) long term applications that have the potential to revolutionize electronics, such as NDR devices, and (3) long term biosensing applications, such as single biomolecule detection, in order to explore the possibility of realizing a complete SoC using 2D nanomaterials.

These three fronts will be addressed using a new approach to the conceptualization of electronic devices, as will be discussed in the next subsection, tackling the second misconception mentioned earlier related to the device conceptualization strategy. By exploring these three fronts, the feasibility of the proposed device conceptualization approach can be assessed in a much more comprehensive sense, giving an indication on its long term potential, but also providing valuable findings that can be implemented immediately in applications that are already within reach.

1.2.2 Device Conceptualization Strategy

Electronic devices have long been associated with the term "planar", such as in "planar electronics", which may allude to the misconception that most electronic devices are planar. However, it is processing that takes place in a planar manner, where each layer of the device structure is defined at the surface, within the plane, and then pattered or etched down, in a process that has been termed as "planar processing". However, the final device is in no-way planar, but is a truly three-dimensional device. This makes complete sense, given that all materials prior to the discovery of graphene were three-dimensional. Accordingly, most device architectures were based upon this fact and were tailored for three-dimensional bulk materials.

With the recent discovery of two-dimensional materials, this is no longer the case, and devices need not be three-dimensional nor do their current architectures need to be the starting point for new device conceptualization. This does not mean that we cannot benefit from the large valuable amount of rich knowledge in the field, but rather it may be important for us to view it from a different angle, focusing on this new opportunity of two-dimensionality. It is important to acknowledge that two-dimensional materials generally exhibit very interesting electronic properties, which does make them strong candidates for electronic devices, but it is not these properties that are the new ingredient that has been recently introduced, rather it is the attribute that defines them, their two-dimensionality. Accordingly, this attribute will be the starting point from which different device concepts stem, and this is specifically the approach that will be adopted in this thesis.

By conceiving devices based on exploiting this property of two-dimensionality, the conceived device architectures may be easily implemented with any new 2D material that is discovered, harnessing any new properties it brings forth, or even taking advantage of its more economical and practical synthesis methods. This way, devices would not be restricted to graphene, which may not end up finding a practical and economically reliable synthesis method to match that of silicon. Moreover, two-dimensionality is well-suited to planar processing technologies that have been developed to a great level of reliability and maturity over the years, and hence building devices focused on two-dimensionality may not require large reinvestments to the currently available fabrication infrastructures, providing a reasonable route for the commercialization of such devices.

Based on the above, with two-dimensional materials being the main ingredient in a device structure, and planar processing being the main approach adopted in the fabrication recipe, it would be very appealing and reasonable to have completely two-dimensional planar device architecture as the end product of the process, in which the whole device lies within the plane, i.e. the monolayer, that constitutes the two-dimensional material. This would mean that the resulting device is “atomically-thin”, and this can have important implications on the device’s miniaturization limit, as will be discussed in the next subsection.

1.2.3 Miniaturization Limit

Miniaturization has been the central driving force for the advancement of electronic devices over the past decades, following a trend that has been known as *Moore's Law*, in which device dimensions have been shrinking at a rapid rate. While the main focus has been on shrinking the length of devices, specifically when referring to field effect transistors, all the other dimensions of the devices needed to also shrink in order to keep up with the shrinking length. Accordingly, having an atomically-thin device would bring one of the device's dimensions, namely its thickness, which extends inside the plane of fabrication, to its ultimate miniaturization limit: a single atom. This would allow unrestricted miniaturization of the remaining two-dimensions, namely its width and length, which reside within the device's plane of fabrication.

Once the thickness is reduced to its minimum, the remaining factors that would limit the miniaturization of the other two dimensions would be the precision of the fabrication technologies and the device architecture. The first is out of the scope of this thesis, however, it is important to note that this has been making great progress in recent years with the development of numerous high precision patterning techniques [51-54]. On the other hand, the second factor, which is the device architecture, will be a central focus of the work presented in this thesis.

In order to address this factor, an important goal of this thesis will be the conceptualization of devices that permit ultimate miniaturization within the plane, while maintaining the device thickness at a minimum; a single atom wherever possible. This would ensure that any limitations due to the finite thickness of nanoscale devices, such as the well-known undesirable short channel effects that limit the operation of nanoscale field effect transistors [18], are eliminated as much as possible. This way the only limit will be that set by fabrication technologies.

Nevertheless, it is highly desirable that any newly proposed device concept would not be restricted to the nanoscale only, but would also be feasible at larger scales permitted by currently available processing technologies. However, this goal, although highly desirable, brings about a challenge to the methods used for investigating and simulating such new 'scalable' device concepts. This fact added to the fact that the materials used for the devices are relatively new and their properties are not yet completely understood, requires highly accurate and highly reliable theoretical methods of investigation and

simulation. This challenge will be addressed in the methods section later on, in section 1.5.

1.2.4 Why Two-Dimensional?

However, prior to the discussion of the used methods, it is important to point out two questions that would come to mind before pursuing the aforementioned quest. These two questions are as follows:

1. Are completely two-dimensional planar devices feasible?
2. What advantages and opportunities would a completely two-dimensional device bring forth when compared with a conventional three-dimensional device?

The first question is exactly what this thesis tries to investigate and address, and the answer to this question lies in what is to be presented in subsequent chapters of this thesis. However, a brief summary of these findings are presented in section 1.6, later on.

The second question, on the other hand, does indeed define the motivation of the work, and has two parts to its answer. The first part is the short term advantages, while the second part is the long term potentially greater impact advantages. The first part can be summarized with the following points, which if mentioned on their own, would serve as the motivation behind the research conducted in this thesis. These short term advantages of realizing completely two-dimensional planar devices are as follows:

1. *Ability for ultimate miniaturization*. This point has been addressed in the discussion above, and this in itself is a goal of great importance for any electronic device. The ability of reducing the size of electronic devices reduces their electronic footprint on Integrated Circuits (ICs) reducing the overall size of the IC and allowing its use in smaller gadgets, implantable systems and new applications where size is of importance such as nanoscale robots. Furthermore, reduction of the size of an IC usually reflects directly in lower cost of production as it allows the production of a larger number of ICs using the same wafer, which goes through the costly processing steps only once. Finally, reduction in size usually brings about enhancement in performance such as faster speed of operation and reduced parasitics.
2. *Reduced processing steps.* If a device is realized within the plane of a two-dimensional material using planar processing techniques, then it is very likely

that the device would require minimal process steps during fabrication, which directly reflects in lower cost and also enables the next advantage.

3. *Possible compatibility with standard electronics*, such as CMOS electronics. If a device can be realized within a single material layer that is two-dimensional, then it will not need a new wafer that needs bonding or integration with the CMOS wafer, nor will it need to take up multiple material layers and introduce numerous processing steps that would disturb the flow of the CMOS process. It may require a few process steps that may be introduced towards the end of the process. The final new device layer, using the new 2D nanomaterial, may be integrated above the metallization layers of the CMOS IC as a top layer.

The above points summarize the short term advantages of two-dimensional planar devices, and these will be further consolidated throughout the thesis, through the presentation of a number of conceptualized devices later on. As for the long term potentially greater-impact advantages, their discussion will be delayed towards the end of the thesis, after an answer, or at least some indications to it, has been established for the first question of whether completely two-dimensional planar devices are feasible or not. At that point the discussion of the longer term, potentially greater impact, advantages becomes more appreciable, and hence, this will be postponed to chapter 9: "Discussion"; the final chapter of this thesis.

1.3 Research Objectives

Based on the motivation outlined earlier, the **research question** that this thesis tries to address is the following:

Can 2D nanomaterials provide the future platform for electronic devices?

Being a broad research question, this will be rephrased and narrowed down into **three points** that are necessary for the assessment of the above question, which are as follows:

Can 2D materials provide a platform for the realization of electronic devices that:

(1) can complement and advance electronics on the short term,
(2) but also potentially revolutionize electronics on the longer term,
(3) while offering new opportunities for the interaction and integration of electronics with other types of systems?

In order to address the above points, three **research objectives** are set, each addressing one or two of the above mentioned points. The research objectives are:

The conception of electronic devices, based on 2D nanomaterials, which can achieve:

(1) Rectification (complementing electronics)
(2) Negative Differential Resistance (potentially revolutionizing electronics)
(3) Single Biomolecule Detection (interaction with other systems)

In order for the conceptualized devices to have a potential for great impact, while still ensuring a viable path towards commercialization, a number of **design strategies** are set with regards to the conceptualised devices. The devices should:

(1) Have completely two-dimensional planar architectures
(2) Permit ultimate miniaturization, while having scalable architectures
(3) Require minimal process steps for fabrication

In order to study the properties and expected performance of the conceptualized devices, theoretical **methods** will be employed, keeping in mind that they need to:

(1) Capture quantum effects
(2) Be able to investigate quantum systems with large numbers of atoms
(3) Provide a reasonable trade-off between accuracy and computational efficiency

The next section gives an overview of the thesis, explaining how each of the set research objectives has been addressed, and summarizing the overall structure of the thesis.

1.4 Thesis Overview

Three main research objectives had been previously set, however, due to its potentially direct short-term impact; the starting point of the research was set around the first research objective: conceptualization of novel electronic devices, based on two-dimensional nanomaterials, which can achieve rectification.

In order to reduce the number of unknown variables accompanying the set objective, the vast and rich literature related to electronic rectifying devices was revisited, with a mind-set focused on two-dimensionality, in quest of identifying an existing device architecture that could potentially serve as a starting point for the research. Most existing devices were implemented using bulk three-dimensional materials, and hence were three-dimensional in architecture. However, one device, which is termed as a Self-Switching Diode (SSD) [55], seemed to be a little different. Although the device was implemented using an array of different materials [55-58], all of which were three-dimensional bulk materials, the device in its essence had a two-dimensional architecture, which required some form of confinement for the unwanted third dimension through different methods. This was achieved through the use of thin films[57], vertical compound semiconductor heterostructures that give rise to a two-dimensional Electron Gas (2DEG) [55, 58], or silicon on insulator wafers [56]. However, although the device was implemented using 3D bulk materials that were not completely well-suited for its 2D architecture, it still showed very promising unreported performance in a number of important applications such as Terahertz and microwave detection [57-60]. Accordingly, the SSD was chosen as the starting point of the research carried out in this thesis, and has received a great focus in subsequent chapters.

In ***Chapter Two*** of this thesis, the realization of the first 2D SSD is proposed using graphene, yielding interesting findings on a promising class of nanoscale rectifiers. By utilizing some of graphene's unique electronic properties, the Graphene Self-Switching Diode (G-SSD) was transformed into a novel enhanced form of an SSD, boosting it rectification capabilities orders of magnitude, as will be presented in the chapter. This enhanced class of SSDs was termed as an all-graphene Self-Switching Metal-Insulator-Semiconductor Field Effect Diode (G-SS MISFED), and the reasons behind this name, as well as the in-depth conceptualization and investigation of this device, will be kept for chapter 2.

In ***Chapter Three***, the G-SSD presented in chapter two is enhanced and transformed once again into another new class of SSDs, however this time achieving a new device functionality: Negative Differential Resistance (NDR) operation. Apart from being the first SSD reported to achieve NDR, the physical phenomenon that it achieves NDR with is a completely new unreported physical phenomenon, details of which are kept for chapter 3.

Chapter Four then takes a new direction exploring the realization of single biomolecule detection devices using graphene. The research in this chapter builds upon a very promising existing class of graphene devices; graphene nanopores [61, 62]. While graphene nanopores are 2D in their architectures, the way they are operated can make them either 3D devices or 2D devices. Electrochemical operation based on ionic current measurement results in a 3D device [63, 64], while complete electronic operation and readout yields a completely 2D device [65-67]. The electronic 2D approach is adopted in this chapter. Embarking upon the work on G-SSDs, a completely new class of graphene nanopore biosensors is proposed by merging the graphene nanopore device concept with the G-SSD in a completely 2D architecture, yielding a self-tuneable class of biosensing devices. The work presented in this chapter represents the first proposal to the application of a SSD-based device in a biosensing application. The proposed devices are termed as tuneable graphene nanopores and show very promising biosensing capabilities that do not only stop at single biomolecule detection, but go further into probing intramolecular electrostatics within single biomolecules, details of which are kept for chapter 4.

Chapter Five revisits SSDs exploring a new promising 2D material for their realization. The chosen material is Molybdenum Disulphide (MoS_2) [68] and was chosen for two important factors, the first being its readily available wafer-scale synthesis methods that can be achieved directly on insulating substrates [69-71], providing a potentially closer route towards commercialization for such devices when compared with G-SSDs, and the second is its wide electronic bandgap [72]. Simulation results suggest that due to this wide bandgap the conductance of the device may be controlled more effectively when compared to the G-SSD. However lack of passivation introduces a challenge for such a device, which is addressed through doping as will be shown in chapter 5.

Chapter Six explores another promising 2D material for the realization of SSDs, however this time with a focus on long term impact rather than a potentially shorter lower-risk path towards commercialization. The chosen material is silicon's two-

dimensional allotrope, silicene [73], which exhibits a unique structural property referred to as "buckling" [74]. It is shown how this property results in greatly enhanced rectification in silicene SSDs when compared to graphene SSDs. The findings presented in this chapter may open up great opportunities, not only for SSDs, but more interestingly for any 2D planar silicene field effect device, suggesting another candidate route for the long term sustainability of silicon-based electronics, through its silicene form, as will be discussed in chapter 6.

Chapter Seven turns its focus towards a very important quantum phenomenon that is well exploited in existing electronic devices; resonant tunnelling [37]. However, in this chapter, resonant tunnelling is revisited and viewed from a new two-dimensional angle. Devices that operate based on resonant tunnelling, known as Resonant Tunnelling Diodes (RTDs), are a unique class of rectifiers that find use in a range of important applications. Although RTDs can be realized using a range of materials and geometries, they all have vertical 3D architectures. These vertical architectures require complex fabrication processes, which have restricted their ability to integrate with standard electronics. In this chapter, an enhanced class of RTDs, the Double Barrier RTD (DB-RTD), is reinvented into a completely two-dimensional planar device, and is termed as an all-graphene planar DB-RTD. The proposed planar device architecture can be realized using minimal process steps and enables many of the limitations that its vertical counterpart suffered from. However, the truly exciting attribute about the proposed device is its excellent performance, which results in greatly enhanced rectification as will be shown later on in this chapter.

Chapter Eight builds upon the all-graphene planar DB-RTD that was proposed in chapter 7. The two-dimensionality of the planar DB-RTD enables the integration of multiple quantum confinement regions within the device structure. By exploiting this capability, two highly confined quantum dots are coupled within a single RTD, giving rise to a new class of RTDs termed as an all-graphene Double-Quantum-Dot RTD with very unique electronic properties and exceptional Negative Differential Resistance operation as will be shown in this chapter. The very highly pronounced NDR effect that the proposed device achieves may enable a number of envisioned applications for NDR devices which were previously out-of-reach including ultrafast multi-state logic and memory. The details of this interesting NDR effect are kept for chapter 8.

Finally, ***Chapter Nine*** summarizes the overall findings presented throughout the thesis discussing the main conclusions that may be drawn from them in-light of the originally set research question and objectives. A number of recommendations for future work are presented. Finally, potentially promising future directions are discussed, highlighting the previously mentioned, though unrevealed, potentially high impact long-term opportunities and advantages that two-dimensional electronic devices may bring about to the future electronics roadmap.

In summary, ***Chapter One*** provides an introduction to the thesis highlighting the motivation and research objectives and outlining the strategies and methods adopted throughout the thesis. ***Chapters Two, Three and Four*** present three planar completely two-dimensional graphene field effect devices, derived from the self-switching diode geometry, which are used to achieve rectification, NDR operation and single biomolecule detection respectively. ***Chapters Five and Six*** investigate the extendibility of such field effect device concepts to other two-dimensional materials by proposing the implementation of SSDs using MoS_2 and Silicene respectively. ***Chapters Seven and Eight*** then present two new classes of graphene-based RTDs that exhibit a planar completely two-dimensional architecture, and achieve enhanced rectification and highly pronounced NDR operation respectively. Finally, ***Chapter Nine*** discusses the main conclusions drawn from the presented work, makes a number of recommendations for future work and highlights possible future directions.

The next section of this chapter outlines the methods that have been adopted for the study and simulation of the above mentioned conceptualized devices that are presented later on in the subsequent chapters of the thesis.

1.5 Methods

When investigating electronic devices at their ultimate downscaled dimensions quantum effects become of great importance as they directly impact the charge transport properties of the device. Semi-classical and classical transport models based on *Boltzmann*'s transport equation (BTE), including drift-diffusion transport models, would not capture such effects, nor would be reliable for new device architectures especially when they are also implemented using new types of materials. Accordingly, quantum mechanical simulations become necessary. The non-equilibrium Green's function (NEGF) formalism is a powerful method to handle quantum systems, and in recent years there have been several developments of atomic-scale electron-transport simulation models based on the NEGF formalism. These simulation approaches can be divided into two main categories: (1) *ab initio* approaches, where the electronic structure of the system is calculated from first principles, typically with density-functional theory (DFT) [75], and (2) semi-empirical approaches, where the electronic structure is calculated using a model with adjustable parameters fitted to experiments or first principles calculations [76]. While it would be tempting to use first principles calculation methods based on the Density Functional Theory (DFT) [75] in order to obtain a highly accurate understanding of the transport processes that take place in the device under investigation, such methods are computationally very expensive and become relatively inefficient especially if the quantum system under investigation involves a large number of atoms. This is the case for most planar devices that have "scalable architectures". The term "scalable" here refers to nanoscale architectures that can be realized at larger sizes while still maintaining most of their qualitative features and electronic functionalities, eliminating molecular electronic devices for example.

The more computationally efficient quantum mechanical simulation approach capable of simulating larger quantum systems, while still being able to capture quantum transport effects, is through semi-empirical methods that are based on tight-binding models. Out of these semi-empirical methods, the Extended Huckel (EH) method [76] offers favourable accuracy as it accounts for effects due to atoms as far as the third nearest neighbouring atom, unlike most other semi-empirical methods that only account for effects due to the nearest or the second nearest neighbouring atoms.

Accordingly, transport calculations for obtaining I-V characteristic curves, transmission spectra and transmission pathways plots, presented throughout the thesis, were all based

on the Extended Huckel (EH) [76] method coupled with Non-Equilibrium Green's Function (NEGF) formalism [75] as implemented in Atomistic Tool Kit (ATK) software package [77]. This SE EH method treats the effect of the external potential on the entire system (atomic and also trench regions) with desirable computational efficiency. Moreover, it has been reported that calculations based on the EH method for large atomic structures show quantitative agreement with experimental results when compared with DFT-based *ab initio* approaches [76].

Another very important feature of the used method is that it permits the inclusion of biomolecules and biological systems in the calculation and includes their effect on the electronic properties of the electronic device under investigation, while also taking into consideration the effect that the electronic device has on the biomolecules or the biological system. This enables the study of the interaction of biomolecules and biological systems with electronic systems.

1.5.1 Calculation of Transport (I-V) Characteristics

Prior to transport calculations, device geometries were optimized and their coordinates were relaxed using quick optimization methods, such as the *Brenner* [78] and the *Tersof*[79] potentials, until forces on individual atoms were minimized to be at least smaller than 0.5 eV/Å^2, and wherever possible (for smaller device structures) this criterion was reduced even further, down to 0.005 eV/Å^2 as with the smallest device structures of Chapter 7. The *Brenner* potential is a second-generation potential energy function for solid carbon and hydrocarbon molecules that is based on an empirical bond order formalism and was first developed by Brenner in 1990 [80] and then revised in 2002 [78]. The *Tersof* potential is an earlier more general approach developed by Tersof in 1988 to the formulation of interatomic potentials for covalent systems [79], which the *Brenner* potential is based upon. For individual chapters, specific quick optimization methods and exact optimization criteria are mentioned at the end of each chapter. Generally, quick optimization methods were used instead of the computationally expensive DFT based approaches as they provide a reliable estimate due to the fact that in most device structures the optimized crystal lattice of the two-dimensional material is minimally altered by the creation of simple in-plane trenches or pores. Stacking of material layers, complex material interfaces and binding of biomolecules to material surfaces were all not needed. Generally, quick optimization was able to capture all relevant material properties and achieve a desirable optimized geometry. Only in the

case of silicene, DFT based optimization was needed in order to accurately capture its buckling property, as will be described later on in chapter 6.

Each device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of either (1 x 10 x 50) or (1 x 20 x 50) for all devices, with 50 sample points along the length (transport direction) and 10 or 20 points along the width of the two-terminal structure. The used k-points mesh for each chapter is specified at the end of the chapter.

In the used tight-binding model, which is based on the Extended Huckel Method as implemented in the ATK-SE package, the tight-binding Hamiltonian is parameterized using a two-center approximation, where the matrix elements are described in terms of overlaps between *Slater* orbitals on each site. The used weighting scheme of the orbital energies of the offsite Hamiltonian was according to Wolfsburg [81]. Further details about the calculation method can be found in [77].

The electronic transport properties were then calculated using Nonequilibrium Green's Function (NEGF) formalism. Each device structure was constructed as the three previously mentioned regions (left-electrode, central-region and right-electrode) and coherent transport of electrons was assumed to occur between left and right electrodes with Fermi levels μ_L and μ_R through the central region. According to Landauer's formula [82], the coherent current between the electrodes is given by:

$$I(V) = \frac{2e}{h}\int_{\mu_R}^{\mu_L} T(E,V)[f_0(E-\mu_L) - f_0(E-\mu_R)]dE \tag{1.1}$$

where $T(E,V)$ is the transmission probability of incident electrons with energy E from the left-electrode (L) to the right-electrode (R), $f_0(E-\mu_{L(R)})$ is the Fermi-Dirac distribution function of electrons in (L) and (R) respectively, and $V = \frac{\mu_R - \mu_L}{e}$ is the potential difference between (L) and (R). The $T(E,V)$ is correlated with $\hat{G}^a(E)$ and $\hat{G}^r(E)$, the Green's function matrices reflected from (L) and (R) to the central scattering region respectively, as:

$$T(E,V) = Tr\left[\mathrm{Im}\sum_L\left(E-\frac{eV}{2}\right)\hat{G}^r(E)\mathrm{Im}\sum_R\left(E+\frac{eV}{2}\right)\hat{G}^a(E)\right] \tag{1.2}$$

where $\sum_{L(R)}$ are electrodes' self-energies describing the coupling with the central region.

1.5.2 Calculation of Transmission Pathways

As the Landauer approach only connects the external electrode current $I(V)$ with the summed energy dependent transmission probability $T(E,V)$, we need to express local current components at the atomic level along the chemical bonds to describe the variation of coherent electron transport through the system. Local current components may be investigated by extracting local transmission components. The total transmission coefficient can be split into local bond contributions, T_{ij}, which are represented in ATK by lines along the bond lengths, called transmission pathways. The relationship between the total transmission coefficient and the local bond contributions can be described as:

$$T(E,V) = \sum_{i \in A, j \in B} T_{ij}(E,V) \tag{1.3}$$

where A and B represent pairs of atoms separated by an imaginary surface perpendicular along the bond length. The total transmission coefficient is the sum of the local bond contributions between all pairs of atoms A and B. A negative value of T_{ij} corresponds to back scattered electrons along the bond, while a positive value corresponds to transmitted electrons. Further details can be found in [83].

1.6 Main Contributions

In this section, a summary of the original contributions made in each contributing chapter is presented in point-form. The contributions are as follows:

Chapter Two:

- Proposed for the first time a 2D SSD, the Graphene SSD (G-SSD).
- Discovered that zigzag-channel G-SSDs do not rectify current, while armchair-channel G-SSDs do.
- Proposed a method for the realization of all-graphene Metal-Insulator-Semiconductor (MIS) based structures within a single graphene monolayer, in which graphene acts as the metal and the semiconductor concurrently, enabled by the property of bandgap tuneability of graphene nanoribbons with width variation.
- Proposed and conceptualized a new class of SSDs, the all-graphene self-switching MISFED (G-SS MISFED) which achieves enhanced current rectification compared to the standard G-SSD.
- Studied the different transport mechanisms in a G-SS MISFED, showing how tunnelling current through the trenches becomes a major issue at the nanoscale.
- Proposed the use of nitrogen passivation in order to limit unwanted tunnelling current and increase charge carrier concentration, enhancing rectification.
- Optimized the G-SS MISFED geometry achieving a very high current rectification that exceeds 5,000, using an atomically-thin nanoscale rectifier with sub-10 nm dimensions.
- Proposed a number of fabrication techniques for the realization of the proposed devices.

Chapter Three:

- Proposed a new class of SSDs; the asymmetrically gated G-SSD, which is the first SSD to exhibit NDR operation.
- Presented a new NDR mechanism, in which the small tunnelling current controls a much larger channel conduction current, giving rise to high peak current values in the micro amps range.

- Confirmed the physical phenomena that drive the new NDR mechanism through transmission pathways mapping within the device and presented a physical understanding of the origins of such phenomena.
- Studied how scaling affects the performance of an asymmetrically gated G-SSD, and achieved a high peak-to-valley current ratio of 40 in a relatively large scale device.
- Discussed the fabrication feasibility of the proposed devices.

Chapter Four:

- Proposed a new class of graphene nanopore devices based on incorporating the nanopore within a G-SSD geometry, giving rise to the first self-tuneable graphene nanopore device, in which the nanopore's conductivity can be tuned to levels comparable to the conductance changes caused by the translocation of single biomolecules.
- Proposed for the first time the application of a SSD-based device in a biosensing application.
- Investigated the effect of the translocation of a single biomolecule, the smallest amino acid – glycine, through the device's nanopore, showing very high change in conductance that reaches close to 90%.
- Compared the detection of glycine with that of water molecules, showing high specificity for glycine detection when present in an aqueous solution.
- Proposed the use of nitrogen passivation in order to make an n-type tuneable graphene nanopore device that has a high concentration of charge carriers, making it a highly sensitive electrostatic detector.
- Investigated the effect of the translocation of a single glycine molecule through the nitrogen passivated tuneable graphene nanopore device, showing high changes in conductance that reach close to 90%.
- Confirmed, using transmission pathways mapping through the device, that the device is highly sensitive to intramolecular electrostatics, detecting the charge carried by the carboxyl group in the glycine molecule, which is equivalent to a single electron, with high detection sensitivities and enabling the device to probe charge distribution within single biomolecules.

Chapter Five:

- Proposed and investigated the implementation of SSDs using MoS_2 for the first time, indicating their p-type operation, contrary to G-SSDs, which are n-type.
- Confirmed, using transmission pathways mapping through the device, that the wide bandgap of MoS_2 enables strong field effect control over the SSD's channel, turning it off completely.
- Showed that a major challenge in MoS_2 SSDs in unwanted tunnelling current through the trenches, due to lack of passivation.
- Proposed substitutional Phosphorous doping, in place of Sulphur, in order to make the device more p-type and enhance rectification.
- Showed how p-type doping of the channel reduces tunnelling current through the side gates, increasing the rectification ratio of the device an order of magnitude up to a value of 70.

Chapter Six:

- Proposed and investigated the implementation of SSDs using Silicene for the first time, indicating relatively similar properties to G-SSDs.
- Showed how zigzag-channel Silicene SSDs do not achieve rectification, while armchair-channel Silicene SSDs do, similar to G-SSDs.
- Showed how bandgap tuneability of silicene nanoribbons with width variation, enables the realization of Silicene Self-Switching MISFEDs, which achieve enhanced rectification.
- Compared the performance of Silicene SSDs and MISFEDs with Graphene SSDs and MISFEDs, showing a 30 fold enhancement in the rectification ratio for Silicene devices.
- Achieved a high rectification ratio of 240 using an atomically-thin silicene MISFED with sub-10 nm dimensions, without the need for special passivation or doping, as in graphene and MoS_2.
- Attributed the stronger field effect control in planar Silicene devices, when compared to planar graphene devices, to the buckling property of Silicene, which enables bandgap tuneability of the Silicene channel through an in-plane electric field that has a vertical component, as in a SSD and a MISFED.

Chapter Seven:

- Proposed a new class of planar completely two-dimensional RTDs, the all-graphene planar double barrier RTDs (DB-RTDs), which can be realized within a single graphene nanoribbon with minimal process steps.
- Investigated the device's transport properties, showing how the double barriers block the flow of electrons at most energies except within a narrow range, within which resonance occurs.
- Used the device to achieve current rectification with an extremely high rectification ratio exceeding 50,000.
- Proposed an in-plane parallel connection of multiple devices in order to increase the peak current values provided by the devices making them well into the micro amps range.
- Proposed a number of fabrication strategies for the realization of the proposed devices.

Chapter Eight:

- Proposed a new class of planar completely two-dimensional RTDs, the all graphene double-quantum-dot RTD, which can be realized within a single graphene nanoribbon within minimal process steps.
- Investigated the transport properties of the device, showing how the coupling of the double quantum dots within a single device results in the blockage of current flow at most bias voltages except a narrow range, within which the double quantum dots couple coherently, giving rise to a very unique current-voltage curve that comprises a single current peak.
- Showed through quantum simulations that the proposed devices achieve a highly pronounced NDR effect with extremely high unreported peak-to-valley current ratios (PVCRs) that exceeds 50,000.
- Showed that the position of the single current peak, within the device's I-V curve, can be tuned between discrete voltage levels by varying the length of the quantum dots, giving rise to a digitally tuneable NDR effect.
- Proposed a multi-peak NDR effect device through an in-plane parallel connection of multiple tuned devices at no extra fabrication steps.
- Proposed a number of fabrication strategies for the realization of the proposed devices.

1.7 Derived Publications

This section lists the publications that were derived from this thesis. From each of the seven contributing chapters (chapter 2 – 8) a journal paper was derived, adding up to a total of seven journal papers, some of which are already published [84-88], while others are currently under consideration [89, 90]. In all of these papers the author of this thesis was the main, first and corresponding author. These papers are as follows:

Journal Papers

[1] ***Chapter Two:*** **F. Al-Dirini,** F. M. Hossain, A. Nirmalathas, E. Skafidas, "All-Graphene Planar Self-Switching MISFEDs, Metal-Insulator-Semiconductor Field-Effect Diodes," *Scientific Reports*, vol. 4, p. 3983, Feb. 2014.

[2] ***Chapter Three:*** **F. Al-Dirini,** F. M. Hossain, A. Nirmalathas, E. Skafidas, "Asymmetrically-Gated Graphene Self Switching Diodes as Negative Differential Resistance Devices," *Nanoscale*, vol. 6, pp. 7628-7634, Apr. 2014.

[3] ***Chapter Four:*** **F. Al-Dirini,** M. A. Mohammed, M. S. Hossain, F. M. Hossain, A. Nirmalathas, E. Skafidas, "Tuneable Graphene Nanopores for Single Biomolecule Detection," Submitted to *Nanoscale*. ***(Under Consideration)***

[4] ***Chapter Five:*** **F. Al-Dirini,** F. M. Hossain, M. A. Mohammed, M. S. Hossain, A. Nirmalathas, E. Skafidas, "Monolayer MoS_2 Self Switching Diodes," Submitted to *Journal of Applied Physics*. ***(Under Consideration)***

[5] ***Chapter Six:*** **F. Al-Dirini,** F. M. Hossain, M. A. Mohammed, A. Nirmalathas, E. Skafidas, "Highly Effective Conductance Modulation in Planar Silicene Field Effect Devices," *Scientific Reports*, vol. 5, p. 14815, Oct. 2015.

[6] ***Chapter Seven:*** **F. Al-Dirini,** F. M. Hossain, A. Nirmalathas, E. Skafidas, "All-Graphene Planar Double Barrier Resonant Tunneling Diodes," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 5, pp. 118-122, Sep. 2014.

[7] ***Chapter Eight:*** **F. Al-Dirini,** M. A. Mohammed, F. M. Hossain, A. Nirmalathas, E. Skafidas, "All-Graphene Double-Quantum-Dot Resonant Tunneling Diodes," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 1, pp. 30-39, Jan. 2016.

Also a number of conference papers [91, 92] and abstracts [93, 94] were presented at international conferences and published in the conference proceedings, in which the author of this thesis was also the main, first and corresponding author. These papers are as follows:

Conference Papers and Abstracts:

[8] ***Chapter Two:*** **F. Al-Dirini,** S. Skafidas, A. Nirmalathas, "Graphene Self-Switching Diodes", presented at *Graphene 2013 Conference*, Bilbao, Spain, April 2013.

[9] ***Chapter Two:*** **F. Al-Dirini,** A. Nirmalathas, E. Skafidas, "Graphene Self-Switching Diodes with high rectification ratios," in *13th IEEE Conference on Nanotechnology (IEEE-NANO)*, Beijing, China, Aug. 2013, pp. 698-701.

[10] ***Chapter Four:*** **F. Al-Dirini,** M. S. Hossain, W. Qui, F. M. Hossain, A. Nirmalathas, E. Skafidas, "Graphene Field Effect Nanopore Glycine Detector," in *14th IEEE Conference on Nanotechnology (IEEE-NANO)*, Toronto, Canada, Aug. 2014, pp. 1004-1007.

[11] ***Overall Thesis:*** **F. Al-Dirini,** M. A. Mohammed, M. S. Hossain, F. M. Hossain, A. Nirmalathas, E. Skafidas, "**(Invited)** Planar Nanoelectronic Devices and Biosensors Using Two-Dimensional Nanomaterials," *Meeting Abstracts – The Electrochemical Society*, vol. MA2015-03, no. 20, p. 1347, May 2015.

2 All-Graphene Planar Self-Switching MISFEDs

Graphene normally behaves as a semimetal because it lacks a bandgap, but when it is patterned into nanoribbons a bandgap can be introduced. By varying the width of these nanoribbons this band gap can be tuned from semiconducting to metallic. This property allows metallic and semiconducting regions within a single Graphene monolayer, which can be used in realising two-dimensional (2D) planar Metal-Insulator-Semiconductor field effect devices. Based on this concept, this chapter proposes a new class of nano-scale planar devices named Graphene Self-Switching MISFEDs (Metal-Insulator-Semiconductor Field-Effect Diodes), in which Graphene is used as the metal and the semiconductor concurrently. The proposed devices exhibit excellent current-voltage characteristics while occupying an ultra-small area with sub-10 nm dimensions and an ultimate thinness of a single atom. Quantum mechanical simulation results, based on the Extended Huckel method and Nonequilibrium Green's Function Formalism, show that a Graphene Self-Switching MISFED with a channel as short as 5 nm can achieve forward-to-reverse current rectification ratios exceeding 5000.

2.1 Introduction

Graphene, an atomically-thin sheet of carbon atoms [3], has opened many opportunities in the field of electronics due to its unique electronic properties [5, 95] including enhanced performance electronics and sensors [11]. The realization of high frequency Graphene Field Effect Transistors (FETs) [6-9] has led to the realization of wafer scale Graphene integrated circuits [10] with FETs that have enhanced functionalities [19, 96]. More recently, new classes of devices have been realized by exploiting some of Graphene's unique properties [97, 98]. On the other hand, realization of Graphene-based diodes has received much less attention. High performance diodes will enable next generation terahertz detectors and new RF systems, but their realization at the nano-scale with high operation frequency has been a challenge. Graphene-based schottky diodes, in which Graphene was used as the metal [99-101] or the semiconductor [102], have been realized, but are limited to large sizes for high frequency operation. The nano-scale alternative to a schottky diode would be a diode-connected FET, but this extra diode connection introduces increased parasitic capacitances and inductances that limit the operation frequency of the diode-connected FET.

In order to overcome this problem diodes based on new rectification mechanisms were proposed, one of which was the Self-Switching Diode (SSD) [55]. A SSD is an asymmetrical nanowire in which rectification occurs due to a self-induced field-effect that enhances conduction through the nanowire in one direction, while suppressing it in the opposite direction. Self-Switching Diodes showed excellent high frequency performance at 110 GHz [59], and were later demonstrated as room-temperature Terahertz detectors [60]. Self-switching diodes are two-dimensional (2D) planar devices that require very minimal lithography steps during fabrication and are very well suited for a two dimensional material like Graphene. Nevertheless, these devices suffer from the constraint of not having a metallic gate, as the channel (the nanowire) and the side gates in them need to be made from the same material, which is usually a semiconductor. Until recently there was no single material that could have metallic regions and also semiconducting regions within the same plane, until the discovery of Graphene Nanoribbons (GNRs) [103, 104].

Graphene Nanoribbons, which are long narrow strips of Graphene, can be either zigzag-edged or armchair-edged and can behave as metallic or semiconducting respectively[105]. Etching GNRs with smooth edges [52, 106-111] or realizing them

through other means [112-115] has been making good progress in recent years, and this can lead to the ability of making zGNRs and aGNRs from a single Graphene monolayer. This would mean that, within a single Graphene monolayer, metallic and semiconducting regions can be formed, and a number of planar atomically-thin 2D devices have been proposed based on this concept [116, 117]. Moreover, these devices may also be interconnected within the same single Graphene monolayer using GNRs[118], which may lead to not only atomically-thin devices, but more interestingly, all-Graphene atomically-thin electronic circuits. However, it is important to note that there is a great limitation in this, as these regions can only be realized at an angle to each other, since the different edge shapes arise from etching at different angles [119]. This would exclude all types of field effect devices, since the field in them is usually applied from a metallic region that is directly adjacent to a semiconducting region.

In this chapter, it is shown how etching a Graphene monolayer into adjacent parallel aGNRs with precisely defined edges, can give rise to high performance nano-scale field effect devices that are planar and completely 2D, i.e. atomically thin. Armchair GNRs are generally semiconducting and exhibit a bandgap, but at certain widths they start to behave as metals with vanishingly small band gaps or no band gaps at all [120]. This occurs in aGNRs that have a width of $3p + 2$ carbon atoms, where p is an integer. For all other widths, aGNRs are semiconducting.

By exploiting this property, a new class of self-switching diodes is proposed, having metallic gates controlling a semiconducting channel, all built with a single Graphene monolayer. This new class of devices is referred to here as Graphene Self-Switching MISFEDs (Metal-Insulator-Semiconductor Field-Effect Diodes). Both the metal and the semiconductor in the proposed class of devices are aGNRs but with different widths, separated by an insulating region. The proposed devices are at sub-10 nm dimensions and still achieve forward-to-reverse current rectification ratios exceeding 5000.

This chapter begins by highlighting how the constraint of not having a metallic gate in a SSD limits its performance, and then shows how a Graphene SSD (G-SSD) can be transformed into a much more superior Graphene Self-Switching MISFED (G-SS MISFED) by tackling this issue, highlighting this through the comparison of the performance of both devices.

2.2 Results and Discussion

2.2.1 The Graphene Self-Switching Diode (G-SSD)

Self-Switching Diodes are formed by etching two L-shaped trenches back-to-back forming a narrow nano-channel in between them, through which conduction occurs. The conductance of this nano-channel is controlled by a field effect, which is applied by two side gates surrounding the channel, and these are connected to one of the two-terminals of the device. The geometry of the device (Fig. 2.1(a)) and its principle of operation are illustrated in Fig. 2.1. With no bias voltage applied, natural depletion regions are formed at the edges of the nano-channel due to the presence of surface energy states at the edges of the L-shaped trenches (Fig. 2.1(b)). Applying a negative bias voltage widens these depletion regions eventually pinching-off the channel and suppressing current flow through it in the reverse direction (Fig. 2.1(c)). On the other hand, a positive applied voltage results in narrowing the depletion regions, eventually opening up the channel and allowing current conduction in the forward direction (Fig. 2.1(d)). This unidirectional current flow results in non-linear current-voltage characteristics very similar to those of a conventional diode (Fig. 2.1(e)).

The nano-channel in a G-SSD is a Graphene nano-ribbon, and in order to control the conductance of this channel by an electric field it needs to be semiconducting, this is achieved using an aGNR. A corollary to this is that a G-SSD geometry with a zGNR channel should not behave like a diode if the rectification mechanism in a G-SSD is purely based on an electric field effect, since zGNRs are metallic and a metal's conductance should not be affected by an electric field. In order to confirm this, Nonequilibrium Green's Function (NEGF) formalism and a tight-binding model based on the Extended Huckel (EH) Method [76] as implemented in Quantum Wise Atomistix Tool Kit [77] (calculation details are discussed in the methods section), are used to calculate the I-V characteristics of two G-SSD device geometries, one with a zGNR channel and the other with an aGNR channel. The simulated device geometries are shown in Figs. 2.2(a) and 2.2(c) respectively, while their I-V characteristics are shown in Figs. 2.2(b) and 2.2(d) respectively.

Figure 2.2(b) shows a linear I-V relationship for the G-SSD geometry with a zGNR, representing no rectification and confirming that rectification in a G-SSD is a field effect phenomenon, and is not related to other transport mechanisms.

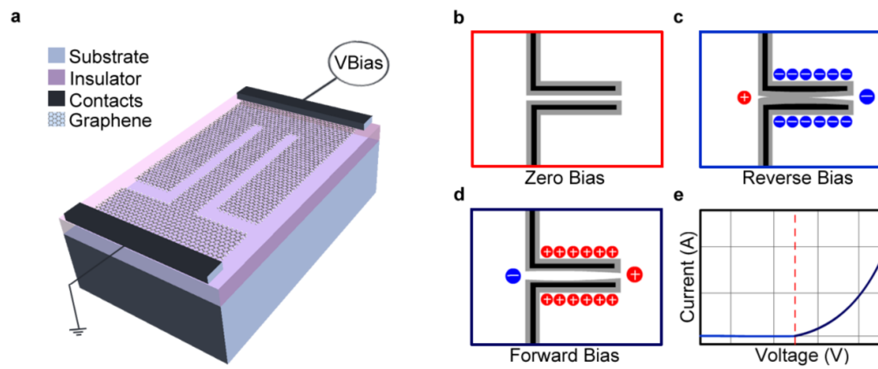

Figure 2.1 | Graphene Self-Switching Diode (G-SSD) architecture and principle of operation. (a) Schematic diagram showing the structure and architecture of a G-SSD and showing the biasing direction of the device. (b) Illustration showing where the natural depletion regions (grey regions) form in a G-SSD due to the presence of surface states at the boundaries of the L-shaped trenches. (c) Illustration showing how the depletions regions are widened eventually pinching-off the channel due to the application of a negative bias voltage across the device. (d) Illustration showing how the depletion regions are narrowed eventually opening up the channel due to the application of a positive bias voltage across the device. (e) Expected I-V characteristics of the device. The light blue part of the curve represents the region in which the device has a pinched-off channel and is not conducting, while the dark blue part of the curve represents the region in which the device has an open channel and is conducting.

On the other hand Fig. 2.2(d) does show a clearly non-linear I-V response curve for a G-SSD with an aGNR channel, but asymmetry is not noticeable, and consequently no rectification occurs. In order to understand this, further analysis of the device geometry presented in Fig. 2.2(c) is required. As can be seen from Fig. 2.2(c), having a semiconducting aGNR channel also requires having the side gates as aGNRs. This means that the side gates are also semiconducting, as is the case with any SSD. In Fig. 2.2(c) the channel is 6 atoms wide, and so are each of the side gates, and since all of them are semiconducting and equal in size it is expected that they will affect each other equally. This means that depletion regions will form, not only in the channel, but also in the gates, resulting in what may be referred to as an image field effect from the channel on to the gates. This is illustrated in Fig. 2.1(b). This image effect greatly weakens the control the gates can have on the channel's conductance, and since in this case the gates are equal in size to the channel, it is expected that they will not be able to control the channel. However, this also implies that if the gates are larger in size than the channel, then the effective field generated by the gates on the channel will dominate and hence may have some control over its conductance.

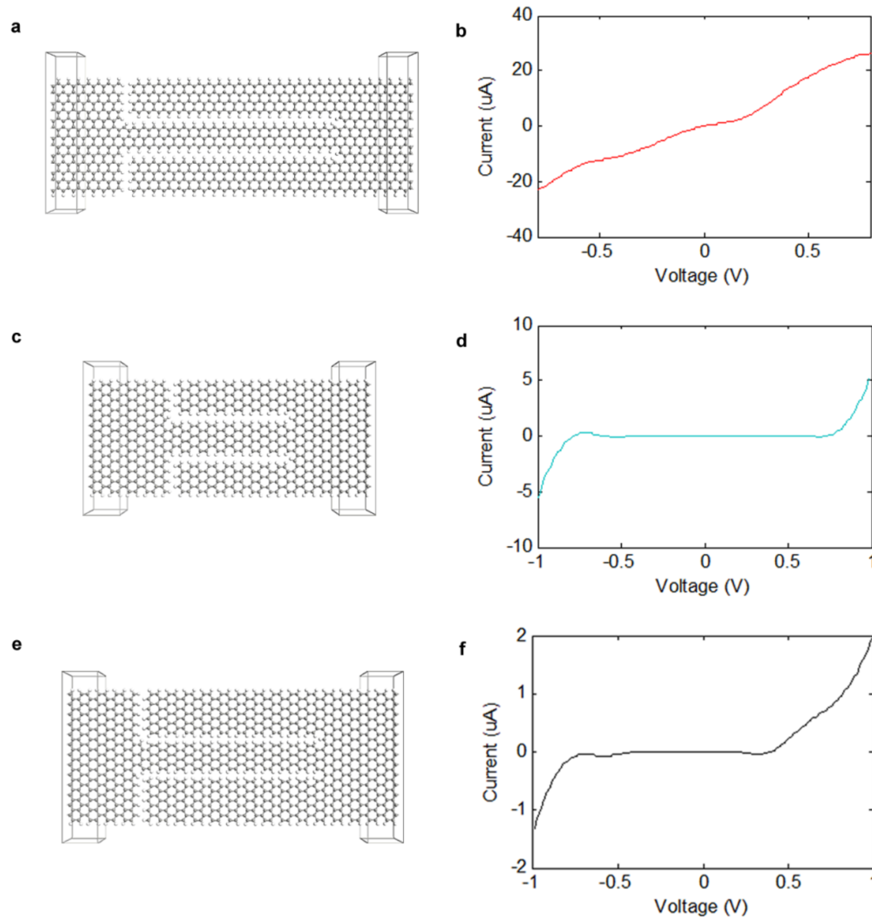

Figure 2.2 | Comparison between different G-SSD types. (a) A G-SSD structure with a metallic zigzag GNR as the channel. All dangling carbon bonds are passivated with hydrogen in this device and in all subsequent device structures, unless stated otherwise. (b) The simulated I-V characteristics of the device in (a) showing an almost linear response with no rectification and very high current values due to the metallic behaviour of the channel. (c) A G-SSD structure with a semiconducting armchair GNR as the channel. The channel and the two side gates are chosen to be 6 atoms wide making them all equal in width. (d) The I-V characteristics of the device in (c) showing a non-linear response that is almost symmetrical due to the image field-effect from the channel on to the gates and vice versa. (e) A G-SSD structure with a semiconducting armchair GNR as the channel. The channel is chosen to be 6 atoms wide, while the two side gates are chosen to be 9 atoms wide respectively, and the channel is made longer than the channel of the device in (c). (f) The I-V characteristics of the device in (e) showing a non-linear response with significant asymmetry achieving proper rectification. The threshold turn-on voltage of the device is about 0.4 V, while the reverse breakdown voltage of the device is about -0.75 V. Within the rectification region of operation (-0.75 V – 0.75 V) the rectification ratio of the device reaches almost close to one order of magnitude.

In order to confirm this, another G-SSD device with an aGNR channel was investigated, but this time the gates were made 9 atoms wide, making each of them one and a half times wider than the channel, and is shown in Fig. 2.2(e). Moreover, the channel length

was made longer, in order to increase the interacting area between the gates and the channel, and achieve better field-effect control. The I-V characteristics of the optimized device are shown in Fig. 2.2(f), and as expected, they show very good asymmetry; in which forward conduction is enhanced while reverse conduction is suppressed. The optimized device achieves a relatively comparable rectification ratio of forward current to reverse current in comparison with other previously reported SSDs, reaching close to almost one order of magnitude. Nevertheless, this ratio needs to be improved.

2.2.2 Graphene Self-Switching MISFEDs

In order to overcome the limitations of conventional all-semiconducting Self-Switching Diodes, a new class of planar self-switching devices is proposed here, and is named a Graphene Self-Switching MISFED (G-SS MISFED), and is shown in Fig. 2.3.

Figure 2.3(a) shows a perspective view of the geometry of a G-SS MISFED, while Figs. 2.3(b) and 2.3(c) illustrate the difference between a G-SS MISFED and a G-SSD, respectively. The fundamental difference between the two devices, is that the side gates in a G-SSD are semiconducting, while the side gates in a G-SS MISFED are metallic and the latter is achieved by ensuring that the side gating aGNRs are $3p+2$ carbon atoms wide.

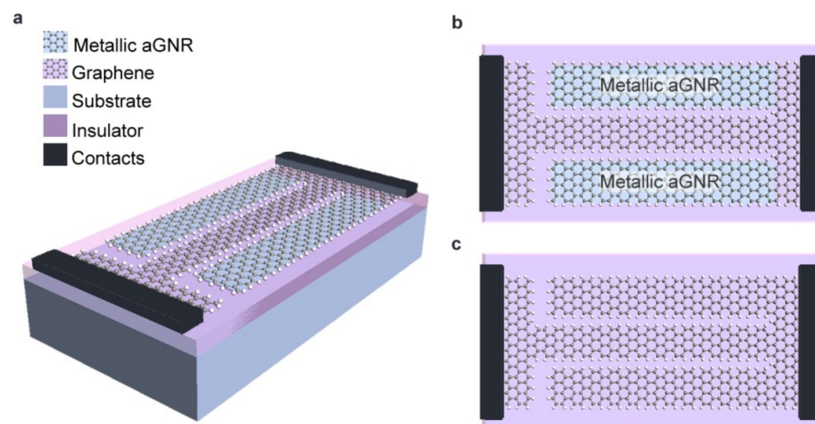

Figure 2.3 | The fundamental difference between a G-SS MISFED and a G-SSD. (a) A schematic diagram showing a perspective view of the structure of a Graphene Self-Switching MISFED (G-SS MISFED). Graphene regions that are highlighted in blue represent aGNRs that are metallic with a width of $3p+2$ atoms, where p is an integer. (b) A top-view of the G-SS MISFED in (a) illustrating how the choice of the width of the side gates can make them metallic and highlighting the fundamental difference between a G-SS MISFED and a G-SSD.The side gates are 8 atoms wide. (c) A top-view of a G-SSD showing that the side gates are semiconducting like the channel. The side gates here are 7 atoms wide.

However, it is worth noting that precise width control is only relevant at extremely downscaled dimensions, where quantum effects dominate, but at larger dimensions, this can also be realized based on a different approach that is experimentally more feasible, without the need for GNRs with perfect edges. This can be achieved through a single etching step, in which the channel is etched down as narrow as possible (narrower than 20 nm), making it semiconducting due to its edge imperfections, while the side gates are defined as wide as possible (at least wider than 50 nm), ensuring that they have very small bandgaps, or no bandgaps at all. Here we will implement the first approach based on the quantum effects in order to investigate the performance of a G-SS MISFED at its ultimate downscaled dimensions.

In order to see how this reflects on the performance of the device, the I-V characteristics of a Graphene Self-Switching MISFED, shown in Fig. 2.4(a), were calculated using the previously mentioned methods and are shown in Fig. 2.4(d). The geometry of the simulated device in Fig. 2.4(a) represents a comparable geometry to the one in Fig. 2.2(c), which did not achieve any rectification. The device in Fig. 2.2(c) had side gating aGNRs that were 6 atoms wide, and hence they were semiconducting, while the device in Fig. 2.4(a) has side gating aGNRs that are 5 atoms wide, making them metallic. Unlike the I-V characteristics of the G-SSD with similar dimensions shown in Fig. 2.2(c), the Graphene Self-Switching MISFED shown in Fig. 2.4(a) shows very good asymmetry and strong rectification. Even when compared with the optimized G-SSD that was presented in Fig. 2.2(e), the Graphene Self-Switching MISFED without any optimization still greatly outperforms the optimized G-SSD, as shown in Fig. 2.4(d).

In order to obtain a better understanding of the transport mechanisms in a Graphene Self-Switching MISFED, local current components can be investigated by extracting local transmission mechanisms on an atomic scale. Local charge transmission can be expressed as lines in the direction of the chemical bonds between the atoms, and these lines are referred to as transmission pathways. The thickness and the colour of these lines represent the magnitude of the local charge transmission. Transmission pathways were calculated for the device in Fig. 2.4(a) under reverse bias (-1V) and forward bias (+1V), and are shown as 3D plots in Figs. 2.4(b) and 2.4(c) respectively (calculation details are discussed in the methods section). As expected, under the forward bias case, which is shown in Fig. 2.4(c), continuous transmission pathways through the channel are clearly observed allowing the forward conduction of current through the channel.

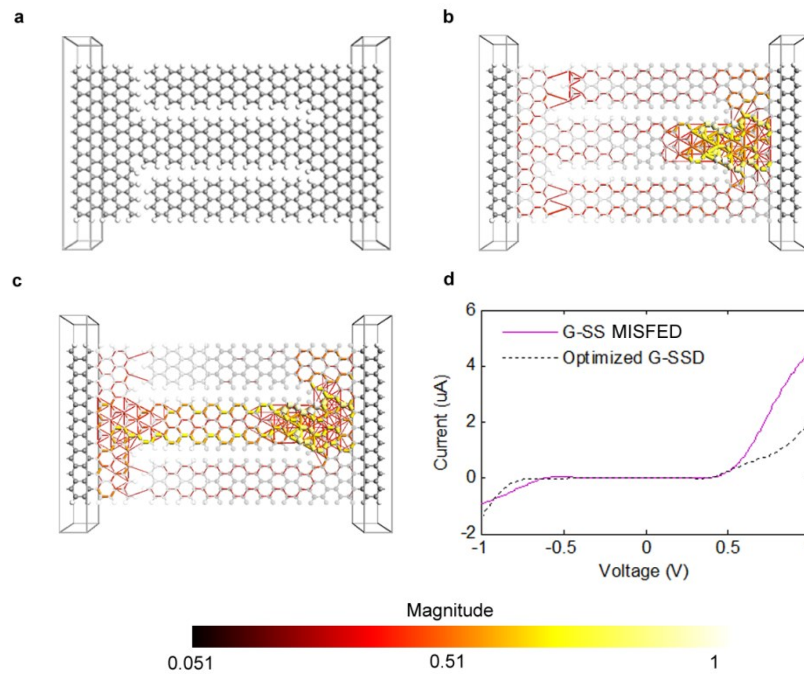

Figure 2.4 | Transport characteristics of a G-SS MISFED. (a) The structure of the simulated G-SS MISFED. (b) A transmission pathways plot of the device in a under reverse bias (-1 V) showing no continuous conduction through the channel and demonstrating how the channel is pinched-off by the field-effect applied through the side gates. Weak but continuous tunneling can be seen across the vertical insulating trenches. This is illustrated by the continuous path of red lines along the edges of the side gates and through the vertical insulating trenches. (c) A transmission pathways plot of the device in a under forward bias (1 V) showing continuous conduction through the channel, which is illustrated by the yellow lines along the edges of the channel. The color of a line resembles the magnitude of the local transmission component along a bond according to the color bar at the bottom of the figure. In (b) and (c) the atoms and the bonds in the central region of the device geometry are drawn with 80 % transparency to allow better visualization of the transmission pathways. (d) I-V characteristics of the G-SS MISFED in (a) (purple curve) compared with the I-V characteristics of the optimized G-SSD of Fig. 2.2(e) (dotted black curve), showing the superior performance of the G-SS MISFED.

On the other hand for the reverse bias case it can be clearly observed from Fig. 2.4(b) that there are no continuous transmission pathways through the channel, and this confirms that the reverse conduction through the channel is greatly suppressed, if not completely blocked. Figure 2.4(b) confirms the strong effect that the applied field has on controlling the channel's conductance, and illustrates how it leads to the channel's pinch-off, which prevents reverse conduction through it.

However, Fig. 2.4(b) indicates some continuous transmission pathways through the vertical insulating trenches, suggesting a flow of reverse tunnelling current through

these trenches. This tunnelling current explains the flow of reverse current through the device under a reverse bias, as observed in Fig. 2.4(d).

2.2.3 Optimization of Device Dimensions

In order to suppress the unwanted tunnelling current through the vertical insulating trenches, these trenches can be made wider, resulting in the structure shown in Fig. 2.5(a).

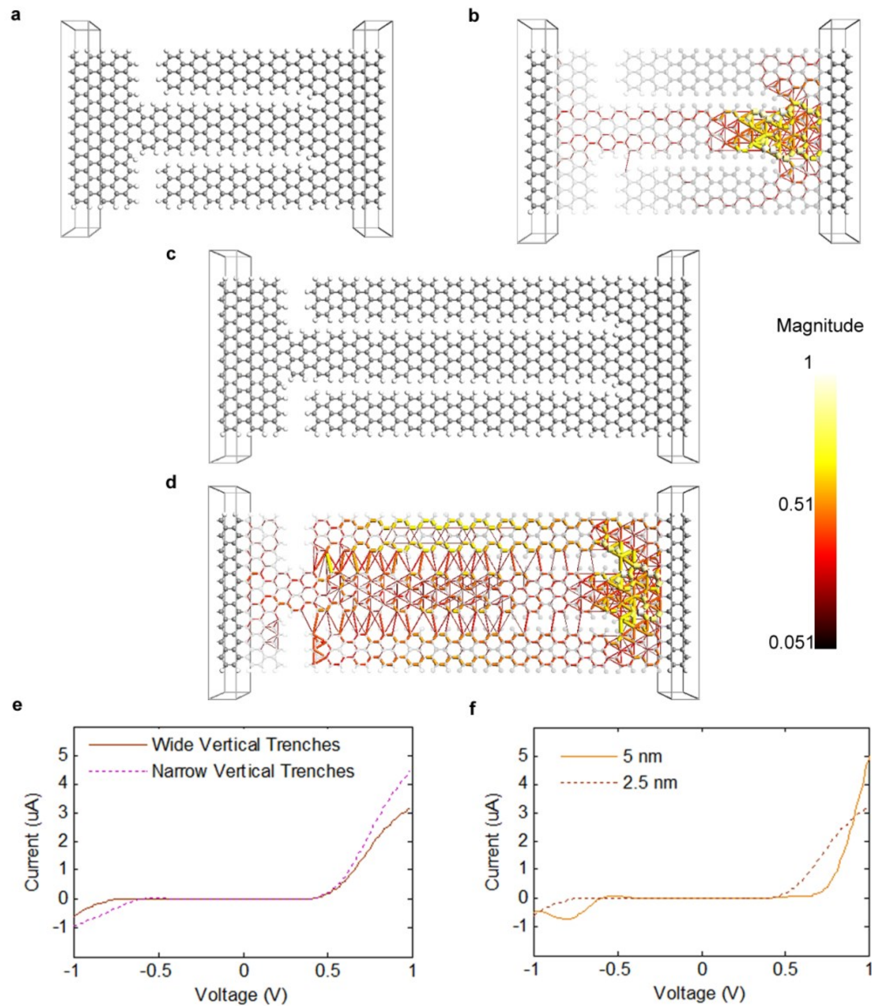

Figure 2.5 | Optimization of G-SS MISFED geometry. (a) A G-SS MISFED structure similar to the one in Fig. 2.4(a) but with wider vertical insulating trenches to suppress tunneling current through them. (b) Transmission pathways plot for the device in (a) under reverse bias (-1 V), showing suppression of tunneling current through the vertical insulating trenches. (c) A G-SS MISFED structure similar to the one in (a) but with a 5 nm long channel, which is twice as long as the 2.5 nm channel in the device of (a). (d) Transmission pathways plot for the device in (c) under reverse bias (-1 V), showing that tunneling current through the horizontal insulating trenches becomes significant when the channel is made twice as long. (e) I-V characteristics of the device in (a) (brown curve) compared with the I-V characteristics of the device of Fig. 2.4(a) (dotted purple curve). (f) I-V characteristics of the device in (c) (orange curve) compared with the I-V characteristics of the device in (a) (dotted brown curve).

Figure 2.5(b) shows the transmission pathways plot of this new geometry under reverse bias (-1V), and confirms the significant reduction of tunnelling current through the vertical insulating trenches as required. Figure 2.5(e) shows how this reflects on the I-V characteristics of the device, confirming the suppression of reverse current, but also resulting in weaker forward current. This may be due to the fact that widening the vertical insulating trenches reduces the gated length of the channel and hence weakens the field effect control over its conductance slightly. The length of the channel in the device under investigation is only 2.5 nm, and making it twice as long should not degrade its performance or speed significantly since the transport through the channel is ballistic [17], but could potentially result in stronger control over its conductance.

The channel of the device is made 5 nm long, forming the geometry shown in Fig. 2.5(c), and its I-V characteristics are shown in Fig. 2.5(f). From Fig. 2.5(f) it is clearly seen that forward conduction is significantly enhanced, and this time it was achieved by increasing the length of the gated region of the channel. However, a new phenomenon occurs at reverse bias, as indicated by the non-linear reverse current flow at negative bias voltages. A transmission pathways plot is used once again in order to explore the origins of this non-linear current component, and is shown in Fig. 2.5(d) for the device under reverse bias (-1V). Figure 2.5(d) indicates that the non-linear current component is due to tunnelling current through the horizontal insulating trenches that isolate the channel from the side gates. It would not be desirable to increase the width of these horizontal trenches, as this would weaken the control that the side gates have over the channel's conductance, and hence a different approach might be needed.

2.2.4 Nitrogen Passivation

The problem of tunnelling current that flows from the side gates to the channel through the horizontal insulating trenches may be addressed through better insulation between the side gates and the channel. Insulation in the proposed G-SS MISFED had been achieved through the etching of L-shaped trenches followed by the passivation of dangling carbon bonds with hydrogen at the edges of the GNRs. It had been proposed earlier that the use of nitrogen for passivation of dangling bonds in GNRs instead of hydrogen, can enhance the performance of GNR field-effect devices such as Graphene Nanopores [66]. This passivation of dangling bonds with nitrogen in GNRs can be achieved by high-power electrical joule heating of the GNRs in ammonia gas [121]. Also interestingly, this process can lead to GNRs with excess free electrons [122].

Based on the above, we investigate a new device structure shown in Fig. 2.6(a), which is similar to the device in Fig. 2.5(c) but with nitrogen, instead of hydrogen, passivation for dangling carbon bonds at the edges of the GNRs. The I-V characteristics of this new nitrogen-passivated Graphene Self-Switching MISFED were calculated and are shown in Fig. 2.6(b). It can be seen from Fig. 2.6(b) that nitrogen passivation greatly suppresses reverse conduction by preventing the non-linear tunnelling current from flowing through the horizontal insulating trenches, as desired. Interestingly, the effect of the excess free electron charge carriers that nitrogen passivation introduces is clearly apparent through the significant enhancement of forward current through the device. After all the optimization steps presented for the Graphene Self-Switching MISFED, the atomically-thin field-effect diode, which has nano-scale dimensions of only 3 nm x 7 nm and a very short channel length of only 5 nm, was able to achieve a very high forward-to-reverse current rectification ratio of 5000, and this is illustrated in Fig. 2.6(c).

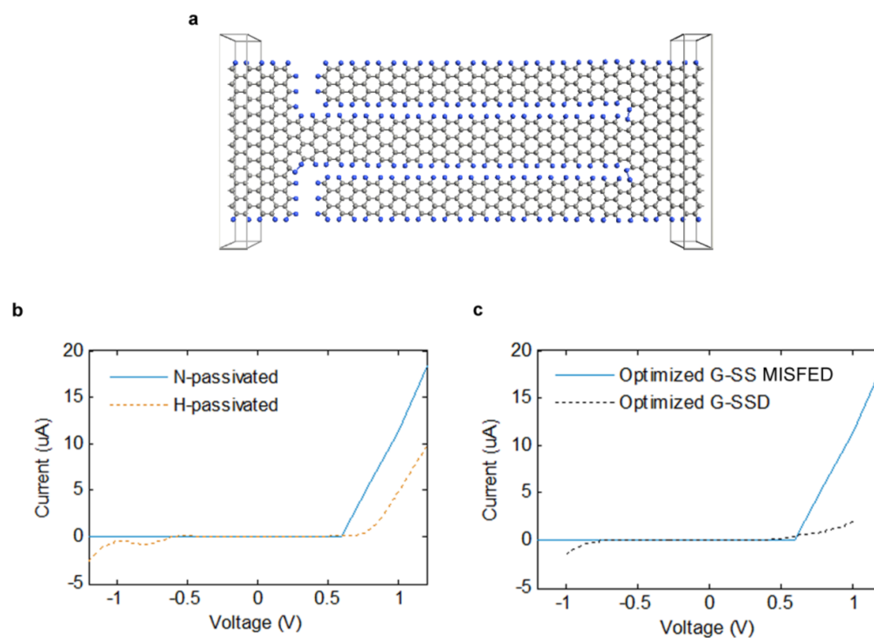

Figure 2.6 | Nitrogen Passivation. (a) Nitrogen passivated G-SS MISFED. The structure of the device is similar to the device in Fig. 2.5(c) but with nitrogen passivation instead of hydrogen. (b) I-V characteristics of the device in (a) (blue curve) compared with the I-V characteristics of the device of Fig. 2.5(c) (dotted orange curve), showing a greatly suppressed reverse current and a greatly enhanced forward current. (c) Comparrison between the I-V characteristics of the optimized G-SS MISFED in (a) (blue curve) and the optimized G-SSD in Fig. 2.2(e) (dotted black curve). The forward-to-reverse current rectification ratio of the optimized G-SS MISFED, within the rectification region of operation (-1.2 V – 1.2 V) reaches up to 5×10^3, representing an enhancement of almost 3 orders of magnitude when compared with the optimized G-SSD (dotted black curve).

Finally, before concluding, it is worth mentioning that following the publication of the findings presented in this study, through a number of research outlets [85, 86] and technical meetings [91, 94], successful experimental realization of G-SSDs with very promising performance was reported [123-125], confirming the predictions made in this chapter. Monolayer G-SSDs were shown to be n-type, as predicted here, while bilayer G-SSDs were shown to be p-type [123]. Furthermore, G-SSDs with a channel width smaller than 20 nm were able to achieve rectification [123], due to the semiconducting behaviour of their narrow device channels as a result of GNR edge roughness, while G-SSDs wider than 20 nm were not able to achieve significant rectification due to the semi-metallic behaviour of their wide channels [124]. Nonetheless, all reported G-SSDs were able to operate as detectors, either through their rectifying behaviour or due to a range of other non-linear effects in their operation such as current saturation [124]. The AC performance of the reported devices compares well with state-of-the-art SSDs, achieving good responsivities and low Noise Equivalent Powers (NEP), a detailed comparison of which is found in [125]. However, this performance may be greatly enhanced through miniaturizing and optimizing a range of device dimensions, specifically the width of the insulating trenches and the width and length of the channel, as suggested by the presented simulations here. Nitrogen passivation may also be pursued in order to enhance the device's performance, as suggested earlier in this chapter.

2.3 Summary

In this chapter, a new class of planar all-Graphene Metal-Insulator-Semiconductor field-effect devices was proposed. The proposed devices are atomically-thin, realized within a single Graphene monolayer. A new type of device, termed a Graphene Self-Switching MISFED (G-SS MISFED), which is a 2D field-effect diode that incorporates metallic gates used to control a semiconducting channel's conductance by means of a self-induced field-effect, was presented. Both the metallic and the semiconducting regions were constructed from a single Graphene monolayer by patterning it into parallel adjacent aGNRs with varying widths. Insulation between the gates and the channel was achieved by nitrogen passivation. Nitrogen passivation resulted in a material with excess free electron charge carriers, which further enhanced the device's performance. The presented results showed that a G-SS MISFED with a channel length as short as 5 nm can achieve a forward-to-reverse current rectification ratio as high as 5000,

representing an enhancement of three orders of magnitude compared to a G-SSD with comparable dimensions. The presented approach can readily be adopted for the realization of other types of all-Graphene MIS based structures and devices, such as MIS capacitors or even three-terminal MIS Field Effect Transistors, within a single Graphene monolayer. These results promise a potential for the realization of atomically-thin all-Graphene integrated circuits, which can be highly flexible, highly transparent and very economical.

2.4 Methods

Transport calculations were conducted on the devices based on the Extended Huckel (EH) [76] method and Non-Equilibrium Green's Function (NEGF) formalism [75] as implemented in Atomistix Tool Kit (ATK) software package [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

Prior to transport calculations, the device geometries were optimized and their coordinates were relaxed using the *Brenner* potential [78] until the forces on individual atoms were minimized to be smaller than 0.05 eV/Å^2. In the nitrogen passivated device structure of Fig. 2.6(a), nitrogen atoms were substituted for hydrogen atoms.

Each device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1 x 10 x 50 for all devices, with 50 sample points along the length (transport direction) and 10 points along the width (induced electric field direction) of the two-terminal structure. The same method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

3 Asymmetrically-Gated Graphene Self-Switching Diodes

This chapter proposes an asymmetrically-gated Graphene Self-Switching Diode (G-SSD) as a new negative differential resistance (NDR) device, and studies its transport properties using Nonequilibrium Green's Function (NEGF) formalism and the Extended Huckel (EH) method. The device exhibits a new NDR mechanism, in which the very small quantum tunnelling current is used to control a much-larger channel conduction current, resulting in a very pronounced NDR effect. This NDR effect occurs at low bias voltages, below 1V, and results in a very high current peak in the µA range and a high peak-to-valley current ratio (PVCR) of 40. The device has an atomically-thin structure with sub-10 nm dimensions, and does not require any doping or external gating. These results suggest a potential for the device in applications such as high frequency oscillators, memory devices, and fast switches.

3.1 Introduction

Negative differential resistance (NDR) [37] devices exhibit interesting current-voltage (I-V) characteristics that result in a non-ohmic N-shaped I-V curve. This effect enables a number of important applications, such as high-frequency oscillators [126-129], memory devices [130-132], multi-level logic [38, 133, 134] and fast switches [38, 135], and hence many efforts have been directed towards discovering transport mechanisms that lead to it. The most common transport mechanism that gives rise to an NDR effect is quantum tunnelling, which is present in resonant tunnelling diodes (RTDs) [136] and transistors[137]. Quantum tunnelling can achieve high peak-to-valley current ratios (PVCR), but results in very low peak current densities (PCD) due to the small current that can be transported by it. A high PCD is of great importance, as it determines the amount of power that can be provided by an NDR device.

Other efforts have investigated the use of molecular electronics [138-143] for the realization of an NDR effect, but have also faced the challenge of limited PCD values and the difficulty of integration with electronics. Recently, Graphene has become of interest for the realization of NDR devices [144-153] due to its unique electronic properties [5, 11] including its high breakdown current density [154]. A new NDR mechanism based on the ambipolar behaviour of Graphene field-effect transistors (FETs) has been reported [155], but although such a transport mechanisms can offer an NDR effect with a high PCD value, the effect is not very pronounced and is not able to provide a high PVCR comparable to that achieved by means of quantum tunnelling effects.

This chapter proposes a new Graphene nanodevice that can achieve an NDR effect based on a new mechanism that utilizes the quantum tunnelling effect in controlling a much larger conduction mechanism; conventional carrier transport through a channel. Based on this, the proposed nano-device is able to achieve a high peak current value in the µA range, while still achieving a high PVCR. The device is based on the Graphene Self-Switching Diode [91] (G-SSD), shown in Fig. 3.1, but enhances it by exploiting a unique property of armchair Graphene nanoribbons (aGNRs) related to their widths.

Armchair Graphene Nanoribbons are generally semiconducting, with varying bandgaps depending on their width [120]. At certain widths, this band gap becomes vanishingly small making the aGNRs almost metallic, and this occurs at widths of $3p+2$ carbon atoms, where p is an integer. Using this property, an enhanced version of a G-SSD,

named a Graphene Self-Switching Metal-Insulator-Semiconductor Field-Effect Diode (G-SS MISFED) was proposed in chapter 2 earlier , in which the side-gates that are usually semiconducting aGNRs (Fig. 3.1(a)), are metallic (Fig. 3.1(b)). This allowed stronger field-effect control over the channel's conductance, and achieved enhanced rectification. In this chapter, a new NDR device that also exploits this unique property of aGNRs is proposed, but differs from a G-SS MISFED in the fact that it has asymmetrical aGNR side-gates with different widths; one is semiconducting, while the other is metallic (Figs. 3.1(c) and 3.1(d)). These asymmetrical side-gates are the reason for the presence of this new NDR mechanism within this device. This new NDR mechanism is investigated by studying the device's transport properties using Nonequilibrium Green's Function (NEGF) and the Extended Huckel (EH) method.

The next section describes the used calculation method, while the following section presents the results that show the presence of this NDR effect within the device and then discusses a physical understanding of the mechanism that leads to it and the experimental feasibility of realizing the devices. Finally the conclusions are summarised in the last section.

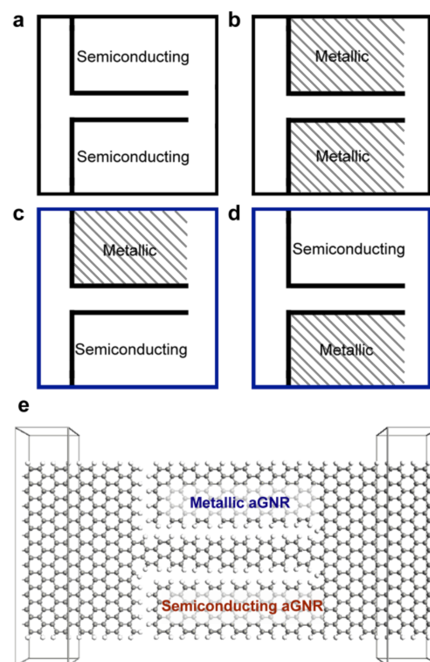

Figure 3.1 | An illustration of different types of Graphene Self-Switching Diodes that differ in their side gates. (a) Symmetrical semiconducting side-gates. (b) Symmetrical metallic side-gates (MISFED). (c) and (d) Asymmetrical side-gates (NDR Device). The shaded regions resemble metallic aGNRs, while the unshaded regions resemble semiconducting aGNRs. (e) The device structure of the simulated asymmetrically gated G-SSD after optimization, with labels to distinguish the metallic gate from the semiconducting gate.

3.2 Results and Discussion

3.2.1 Reverse Bias NDR Effect

Based on the previously proposed concept, an asymmetrically-gated G-SSD was constructed and relaxed according to the optimization method described in the methods section (section 3.4), and is shown in Fig. 3.1(e). The metallic and semiconducting side gates in the device were aGNRs with widths of 8 and 7 carbon atoms, respectively, while the semiconducting channel was an aGNR with a width of 4 carbon atoms. All dangling bonds at the edges were passivated with hydrogen. Using the calculation method described in the methods section (section 3.4), the I-V characteristics of the device were calculated and are shown in Fig. 3.2(a). As the figure suggests, the device exhibits a clear NDR effect in the reverse bias region. The NDR region shows a noticeable peak-to-valley transition that gives rise to the NDR effect, which results in the observed N-shaped curve. A plot of the differential conductance plotted against the bias voltage for the device is shown in Fig. 3.2(d), and further confirms the presence of this NDR region, where the differential conductance drops below zero.

Transmission spectrum plots for the device at the peak and the valley of the reverse bias NDR region are shown in Figs. 3.2(b) and 3.2(c) respectively. The two plots suggest that the decrease in current after the peak in the I-V curve may be attributed to the suppression of the transmission peak that lies within the bias window of the transmission spectrum plots. In order to investigate the origins of the NDR effect, transmission pathways within the device were calculated, based on the calculation method mentioned in the methods sections (section 3.4). Transmission pathways within the device near the peak (-0.4 V) and near the valley (-0.6 V) of the reverse bias NDR region were calculated, and are plotted in Figs. 3.2(e) and 3.2(f) respectively.

At the peak, in Fig. 3.2(e), it is observed that there are no transmission pathways through the channel, as is expected from a G-SSD. This is because the negative voltage applied to the channel by the side gates depletes the channel from charge carriers and pinches off the channel. It is also shown that conduction occurs due to quantum tunneling current from the side gates to the left terminal of the device through the vertical insulating trenches. In a standard G-SSD it is desirable to eliminate this unwanted leakage current, while here it provides the mechanism for conduction at the peak of the NDR effect. It is noted that the transmission pathways in the metallic side-gate are larger than those in the semiconducting side-gate.

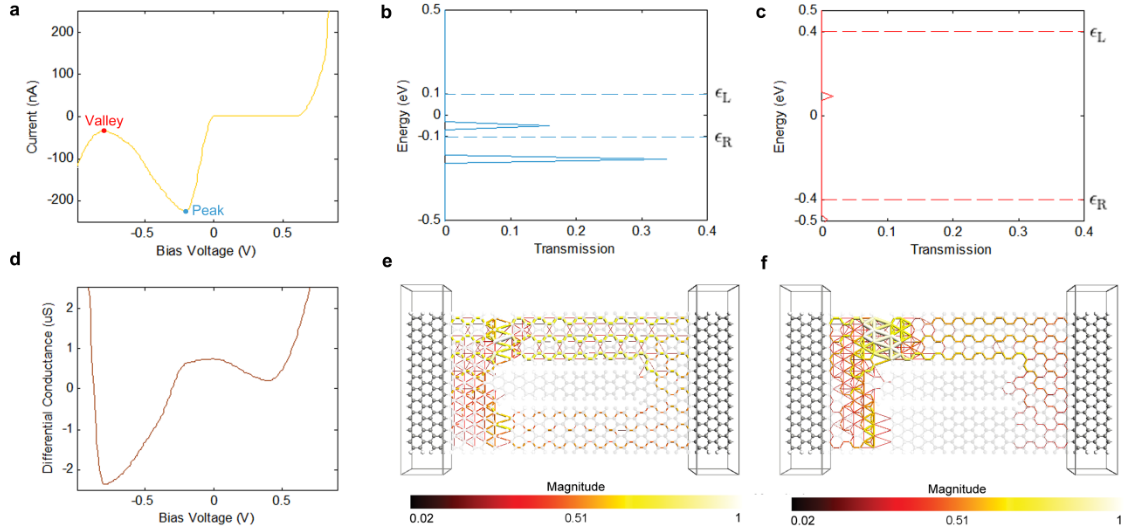

Figure 3.2 | Reverse bias NDR effect in an asymmetrically gated G-SSD. (a) I-V Characteristics of the simulated asymmetrically-gated G-SSD of Fig. 3.1(e). (b) Transmission spectrum of the device at the peak (blue continuous line) and (c) the valley (red continuous line) of the reverse bias NDR region within the device's I-V curve (dotted lines show the bias window). (d) Differential conductance plotted against bias voltage for the device. (e) Transmission pathways plots for the device near the peak and (f) near the valley of the reverse bias NDR region (the central region of the device in both plots was drawn with 90% transparency in order to clarify the visualization of the transmission pathways).

As the reverse bias voltage is increased, the transmission pathways through the semiconducting side gate disappear, preventing the flow of quantum tunnelling current from it into the left terminal of the device, as shown in Fig. 3.2(f). This result suggests that the suppression of this tunnelling current from the semiconducting side gate is the reason for the decrease in the current after the peak and the presence of the NDR effect. This may be explained by the fact that the increased negative voltage applied to the metallic side gate induces a greater electric field that does not only deplete the semiconducting channel from charge carriers, but further extends this effect to the semiconducting side gate, depleting it also from charge carriers, and hence preventing any conduction through it and suppressing the tunnelling current component due to it.

3.2.2 Forward Bias NDR Effect

In order to verify the presence of this NDR effect in larger asymmetrically-gated G-SSDs, a larger device structure was constructed and relaxed according to the optimization method described in the methods section (section 3.4). The device structure is shown in Fig. 3.3(a).

The device has a semiconducting aGNR channel with a width of 6 carbon atoms. The semiconducting side gate is an aGNR with a width of 19 carbon atoms, while the metallic side gate is an aGNR with a width of 17 carbon atoms. Transport calculations were conducted on the device structure to obtain its I-V characteristics and its differential conductance plot, and these are shown in Figs. 3.3(b) and 3.3(c) respectively.

The I-V curve of the larger device is shown in Fig. 3.3(b) and looks qualitatively different than that of the smaller device in Fig. 3.2(a). A forward bias NDR effect occurs and is greatly enhanced, to the extent that the reverse bias NDR effect seems to be negligible compared to it. A closer look at the reverse bias region, shown in the inset of Fig. 3.3(b), confirms the presence of the reverse bias NDR effect, but here the peak current value is at least 2 orders of magnitude smaller than that of the forward bias NDR effect. This suggests that the NDR mechanism in forward bias is driven by a different transport mechanism.

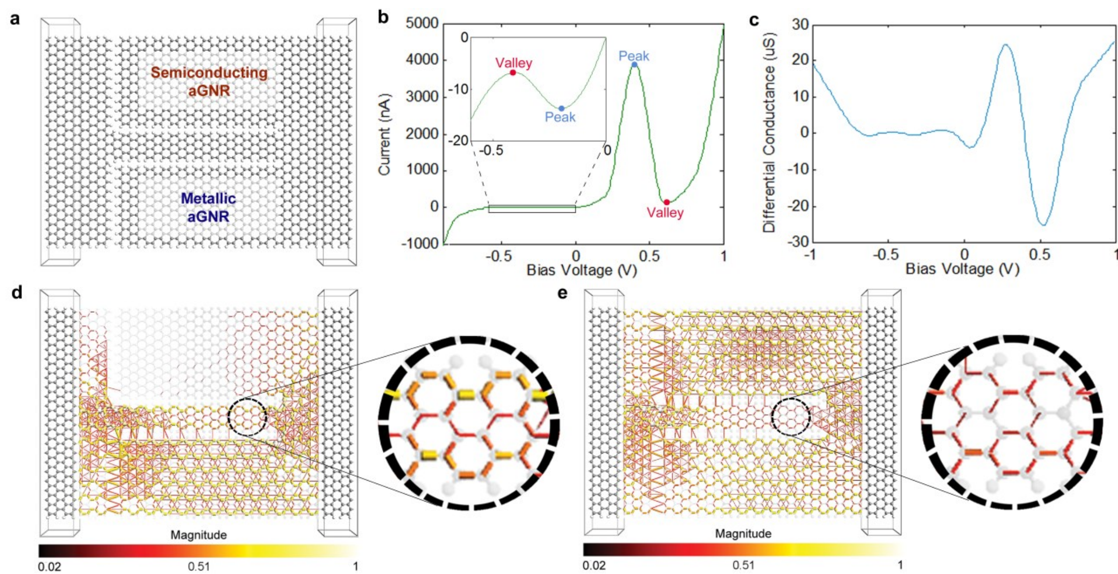

Figure 3.3 | Forward bias NDR effect in an asymmetrically gated G-SSD. (a) The device structure of the larger simulated asymmetrically-gated G-SSD after optimization, with labels to distinguish the metallic side-gate from the semiconducting side-gate. (b) I-V Characteristics of the device. (c) Differential conductance plotted against bias voltage for the device. (d) Transmission pathways plots for the device at the peak and (e) the valley of the forward bias NDR region of the device's I-V curve (the central region of the device in both plots was drawn with 90% transparency in order to clarify the visualization of the transmission pathways). Sub-figures (d) and (e) include a zoomed-in portion of the channel in order to highlight the suppression of the transmission pathways in it from the peak to the valley point.

In order to understand the origins of this new transport mechanism that gives rise to the enhanced forward bias NDR effect, the transmission pathways for the device at the peak and at the valley of this forward bias NDR region were calculated using the previously mentioned methods, and are plotted in Figs. 3.3(d) and 3.3(e) respectively.

At the peak, Fig. 3.3(d) suggests that tunnelling current tunnels from the metallic side-gate and not from the semiconducting side-gate, however, the channel shows continuous transmission pathways lines, some with values close to unity (illustrated by the yellowish colour of the lines), suggesting that the channel is open and is strongly conducting, unlike the reverse bias case. The channel here is wider than that of the smaller device and hence it is expected that it will have a smaller threshold turn-on voltage. This conduction through the channel would dominate the total current, as tunnelling current is much smaller than conduction current, and hence explains the very high peak current value of 4 μA at a very small bias voltage of only 0.4 V, which cannot be due to tunnelling current only. On the other hand, after the bias voltage is increased to 0.6 V reaching the valley point, Fig. 3.3(e) suggests that the semiconducting side gate starts to tunnel current. However, this does not explain the sudden drop in current down to 100 nA (2.5 % of the peak).

A closer look at the figure shows that when both side gates tunnel simultaneously, the transmission pathways through the channel are significantly suppressed, especially towards the right end close to the right electrode (as highlighted by the zoomed-in portions of Figs. 3.3(d) and 3.3(e)), suggesting that the channel conduction current, which dominates the total current, might have been greatly suppressed. This explains the reason for the sudden drop in current flow through the device, which gives rise to the pronounced positive bias NDR effect. The peak-to-valley current ratio (PVCR) achieved by this new NDR mechanism reaches a high value of 40.

3.2.3 New NDR Mechanism

In order to understand this new NDR mechanism, which occurs in forward bias, a discussion of the operation principle of the device under forward bias is presented, and is clarified through the illustrations in Fig. 3.4. The four illustration show the device's operation under no bias (Fig. 3.4(a)), at the positive peak point (Fig. 3.4(b)), within the NDR region (Fig. 3.4(c)) and at the positive valley point (Fig. 3.4 (d)).

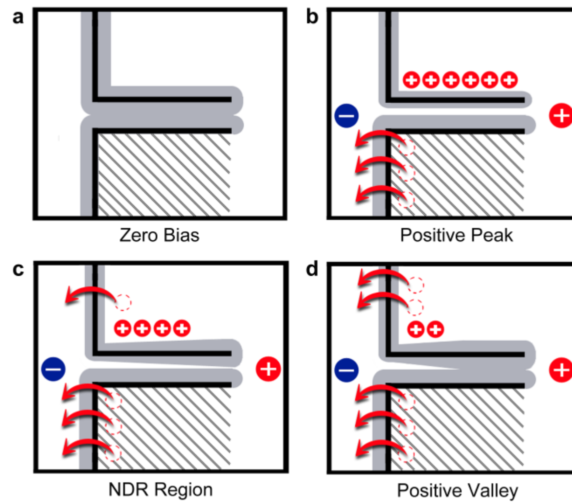

Figure 3.4 | Schematic illustrations of the new NDR mechanism in asymmetrically-gated G-SSDs, illustrating how the asymmetrical tunnelling mechanism affects the opening and closure of the channel. The sub-figures in increasing positive bias voltage order show the device (a) with no bias voltage applied, (b) at the peak current point, (c) in the region between the peak and the valley current points (the NDR region) and (d) at the valley current point. In all sub-figures, the shaded side-gate resembles the metallic side-gate.

With no applied bias across the device, the semiconducting channel would have natural depletion regions at the edges of the insulating trenches due to repulsion between electrons on either side of the trench [55]. In SSDs these depletion regions are generally small, but since the channel in our device is narrow, it is expected that these depletion regions would have the channel completely pinched-off [55, 59], even with no bias voltage applied, as illustrated in Fig. 3.4(a). However, when a positive bias is applied across the device, it is expected that positive charges would start to accumulate at the edges of the insulating trenches inside the side-gates. However, since the metallic gate does not have any depletion regions within it, positive charges are able to tunnel through the insulating trenches from it earlier than from the semiconducting side gate, which does have depletion regions extending in it. This tunnelling current from the metallic side-gate provides a discharge path for holes in it, and hence holes do not accumulate, contrary to the semiconducting side-gate case, where positive charges begin to accumulate near the trench. These positive charges attract electrons on the other side inside the channel, and hence narrow the depletion regions, eventually opening up the channel. This effect is illustrated in Fig. 3.4(b). This explains what happens at the positive bias NDR peak, where the channel is open due to the accumulation of positive

charges within the semiconducting side-gate, and hence conduction occurs through this open channel, resulting in a large current in the μA range.

As the bias voltage is further increased, the bias voltage becomes high enough for the holes accumulated in the semiconducting side-gate to also begin tunnelling across the vertical insulating trench and into the left terminal of the device, providing a discharge path for the accumulated positive charges inside the semiconducting side gate. This discharge allows the channel to return back towards its depleted state, as illustrated in Fig. 3.4(c). As the channel is depleted, the current flow through it is suppressed, and this causes the drop in the overall current through the device during the NDR region (the region between the peak and the valley current points).

Increasing the bias voltage further, increases the tunnelling current from the semiconducting side-gate, discharging more of the accumulated positive charges at the trenches, and allowing the channel to become more depleted, until it is completely pinched-off again, as illustrated in Fig. 3.4(d). At this point the current through the device reaches the valley point. Any further increase in bias voltage afterwards results in an increase in the overall current through the device because it would be dominated by tunnelling current through the insulating trenches.

Figure 3.5 summarizes the overall operation of the device under forward bias by mapping the illustrations of Fig 3.4 on to the forward bias I-V curve of Fig. 3.3(b).

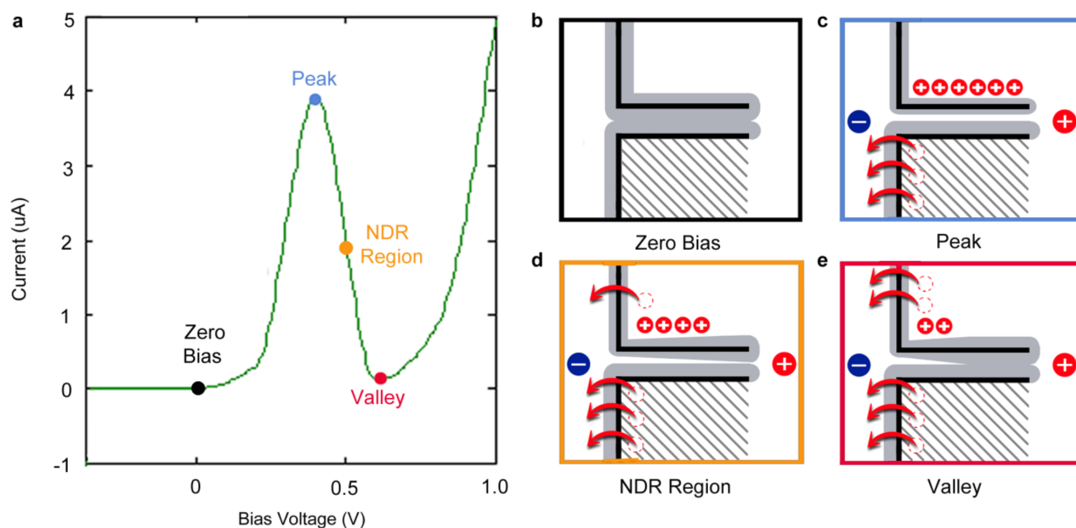

Figure 3.5 | Overall operation of the device under forward bias. (a) A zoom-in at the forward bias I-V curve of Fig. 3.3(a). (b), (c), (d) and (e) The four illustrations that were shown previously in Fig. 3.4, for the device's operation under no bias, at the peak point, during the NDR region and at the valley point respectively.

In order for this NDR effect to take place, the threshold voltage of the device (the voltage at which the channel opens up and starts to conduct) should be less than the onset voltage of tunnelling current from the semiconducting side-gate. This explains why this enhanced forward bias effect was not observed for the device of Fig. 3.1(e), which had a narrow channel and hence a high threshold voltage, but was observed for the device of Fig. 3.3(a), which had a wider channel and hence a lower threshold voltage.

3.2.4 Experimental Feasibility

Asymmetrically-gated G-SSDs require the concurrent realization of semiconducting and metallic GNRs in order to achieve asymmetrical gating. This can be achieved through tuning the bandgap of the GNRs by varying their widths. At the atomistic scale, GNRs need to have smooth edges to achieve precise control and effective tuning of their bandgap. This has proven to be a challenging task. However, recent work has shown promising results towards achieving this goal [51, 109, 113, 114, 119, 156, 157] where the experimental fabrication of Graphene Nanoribbons (GNRs) with smooth edges has been reported [119, 156, 157]. Other methods, using Helium Ion Beam lithography [52-54] and single-atom catalyst chiselling [51], are also promising candidates for the fabrication of GNRs with smooth edges.

In addition to the methods described above, a photo lithographic method, more conducive to mass fabrication, is also possible. This approach is based on the fact that photo lithographically etched GNRs are always semiconducting when made narrower than 20 nm in width, due to their edge roughness, and are always semi-metallic when made wider than 50 nm in width [120, 158]. Based on this concept, Asymmetrically-gated G-SSDs can be realized without the need for GNRs with perfect edges, given that the semiconducting channel and side-gate are lithographically defined narrower than 20 nm, while the metallic side gate is lithographically defined and wider than 50 nm.

3.3 Summary

In summary, this chapter presented a new type of Graphene nanodevice, based on an asymmetrically-gated self-switching diode geometry, which achieves an NDR effect based on a new mechanism that allows very high peak current values, while still achieving a significant peak-to-valley current ratio. The calculated I-V characteristics of the device suggested the presence of two NDR effects, one in reverse bias and the other

in forward bias, and the origins of these two effects were investigated using transmission pathways mapping within the device. It was found that the reverse bias NDR effect is due to asymmetrical tunnelling from the asymmetrical side-gates, while the forward bias NDR effect arises due to a different mechanism. In this mechanism, the asymmetrical tunnelling current from the side-gates is used to control a much larger conduction current through the channel, resulting in a much more pronounced effect with a peak current value two orders of magnitude higher than that attributed to tunnelling current only. The results show a calculated peak-to-valley current ratio (PVCR) of 40 for an atomically-thin device that can be realized within a single aGNR and with sub-10 nm dimensions.

3.4 Methods

Transport calculations were conducted on the devices based on the Extended Huckel (EH) [76] method and Non-Equilibrium Green's Function (NEGF) formalism [75] as implemented in Atomistix Tool Kit (ATK) software package [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

Prior to transport calculations the device geometries were optimized and their coordinates were relaxed using the *Brenner* potential [78] until forces on individual atoms were smaller than 0.05 eV/Å^2 for the device of Fig. 3.1(e), and smaller than 0.5 eV/Å^2 for the much larger device of Fig. 3.3(a).

Each device structures was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1 x 10 x 50, with 50 sample points along the transport direction, and 10 points along the width (induced electric field direction). The same method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

3.4.1 Calculation of the Differential Conductance

The differential conductance, plotted in Figs. 3.2(d) and 3.3(c), was calculated by differentiating the calculated current curve with respect to the bias voltage as:

$$Differential\ Conductance = \frac{dI}{dV} \quad (3.1)$$

4 TUNEABLE GRAPHENE NANOPORES

Solid-state nanopores are promising candidates for next generation DNA and protein sequencing. However, once fabricated, such devices lack tunability, which greatly restricts their biosensing capabilities. This chapter proposes a new class of solid-state graphene-based nanopore devices that exhibit an interesting capability of self-tunability, which is used to control their conductance, tuning it to levels comparable to the changes caused by a translocation of a single biomolecule, enabling high detection sensitivities. The presented quantum simulation results suggest that the smallest amino acid, glycine, when present in aqueous solution can be detected with a 90 % change in conductance, by operating the device near its reverse breakdown voltage. The presented results also suggest that passivating the device with nitrogen, making it an n-type device, greatly enhances its sensitivity, and when operated at the limits of its off-state, makes it highly sensitive to not only the translocation of a single biomolecule, but more interestingly to intramolecular electrostatics within the biomolecule. Sensitive detection of the carboxyl group present within the glycine molecule, which carries a charge equivalent to a single electron, is achieved with a conductance change that also reaches as high as 90 %. The presented findings suggest that tuneable graphene nanopores, with their capability of probing intramolecular electrostatics, could pave the way towards a new generation of sequencing devices.

4.1 Introduction

Nanopore sensors [159, 160] are promising candidates for next generation [43-45] DNA[48, 160] and protein [46, 161, 162] sequencing, enabled by their single-molecule detection capabilities [48-50, 159, 163-166]. Nanopores can be natural [159, 165], present within protein structures, or artificial [164], drilled within solid-state materials. Solid-state nanopores [161-163, 167-177] benefit from robustness and durability [160], mass production [164, 170, 178] and integration with electronic readout and processing circuitry [179] and hence have attracted great interest in the past decade.

When a DNA strand or an amino acid chain in a protein molecule translocates through a nanopore, individual building blocks of its structure, usually nucleobases or amino acids, are detected in order to decipher their overall sequence, providing very valuable biological information that can be used in genetic as well as diagnostic applications [43, 46, 47, 160]. This detection mechanism can be based on measuring the blockage of ionic current travelling through the nanopore, or measuring the modulation of transverse conduction current in the device incorporating the nanopore [65, 66, 179], in response to the translocation of an individual nucleobase or amino acid. The latter method enjoys the advantage of easier electronic readout due to higher current levels, but suffers from low sensitivity, due to the small changes in conductance caused by the translocation of a single biomolecule, compared to the originally high conductance of the device.

Solid-state nanopores can be realized using a number of different materials, however, graphene [61-67, 180-183], the first two-dimensional material to be isolated [3], offers a great advantage due to its single atomic thinness [62], which is comparable to the size of single nucleobases or small amino acids [62], and hence makes it more likely to be affected by their translocation than other types of bulk materials. Once constructed, graphene nanopores, similar to other types of nanopores, cannot be controlled or tuned, limiting their ability to distinguish between different amino acids, let alone be able to detect their intramolecular electrostatics. Being able to detect intramolecular electrostatics can be a very powerful tool for distinguishing between different amino acids and moreover for detecting chemical modifications [175, 184] or structural conformational changes [185] they undergo. In this chapter, the realization of a tuneable highly sensitive graphene nanopore biosensor [92] is proposed through the incorporation of the nanopore within the channel of another self-tuneable device [55]; the self-switching diode (SSD) [59, 85, 86].

This study represents the first proposal for the application of a SSD-based structure in a biosensing application. The transport properties of the proposed tuneable nanopore device are studied using quantum simulations based on Non-Equilibrium Green's Function (NEGF) formalism[75] and the Extended Huckel (EH) method [76]. The effect of the translocation of the smallest amino acid, glycine, through the nanopore on the device's conductivity is investigated. The presented results show that the device acts as a highly sensitive biosensor being able to selectively detect the translocation of a single glycine molecule in aqueous solution. More interestingly, when the device is passivated with nitrogen, making it an n-type device [85, 121], the device is able to not only detect the translocation of the glycine molecule, but also some of its structural features, namely its carboxyl group, through probing its intramolecular electrostatics.

The following results and discussion section describes the structure and operation principle of the proposed device and investigates its sensitivity to glycine detection.

4.2 Results and Discussion

4.2.1 Device Structure

Figure 4.1(a) shows the geometry of a standard graphene nanopore device, while Fig. 4.1(b) shows the geometry of a standard self-switching diode. Figure 4.1(c) shows the proposed tuneable nanopore device, which is a self-switching diode incorporating a nanopore. The channel in a self-switching diode is defined by two L-shaped trenches that are etched back-to-back. The conductivity of this channel is controlled by two in-plane side gates that induce an electric field when a bias voltage is applied to the device. This in-plane electric field modulates the distribution of charge carriers within the channel, controlling its conductance. In the proposed device the nanopore through which translocation occurs is incorporated within this channel. The resulting device has two mechanisms of conductance modulation, one driven by amino acid translocation, which cannot be controlled, and one driven by bias voltage application, which can be controlled. The latter mechanism is used for tuning the device's original conductance in order to make it comparable to the conductance change caused by the translocation.

The overall structure of the proposed tuneable graphene nanopore device is shown through the schematic illustrations of Fig. 4.2, presented in top view (Fig. 4.2(a)), perspective view (Fig. 4.2(b)) and side view (Fig. 4.2(c)).

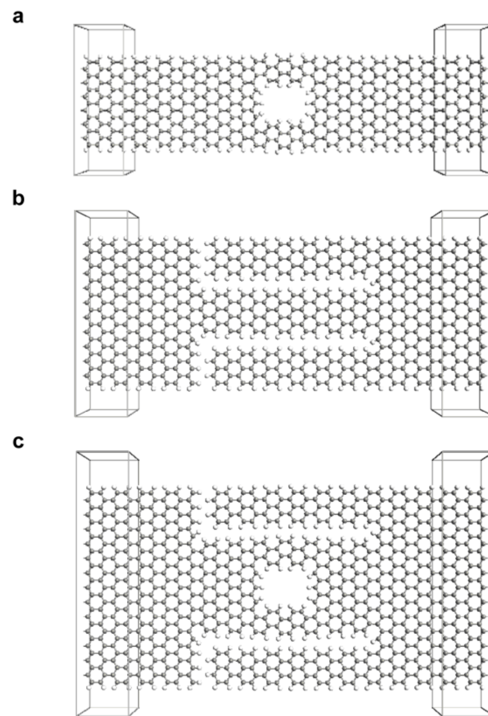

Figure 4.1 | Comparison between standard and tunable graphene nanopores. A standard graphene nanopore is shown in (a) and a standard graphene self-switching diode is shown in (b). A tunable graphene nanopore device, shown in (c), is obtained by incorporating a nanopore, as in (a), within the channel of a graphene self-switching diode similar to the one in (b).

The whole device is realized within a single graphene monolayer, by defining a wide nanoribbon and then etching the two L-shaped trenches back-to-back across the width of the nanoribbon. This leaves a narrow nanoribbon channel, defined by the L-shaped trenches, through which conduction occurs. A hole is created within this channel, defining the nanopore, and then all dangling bonds within the device are passivated. Passivation can be achieved by hydrogen or nitrogen [66, 85, 121], where the latter results in a device with excess free electrons behaving as an n-type device.

The device incorporates two terminals only and does not require a third gate terminal for conductance modulation. Conductance modulation is achieved using the side nanoribbons that are adjacent to the channel of the device, which act as side gates. These side gates are connected to one terminal of the device but are isolated from the other in an asymmetrical geometry that enables the bias voltage to create a potential difference across the channel of the device as well as modulate its conductance at the same time. The side gates are designed to have widths of $3p+2$ atoms, were p is an integer, in order for them to have vanishingly small bands gaps and hence behave as if they were metallic, achieving stronger control over the channel's conductivity [85].

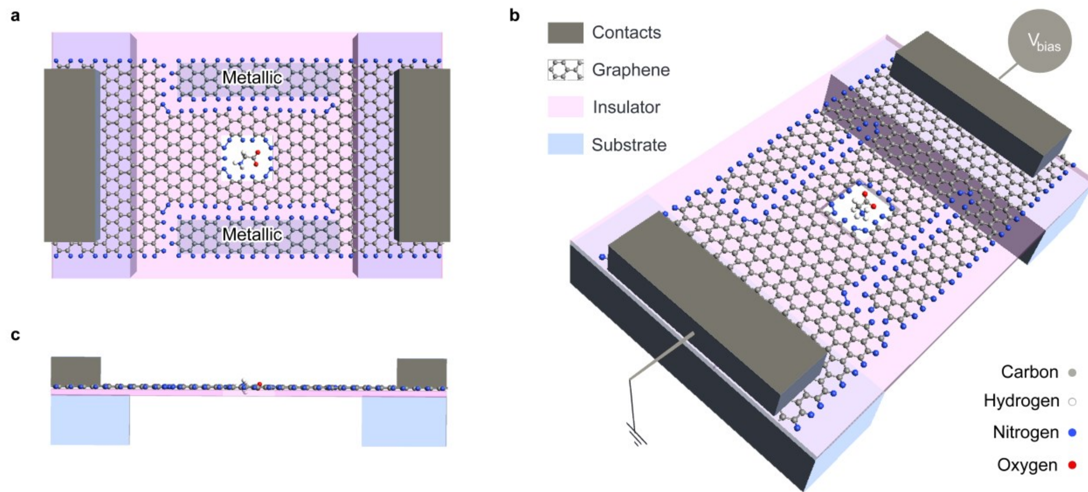

Figure 4.2 | Schematic illustrations of the geometry of a tuneable graphene nanopore, shown in (a) top view, (b) perspective view and (c) side view. The top view illustration (a) shows how the side gates of the device are chosen to have a width of $3p+2$ carbon atoms in order for them to behave as if they are metallic and achieve stronger control over the channel's conductivity. The perspective view illustration in (b) shows the applied bias voltage direction.

The current-voltage characteristics of the device are similar to self-switching diodes, allowing forward conduction under positive bias voltages that are higher than the threshold voltage of the device, while preventing reverse conduction under reverse bias voltages that are lower than the reverse breakdown voltage of the device. Due to the presence of the nanopore within the channel, these two critical voltages, namely forward threshold voltage and reverse breakdown voltage, are expected to occur at lower voltages than in a standard self-switching diode, as will be shown later on, and hence play critical roles in the operation of tuneable graphene nanopore devices.

4.2.2 Hydrogen Passivation

The transport properties of the hydrogen passivated tuneable graphene nanopore device, shown in Fig. 4.1(c), are studied and the effect of the translocation of a single glycine molecule in aqueous solution on them is investigated. Glycine takes the form of a zwitterion when present in aqueous solution [186, 187], having a negatively charged carboxyl (COO^-) group on one side and a positively charged amine (NH_3^+) group on the other, creating a dipole within the molecule. However, this dipole does not affect the overall charge of the glycine molecule, which remains to be neutral. This glycine molecule is incorporated into the nanopore of the device of Fig. 4.1(c), at two different orientations that are 180° apart, shown in Figs. 4.3(b) and 4.3(c). Since glycine is present in aqueous solution, water molecules would also be present, and accordingly the

effect of their translocation through the device needs to be investigated. This is achieved by incorporating the maximum number of water molecules within the device's nanopore, three in this case, as shown in Fig. 4.3(a). The transport properties for the three configurations, as well as the control case of Fig. 4.1(c), in which no translocation occurs, were calculated using Non-Equilibrium Green's Function (NEGF) Formalism and the Extended Huckel (EH) method as implemented in Atomistix Toolkit (ATK) package. Details of the calculation method are discussed in the methods section (Section 4.3).

The current-voltage characteristics of the four configurations are plotted in Fig. 4.3(d). A significant difference is observed between the I-V curves of the four configurations at extreme reverse bias voltages lower than -1 V. This is further highlighted by the zoomed-in regions in Figs. 4.3(e) and 4.3(f). The figures suggest that the translocation of the glycine molecule results in a significant increase in current levels, occurring consistently for both orientations. On the other hand, the translocation of the water molecules does not result in any noticeable change compared to the control case. Looking at the overall I-V curves for a wider bias range, as shown in Fig. 4.4 (a), it is observed that this region, in which a large change in conductance takes places, is near the reverse breakdown voltage of the device.

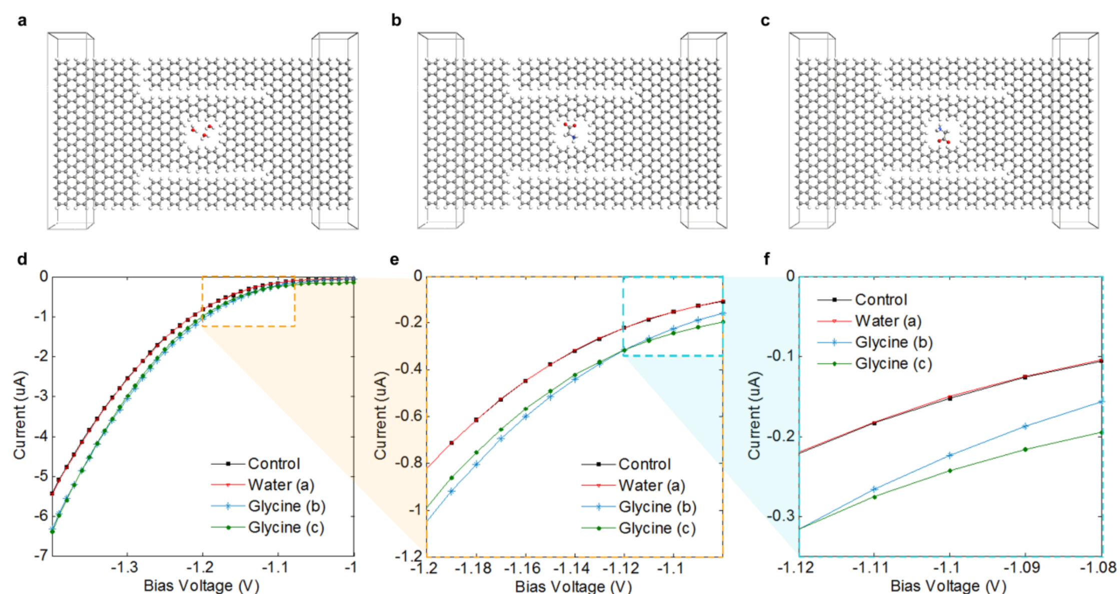

Figure 4.3 | Glycine detection in aqueous solution. Configurations of tuneable graphene nanopores incorporating (a) three water molecules, (b) one glycine molecule and (c) the same glycine molecule titled 180°. The I-V characteristics of the devices in (a), (b) and (c) as well as the device in Fig. 4.1(c) are plotted on the same axes for reverse bias voltages near the reverse breakdown region in (d), zoomed-in near the breakdown point in (e), and zoomed-in furthermore in (f).

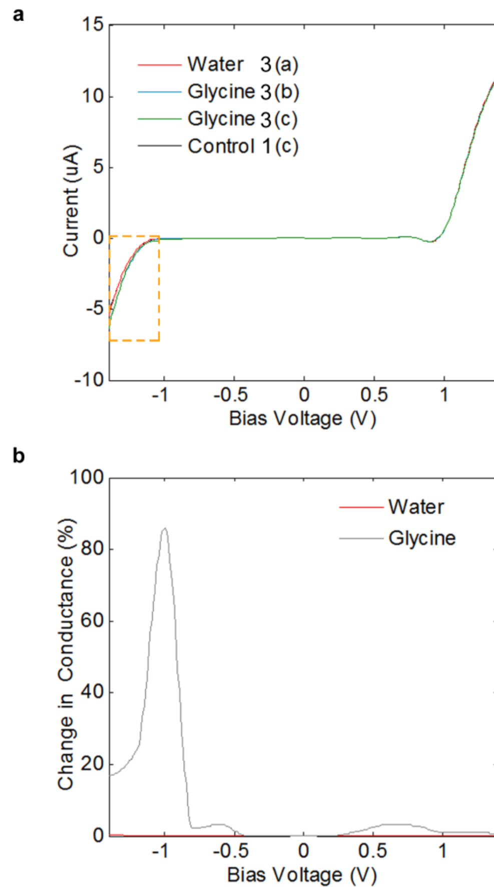

Figure 4.4 | Sensitivity to Glycine Detection. The I-V characteristics of the devices in Fig. 4.1(c) and Figs. 4.3(a), 4.3(b) and 4.3(c), are plotted in (a) across a wide bias voltage range from -1.4 V to 1.4 V. The dotted orange rectangle highlights the portion of the plot in which the device operates in reverse breakdown, which was shown earlier at higher magnification in Fig. 4.3(d). The absolute average change in conductance due to glycine translocation with different orientations (Figs. 4.3(b) and 4.3(c)) – grey curve –, and due to water translocation (Fig. 4.3(a)) – red curve – are plotted in (b) against bias voltage.

In order to quantify the sensitivity of the device to glycine detection, the absolute change in conductance, relative to the control case, was calculated for the two glycine translocation orientations and averaged in order to get an average absolute change of conductance that represents both cases. This is plotted against bias voltage in Fig. 4.4(b), and compared to the absolute change in conductance due to the translocation of the water molecules. It can be clearly seen that the device selectively distinguishes glycine from water molecules. The device's sensitivity is the highest at the reverse breakdown voltage reaching up to a very high value close to 90 %. This value remains relatively high as the device continues to operate deeper into breakdown under negative voltages lower than -1V. The reason for this, as observed from Fig. 4.3(d), is that the presence of glycine within the nanopore seems to result in earlier breakdown. In order to clarify this, a brief illustration of the operation principle of the device under reverse

bias is presented through the schematic illustrations of Figs. 4.5(a) – 4.5(d). As Figs. 4.5(a) and 4.5(b) illustrate, under reverse bias the negative charges that accumulate at the side gates repel electrons within the channel, depleting it from negative charge carriers and preventing current flow through the device. As this negative bias is increased, more negative charges are accumulated near the side gates, eventually resulting in the creation of inversion layers at the edges inside the channel, which are regions with excess positive charge carriers; holes. At this point, the channel, which is meant to be off, breaks down and begins to conduct through positive charge carriers, marking this voltage as the reverse breakdown voltage of the device. The presence of the glycine molecule within the channel seems to shift this reverse breakdown voltage to a lower value, as illustrated through Fig. 4.3(d), resulting in higher current values within the reverse breakdown region during glycine translocation. More detailed discussions of the principle of operation of SSDs is found in earlier work [55, 85, 86].

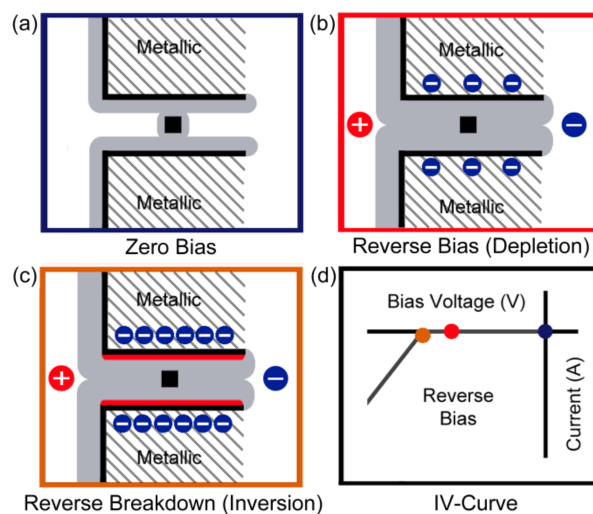

Figure 4.5 | Schematic illustrations of transport mechanisms within the device under reverse bias. At zero bias (a), marked with a blue circle in (d), the device exhibits natural depletion regions surrounding the insulating trenches as well as the nanopore. As the reverse bias voltage is increased (b), marked with a red circle in (d), the channel eventually becomes completely depleted from electrons due to the accumulation of negative charges near the trenches within the side gates suppressing flow of current through the channel. As the reverse bias voltage is increased further (c), marked with an orange circle in (d), an inversion layer of holes begins to form near the trenches within the channel facilitating charge transport within the channel. This is the reverse breakdown point at which current begins to abruptly increase with any further increase in reverse bias voltage. The expected I-V characteristics of a tuneable graphene nanopore device under reverse bias is plotted in (d), with the positions of zero bias, reverse bias and reverse breakdown mapped on the I-V curve with blue, red and orange circles respectively. The grey regions in (a), (b) and (c) represent regions that are depleted from electrons.

4.2.3 Nitrogen Passivation

Passivating a self-switching diode with nitrogen results in an n-type device in which transport is dominated by majority charge carriers, which are negatively charged electrons. It is expected that the presence of excess charge carriers in a tuneable graphene nanopore device would make it more sensitive to electrostatic changes within the nanopore. Accordingly, the device of Fig. 4.1(c) was passivated with nitrogen instead of hydrogen, obtaining the device shown in Fig. 4.6(a). The effect of glycine translocation through the nitrogen passivated device was investigated by placing a glycine molecule within the nanopore of the device. The resulting configuration is shown in Fig. 4.6(c). The I-V characteristics of the two devices of Figs. 4.6(a) and 4.6(c) were calculated and are shown in Fig. 4.6 (b).

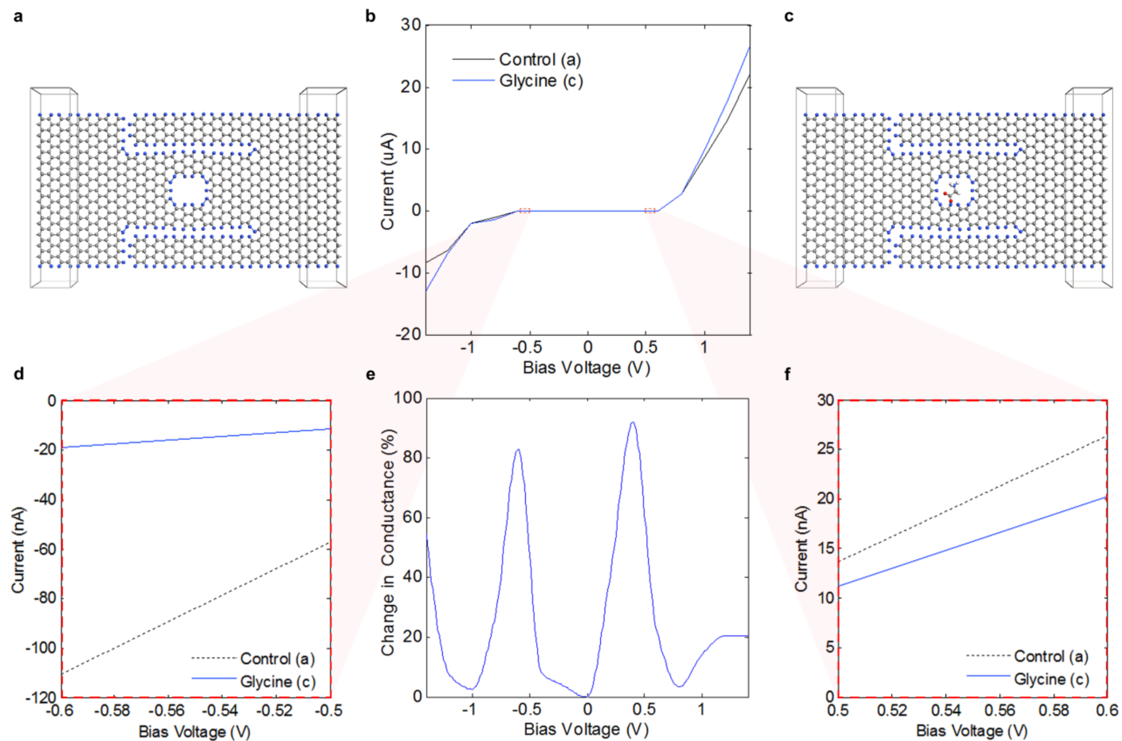

Figure 4.6 | I-V Characteristics of nitrogen passivated tuneable graphene nanopores with glycine translocation. The structures of nitrogen passivated tuneable graphene nanopore devices with (a) no translocation and (c) glycine translocation, and their I-V characteristics plotted in (b), with a black curve and a blue curve respectively. The resulting absolute change in conductance due to glycine translocation as in (c) relative to no translocation as in (a), is plotted against bias voltage in (e). The plot shows the presence of two unexpected peaks before the reverse breakdown voltage in reverse bias and before the threshold voltage in forward bias. Zoomed-in plots of the I-V curve of (b) are shown in (d) and (f) covering the bias voltage ranges within which the two unexpected change-in-conductance peaks appear.

The figure shows an enhanced increase in current due to glycine translocation, when compared to the hydrogen passivated device, under both forward and reverse biases. In both regions the change is most noticeable after the threshold voltage and after the reverse breakdown voltage points. This change is quantified through the absolute change in conductance due to glycine translocation, which is plotted against bias voltage in Fig. 4.6(e). The plot suggests relatively high changes at extreme positive and negative voltages reaching close to 50 % under reverse breakdown operation. However, two very high peaks are observed in the plot before the reverse breakdown and before the threshold voltage points of the device, one being in reverse bias (around – 0.6 V) and the other in forward bias (around 0.6 V). Magnified zoomed-in plots of the I-V characteristics near the bias voltages where the peaks appear are shown in Figs. 4.6(d) and 4.6(f) for the reverse and forward bias peaks respectively. Both figures suggest that the change in conductance is a decrease in current rather than an increase, suggesting that this change may be driven by a different phenomenon to the changes taking place at higher voltages.

In order to obtain a deeper insight at the origins of these large changes in conductance, the local transmission pathways within the device were calculated under both reverse (-0.6 V) and forward (0.6 V) biases for the control configuration with no translocation (Fig. 4.6(a)), plotted in Figs. 4.7(a) and 4.7(b) respectively, and for the glycine translocation configuration (Fig. 4.6(c)), plotted in Figs. 4.7(c) and 4.7(d) respectively. Under reverse bias, with no translocation, the channel of the device is closed with no available transmission pathway, and conduction is dominated by tunnelling current through the insulating trenches, as shown in Fig. 4.7(a). Tunnelling current flows from the left electrode, as well as the channel, into the side gates resulting in the small current values in the nA range seen in Fig. 4.6(d). When the glycine molecule translocates through the nanopore (Fig. 4.7(c)) tunnelling current from the channel to the side gate is suppressed from the lower path in the channel which is adjacent to the carboxyl (COO^-) group of the glycine molecule. This not observed for the upper path of the channel which is adjacent to the amine group (NH_3^+). This can be explained by the fact that the carboxyl group is negatively charged and hence repels the negatively charged majority carriers within the channel keeping them away from the trenches and making it more difficult for them to tunnel across to the lower side gate. However, the amine group is positively charged and only repels holes, which are minority carriers in an n-type device and hence do not contribute significantly to the overall conduction.

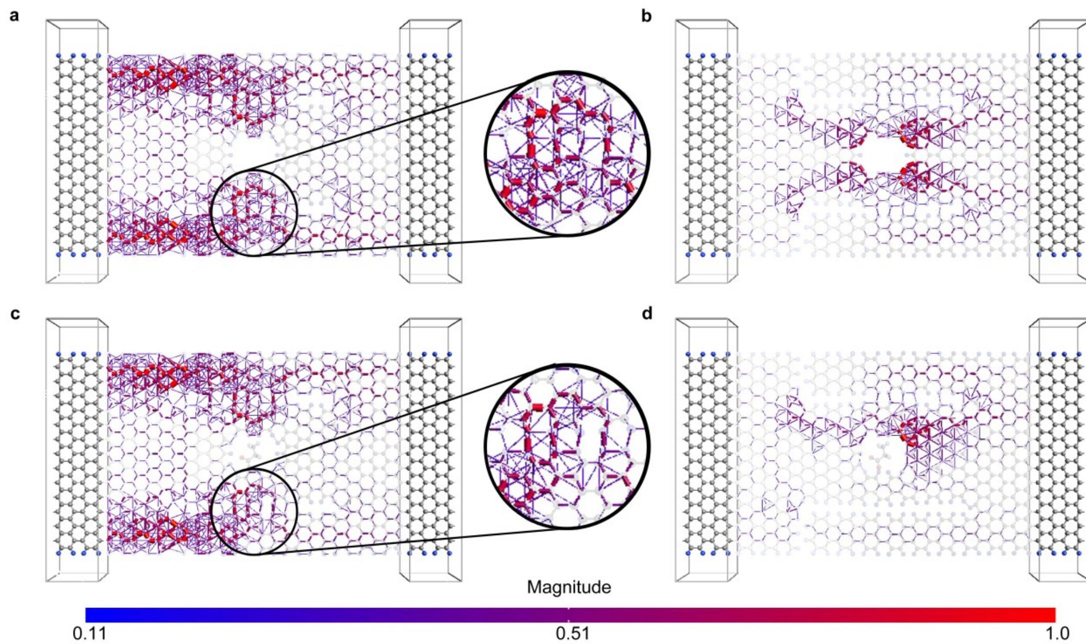

Figure 4.7 | Detection of the carboxyl group within the glycine molecule. Local transmission pathways for the nitrogen passivated tuneable graphene nanopore device, with no translocation, under (a) a reverse bias of -0.6 V and (b) a forward bias of 0.6 V, and with glycine translocation under (c) a reverse bias of -0.6 V and (d) a forward bias of 0.6 V. Under reverse bias, the zoomed-in portions of (a) and (c) highlight how the proximity of the carboxyl group to the lower side of the channel, during glycine translocation, suppresses tunnelling that flows from the channel into the lower side gate. Under forward bias, the transmission pathways within the lower side of the channel are greatly suppressed due to the close proximity of the carboxyl group, which is evident through the comparison of (b) and (d). The magnitudes of the transmission pathways are according to the colour bar scale at the bottom of the figure.

Under forward bias, with no translocation (Fig. 4.7(b)), the channel begins to open up showing continuous transmission pathways along the length of the channel consistently for both the upper and lower paths. When the glycine molecule translocates through the pore (Fig. 4.7(d)), the lower path is completely blocked with no available transmission pathway, reducing the conduction current within the device (Fig. 4.6(f)). The upper path is unaffected once again, consolidating the hypothesis that the conductance change is only due to the negatively charged carboxyl group, which repels electrons away from the lower path of the channel depleting it from charge carriers and preventing conduction through it. The absolute change in conductance that results due to the carboxyl group is very high reaching values above 80 % for both the reverse and forward bias cases (Fig. 4.6(e)). These findings suggest that the nitrogen passivated tuneable graphene nanopore device is highly sensitive to intramolecular electrostatics to the extent that it is able to detect an intramolecular structural feature within the glycine molecule carrying charge equivalent to a single electron; a negatively charged carboxyl

group. It is intuitive that larger negative charges would result in larger changes in conductance, while it is postulated that a p-type device dominated by holes, would also be able to sensitively detect structural features that carry positive charges, similar to the amine group in glycine.

Finally it is important to clarify that while the process of biomolecule translocation through the nanopore is a dynamic process; all simulations presented in this chapter were based on a static quantum mechanical (QM) simulation approach. Accordingly, the investigation of different extreme orientations of the glycine molecule translocation would be important in order to validate the reliability of the detection mechanism. This is currently being researched; and promising preliminary results have already been reported [84]. However, further work that can combine the used static QM approach with a dynamic molecular dynamics (MD) simulation approach [188] may prove to be efficient and reliable, as it may take into account other possible orientations of the glycine molecule translocation, including out-of-plane orientations that were not addressed here as well as the possibility of a hydrated configuration with a hydration water shell [189], to add to a range of possible orientations for the translocation of the water molecules and the ionic impurities.

4.3 Summary

In summary, this chapter proposed a new class of tuneable nanopore biosensors, which can be realized completely within a single graphene monolayer. The device's realization requires minimal process steps and results in a highly sensitive biosensor that is able to detect translocation of single biomolecules. This was demonstrated through the detection of the smallest amino acid, glycine, in aqueous solution. It was also shown how nitrogen passivation makes the device an n-type device with negative majority charge carriers, transforming the device into a highly sensitive electrostatic detector that is capable of detecting intramolecular electrostatic effects as small as a negative charge equivalent to a single electron. This was also demonstrated through the highly sensitive detection of the negatively charged carboxyl group in a glycine zwitterion, which modulates the conductance of the device with a very high change in conductance that reaches as high as 90 %. The presented findings suggest a promising potential for the proposed tuneable graphene nanopore biosensors towards the detection of intramolecular electrostatics, which could be an exciting route towards next generation sequencing devices.

4.4 Methods

Transport calculations for obtaining I-V characteristic curves and transmission pathway plots were all based on the Extended Huckel (EH) method[76] and Non-Equilibrium Green's Function (NEGF) formalism[75] as implemented in Atomistix Tool Kit (ATK) software package [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

Prior to transport calculations, the device geometries were optimized and their coordinates were relaxed using the *Brenner* potential [78] until the forces on individual atoms were minimized to be smaller than 0.05 eV/Å^2. In the nitrogen passivated devices of Figs. 4.6(a) and 4.6(c) nitrogen atoms were substituted for hydrogen atoms.

Each device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1 x 10 x 50 for all devices, with 50 sample points along the length (transport direction) and 10 points along the width of the two-terminal structure. The same method was used in previous work[85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

4.4.1 Calculation of Absolute Change in Conductance

The absolute change in conductance, expressed in percentage relative to a controlled case, was calculated in order to quantify the sensitivity of the device to the translocation of different biomolecules, according to the following equation:

$$Absolute\ Change\ in\ Conductance\ (V) = \frac{|I_{trans}(V) - I_{cont}(V)|}{I_{cont}(V)} \times 100 \qquad (4.1)$$

where $I_{trans}(V)$ is the current in the device with the biomolecule positioned within the nanopore, and $I_{cont}(V)$ is the current in the device under the controlled case with no translocation.

5 MONOLAYER MoS_2 SELF-SWITCHING DIODES

This chapter presents a new Molybdenum Disulphide (MoS_2) nanodevice that acts as a two-terminal field-effect rectifier. The device is an atomically-thin two-dimensional Self-Switching Diode (SSD) that can be realized within a single MoS_2 monolayer with very minimal process steps. Quantum simulation results are presented confirming the device's operation as a diode and showing strong non-linear I-V characteristics. Interestingly the device shows a p-type behaviour, in which the flow of reverse current is enhanced while the flow of forward current is suppressed, in contrast to monolayer Graphene SSDs, which behave as n-type devices. The presence of a large bandgap in monolayer MoS_2 results in very strong control over the channel, showing complete channel pinch-off in forward conduction, and this was confirmed with transmission pathways plots. The lack of passivation resulted in large leakage tunnelling current through the insulating trenches; nevertheless, reverse current remained to be 6 times higher than forward current, showing strong p-type rectification. Furthermore, the effect of p-type substitutional doping of sulphur with phosphorus was investigated and showed that it greatly enhances the performance of the device, increasing the reverse-to-forward current rectification ratio more than an order of magnitude, up to a value of 70.

5.1 Introduction

Monolayer Molybdenum Disulphide (MoS_2) is a promising material for two-dimensional electronics. It is similar to Graphene in its hexagonal structure and two-dimensional nature and shares a lot of its interesting electronic and optical properties[68]. Unlike Graphene, MoS_2 has a large bandgap which is very useful for many device applications, especially Field Effect Transistors (FETs) and devices. Due to this large bandgap [72], MoS_2 FETs have been reported to achieve On/Off current ratios of 10^7 [68], and according to theoretical calculations these may reach as high as 10^{10} [190]. This has led to the realization of MoS_2 integrated circuits with very good performance [191].

Furthermore, monolayer MoS_2 has a direct bandgap promising potential for optoelectronics [192], and is considered to be a strong candidate for valleytronics [193]. Also, since MoS_2 performs well as a highly flexible material [194], it opens opportunities for realizing atomically-thin flexible electronics.

One very important advantage of MoS_2 over other two dimensional materials, such as Graphene, is that it can be produced using a wafer scale CVD process on insulating substrates such as SiO_2 [69-71]. This is in contrast to Graphene, which needs to be first grown on a metal and then transferred to an insulating substrate. This property may allow mass production of MoS_2 circuits or integration of MoS_2 devices with CMOS technology. Another very useful advantage of MoS_2 is the fact that it can be doped into both n and p-type [195].

Numerous research efforts have focused on the realization of MoS_2 transistors, however, much less effort has been directed towards the realization of MoS_2 diodes, which are of equal importance. There are many diode architectures with which rectification can be achieved, but one of them stands out to be well-suited for two-dimensional materials due to its completely two-dimensional architecture; the Self-Switching Diode (SSD). Based on this, Graphene Self-Switching Diodes (G-SSDs) had been proposed and showed promising performance [85, 86]. Self-Switching Diodes rectify current based on a field-effect mechanism and hence require a bandgap for strong rectification. Graphene can only have a small bandgap when etched down to narrow nanoribbons, and hence MoS_2, a material with a much larger bandgap, may prove to be more suitable for the practical realization of SSDs.

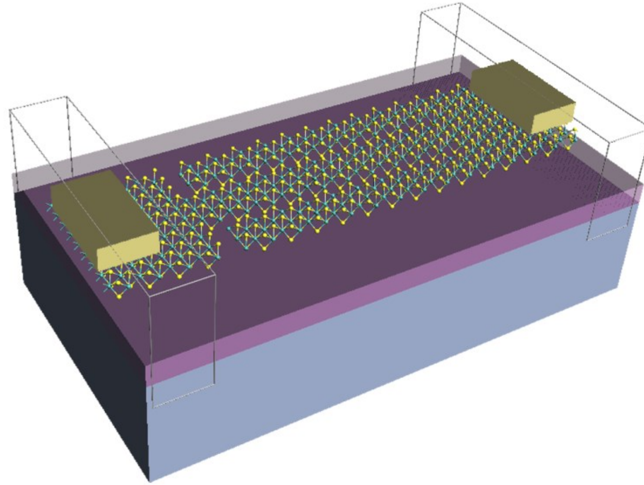

Figure 5.1 | The structure of a MoS_2 Self-Switching Diode shown in perspective view.

This chapter proposes the use of MoS_2 in realizing a completely two-dimensional SSD, using a single MoS_2 monolayer. The proposed device structure is shown in Fig. 5.1, and is referred to as a MoS_2 SSD.

Quantum simulation results, based on the Extended Huckel (EH) method and Nonequilibrium Green's Function (NEGF) formalism are presented, confirming the device's operation as a rectifier and showing strong non-linear I-V characteristics. Interestingly, the results suggest that the MoS_2 SSD behaves as a p-type device, complementary to the n-type Graphene SSD presented in earlier work [85, 86]. Further analysis about the transport mechanisms in the device are presented, confirming the strong field-effect control that can be achieved in the device, due to the presence of the large bandgap, and suggesting a great potential for further improvement of the device's performance. Finally, the effect of p-type substitutional doping using phosphorus is investigated, and shows promising results. Through the use of p-type doping, the presented device achieves a rectification ratio one order of magnitude greater than what can be achieved without doping.

The device structure is presented in the next section followed by the simulation results and an analysis of the different transport mechanisms within the device. The next section then concludes by investigating of the effect of p-type doping on the device’s performance.

5.2 Results and Discussion

5.2.1 Device Structure

A Self Switching Diode is a two-terminal nano-diode that rectifies current purely based on a self-induced field-effect mechanism that does not require a third gate terminal, junction formation or even doping and hence can be fabricated with minimal process steps [55]. An SSD requires a material in which conduction is confined in a two-dimensional plane, within which two L-shaped insulating trenches can be etched, defining a nano-channel in between them through which conduction occurs. This nano-channel is surrounded by two side gates, which are connected to one of the two device terminals, and these two side gates are used to control the conductivity of the nano-channel using the self-induced electric field that is produced by applying a bias voltage across the device. Conduction takes place within the same plane that the electric field is applied in, and based on this, a SSD is considered as a completely a two-dimensional planar device.

Self-Switching Diodes were previously realized on three-dimensional bulk materials such as compound semiconductor heterostructures [59], Silicon-On-Insulator wafers[56], and Zinc Oxide thin films [57, 196], and have shown a great potential for high speed operation, achieving Terahertz detection at room temperature [58, 60, 197]. Only recently SSDs were proposed using a two-dimensional material; Graphene [12-14]. Two-dimensional materials are well suited to the two-dimensional architecture of SSDs and greatly simplify their fabrication process, requiring only two patterning steps; one for defining the device and the L-shaped trenches, and one for defining the contacts. This chapter proposes their realization on MoS_2, which promises enhanced field-effect control due to its large bandgap and easier fabrication due to the ability of synthesizing it using wafer-scale processes without the need for subsequent transfer.

The structure of a MoS_2 SSD is shown in Figs. 5.1, 5.2 and 5.3, in perspective view, side view and top view, respectively. The proposed device is a nanoscale device with sub-10 nm dimensions, incorporating a 6 nm long channel that is 6 atoms wide, and two side gates that are 5 atoms wide each. The device was constructed and its transport properties were studied using Atomistix Toolkit (ATK) 12.8 [15]. The used calculation method is outlined in Section 5.4.

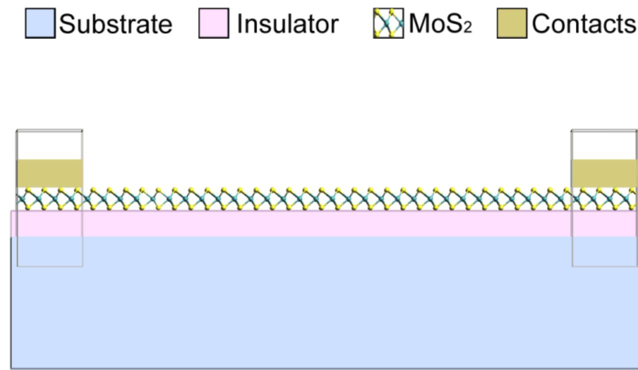

Figure 5.2 | Side view of the MoS_2 Self-Switching Diode, showing the device layers including the MoS_2 monolayer.

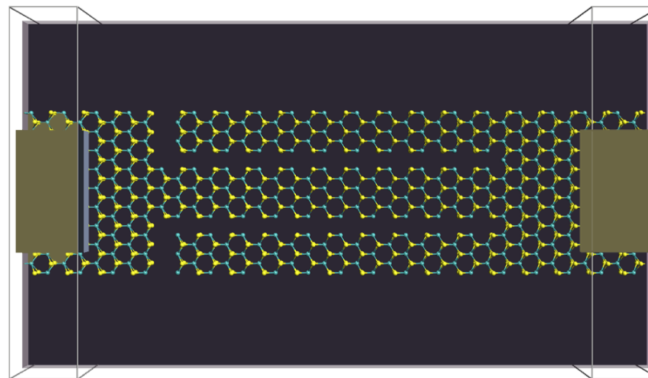

Figure 5.3 | Top view of the MoS_2 Self-Switching Diode, showing the L-shaped insulating trenches that define the nano-channel.

5.2.2 Current-Voltage (I-V) Characteristics

Current-Voltage (I-V) characteristics of the device, shown in Figs. 5.1-5.3, were calculated, and are shown in Fig. 5.4. It can be clearly observed through the figure that the device exhibits a non-linear asymmetric I-V curve, and hence achieves rectification. However, it is noted that reverse current is enhanced, while forward current is suppressed, suggesting that the device behaves as a p-type SSD. In order to clarify this, Fig. 5.5 is presented, which explains the principle of operation of a p-type SDD, in which conduction is dominated by holes.

In an SSD, whether n or p-type, at zero bias natural depletion regions are formed around the boundaries of the L-shaped insulating trenches due to the presence of surface states. These result as a consequence of the repulsion between the majority charge carriers accumulated at the edges surrounding the insulating trenches, and hence these would

mean that in an n-type material these regions would be depleted from electrons, and in a p-type material these depletion regions would be depleted from holes. The latter case is illustrated through Fig. 5.5(a). The nature of carriers (n or p-type) and their concentration can be controlled by doping, trapped surface charges between the MoS_2 monolayer and the substrate and the application of a gate potential. The latter can be achieved using a back or a top gate.

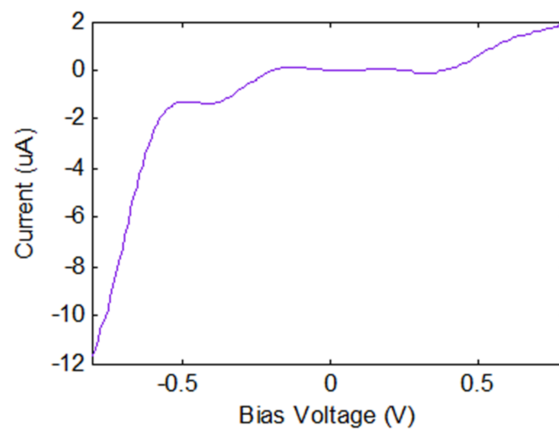

Figure 5.4 | I-V Characteristics of the MoS_2 Self-Switching Diode

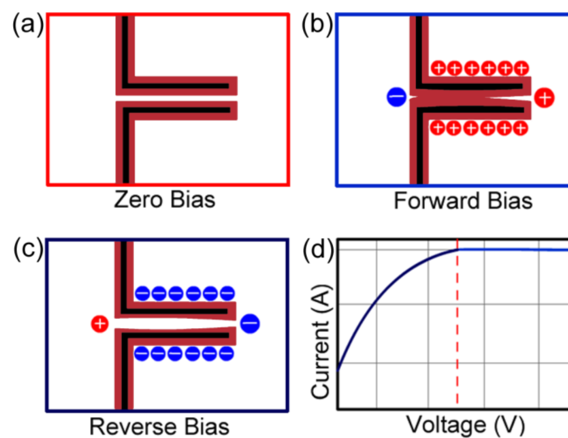

Figure 5.5 | Schematic diagram illustrating the principle of operation of a p-type Self-Swtiching Diode and illustrating how the channel is depleted from holes. The subfigures illustrate (a) the formation of natural depletion regions with zero bias voltage, (b) their widening and the blockage of the channel under forward bias, (c) their narrowing and the opening of the channel under reverse bias, and (d) the expected I-V characteristics of a typical p-type SSD. (hole-depletion regions are represented by the light red regions in the figures).

For the p-type case, applying a forward bias would deplete more holes, widening these depletion regions, and eventually pinching-off the channel and preventing forward conduction, as shown in Fig. 5.5(b). On the other hand, a reverse bias would narrow down the depletion regions, opening the channel and enhancing reverse conduction, as illustrated by Fig. 5.5(c). This effect would result in I-V characteristics similar to Fig. 5.5(d), where rectification occurs in the third quadrant, and this is what is being referred to here as p-type rectification.

In the I-V characteristics of the MoS_2 SSD (Fig. 5.4), reverse current reaches a value 6 times greater than forward current, representing a respectable rectification ratio, and confirming the device's operation as a diode. However, in order to confirm that this is due to the field effect mechanism described above, and in order to understand the origins of the unwanted forward current, further analysis is presented in the next section, discussing the different transport mechanisms taking place in the MoS_2 SSD.

5.2.3 Transport Mechanisms in the Device

In order to investigate how the conductance of the device is changing, the differential conductance of the device was calculated and is plotted against the bias voltage in Fig. 5.6. The plot suggests that in reverse conduction, the conductance begins to rise abruptly at negative voltages lower than -0.5 V. The point at which the conductance begins to rise abruptly is the threshold voltage of the device, at which the channel opens up. Once the channel is open, increasing the bias voltage greatly increases the conductance, due to the effect of the self-induced field applied by the side gates. On the other hand, in forward conduction, the conductance does not seem to change significantly and continuously, suggesting that the conduction might be based on a different transport mechanism and not on the flow of current through the channel. This mechanism may also be present in reverse conduction as the shape of the differential conductance plot shows some similarity between the forward conduction region and the reverse conduction region prior to the threshold voltage. It is only after the threshold voltage that this transport mechanism becomes over dominated by the conduction through the channel in reverse bias.

In order to investigate the origin of the unwanted current during forward conduction and investigate the transport mechanism that drives it, the transmission pathways in the device, under both forward and reverse biases, were calculated and are presented in the illustrations in Figs. 5.7 and 5.8 respectively.

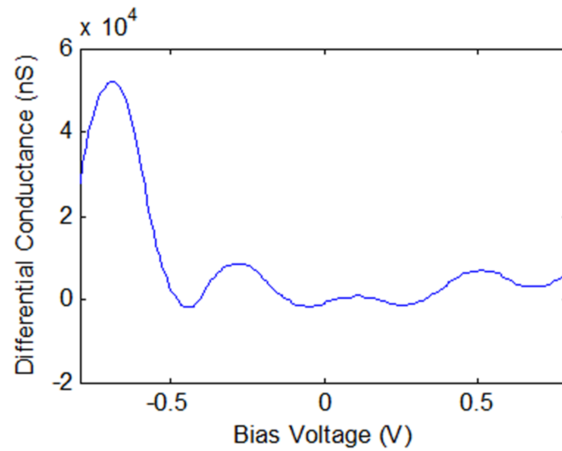

Figure 5.6 | Plot of Differential Conductance vs. Bias Voltage for the MoS_2 SSD.

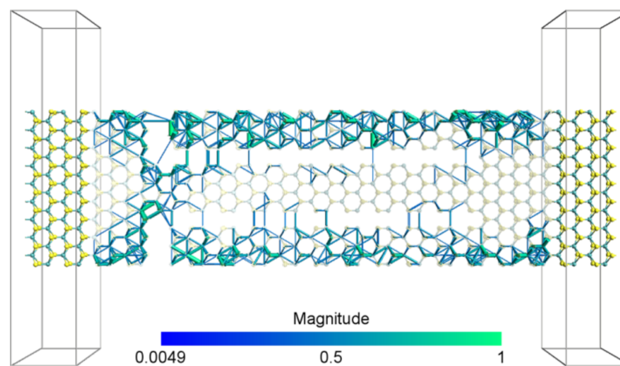

Figure 5.7 | Transmission pathways plot for the MoS_2 SSD under a forward bias voltage of +1V (the central region of the device configuration is made 90% transparent in order to make the transmission pathways easier to visualize).

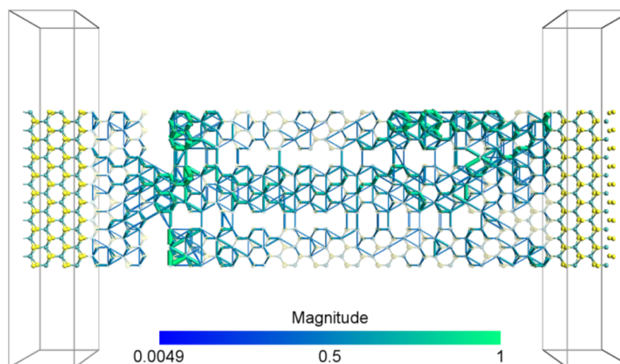

Figure 5.8 | Transmission pathways plot for the MoS_2 SSD under a reverse bias voltage of -1V (the central region of the device configuration is made 90% transparent in order to make the transmission pathways easier to visualize).

The transmission pathways can be used to visualize the transport channels available for current flow in a device configuration under different bias voltages. Under forward bias, as shown in Fig. 5.7, it is clearly confirmed that there is no conduction through the channel due to the absence of a continuous transmission pathway through it. Furthermore, the channel pinch-off is also confirmed and as Fig. 5.7 suggests, the channel is indeed completely pinched-off unlike the situation in a Graphene SSD [85, 86]. In a Graphene SSD the channel pinch-off is partial, or takes place only towards the end of the channel. This may be due to the large band gap present in MoS_2 compared to the very small band gap present in armchair Graphene nanoribbons. This suggests that in a MoS_2 SSD, channel conduction may be much more efficiently controlled than that in a Graphene SSD.

This is further confirmed by Fig. 5.8, which shows very strong conduction through the channel under reverse bias, illustrated by the continuous thick transmission pathways through the channel, and confirming the that channel is opened under reverse bias.

A very important finding suggested by Fig. 5.7 is that, although conduction through the channel is blocked under forward bias, significant conduction occurs through current that tunnels from the side gates through the insulating trenches. This tunnelling mechanism is driving the unwanted current during forward conduction. Furthermore, as suggested by Fig. 5.6, this same mechanism remains under reverse bias, as shown in Fig. 5.8, but conduction through the channel dominates. Based on this finding, it can be concluded that the field-effect control over the channel's conductivity and the self-switching mechanism in a MoS_2 SSD are highly efficient, and promise a great potential for realizing MoS_2 SSDs with even higher rectification ratios. The major constraint that needs to be addressed in a MoS_2 SSD is suppression of tunnelling current through the insulating trenches, and this may be achieved through better insulation or the use of passivation.

5.2.4 P-Type Doping

As mentioned earlier, MoS_2 exhibits a very important advantage when compared to Graphene; its feasibility of being doped into both n and p-type. In a SSD, conduction is based on majority charge carriers and hence increasing the concentration of majority charge carriers through doping may greatly enhance the performance of the device. This section proposes the introduction of substitutional Phosphorus doping in MoS_2, in order to enhance the performance of the device.

A MoS_2 SSD behaves as a p-type rectifier, and hence conduction in it is dominated by holes. In order to make the device more p-type, the concentration of holes needs to be increased and this can be achieved through the introduction of acceptor atoms in the device. Phosphorus has proven to be an acceptor atom in MoS_2 when it substitutes a Sulphur atom [195, 198], and this is because Phosphorus has one less electron in its outer shell when compared to Sulphur.

In order to investigate how this proposed concept can affect the performance of the device, the channel of the device in Figs. 5.1-5.3 was doped with Phosphorus, by substituting a number of Sulphur atoms in the channel with Phosphorus. The used doping concentration was 3%. The structure of this new Phosphorus doped MoS_2 SSD is shown in Figs. 5.9(a) and 5.9(b) in perspective view and top view respectively.

The transmission spectrum of the device was calculated for the device under forward bias (+0.4V) and reverse bias (-0.4V) and is plotted in Figs. 5.9(c) and 5.9(d) respectively. Within the applied bias window in both cases a single transmission peak can be observed, which lies at around 0.09 eV above the Fermi level. This peak is greatly suppressed for the forward bias case (Fig. 5.9(c)) and is significantly pronounced for the reverse bias case (Fig. 5.9(d)), illustrating strong rectification.

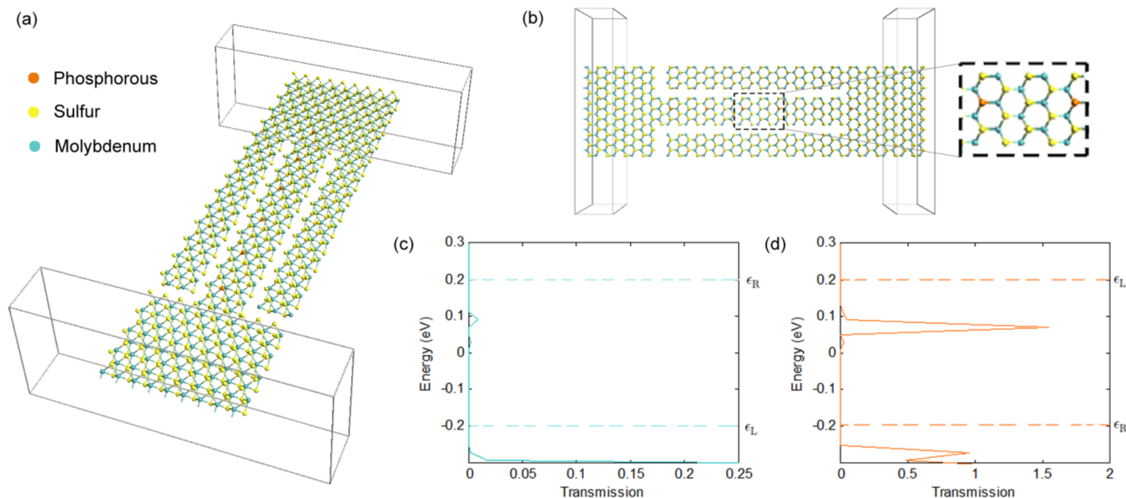

Figure 5.9 | Transport properties of Phosphorus doped MoS_2 Self-Switching Diodes. The structure of a Phosphorus doped MoS2 Self-Switching Diode shown in (a) perspective view and (b) top view. The transmission spectrum of the device shown under (c) a forward bias voltage of +0.4V and (d) a reverse bias voltage of -0.4V. The dotted lines in (c) and (d) represent the Fermi levels of the right electrode (ε_R) and the left electrode (ε_L) relative to the Fermi level of the overall system, and the region between the two dotted lines represents the bias window.

This is further confirmed through Fig. 5.10, which shows the I-V characteristics of the device, and confirms the presence of strong p-type rectification, with great improvement compared to the I-V characteristics of the device without doping (Fig. 5.4).

One noticeable difference between the I-V characteristics of the doped device (Fig. 5.10) and the undoped device (Fig. 5.4) is that in the doped device the unwanted forward current is greatly suppressed. In order to understand why this occurs in the doped device, the transmission pathways within the device under forward and reverse biases were calculated and are plotted in Figs. 5.11 and 5.12 respectively.

A very important observation can be made from the plot of Fig. 5.11 relating to the tunnelling current through the side gates. It is seen that this tunnelling current is greatly suppressed in the upper side gate, and is restricted and concentrated along the edges of the lower side gate. The transmission pathways near the trench in the lower side gate are greatly suppressed, while they are completely suppressed in the upper side gate. An explanation to this can be due to the increased concentration of holes in the doped channel. The increased concentration of holes within the channel accumulates more positive charges near the edge of the insulating trench from the side of the channel. These increased accumulated positive charges near the trench repel similar positive charges on the other side of the trench within the side gate, depleting it from positive charges, i.e. depleting it from holes. These depletion regions are natural for a SSD and were described and illustrated earlier in Fig. 5.5, however here in this case, where the channel is doped and has an increased concentration of holes, these depletion regions within the side gates are extended and the gates are more depleted from holes, when compared with the case of the undoped channel. Accordingly, since the side gates are now more depleted from holes, tunnelling of holes from them to the left electrode would be suppressed, suppressing the amount of unwanted tunnelling current. It is also noted that since dopant atoms are closer to the upper side gate, as seen through Fig. 5.9(b), the upper side gate is more depleted of holes and tunnelling through it is suppressed more than tunnelling through the lower side gate.

On the other hand, looking at the transmission pathways plot for the reverse bias case in Fig. 5.12, there is no significant difference between it and that of the undoped device shown in Fig. 5.8, except for some slight patches in the transmission pathways through the channel, which are only due to the presence of the impurity dopant atoms. Although

this does not show a significant effect in the I-V characteristics, this may have an effect on the frequency response of the device.

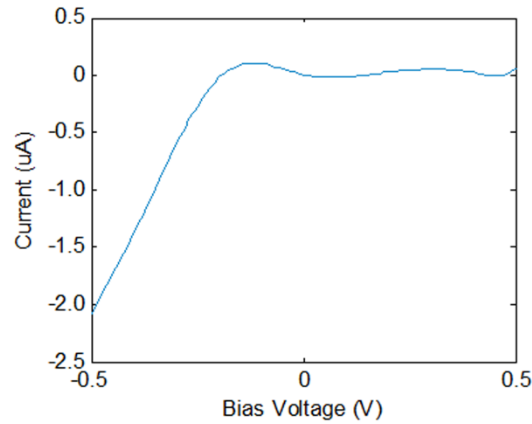

Figure 5.10 | The I-V Characteristics of the Phosphorus doped MoS_2 Self-Switching Diode.

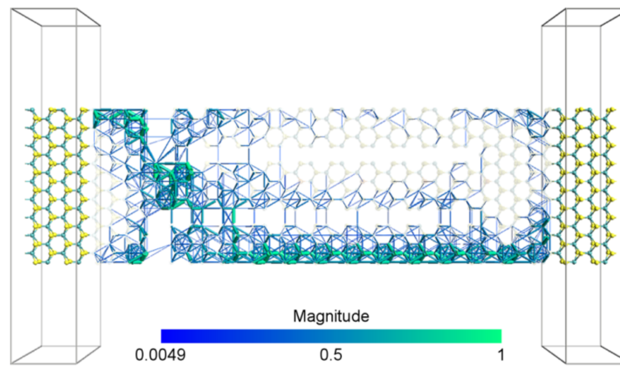

Figure 5.11 | Transmission pathways plot for the P-doped MoS_2 SSD under a forward bias voltage of +0.6V (the central region of the device configuration is made 90% transparent in order to make the transmission pathways easier to visualize).

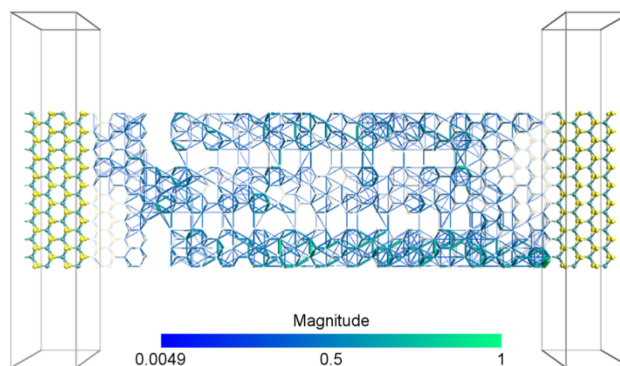

Figure 5.12 | Transmission pathways plot for the P-doped MoS_2 SSD under a reverse bias voltage of -0.6V (the central region of the device configuration is made 90% transparent in order to make the transmission pathways easier to visualize).

Previous studies [199, 200] on SSDs realized using 3D bulk materials have shown that lower doping concentration results in improved DC and AC performance of large microscale SSDs. In large SSDs, where the insulating trenches are in the order of hundreds of nanometers, tunnelling current may not contribute significantly to the device's performance, and hence such conclusions about the DC performance of large microscale SSDs might not be applicable to the nanoscale SSDs presented in this study, in which tunnelling current has a significant effect on the overall conduction. On the other hand, while in the previous studies the investigation was concerned with the overall doping concentration across the whole device, and not the channel only as in our case, these previous findings about the AC performance of microscale SSDs open up important queries about the effect of doping concentration on the AC performance of nanoscale SSDs, calling for the need for further investigation before implementing such devices in high frequency applications.

In summary, it was shown that substitutionally doping the channel of MoS_2 SSDs using Phosphorus greatly enhances their performance and suppresses unwanted forward tunnelling current in them. In the presented device, this enhancement was more than one order of magnitude and resulted in a reverse-to-forward current rectification ratio of more than 70.

5.3 Summary

This chapter proposed the concept of MoS_2 Self-Switching Diodes, and showed how they can be realized within a single MoS_2 monolayer. The large bandgap in MoS_2 results in a highly efficient field-effect self-switching mechanism that results in complete channel pinch-off under forward bias, and enhanced channel opening under reverse bias. This mechanism results in the enhancement of reverse current and the suppression of forward current, making the MoS_2 SSD a p-type device that achieves p-type rectification, complementary to the n-type Graphene SSD. The lack of passivation in a MoS_2 SSD results in large unwanted tunnelling currents through the insulating trenches, and suppressing this tunnelling current through passivation or stronger insulation may lead to a great enhancement in the rectification ratio of the device. Another approach to deal with this unwanted tunnelling current was proposed based on channel doping. This can be achieved through the substitutional doping of Sulphur atoms with Phosphorus atoms within the channel, and was investigated here through quantum simulations. The simulation results showed that making the channel more p-

type, through Phosphorus doping, results in the depletion of the side gates from holes and greatly suppresses any unwanted tunnelling current through them. This suppression of unwanted tunnelling current greatly enhanced the performance of the device, resulting in an achieved reverse-to-forward current rectification ratio of 70, which is an enhancement of more than one order of magnitude compared to the undoped case. These results suggest a great potential towards realizing high performance MoS_2 SSDs, which may have a promising future in next generation RF systems and Terahertz detectors.

5.4 Methods

Transport calculations for obtaining I-V characteristics curves and transmission pathways plots were all based on the Extended Huckel (EH) [76] method and Non-Equilibrium Green's Function (NEGF) formalism [75] as implemented in ATK [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

The device structure was partitioned as three regions: semi-infinite left electrode *(L)*, central scattering region *(C)*, and semi-infinite right electrode *(R)*. The mesh points in real space calculation were defined as uniformly spaced *k* points of 1 x 10 x 50, with 50 sample points along the length (transport direction) and 10 points along the width (induced electric field direction) of the two-terminal structure. The same calculation method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

5.4.1 Calculation of the Differential Conductance

The differential conductance, plotted in Fig. 5.6, was calculated by differentiating the calculated current curve with respect to the bias voltage as:

$$Differential\ Conductance = \frac{dI}{dV} \tag{5.1}$$

6 SILICENE SELF-SWITCHING DIODES

Silicene is an exciting two-dimensional material that shares many of graphene's electronic properties, but differs in its structural buckling. This buckling allows opening a bandgap in silicene through the application of a perpendicular electric field. This chapter shows that this buckling also enables highly effective modulation of silicene's conductance by means of an in-plane electric field applied through silicene side gates, which can be realized concurrently within the same silicene monolayer. This is illustrated by using silicene to implement Self-Switching Diodes (SSDs), which are two-dimensional field effect nanorectifiers realized within a single silicene monolayer. The presented quantum simulation results show that the atomically-thin silicene SSDs, with sub-10 nm dimensions, achieve current rectification ratios exceeding 200, without the need for doping, representing a 30 fold enhancement over graphene SSDs. This enhancement is attributed to a bandgap opening due to the in-plane electric field, as a consequence of silicene's buckling. The presented findings suggest that silicene is a promising material for next generation Integrated Circuits.

6.1 Introduction

Graphene has long been envisaged as a promising candidate for post-CMOS electronics. However, graphene lacks an electronic bandgap, making it difficult to turn a graphene device off effectively by means of an electric field. Accordingly, many efforts have been redirected towards finding other two-dimensional materials that have an electronic bandgap but still exhibit many of graphene's desirable electronic properties, such as its high electron mobility.

Amongst numerous candidates, silicene, a new material composed of a monolayer of silicon atoms, has attracted the interest of theorists [201-204] and more recently experimentalists [205-210] as a promising material for next generation electronics [73] and spintronics [211, 212]. It shares many of graphene's electronic properties [213] and exhibits a similar hexagonal structure. However, silicene differs from graphene, which is completely flat, in the fact that it is buckled [74, 214, 215]. Due to this buckling, it has been predicted through Density Functional Theory (DFT) calculations that a band gap can be opened in silicene through the application of a perpendicular electric field[216, 217], a capability that is only possible in bi-layer graphene [218]. This however, requires external gating and the deposition of other materials on silicene, adding more complexity to the already challenging synthesis process of silicene and degrading some of its desirable electronic properties. In order to overcome such challenges, it is highly desirable to be able to introduce a bandgap in silicene and effectively control its conductance by means of an in-plane electric field, which can be applied through planar two-dimensional device geometries.

A unique class of planar field effect devices is the Self-Switching Diode (SSD) [55], which is a two-dimensional nanoscale rectifier that achieves rectification by means of a self-induced in-plane field effect that acts within the same plane of conduction, making the device completely two-dimensional (2D). This 2D architecture of SSDs, shown in Fig. 6.1, makes them very well suited for 2D materials. In earlier chapters, the realization of SSDs on Graphene was proposed [85, 86], showing promising performance [85] and unique negative differential resistance capabilities [86].

In this chapter, silicene SSDs are proposed and studied using Non-Equilibrium Green's Function (NEGF) formalism [75] and the Extended Huckel (EH) method [76]. Their performance is then compared with graphene SSDs, in order to investigate how an in-plane electric field affects silicene in comparison with graphene.

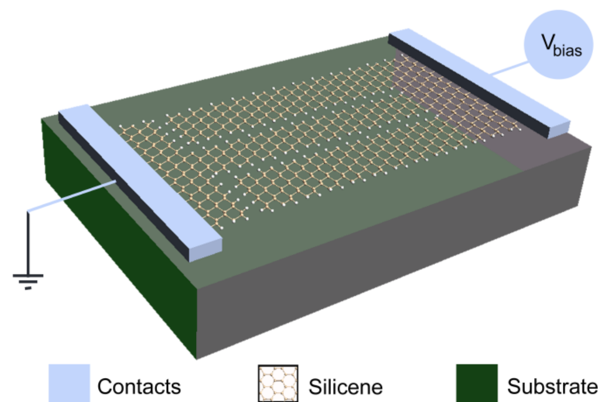

Figure 6.1 | A perspective view of a Silicene Self-Switching Diode (SSD), showing the geometry of the device and the voltage bias direction.

The presented results suggest a similarity between the electronic properties and behaviour of silicene SSDs and graphene SSDs, but show superior performance of silicene SSDs, up to a 30 fold enhancement in rectification ratio, suggesting that an in-plane electric field has much stronger control on the conductivity of silicene nanoribbons in comparison to graphene nanoribbons. This enhanced performance in silicene SSDs is attributed to a bandgap opening that results due to silicene's buckled structure, which is shown in Fig. 6.2(a). These findings suggest that silicene could potentially be a very promising material for the realization of planar field effect devices for next generation Integrated Circuits (ICs).

In the next section the simulation results for the proposed silicene SSDs are presented and compared with graphene, followed by a discussion of the relationship between silicene's buckling and the presented findings. The calculation method is described separately in the methods sections at the end of the chapter (Section 6.4).

6.2 Results and Discussion

A self-switching diode is formed by etching two L-shaped trenches through a two-dimensional material. These two L-shaped trenches define a nanoribbon in between them, which acts as the nano-channel of the device, through which conduction occurs. This nano-channel is surrounded by two side gating nanoribbons, which are used to apply a self-induced electric field onto the channel in order to control its conductance. This is illustrated through Fig. 6.2(b).

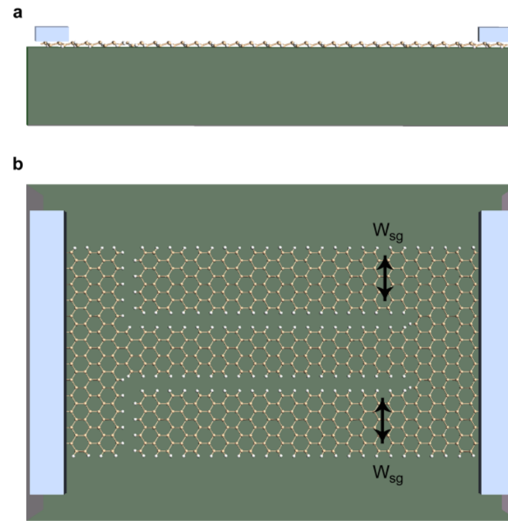

Figure 6.2 | The geometry of a silicene SSD. (a) Side view showing the buckling property of silicene. (b) Top view showing the two L-shaped trenches that define the nano-channel of the device and its surrounding two side gates, which have a width of W_{sg} atoms (8 atoms in this case).

Since the channel in a silicene SSD is a nanoribbon, it can have either armchair or zigzag edges depending on the orientation of the etched L-shaped trenches. The channel of the device illustrated in Figs. 6.1 and 6.2(b) is an armchair nanoribbon, while the channel of the devices shown in Figs. 6.3(a) and 6.3(b) is a zigzag nanoribbon. The latter can be realized by etching the L-shaped trenches in an orientation that is perpendicular to their orientation in Figs. 6.1 and 6.2(b). The two side-gating nanoribbons would unavoidably have similar edges to those of the channel, and hence, they are armchair in Figs. 6.1 and 6.2(b), and zigzag in Figs. 6.3(a) and 6.3(b). In order to investigate how an in-plane electric field affects each of the two types of silicene nanoribbons, the transport properties of silicene SSDs that have both zigzag and armchair nanoribbon channels will be studied in the subsequent subsections.

6.2.1 Zigzag Nanoribbon Channels

Figures 6.3(a) and 6.3(b) show two similar SSDs with zigzag nanoribbon channels 6 atoms wide, and side-gating nanoribbons with a width of 6 and 8 atoms respectively.

The current-voltage (I-V) characteristics of both devices were calculated as described in the methods section (Section 6.4), and are shown in Fig. 6.3(c). Both SSDs do not achieve rectification and are not affected by the in-plane electric field, behaving as

metallic nanoribbons. Even when the side gating nanoribbons are wider than the channel of the device, as in Fig. 6.3(b), the device continues to conduct across the whole bias voltage range and does not achieve any noticeable rectification. This is consistent with DFT calculations and previous predictions [201], and consistent with graphene SSDs with zigzag nanoribbon channels [85].

To exclude the possibility that conduction is dominated by tunnelling current through the insulating trenches of the devices of Figs. 6.3(a) and 6.3(b), the dangling bonds at the edges of the nanoribbons were passivated with hydrogen, as shown in Figs. 6.4(a) and 6.4(b) respectively. The calculated I-V characteristics of the passivated devices are shown in Fig. 6.4(c). The devices show no rectification, confirming that the channel is conducting equally under both reverse and forward biases and is not affected by the in-plane electric field.

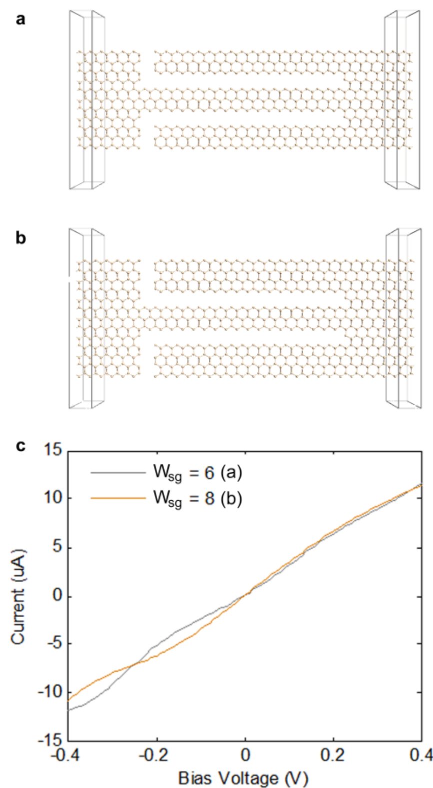

Figure 6.3 | Silicene SSDs with zigzag nanoribbon channels that are 6 atoms wide and side-gating zigzag nanoribbons that are (a) 6 atoms wide and (b) 8 atoms wide. (c) I-V characteristics of the devices in (a) and (b) plotted on the same axes in grey and brown colours respectively.

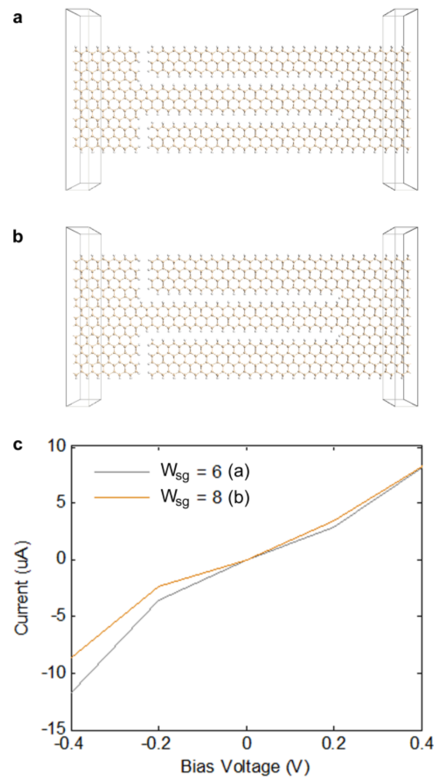

Figure 6.4 | Silicene SSDs with H-passivated zigzag nanoribbon channels that are 6 atoms wide and side-gating zigzag nanoribbons that are (a) 6 atoms wide and (b) 8 atoms wide. (c) I-V characteristics of the devices in (a) and (b) plotted on the same axes in grey and brown colours respectively. Hydrogen passivation is at the edges of the nanoribbons.

6.2.2 Armchair Nanoribbon Channels

The transport properties of silicene SSDs with armchair nanoribbon channels were then investigated. Figure 6.5(a) shows a silicene SSD with an armchair nanoribbon channel that is 6 atoms wide and side gating nanoribbons that are 9 atoms wide, while Fig. 6.5(b) shows its calculated I-V characteristics. As the figure suggests, the device's I-V characteristics exhibit significant asymmetry, and achieve noticeable rectification. Transmission pathways plots under reverse and forward biases for the device are shown in Figs. 6.5(c) and 6.5(d) respectively. Under a reverse bias voltage of -1V, Fig. 6.5(c), the device channel does not have an available transmission pathway, confirming its closure. Under a forward bias voltage of 1V, Fig. 6.5(d), the channel exhibits strong continuous transmission pathways, confirming its opening. The observed differences between the transmission pathways under reverse and forward biases confirm the strong control that the in-plane field has on the semiconducting armchair silicene nanoribbon channel.

One important observation in Fig. 6.5(c) is the significant transmission pathways that are observed across the vertical insulating trenches, which suggest significant unwanted tunnelling current under reverse bias. This large tunnelling current is predominantly due to the presence of dangling bonds at the edges of the nanoribbons. In order to minimize it, all dangling bonds at the edges of the nanoribbons were passivated with hydrogen, as shown in Fig. 6.6(a). The transmission pathways plots for the hydrogen passivated device under reverse and forward biases are shown in Figs. 6.6(c) and 6.6(e) respectively. The plot of Fig. 6.6(c) confirms the minimization of tunnelling current through the vertical insulating trenches, and illustrates how the channel is strongly turned off in a silicene SSD under reverse bias, while the plot of Fig. 6.6(e) confirms that the channel is conducting strongly under forward bias.

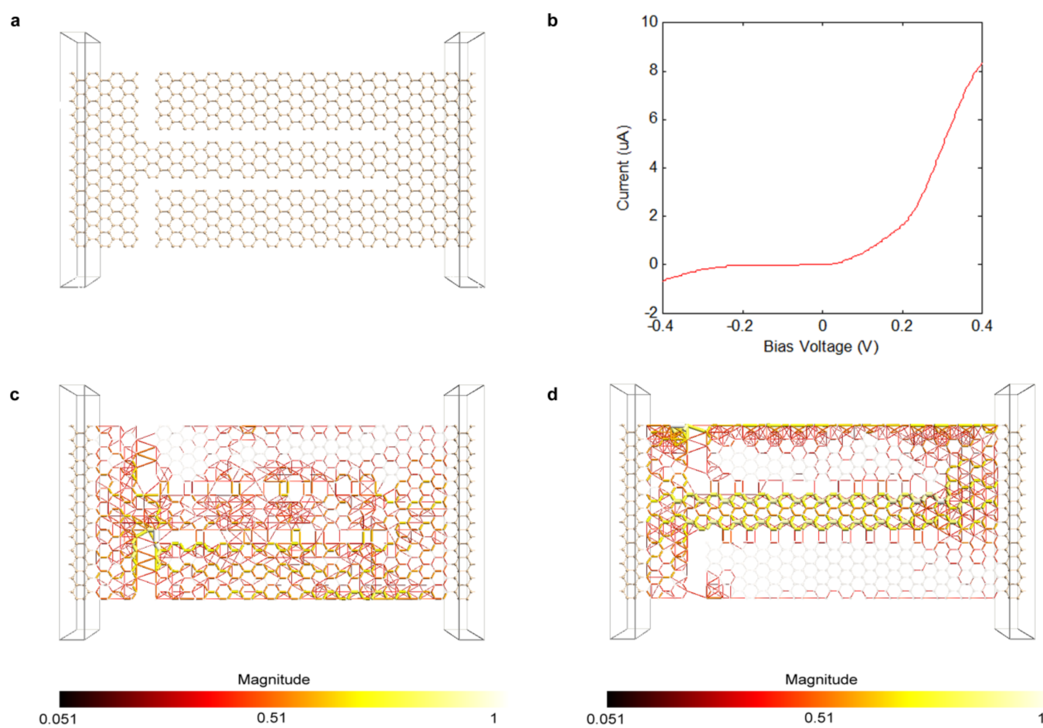

Figure 6.5 | A Silicene SSD with a semiconducting armchair nanoribbon channel that is 6 atoms wide and armchair nanoribbon side gates that are 9 atoms wide. (a) The structure of the device. (b) I-V characteristics of the device. Transmission pathways plots of the device under (c) a reverse bias voltage of –1V and (d) a forward bias voltage of 1 V illustrate how the channel's conductivity is controlled by the in-plane electric field, turning it off under reverse bias in (c) and making it conduct heavily under forward bias in (d). The colour of a line resembles the magnitude of the local transmission component along a bond according to the colour bar at the bottom of each figure. In (c) and (d) the atoms and the bonds in the central region of the device geometry are drawn with 90 % transparency to allow better visualization of the transmission pathways.

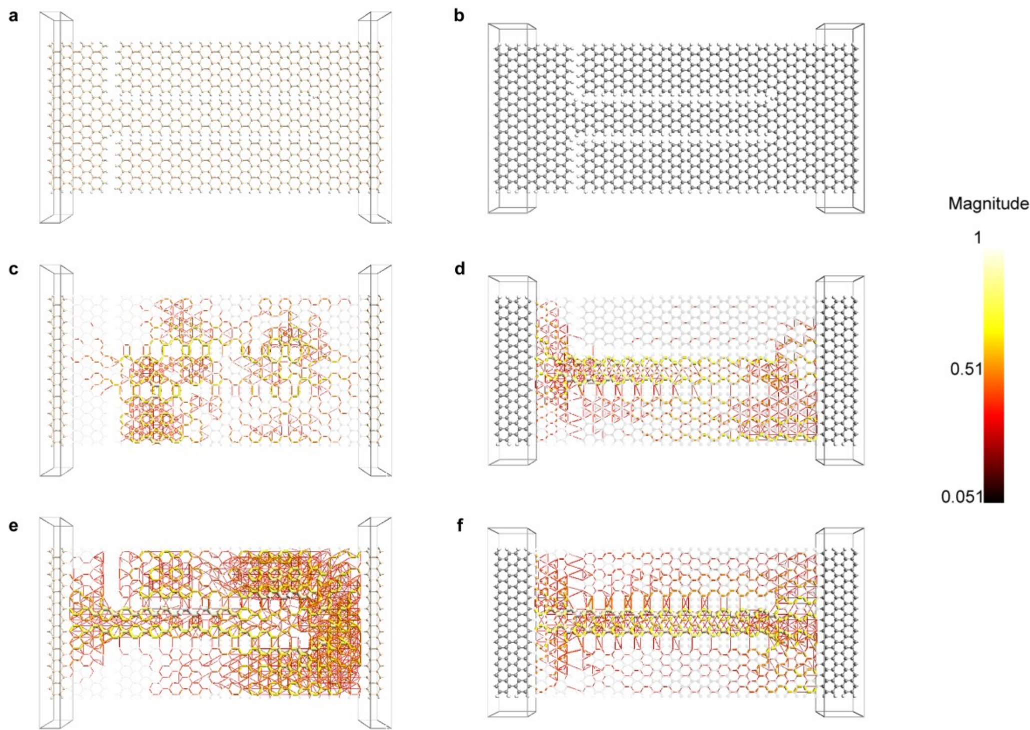

Figure 6.6 | Comparison between silicene and graphene SSDs with semiconducting H-passivated armchair nanoribbon channels. (a) Silicene and (b) graphene SSDs with armchair nanoribbon channels that are 6 atoms wide and armchair nanoribbon side gates that are 9 atoms wide. The central regions in the two devices are similar; however, the semi-infinite electrodes in (b) are longer than in (a) due to graphene's smaller lattice constant, which requires at least two units cells in order to ensure that the electrodes are longer than 6 Å. Transmission pathways plots for (c) the silicene and (d) the graphene SSDs under a reverse bias voltage of -1V, showing how the channel is turned off much more efficiently in a silicene SSD. Transmission pathways plots for (e) the silicene and (f) the graphene SSDs under a forward bias voltage of 1V, showing how the channel is turned on in both devices. The colour of a line resembles the magnitude of the local transmission component along a bond according to the colour bar at the side of the figure. In (c-f) the atoms and the bonds in the central region of the device geometries are drawn with 90 % transparency to allow better visualization of the transmission pathways.

The presented findings on silicene SSDs with armchair channels are consistent with previous findings for graphene SSDs with armchair channels [85]. However, in order to investigate how silicene and graphene compare with each other, a graphene SSD with a geometry similar to the silicene SSD of Fig. 6.6(a) was constructed, and is shown in Fig. 6.6(b). The transmission pathways plots for the device under reverse and forward biases are shown in Figs. 6.6(d) and 6.6(f) respectively. Under forward bias, the channels of both devices open up and conduct strongly for silicene and graphene (Figs. 6.6(e) and 6.6(f)), respectively. However, under reverse bias, the transmission pathways within the graphene device (Fig. 6.6(d)) show only a slight suppression towards the end

of the channel, unlike the complete channel turn-off observed for the silicene device (Fig. 6.6(c)). This confirms that the silicene channel is more efficiently turned-off than the graphene channel.

In this next subsection we investigate a special class of silicene SSDs; the all-silicene self-switching MISFED, Metal-Insulator-Semiconductor Field Effect Diode.

6.2.3 All-Silicene Self-Switching MISFEDs

In graphene, armchair nanoribbons have a unique property, in which the bandgap of the nanoribbon varies with its width [103, 104]. Armchair graphene nanoribbons with a width of 3*p* and 3*p*+1 atoms, where *p* is an integer, have sizable bandgaps making them semiconducting [103], while those with a width of 3*p*+2 atoms have vanishingly small bandgaps, making them behave as if they were metallic [103].

By utilizing the property of being able to tune armchair graphene nanoribbons from metallic to semiconducting by width variation, the all-graphene self-switching MISFED (Metal-Insulator-Semiconductor Field Effect Diode) [85] was proposed in previous chapters, which is a class of graphene SSDs with metallic side-gates, and semiconducting channels, and can be realized by designing the width of the side gates (W_{sg}), marked on Fig. 6.2(b), to be 3*p*+2 atoms. This class of graphene SSDs achieves superior rectification when compared to the other two classes of graphene SSDs with semiconducting side-gates [85].

Building upon the similarity between graphene and silicene nanoribbons [201, 219], it is expected that bandgap tunability with width would also be present in armchair silicene nanoribbons. This is investigated by studying the transport properties of three different silicene SSDs with armchair nanoribbon channels. The three geometries are shown in Figs. 6.7(a), 6.7(b) and 6.7(c), and have similar armchair nanoribbon channels with a width of 6 atoms, while their side gates' widths (W_{sg}), are 5 (3*p*+2), 6 (3*p*) and 7 (3*p*+1) atoms respectively. The device in Fig. 6.7(a) has side gating nanoribbons of the 3*p*+2 type, which are expected to have metallic behaviour, and therefore, the device is expected to behave in a similar fashion to a graphene self-switching MISFED [85].

The calculated current-voltage (I-V) characteristics of the three devices are plotted in Fig. 6.7(d). All three devices show strong rectification confirming the semiconducting behaviour of their armchair silicene nanoribbon channels, and the control that an in-plane electric field has on their armchair nanoribbon channels' conductivity.

Furthermore, the device in Fig. 6.7(a) shows superior performance, behaving in a similar fashion to the graphene self-switching MISFED. However, a very important unexpected finding seen in Fig. 6.7(d) is the fact that all types of silicene SSDs, including the ones with semiconducting side-gates (Figs. 6.7(b) and 6.7(c)), achieve strong rectification. It is postulated that this effect is due to the manner in which silicene nanoribbons interact with an in-plane electric field.

In order to quantify the performance of the three devices, the current rectification ratio of each device (the ratio of forward current to unwanted reverse current) was calculated and is shown in Fig. 6.7(e). Figure 6.7(e) confirms the previous findings, showing high current rectification ratios in all three devices, when compared to what can be achieved with graphene without the use of doping. Graphene SSDs with similar geometry to the silicene SSDs in Figs. 6.7(b) and 6.7(c) do not exhibit significant rectification, with a rectification ratio in the order of 1 (i.e. forward current would equal reverse current)[85], whilst a graphene SSD (of the MISFED type) similar to the silicene SSD in Fig. 6.7(a) achieves a rectification ratio of eight [85]. In order to achieve higher rectification ratios, graphene MISFEDs require nitrogen edge passivation [85].

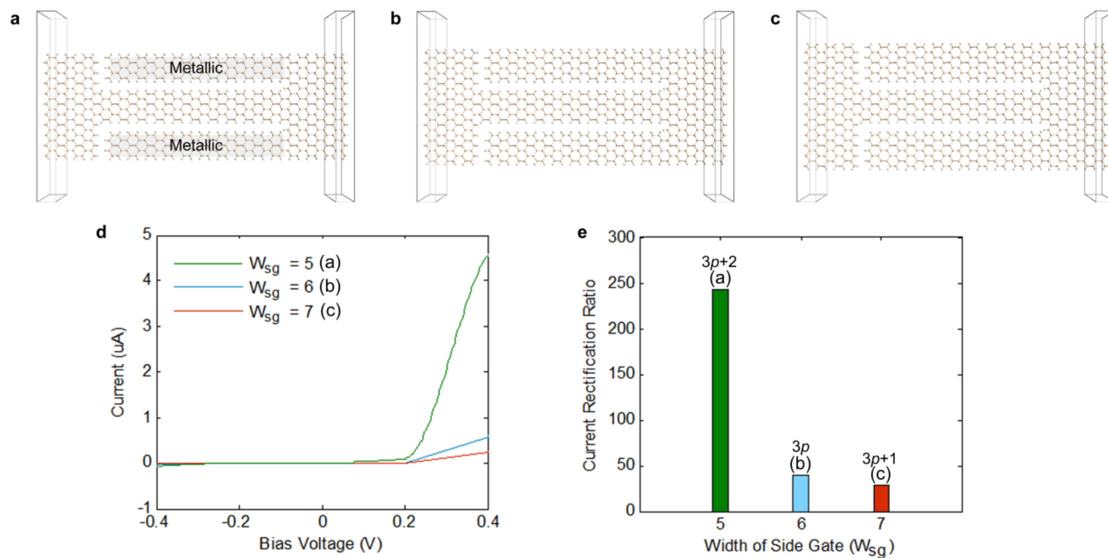

Figure 6.7 | Different types of silicene SSDs with semiconducting H-passivated armchair nanoribbon channels that are 6 atoms wide and armchair nanoribbon side gates that are: (a) 5 atoms, (b) 6 atoms and (c) 7 atoms wide. Hydrogen passivation is at the edges. The side gates of the device in (a), highlighted in grey, behave as metallic side gates due to their very small bandgap, making the device behave as a silicene self-switching MISFED. (d) I-V Characteristics of the devices in (a), (b) and (c) plotted on the same axes in green, blue and red colours respectively. (e) A bar chart showing the calculated current rectification ratios of the devices in (a), (b) and (c). The current rectification ratio is the maximum ratio of forward current to unwanted reverse current.

In contrast, the achieved rectification ratio for a silicene self-switching MISFED (Fig. 6.7(a)), without the use of dopants, reaches a value of 240. This is high in comparison to graphene and other types of SSDs realized on 2D materials such as MoS_2, bulk materials such as compound semiconductor heterostructures [59, 60], zinc oxide thin films [196] or silicon on insulator [56].

6.2.4 Effect of Buckling

Silicene shares many of graphene's properties, but differs in the fact that it exhibits a buckled structure. When a perpendicular electric field is applied to silicene, as shown in Fig. 6.8(a), an electronic bandgap is observed and can be tuned by varying the applied electric field strength [216, 217]. When a similar perpendicular electric field is applied to graphene, as shown in Fig. 6.8(c), no bandgap change is observed and only a Fermi level shift occurs. When an in-plane electric field is applied to an armchair silicene nanoribbon by two side gates with equal voltage, as in a SSD, the electric field lines between the side gates and the channel would have the distribution shown in Fig. 6.8(b), whilst for an armchair graphene nanoribbon the distribution would be as in Fig. 6.8(d).

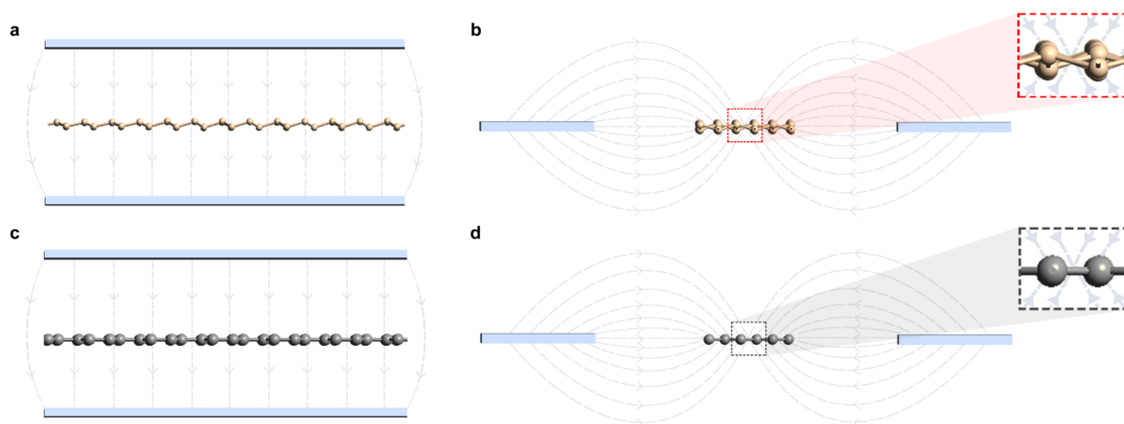

Figure 6.8 | The interaction of perpendicular and in-plane electric fields with silicene and graphene nanoribbons. The two subfigures on the left illustrate the interaction of perpendicular electric fields, applied by top and bottom gates, with: (a) a silicene nanoribbon and (c) a graphene nanoribbon. The figures show cross-sectional views taken along the length of: (a) an armchair silicene nanoribbon and (c) an armchair graphene nanoribbon. The two subfigures on the right illustrate the interaction of in-plane electric fields, applied by two in-plane side gates, with (b) a silicene nanoribbon and (d) a graphene nanoribbon. The figures show cross-sectional views taken along the width of: (b) an armchair silicene nanoribbon and (d) an armchair graphene nanoribbon. The two subfigures include zoomed-in portions in order to highlight: (b) the buckled structure of silicene and how it experiences a net vertical electric field component from the applied in-plane electric field, and (d) the completely flat structure of graphene and how it experiences no net vertical electric field component from the applied in-plane electric field.

In both cases, the electric field lines are not straight and interact with the nanoribbon at an angle, giving them a transverse as well as a vertical component. For the case of flat graphene, the vertical components from the field lines above the nanoribbon are cancelled by the vertical components from the field lines below the nanoribbon, resulting in no net vertical component (Fig. 6.8(d)). For the case of silicene, these two vertical components of the electric field do not meet at a midpoint, due to silicene's buckling, and do not cancel out completely. This results in a net vertical electric field component, similar to that of Fig. 6.8(a), which opens up a bandgap in the nanoribbon and allows it to be turned-off efficiently. Varying the strength of this electric field, allows for bandgap tunability, and leads to effective field-effect control over silicene's conductivity.

6.3 Summary

In summary, the effect of an in-plane electric field on silicene was investigated and showed that it results in strong control over silicene's conductivity. The control that is achieved by the in-plane electric field on silicene is much stronger than what can be achieved on graphene due to the buckled structure of silicene, which allows bandgap tunability. It was demonstrated how this effect can be utilized in order to realize high performance planar silicene self-switching diodes. Quantum simulation results show that silicene SSDs can achieve current rectification ratios that exceed 200, without the need for doping or special passivation. This is a 30 fold improvement over what can be achieved with similar graphene devices. The presented findings suggest that silicene might offer an attractive platform for the realization of next generation field effect devices.

6.4 Methods

In order to capture silicene's buckling property, its atomic structure was optimized using the Density Functional Theory (DFT) as implemented in Atomistix Toolkit (ATK) package [77]. The Generalized Gradient Approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) functional was adopted to describe the exchange-correlation interaction [220]. The k-points mesh for the structural optimization was set to $21 \times 21 \times 1$ k-points. The Atomic positions and lattice constant were relaxed until all atomic forces were less than 0.01 eV/Å. A buckling height of 0.5 Å and an optimized lattice constant of 3.86 Å were obtained, showing good agreement with previous

studies[201, 221, 222]. The optimized structure of silicene was shown in Fig. 6.2(a). The insulating trenches were then formed in the silicene layer, and, for the hydrogen passivated devices, dangling bonds at the edges were then passivated with hydrogen. This process was conducted for all simulated device geometries prior to transport calculations.

Transport calculations were conducted on each device using the Extended Huckel method [76] and Non-Equilibrium Green's Function formalism [75] as implemented in ATK [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

The device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of $1 \times 10 \times 50$, with 50 sample points along the transport direction, and 10 points along the width (induced electric field direction). The same calculation method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

7 All-Graphene Planar Double Barrier RTDs

Resonant tunnelling diodes (RTDs) exhibit excellent high frequency performance, but suffer from the disadvantages of their complicated vertical structures. In this chapter, an atomically-thin all-Graphene planar Double Barrier RTD (DB-RTD) that can be realized within a single Graphene Nanoribbon (GNR) is proposed, overcoming this long-lived disadvantage of RTDs. The proposed device does not require any doping or external gating and can be fabricated using minimal process steps. The planar architecture of the device allows a simple in-plane connection of multiple devices in parallel without any extra processing steps during fabrication, enhancing the current driving capabilities of the device. Quantum mechanical simulation results, based on Non-Equilibrium Green's Function (NEGF) formalism and the Extended Huckel (EH) method, show promising device performance with a high reverse-to-forward current rectification ratio exceeding 50,000, and confirm the presence of Negative Differential Resistance (NDR) within the device's current-voltage characteristics.

7.1 Introduction

Graphene has triggered great excitement in the electron devices research community because of the new opportunities it brings forward through its atomically-thin structure and its unique electronic properties [11]. The lack of a bandgap in graphene has stood as a challenge for graphene-based field effect devices, however, it has opened new opportunities in analogue and RF electronics [223].

Diodes are very important components of analogue and RF electronics, and their realization with high performance would enable next generation RF systems and Terahertz detectors. Resonant tunnelling diodes (RTDs) are a family of diodes with unique capabilities, as they do not only act as rectifiers, but also exhibit Negative Differential Resistance (NDR). This NDR property enables a number of important applications, such as high frequency oscillators, ultra-fast logic devices and multi-state memory devices [38].

An RTD incorporates a barrier across which electrons tunnel. Complementing this barrier with another barrier can further enhance the device's performance, giving rise to a structure known as the double-barrier resonant tunnelling diode (DB-RTD) [34], which blocks the flow of electrons through the device but, counter intuitively, makes it transparent to the tunnelling of electrons at certain resonant energy levels. The fabrication of such a DB-RTD structure has been a great challenge as it requires vertical stacking of compound semiconductor heterostructures [34] or Si/SiGe layers [33], which involves great fabrication complexity. Also, since it is difficult to connect multiple of them in parallel due to their vertical structure and because conduction in them is driven by tunnelling only, they can only provide low peak current values.

This chapter proposes an all-Graphene planar DB-RTD which can be realized using a single Graphene Nanoribbon (GNR), without the need for doping [224], external gating[150], vertical stacking [196] or horizontal heterostructures [225] and requires minimum processing steps during fabrication. The planar architecture of the device also enables parallel interconnection of multiple devices in-plane without the need for any extra processing steps, enhancing the current driving capabilities of the device. The double barrier structure in the proposed device is formed by etching two insulating trenches across the width of a GNR, defining a graphene quantum dot in between them. The device structure is shown in Fig. 7.1, which illustrates the in-plane parallel connection of 4 devices, while Fig. 7.2(a) shows a single device.

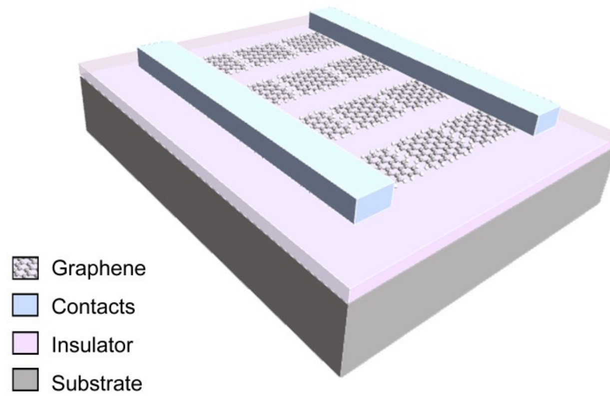

Figure 7.1 | A schematic diagram of planar all-Graphene Double Barrier Resonant Tunnelling Diodes, showing 4 devices connected in parallel.

The device's electronic properties and performance are studied using Nonequilibrium Green's Function (NEGF) formalism and the Extended Huckel (EH) method. The next section presents the simulation results, while the calculation method is described separately at the end of the chapter (Section 7.4).

7.2 Results and Discussion

The simulated device structure is shown in Fig. 7.2(a) and its calculated transmission spectrum at zero bias voltage is shown in Fig. 7.2(d). The device was constructed from an armchair GNR (aGNR) with a width of 8 carbon atoms, making it from the family of aGNRs that have widths of $3p+2$ carbon atoms (p is an integer). This family of aGNRs has vanishingly small band gaps or no band gaps at all [120] and hence can carry larger currents compared to other aGNRs ($3p$ and $3p+1$ families). The two insulating trenches were etched across the width of the nanoribbon and all dangling bonds were then passivated with hydrogen.

7.2.1 Transport Properties

It can be clearly seen from Fig. 7.2(d) that the double barrier structure gives rise to a very sharp transmission peak that allows the transmission of a very narrow range of energies. The peak is centred at -0.33 eV (0.33 eV below the Fermi level (ϵ_F)). At all other energies, the transmission probability is almost zero. This may be due to the extreme quantum confinement within the graphene quantum dot defined by the two insulating barrier trenches, which is confined from all three dimensions (thickness, width and length).

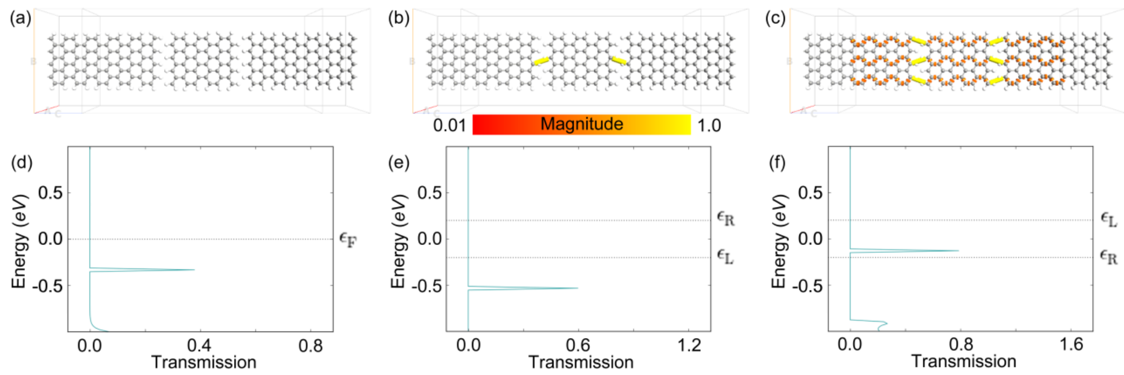

Figure 7.2 | Transport properties of planar all-Graphene DB-RTDs. (a) The planar Graphene DB-RTD device structure. (b) Transmission pathways plot of the device under forward bias (+0.4 V) and (c) reverse bias (-0.4 V). The colour bar represents the scale for the magnitude of the transmission pathway lines. (d) The transmission spectrum of the device with no applied bias. (e) The transmission spectrum of the device at +0.4 V bias and (f) -0.4 V bias. The left electrode is grounded and the bias voltage is applied to the right electrode.

When a positive bias voltage (+0.4 V) is applied across the device, as shown in Fig. 7.2(e), the transmission peak lies outside the bias window (the range of energies between the left (ϵ_L) and right (ϵ_R) electrode potentials) and hence no current flows through the device. This is further confirmed by the transmission pathways plot in Fig. 7.2(b) for the same bias voltage, which shows no continuous pathways within the device for current to flow through. On the other hand, when a negative bias voltage (-0.4 V) is applied, as shown in Fig. 7.2(f), the transmission peak appears within the bias window. This results in strong current flow through the device by means of tunnelling through the insulating trenches. This is also confirmed by the transmission pathways plot of Fig. 7.2(c) for the same bias voltage, which shows the presence of continuous pathways within the device and through the insulating trenches.

Figure 7.3(a) presents the calculated current-voltage (I-V) characteristics of the device of Fig. 7.2(a), showing enhanced reverse conduction and suppressed forward conduction, resulting in strong rectification. The I-V curve also shows an NDR effect between -0.6 V and -1.0 V. At the peak (-0.6 V) a strong resonance occurs with constructive interference near the trenches greatly enhancing the flow of tunnelling current through them as illustrated through Fig. 7.3(d), which is a transmission pathways plot of the device at -0.6 V bias. At the valley point (-1.0 V) this resonance effect disappears and the transmission pathways, shown in Fig. 7.3(e), settle back to their stable state, looking steady and continuous, as in Fig. 7.2(c).

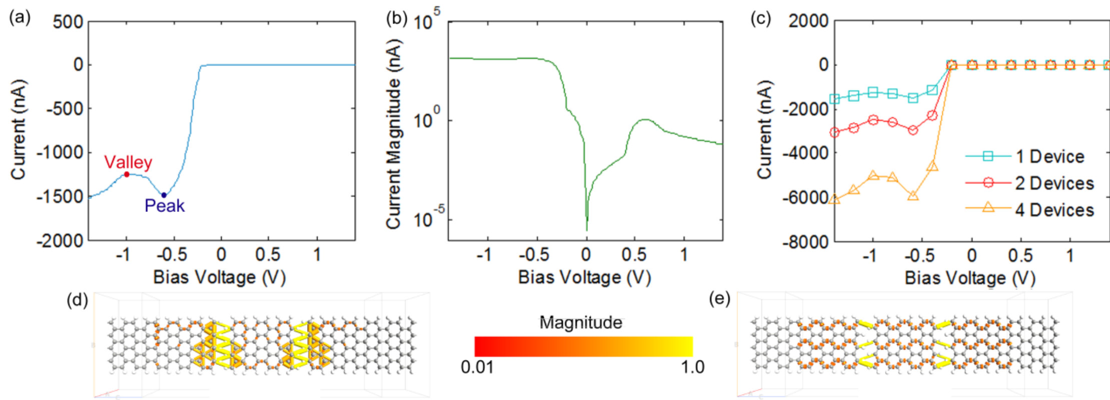

Figure 7.3 | Rectification and NDR in planar all-Graphene DB-RTDs. (a) Current-voltage (I-V) characteristics of the planar Graphene DB-RTD. (b) The I-V characteristics of the device with the current axis plotted in logarithmic scale. (c) I-V curves of one (squares), two (circles) and four (triangles) planar Graphene DB-RTDs connected in parallel. (d) Transmission pathways plot of the device at the peak point (-0.6 V) and (e) at the valley point (-1.0 V). The colour bar represents the scale for the magnitude of the transmission pathways.

The I-V curve of Fig. 7.3(a) is re-plotted in Fig. 7.3(b) with logarithmic scale for the current axis in order to clarify the ratio between reverse and forward currents. The figure suggests a very promising reverse-to-forward current rectification ratio that exceeds 50,000. Finally, Fig. 7.3(c) shows how the proposed in-plane parallel connection of multiple devices (Fig. 7.1) can greatly enhance the current driving capability of the device, which extends well into the µA range.

7.2.2 Fabrication Feasibility

The proposed all-Graphene DB-RTDs are two-dimensional (2D) planar devices, which do not require any external gating, doping or stacking of other material layers. Their fabrication can be achieved by the following steps. Once a Graphene monolayer is transferred to an insulating substrate, it can be patterned into the planar DB-RTD structure using a single photo-lithography step. Metallic contacts such as platinum or gold, as shown in Fig. 7.1, are then formed. It is important to note that the process described above gives rise to GNRs with rough edges [158], and may not be able to define narrow trenches for the insulating barriers. Before volume fabrication, the performance of such devices would require a Monte Carlo simulation study, in order to investigate the effect of GNR edge roughness on the device's performance, specifically its resonant behaviour. Such a statistical reliability study is an important further step required before the mass production of such devices.

Nevertheless, the experimental realization of small production volumes of the devices proposed here may be achieved by first realizing GNRs with smooth edges, and then precisely etching the insulating trenches within them. The experimental realization of GNRs with smooth edges has proven to be a challenge, however, recent work has shown promising results towards achieving this goal [51, 109, 113, 114, 119, 156, 157], and a number of experimental reports have reported techniques to achieve this [119, 156, 157]. As for the precise etching of the insulating trenches, this may be performed using Helium Ion Beam lithography [52-54] or single-atom catalyst chiselling [51], both of which have been able to achieve high resolution patterning of Graphene.

7.3 Summary

This chapter proposed a new planar all-Graphene DB-RTD that greatly outperforms other types of DB-RTDs by its high reverse-to-forward current rectification ratio, which exceeds 50,000. The device involves minimal processing steps during fabrication and offers a high current driving capability through its in-plane parallel connection. The transmission spectrum of the device suggests that the device allows the transmission of electrons within a very narrow energy window, and blocks conduction at all other energies. The device also exhibits NDR behaviour due to resonant tunnelling through the insulating trenches, and hence can have a potential not only in analogue and RF applications but also in ultra-fast multi-state logic and memory devices.

7.4 Methods

Transport calculations conducted on the device were based on the EH method [76] and NEGF formalism [75] as implemented in Atomistix Tool Kit (ATK) [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

The device geometry was optimized and the coordinates were relaxed using the *Tersof* potential [79] until forces on individual atoms were smaller than 0.001 eV/Å^2. The device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1 x 20 x 50, with 50 sample points along the transport direction, and 20 points along the width. The same method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

8 ALL-GRAPHENE PLANAR DOUBLE-QUANTUM-DOT RTDS

This chapter proposes a new class of Resonant Tunnelling Diodes (RTDs) that are planar and realizable with a single graphene nanoribbon. Unlike conventional RTDs, which incorporate vertical quantum well regions, the proposed devices incorporate two confined planar quantum dots within the single graphene nanoribbon, giving rise to a pronounced Negative Differential Resistance (NDR) effect. The proposed devices, termed here as planar double-quantum-dot RTDs, and their transport properties are investigated using quantum simulations based on Nonequilibrium Green's Function (NEGF) formalism and the Extended Huckel (EH) method. The proposed devices exhibit a unique current-voltage waveform consisting of a single pronounced current peak with an extremely high, in the order of 10^4, peak-to-valley ratio. The position of the current peak can be tuned between discrete voltage levels, allowing digitized tunability, which is exploited in realizing multi-peak NDR devices.

8.1 Introduction

Due to its exceptional electronic properties [3, 95, 97], graphene has become a popular candidate for next generation electronics [5, 104]. However, its lack of an electronic bandgap stands as an obstacle towards realizing high performance graphene field effect devices [95]. Accordingly, much effort has been directed towards the realization of graphene tunnelling devices [97, 196, 226], which are promising candidates for next-generation electronics [227]. Graphene tunnelling devices can achieve very high on-off ratios [97], an essential property for efficient switching. However, their full potential lies in achieving resonant tunnelling [228], which gives rise to a property known as Negative Differential Resistance (NDR) . This property enables devices that can be used as ultra-fast multi-state logic and memory devices [38] as well as high frequency oscillators and multipliers operating well into the Terahertz regime [34, 36, 229].

An essential component of any tunnelling device is the barrier across which electrons tunnel. This barrier can be a traditional insulating material deposited on top of graphene or another 2D material such as hexagonal Boron Nitride (hBN) [97, 228, 230, 231]. However, such an approach gives rise to a vertical device, which requires vertical stacking and precise alignment of multiple graphene layers.[10] Moreover, the introduction of multiple barriers within such a device, in order to realize a double barrier resonant tunnelling diode (DB-RTDs) [232], requires further stacking and alignment of more graphene layers. In order to overcome such a drawback, an in-plane barrier was previously proposed in chapter 7, by incorporating an insulating trench in a graphene nanoribbon (GNR) along its transport direction [85], giving rise to a completely planar device architecture; a planar all-graphene DB-RTD [85]. This chapter builds upon the previous work presented in chapter 7 [85].

Double barrier RTDs are able to achieve enhanced NDR due to the presence of a quantum confinement region within them, the region defined by the double barriers, in which electrons resonate. In conventional vertical DB-RTDs [34, 36, 229, 232], this is referred to as a quantum well, and is usually a thin semiconductor layer sandwiched vertically between two layers of another material with a larger bandgap. In the proposed planar all-graphene DB-RTDs [85], the quantum well region is replaced by a length of the GNR that is isolated by the in-plane insulating trenches, forming a confining structure; a zero-dimensional graphene quantum dot [233], as shown in Fig. 8.1(a).

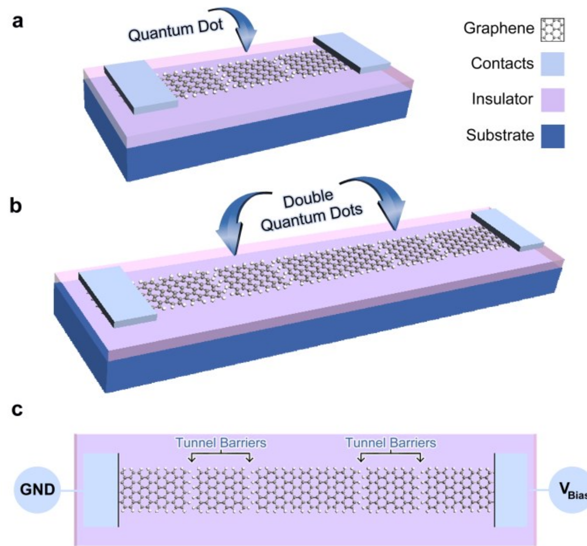

Figure 8.1 | Planar all-graphene double-barrier (single-quantum-dot) and double-quantum-dot resonant tunnelling diodes (RTDs). (a) 3D perspective views of the single-quantum-dot RTD and (b) the double-quantum-dot RTD, highlighting the positions of the quantum dots. (c) Top view of the device in (b) showing the bias direction and highlighting the position of the tunnel barriers.

In this chapter a new class of RTDs is presented based on the concept of cascading two planar graphene quantum dots within a single device, as shown in Figs. 8.1(b) and 8.1(c), which gives rise to a planar all-graphene double-quantum-dot RTD with unique current-voltage characteristics. The transport properties of this proposed device are studied using Nonequilibrium Green's Function (NEGF) formalism [75] and the Extended Huckel (EH) method [76]. The presented results show that the coupling of two quantum dots together, within the same nanoribbon, allows the flow of current at specific bias voltages, only when both dots couple coherently, preventing the flow of current at all other voltages. This gives rise to a giant NDR effect that takes the shape of a current-voltage (I-V) waveform consisting of a single pronounced current peak.

An important measure of NDR is the peak-to-valley current ratio (PVCR), which needs to be maximized. The presented quantum simulation results show that the proposed devices exhibit extremely high PVCR of 50,000, greatly outperforming both experimental reports and theoretical predictions for solid-state [33, 34, 36, 85, 86, 150, 224, 228, 229, 232, 234, 235] and molecular electronic devices [142, 236-240].

Furthermore, it is also shown that due to the planar architecture of the proposed device, the voltage at which the current peak appears can be tuned by appropriately choosing the dimensions of the quantum dots. Due to the presence of quantized energy states

within the quantum dots, the position of the current peak is restricted to specific discrete voltage levels, which enables digitized tunability of its position. By exploiting this property, a multi-peak NDR effect device is presented, using an in-plane parallel connection of multiple tuned devices at no extra fabrication steps.

The presented findings suggest that the proposed devices have unique properties that may facilitate new important electronic devices and components. In the next section, the simulation results are presented and discussed. The section begins by comparing all-graphene planar double-quantum-dot RTDs with all-graphene planar DB-RTDs, which will be referred to in subsequent text as single-quantum-dot RTDs. Then the effect of tuning the dimensions of the quantum dots on the device's I-V characteristics is studied, showing how they can be used in order to achieve a multi-peak NDR effect device. Finally, a number of suggested fabrication strategies are discussed.

8.2 Results and Discussion

8.2.1 Transport Properties

In this section the transport properties of a planar all-graphene double-quantum-dot (Double QDot) RTD are studied and compared with those of a planar all-graphene single-quantum-dot (Single QDot) RTD. Both simulated device structures are shown in Fig. 8.2(b). The transport properties of both devices are summarized in Fig. 8.2.

In the single-quantum-dot RTD, the barriers allow the tunnelling of electrons within a narrow energy range only, whilst blocking them at all other energies, as shown in Fig. 8.2(a), which illustrates the transmission probability of electrons at different energy levels for the single-quantum-dot RTD under zero bias. The figure shows that the transmission probability of electrons at all energies is almost zero, except within a narrow energy window within which resonance occurs, giving rise to the single resonance peak at 0.33 eV below the Fermi level (ϵ_F) of the device. At this energy level of -0.33 eV, the probability of electron transmission across the whole device reaches almost 0.4. On the other hand, for the double-quantum-dot RTD, the presence of the second quantum dot within the same nanoribbon allows coherent coupling with the first quantum dot, facilitating stronger tunnelling across the nanoribbon, and making the device almost completely transparent to the transmission of electrons at the resonance peak at which the transmission probability reaches a much higher value of 0.98, as shown in Fig. 8.2(c).

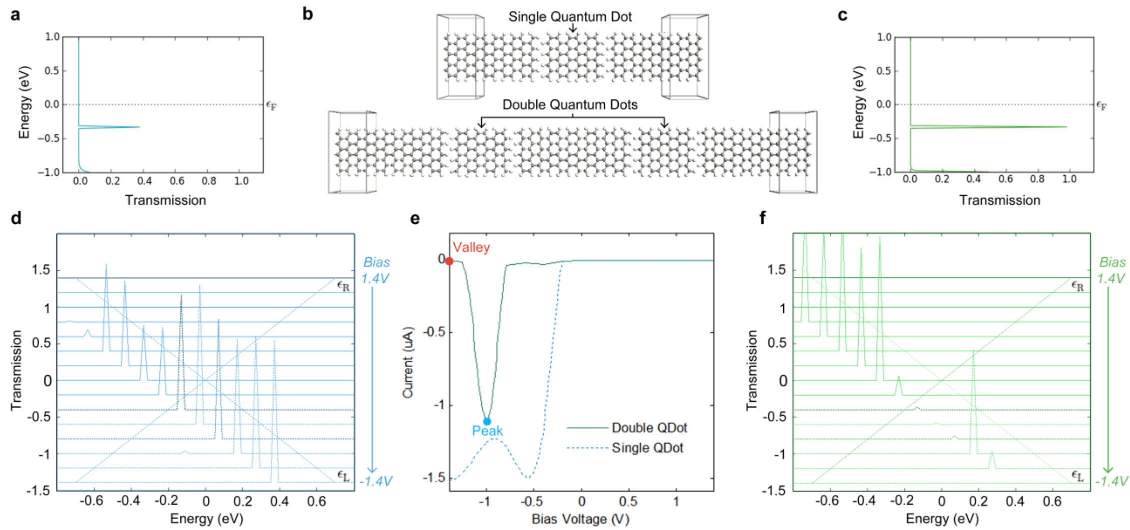

Figure 8.2 | Comparison of the transport properties of planar all-graphene single and double-quantum-dot RTDs. The structures of the simulated planar all-graphene single-quantum-dot and double-quantum-dot RTDs are shown in (b) illustrating how a double-quantum-dot RTD can be constructed by cascading two single-quantum-dot RTDs in series within a single graphene nanoribbon. Plots of Energy vs. Transmission probability at zero bias are shown for (a) the single-quantum-dot RTD, and (c) the double-quantum-dot RTD. A spectrum of transmission probability vs. energy plots obtained at different bias voltages for (d) the single-quantum-dot RTD and (f) the double-quantum-dot RTD. The bias voltage range extends from -1.4 V to 1.4 V, with the lowest plot for a bias of -1.4 V and the highest for a bias of 1.4 V, with increasing 0.2 V steps in between. The region between the Fermi level of the left electrode (ϵ_L) and that of the right electrode (ϵ_R), which are illustrated by the diagonal dotted lines, represents the bias window. (e) The current voltage characteristics of the single-quantum-dot RTD –dotted blue line– and the double-quantum-dot RTD –solid green line– plotted on the same axes. Peak and valley current points for the double-quantum-dot RTD are marked with blue and red dots respectively.

In order for current to flow through the devices, a bias voltage needs to be applied to each of the two devices. In order to investigate the effect of bias voltage on the transport properties of the devices, the transmission spectra of both devices were calculated for a range of bias voltages, and the results are summarized in Figs. 8.2(d) and 8.2(f) for the single-quantum-dot RTD and the double-quantum-dot RTD respectively.

As Fig. 8.2(d) suggests, for the single-quantum-dot RTD, the bias window either extends above the Fermi level and away from the transmission peak resulting in no current flow under forward bias, or extends below the Fermi level capturing the transmission peak and allowing the flow of current through the device under reverse bias. This effect results in rectification, as shown in Fig. 8.2(e).

On the other hand, for the double-quantum-dot RTD, as suggested by Fig. 8.2(f), the transmission peak also lies outside the bias window under forward bias, resulting in no

current flow through the device, similar to the single-quantum-dot RTD case. However, under reverse bias the effect of the second quantum dot appears and an interesting phenomenon manifests itself. The transmission peak disappears for most negative bias voltages and only appears within a narrow bias voltage range. This indicates that when the two quantum dots resonate, they result in destructive interference that causes the transmission peak to disappear. Coherent coupling between the two quantum dots only occurs within a narrow voltage range, giving rise to the enhanced transmission peak seen in the transmission spectrum for a bias voltage of -1.0 V, as shown in Fig. 8.2(f).

The coupling effect of the double-quantum-dots results in a very unique I-V curve that comprises a single pronounced current peak with a giant NDR effect, as shown in Fig. 8.2(e). This current peak (marked with a blue dot on the figure) reaches a very high value above the 1 μA point. A high current peak in the μA range, is uncommon in tunnelling devices, and is highly favourable, especially for a nanoscale RTD, as it enhances the amount of power that the device is capable of delivering to a connected load.

Past the peak point, current begins to decrease continuously until it reaches the valley point (marked with a red dot on the figure) at which the current magnitude reaches below 1 nA (quantified later on in Fig. 8.3(f)), representing an extremely high peak-to-valley current ratio (PVCR) in excess of 1000.

8.2.2 Current Peak Tunability

In this subsection the effect of varying the quantum dot length within the double-quantum-dot RTD structure is investigated by constructing 4 different double-quantum-dot RTD geometries. The four geometries are shown in Figs. 8.3(a), 8.3(b), 8.3(c) and 8.3(d) and are constructed from identical nanoribbons that have equal widths and lengths. The difference between the four geometries is the length of the quantum dots, being 8, 10, 12 and 14 carbon atoms long for the devices of Figs. 8.3(a), 8.3(b), 8.3(c) and 8.3(d) respectively. The overall length of all devices was kept constant.

The current-voltage characteristics of the four devices are shown in Fig. 8.3(e). Interestingly, the single current peak waveform is achieved consistently for all the four device geometries, confirming its reproducibility.

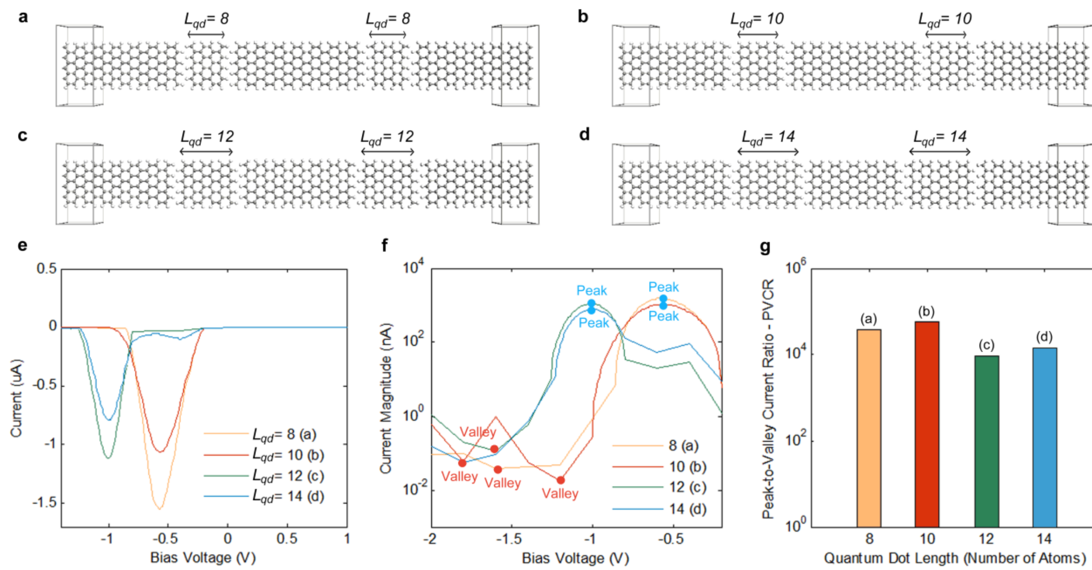

Figure 8.3 | Giant tuneable NDR effect in planar all-graphene double-quantum-dot RTDs. Four device geometries are shown with equal nanoribbon width and length, but with varying quantum dot lengths of (a) 8, (b) 10, (c) 12 and (d) 14 atoms. The I-V characteristics for the four devices are shown in (e), while a zoom-in at their reverse bias I-V characteristics is shown in (f) with the current axis plotted in log-scale in order to highlight the very low valley current points for all devices. Peak and valley current points are marked with blue and red dots respectively. Achieved PVCR values for the four devices are shown through the bar chart in (g), confirming a consistently high PVCR that exceeds 10^4 in all devices.

More interestingly, the plot of Fig. 8.3(f), with current plotted in logarithmic scale, illustrates that the achieved peak-to-valley current ratio for the four devices is extremely high at values that consistently exceed four orders of magnitude. The valley current levels reach values down to tens of pico-amps, a feature that would be highly desirable for ultra-low power operation in logic and memory devices. Figure 8.3(g) summarizes the achieved PVCR for the 4 devices and suggests that not only do they all achieve PVCR values above 10^4 but also, as with the device of Fig. 8.3(b), can reach values close to 10^5 (50,000 in this case).

A very important observation is noted from Fig. 8.3(e) regarding the position of the current peak. The device of Fig. 8.3(a), with a quantum dot length of 8 atoms, has the current peak centred at -0.6 V. Increasing the length of the quantum dot to 10 atoms, as in the device of Fig. 8.3(b), does not affect the position of the current peak, keeping it centred at -0.6 V. However, a further increase in the length up to 12 atoms, results in a shift in the position of the current peak towards higher voltages, making it centred around -1.0 V. In contrast, another further increase in the length of the quantum dot to 14 atoms does not result in another shift, maintaining the centre of the peak at -1.0 V

once again. This suggests that a trend is emerging which is investigated by studying more devices with L_{qd} ranging from 6 atoms to 16 atoms, and the results are summarized through the plot of Fig. 8.4.

Figure 8.4 maps the current peak position to the length of the quantum dots in atoms. The resulting curve takes a staircase-like shape that indicates the presence of highly quantized energy states within the quantum dots, which limit the shifting of the position of the current peak from and to specific discrete voltage levels. In the next subsection this interesting behaviour is exploited in achieving an exciting property; multi-peak NDR. However, it is also worth pointing out that this behaviour has interesting implications on the fabrication of such devices, as it allows tolerance to fabrication errors, in the range of atoms (± 1 atom), that arise when defining the quantum dots within the GNRs. The fabrication method is discussed in more details in the fabrication feasibility subsection later on.

8.2.3 Multi-Peak Negative Differential Resistance Effect

While the shifting trend of the current peak can provide interesting insights into the quantum behaviour of the devices, the fact that it can be shifted between discrete voltage levels allows digitized tunability, giving rise to a tuneable NDR effect. This digitized tunability property, coupled with the planar architecture of the devices, indicates a very interesting device capability that is not possible with field effect devices and very difficult to achieve with vertical tunnelling devices [33, 36, 97, 227, 228, 230, 231]; multi-peak NDR [38, 234, 236, 239].

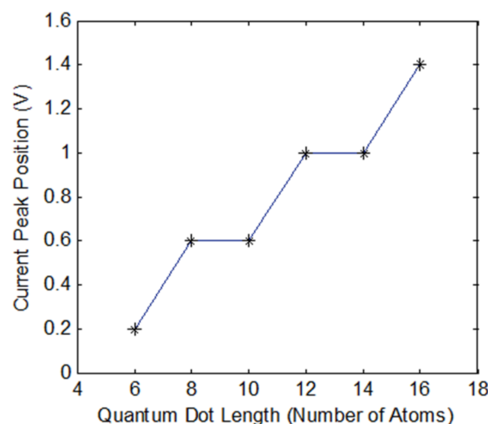

Figure 8.4 | Digitized Tunability of the current peak position using quantum dot length variation. The figure maps the current peak position in Volts to the length of the quantum dots in number of atoms. By varying the length of the quantum dots the current peak position can be tuned across a wide voltage range between discrete voltage levels.

Multi-peak NDR enables exciting device functionalities such as multi-state logic and memory [38, 39] as well as very high frequency multiplication and oscillation [34, 36, 229]. Multi-peak NDR is hard to achieve in vertical tunnelling devices due to the associated complexity in fabrication and results in low PVCR values. However, using the proposed planar double-quantum-dot RTDs a multi-peak NDR effect can be achieved by connecting two double-quantum-dot RTDs in parallel through an in-plane parallel connection, facilitated by their planar architectures, as shown in Figs. 8.5(a) and 8.5(b). One device is tuned to exhibit a current peak at a certain voltage position (-0.6V), while the other is tuned to exhibit the current peak at a different voltage position (-1.0V).

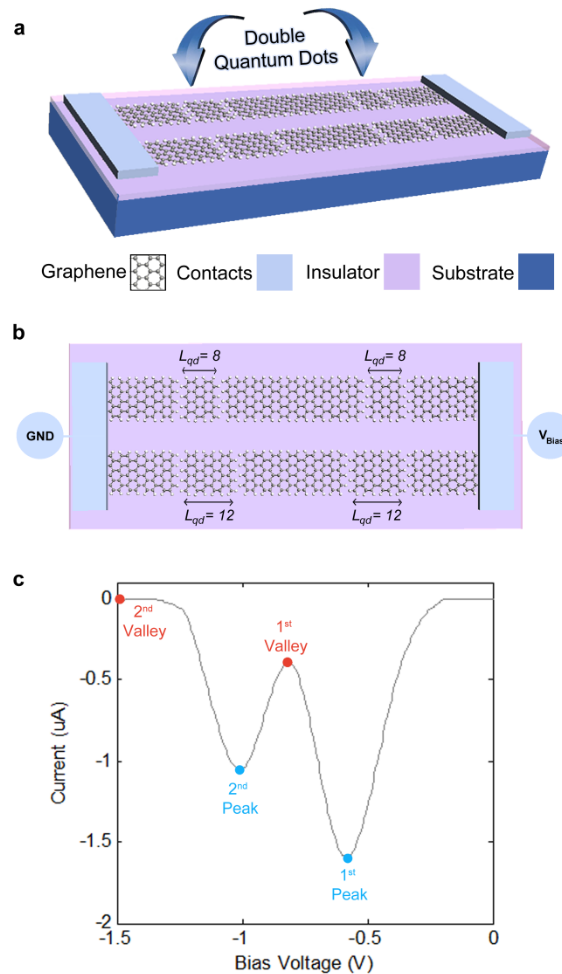

Figure 8.5 | Multi-peak NDR effect in parallel planar all-graphene double-quantum-dot RTDs. (a) A perspective view and (b) a top view of two double-quantum-dot RTDs connected in parallel through an in-plane parallel connection. The two devices have different quantum dot lengths (8 and 12 carbon atoms) resulting in different current peak positions and, when connected in parallel, achieve a multi-peak NDR effect, with two pronounced NDR peaks and high peak current values in the micro-amps range, as shown through the device's current-voltage characteristics in (c). Peak and valley current points are marked with blue and red dots respectively.

The I-V characteristics of the overall device are shown in Fig. 8.5(c), and exhibit two pronounced NDR peaks that are clearly distinguishable. In principle this concept can be applied to a larger number of devices in order to achieve a larger number of multiple peaks, without introducing any extra fabrication steps.

8.2.4 Fabrication Feasibility

The proposed devices are planar devices that do not require any external gating, doping or stacking of material layers. Their fabrication can be achieved by the following steps. Once a Graphene monolayer is transferred to an insulating substrate, it can be patterned into the device structure using a single photo-lithography step. Metallic contacts such as platinum or gold, as shown in Figs. 8.1 and 8.5, are then formed. It is important to note that this process gives rise to GNRs with rough edges [158], and may not be able to define narrow trenches for the tunnel barriers. Before volume fabrication, the performance of such devices would require a Monte Carlo simulation study, in order to investigate the effect of GNR edge roughness on the device's performance, specifically its resonant behaviour.

Nevertheless, the experimental realization of small production volumes of the devices proposed here may be achieved by first realizing GNRs with smooth edges, and then precisely etching the insulating trenches within them using high precision etching techniques. The experimental realization of GNRs with smooth edges has proven to be a challenge, however, recent work has shown promising results towards achieving this goal [51, 109, 113, 114, 119, 156, 157], and a number of experimental reports have reported techniques to achieve this [119, 156, 157]. As for the precise etching of the insulating trenches, this may be performed using Helium Ion Beam lithography [52-54] or single-atom catalyst chiselling [51], both of which have been able to achieve high resolution patterning of Graphene.

Any remaining fabrication errors that arise as a result of using such high resolution methods are expected to be in the order of atoms, and such small errors are expected to be tolerable in the proposed devices due to the reproducibility of their NDR effect with varying quantum dot lengths, as was suggested earlier through Fig. 8.3, and due to the fact that the position of the current peak in them does not shift if the length of the quantum dot is made an atom or two more than what it was designed for, as was suggested earlier through Fig. 8.4. Nevertheless, further experimental efforts are a very important step towards consolidating these very interesting physical insights.

8.3 Summary

In summary, a new class of planar NDR devices was presented, termed as planar all-graphene double-quantum-dot RTDs, which can be realized completely within single graphene nanoribbons. Quantum simulation results have shown that such devices exhibit a very interesting property of having a single pronounced current peak in their I-V characteristics, resulting in a giant NDR effect that exhibits PVCR values exceeding four orders of magnitude. Such a property takes place due to destructive interference between the cascaded quantum dots, which only couple coherently within a narrow bias voltage range, under which current conduction occurs. By tuning the dimensions of the quantum dots the voltage at which this coherent coupling occurs can be tuned, allowing tunability of the current peak position. Due to the presence of quantized energy states within the quantum dots, the current peak position can only be tuned between discrete voltage levels, enabling digitized tunability. It was shown how this property can be exploited in order to achieve a multi-peak NDR effect device through an in-plane parallel connection of multiple tuned devices. The findings presented here suggest a promising potential for the application of planar all-graphene double-quantum-dot RTDs in next generation electronics.

8.4 Methods

Transport calculations conducted on the device were based on the EH method [76] and NEGF formalism [75] as implemented in Atomistix Tool Kit (ATK) [77] and as described in depth earlier in the main methods section of chapter 1 (Section 1.5).

The device geometry was optimized and the coordinates were relaxed using the *Tersof* potential [79] until forces on individual atoms were smaller than 0.001 eV/Å^2. Each device structure was partitioned as three regions: semi-infinite left electrode (L), central scattering region (C), and semi-infinite right electrode (R). The mesh points in real space calculation were defined as uniformly spaced k points of 1 x 20 x 50, with 50 sample points along the transport direction, and 20 points along the width. The same method was used in previous published work [85, 86, 88] and is described in depth in the main methods section presented earlier in chapter 1 of this thesis (Section 1.5).

9 CONCLUSIONS

This thesis proposed a new approach for the conceptualization of nanoelectronic devices, based on exploiting 2D nanomaterials as a platform for the realization of completely 2D planar device architectures. Using this approach, new classes of nanoelectronic devices, achieving different types of device functions, were conceptualized and studied theoretically using quantum mechanical simulations. The presented devices were atomically-thin with sub-10 nm dimensions and were able to achieve rectification, Negative Differential Resistance (NDR) operation and single biomolecule detection, promising a potential for complementing as well as revolutionizing electronics. The planar 2D architecture of the devices enabled their implementation using a range of different 2D nanomaterials, including Graphene, MoS_2 and Silicene. Each of these nanomaterials offered different advantages that stem from different attributes such as unique electronic properties, economical synthesis methods or unique structural properties. This chapter summarizes the findings presented earlier and recommends a number of future work suggestions. Finally, this chapter concludes the thesis by discussing a number of potentially greater-impact long-term opportunities and advantages that planar 2D nanoelectronic devices may offer in the future, which could potentially revolutionize the future electronics roadmap.

9.1 Summary

At the beginning of this thesis, in section 1.3, a research question that addresses three main research enquiries was put forth, and in order to address these enquiries, three main research objectives were set. In this section, the findings related to these three objectives are summarized and used to draw conclusions on the three main research enquiries that these objectives were set for.

First Enquiry: *Can 2D nanomaterials complement and advance electronics?*

First Objective: *Realization of nanoscale rectifiers using 2D nanomaterials*

This first objective received greater focus compared to the other two objectives, mainly due to the fact that findings related to it may directly be materialized into beneficial applications, with lower risk and less reliance on other unknown variables. This objective was addressed through four out of the seven contributing chapters of this thesis. These chapters were***, Chapters Two, Five, Six and Seven***.

In chapter two, a new class of rectifiers was proposed, the Graphene Self Switching Diode (G-SSD), and showed excellent rectification capabilities. Graphene's unique property of behaving as a semimetal as well as a semiconductor, when etched down into narrow nanoribbons, enabled the realization of a new enhanced class of SSDs that were not possible with other types of materials; the Graphene Self-Switching Metal-Insulator-Semiconductor Field Effect Diode (G-SS MISFED). After optimization of device dimensions and use of nitrogen passivation as a novel method for limiting unwanted tunnelling current and introducing extra charge carriers into the device, the G-SS MISFED showed a very high rectification ratio in excess of 5,000. Such a rectification ratio is high compared to previously reported rectification ratios in SSDs, however, the fact that it can be achieved using a device with sub-10 nm dimensions and single atomic thickness was the most interesting finding.

The work presented in this thesis related to G-SSDs, which was also disseminated earlier to the public domain through a number of publications (papers 1, 8 and 9 in the list of derived publications presented in section 1.7), triggered a number of efforts aimed at the fabrication and experimental realization of such devices. Notable recent work demonstrated G-SSDs as zero-bias microwave detectors [123], detecting microwave signals with frequencies up to 67 GHz. The fabricated devices had a channel length close to a micrometre but were still able to detect relatively high frequencies. It is

expected that if the length of the channel is reduced down to the nanoscale, as with the simulated devices in chapter 2, much higher frequencies, up to the Terahertz, may be detected. Furthermore, the fabricated devices were realized using minimal process steps, consolidating their potential for integration with standard electronics.

Chapters five and six explored the use of other types of 2D nanomaterials for the realization of SSDs. In chapter five, it was shown that MoS_2 can be used for the realization of nanoscale SSDs with notable rectification ratios up to 70. Although not as good as graphene, such devices may outperform their graphene counterparts if the problem of tunnelling current is dealt with using different passivation methods. Nevertheless, MoS_2 still offers advantages, mainly due to its direct wafer scale synthesis methods, which may enable the integration of MoS_2 SSDs with standard electronics or their use in flexible and transparent electronics applications. In chapter six, it was shown that silicene may offer great opportunities for the realization of SSDs, as well as other types of planar 2D field effect devices, due to its buckling property. Buckling enables highly effective conductance modulation in planar silicene field effect devices, such as SSDs, which would outperform similar graphene devices by a 30 fold enhancement. However, progress in silicene synthesis methods is highly needed at this stage before reliability of silicene devices can truly be assessed. Nevertheless, the fact that silicene is an allotrope of silicon may also open up future opportunities for possible integration of silicene devices with silicon-based electronics.

Finally, chapter seven, addressed the first research objective using another device concept; planar 2D Resonant Tunnelling Diodes (RTDs). A new class of RTDs was proposed and termed as an all-graphene planar Double Barrier RTD (DB-RTD), showing very promising performance as a nanoscale rectifier. The device, unlike conventional vertical RTDs, exhibits a planar architecture that requires minimal process steps during fabrication, and promises an extremely high rectification ratio in excess of 50,000. The planar structure of the device enables the in-plane parallel connection of multiple devices at no extra fabrication steps, boosting the device's current driving capabilities.

Based on the above findings, it can be concluded that 2D nanomaterials can truly complement and advance standard electronics on the short term, and a very promising path towards achieving this endeavour would be through adopting the proposed device conceptualization approach presented in this thesis.

Second Enquiry: *Can 2D nanomaterials potentially revolutionize electronics?*

Second Objective: *Realization of nanoscale NDR devices using 2D nanomaterials*

This second objective was addressed through ***Chapters Three and Eight*** of this thesis. It was tackled through capitalizing upon the findings obtained from the first objective. This strategy, of exploring new materials and new devices through first applying them in low-risk beneficial applications that address unfulfilled needs, even if these were narrow niche applications, then capitalizing on the accomplished achievements in trying to tackle higher-risk higher-potential research enquiries, such as the one set here, may prove to be an efficient strategy when trying to revolutionize an already well-established technology or application, such as digital electronics.

In chapter three, the G-SSD proposed and studied in chapter two, was altered and reformed in order to achieve the desired device functionality; Negative Differential Resistance (NDR) operation. This was achieved through exploiting the same property of graphene, which was earlier exploited in order to realise the G-SSD MISFED. By asymmetrically gating the G-SSD, with one side gate being a semi-metallic Graphene Nanoribbon (GNR) while the other being a semiconducting GNR, asymmetrical tunnelling current from the side gates was used in order to control the conductivity of the channel of the G-SSD in an unconventional manner, giving rise to a pronounced NDR effect with high peak current values.

In conventional NDR devices, small tunnelling current is usually the driving mechanism for NDR, however, in the proposed devices, it is only a controlling mechanism that triggers a much larger channel conduction current that is capable of driving much larger loads. The above advantage, added to the planar architecture of the device, which requires minimal process steps for fabrication, open up opportunities that were not possible previously. Such a device may be applied in order to realize Terahertz oscillators, complementing and integrating with standard electronics, or could also potentially be used for the realization of logic and memory devices that could revolutionize electronics.

In chapter eight, the concept of the DB-RTD proposed and studied earlier in chapter seven, was exploited in order to conceptualize a new class of RTDs; the all-graphene planar Double-Quantum-Dot RTD. This new class of devices was shown to exhibit unique transport properties that give rise to a highly pronounced NDR effect, with extremely high unreported peak-to-valley current ratios in excess of 50,000. Such high

peak-to-valley current ratios can open up great opportunities for the realization of multi-state logic and memory devices. This fact, also added to the planar architecture of the devices, and their nanoscale dimensions, may allow the realization of high density device arrays, which could enable highly dense memories and integrated circuits. The ability to achieve a multi-peak NDR effect through an in-plane parallel connection of multiple tuned devices, at no extra fabrication steps, also opens up opportunities for realizing multi-state logic and memory devices with a wider range of multiple states, rather than two or three states only. This could have important implications on digital electronics and the digital processing of signals, which may truly revolutionize electronics.

Another important research forefront that promises a great potential for revolutionizing electronics, which has not been touched upon throughout this thesis, is the realization of spin-based devices using 2D materials. Spin-based devices have the potential to address some of the bottleneck challenges facing the electronics industry, such as the increased power dissipation in integrated circuits. Silicene and MoS_2 exhibit interesting properties that may be exploited for the realization of high performance spin-based devices. For example, silicene exhibits strong spin-orbit coupling [241], which may lead to transport phenomena like the spin Hall Effect [242, 243] and quantum anomalous Hall effect[244, 245]. Other interesting properties of graphene include the presence of other spin-like degrees of freedom, such as valley spin, which may lead to valleytronic devices [246] and valley-polarized current generation [247].

While it is difficult to conclude a definitive answer for the broad research enquiry set here, the findings presented above do provide strong indications on a range of new opportunities that 2D materials, and 2D devices based on them, bring forth to the electronics industry, which may potentially revolutionize it. Further experimental efforts for the realization and application of the presented devices in new systems that exploit their unique properties would consolidate these findings and open-up further opportunities. However, although it was shown how the proposed device conceptualization approach can lead to some new exciting opportunities, such as the proposed NDR devices, this approach may open up even greater opportunities and advantages that would pave the way towards revolutionizing electronics even more, and these are touched upon in the final section of this chapter in section 9.3.

Third Enquiry: *Can 2D nanomaterials offer new opportunities for the interaction and integration of electronics with other types of systems?*

Third Objective: *Realization of single biomolecule detection devices using 2D nanomaterials*

This objective was addressed in ***Chapter Four*** of the thesis. Once again, findings obtained in previous chapters, specifically with reference to chapters two and three, proved to be very valuable when trying to address this objective. Although the research did not initiate from these previous works, the research was greatly enriched through the findings obtained earlier.

In chapter four, the first 2D planar tuneable graphene nanopore device was proposed, through applying the concept of a G-SS MISFED on a graphene nanopore device. The proposed tuneable graphene nanopore device can also be viewed as an enhancement of the applicability of self-switching diodes to the field of biosensing for the first time. The newly introduced capability of tuneability in the proposed tuneable graphene nanopore devices was shown to be a highly effective method of increasing their sensitivity to the detection of single biomolecules. This was achieved by tuning the device's overall conductance to values that are comparable to the changes in conductance caused by the translocation of the single biomolecules. In this chapter, the translocation of glycine, being the smallest amino acid, was investigated; however, the principle should also be valid for larger biomolecules, which are expected to cause larger changes to the conductance of the nanopore device, as a result of their translocation.

Passivating the device with nitrogen was shown to be a very effective way of increasing the sensitivity of the device to the electrostatics within the single biomolecules that translocate through the nanopore. Glycine was once again investigated, and it was shown how the device was able to sensitively detect the carboxyl group within the glycine molecule, which carries a charge equivalent to a single electron.

It is important to note that the study presented in this chapter assumed a number of idealities, which need further verification (addressed in future work, section 9.2), before any conclusion can be drawn about the reliability of such devices for DNA or protein sequencing applications. Nevertheless, the presented findings strongly indicate that 2D planar nanodevices, based on 2D nanomaterials, can potentially offer a number of exciting opportunities for interaction with other types of systems, such as biological systems, in ways that may have not been possible before.

9.2 Future Work

In this section, a list of recommendations for future work is presented, providing starting points for building up on the work presented in each of the seven contributing chapters (chapters 2 – 8). These recommendations are presented in point-form for each individual chapter.

Chapter Two:

- Fabrication of G-SSDs and G-SS MISFEDs at nanoscale dimensions using the proposed fabrication methods in chapter two and their characterization as microwave and Terahertz detectors.
- Investigation of passivation using different materials, such as boron or fluorine, in order to obtain p-type devices that rectify in the third quadrant.
- Investigation of three-terminal all-graphene planar MISFETs, Metal-Insulator-Semiconductor Field Effect Transistors, in which both the left and right terminals of the device are separated from the side gate by insulating trenches.
- Investigation of the possibility of realizing all-graphene planar complementary MISFETs, using different passivation methods.
- Calculation of the charge distribution and accumulation within the device in order to show the variation of the depletion width and predict the threshold voltage of the device.
- Derivation of analytical models and/or theoretical frameworks that describe the operation of G-SSDs and G-SS MISFEDs in order to predict their performance and allow their comparison with quantum mechanical simulation results enabling the validation and identification of the most efficient quantum mechanical simulation approach for simulating such devices. This may also enable the prediction of the depletion and pinch-off of the graphene channel.
- Derivation and extraction of compact device models for G-SSDs and G-SS MISFEDs to enable investigating the application of these devices in different circuit topologies.

Chapter Three:

- Fabrication of asymmetrically gated G-SSDs, with nanoscale as well as micro scale dimensions, using the two proposed fabrication methods and characterization of their transport properties.

- Investigation of the effect of widening the insulating trenches on the tunnelling current from the side gates and its overall effect on the device's transport properties.
- Calculation of the charge distribution and accumulation within the device in order to show the variation of the depletion width, validate the proposed physical understanding and aid in the derivation of an analytical model and/or a theoretical framework that can predict the sharpness of the NDR peak as well as the bias voltage where it occurs.
- Derivation and extraction of compact device models for asymmetrically gated G-SSDs and using these models to simulate the application of these devices in order to realize high frequency oscillators.
- Investigation of the effect of different passivation methods, such as nitrogen passivation, on the performance of the devices and their NDR operation.
- Investigation of the relationship between the width of the channel and the threshold voltage of the device, and how they affect the forward bias NDR effect.

Chapter Four:

- Calculation of quantum noise (shot and thermal noise) in order to estimate the signal to noise ratio when detecting the translocation of glycine and when detecting glycine's carboxyl group in the nitrogen passivated device.
- The use of different passivation methods, such as boron or fluorine, in order to obtain a p-type device that is sensitive to positive charges.
- Investigation of the sensitivity of the above proposed p-type device in detecting glycine's amine group.
- Investigation of the effect of pore size on the device's detection capabilities.
- Investigation of having an asymmetrically-gated tuneable graphene nanopore device, in a geometry similar to that of the device proposed in chapter three, but with a nanopore drilled in the channel of the device.
- Investigating the ability of the device to distinguish between different DNA bases.
- Investigation of the effect of the in-plane electric field applied by the side gates on the translocation speed of amino acid chains and DNA strands through molecular dynamics simulations.

- Fabrication of the proposed device using the same nanoscale methods proposed for the devices of chapters two and three, and testing the device in a laboratory setting.

Chapter Five:

- Fabrication of the proposed devices with nanoscale and microscale dimensions and characterizing their performance at high frequencies.
- Fabrication and characterization of the proposed devices on flexible, transparent and biocompatible substrates.
- Investigation of different methods of passivation and how they can be used in order to limit unwanted tunnelling current in the devices.
- Investigation of the effect of widening the insulating trenches in order to minimize tunnelling current, and how it affects rectification.
- Investigation of the effect of substitutional doping of other materials in order to obtain n-type devices.
- Investigation of three terminal planar MoS_2 devices.
- Investigation of SSD realization using related 2D nanomaterials such as WS_2.

Chapter Six:

- Fabrication and characterization of silicene SSDs and self-switching MISFEDs, however, this is dependent upon progress in silicene synthesis methods.
- Calculation of the *device density of states* (DDOS) in order to investigate the effect of the in-plane field effect on silicene's electronic bandgap.
- Investigation of the use of other types of passivation in order to achieve complementary, n- and p-type, silicene SSDs.
- Investigation of the performance of three terminal planar silicene MISFETs.
- Investigation of SSD realization using related 2D nanomaterials such as Germanene.

Chapter Seven:

- Fabrication of the proposed all-graphene DB-RTDs, at the nanoscale scale using high precision techniques and at the microscale using mass-production techniques, and their characterization at high frequencies.
- Derivation of an analytical model that can predict and explain the energy value of the transmission in the absence of any applied bias.

- Investigation of the effect of varying the width of the insulating trenches and varying the width of the GNRs on the performance of the devices.
- Investigation of the effect of GNR edge roughness, using *Monte Carlo* simulations, on the performance of the devices.
- Investigation of the effect of dimensions mismatch between different devices connected in parallel on their overall transport properties.
- Investigation of the effect of other types of passivation on the performance of the devices.
- Application of the fabricated devices for Terahertz detection and generation.

Chapter Eight:

- All of the points mentioned above for chapter seven applied to all-graphene planar double-quantum-dot RTDs.
- Derivation of an analytical model that can explain the trend observed for the tunability of the current peak position between discrete voltage levels, and predict the positions of the multiple peaks, for multiple devices connected in parallel, by relating them to the energy spectrum of the graphene quantum dots.
- Investigation of the effect of a mismatch in dimensions between the double quantum dots on the resonance effect in the devices.
- Investigation of the effect of a mismatch between the width of the quantum dots and the width of the GNR incorporating them.
- Application of the fabricated devices in multi-state logic and memory applications.

9.3 Future Directions: *There's Plenty More Room at the Top!*

In this section, a personal perspective on future directions is presented. A relatively general perspective on the future of electronics is discussed in order to highlight some very exciting advantages and opportunities that 2D planar electronic devices can facilitate, which would truly revolutionize the future electronics roadmap. This revolution would not only mean a new generation, or two, of integrated circuits, but rather a whole new line of future generations, by the will of God. However, before this perspective can be appreciated, a brief overview of a number of important trends that have shaped the recent history of electronics, and technology in general, is presented.

9.3.1 There's Plenty of Room at the Bottom

In the year 1959, Richard Feynman delivered a lecture titled: "There's plenty of room at the bottom", in which he tried to highlight the importance of looking at, manipulating and controlling things at the atomic level [248]. In his lecture he tried to highlight the opportunities that would be possible through being able to manipulate and control things at a small scale, down to the atomic level, through the comparison of artificial man-made systems with naturally occurring biological systems - the flawless creation of God. He tried to emphasize that going small in size, down to the bottom, would provide "plenty" of room to accommodate, discover and even do almost anything!

Irrespective of what he anticipated correctly or what ended up being otherwise, the ability of manipulating and controlling things on a small scale, which the overall lecture was inviting to, has truly become a very important tool that has contributed to shaping many important fields of research, including nanotechnology and electronics. While "miniaturization" – at that time – was at a state far away from Feynman's vision, in this day and age – after more than half a century since his lecture – , it seems to be heading towards what Feynman had in mind; miniaturization down to the atomic level. This level of miniaturization was what this thesis referred to as "ultimate miniaturization". In order to emphasize this concept, as can be observed throughout this thesis, dimensions of devices were described in atoms rather than micro, or even nanometres.

However, while miniaturization had truly contributed to shaping many fields of research, electronics stands out to be one of the most highly influenced of these. The way that miniaturization has affected, and even empowered, electronics has a sense of uniqueness, which can be understood through the discussion of a very important trend

that has been taking place within the electronics industry, and which is currently known by the term: *Moore's Law*.

9.3.2 Moore's Law

Although Richard Feynman made many speculations on what may be achieved in the future, these speculations were driven by observations of a direction or a trend that was in the making at the time. That direction was miniaturization, and it already had its influence on the electronics industry. As a result of that trend, the amount of components (mainly devices) that can be "crammed" onto an Integrated Circuit (IC) was increasing, mainly due to the fact that the components can be made smaller. Making a careful observation, Gordon Moore calculated that the number of components, which can be crammed onto an IC, was doubling every year [249]. Gordon Moore did not stop there, but went further to speculate, insightfully, that this trend will at least continue for the next decade [249]. Almost five decades since Moore's speculation, or what later became known as *Moore's Law*, this speculation still holds to a very close degree of accuracy. However, a debate remains to take place amongst electronics engineers, questioning whether, and for how long, can *Moore's Law* continue?

The importance of *Moore's Law* is not only due to the fact that it has been taking place, but rather due to its implications on the electronics industry. Increasing the number of components on an IC increases its complexity, and its processing and computational capabilities. It also has many advantages from the economical aspect, as well as the performance aspect. The real question that has been the concern of the electronics industry is not whether *Moore's Law* can continue, but rather how can we make it continue? (In order to continue increasing the complexity of ICs and harness the associated advantages).

9.3.3 Surface Area vs. Volume

Integrated circuits are made from wafers of different materials, the most common being silicon. Devices that dominate the electronics industry, nowadays, reside on, or within, the surface of the silicon wafer, occupying part of the available real estate on that silicon wafer. The surface of any silicon wafer is finite, and accordingly the number of devices it can accommodate is also finite. With a limited real estate on a silicon wafer, making a device smaller, enables fitting more of that device on a single wafer (or IC).

Accordingly, the driving force that has been enabling the continuation of *Moore's Law* is miniaturization of device dimensions, in order to reduce the area they occupy, and hence be able to fit, or cram, more of them onto the IC.

At the time Feynman gave his talk, device dimensions were very large in terms of number of atoms. Nowadays, they have been getting smaller and smaller, reaching up to tens of atoms for dimensions such as channel length and oxide thickness. However, no matter how small the devices can get, there will always be a limit set by the number of atoms. This was illustrated throughout this thesis, where most device dimensions were only a few atoms across, and in some devices, such as the double-quantum-dot RTD proposed in chapter 8, a single atom can be critical. This means that, sooner or later, regardless of how far fabrication and synthesis methods and technologies advance, there will always be a limit to how far a device can be miniaturized. Accordingly, given a finite area, there will always be a finite maximum number of devices that can fit within that area. Does this mean that *Moore's Law*, sooner or later, will face an end?!

While answering this question with a "yes" or "no" answer would seem to be tempting, this is not the concern of the discussion here. The main concern is trying to highlight a possible future direction, which may prove that *Moore's Law* does not have to be restricted to miniaturization of device dimensions in order to fit more of them within a finite "area", but rather within a finite "volume". What this statement actually means is left for the next subsection.

9.3.4 2D Nanoelectronic Devices for 3D Integrated Circuits

In large cities where the population of people increases rapidly, a common trend is to make houses smaller in order to fit more houses within the same area. However, while this can accommodate a larger number of houses, space will eventually run out, and what might have been "plenty" at one point in time, may not be "plenty enough" later on. This is the case with the IC, which might have had plenty of space for an increasing number of shrinking devices at one point in time, but is now heading towards its limit. This is mainly not because its area has been getting smaller, but because devices, sooner or later, will eventually stop getting any smaller.

Going back to large cities, we realize that an important lesson that building architects learnt over the years, is that if you don't have space for houses, then build tall towers! In other words, "stack" smaller houses on top of each other, and do not restrict yourself to

the ground floor. In an IC, the ground floor is the wafer's surface, and trying to stack devices on top of the wafer might seem to be an appealing and trivial solution. Indeed, this thought is not new to the electronics industry, as many research efforts have actually proposed this and even demonstrated it experimentally [250, 251]. However, due to the way devices are built, this proposal had severe complications, which made it impractical. These complications were mainly due to the fact that electronic devices reside on or within the wafer's surface, and hence trying to stack multiple device layers will actually mean trying to stack multiple wafers! This is very similar to trying to stack two football stadiums on top of each other, while in theory it may be possible, in reality it may be impractical.

The question that comes to mind now is: how were building architects able to build these tall towers, each of which has many apartments stacked on top of each other?! In order to figure this out, a comparison between houses and apartments is essential. The first observation is that houses are usually bulky with features in all three dimensions, while apartments are planar and flat, giving them their common name: "flats". Accordingly, stacking planar apartments becomes possible, contrary to the stacking of bulky 3D houses! Therefore, in order for us to stack devices, they need to be planar in architecture and not bulky and 3D. This is not the case with present electronic devices which are truly bulky and 3D, regardless of being manufactured using planar processing techniques or bulk micromachining techniques. The important requirement is that the final device architecture needs to be planar. And this is exactly why the requirement of a 'planar device architecture' was the first requirement set in the proposed device conceptualization strategy adopted throughout this thesis.

However, does "planar" mean "completely 2D"? The answer is: not necessarily. Looking at apartments, we realize that they do have finite heights, in order to be able to accommodate people. However, in electronics, devices do not need to accommodate people, but rather need to accommodate electrons. Interestingly, with the discovery of graphene, and 2D materials in general, it has been shown that electrons indeed are happy with a 2D monolayer and do not require bulk 3D materials. Nonetheless, why should we restrict ourselves to 2D nanomaterials and 2D device architectures?

While towers can accommodate a large number of apartments, they still do have a limit. This limit is set by the height of the tower, above which it may end up collapsing. Now once again, with this restriction of finite height (the 3rd dimension), in order to accommodate more floors (and hence more apartments), the floors need to have lower

heights. This happens to take us back, once again, to the concept of miniaturization and the importance of going down to the atomic level!

Building upon what we had established earlier, whenever we go down to the atomic level, no matter how small we can get, there will always be a limit for each dimension that is set by the number of atoms, with the absolute minimum being a single atom. Now in this situation, this limit on the 3rd dimension (the height) is not something we may be able to achieve in the future, but is rather something that we have recently been blessed with, by the Grace of God, through the discovery of the new family of 2D nanomaterials, which have this single atomic thinness! If we are able to realize a complete device within these 2D monolayers, then we have truly reached this absolute limit of miniaturization with regards to this 3rd dimension (the height), and this way we open up a path towards the realization of the tallest tower of stacked device layers, which may be able to accommodate the largest number of devices possible!

By exploiting this 3rd dimension to its limits, through stacking of 2D planar devices, there will be room for not only a future generation, or two, of ICs, but rather a new horizon of future generations of ICs. If at one point in time there may have been plenty of room at the bottom (here referring to the surface of the IC), then certainly "*There's plenty more room at the top!*"

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