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Damping Optimum-Based Design of Control Strategy Suitable for Battery/Ultracapacitor Electric Vehicles

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Abstract: This contribution outlines the design of electric vehicle direct-current (DC) bus control system supplied by a battery/ultracapacitor hybrid energy storage system, and its coordination with the fully electrified vehicle driveline control system. The control strategy features an upper-level DC bus voltage feedback controller and a direct load compensator for stiff tracking of variable (speed-dependent) voltage target. The inner control level, comprising dedicated battery and ultracapacitor current controllers, is commanded by an intermediate-level control scheme which dynamically distributes the upper-level current command between the ultracapacitor and the battery energy storage systems. The feedback control system is designed and analytical expressions for feedback controller parameters are obtained by using the damping optimum criterion. The proposed methodology is verified by means of simulations and experimentally for different realistic operating regimes, including electric vehicle DC bus load step change, hybrid energy storage system charging/discharging, and electric vehicle driveline subject to New European Driving Cycle (NEDC), Urban Driving Dynamometer Schedule (UDDS), New York Certification Cycle (NYCC) and California Unified Cycle (LA92), as well as for abrupt acceleration/deceleration regimes.

Keywords: advanced transportation technologies; electric vehicles; batteries; ultracapacitors; linear feedback control systems; power converters; certification driving cycles

1. Introduction

According to reference [1], road transport significantly contributes to the already alarmingly high levels of CO₂ in the atmosphere, which are the main cause of the greenhouse effect [2]. Since this sector is also highly sensitive to the availability of oil [3], it has gradually moved towards greater inclusion of electric vehicles (EVs) into the transportation sector due to their favorable fuel economy and low CO₂ footprint during exploitation [1,3]. Moreover, electrical vehicle technology has also been recognized as one of the key factors in the development of intelligent transportation system (ITS) [4], and its integration within the smart grid framework [5].

However, one of the main limitations of currently deployed EVs is that, generally speaking, their batteries can be optimized either for high-power operation or high energy capacity [6–8], wherein batteries characterized by high-power operating capabilities would be able to support abrupt loads such as those encountered during vehicle acceleration and regenerative braking regimes, whereas batteries characterized by high energy density can facilitate higher EVs autonomy and larger all-electric

driving range [9–11]. Additionally, when batteries are subject to frequent high-power abrupt loading regimes, their useful operating life tends to significantly decrease, as opposed to those operating under steady loads [12–14]. Under the aforementioned highly dynamic driving conditions, battery thermal stress may become a serious issue, which mandates battery temperature monitoring based on vehicle power-train energy consumption and appropriate battery thermal model [15]. Different battery pack cooling strategies may be employed to prolong the battery useful life and discharge capability (see e.g., [16] and references therein). Both references [15] and [16] emphasize the need for precise overall battery system modeling for thermal monitoring and management.

One way of dealing with the aforementioned battery limitations would be to oversize the EV high-power battery pack [7], but this would in turn increase the EV weight and production costs and would also result in lower efficiency of the electric power-train [14]. A practical alternative to battery over-sizing would be augmentation of the high-energy-density battery with an ultracapacitor-based energy storage system (ESS) [17]. Being characterized by exceptional power densities and cycling abilities (durability) compared to batteries, ultracapacitors represent a viable auxiliary energy storage solution for peak shaving of aforementioned EV pulsed loads [18,19]. Furthermore, a study presented in [20] has suggested that battery hybridization with ultracapacitors within EVs might result in approximately 75% battery cycle life extension through peak load shaving by means of ultracapacitors and associated reduction of battery thermal burden. Moreover, the benefits of employing battery/ultracapacitor hybrid energy storage (HESS) have been confirmed in [21], wherein the cost of temperature-related battery degradation strongly favors the use of ultracapacitors, which would facilitate profitable HESS operation over the anticipated 10-year period of exploitation. Of course, proper sizing of the individual battery and ultracapacitor energy storages within the HESS is needed with respect to the anticipated operating conditions of the EVs [22].

The aforementioned energy storage hybridization concept has shown clear benefits in the transportation sector [23] and has resulted in numerous successful EV applications [9,10,24–26]. A parallel battery/ultracapacitor HESS topology with independent load control of individual energy storages should be well suited for energy management control tasks [6,7,11,26,27]. In such an arrangement, both the battery and the ultracapacitor system are equipped with high-performance current-controlled power converters [28], providing bidirectional energy management within the EVs through the common direct-current (DC) bus (see Figure 1). This may be a challenging control problem because the supervisory control strategy should simultaneously keep the DC bus voltage within narrow bounds [9,25], while also distributing the DC bus load between the battery and ultracapacitor ESS to facilitate smooth EV power-train operation for a wide range of operating regimes [29,30]. In particular, the power converter coordination (load distribution) in EV applications should be aimed at ultracapacitor taking on the excessive (pulsed) power demand [31] and acting as a transient power load buffer. This may be facilitated through conditioning of the power demanded from the ultracapacitor power converter with respect to the battery by using a rule-based [32] or a proportional load distribution strategy [31]. Naturally, due to low energy density of ultracapacitor ESS, ultracapacitor system voltage should also be monitored and controlled to avoid overcharging or operation at low state of charge [28].

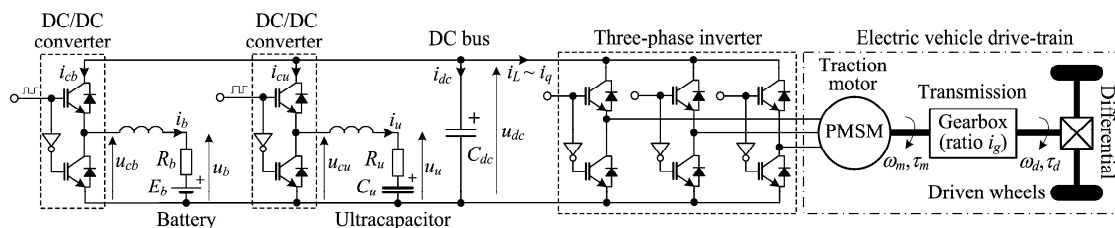


Figure 1. Considered EV power-train with parallel-connected battery and ultracapacitor ESS and vehicle traction AC electrical drive based on permanent-magnet synchronous motor (PMSM).

Simultaneous load sharing and DC bus voltage control typically requires an additional control level. In the case of off-line optimization studies of battery/ultracapacitor HESS, a dynamic programming-based off-line control law may achieve a global optimum in terms of minimum battery degradation over time [21]. This approach, however, cannot be used in real-time applications due to its non-causality (i.e., the requirement to know the driving cycle beforehand), and its intense computational burden. Other optimization-based approaches, such as those based on pseudo-spectral method [33] have also been investigated, wherein the battery cycle life and energy capacity retention optimization problem is solved by using nonlinear programming (NLP). For on-line applications, the aforementioned load allocation problem may be addressed within the framework of robust state control in the form of linear quadratic regulator (LQR) [9] with the EV power-train load treated as a system uncertainty. Successful application of a model predictive controller (MPC) for the energy management task has been demonstrated for the case of fully deterministic process model [34], and stochastic process model representation within MPC framework [12]. The predictive control approach has also been used to minimize the battery and ultracapacitor losses, while simultaneously maintaining the ultracapacitor state of charge within prescribed bounds [35]. Artificial intelligence control methods, such as those based on artificial neural networks (ANNs) [36] and fuzzy logic [37] have also been successful in achieving favorable battery performance indices in terms of battery life extension and capacity preservation within EVs based on HESS. However, these control approaches may be characterized by a rather high level of design complexity and intricate implementation requiring sophisticated control hardware [9,34], which may not be suitable for industry applications. Moreover, in the aforementioned cases of MPC and LQR controllers, the power converter response dynamics and limits are dealt with implicitly through cost function weighting, which might entail some closed-loop performance trade-offs related to weighting factors choices. Therefore, it would be favorable from the standpoint of practical control system design to provide a simple and robust power sharing strategy which would prioritize the power demand to avoid abrupt battery loading issues [38].

Having this in mind, the engineering practice suggests that the prospective control strategy should be characterized by:

- (1) Top-down cascade control system structure, to facilitate direct saturation of current demands via power converter references [39];
- (2) Bottom-up control system design wherein the current control systems for the battery and ultracapacitor ESS are designed and tested first, which is then followed by the comprehensive design of the superimposed feedback control levels [40];
- (3) A direct or indirect load compensator should augment the feedback controllers to deal with potentially abrupt loads at the EV DC bus side [41,42];
- (4) Variable DC bus voltage target, which is characteristic for hybrid-EVs [43,44] and those with fully electrified power-trains [45], and may also be beneficial to useful life extension of capacitors within the inverter DC bus [46];
- (5) Use of control system design methodology which could facilitate straightforward tuning of the closed-loop control system response dynamics;
- (6) Simplicity of code implementation that would enable use on robust microcontroller platforms suitable for automotive applications.

Having this in mind, the hypothesis of this work is that favorable performance of DC bus control system in terms of load suppression can be achieved by using a DC bus cascade control system structure and feed-forward load compensating action (see e.g., [39]), both for the case of constant and variable (EV-operating regime-dependent) DC bus voltage target. The proposed solution is based on the well-established proportional-integral (PI) feedback controller of DC bus voltage augmented with direct load compensator, which command suitable current demands to the hybrid battery/ultracapacitor HESS via a dynamic load distribution scheme. A damping optimum-based methodology [47] is used for feedback control system design, whereas direct zero-pole canceling approach is used for

load compensator tuning. The proposed design approach has been verified through simulations and experimentally for different realistic EV power-train operating scenarios. These included a DC bus load step disturbance, EV driveline subject to urban-type driving cycles, such as the New European Driving Cycle (NEDC), Urban Driving Dynamometer Schedule (UDDS), New York Certification Cycle (NYCC) and California Unified Cycle (also known as LA92 cycle) [48] and abrupt EV acceleration and deceleration commands.

The paper is organized in six sections. Section 2 presents the DC bus system and vehicle driveline load model, whereas Section 3 outlines the control system design. Simulation results are included in Section 4, while Section 5 presents the result of experimental verification on a down-scaled DC bus laboratory setup. Discussion of obtained results and final remarks are given in Section 6.

2. EV Power-Train Model

This section presents the models of EV power-train and the DC bus topology based on parallel-connected battery and ultracapacitor ESS.

2.1. Fully Electric Power-Train Topology

The power-train topology of the EVs analyzed herein is shown in Figure 1. The hypothetical vehicle is equipped with the battery and ultracapacitor ESSs parallel-connected via individual two-quadrant DC/DC power converters [32] to the common DC bus, which also supplies the power converter (inverter) of the alternating current (AC) servo motor which provides wheel traction through the fixed-ratio transmission (gearbox). Even though the electric drive-train should also include a hydraulic braking system, a power dissipation resistor for additional electro-dynamic braking capability, and different electrical auxiliaries, these are omitted from the “idealized” EV power-train representation in Figure 1 to simplify the subsequent analysis. Nevertheless, these systems could be taken into account through an additional load component in the DC bus load current i_L .

2.2. Traction Motor Control System

An AC permanent-magnet synchronous motor (PMSM) is considered for vehicle traction in this work, primarily due to its advantages over the AC induction motor in terms of higher power density, better overall efficiency, and generally smaller rotor inertia [49]. The natural PMSM machine description in the so-called stationary (stator-side) reference frame is described by a highly nonlinear dynamic model, which is not convenient from the standpoint of control system design. The PMSM control system is realized within the framework of field-oriented (or vector) control, which enables decoupled field flux and torque control at the rotor [39]. For that purpose, the PMSM machine stator-side variables (e.g., phase currents) are transformed into the so-called rotating d - q coordinate frame, where the d -axis relates to the rotor permanent-magnet field flux direction and the q -axis is perpendicular to it. In this way, the PMSM machine model resembles the model of the DC machine which is more convenient for analysis and control system design [39]. The resulting so-called field (d) and torque (q) currents i_d and i_q are obtained from the motor phase sinusoidal currents i_1 , i_2 and i_3 by using the well-known Park transform [50]:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (1)$$

where $\theta = \omega t$ is the rotor “electrical” angular position, and ω is the rotor “electrical” speed.

Figure 2 shows the block diagram representation of the PMSM current control system in the d - q reference frame. The PMSM servo-machine model comprises the simplified representation of the motor inverter, denoted by a first-order lag term with time constant T_{di} corresponding to the small lag of the inverter voltage response. The traction motor model comprises the first-order armature

(stator winding) lag model in both the field (d) and torque (q) axis, characterized by armature inductance L_a and resistance R_a , which determine the respective motor current components based on input voltages u_d and u_q and the motor electromotive force $u_{emf} = \Phi_r \omega = p \Phi_r \omega_m$ (ω_m is the rotor angular speed, Φ_r is the rotor field flux, and p is the number of motor pole pairs). The model also includes the so-called cross-axis coupling terms $\Delta u_d = \omega L_a i_q$ and $\Delta u_q = \omega L_a i_d$ which are the result of the aforementioned Park transform. Dual fast PI controllers are used to control the aforementioned currents i_d and i_q , and their design is presented in the next section. However, to obtain effective suppression of cross-axis coupling terms Δu_d and Δu_q , feed-forward d - q -axis cross-axis compensation terms are also included within the control system in Figure 2. These additive control terms are based on the available motor speed ω_m and current signals (see Figure 2). Finally, the current control system in Figure 2 may also include the compensation of counter electromotive force (EMF) ($p \Phi_r \omega_m$ term in Figure 2). The aforementioned PMSM machine parameters which can be used in subsequent simulation analysis can be obtained from the catalogue data for a suitably sized PMSM motor (see Section 4), whereas the current PI controller parameters are obtained as the result of control system design procedure described in Section 3.4 and are listed in Section 4.

The voltage command signals u_{dR} and u_{qR} , provided by respective current controllers are then transformed back to the stator-side coordinate frame quantities (i.e., phase voltage references u_{1R} , u_{2R} and u_{3R}) through the inverse Park transform:

$$\begin{bmatrix} u_{1R} \\ u_{2R} \\ u_{3R} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ \cos(\theta - 2\pi/3) & \sin(\theta - 2\pi/3) \\ \cos(\theta - 4\pi/3) & \sin(\theta - 4\pi/3) \end{bmatrix} \begin{bmatrix} u_{dR} \\ u_{qR} \end{bmatrix} \quad (2)$$

Operation below the rated speed is considered herein, so current i_d is kept at zero under closed-loop current control ($i_{dR} = 0$), and the PMSM overall field flux $\Psi = \Phi_r + L_a i_d$ corresponds to the rated rotor flux Φ_r . In that case the relationship between torque current reference i_{qR} and the motor torque target τ_R simplifies to (see i_{qR} reference path in Figure 2):

$$i_{qR} = \frac{\tau_R}{k_T} = \frac{2}{3p\Phi_r} \tau_R \quad (3)$$

with $k_T = 1.5p\Phi_r$ being the motor torque constant.

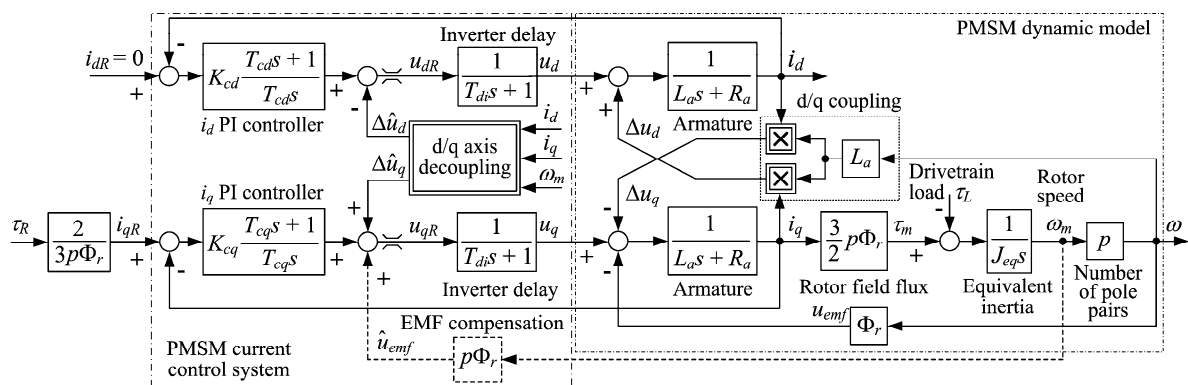


Figure 2. Block diagram of d - q coordinate frame current control system for inverter-fed PMSM traction motor operating below rated speed.

2.3. Dynamic Model of DC Bus

The DC bus system in Figure 1 is described by the following integral-type process model:

$$u_{dc} = -\frac{1}{C_{dc}} \int (i_{cb} + i_{cu} + i_L) dt \quad (4)$$

where C_{dc} represents the capacitance of the DC bus, u_{dc} is the voltage across the DC bus, i_L represents the EV power-train-related load current, and i_{cb} and i_{cu} are input currents of battery and ultracapacitor ESS, i.e., input currents of their respective DC/DC power converters.

If battery and ultracapacitor-side current measurements i_b and i_u (see Figure 1) are available, DC bus-side currents i_{cb} and i_{cu} could be estimated based on the following relationships between the average values of battery and ultracapacitor currents i_b and i_u and the corresponding DC/DC power converter instantaneous input currents i_{cb} and i_{cu} are valid (Figure 3, see also [51,52]):

$$\begin{aligned} \bar{i}_{cb} &= d_b \bar{i}_b \\ \bar{i}_{cu} &= d_u \bar{i}_u \end{aligned} \tag{5}$$

where d_b and d_u are battery and ultracapacitor DC/DC converter pulse-width-modulated (PWM) output voltage duty cycles, respectively, which are readily available from the current controller-based voltage reference commanded to power converter [40]. Since the voltage PWM switching frequency is relatively high, the above averaged currents may be used instead of their instantaneous values within the DC bus model (4). In this way, the subsequent design of the DC bus control system can be greatly simplified [41].

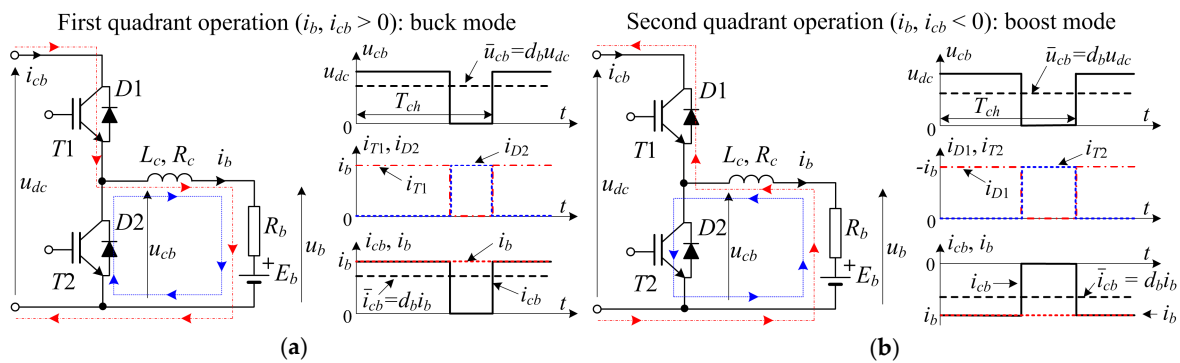


Figure 3. Illustration of voltage and current relationships at semiconductor switches T1 and T2 and fly-wheeling diodes D1 and D2, and input/output current and voltage relationships of two-quadrant DC/DC power converter for buck operation (a) and boost operation (b).

The following expression is valid for the averaged DC bus load i_L due to the operation of three-phase motor inverter [46]:

$$\bar{i}_L = \frac{3}{2} \frac{U_{ph}}{u_{dc}} I_{ph} \cos \varphi \tag{6}$$

where I_{ph} is the amplitude of the phase current fundamental component, U_{ph} is the amplitude of inverter phase voltage fundamental component, and $\cos \varphi$ is the traction motor power factor.

The principal components of the PMSM stator reference frame currents are given as follows:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = I_{ph} \begin{bmatrix} \sin(\theta + \varphi) \\ \sin(\theta - 2\pi/3 + \varphi) \\ \sin(\theta - 4\pi/3 + \varphi) \end{bmatrix} \tag{7}$$

These can be transformed to the d - q coordinate frame according to (1), yielding the following relationships between i_d and i_q and the inverter reactive and active current:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} I_{ph} \sin \varphi \\ I_{ph} \cos \varphi \end{bmatrix} \tag{8}$$

Finally, by using the d - q frame voltage references u_{dR} and u_{qR} obtained from respective current controllers (Figure 2), the amplitude U_{ph} of the inverter phase voltage can be directly calculated in the following manner [42]:

$$U_{ph} = \sqrt{u_{dR}^2 + u_{qR}^2} \quad (9)$$

Hence, the DC bus load i_L according to Equation (6) can be directly estimated based on Equations (8) and (9), and direct load compensation can be easily facilitated.

2.4. ESS Models

As illustrated by the principal schematic in Figure 1, the battery ESS can be described by the quasi-static Thevenin process model [7]:

$$u_b = i_b R_b + E_b(\xi) \quad (10)$$

$$\xi = \frac{1}{Q_b} \int i_b dt \quad (11)$$

where u_b is the battery terminal voltage, i_b is the battery current, R_b is the battery equivalent series resistance, Q_b is the battery charge capacity, and E_b and ξ are battery electromotive force and state of charge, respectively.

Similarly, ultracapacitor ESS in Figure 1 is modeled as a simple series connection of the equivalent series resistance R_u and ultracapacitor capacitance C_u [7]:

$$u_u = i_u R_u + \frac{1}{C_u} \int i_u dt \quad (12)$$

where u_u and i_u are the ultracapacitor terminal voltage and input current, respectively.

3. Control System Design

Based on the previously described models of individual EV power-train subsystems, a suitable energy management control strategy is designed in this section.

3.1. Damping Optimum Criterion

Damping optimum criterion [47] is a practical pole-placement-like method of design of linear continuous-time closed-loop systems and is used herein for the tuning of feedback control loops. The tuning procedure is based on the following closed-loop characteristic polynomial:

$$A_c(s) = D_2^{n-1} D_3^{n-2} \dots D_n T_e^n s^n + \dots + D_2 T_e^2 s^2 + T_e s + 1 \quad (13)$$

where T_e represents the so-called closed-loop equivalent time constant, and D_2, D_3, \dots, D_n represent the damping optimum characteristic ratios of the n th order closed-loop system.

In the so-called "optimal" case, characterized by $D_i = 0.5$ ($i = 2, \dots, n$), the closed-loop system has a quasi-aperiodic step response characterized by an overshoot of approximately 6% (resembling a second-order system with damping ratio $\zeta = 0.71$) and the approximate rise time $(1.8\text{--}2.1)T_e$. The aforementioned closed-loop damping ratio value 0.71 is considered an "optimal" choice in practical applications because it provides relatively fast step reference response with small (negligible) overshoot without any weakly damped oscillations in the control loop state variables during the response settling stage. The closed-loop damping adjustment corresponds to the adjustment of the individual characteristic ratios D_i , wherein the most dominant characteristic ratio D_2 determines the damping of the dominant closed-loop dynamics. In particular, by increasing the characteristic ratio D_2 above the optimal value 0.5 (while keeping the less-dominant characteristic ratios at optimal values $D_i = 0.5, i = 3, \dots, n$), the closed-loop response becomes faster and more oscillatory. On the

other hand, by decreasing D_2 below 0.5, the closed-loop system damping level is increased, and the closed-loop system is characterized by slower response without overshoot, i.e., the so-called aperiodic dynamics are obtained (see e.g., discussions in [47,53]). Finally, by choosing a larger value of equivalent closed-loop time constant T_e , the control system generally tends to be more robust and its sensitivity to noise is greatly improved (i.e., bandwidth Ω_{BW} is proportional to $1/T_e$). However, this results in control system response slowdown and poorer disturbance rejection performance.

3.2. Low-Level Control of ESSs

Block diagram models of current control loops for the battery and ultracapacitor ESS are shown in Figure 4a,b, respectively. The battery and ultracapacitor energy storages are characterized by their respective equivalent electrical-circuit models given by Equations (10) and (11) in the case of battery, and Equation (12) in the case of ultracapacitor. Individual ESS current control is based on the PI controller in its modified form characterized by the proportional gain being in the local feedback path, while the integral term acts upon the current control error. In this way, controller zeros do not occur in the closed-loop transfer function model between the reference and the controlled variable (see discussion in [53]).

Since charge accumulation processes are typically slow, the battery electromotive force and ultracapacitor charge-related voltage variations are rather non-emphasized compared to voltage variations due to voltage drop across the series resistance, especially during transients. Thus, the dominant current transient dynamics may be expressed by a simple equivalent first-order transfer function model [40]:

$$G_c(s) = \frac{i_{b(u)}(s)}{u_{cb(cu)}(s)} = \frac{R_{tot}^{-1}}{(R_{tot}^{-1}L_c)s + 1}, \tag{14}$$

where L_c is the inductance of the embedded inductor within the DC/DC power converter and R_{tot} is the total series resistance of the respective ESS in Figure 4 ($R_{tot} = R_c + R_b$ in the case of battery and $R_{tot} = R_c + R_u$ for the case of ultracapacitor).

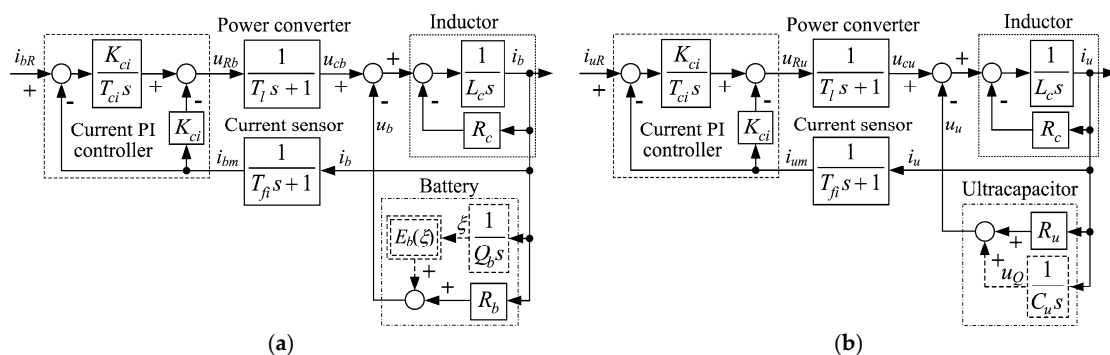


Figure 4. Current control loops for battery ESS (a) and ultracapacitor ESS (b), featuring feedback PI controller, simplified power converter model with embedded inductor and simplified ESS models.

Based on block diagram representations of battery and ultracapacitor ESS current control loops, the damping optimum-based control system design is carried out. To simplify the design procedure, the small delay due to power converter and current sensor (filter) lags are lumped into a single equivalent lag action:

$$G_{par}(s) = \frac{1}{T_{\Sigma i} s + 1} \tag{15}$$

wherein the equivalent parasitic lag constant $T_{\Sigma i} = T_l + T_{fi}$ may also include the sampling delay if a discrete-time (digital) controller is considered.

Based on Equation (15) and current vs. voltage model (14) under the assumption of slow charge accumulation-related phenomena, the current measurement vs. reference value transfer function model $i_m(s)/i_R(s)$ of both closed-loop current control systems in Figure 4 is given by:

$$G_{ci}(s) = \frac{1}{\frac{T_{\Sigma i} L_c T_{ci} s^3}{K_{ci}} + \frac{(R_{tot} T_{\Sigma i} + L_c) T_{ci} s^2}{K_{ci}} + \frac{(R_{tot} + K_{ci}) T_{ci} s}{K_{ci}} + 1} \quad (16)$$

The damping optimum tuning procedure for the current control system is carried out by equating the coefficients of the denominator of the transfer function model (16) with the coefficients of the damping optimum characteristic polynomial defined by Equation (13) for the case of third-order nominal model ($n = 3$). After some manipulation and rearranging, the following analytical relationships are obtained, which relate the PI controller parameters with the process parameters and damping optimum tuning parameters (i.e., characteristic ratios) [40–42]:

$$T_e \geq T_{e,min} = \frac{1}{D_{2i} D_{3i}} \frac{T_{\Sigma i}}{1 + T_{\Sigma i} R_{tot} / L_c} \quad (17)$$

$$T_{ci} = T_e \left(1 - \frac{D_{2i} T_e}{T_{\Sigma i} + L_c / R_{tot}} \right) \quad (18)$$

$$K_{ci} = R_{tot} \left(\frac{T_{\Sigma i} + L_c / R_{tot}}{D_{2i} T_e} - 1 \right) \quad (19)$$

Clearly, this tuning approach enables independent tuning of the response speed (equivalent time constant T_{ei}) and closed-loop damping (dominant characteristic ratio D_{2i}).

Unlike the battery, the ultracapacitor is characterized by rather low energy density (charge capacity). Hence, it may relatively quickly become discharged if frequent discharging demands are commanded to ultracapacitor ESS. Therefore, a supplementary controller of ultracapacitor state of charge is also needed [40,41]. For the sake of simplicity, it can be realized as ultracapacitor terminal voltage PI controller, as shown in Figure 5.

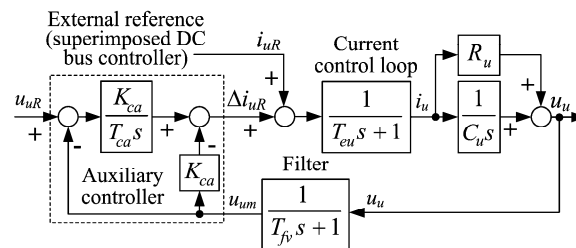


Figure 5. Block diagram of ultracapacitor terminal voltage control system featuring a feedback PI controller commanding an additional current reference to inner ultracapacitor current control loop.

Again, to simplify the design procedure, the rather small time constants of the inner current control loop (T_{eu}) and voltage measurement (T_{fv}) are lumped into a single equivalent time constant $T_{\Sigma u} = T_{eu} + T_{fv}$, which results in the following form of the closed-loop system characteristic polynomial:

$$A_c(s) = C_u T_{\Sigma u} T_I K_R^{-1} s^3 + (K_R^{-1} + R_u C_u T_I) s^2 + (R_u C_u + T_I) s + 1 \quad (20)$$

The previously described damping optimum design yields the following analytical expressions for the controller parameters (i.e., time constant T_{ca} and gain K_{ca}):

$$T_{ca} = T_{ea} - R_u C_u \quad (21)$$

$$K_{ca} = \frac{C_u (T_{ea} - R_u C_u)}{D_{2a} T_{ea}^2 - R_u C_u (T_{ea} - R_u C_u)} \quad (22)$$

with the equivalent time constant T_{ea} in above expressions obtained through solving of the following cubic equation:

$$T_{ea}^3 - \frac{T_{\Sigma u} T_{ea}^2}{D_{2a} D_{3a}} + \frac{R_u C_u T_{\Sigma u} T_{ea}}{D_{2a}^2 D_{3a}} - \frac{R_u^2 C_u^2 T_{\Sigma u}}{D_{2a}^2 D_{3a}} = 0 \quad (23)$$

whose solution also needs to satisfy the following feasibility condition to obtain non-negative values of controller parameters:

$$T_{ea} > R_u C_u \quad (24)$$

Please note that the auxiliary state of charge control loop response dynamics need to be much slower than the command from the superimposed control level (see next subsection), so that any interference with the control action i_{uR} from the upper-level DC bus control strategy (also shown in Figure 5) may be effectively avoided.

3.3. Design of DC Bus Voltage Control System

Figure 6 shows the DC bus control system arrangement, comprising the upper-level DC voltage feedback controller and feed-forward load compensator which command the inner current control loops of the battery and ultracapacitor ESS through the dynamic load distribution scheme.

The DC bus voltage reference u_{dcR} is calculated based on PMSM inverter phase voltage amplitude estimate according to Equation (9), subject to the following constraint related to the upper bound of the phase voltage modulation index $M_{max} = 1.155$ to avoid traction motor phase voltage over-modulation issues [46]:

$$2U_{ph}/u_{dc} < M_{max} \quad (25)$$

This is done in Figure 6 by simply augmenting the theoretical DC voltage result $u_{dc} = 2U_{ph}/M_{max}$ according to (25) through a voltage scaling factor $\kappa_u > 1$. Note also that the DC bus voltage reference u_{dcR} needs to be limited to prevent: (1) DC bus under-voltages and (2) rather inefficient boost operation of the DC/DC power converter at high DC bus voltages (see [54]).

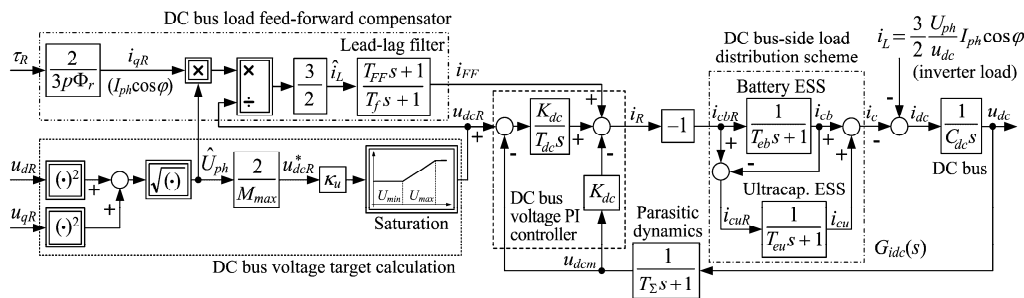


Figure 6. DC bus control system block diagram representation featuring DC bus voltage target calculation from motor phase voltage demand, DC bus load feed-forward compensator and DC bus voltage feedback PI controller commanding the dynamic load distribution scheme.

According to Figure 6, the current reference from the upper-level DC bus PI feedback controller and load compensator should be dynamically distributed between the battery and ultracapacitor ESS to facilitate effective load disturbance suppression of the closed-loop system. Since batteries are typically intended for steady and slowly changing loads [55], the battery ESS current controller should be tuned for slow response (i.e., tuned with large equivalent time constant T_{cb}). On the other hand, ultracapacitor ESS, being able to provide peak shaving capability, should be equipped with fast-current controller (i.e., characterized by small equivalent lag T_{eu}). Indeed, within the load distribution strategy in Figure 6 the “slow” battery ESS receives the upper-level command directly, and any abrupt power demand that the battery ESS cannot immediately provide due to its bandwidth limitations is forwarded to the ultracapacitor ESS whose current reference is calculated as $i_{cuR} = i_{cbR} - i_{cb}$. Note that these current commands (i_{cbR} and i_{cuR}) need to be referred to the battery-side and ultracapacitor-side currents

through scaling with respect to individual DC/DC power converter duty cycles as explained in Section 2.3 and elaborated in detail in [41].

The dynamic model of the current reference distribution scheme in Figure 6 is given by the following transfer function:

$$G_{idc}(s) = \frac{i_c(s)}{i_R(s)} = \frac{1}{T_{eb}s + 1} + \left(1 - \frac{1}{T_{eb}s + 1}\right) \frac{1}{T_{eu}s + 1} \quad (26)$$

If the ultracapacitor ESS is characterized by much faster response ($T_{eu} \ll T_{eb}$), the above relationship can be simplified as follows [41]:

$$G_{idc}(s) \approx \frac{1}{T_{eu}s + 1} \quad (27)$$

i.e., the transient dynamics of current supplied to the DC bus are only due to the fast ultracapacitor ESS action characterized by a small lag T_{eu} . For voltage feedback control system design, this relatively small lag may be augmented with the small lag T_{Σ} corresponding to voltage measurement and sampling effect in the case of digital controller.

Based on the above analysis, the DC bus feedback control system transfer function model reads as follows:

$$G_{udc}(s) = \frac{u_{dcm}(s)}{u_{dcr}(s)} = \frac{1}{\frac{C_{dc}(T_{\Sigma} + T_{eu})T_{dc}}{K_{dc}}s^3 + \frac{C_{dc}T_{dc}}{K_{dc}}s^2 + T_{dc}s + 1} \quad (28)$$

which yields the following expressions for PI controller parameters:

$$T_{dc} = T_{edc} = \frac{T_{\Sigma} + T_{eu}}{D_{2dc}D_{3dc}} \quad (29)$$

$$K_{dc} = \frac{C_{dc}}{D_{2dc}T_{edc}} \quad (30)$$

The feed-forward compensator design is aimed at canceling out the dominant lag in the path of the current reference, which yields the result for the compensator lead time constant [42]:

$$T_{FF} = T_{eu} \quad (31)$$

while the filtering time constant T_f is tuned to achieve a good trade-off between direct compensator response speed and noise attenuation:

$$T_f = \alpha T_{FF} \quad (32)$$

with the scaling factor $\alpha = 0.2$ chosen herein.

3.4. Traction Motor Current/Torque Control

It is assumed that traction motor electromotive force $u_{emf} = p\Phi_r\omega_m$ is compensated for and that the compensation of voltage cross-coupling terms $\Delta u_d = L_a i_q p\omega_m$ and $\Delta u_q = L_a i_d p\omega_m$ is also included (see Figure 2). In that case the feedback controller design should be the same for both axes of the rotating d - q coordinate frame, because of their symmetrical structures. Typically, in the case of current control loop design the armature time constant $T_a = L_a/R_a$ is canceled out by the current PI controller zero (see [39]):

$$T_{cd} = T_{cq} = T_a \quad (33)$$

In that case the closed-loop transfer functions of d - q current control systems read as follows:

$$G_{ci}(s) = \frac{i_{d(q)}(s)}{i_{dR(qR)}(s)} = \frac{1}{1 + \frac{R_a T_{cd(cq)}}{K_{cd(cq)}}s + \frac{T_{di} T_{cd(cq)}}{K_{cd(cq)}}s^2} \quad (34)$$

The damping optimum-based design (with $n = 2$ in Equation (13)), results in the following expressions for the current controller proportional gains K_{cd} and K_{cq} and the current control loop equivalent time constant T_{ei} :

$$T_{ei} = \frac{T_{di}}{D_{2i}} \quad (35)$$

$$K_{cd} = K_{cq} = D_{2i} \frac{T_a}{T_{di}} R_a \quad (36)$$

4. Results of Simulation Analysis

The presented control system design has been verified first by means of comprehensive simulation analysis for different scenarios. These included a DC bus load step disturbance and related ESS charging and discharging operation, EV driveline subject to urban-type driving cycles such as NEDC, UDDS, NYCC and California Unified Cycle (also known as LA92 cycle), and abrupt EV acceleration and deceleration commands. The overall EVs simulation model and all sub-models and control systems are implemented within MATLAB/Simulink software environment by using standard blocks and libraries.

4.1. Simulation Model Parameterization

The simulation model comprising the hybrid battery/ultracapacitor energy storage equipped with the previously designed DC bus control system and the traction motor drive within the hypothetical EVs is parameterized based on realistic power-train component data obtained from [43,56–59].

In addition, for the case of simulation verification based on standard certification driving cycles and abrupt acceleration and deceleration scenarios, it is assumed that vehicle deceleration is predominantly due to traction machine inverter regenerative braking operation. For these scenarios, the traction motor torque reference can be obtained by using a vehicle inertia model extended with rolling resistance and air drag terms, and whose speed is controlled by means of a virtual driver model [60] implemented in the form of a PI controller, as illustrated in Figure 7. The virtual driver PI controller parameters are also determined according to damping optimum, with the assumption that power-train load due to air drag is treated as a slow external disturbance within the vehicle model:

$$T_{dr} = \frac{T_d + T_{ei}}{D_{2dr} D_{3dr}} \quad (37)$$

$$K_{dr} = \frac{J_{eq}}{D_{2dr} T_{dr} r_w} = \frac{i_g^2 [J_m + 2J_w / i_g^2 + m_v (r_w / i_g)^2]}{D_{2dr} T_{dr} r_w} \quad (38)$$

where J_{eq} is the equivalent inertia referred to the PMSM traction machine output shaft, i_g is the transmission gearbox ratio, r_w is the wheel radius, and characteristic ratios $D_{2dr} = D_{3dr} = 0.5$ are chosen to obtain fast and well-damped closed-loop response.

The resulting parameters of the process models and respective controllers are listed in Table 1, whereas Table 2 lists the parameters of the hypothetical EVs and the virtual driver, the parameters of a suitable traction motor (PMSM) characterized by the rated power of 72 kW (see [58]), and the parameters of the corresponding traction motor current/torque control system. Moreover, the battery and ultracapacitor ESS can be sized based on analyzing the catalogue data from [56,57]. The resulting analysis has shown that the prospective battery with rated capacity of 32 kWh would be characterized by the mass of 320 kg, and the length of 1.4 m, and would measure 0.73 m in width and 0.22 m in height, thus yielding the total volume of 0.22 m³. Similar analysis has yielded the dimensions of ultracapacitor ESS to be 1.29 m in length, 0.62 m in width and 0.22 m in height, thus yielding the overall ultracapacitor ESS volume of 0.22 m³, and weight of about 180 kg.

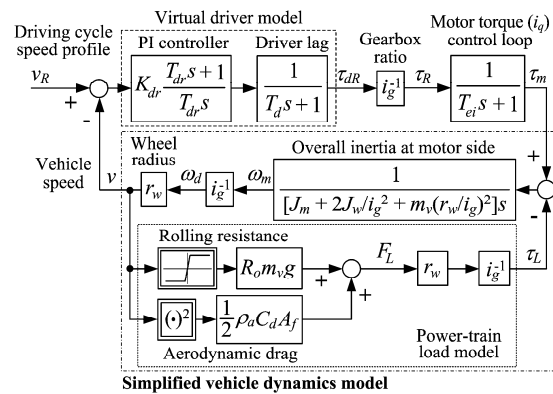


Figure 7. Vehicle dynamics model comprising equivalent vehicle inertia, rolling resistance and air drag effect referred to the motor side, controlled by a PI controller-based virtual driver.

Table 1. Parameters of DC bus control system simulation model.

Parameter	Value	Parameter	Value
Inductor inductance L_c	13 mH	DC bus capacitance C_{dc}	40 mF
Series resistance of inductor R_c	0.1 Ω	Ultracapacitor ESS equivalent lag T_{eu}	15 ms
Rated voltage of battery U_b	320 V	Battery ESS equivalent lag T_{eb}	200 ms
Rated charge capacity of battery Q_b	100 Ah	Voltage reference scaling factor $\kappa\kappa_u$	1.1
Battery internal resistance R_b	0.08 Ω	Feed-forward lead time constant T_{ff}	15 ms
Ultracapacitor voltage limit $U_{u,max}$	375 V	DC bus voltage lower limit U_{min}	328 V
Ultracapacitor rated capacitance C_u	21 F	DC bus voltage upper limit U_{max}	690 V
Ultracapacitor resistance R_u	45 m Ω	DC bus parasitic lag T_Σ	5 ms
Ultracapacitor ESS current controller (fast) proportional gain K_{ci}	1.78 V/A	Ultracapacitor ESS current controller (fast) integral time constant T_{ci}	13 ms
Ultracapacitor ESS current controller (slow) proportional gain K_{ci}	1.78 V/A	Ultracapacitor ESS current controller (fast) integral time constant T_{ci}	26 ms
Battery ESS current controller (fast) proportional gain K_{ci}	1.63 V/A	Battery ESS current controller (slow) proportional gain K_{ci}	14 ms
Battery ESS current controller (slow) integral time constant T_{ci}	1.63 V/A	Battery ESS current controller (slow) integral time constant T_{ci}	140 ms
Ultracapacitor auxiliary controller proportional gain K_{ca}	8.62 A/V	Ultracapacitor auxiliary controller integral time constant T_{ca}	191 ms
DC bus voltage controller proportional gain K_{dc}	1 A/V	DC bus voltage controller integral time constant T_{dc}	80 ms

Table 2. EV power-train simulation model parameters.

Parameter	Value	Parameter	Value
Overall vehicle mass m_v	1500 kg	Transmission (gearbox) ratio i_g	2
Battery ESS mass	320 kg	PMSM torque constant $k_T = 1.5 p\Phi_r$	1.52 Nm/A
Battery ESS volume	0.22 m ³	PMSM EMF constant $k_E = p\Phi_r$	1.01 Vs/rad
Ultracapacitor ESS mass	180 kg	PMSM armature inductance L_a	0.95 mH
Ultracapacitor ESS volume	0.22 m ³	PMSM armature resistance R_a	26 m Ω
Free fall acceleration g	9.81 m/s ²	PMSM inverter voltage lag T_{di}	1 ms
Coefficient of rolling resistance R_o	0.008	PMSM moment of inertia J_m	0.066 kgm ²
Air density ρ_a	1.224 kg/m ³	PMSM number of pole pairs p	3
Coefficient of air drag C_d	0.29	PMSM current controller proportional gain $K_{cd(cq)}$	1.083 V/A
Vehicle frontal area A_f	2.3 m ²	PMSM current controller integral time constant $T_{cd(cq)}$	36.5 ms
Wheel radius r_w	0.305 m	PMSM torque loop lag T_{ei}	2 ms
Wheel moment of inertia J_w	0.8 kgm ²	Virtual driver gain K_{dr}	1877 N·s
Driver lag T_d	100 ms	Virtual driver time constant T_{dr}	400 ms

4.2. Verification of HESS and DC Bus Control System

The comparative simulation responses of the low-level current control loops within ultracapacitor and battery ESS are shown in Figure 8 for the stepwise discharging command with current reference step magnitude of -10 A. The ultracapacitor current control system is tuned for a fast and well-damped step response according to the damping optimum procedure, resulting in the closed-loop equivalent time constant $T_{eu} = 15$ ms (Table 1), which yields the response settling time of about 30 ms with less than 6% step response overshoot (Figure 8a). The response speed (bandwidth) of the ultracapacitor current control loop can be arbitrarily slowed down by means of increasing the closed-loop equivalent time constant T_{eu} according to Equation (17). Figure 8a further shows that decreasing the most dominant characteristic ratio D_{2i} below the optimal value (0.5) results in T_{eu} increase, as well as in increased damping of the closed-loop system. In the case of battery ESS (Figure 8b), two distinctive PI controller tuning cases have been considered with respect to the closed-loop equivalent time constant T_{eb} choices (Figure 8b). Namely, the battery ESS control system can be tuned for rather fast response characterized by favorable response damping ($T_{eb} = 20$ ms in Figure 8b). However, a more conservative tuning aimed at slower closed response should be preferred because the battery ESS is intended for slowly varying loads. The comparative simulation responses obtained for the “slower” PI controller tuning (with $T_{eb} = 200$ ms) in Figure 8b, indeed show a ten-fold longer closed-loop transient settling time with respect to “fast” controller tuning.

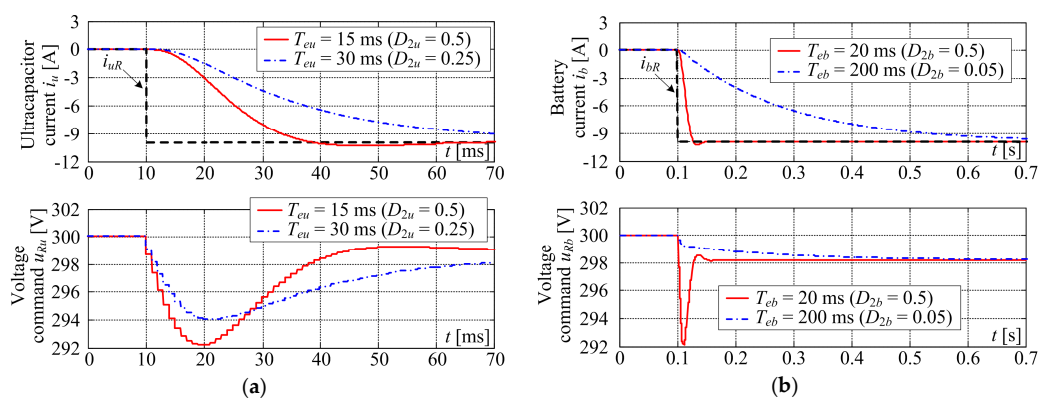


Figure 8. Results of simulation analysis of ultracapacitor ESS (a) and battery ESS (b) current control systems, illustrating the damping optimum tuning procedure and its ability to arbitrarily adjust closed-loop response speed.

Figure 9 shows the comparative simulation responses of the DC bus control system subject to load current step with the magnitude of 50 A, effectively emulating a sudden 18 kW driveline acceleration command (25% of the traction motor rated power). When PI feedback controller alone is used (Figure 9a), the DC bus voltage is characterized by well-damped dynamic behavior. However, the stepwise disturbance response is characterized by a relatively large voltage drop of 8.9% with respect to the selected DC bus voltage target $u_{dcR} = 360$ V, with the voltage response settling to the target value within 140 ms due to non-negligible lag the feedback loop characterized by the equivalent time constant $T_{edc} = 80$ ms (top trace in Figure 9a). The HESS responses (bottom plot in Figure 9a) confirm that the ultracapacitor ESS reacts notably faster compared to the battery ESS within the proposed dynamic load distribution scheme. When the PI controller is augmented by the direct feed-forward compensator (Figure 9b), the DC bus voltage drop after the stepwise load is reduced to 1.7% of the DC bus voltage target due to the fast reaction of the feed-forward compensator, which directly forwards a rather fast-current command to the intermediate-level load distribution scheme. As a result, the load suppression potential of the control system featuring the ultracapacitor ESS equipped with fast-current controller is better used, as opposed to the when only the PI feedback controller is used (see Figure 9a,b).

Figure 10 illustrates the DC bus system behavior for the case when the ultracapacitor ESS is being charged from the common DC bus under the auxiliary ultracapacitor voltage controller, which commands appropriate current command to the ultracapacitor ESS current control system. Since the auxiliary controller output is limited to avoid excessive DC bus loads for the purpose of ultracapacitor ESS voltage control, the ultracapacitor ESS represents a near-constant DC load throughout most of the charging transient, which results in a linear rise of the ultracapacitor terminal voltage towards the target value $u_{ur} = 300$ V (top plot Figure 10a). The DC bus voltage response is characterized by an initial voltage drop (bottom plot in Figure 10a) corresponding to the ultracapacitor ESS load being demanded by the auxiliary controller (top plot in Figure 10b). As indicated by the battery ESS response (bottom plot in Figure 10b), the required ultracapacitor charging current is provided by the battery ESS, which points out to effective load distribution performed by the intermediate-level control scheme in Figure 6.

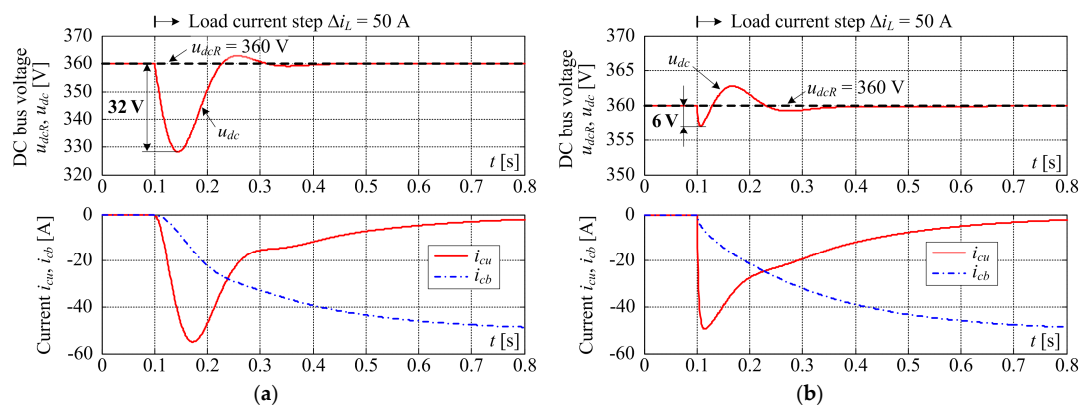


Figure 9. DC bus control voltage and battery/ultracapacitor ESS current simulation results for abrupt load current change when PI controller is used alone (a), and with direct feed-forward load compensator (b).

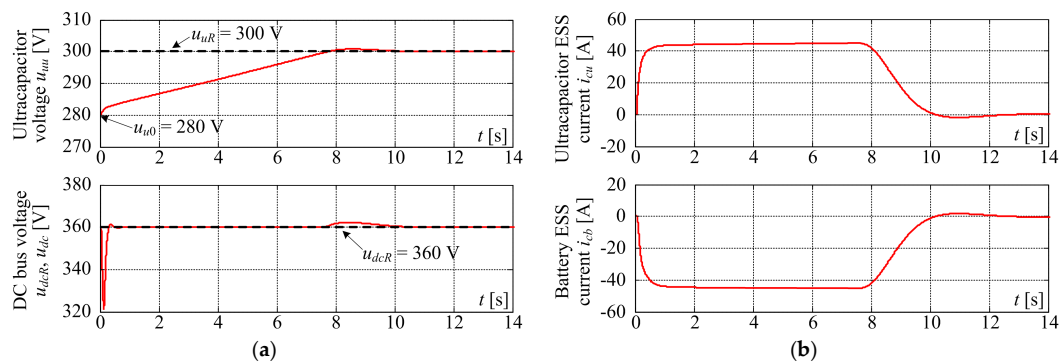


Figure 10. Simulation responses of ultracapacitor auxiliary voltage control system: ultracapacitor and DC bus voltage traces (a) and battery/ultracapacitor ESS current responses (b).

4.3. Driving Cycle-Based Analysis

Figure 11 shows the simulation results of the vehicle model equipped with the virtual driver for the chosen certification driving cycles, i.e., NEDC, UDDS, LA92 and NYCC (see e.g., [15,48]). The driving cycle data are obtained from the US Environmental Protection Agency (EPA) website [48] and have been downloaded as vehicle speed over time traces in ASCII format, and used within the MATLAB/Simulink simulation environment. Since NEDC cycle comprises an interval of urban-like driving (frequent vehicle starting and stopping), followed by a highway-like driving and final rapid deceleration, vehicle driveline is characterized by notable driveline torque τ_d and vehicle speed v variations. The aforementioned torque variations are even more emphasized for the UDDS cycle (see Figure 11a). Similar result is obtained for the cases of LA92 and NYCC driving cycles, wherein the former combines high-speed and low-speed driving with rather abrupt and frequent vehicle

acceleration and deceleration, while the latter is characterized by frequent starting and stopping, albeit at lower vehicle speeds characteristic to congested traffic conditions (Figure 11b). The traction motor phase voltage U_{ph} and active current component $I_{ph} \cdot \cos(\phi)$ traces shown in Figure 11 closely reflect the above vehicle speed and driveline torque profiles.

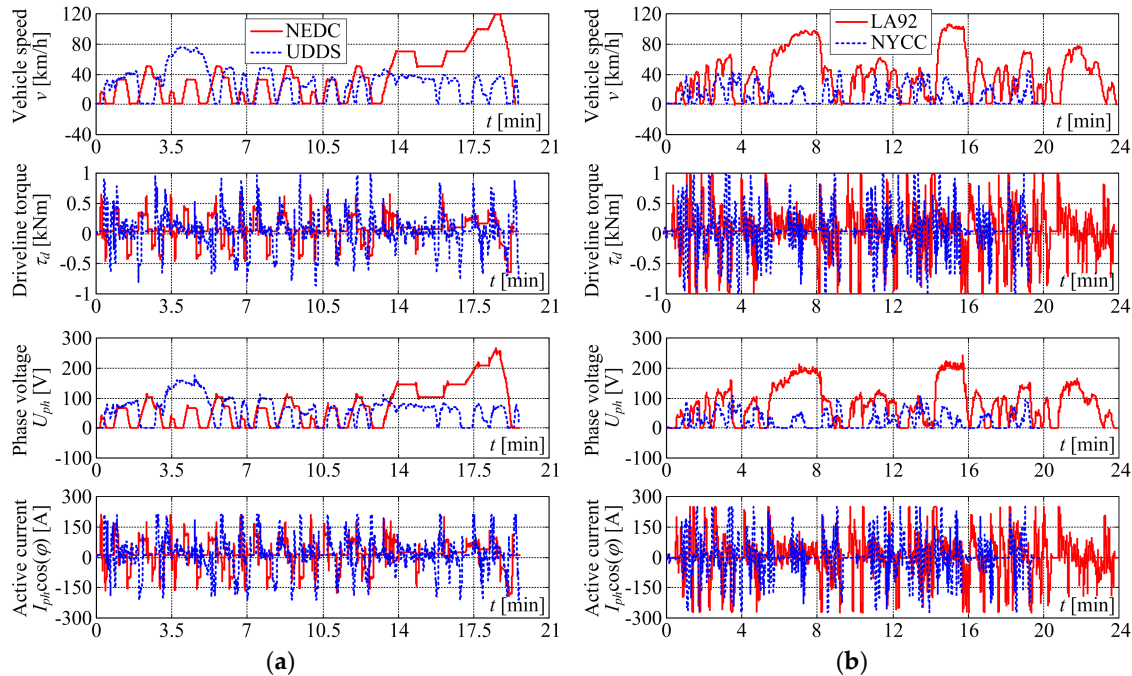


Figure 11. Simulation responses of vehicle speed, driveline torque, traction motor phase voltage and active current component traces for NEDC and UDSS driving cycles (a) and LA92 and NYCC driving cycles (b).

Figure 12 shows the corresponding load current i_L and DC voltage profiles u_{dc} for the individual cases of vehicle driveline and traction motor inverter responses in Figure 11. The comparative DC bus voltage responses in Figure 12 indicate that NEDC driving cycle is characterized by a notable DC bus voltage target increase above the lower threshold $U_{min} = 328$ V in the final, highway-like driving interval (top plot in Figure 12a). Namely, this increased DC bus voltage is needed to cover for increased traction motor voltage demand corresponding to high motor (and vehicle) speeds characterized by high motor back-EMF values. Similar requirement with respect to DC bus voltage reference is also observed in the case of LA92 cycle when the vehicle speed increases above the 80 km/h (check traces in Figures 11b and 12c). The UDSS and NYCC driving cycles, being characterized by vehicle speeds below 80 km/h, do not mandate DC bus voltage increase above the lower threshold U_{min} , as indicated by traces in Figure 12b,d. Moreover, all driving cycles are characterized by notably smaller DC bus voltage tracking errors when direct feed-forward compensator is used, as opposed to the case when PI feedback controller has not been augmented by the feed-forward load compensating action. This is also illustrated by DC bus load current tracking error $\Delta i_c = -(i_L + i_c)$ traces in bottom plots in Figure 12a,d, wherein a notable reduction of load current tracking error magnitudes is observed when direct feed-forward compensator is used.

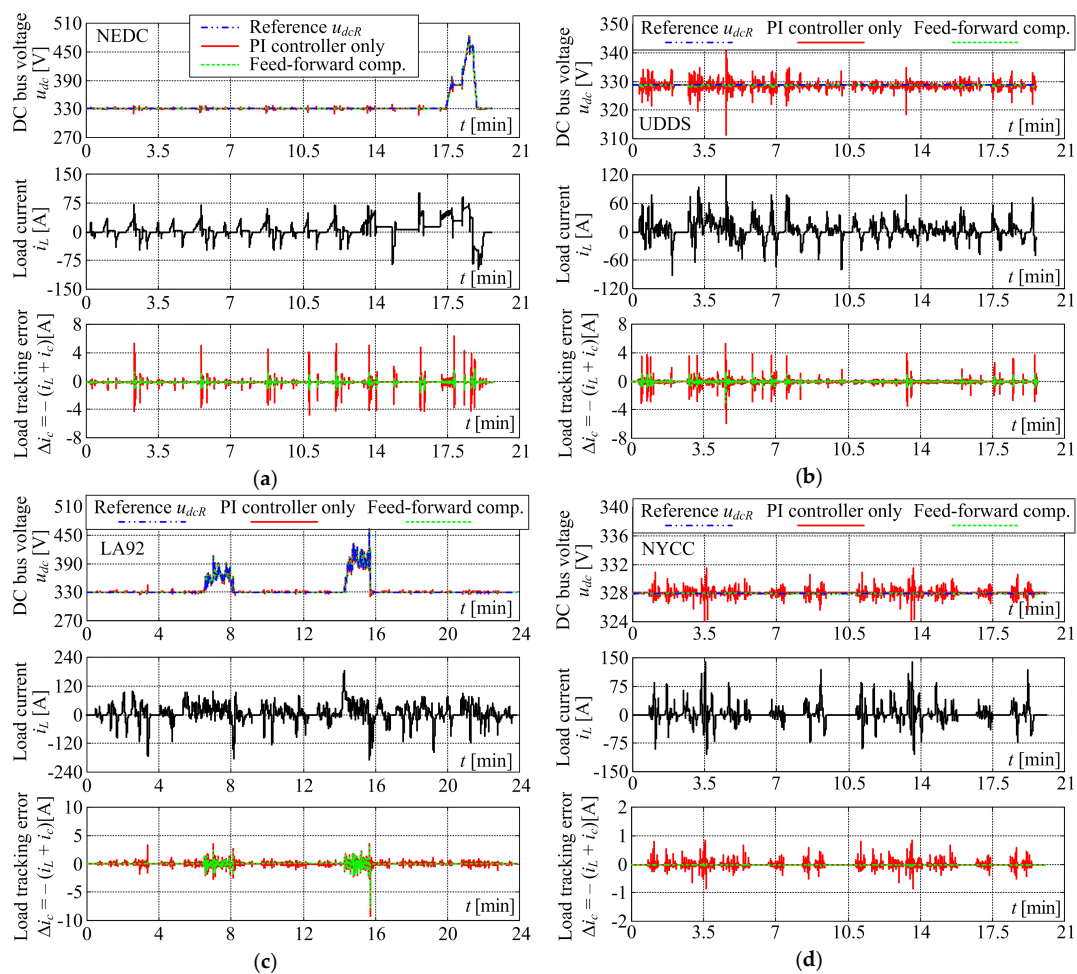


Figure 12. DC bus voltage, load current responses and load current tracking error traces obtained by means of vehicle simulation model for different certification driving cycles: NEDC (a), UDDS (b), LA92 (c) and NYCC (d).

The above conclusions are further strengthened by the comparative DC bus voltage tracking error and load tracking error indices, shown in Figure 13. In particular, when PI controller is used alone, the more dynamic UDDS and LA92 driving cycles are characterized by somewhat larger DC bus voltage tracking errors compared to the case of NEDC, and especially with respect to relatively low-speed NYCC driving cycle (see Figure 13a,b). As expected, introduction of feed-forward load compensator results in notable decrease of DC voltage target tracking error, especially in the case of the highly dynamic UDDS driving cycle. The LA92 driving cycle, on the other hand, is characterized by the least emphasized reduction of maximum voltage tracking error, which is due to two rather dynamic (high-bandwidth) DC bus voltage and load profiles (t between 6.5 s and 8.2 s and t between 14.5 s and 15.7 s in Figure 12c), which relates to higher magnitudes of the maximum DC bus and load current tracking indices in Figure 13a,c. Nevertheless, it may be concluded that in general the feed-forward load compensator, being able to directly react to readily available traction motor torque command (see feed-forward path Figure 6), should be capable of timely commanding precise current demand to the common DC bus, thus improving the anticipated load current tracking ability of the overall control system (as shown in Figures 12 and 13), and to effectively suppress the majority of DC bus voltage excursions in a systematic manner.

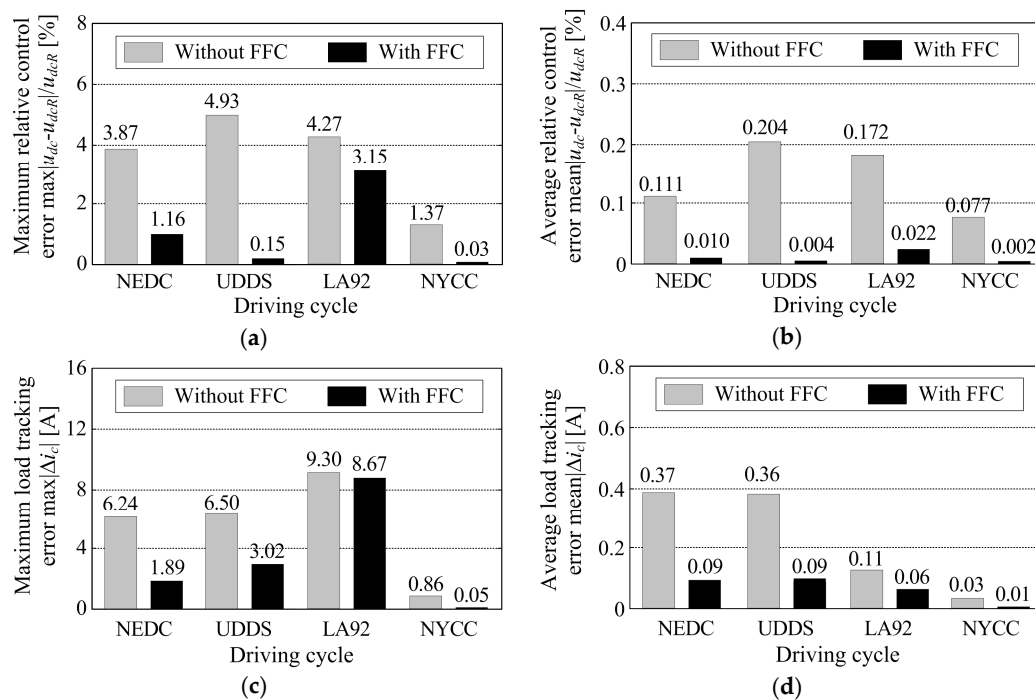


Figure 13. DC bus voltage maximum error (a) and average error (b), load current maximum tracking error (c) and average tracking error (d) quality indices for NEDC, UDDS, LA92, and NYCC driving cycles.

4.4. Analysis for EV Constant Acceleration/Deceleration Regime

The proposed DC bus control strategy, with feed-forward load compensator included, has also been tested for the EVs subject to abrupt acceleration and deceleration regimes, and the comparative results are shown in Figure 14. The responses are characterized by abrupt changes of driveline torque followed by quasi-steady-state torque demand during acceleration and deceleration phases (Figure 14a), which apparently represents a kind of a worst-case scenario for the DC bus control strategy. Namely, the aforementioned driveline torque profile results in relatively slow ramp-like profile of DC bus load i_L during steady acceleration and deceleration, whereas abrupt DC load changes occur at the vehicle acceleration to deceleration (reversal) point (Figure 14b). Note also that the sudden DC bus voltage drop at reversal from acceleration to deceleration command is needed to facilitate reduced motor phase and DC bus voltage required during transient from driving to regenerative braking. The aforementioned abrupt DC bus load i_L transient is, as expected, effectively handled by the ultracapacitor ESS, while the gradual ramp-like DC bus load profiles (during constant acceleration/deceleration) are handled by the battery ESS.

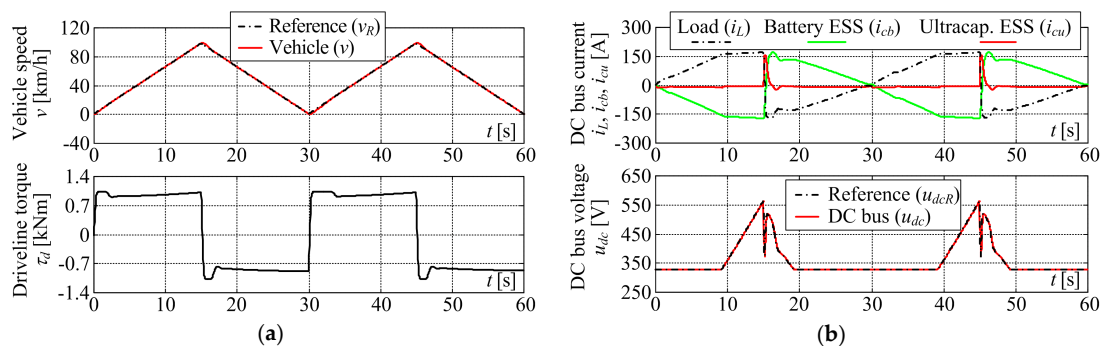


Figure 14. Simulation results for alternating constant acceleration/constant deceleration commands: vehicle speed and driveline torque (a) and DC bus load current and voltage profiles (b).

5. Results of Experimental Verification

The core of the DC bus control system has also been verified by means of experiments conducted on the dedicated down-scaled laboratory setup, previously designed and tested in [40,41]. Figure 15 shows the principal schematic of the laboratory setup which can be externally supplied from the AC grid, or can work in the isolated (islanded) mode. Setup comprises three two-quadrant (buck-boost) DC/DC power converters connected in parallel to the common DC bus, wherein two of those power converters are used for power flow control of the battery and ultracapacitor module-based ESS, and the third power converter is used to emulate a passive or active DC bus load by supplying power to the dissipation resistor or an another battery. Due to safety concerns, the safety and diagnostics system implemented within the programmable logic controller (PLC) limits the DC voltage to 45 V, while the under-voltage trip is pre-set to 30 V. Battery and ultracapacitor ESS current control, and DC bus voltage control algorithms are implemented within an inexpensive PLC, whereas the DC bus load control, and data collection and supervision of the laboratory setup is implemented within the National Instruments LabView environment by using a CompactRIO acquisition and control system. The parameters of the down-scaled laboratory setup and the corresponding DC bus control system are listed in Table 3.

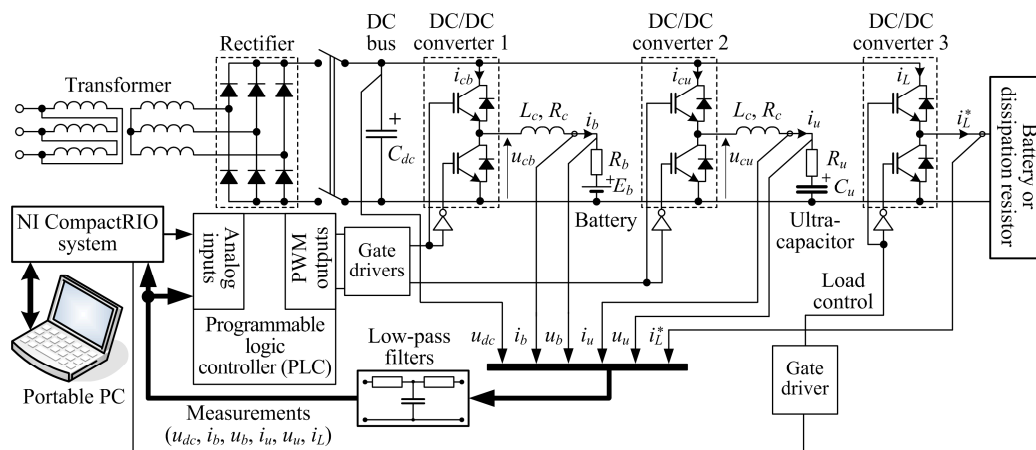


Figure 15. Principal schematic representation of DC bus control system down-scaled laboratory setup featuring three independently controlled DC/DC power converters, battery and ultracapacitor energy storages and variable load, and PLC-based DC bus control system and NI CompactRIO-based supervisory system.

Table 3. Parameters of DC bus control system for down-scaled laboratory setup.

Parameter	Value	Parameter	Value
Inductor inductance L_c	0.7 mH	Ultracapacitor resistance R_u	0.1 Ω
Series resistance of inductor R_c	0.05 Ω	DC bus parasitic lag T_Σ	5 ms
Battery rated voltage and capacity	12V/55Ah	DC bus capacitance C_{dc}	40 mF
Battery internal resistance R_b	0.025 Ω	Ultracapacitor ESS equivalent lag T_{eu}	15 ms
Ultracapacitor voltage limit $U_{u,max}$	28 V	Battery ESS equivalent lag T_{eb}	100 ms
Ultracapacitor rated capacitance C_u	22.2 F	Feed-forward lead time constant T_{ff}	15 ms
Ultracapacitor ESS current controller proportional gain K_{ci}	0.165 V/A	Ultracapacitor ESS current controller integral time constant T_{ci}	7 ms
Battery ESS current controller proportional gain K_{ci}	0.007 V/A	Battery ESS current controller integral time constant T_{ci}	47.5 ms
Ultracapacitor auxiliary controller proportional gain K_{ca}	2.48 A/V	Ultracapacitor auxiliary controller integral time constant T_{ca}	280 ms
DC bus controller proportional gain K_{dc}	1 V/V	DC bus controller integral time constant T_{dc}	80 ms

The results of experimental verification of the DC bus control system for the case of abrupt (stepwise) DC bus load and load profile corresponding to the NEDC driving cycle are shown in Figure 16a,b, respectively. Due to the aforementioned safety features, the DC bus voltage has been

pre-set in both cases in the middle of the usable voltage range (i.e., $u_{dcR} = 37.5$ V is used). For the same reason, the final part of the NEDC certification cycle, corresponding to the final accelerating of the vehicle towards 120 km/h and subsequent abrupt braking have been omitted from the analysis to avoid tripping the over-voltage and under-voltage protections at the laboratory setup.

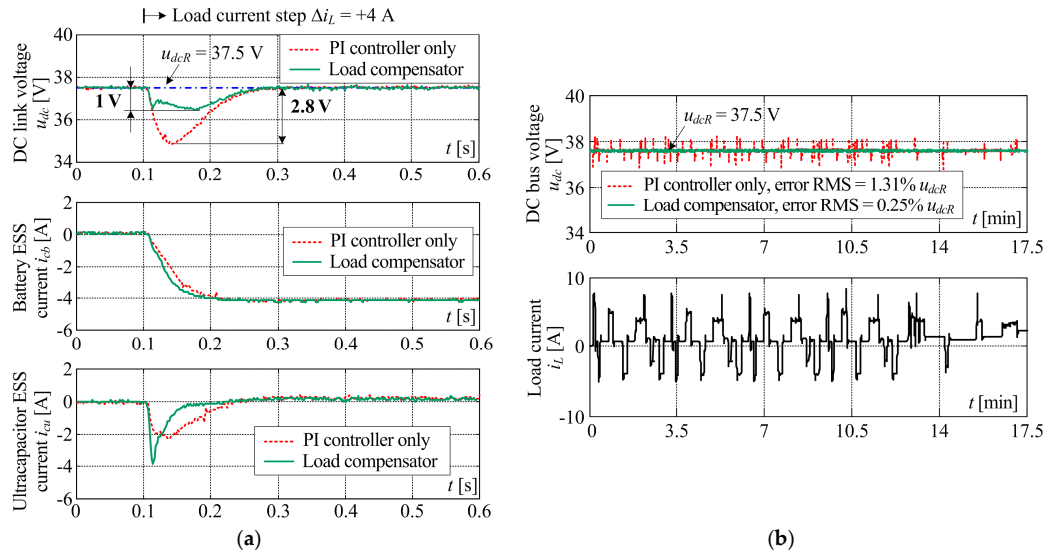


Figure 16. Comparative experimental results of DC bus control system without and with direct feed-forward load compensator: stepwise load change (a) and scaled-down NEDC-like load profile (b).

The comparative results in Figure 16a, obtained for stepwise load current change with the step magnitude of 4 A, indeed show that the proposed control system design results in well-damped and rather fast response of the DC bus control system and the inner current control loops of individual ESSs (i.e., battery and ultracapacitor). As expected, the use of DC bus control system comprising both the PI feedback controller and the direct load compensator results in notably smaller DC bus voltage drop and faster DC bus voltage recovery compared to the case when PI feedback controller is used alone. This is further confirmed by the comparative traces obtained for the case of down-scaled DC bus load corresponding to EV driveline subject to highly dynamic NEDC certification cycle. In particular, the feed-forward compensator-based control system load suppression ability, expressed in terms of DC bus voltage reference tracking root mean squared (RMS) error, is over five-fold improved compared to the case when only PI feedback controller is used. As explained earlier, this is primarily due to the better use of load suppression potential of the ultracapacitor ESS featuring a fast current controller under the fast current demand from the direct feed-forward load compensator.

6. Discussion and Concluding Remarks

This paper has presented the design of EV DC bus control system based on a battery/ultracapacitor HESS, and its coordination with the fully electrified vehicle driveline control system via the readily available traction motor current and voltage variables. The control strategy has included the upper-level DC bus voltage feedback PI controller augmented with a direct load compensator for fast suppression of abrupt DC bus loads, which have commanded appropriate current references to the battery/ultracapacitor HESS via the intermediate-level dynamic load distribution scheme. The feedback control design has been carried out by using the damping optimum criterion. The proposed methodology has been verified by means of simulations for different realistic EV-operating regimes, and experimentally on the down-scaled DC bus laboratory setup. Simulation and experimental results have pointed out to:

1. Damping optimum tuning approach having been able to ensure well-damped closed-loop behavior of designed feedback systems (i.e., less than 6% step response overshoot). It has also

been able to precisely adjust the closed-loop response speed of battery/ultracapacitor HESS inner current control loops via the choice of the closed-loop equivalent time constant. This has enabled rather fast-current reference tracking of the ultracapacitor ESS (30 ms step response settling time has been obtained), while also achieving notably slower battery ESS response (characterized by 400 ms response time) within the DC bus control system.

2. The load suppression ability of the overall DC bus control system having been notably improved by the introduction of the direct load compensator, which has typically resulted in three to five times smaller DC bus voltage excursion after an abrupt DC bus load. In particular, for the realistic scenario of 25% stepwise change of EV driveline load, DC voltage excursion is reduced from 8.9% of the target DC bus voltage value in the case of PI feedback controller to 1.7% in the case when PI controller has been augmented by the load compensator based on DC bus load reconstruction from traction motor variables.
3. The DC bus voltage target tracking performance having benefited from the inclusion of direct feed-forward load compensator for different certification driving cycles and corresponding DC bus voltage profiles calculated from traction motor variables. Namely, use of direct feed-forward load compensator has resulted in the reduction of the maximum DC bus voltage tracking error from 3.87% to 1.16% of the DC voltage target in the case of NEDC driving cycle, and from 4.93% to just 0.15% in the case of UDDS scenario. Similar reduction has also been observed for NYCC driving scenario (i.e., from 1.37% to just 0.03% has been obtained), whereas LA92 driving cycle has been characterized by the DC bus excursion reduction from 4.27% to 3.15%. Generally speaking, the DC bus voltage average tracking error has been reduced between one and two orders of magnitude for all driving cycles when load compensator has been used.

Future research may be directed towards the extension of the proposed control strategy for multiple energy storages, and related applications in renewable energy systems and EVs.

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Nomenclature

Abbreviations

AC	Alternating current
$d-q$	Field-torque rotating reference frame
DC	Direct current
DC/DC	DC-to-DC (power conversion)
EMF	Electromotive force
ESS	Energy storage system
EV	Electric vehicle
HESS	Hybrid energy storage system
LA92	California Unified Cycle
NEDC	New European Driving Cycle
NYCC	New York Certification Cycle
PI	Proportional-integral
PWM	Pulse-width Modulation
RMS	Root mean squared (error)
UDDS	Urban Driving Dynamometer Schedule

Greek Symbols

α	Filtering time constant scaling factor
κ_u	DC bus voltage target scaling factor
ρ_a	Density of air
Φ_r	Rotor permanent-magnet field flux
Ω_{bw}	Closed-loop bandwidth
Δi_c	DC bus load tracking error
Δi_{Ur}	Ultracapacitor ESS auxiliary controller output
$\Delta u_d, \Delta u_q$	d - q frame cross-axis coupling terms
ϕ	Stator current vs. voltage phase angle
θ	Rotor electrical angle
τ_R	Traction motor torque reference
ω	Rotor electrical speed
ω_m, τ_m	Traction motor speed and torque
ω_d, τ_d	Driveline speed and torque
ξ	Battery state of charge

Subscripts

1,2,3	PMSM stator quantity
a	Auxiliary control loop
b	Battery control loop quantity
dr	Virtual driver
$D1, D2$	Quantity of fly-wheeling diode within DC/DC power converter
di	Lag (of motor inverter voltage)
e	Equivalent (time constant)
i	PMSM current control loop
l	Lag (of power converter voltage)
u	Ultracapacitor ESS quantity
v	Voltage control loop
L	Load
ph	Phase quantity
r	PMSM rotor (field flux)
R	Reference (target) value
$T1, T2$	Quantity of semiconductor-controlled switch within DC/DC power converter
Σ	Lumped quantity

Superscripts

\hat{x}	Estimated value of x
\bar{x}	Average value of x

Variables

$\cos\phi$	Motor power factor
d_b, d_u	Battery and ultracapacitor ESS DC/DC power converter PWM duty cycles
E_b	Battery electromotive force
i_b, i_u	Battery and ultracapacitor currents
i_c	DC bus input current
i_{cb}, i_{cu}	Battery/ultracapacitor ESS input currents
i_d, i_q	Direct (field) and quadrature (torque) currents in the d - q rotating reference frame
i_{dR}, i_{qR}	Field and torque current references
i_L	DC bus load current
I_{ph}	Stator phase current amplitude
$u_{1,2,3(R)}$	PMSM stator voltages (references)
u_{cb}, u_{cu}	Battery and ultracapacitor ESS DC/DC power converter output voltage
u_{dR}, u_{qR}	Direct and quadrature axis voltage components
u_{dR}, u_{qR}	Direct and quadrature axis voltage references from PI current controllers
u_{uR}	Ultracapacitor ESS voltage reference

u_{dc}	DC bus voltage
u_{emf}	AC machine electromotive force
U_{ph}	Stator phase voltage amplitude
v	Vehicle longitudinal speed
Parameters	
C_d	Air drag coefficient
C_{dc}	DC link capacitance
C_u	Ultracapacitor capacitance
D_2, \dots, D_n	Damping optimum characteristic ratios
g	Free fall (gravity) acceleration
i_g	Gearbox transmission ratio
J_m, J_w	Motor and wheel inertia, respectively
J_{eq}	Equivalent inertia at PMSM rotor side
k_E, k_T	PMSM electromotive force and torque constants, respectively
K_{ca}, T_{ca}	Auxiliary ultracapacitor ESS state-of-charge controller gain and integral time constant
K_{cd}, K_{cq}	PMSM current controller proportional gains
K_{ci}, T_{ci}	Battery and ultracapacitor ESS current controller gain and integral time constant
K_{dc}, T_{dc}	DC bus controller proportional gain and integral time constant
K_{dr}, T_{dr}	Virtual driver proportional gain and integral time constant
L_a, R_a	PMSM armature inductance and resistance
L_c, R_c	Inductor inductance and resistance
R_{tot}	Overall series resistance
m_v	Vehicle mass
M_{max}	Maximum value of modulation index
p	PMSM number of pole pairs
r_w	Wheel radius
R_o	Rolling resistance coefficient
T_a	PMSM armature time constant
T_l, T_{di}	Voltage response delay of DC/DC power converter and motor inverter
T_e	Closed-loop equivalent time constant
T_{ea}	Equivalent time constant of the auxiliary ultracapacitor state-of-charge control loop
T_{ei}	Equivalent time constant of the PMSM current control loop
T_{cd}, T_{cq}	PMSM current controller integral time constants
T_{eb}, T_{eu}	Equivalent time constants of battery and ultracapacitor current control loops
T_{fi}, T_{fo}	Current and voltage measurement (filter) time constants
T_f, T_{FF}	Feed-forward load compensator lag time constant and lead time constant
T_{Σ}	Parasitic time constant of the voltage control loop
$T_{\Sigma i}$	Parasitic time constant of the current control loop
$T_{\Sigma u}$	Parasitic time constant of the auxiliary state-of-charge control loop
U_{min}	DC bus voltage lower bound
U_{max}	DC bus voltage upper bound

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