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Readout schemes for low noise single-photon avalanche diodes fabricated in conventional HV-CMOS technologies

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ABSTRACT

Three different pixels based on single-photon avalanche diodes for triggered applications, such as fluorescence lifetime measurements and high energy physics experiments, are presented. Each pixel consists of a 20 μm × 100 μm (width × length) single photon avalanche diode and a monolithically integrated readout circuit. The sensors are operated in the gated mode of acquisition to reduce the probability to detect noise counts interferring with real radiation events. Each pixel includes a different readout circuit that allows to use low reverse bias overvoltages. Experimental results demonstrate that the three pixels present a similar behavior. The pixels get rid of afterpulses and present a reduced dark count probability by applying the gated operation. Noise figures are further improved by using low reverse bias overvoltages. The detectors exhibit an input dynamic range of 13.35 bits with short gated 'on' periods of 10 ns and a reverse bias overvoltage of 0.5 V. The three pixels have been fabricated in a standard HV-CMOS process.

1. Introduction

An increasing number of novel applications requiring fast and accurate radiation detectors has appeared over the last years. These applications cover a wide range of fields, including time-of-flight (TOF) ranging, fluorescence lifetime measurements, 3D imaging for bio-applications, astronomical observations and high energy physics (HEP) experiments. High sensitivity, timing precision and low costs of fabrication are the most severe constraints.

This situation has created a favorable atmosphere for the development of a large variety of sensor technologies, such as Charge Coupled Devices (CCDs) [1], CMOS Monolithic Active Pixel Sensors (MAPS) [2], Silicon PhotoMultipliers (SiPMs) [3] and DEPleted Field Effect Transistors (DEPFETs) [4]. Although much progress has been made, the present options provide a reduced readout speed, generate weak signals or regard dedicated technologies. More recently, a very innovative alternative based on 3D integration has also emerged [5], yet this option is at a very early stage of exploitation due to cost concerns. Nevertheless, Single-Photon Avalanche Photodiodes (SPADs, or alternatively Geiger-mode APDs or GAPDs) [6,7] offer a virtually infinite internal gain and precise time response that are well above the other options. Moreover, the sensor and the readout electronics can be monolithically integrated on a single CMOS die [8]. However, these sensors suffer from high levels of intrinsic noise that degrade their performance. In addition, in order to not lose any events due to signal, the noise also increases the amount of necessary area to store the generated data. In this article, three different monolithic pixel detectors based on SPADs that perform gated acquisition to minimize the detection of false counts are presented. Each pixel includes a different readout scheme that is used to minimize the sensor intrinsic noise by means of low sensor bias operation. The characterization of the three fabricated pixels is also described here.

2. Avalanche photodiodes

An SPAD is based on a p–n junction reverse biased above its breakdown voltage (V_{BD}) in the so-called Geiger mode. At this polarization, a high electric field exists inside the junction area forming the multiplication region. If a free carrier having more energy than the band gap of the material reaches the multiplication region, it can generate an e^-–h^+ pair. This e^-–h^+ pair can be accelerated by the high electric field up to the point at which it can generate another e^-–h^+ pair by impact ionization. The new pair can be accelerated as well, thus starting an avalanche multiplication process that gives raise to the prompt generation of a detectable macroscopic current pulse. This process results in an internal gain of between 10^5 and 10^6. However, since the avalanche is self-sustained, the current continues to flow and it needs to be stopped in order to avoid damaging the

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device. This operation is performed by the quenching electronics by lowering the reverse bias voltage down to or below V_{BD}. Finally, the bias of the sensor has to be restored so that the sensor is made sensitive again for upcoming avalanches.

The quenching circuits are either implemented by means of passive or active components [9]. The Passive Quenching Circuits (PQCs) use a resistive element (R_Q), usually a simple resistor or a MOS transistor properly biased, placed in series with the sensor. The resistive element (R_Q) together with the sensor resistance (R_D), the sensor capacitance (C_D) and the parasitic capacitance (C_P) due to the interconnections and the front-end electronics generate an RC circuit. When the photodiode is triggered, the RC circuit quenches the avalanche by lowering the reverse bias voltage down to V_{BD}. The quenching time is given by $(C_D+C_P)R_D$, provided that $R_Q \gg R_D$ [9]. In addition, the same circuit can also return the sensor to its operating voltage after the quenching time. This operation is known as recharge or reset. The recharge time is given by $(C_D+C_P)R_Q$ [9]. The PQCs present poor control over the quenching and recharging times, since high R_Q generate short quenching but long recharging times, and vice versa. On the other hand, the Active Quenching Circuits (AQCs) sense the raising edge of the avalanche and react back on the device by forcing the reverse bias voltage below V_{BD}. Although the AQCs allow to reduce the quenching time, they also tend to increase the parasitic capacitance as a consequence of the higher number of components connected to the sensing node. Active Recharge Circuits (ARCs) provide a full control of the recharge time of the sensor and are typically implemented through a MOS switch. Mixed active–passive quenching circuits that combine the advantages of purely passive and purely active quenching circuits are also possible.

Despite the extraordinary efficiency of SPADs in single photon detection, there are however some drawbacks and limitations. Charge carriers that are trapped during an avalanche flow by trapping centers due to impurities and crystal defects can trigger Geiger pulses (indistinguishable from actual radiation-triggered pulses) if they are released after the recharge time. These false pulses are called afterpulses and they depend on the trap density, the number of carriers generated during an avalanche and the release time of these carriers. Moreover, thermal and tunneling generated carriers within the p–n junction can also trigger false pulses. The frequency of generation of these spurious pulses, known as Dark Count Rate (DCR, usually expressed in counts per second or Hz), depends on the technology, the sensor area, the reverse bias overvoltage (V_{OV}) over V_{BD} and the temperature. Both afterpulses and dark counts degrade the performance of the sensor, limiting the range of detectable signals in light intensity measurements and leading to erroneous results in yes/no applications. In addition, they also increase the amount of data that has to be stored for the subsequent processing in which the signal is discriminated from the noise.

Solutions commonly adopted to reduce the noise in SPAD detectors regard dedicated technologies with lower doping profiles [10], cooling methods either with Peltier elements [11] or air cooling [12], and advanced front-end circuits that use PQCs or AQCs with ARCs [13–16]. However, none of the presented techniques is completely satisfactory given the high fabrication costs of dedicated technologies, the reduced applicability of cooling methods or the limited efficiency of advanced front-end circuits in reducing the afterpulsing probability only.

Apart from that, in those applications where the signal arrival time is known, as for example in TOF ranging, fluorescence lifetime measurements or HEP experiments, the sensor can be operated in the gated acquisition mode. In contrast with the free-running mode of operation, where the sensor is always reverse biased above V_{BD} at a fixed voltage, in the gated acquisition the reverse bias voltage swings from over to under V_{BD} to periodically enable and disable the photodiode. The sensor is then kept active for short periods of time only. As a consequence, the probability to detect dark counts interfering with signal triggered counts (known as Dark Count Probability or DCP) is linearly reduced with the width of the active period of the sensor. In addition, since the active periods of the sensor can be synchronized with the expected signal arrival, no photon counts are missed. On the other hand, considering a fixed operating voltage and temperature, non-active periods longer than the lifetime of the trapping centers allow to completely release the trapped charges. Therefore, the afterpulsing probability can be completely eliminated. In this article, we propose the gated mode of acquisition to synchronize the sensor operation with the expected signal arrival, to reduce the DCP and also to get rid of afterpulses in CMOS SPAD pixel detectors. Moreover, the photodiode can also function with low biases to reduce the DCR. As it will be demonstrated, the reduction of the DCP and the DCR allows to increase the detector performance.

3. Pixel design

The generic schematics diagram of the proposed pixel detector, together with the electronics waveforms, is shown in Fig. 1. It was designed and fabricated with the standard HV-AMS 0.35 μm CMOS technology (h35b4). The pixel detector consists of an SPAD, active inhibition (M_{P0}) and active reset (M_{N0}) switches to perform the gated mode of acquisition and a readout circuit. The transistor M_R was included to study the response of the detector for different recharge times, achieved through an externally adjustable V_{bias}, but it is not used in the gated operation. It could be removed to minimize the area occupation as well as the charge flowing during an avalanche. Note that no components aimed to quench the avalanches have been included [17]. The resistance of the reset switch is taken as R_Q. In the following subsections, the electronics to control the gated mode of acquisition and three different readout circuits that enable low V_{OV} operation will be presented.

3.1. Sensor and mode of operation

The photodiode is implemented by means of a p^+/deep n-tub junction, which is surrounded by a p-tub implantation set to prevent premature edge breakdown (see Fig. 2 for cross section). Additionally, the corners of the sensor are rounded to avoid electric field peaks at the junction corners. The p-substrate is shared with the electronics and therefore connected to ground. The sensitive area is 20 μm × 100 μm (width × length). Reverse bias overvoltages over the breakdown voltage are applied to the sensor cathode to operate the Geiger mode. The readout is performed at the anode or sensing node (V_S) due to its lower intrinsic capacitance to ground, which is beneficial in reducing the afterpulsing probability.

The advantages of the gated operation with commercially available germanium [18] and InGaAs/InP [19] APDs for the detection of 1–1.3 μm wavelengths have already been discussed in the literature. In these cases, short gate pulses are achieved with voltage generators. Other possibilities to apply the gating pulse are based on AC coupling [20] or high frequency sinusoidal voltages [21], but whereas the former imposes a limitation on the repetition rate due to the coupling capacitor recharge time constant, the latter keeps variable the reverse bias of the sensor during gating periods. Recently, CMOS SPAD detectors with monolithically integrated electronics to operate the gated mode were also reported for fluorescence measurements [15,22].

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However, a large number of transistors per pixel is needed in these configurations.

In the SPAD pixel detectors proposed in this work, the sensor is operated in the gated acquisition mode by means of two external signals (RST and INH) implemented through MOS transistors (M_{N0}–M_{P0}). When the RST signal is high, and thus the transistor M_{N0} is 'on', the sensor bias is promptly increased up to $V_{BD}+V_{OV}$. As a result, the sensor is recharged and the gated 'on' period is started. Given that avalanches can still occur while the sensor is in its recharge phase (RST='1' and M_{N0} 'on'), the external RST pulse has to be shorter as possible in order to avoid low resistive paths quenching the avalanche. In this work, short RST pulses of 2 ns with a recharge transition of less than 1 ns have been used. On the contrary, when the INH signal is low, and thus the transistor M_{P0} is 'on', the polarization of the sensor is reduced below V_{BD} ($V_{BD}+V_{OV}-V_{DD}$, with V_{DD}=3.3 V). The sensor enters the gated 'off' period and it remains in this state until the next raising of the RST signal. Note that V_{OV} is limited to V_{DD} to perform the gated operation with the proposed configuration. When an avalanche is triggered during the gated 'on' periods, the self-sustained current that flows through the junction discharges the sensor capacitance (C_D) and charges the parasitic capacitance (C_P) of V_S in picoseconds until its voltage raises up to V_{OV}. At this point, the polarization of the sensor has dropped down to V_{BD} and the avalanche is quenched. The node V_S is connected to the readout electronics, which converts the analog voltage into a digital pulse.

3.2. Readout schemes

A low V_{OV} is desired to reduce the DCR. However, low overvoltages are not allowed in this technology given that the threshold voltage of the nMOS transistors is set at 0.5 V. Three readout circuits that overcome this drawback by using different strategies have been used in this work. However, although the scheme adopted to detect the avalanche voltage (V_{OV}) is different in each circuit, the readout circuits share some features. They are all compatible with the gated operation and they allow to store 1 bit of information within the pixel cell. To achieve this, the storage component goes through two stages. The first stage takes place during the gated 'on' periods of the sensor, when the storage component is at its sampling mode. The duration of the sampling mode is called period of observation (t_{obs}). In contrast, the second stage occurs during the gated 'off' periods, when the 1 bit memory is latched. The performance of this component is controlled by means of an external signal (CLK1), which has been implemented through a MOS switch. Moreover, all the pixels use a simple address circuit based on a pass gate (M_{N14}, in Fig. 1) activated by an external signal (CLK2) to control the reading of the pixel. When triggered by the CLK2 signal (i.e., CLK2=1'), the pixel feeds its corresponding output pad and the readout is completed.

In a first approach (Fig. 3(a), named 2G), the source node of the RST transistor (GNDA) is raised with regard to the ground node of the readout electronics (V_{SS}). V_{SS} is also the bias of the substrate layer of the sensor and the electronics. Powering, for example,

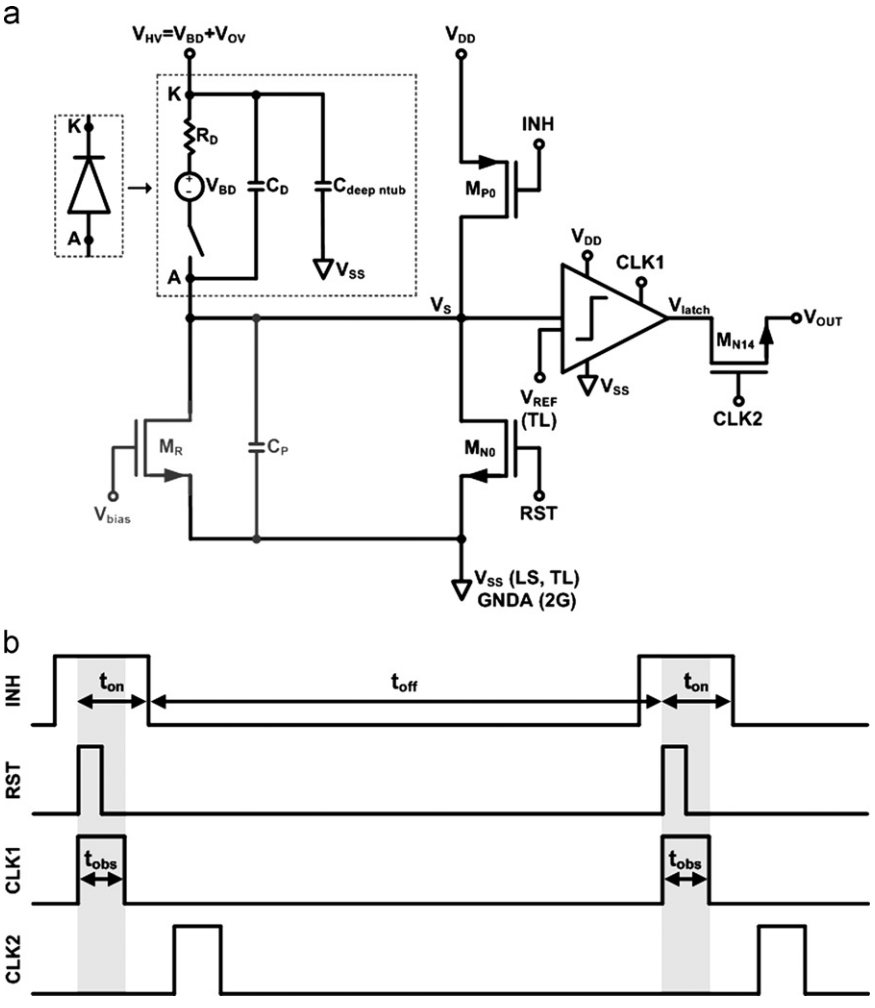

Fig. 1. Generic schematics diagram of the proposed pixel detector (a) and electronics waveforms (b).

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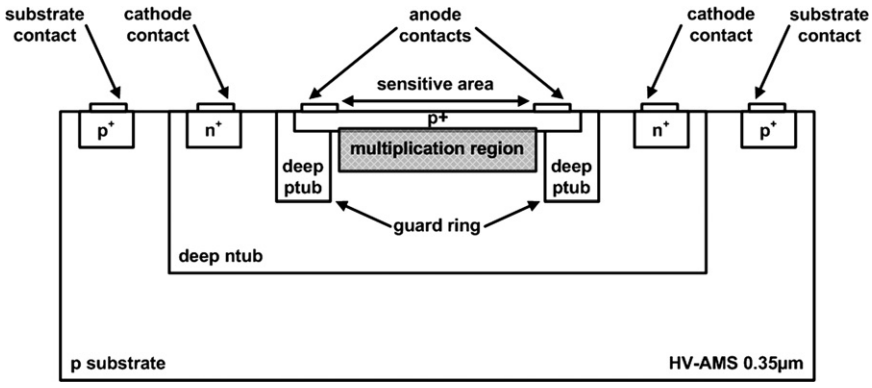

Fig. 2. Cross section of the SPAD fabricated with the standard HV-AMS 0.35 μm CMOS technology.

GNDA to 0.0 V, V_{DD} to 2.3 V and V_{SS} to −1.0 V, low avalanche voltages from 0.65 V can be easily detected by a simple CMOS inverter (M_{P1}–M_{N1}), which was designed to have a threshold voltage of $V_{DD}/2$. The output of the inverter (V_{inv}) is fed in a dynamic latch (M_{N2}–M_{P2}–M_{N3}), which stores in node V_{latch} the result of the gated 'on' period of the sensor ('0' for no avalanche, '1' for avalanche). The external signal CLK1 has been implemented through the MOS transistor M_{N2}. When the CLK1 signal is set high, which occurs at the same exact time as the RST signal does, the gate M_{N2} is switched on and the dynamic latch enters its sampling mode. When the CLK1 signal is set low, the input value of the inverter formed by the transistors M_{P2} and M_{P3} is stored for the gated 'off' period. The CLK1 signal is set low a few nanoseconds before the gated 'off' period is started to avoid storing a false '1'.

In a second proposed circuit that makes use of one ground only (V_{SS}, biased to 0.0 V), low V_{OV} operation is possible thanks to a level-shifter (M_{P4}–M_{P5}–M_{P6}) externally biased (Fig. 3(b), named LS). The level-shifter raises the voltage at the diode output so that V_{OV} is higher than the threshold voltage of the following CMOS inverter (M_{P7}–M_{N4}), which is also set at $V_{DD}/2$. Like in the two grounds scheme, a dynamic latch (M_{N5}–M_{P8}–M_{N9}) functions as a memory element.

In the last case (Fig. 3(c), named TL), the sensing and storage components have been integrated by means of a sole circuit, a track-and-latch comparator [23]. This circuit consists of a pMOS controlled source (M_{P9}), a pMOS differential pair (M_{P10}–M_{P11}), two cross-coupled inverters in positive feedback configuration (M_{P12}–M_{N11}, M_{P13}–M_{N12}) and two nMOS transistors (M_{N10}–M_{N13}). Compared with traditional two-stage comparators, in this design there is no need for a pre-amplifier stage, since the avalanche detection is done by the differential pair. In addition, the threshold voltage of the MOS transistors is not a limitation since the input differential pair is implemented with pMOS transistors.

The operation of the track-and-latch comparator is as follows. During the so-called track phase, which is coincident with the period of observation, the CLK1 external signal is set high and the transistors M_{P10} and M_{P11} sample the two input nodes. These nodes correspond to the sensing node (V_S) and a reference voltage (V_{REF}). The channel current of the transistors M_{P10} and M_{P11} is modulated in function of the values of V_S and V_{REF}, respectively. However, the nodes V_{out+} and V_{out-} are shorted to ground (V_{SS}) through the transistors M_{N10} and M_{N13}. Consequently, the charge injected by the transistors M_{P10} and M_{P11} remains accumulated at their drain nodes. In contrast, during the latch phase, the CLK1 signal is set low, the transistors M_{N10} and M_{N13} are turned off and they no longer connect V_{out+} and V_{out-} to ground. If there has been an avalanche, the accumulated charge at the drain node of the transistor M_{P11} is higher than that of the transistor M_{P10}. Thus, the metastable voltage generated at the node V_{out+} will be higher than that at the node V_{out-} and the transistor M_{N11} will drive more current than the transistor M_{N12}. Consequently, the node V_{out+} will store a logic '1', whereas the node V_{out-} will store a logic '0' due to the positive feedback. The opposite values are generated if no avalanche has been detected [24]. The nodes V_{out+} and V_{out-} are connected to an output buffer to obtain a more robust circuit.

Nevertheless, the design of the track-and-latch comparator deserves special attention. Since the operation mode of the circuit is based on the channel current difference that flows through M_{P10} and M_{P11}, the (W/L) ratios of these transistors have to be optimized so that the cross-coupled inverters enter the saturation mode for a small difference between V_S and V_{REF}. For instance, if the (W/L) ratios of M_{P10} and M_{P11} are too large, the latch circuit will not be able to manage the generated currents and the comparator will always be stuck at the same state [25].

4. Measured results and discussion

A micrograph of the pixel detectors fabricated with the standard HV-AMS 0.35 μm CMOS technology is presented in Fig. 4. In order to obtain the breakdown voltage of the sensor, a test photodiode accessible to the sensing node V_S was included in the same chip. A four wire method implemented by means of a Keithley 2611A source connected to the terminals of the sensor was used for the $I(V)$ characterization. On the other hand, to demonstrate the efficiency of the proposed methods to reduce the noise in SPAD detectors, the response of the pixel in darkness and also to light was tested at a fixed room temperature. The chip was mounted on a printed circuit board and powered with an Agilent E3631A voltage source. An ALTERA Stratix II FPGA-based control board was used to generate the fast logic control signals (RST, INH, CLK1 and CLK2) and also to count off-chip the number of pulses generated by the sensor. The optical response of a pixel was studied as a function of a variable intensity light using a 645 nm LED placed at 0.5 cm far from the SPAD. The light emitter was powered using an HP 3245 A universal source and the current flowing through it was measured by means of an HP 3458A multimeter. The chip, together with the FPGA and the red LED, was placed inside a metallic box to protect the circuit from electromagnetic interferences and uncontrolled light sources and also to avoid increase in the resulting noise. The pixel characterization was done with an adjustable measurement time that depends on the period of observation (t_{obs}) of the sensor and also on the number of times that the observation is repeated (n_{rep}). Different t_{obs} that range from 10 ns to 1280 ns were analyzed for different V_{OV} of 0.5 V, 1.0 V and 1.5 V.

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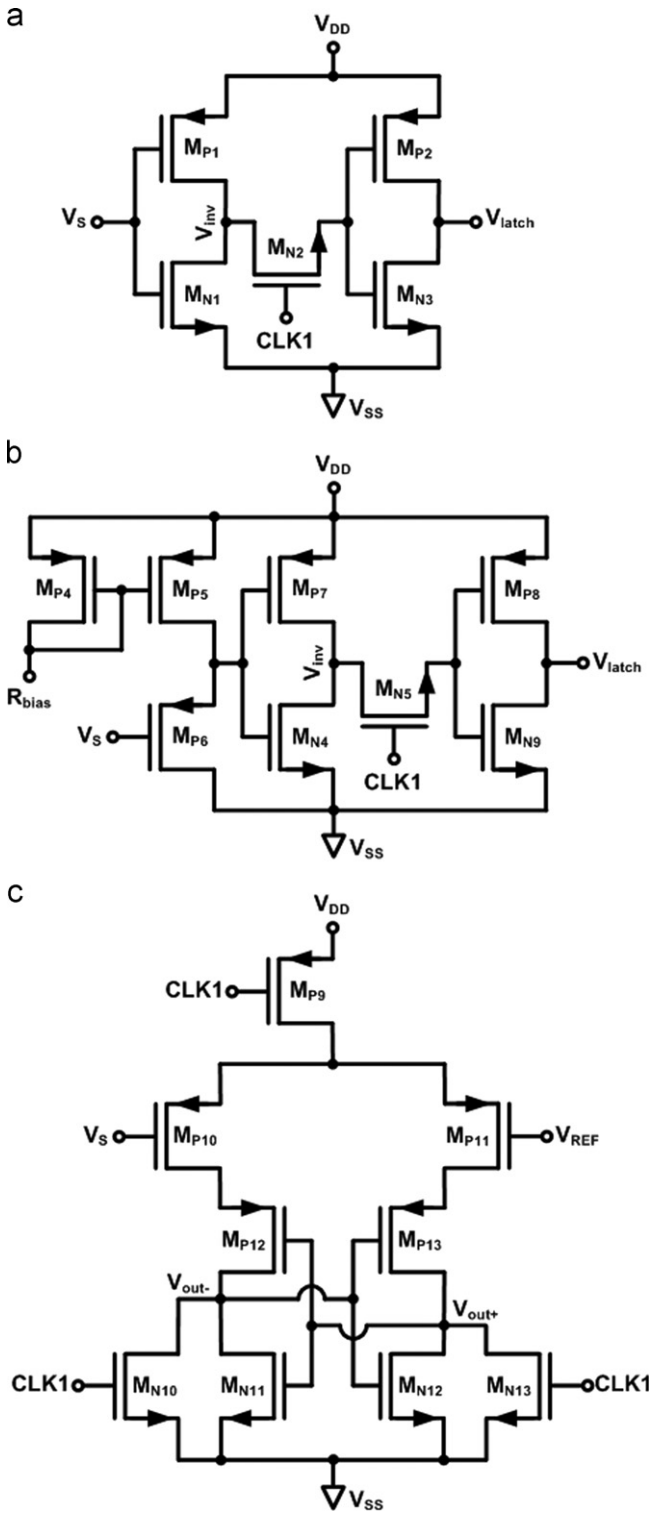

Fig. 3. Schematics diagram of the proposed readout schemes: 2-grounds (a), level-shifter (b) and track-and-latch comparator (c). In (c), nodes V_{out+} and V_{out-} are connected to the output buffer, whose output node is V_{latch}.

Firstly, the measurement of the $I(V)$ characteristic revealed that the breakdown voltage of the sensor is set to 18.94 V. The current generated by the sensor increases from nA to 0.4 mA for a hundred mV range below V_{BD}. Secondly, the afterpulsing probability of the 2-grounds pixel detector from chip 1 was tested by leaving different gated 'off' periods for a fixed t_{obs} of 10 ns. To obtain a statistical population, 100 k repetitions of each

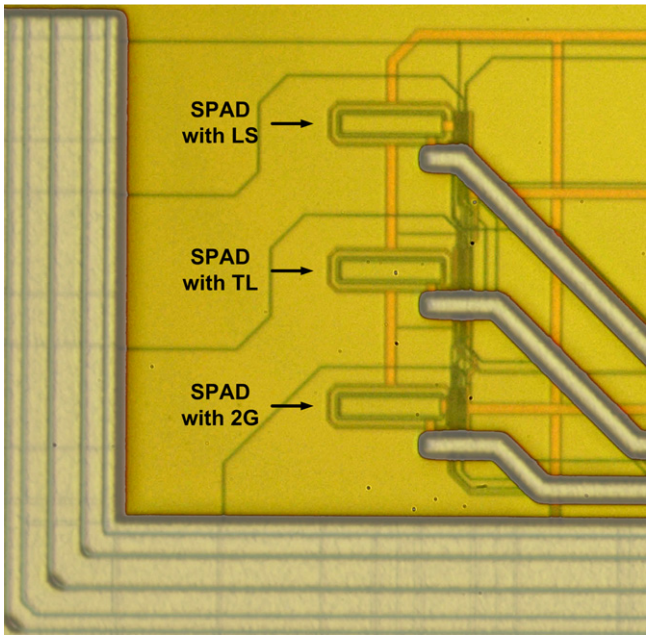

Fig. 4. Micrograph of the fabricated SPAD pixel detectors.

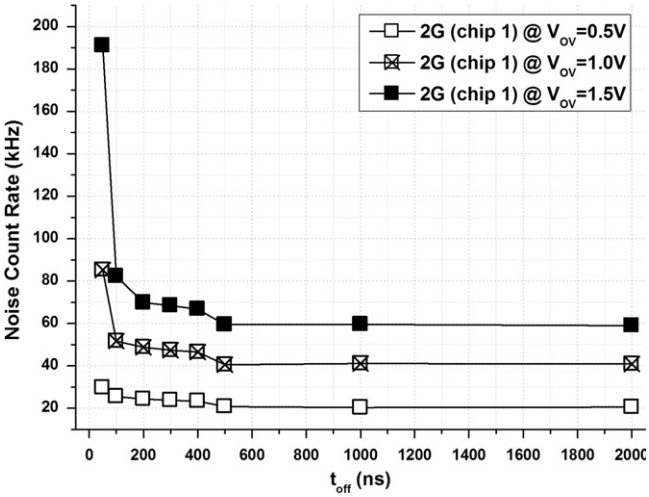

Fig. 5. Noise count rate of the 2G shceme for different t_{off} and V_{OV}.

measurement point were performed. The data extracted from the analysis is shown in Fig. 5, where the Noise Count Rate (NCR) has been obtained from NCR = noise counts/($t_{obs} \cdot n_{rep}$). It was observed that gated 'off' periods of around 500 ns are enough to eliminate the afterpulses for all the V_{OV} measured, which shows that all the trapped charge carriers are released within this time. For short t_{off} periods below 500 ns it was also observed that the probability to detect an afterpulse increases with V_{OV}. This is because the number of carriers generated during an avalanche increases with V_{OV}. After that, the dark counts of the three pixel detectors were measured for different t_{obs} with a fixed t_{off} of 500 ns and different V_{OV} (see Fig. 6). The measurement has also been done for pixel detectors of different chip samples. As expected, the DCR is reduced for a lower V_{OV} (2G pixel detector from chip 1 at 0.5 V, 1.0 V and 1.5 V of V_{OV}). Moreover, the DCR is found to be constant despite the value of t_{obs}, which means that the probability to detect a dark count can be lessened linearly with shorter t_{obs}. Taking for example a DCR of 20 kHz (2G pixel detector at 0.5 V of overvoltage), with a t_{obs} of 10 ns only one dark count will be seen each 5000 repetitions of the measurement.

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For a t_{obs} of 20 ns, this ratio is increased up to 2500 repetitions, and so on for longer t_{obs}. Consequently, in those applications where the signal to be detected is present only in a well defined interval after a triggering signal, the gated operation with discrete t_{obs} in the nanosecond range allows to dramatically reduce the probability to detect dark counts without diminishing the maximum admissible photon counting rate. In Fig. 6, it can also be observed that for a fixed V_{OV} there exist large DCR variations between the different pixels, either from the same chip sample (2G, LS and TL pixel detectors from chip 1 at 0.5 V of V_{OV}) or a different one (2G pixel detector from chips 1 and 5 at 0.5 V of V_{OV}). These results are a consequence of the extreme sensitivity of SPADs to punctual defects in the crystal lattice [26], such as clusters of impurities or dislocations. The variations observed are due to the photodiode and they are not related to the readout circuit.

In the last place, the response to light of the 2-grounds pixel detector from chip 1 was tested for two different t_{obs} of 10 ns and 1280 ns for a fixed V_{OV} of 0.5 V. For each t_{obs}, the detector was illuminated with different light intensities and its response was observed for 100 k times. A counter of a maximum capacity of 100 k counts (n_{rep}) was used to count the generated pulses. The experimental data are plotted in Fig. 7, where the number of counts has been depicted as a function of the LED intensity.

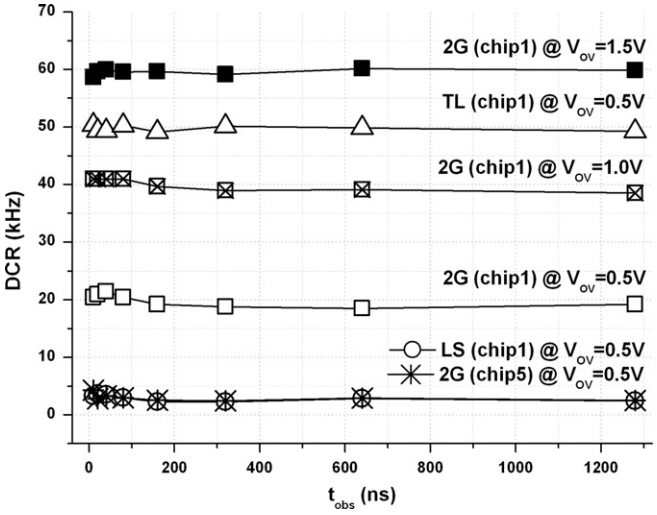

Fig. 6. DCR of the different proposed pixels for different t_{obs} and V_{OV}.

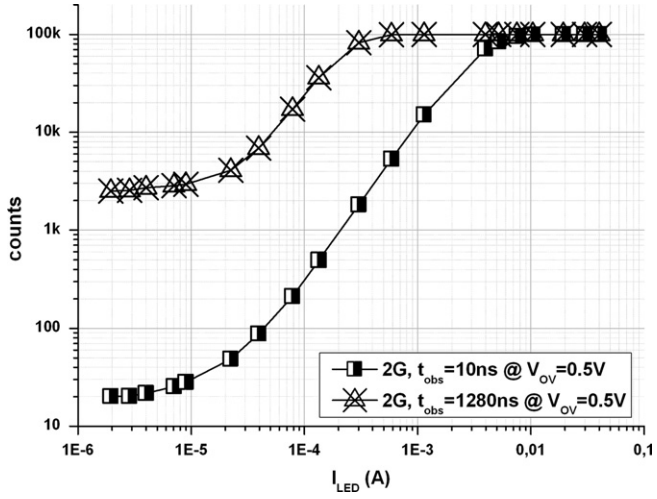

Fig. 7. Response of the 2-grounds SPAD pixel detector to a light intensity of 645 nm at 0.5 V of V_{OV} for different t_{obs} of 10 ns and 1280 ns.

At low intensities, the detected counts are noise counts only (20 noise counts for the 10 ns t_{obs} and 2.58 k noise counts for the 1280 ns t_{obs}) and no signal counts are appreciated. According to DCR=noise counts/($t_{obs} \cdot n_{rep}$), the number of noise counts generated by this pixel are in good agreement with the DCR plotted in Fig. 6. The threshold intensity (I_{th}) corresponds to the minimum light intensity from which signal counts above the noise level are detected. Several light intensities were tested until the generated counts caused counter saturation. The light intensity that causes counter saturation corresponds to the saturation intensity (I_{sat}). As shown in Fig. 7, the measurements with shorter t_{obs} generate lower noise floors. Despite this variation in the noise floor, I_{th} is independent of the width of the t_{obs} time and measured to be 3 μA. However, shorter t_{obs} generate a higher I_{sat}. For the 1280 ns case, I_{sat} is measured to be 1.1 mA, whereas for the 10 ns case I_{sat} is 0.03 A. Due to a reduced noise floor because of the shorter t_{obs}, the range of intensities in which the sensor is sensitive to light is extended at the high end. The input dynamic range (DR) of the gated detector is considered as the ratio between the largest and the smallest detectable light intensities received after the trigger event. It can be expressed in base-2 logarithmic value by DR=$\log_2(I_{sat}/I_{th})$. The DR is 8.65 bits for the 1280 ns case. In contrast, this parameter is increased up to 13.35 bits for the 10 ns case. Identical total measuring times, where the total measuring time is equal to $t_{obs} \cdot n_{rep}$, would give the same DR despite the period of observation used. However, in applications with triggering signals the measurements are taken only during a few nanoseconds after the trigger event and for a fixed number of repetitions. Measurements taken with short t_{obs} yield an extension of the DR, and consequently a better resolution of the pixel, than those ones taken with longer t_{obs}.

All the proposed readout circuits have demonstrated their capability of working with low V_{OV}, which as shown reduces the DCR. However, each circuit has its own advantages and limitations. The 2-grounds scheme, for instance, uses two ground voltages. The bulk node of the transistor M_{N0} (RST) is connected to GNDA and not to V_{SS}, which induces the apparition of the substrate effect. Triple well transistors were discarded due to their high area occupation. In contrast, the level-shifter and the track-and-latch comparator use one ground only, but they need a higher number of transistors. Moreover, both circuits require one additional input, the external bias for the level-shifter and the reference voltage for the track-and-latch comparator. Nevertheless, the track-and-latch comparator offers the advantages of integrating the sensing and storage components within the same circuit and a higher readout speed when compared to the other proposed readout circuits. We can conclude that there is no circuit whose performance is exceptionally better than the other ones.

When referred to gated pixels with low overvoltage operation, two trade-offs may come up for discussion. On the one hand, long gated 'off' periods may reduce the maximum admissible photon counting rate. However, the proposed pixel detectors are intended to triggered applications only, where the gated 'on' periods of the sensor are made coincident with the expected signal arrival. On the other hand, the utilitzation of low overvoltages of a few hundred mV can certainly help to reduce the SPAD's DCR. However, the SPAD's photon detection efficiency (PDE) is not severely reduced, as it could be expected. A good enough PDE has been demonstrated with these sensors biased at low overvoltages [27].

5. Conclusion

Three different pixel detectors based on SPADs operated in the gated mode have been designed and fabricated with the 0.35 μm

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HV-AMS standard technology. Each pixel dectector comprises a readout circuit monolithically integrated with the sensor that allows low overvoltage operation by means of a different scheme. All the readout circuits proposed have showed a similar behavior. It has been demonstrated that the gated mode of operation with short gated 'on' periods allows to eliminate the afterpulsing probability (t_{off}=500 ns) and to minimize the detection of dark counts. In addition, the utilization of low overvoltages reduces the DCR of the sensor. Using periods of observation of 10 ns, the detector performance is highly improved, presenting an extended dynamic range of 13.35bits with a V_{OV}=0.5 V.

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