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A gated single-photon avalanche diode array fabricated in a conventional CMOS process for triggered systems

E. Vilella*, A. Diéguez

Department of Electronics, University of Barcelona (UB), C/Martí i Franquès 1, 08028, Barcelona Spain

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ABSTRACT

A bidimensional array based on single-photon avalanche diodes for triggered imaging systems is presented. The diodes are operated in the gated mode of acquisition to reduce the probability to detect noise counts interfering with photon arrival events. In addition, low reverse bias overvoltages are used to lessen the dark count rate. Experimental results demonstrate that the prototype fabricated with a standard HV-CMOS process gets rid of afterpulses and offers a reduced dark count probability by applying the proposed modes of operation. The detector exhibits a dynamic range of 15 bits with short gated 'on' periods of 10 ns and a reverse bias overvoltage of 1.0 V.

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1. Introduction

Solid-state devices have been used for the detection of radiation, mainly light, since the 1960s. At present time, there exists a good number of sensor technologies and more or less well established. Typical sensors available in the market are charge coupled devices (CCDs) [1], monolithic active pixel sensors (MAPS) [2] and silicon photomultipliers (SiPMs) [3]. CCDs are imaging sensors, whereas SiPMs cannot provide any spatial resolution. MAPS are used for the detection of ionizing particles. Although these sensors can be easily found in cameras, videos and also in the bio-medical field, they cannot supply the required readout speed or temporal and spatial resolution required by many other potential applications. Such a gap in the market has stimulated research and development to improve the already mature technologies but also to explore new ones, like for instance column parallel CCDs (CPCCDs) [4] and depleted field effect transistors (DEPFETs) [5]. DEPFETs offer two-dimensional resolution and are being mainly developed for the detection of ionizing particles. In addition, single-photon avalanche diodes (SPADs) (or alternatively Geiger-mode APDs or GAPDs), which provide an extremely high sensitivity and excellent time resolution that allow to detect single photons in picosecond rise times [6], have regained interest due to the recent achievement to monolithically integrate the sensor and the readout electronics on a

single CMOS die [7]. However, these sensors suffer from high levels of intrinsic noise that degrade their performance.

Each technology has its own advantages and drawbacks, so the appropriate one must be chosen according to the requirements of the application. In this article, we present an SPAD detector with the sensor and the front-end electronics monolithically integrated with the standard HV-AMS 0.35 μm CMOS technology (h35b4). Two main techniques have been implemented to reduce the noise. On the one hand, the sensor can be operated in a gated mode to reduce the probability to detect the noise. On the other hand, the sensor can function with low biases to reduce the intrinsic noise while the photon detection efficiency is still good enough. No cooling methods or digital processing have been used to diminish noise figures. The detector was especially designed regarding applications related with high energy physics experiments. In particular, it was designed to serve as a tracker detector to reconstruct the particle path in future linear colliders [8]. However, it could be used in any other application that operates with a trigger signal, such as three-dimensional imaging, fluorescence spectroscopy and time-of-flight ranging.

2. Single-photon avalanche diodes

An SPAD is based on a p–n junction reverse biased above its breakdown voltage (V_{BD}) in the so-called Geiger mode. At this polarization, there exists a very high electric field within the junction area forming the avalanche region. If a free carrier having more energy than the band gap of the material reaches the

* Corresponding author. Tel.: +34 934 039 157; fax: +34 934 021 148.
E-mail address: evilella@el.ub.es (E. Vilella).

avalanche region, it can generate an e^-h^+ pair. This e^-h^+ pair can be accelerated by the high electric field up to the point at which it can generate another e^-h^+ pair by impact ionization. The new pair can be accelerated as well, thus starting an avalanche multiplication process that gives rise to the prompt generation of a detectable macroscopic current pulse. This process results in an internal gain of between 10^5 and 10^6 . However, since the avalanche is self-sustained, the current continues to flow and it needs to be stopped in order to avoid burning the device. This operation is performed by the quenching electronics, typically implemented by means of a resistor placed in series with the sensor, by lowering the reverse bias voltage down to or below V_{BD} . Finally, the bias of the sensor has to be restored so that the sensor is made sensitive again for upcoming avalanches.

Despite the extraordinary efficiency of SPADs in single photon detection, there are however some drawbacks and limitations. Thermal and tunneling generated carriers within the p-n junction can also trigger avalanche pulses that are indistinguishable from actual radiation-triggered pulses. The frequency of generation of these spurious pulses, known as dark count rate (DCR, usually expressed in Hz), depends on the doping profile, the quality of the technology, the reverse bias overvoltage (V_{OV}) over V_{BD} and the temperature. Moreover, charge carriers that were trapped by crystal defects during an avalanche flow also generate false pulses when they are released at a certain time delay and re-trigger the SPAD. The afterpulsing probability is a function of the trap density, the number of carriers generated during an avalanche and the release time of these carriers. Both dark counts and afterpulses degrade the performance of the sensor, leading to erroneous results in yes/no applications and limiting the range of detectable signals in light intensity measurements. In addition, they also increase the amount of data that has to be stored for the subsequent processing in which signal is discriminated from noise. Apart from that,

given the extreme dependence of the DCR on the cleanness of the fabrication process, an excessively irregular DCR distribution may appear amongst the pixels of bidimensional arrays of SPADs [9]. Punctual defects in the crystal lattice, such as clusters of impurities or dislocations, may also lead to defective pixels with noise levels well above the acceptable threshold. These pixels, called dead pixels or hot pixels, represent a serious problem for SPAD detectors as they reduce the yield.

Solutions commonly adopted to reduce the noise in SPAD detectors regard dedicated technologies with lower doping profiles [10], cooling methods either with Peltier elements [11] or air cooling [12], and advanced front-end circuits that minimize the avalanche charge flow [13]. Dead pixels are simply switched off by means of digital processing [3]. However, none of the presented techniques is completely satisfactory given the high fabrication costs of dedicated technologies, the reduced applicability of cooling methods, the limited efficiency of advanced front-end circuits or the severe loss of sensitive area induced by switching off dead pixels.

Apart from that, in those applications where the signal arrival time is known, the sensor can also be operated in the gated acquisition mode. In contrast with the free-running mode of operation, where the sensor is always reverse biased above V_{BD} at a fixed voltage, in the gated acquisition the reverse bias voltage swings from over to under V_{BD} to periodically enable and disable the photodiode. The sensor is then kept active only for short periods of time that can be synchronized with the expected signal arrival. Consequently, the probability to detect dark counts interfering with signal triggered counts (known as dark count probability or DCP) is linearly reduced with the width of the active period of the sensor without missing any photon counts. In addition, long enough non-active periods, longer than the lifetime of the trapping levels, allow to completely release trapped charges and therefore to eliminate the afterpulsing probability. In this article, we propose the gated mode of acquisition to synchronize sensor operation with the expected signal arrival, to reduce the DCP and also to get rid of afterpulses in CMOS SPAD bidimensional arrays. In addition, the reduction of the DCP also allows to increase the detector performance.

3. Array design and operation

The block diagram of the proposed SPAD detector together with the schematics of the pixels is shown in Fig. 1. The detector consists of an array of 3×3 pixels. It was designed and fabricated with the standard HV-AMS 0.35 μm CMOS technology (h35b4). Each pixel combines a rectangular SPAD with a sensitive area of $20 \mu\text{m} \times 100 \mu\text{m}$ and the proper readout electronics. The photodiode is implemented by means of a p^+ /deep n-tub junction, which

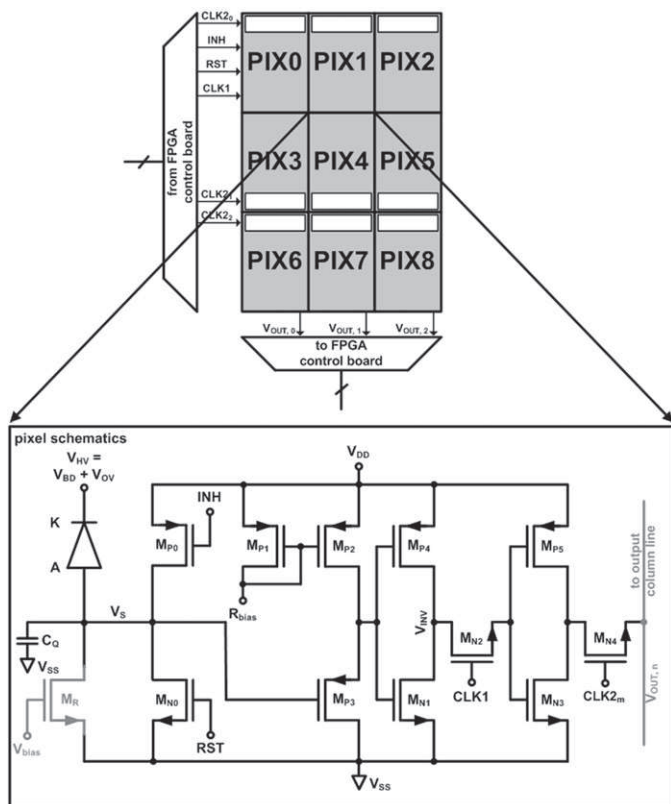


Fig. 1. Block diagram of the proposed 3×3 SPAD array together with the schematics of the proposed digital pixel.

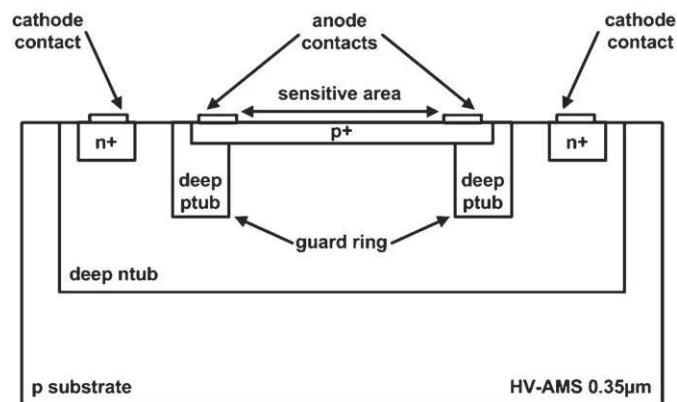


Fig. 2. Cross section of the SPAD fabricated with the standard HV-AMS 0.35 μm CMOS technology.

is surrounded by a p-tub implantation set to prevent premature edge breakdown (see Fig. 2 for SPAD cross section). Additionally, the corners of the sensor are rounded to avoid electric field peaks at the junction corners. The pixels of rows 0 and 1 share the deep n-tub layer, as well as the pixels of row 2 share another one, to obtain a reduced pitch (22.9 μm) and an improved fill factor (90.2%). The breakdown voltage of the junction is measured to be at 18.9 V, while a V_{DD} of 3.3 V powers the rest of the pixel. Reverse bias voltages of $V_{BD} + V_{OV}$ are applied to the sensor cathode to operate the Geiger mode. The readout is performed at the anode or sensing node (V_S). The transistor M_R was included to study the response of the detector for different recharge times, achieved through an externally adjustable V_{bias} , but it is not used in the gated mode of operation. It could be removed to minimize the area occupation as well as the charge flowing during an avalanche.

The benefits of the gated operation with commercially available germanium [14] and InGaAs/InP [15] APDs for the detection of 1–1.3 μm wavelengths have already been discussed in the literature. In these cases, short gate pulses are achieved with voltage generators. Other possibilities to apply the gating pulse are based on AC coupling [16] or high frequency sinusoidal voltages [17], but whereas the former imposes a limitation on the repetition rate due to the coupling capacitor recharge time constant, the latter keeps variable the reverse bias of the sensor during gating periods. Recently, CMOS SPAD detectors with monolithically integrated electronics to operate the gated mode were also reported for lifetime measurements [18,19]. However, a large number of transistors per pixel is needed. We previously claimed the efficiency of the gated operation in SPAD detectors based on single pixels [20].

In the SPAD bidimensional array proposed in this work, the gated operation is controlled by means of two external signals implemented through MOS transistors. When turned on by the RST signal, the transistor M_{N0} quickly recharges the sensor (<1 ns) by increasing its bias over V_{BD} and the gated ‘on’ period is started. However, given that avalanches can still happen while the RST transistor is on, the RST pulse has to be as short as possible in order to minimize the presence of low resistive paths from V_S to ground (V_{SS}) and ensure a robust quenching. On the contrary, when the INH signal switches on transistor M_{P0} , the polarization of the sensor is reduced under V_{BD} , defining this way the gated ‘off’ period. When an avalanche is triggered, the self-sustained current that flows through the junction charges the parasitic capacitance (C_Q) of V_S in picoseconds until its voltage raises up to V_{OV} . At this point, the polarization of the sensor drops down to V_{BD} and the avalanche is quenched. The node V_S is connected to the readout electronics, which is based on a level-shifter (M_{P1} , M_{P2} and M_{P3}) and a CMOS inverter (M_{P4} and M_{N1}). A low V_{OV} is desired to reduce the DCR. However, it is not allowed in this technology given that the threshold voltage of nMOS transistors is set at 0.5 V. In order to overcome this drawback, the level-shifter externally biased was included to rise the avalanche voltage (V_{OV}) over the threshold voltage of the following CMOS inverter, which is set at $V_{DD}/2$. The output of the inverter (V_{INV}) is feed in a dynamic latch (M_{N2} , M_{P5} and M_{N3}) which has been included to make possible in-pixel storage. The dynamic latch is synchronized with the active periods of the sensor by means of the external signal CLK1. This signal switches on the gate M_{N2} at the beginning of the gated ‘on’ period and switches it off a few nanoseconds before the gated ‘off’ period is started to avoid storing a false ‘1’. The interval of time in which the dynamic latch is sampling the inverter output is called period of observation (t_{obs}). The value of V_S at the end of t_{obs} is stored during the gated ‘off’ period. The gating periods are globally applied to all the pixels simultaneously. The waveforms to control the SPAD in the gated operation are depicted in Fig. 3.

The three rows of the SPAD array are read sequentially during the gated ‘off’ periods of the sensor. Thereby, the three columns of

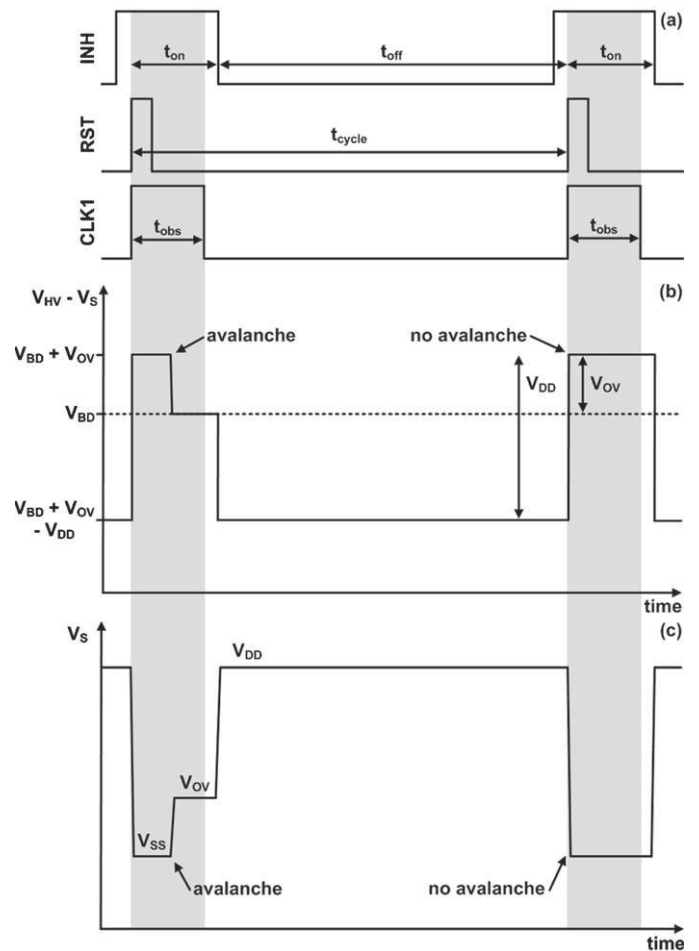


Fig. 3. Waveforms for the gated operation (a), SPAD bias (b) and voltage of the sensing node (c).

each row are read in parallel, requiring only three output pads. To allow external selection of the row m to be read, a simple address circuit based on a pass gate (M_{N4}) activated by the $CLK2_m$ signal has been placed between the dynamic latch and the output column line. The pass gate contacts within one row are connected together and therefore switched on simultaneously. When triggered by $CLK2_m$ (i.e., $CLK2_m = '1'$), each one of the selected pass gates feeds its corresponding output column line, which is directly connected to the output pad. Neither multiplexers nor selection decoders are needed. Despite the small number of pixels, the presented array is a demonstrator of a larger bidimensional camera.

4. Results and discussion

A micrograph of the prototype fabricated with the standard HV-AMS0.35 μm CMOS technology can be seen in Fig. 4. To demonstrate the efficiency of the proposed methods to reduce the noise in SPAD detectors, the response of the pixel in darkness and also to light was tested at room temperature. The chip was mounted on a printed circuit board and powered with an Agilent E3631A voltage source. An ALTERA Stratix II FPGA-based control board was used to generate the fast logic control signals (RST, INH, CLK1 and $CLK2_m$) and also to count off-chip the number of pulses generated by the sensor. The optical response of the pixel to a variable intensity of a 880 nm light was studied by placing an infrared LED above the sensor. The light emitter was powered using an HP 3245A universal source and the current flowing through it was measured by means of an HP 3458A multimeter. The chip, together with the FPGA and

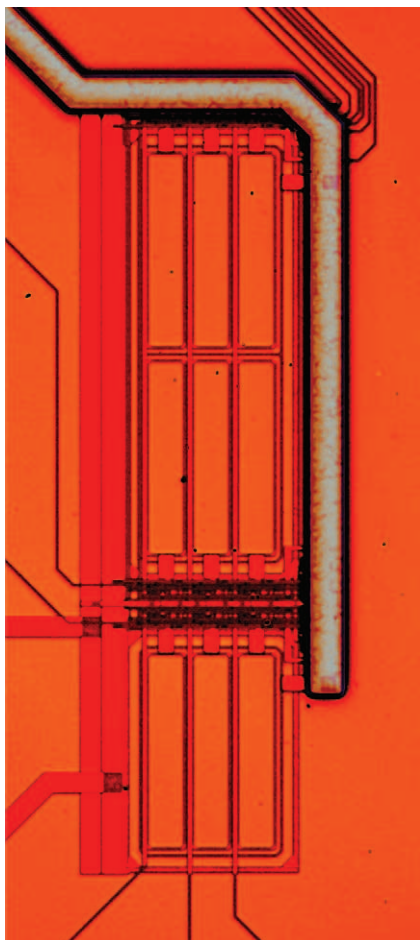


Fig. 4. Micrograph of the fabricated 3 × 3 SPAD array.

the infrared LED, was placed inside a metallic box to protect the circuit from electromagnetic interferences and uncontrolled light sources. The measurements were done with an adjustable integration time that depends on the period of observation of the sensor and also on the number of times that the observation is repeated (n_{rep}). Different t_{obs} that range from 10 ns to 1280 ns were analyzed for different V_{OV} .

Firstly, the afterpulsing probability was tested by leaving different gated 'off' periods for a fixed t_{obs} of 10 ns. It was observed that

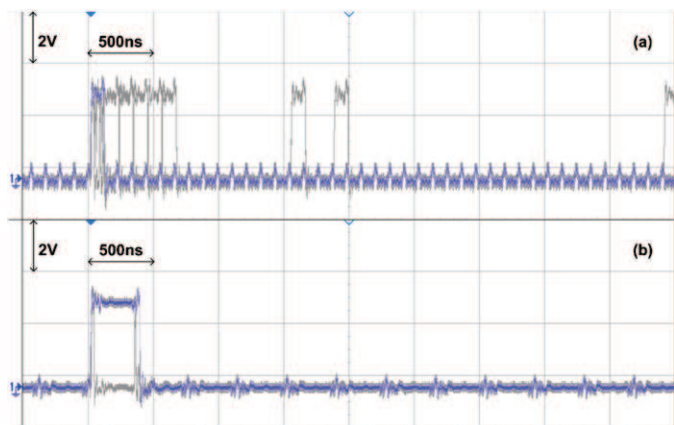


Fig. 5. Presence of afterpulses with a t_{off} of 80 ns (a) and elimination of afterpulses with a t_{off} of 300 ns (b) observed at the pixel output. Measured with the infinite permanence option of the oscilloscope.

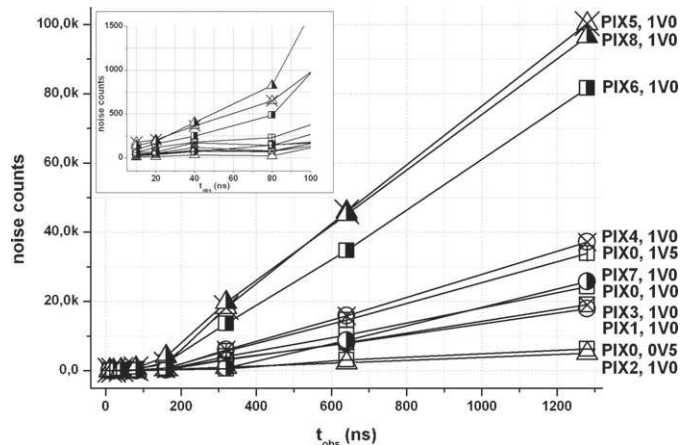


Fig. 6. Noise counts of the different pixels of the array for different t_{obs} and V_{OV} .

gated 'off' periods of 300 ns are enough to eliminate afterpulses at a V_{OV} of 1.0 V (Fig. 5), which shows that the lifetime of the trapping levels is shorter than this time. Secondly, the dark counts of the detector were measured for different t_{obs} with a fixed t_{off} of 300 ns and different V_{OV} of 0.5 V, 1.0 V and 1.5 V. To obtain a statistical population, 400 k repetitions were performed. As expected, dark counts are reduced for a lower V_{OV} (Fig. 6). Moreover, dark counts are lessened linearly with shorter t_{obs} , as it can be inferred from dark counts = DCR × t_{obs} . Taking for example a DCR of 50 kHz, with a t_{obs} of 10 ns only one dark count will be seen each 2000 repetitions of the measurement. For a t_{obs} of 20 ns, this rate increases up to 1000 repetitions, and so on for longer t_{obs} . Consequently, in those applications where the signal to be detected is present only in a well defined interval after a triggering signal, the gated operation with discrete t_{obs} in the nanosecond range allows to dramatically reduce the probability to detect dark counts without missing any photon count. It can also be observed that noise discrepancies amongst the pixels of the array are large (more than a factor 20 between the most and the less noisy ones), as it usually happens in SPAD arrays.

The response of the detector to light was tested for two different t_{obs} of 10 ns and 1280 ns for a fixed V_{OV} of 1.0 V with a counter of a maximum capacity of 8000 counts. For each t_{obs} , the detector was illuminated with different light intensities and its response was observed for 8000 times. The measurement was repeated 10 times to obtain enough statistics. The mean values of the experimental

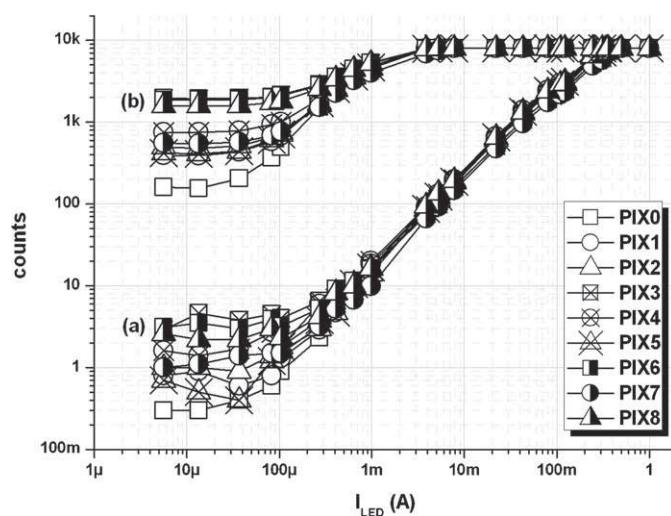


Fig. 7. Response of the SPAD detector to a light intensity of 880 nm at 1.0 V of V_{OV} for different t_{obs} of 10 ns (a) and 1280 ns (b).

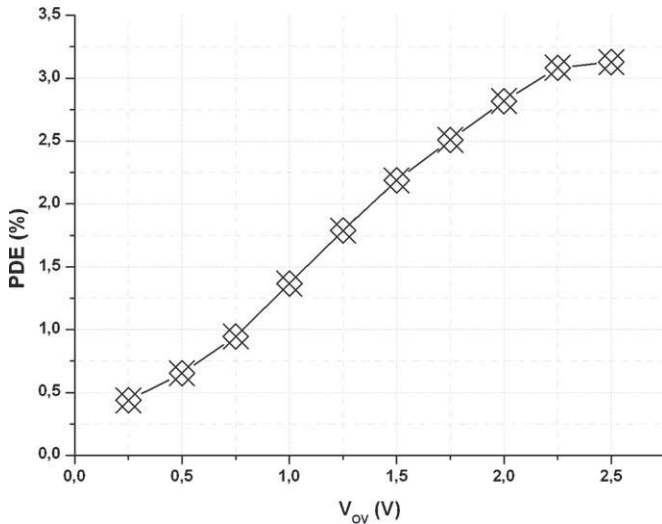


Fig. 8. Photon detection efficiency measured at different V_{OV} for a light intensity of 880 nm.

data are plotted in Fig. 7, where the number of counts has been depicted as a function of the LED intensity. At low intensities, the detected counts are only noise counts and no signal counts are appreciated. The threshold intensity (I_{th}) corresponds to the minimum intensity from which signal counts above the noise floor are obtained. Several light intensities were tested until the generated counts caused counter saturation. The intensity that causes counter saturation corresponds to the saturation intensity (I_{sat}). As shown in Fig. 7, the measurements with shorter t_{obs} generate lower noise floors. Despite this variation in the noise floor, I_{th} is independent of the width of the t_{obs} time and measured to be 13 μ A. However, shorter t_{obs} generate higher I_{sat} . For the 1280 ns case, I_{sat} is measured to be 7.7 mA, whereas for the 10 ns case I_{sat} is 0.35A. Due to a reduced noise floor because of the shorter t_{obs} , the range of intensities in which the sensor is sensitive to light is extended at the high end.

The maximum detectable signal is reached at I_{sat} , whereas the minimum is reached at I_{th} . Hence, the dynamic range (DR) of a gated detector, which is active only for short periods of time that are synchronized with the expected signal arrival, can be obtained by dividing the maximum detectable signal received after the trigger event by the threshold intensity. It can be expressed as $DR = \log_2(I_{sat}/I_{th})$. The DR amongst the different pixels of the detector is of 10 bits for the 1280 ns case. In contrast, this parameter is increased up to 15 bits for the 10 ns case. The DR is not regarded as the response of the detector to light only, as identical total measurement times give the same result despite the period of observation used. Provided that the signal arrival is known, as it happens in applications with triggering signals, the measurements are taken during a few nanoseconds after the trigger events only. Measurements taken with short t_{obs} yield an extension of the DR, and consequently a better resolution of the pixel, than those ones taken with longer t_{obs} .

In the last place, the sensitivity of the detector as a function of V_{OV} was also measured for a fixed wavelength of 880 nm. Fig. 8 shows the mean value of the photon detection efficiency (PDE) of the different pixels of the detector as a function of V_{OV} . The presented values are in good agreement with the literature [18]. As expected, the PDE increases with V_{OV} until saturation. However, low V_{OV} of 1.0 V (PDE of 1.4%) are good enough to allow photon detection.

5. Conclusion

A bidimensional array based on SPADs operated in the gated mode for triggered systems has been designed and fabricated with the 0.35 μ m HV-AMS standard technology. It has been demonstrated that the proposed mode of operation with short gated 'on' periods allows to eliminate the afterpulsing probability and to minimize the triggering of dark counts. A readout circuit to operate the sensor with low reverse bias overvoltages allows to reduce the dark count rate. Using periods of observation of 10 ns, the detector performance is highly improved, presenting an extended dynamic range of 15 bits ($V_{OV} = 1.0$ V). A good enough photon detection efficiency of 1.4% has been measured with a reverse bias overvoltage of 1.0 V. It is concluded that the gated operation allows to reduce noise figures while the sensitivity of the sensor is good enough.

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Biographies

E. Vilella received the BSc degree in Electronic Engineering from the University of Barcelona (UB), Spain, in 2009 and a MSc degree also in Electronic Engineering from the same University in 2010. She is currently working toward the PhD in Engineering and Applied Technologies at UB. Her research interests include the development of low voltage particle tracking pixel detectors based on avalanche photodiodes for future linear colliders such as the International Linear Collider (ILC) and the Compact Linear Collider (CLIC).

A. Diéguez is currently Associate Professor in the University of Barcelona, Spain. He obtained his Physics degree in 1993 by the University of Barcelona. In 1999 he obtained his PhD in Physics from the same University. His research activities during these years have been developed mainly in the field of basic semiconductor research and microelectronic circuit design. He has participated actively in 6 European projects and has more than 40 papers related to the activities commented. From 1993 to 1999 he developed his activity in the field of semiconductor gas sensors. Since 1998 his research activity is devoted to the design of Application Specific Integrated Circuits. The main areas of interest are mixed-signal design of ICs and low-power VLSI design. Specific research topics are microrobotics, low-power smart sensor systems, radiation tolerant electronics and vision systems.