

EXPERIMENTAL AND SIMULATION APPROACHES FOR IMPROVING
INTEGRATED CIRCUIT IMPEDANCE CHARACTERISATION UNDER
ELECTROSTATIC DISCHARGE CONDITION

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To my beloved parents, thank you.



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ABSTRACT

This study was conducted to produce an accurate macro model of an Integrated Circuit (IC) by means of experiment, to be implemented for any application, both in time domain and frequency domain analysis. A probe is designed and optimised to measure a multipin IC with different pin distance. The multipin IC characteristic impedance was experimentally measured using two probes, where the measured combinations of S-Parameter are combined using a self-written software to produce a complete S-Parameter representation of the IC. The S-Parameter file is not suitable for time domain analysis, because vector fitting is required for each simulation. The S-Parameter file is then converted to macro model with controlled accuracy level. The macro model is also ensured its passivity and causality by using commercial macro modelling software (IdEM). The macro model has shown good correlation between time domain and frequency domain analysis. The macro model was then exported as a SPICE model, and was implemented on an Advanced Driver Assistance Systems (ADAS) printed circuit board (PCB). Co-simulation was then performed on the PCB and the results are compared with the measurement results of the fabricated PCB. The SPICE model used in this simulation has shown good resonant frequency correlation between 91 % to 99 %. Finally, the PCB along with the SPICE model was simulated with an Electrostatic Discharge (ESD) gun to observe the current distribution. This research has produced a practical and accurate method, to accurately model an IC as a SPICE model. The SPICE model will help many engineers to improve the accuracy of the virtual prototyping, hence reducing the product's time to market.

ABSTRAK

Kajian ini dilakukan untuk menghasilkan model makro litar bersepadu (IC) yang tepat secara ujikaji. Model makro ini boleh digunakan pada mana-mana aplikasi, baik dalam analisis domain masa ataupun analisis domain frekuensi. Sebuah pengujian frekuensi radio (RF) telah dibina dan dioptimumkan untuk mengukur IC berbilang pin dengan jarak pin yang berbeza. Dua pengujian RF digunakan untuk mengukur galangan IC berbilang pin, di mana kombinasi S-Parameter yang diukur digabungkan menggunakan perisian tersendiri untuk menghasilkan representasi S-Parameter IC yang lengkap. Fail S-Parameter tidak sesuai untuk analisis domain masa, kerana pemasangan vektor diperlukan untuk setiap simulasi. Fail S-Parameter kemudian ditukar kepada model makro dengan tahap ketepatan yang terkawal. Model makro ini juga dipastikan pasif dan kausalitas dengan menggunakan perisian pemodelan makro komersial (IdEM). Model makro ini menunjukkan korelasi yang baik antara analisis domain masa dan domain frekuensi. Model makro kemudian dieksport sebagai model SPICE, dan dilaksanakan pada papan litar bercetak (PCB) Sistem Bantuan Pemandu Termaju (ADAS). Kemudian, simulasi bersama dilakukan pada PCB dan hasilnya dibandingkan dengan hasil pengukuran PCB. Model SPICE yang digunakan dalam simulasi ini telah menunjukkan korelasi resonan yang baik antara 91% hingga 99%. Akhirnya, PCB bersama model SPICE disimulasikan dengan penjana elektrostatik voltan tinggi untuk memerhatikan pengedaran arus elektrik. Kesimpulannya, penyelidikan ini menghasilkan kaedah yang praktikal dan tepat untuk pemodelan IC sebagai model SPICE. Model SPICE ini boleh membantu banyak jurutera meningkatkan ketepatan prototaip, serta mengurangkan masa pemasaran produk.

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LIST OF SYMBOLS AND ABBREVIATIONS

3D	–	Three Dimensional
ADAS	–	Advanced Driver Assistance Systems
BGA	–	Ball Grid Array
BSMS	–	Blind Spot Monitoring System
CAD	–	Computer Aided Design
CAN	–	Controller Area Network
CDM	–	Charge Device Model
CMOS	–	Complementary Metal Oxide Semiconductor
CPWG	–	CoPlanar Waveguide with Ground
DC	–	Direct Current
DSP	–	Digital Signal Processor
DUT	–	Device Under Test
ECU	–	Electronic Control Unit
E-Field	–	Electric Field
EMC	–	Electromagnetic Compatibility
EMI	–	Electromagnetic Interference
ESD	–	Electrostatic Discharge
EV	–	Electric Vehicle
FD	–	Frequency Domain
GSG	–	Ground-Signal-Ground
HBM	–	Human Body Model
HEV	–	Hybrid Electric Vehicle
H-field	–	Magnetic Field
HMM	–	Human Metal Model
I/O	–	Input/Output
IBIS	–	Input/Output Buffer Information Specification

IC	–	Integrated Circuit
IFFT	–	Inverse Fast Fourier Transform
LDW	–	Lane Departure Warning
LIN	–	Local Interconnect Network
MOR	–	Model Order Reduction
MOSFET	–	Metal Oxide Semiconductor Field Effect Transistor
OVF	–	Orthonormal Vector Fitting
PCB	–	Printed Circuit Board
PEV	–	Plug-in Electric Vehicle
PHEV	–	Plug-in Hybrid Electric Vehicle
PI	–	Power Integrity
QFP	–	Quad Flat Package
RF	–	Radio Frequency
RLC	–	Resistor Inductor Capacitor
ROVF	–	Relaxed Orthonormal Vector Fitting
RVF	–	Relaxed Vector Fitting
SI	–	Signal Integrity
SMD	–	Surface-Mount Device
SOC	–	System On Chip
SPICE	–	Simulation Program with Integrated Circuit Emphasis
TD	–	Time Domain
TDR	–	Time Domain Reflectometry
TLM	–	Transmission Level Modelling
TQFP	–	Thin Quad Flat Package
TSV	–	Through Silicon Via
V2X	–	Vehicle-To-Everything
VNA	–	Vector Network Analyser

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CHAPTER 1

INTRODUCTION

1.1 Background of the study

Currently, private companies and government are pushing for cleaner transportation in terms of low carbon emission or even zero emission. Hence more companies are introducing electric vehicles (EV) in support of the move. There are various combinations of electric vehicles, namely Plug-in Hybrid Electric Vehicle (PHEV), Plug-in Electric Vehicle (PEV), and Hybrid Electric Vehicle (HEV). Studies have shown that electric vehicles are able to reduce the emission of greenhouse gases from the fossil fuel combustion engine. However, better control of the power source is still needed to fully benefits from the reduction of the greenhouse gas emission [1]. There will be no actual reduction of the emission if the power source is generated from burning fossil fuel instead of generating electricity from renewable energy sources such as wind, sunlight, geothermal, tides and etc. Therefore it is undeniable that the future vehicle will be mostly powered by electric powertrain.

High power electronics driving the powertrain, coupled with high frequency switching devices often produce Electromagnetic Compatibility (EMC) problems and a lot of research have been done to measure the electromagnetic interference (EMI) from the EV correctly [2], in order to reduce the EMI emission from the electronics driving the powertrain.

Other than the electronics driving the powertrain, the Advanced Driver Assistance Systems (ADAS) is also introduced into modern cars. ADAS is equipped with different sensors including radars and cameras to capture surrounding information

of static and dynamic obstacles [3]. Automotive industry utilizes ADAS for most of the safety precaution systems, such as Advanced Emergency Brake System (AEBS), Lane Departure Warning (LDW), Blind Spot Monitoring System (BSMS) and many more. More advanced vehicles are now using ADAS for their autonomous driving system. Most of the electronics system in a modern car can be sighted in Figure 1.1.

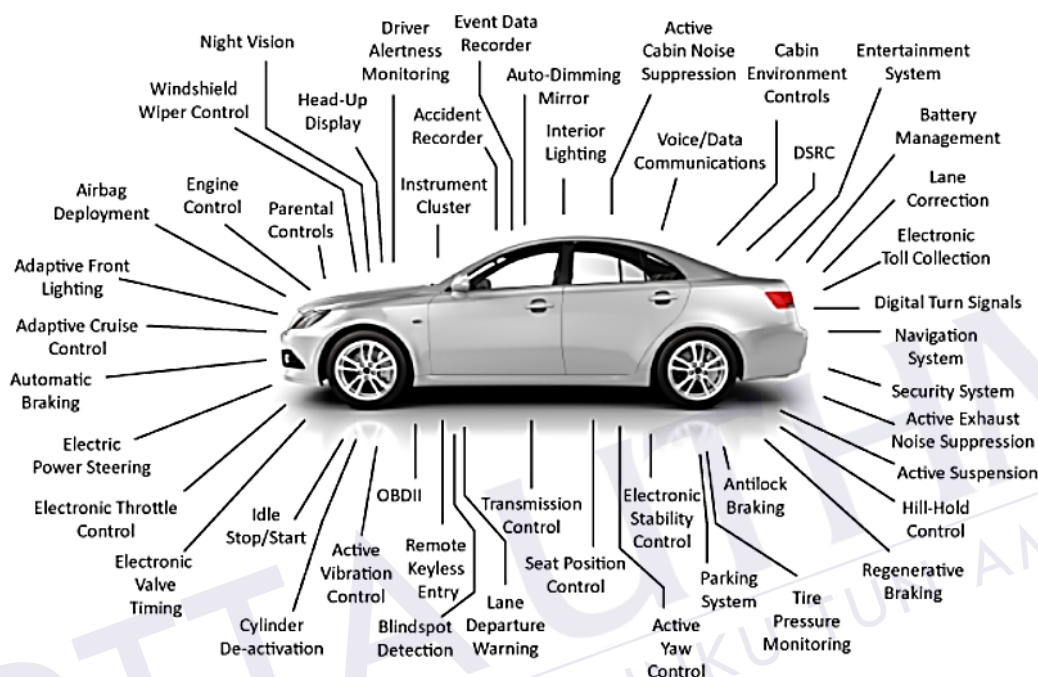


Figure 1.1: Electronics system in a car [4]

ADAS has to be extremely reliable because the safety of the passengers depend heavily on the information processed by ADAS. Some of the ADAS systems are shown in Figure 1.2 where car manufacturers have implemented ADAS to better protect the passenger and to stay competitive in the market. The real-time information collected from the various sensors are processed on a reliable and fast processor to be useful for the ADAS. One of the commonly used sensor for AEBS is a camera sensor. Camera sensors capture and deliver the data, through cables and connectors to the ADAS's Electronic Control Unit (ECU) to be processed by the System On Chip (SOC). The Digital Signal Processor (DSP) is running up to 750 MHz [5] to classify the detected objects into pedestrian, traffic light, vehicles, and other structures. If the ADAS is not functioning as intended, it will not be able to correctly classify objects and hence unable to provide essential information, warnings or automatic intervention to prevent or reduce the severity of the disastrous circumstances.

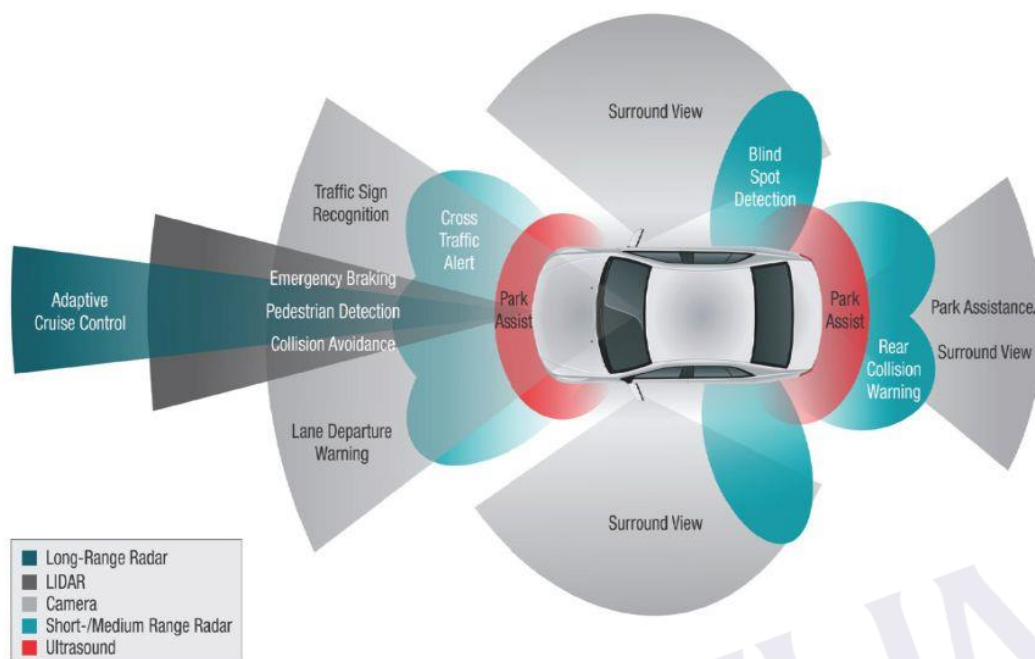


Figure 1.2: ADAS in modern car [6]

Strong attention must be paid to ensure reliable operation of the ADAS. ADAS comprises of complex electronics system where EMC issues must be addressed, among which is the electrostatic discharge (ESD). There are hundreds of microcontrollers in a modern vehicle to monitor every essential operations in the vehicle, such as ignition, braking, acceleration, and power steering. Therefore it is very important to acknowledge that with more electric cars, ESD issue should not be taken lightly. A human body can charge up to 3 kV during exiting and entering the car by tribocharging and this can damage any of the microcontroller by either touching it directly or indirectly [7].

ESD which has similarity to that of a lightning, but at a much smaller scale is often performed in Electromagnetic Compatibility (EMC) testing. However, attention to ESD protection is currently not sufficient because of common misconception that it is unlikely to happen and that most electronics are enclosed inside a metal case which can only offer protection to ESD to some extent. It is also not commercially possible to provide ESD protection measures to every components that are accessible by users, because these ESD protection measures will increase the cost. Current from ESD can penetrate through thin insulating layers and the intense magnetic field resulted from the ESD arc has a frequency range from 1 MHz to 1000 MHz [8]. These fields may

damage components such as the Metal Oxide Silicon Field Effect Transistor (MOSFET) and Complementary Metal Oxide Semiconductor (CMOS) devices.

In today's fast development cycle, board layout changes and ESD protections can add cost to the product and may delay its development schedule [9]. Besides, most of the ESD failure can only be detected at the system level, where mitigation techniques are often impossible. The signal buses such as Controller Area Network (CAN) Bus and Local Interconnect Network (LIN) Bus, are also another important design consideration because shielding of every cables would add additional cost to the vehicle resulting a less competitive price.

1.2 Problem Statement

Recently, the automotive industry has transformed tremendously from mechanical centric to electronics centric. More electronics have been introduced into the car, such as sensors and systems introduced to the drivetrain to ensure comfortable ride handling, and also system to ensure passenger safety. All the electronics has to be controlled by micro-controller and micro-processor with high speed interface and communication link. There are also multiple devices for high speed connectivity such as Bluetooth, Wi-Fi, GPS, and also the upcoming vehicle-to-everything (V2X) application [8-9].

Besides, in order to improve the safety and comfort of the passenger, modern car has also included many safety systems, such as the previously mentioned AEBS, BSMS and etc. These systems such as ADAS is responsible as the safety precaution system. Moreover, to improve passenger's ride comfort and operation easiness, many other systems were included as well, such as active damper system, adaptive cruise control, noise cancelling audio system and etc. [12]. Individual systems are controlled by independent ECUs which are connected by buses to provide central information at the dash board. In summary, there are hundreds of these ECUs within a car working together at the same time sending huge amount of data across very long cables.

Due to the complex system within the car coupled with high speed signals, as well as the digitization of most of the controllers and sensors, EMC issues are inevitable [13]. Many research has been done on the EMC of a car, from infotainment system, to circuit board level, to cabling system [14-15]. Each of the research poses different challenge, as the complexity will greatly increase when more components of

REFERENCES

1. H. Ribberink and E. Entchev, "Electric vehicles - A 'one-size-fits-all' solution for emission reduction from transportation?," *2013 World Electric Vehicle Symposium and Exhibition, EVS 2014*, vol. 1, pp. 1–7, 2014.
2. F. Silva and M. Aragón, "Electromagnetic interferences from electric/hybrid vehicles," *2011 30th URSI General Assembly and Scientific Symposium, URSIGASS 2011*, 2011.
3. J. Khan, "Using ADAS sensors in implementation of novel automotive features for increased safety and guidance," *3rd International Conference on Signal Processing and Integrated Networks, SPIN 2016*, pp. 753–758, 2016.
4. The Clemson University Vehicular Electronics Laboratory, "Automotive Electronic Systems." [Online]. Available: <https://cecas.clemson.edu/cvel/auto/systems/auto-systems.html>. [Accessed: 02-Nov-2020].
5. M. Mody *et al.*, "High Performance Front Camera ADAS Applications on TI's TDA3X Platform," *Proceedings - 22nd IEEE International Conference on High Performance Computing, HiPC 2015*, no. Vd, pp. 456–463, 2016.
6. A. Narayanan, "How Does Advanced Driver Assistance Systems (ADAS) Save Lives and Cars?," 2018. [Online]. Available: <https://www.quest-global.com/advanced-driver-assistance-systems-adassave-lives-cars/>. [Accessed: 02-Nov-2020].
7. P. T. Krein, "Electrostatic discharge issues in electric vehicles," *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1278–1284, 1996.
8. British Standards, "BSI Standards Publication Electromagnetic compatibility (EMC) Part 4-2: Testing and measurement techniques — Electrostatic discharge immunity test," 2009.
9. B. Arndt, F. Zur Nieden, F. Mueller, J. Edenhofer, and S. Frei, "Virtual ESD testing of automotive electronic systems," *2010 Asia-Pacific Symposium on*

- Electromagnetic Compatibility, APEMC 2010*, pp. 683–686, 2010.
10. K. Borgeest, “Practical papers, articles and application notes: EMC aspects of car communication systems,” *IEEE Electromagnetic Compatibility Magazine*, vol. 1, no. 1, pp. 35–41, 2012.
 11. “automotive-electronics-top-5-tech-trends-tomorrows-smart-cars.” [Online]. Available:
<https://www.avnet.com/wps/portal/apac/resources/article/automotive-electronics-top-5-tech-trends-tomorrows-smart-cars/>. [Accessed: 29-Feb-2020].
 12. P. Thoma, “Automotive electronics - a challenge for systems engineering,” *Proceedings - Design, Automation and Test in Europe*, p. 4, 1999.
 13. L. B. Wang, L. Ma, and E. A. Koh, “Analyzing the EMC performance of an automotive display module through 3D electromagnetic simulation,” *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility, EMC/APEMC 2018*, pp. 827–830, 2018.
 14. D. P. Johns and S. Mee, “EMC simulation of an automotive display system,” *2010 Asia-Pacific Symposium on Electromagnetic Compatibility, APEMC 2010*, pp. 904–907, 2010.
 15. M. O’Hara and J. Colebrooke, “Automotive EMC test harnesses: standard lengths and their effect on conducted emissions,” pp. 233-236 Vol.1, 2008.
 16. S. Mee, S. Ranganathan, and R. Taylor, “Effective use of EMC analysis tools in the automotive product development process,” *IEEE International Symposium on Electromagnetic Compatibility*, vol. 3, pp. 744–749, 2005.
 17. A. Englmaier, B. Scholl, R. Weigel, and P. Russer, “EMC modelling strategy for automotive applications,” *1999 29th European Microwave Conference, EuMC 1999*, vol. 2, pp. 317–320, 1999.
 18. G. Braglia, S. Barmada, and A. Duffy, “Simulations and experiments for EMC compliance in automotive environment,” *2016 IEEE/ACES International Conference on Wireless Information Technology, ICWITS 2016 and System and Applied Computational Electromagnetics, ACES 2016 - Proceedings*, vol. 67, pp. 6–7, 2016.
 19. R. Neumayer, A. Stelzer, F. Haslinger, J. Held, F. Schinco, and R. Weigel, “Continuous simulation of system-level automotive EMC problems,” *IEEE International Symposium on Electromagnetic Compatibility*, vol. 1, pp. 409–

- 413, 2003.
20. H. Pues *et al.*, “Translation of automotive module RF immunity test limits into equivalent IC test limits using S-parameter IC models,” *EMC COMPO 2013 Proceedings - 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits*, pp. 249–253, 2013.
 21. A. Durier, C. Marot, and O. Alilou, “Using the EM simulation tools to predict EMC immunity behavior of a automotive electronic board after a component change,” *IEEE International Symposium on Electromagnetic Compatibility*, pp. 57–62, 2013.
 22. T. Li *et al.*, “System-Level Modeling for Transient Electrostatic Discharge Simulation,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 6, pp. 1208–1308, 2015.
 23. N. Monnereau, F. Caignet, N. Nolhier, M. Bafleur, and D. Trémouilles, “Investigation of Modeling System ESD Failure and Probability Using IBIS ESD Models,” vol. 12, no. 4, pp. 599–606, 2012.
 24. M. Park *et al.*, “Measurement and modeling of system-level ESD noise voltages in real mobile products,” *2016 Asia-Pacific International Symposium on Electromagnetic Compatibility, APEMC 2016*, pp. 632–634, 2016.
 25. C. M. Somashekaraiah, “Overview of ESD impacts over Industry Yield,” *2016 International Conference on ElectroMagnetic Interference & Compatibility (INCEMIC)*, pp. 1–4, 2016.
 26. Y. P. Zhou and J. J. Hajjar, “A circuit model of electrostatic discharge generators for ESD and EMC SPICE simulation,” in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits, EDSSC 2014*, 2014, pp. 5–6.
 27. B. Seol, J. Lee, H. Lee, and H. Park, “A circuit model for ESD performance analysis of printed circuit boards,” *Proceedings - 2008 Electrical Design of Advanced Packaging and Systems Symposium, IEEE EDAPS 2008*, pp. 120–123, 2008.
 28. J. Zhang, D. G. Beetner, R. Moseley, S. Herrin, and D. Pommerenke, “Modelling electromagnetic field coupling from an ESD gun to an IC,” *IEEE International Symposium on Electromagnetic Compatibility*, pp. 553–558, 2011.
 29. C. Qing, J. Koo, A. Nandy, and D. Pommerenke, “Advanced full wave ESD generator model for system level coupling simulation,” *IEEE International*

- Symposium on Electromagnetic Compatibility (2008) 2008-January*, pp. 8–13, 2008.
30. R. S. Myoung, B. Seol, and N. Chang, “System-level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation,” *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, vol. November, 2014.
 31. D. Pommerenke, J. Fan, and J. Drewniak, “Simulation challenges in system level electrostatic discharge modeling,” in *2016 IEEE/ACES International Conference on Wireless Information Technology, ICWITS 2016 and System and Applied Computational Electromagnetics, ACES 2016 - Proceedings*, 2016.
 32. S. Caniggia and F. Maradei, “Circuit and numerical modeling of electrostatic discharge generators,” *IEEE Transactions on Industry Applications*, vol. 42, no. 6, pp. 1350–1357, 2006.
 33. F. Centola, D. Pommerenke, W. Kai, T. Van Doren, and S. Caniggia, “ESD excitation model for susceptibility study,” *IEEE International Symposium on Electromagnetic Compatibility*, vol. 1, pp. 58–63, 2003.
 34. T. L. Wu, H. H. Chuang, and T. K. Wang, “Overview of power integrity solutions on package and PCB: Decoupling and EBG isolation,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 346–356, 2010.
 35. C. Warwick and M. Mulligan, “Using behavioral models to drive RF design and verify system performance,” *Microwave Engineering Europe*, 2005. [Online]. Available: https://fr.mathworks.com/content/dam/mathworks/tag-team/Objects/u/26221_91322v00_Using_Behavior_Models_to_Drive_RD.pdf. [Accessed: 28-Apr-2020].
 36. C. C. Huang, H. H. Hsu, and G. C. Guu, “CMOS device de-embedding without impedance standard substrate calibration for on-wafer scattering parameter measurements,” *Asia-Pacific Microwave Conference Proceedings, APMC*, no. 1, pp. 959–961, 2012.
 37. M. Wojnowski, G. Sommer, A. Klumpp, and W. Weber, “Electrical Characterization of 3D Interconnection Structures up to Millimeter Wave Frequencies,” in *2008 10th Electronics Packaging Technology Conference*, 2009, pp. 1393–1402.
 38. Z. Wang, C. Zhou, T. Liu, S. Zhao, and Z. Liang, “Nonlinear Behavior

- Immunity Modeling of an LDO Voltage Regulator under Conducted EMI,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 58, no. 4, pp. 1016–1024, 2016.
39. H. Hettrich and M. Moller, “Design considerations for a 11.3 Gbit/s SiGe bipolar driver array with a 5×6 Vpp chip-to-chip bondwire output to an MZM PIC,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2006–2014, 2016.
 40. N. L. Whyman, “Modelling RF interference effects in Integrated Circuits,” *2001 IEEE EMC International Symposium*, vol. 2, pp. 1203–1208, 2001.
 41. I. Scott, V. Kumar, C. Christopoulos, D. W. P. Thomas, S. Greedy, and P. Sewell, “Integration of behavioral models in the full-field TLM method,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 2, pp. 359–366, 2012.
 42. U. Schaper and B. Holzapfl, “Analytical Parameter Extraction of the HBT Equivalent Circuit with T-Like Topology from Measured S-Parameters,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 3, pp. 493–498, 1995.
 43. P. Pulici *et al.*, “A modified IBIS model aimed at signal integrity analysis of systems in package,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 7, pp. 1921–1928, 2008.
 44. M. O. Sullivan *et al.*, “Guideline for Characterization of Integrated Circuits,” *Automotive Electronics Council*, 2013. [Online]. Available: http://www.aecouncil.com/Documents/AEC_Q003A.pdf. [Accessed: 18-Jun-2019].
 45. J. Teza, “Device Characterization: A key to IC design and test,” *EE Times*. [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1225176. [Accessed: 03-Nov-2020].
 46. R. L. Pritchard, “Transistor equivalent circuits,” *Proceedings of the IEEE*, vol. 86, no. 1, pp. 150–162, 1998.
 47. M. F. Caggiano, J. Ou, S. Bulumulla, and D. Lischner, “RF electrical measurements of fine pitch BGA packages,” *IEEE Transactions on Components and Packaging Technologies*, vol. 24, no. 2, pp. 233–239, 2001.
 48. E. McGibney and J. Barrett, “An overview of electrical characterization techniques and theory for IC packages and interconnects,” *IEEE Transactions on Advanced Packaging*, vol. 29, no. 1, pp. 131–139, 2006.

49. J. Jeong, "Electrical characterization of ball grid array packages from S-parameter measurements below 500 MHz," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, pp. 343–347, 1999.
50. T. S. Horng, A. Tseng, H. H. Huang, S. M. Wu, and J. J. Lee, "Comparison of advanced measurement and modeling techniques for electrical characterization of ball grid array packages," *Proceedings - Electronic Components and Technology Conference*, vol. Part F1334, pp. 1464–1471, 1998.
51. J. C. Tippet and R. A. Speciale, "A Rigorous Technique for Measuring the Scattering Matrix of a Multiport Device with a 2-Port Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 3, pp. 286–287, 1985.
52. D. G. Kam and J. Kim, "Multiport measurement method using a two-port network analyzer with remaining ports unterminated," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 9, pp. 694–696, 2007.
53. I. Rolfes and B. Schick, "Multiport method for the measurement of the scattering parameters of N-ports," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 6, pp. 1990–1996, 2005.
54. A. El Fellahi *et al.*, "Integrated MEMS RF Probe for SEM Station-Pad Size and Parasitic Capacitance Reduction," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 10, pp. 693–695, 2015.
55. B. D. Gonzalez, M. F. Bauwens, C. Zhang, A. W. Lichtenberger, N. S. Barker, and R. M. Weikle, "A 0-40 GHz On-Wafer Probe with Replaceable Micromachined Silicon Tip," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 2, pp. 110–112, 2016.
56. T. Probst, R. Doerner, M. Ohlrogge, R. Lozar, and U. Arz, "110 GHz on-wafer measurement comparison on alumina substrate," in *2017 90th ARFTG Microwave Measurement Conference*, 2018, vol. January, pp. 1–4.
57. R. Sakamaki and M. Horibe, "Proposal of a Precision Probe-Tilt Adjustment with the RF Signal Detection Technique," *CPEM 2018 - Conference on Precision Electromagnetic Measurements*, vol. 1, pp. 1–2, 2018.
58. F. T. Von Kleist-Retzow, O. C. Haenssler, and S. Fatikow, "Simulation of probe misalignment effects during RF on-wafer probing," in *International Conference on Infrared, Millimeter, and Terahertz Waves, IRMMW-THz*, 2016, vol. November, pp. 1–2.

59. S. Lee and A. Gopinath, "New Circuit Model for Rf Probe Pads and Interconnections for the Extraction of Hbt Equivalent Circuits," *IEEE Electron Device Letters*, vol. 12, no. 10, pp. 521–523, 1991.
60. J. E. Schutt-Ainé *et al.*, "Comparative study of convolution and order reduction techniques for blackbox macromodeling using scattering parameters," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 10, pp. 1642–1650, 2011.
61. S. H. Min and M. Swaminathan, "Efficient construction of two-port passive macromodels for resonant networks," *IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, no. 1, pp. 229–232, 2001.
62. R. Neumayer, A. Stelzer, F. Haslinger, and R. Weigel, "On the synthesis of equivalent-circuit models for multiports characterized by frequency-dependent parameters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2789–2796, 2002.
63. A. Chinae *et al.*, "Signal integrity verification of multichip links using passive channel macromodels," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 6, pp. 920–933, 2011.
64. B. Gustavsen and A. Semlyen, "Fast passivity assessment for S-parameter rational models via a half-size test matrix," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 12, pp. 2701–2708, 2008.
65. A. Odabasioglu, M. Celik, and L. T. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, no. 8, pp. 645–654, 1998.
66. B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *Journal of Approximation Theory*, vol. 21, no. 2, pp. 117–125, 1977.
67. B. Gustavsen, "The Vector Fitting Website." [Online]. Available: <https://www.sintef.no/projectweb/vectorfitting/>. [Accessed: 03-Nov-2020].
68. D. Deschrijver, B. Gustavsen, and T. Dhaene, "Computer code for fast macromodeling of large multiport systems," *Electrical Performance of Electronic Packaging, EPEP*, pp. 299–302, 2008.
69. Q. Yu, J. M. L. Wang, and E. S. Kuh, "Passive multipoint moment matching model order reduction algorithm on multiport distributed interconnect

- networks,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 1, pp. 140–160, 1999.
70. D. Deschrijver, B. Gustavsen, and T. Dhaene, “Advancements in iterative methods for rational approximation in the frequency domain,” *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1633–1642, 2007.
 71. D. Deschrijver, M. Mrozowski, T. Dhaene, and D. De Zutter, “Macromodeling of Multiport Systems using a Fast Implementation of the Vector Fitting Method,” *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 9, p. 602, 2009.
 72. Y. S. Mekonnen and J. E. Schutt-Ainé, “Fast broadband macromodeling technique of sampled time/frequency data using z-domain vector-fitting method,” *Proceedings - Electronic Components and Technology Conference*, pp. 1231–1235, 2008.
 73. D. Deschrijver, B. Haegeman, and T. Dhaene, “Orthonormal vector fitting: A robust macromodeling tool for rational approximation of frequency domain responses,” *IEEE Transactions on Advanced Packaging*, vol. 30, no. 2, pp. 216–225, 2007.
 74. B. Gustavsen, “Improving the pole relocating properties of vector fitting,” *2006 IEEE Power Engineering Society General Meeting, PES*, vol. 21, no. 3, pp. 1587–1592, 2006.
 75. Y. S. Mekonnen and J. E. Schutt-Ainé, “Broadband macromodeling of sampled frequency data using z-domain vector-fitting method,” *Proceedings - 11th IEEE Workshop on Signal Propagation on Interconnects, SPI 2007*, no. 1, pp. 45–48, 2007.
 76. P. Triverio, S. Grivet-Talocia, M. S. Nakhla, F. G. Canavero, and R. Achar, “Stability, causality, and passivity in electrical interconnect models,” *IEEE Transactions on Advanced Packaging*, vol. 30, no. 4, pp. 795–808, 2007.
 77. S. Grivet-Talocia and A. Ubolli, “Passivity enforcement with relative error control,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 11, pp. 2374–2382, 2007.
 78. S. Grivet-Talocia and A. Ubolli, “On the generation of large passive macromodels for complex interconnect structures,” *IEEE Transactions on Advanced Packaging*, vol. 29, no. 1, pp. 39–54, 2006.
 79. Z. Mahmood, S. Grivet-Talocia, A. Chinea, G. C. Calafiore, and L. Daniel, “Efficient localization methods for passivity enforcement of linear dynamical

- models,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 9, pp. 1328–1341, 2014.
80. P. Triverio and S. Grivet-Talocia, “Robust causality characterization via generalized dispersion relations,” *IEEE Transactions on Advanced Packaging*, vol. 31, no. 3, pp. 579–593, 2008.
 81. Dassault Systemes, “IdEM - Electronic Device Characterization.” [Online]. Available: <https://www.3ds.com/products-services/simulia/products/idem/>. [Accessed: 04-Nov-2020].
 82. Dassault Systemes, “CST Studio Suite - Electromagnetic Field Simulation Software.” [Online]. Available: <https://www.3ds.com/products-services/simulia/products/cst-studio-suite/>. [Accessed: 04-Nov-2020].
 83. S. Grivet-Talocia, I. S. Stievano, I. A. Maio, and F. Canavero, “Time-domain and frequency-domain macromodeling: Application to package structures,” *IEEE International Symposium on Electromagnetic Compatibility*, vol. 2, pp. 570–574, 2003.
 84. A. Chinea, S. Grivet-Talocia, S. B. Olivadese, and L. Gobbato, “High-performance passive macromodeling algorithms for parallel computing platforms,” *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 7, pp. 1188–1203, 2013.
 85. V. Jandhyala *et al.*, “electromagnetic modeling and electromagnetic-circuit co-simulation oof mixed-signal systems-on-chip,” pp. 3281–3284.
 86. K. Yoshikawa and T. Oshikata, “Performance Evaluation of Electromagnetic and Circuit Co-Simulation for LLC DC-DC Converter,” *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*, pp. 4386–4391, 2018.
 87. A. C. Scogna and L. K. Teoh, “SIPI co-extraction and SPICE co-simulation for package on-die decap optimization,” *2016 IEEE 20th Workshop on Signal and Power Integrity, SPI 2016 - Proceedings*, pp. 1–4, 2016.
 88. A. Bhargava *et al.*, “EMI prediction in switched power supplies by full-wave and non-linear circuit co-simulation,” *IEEE International Symposium on Electromagnetic Compatibility*, pp. 41–46, 2009.
 89. S. Wane and G. Boguszewski, “Global digital-analog co-simulation methodology for power and signal integrity aware design and analysis,” in *2008 European Microwave Integrated Circuit Conference, EuMIC 2008*, 2008, pp. 450–453.

90. S. Wane and D. Bajon, "Partition-recomposition methodology for accurate electromagnetic analysis of SiP passive circuitry," *EUROCON 2007 - The International Conference on Computer as a Tool*, pp. 15–23, 2007.
91. S. Wane, "Partition and global methodologies for IC, package and board co-simulation in SiP applications," in *Proceedings of the 37th European Microwave Conference, EUMC*, 2007, pp. 1249–1252.
92. J. Mao, G. Fitzgerald, A. Y. Kuo, and S. Wane, "Coupled analysis of quasi-static and full-wave solution towards IC, package and board co-design," *IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, no. 100, pp. 111–114, 2007.
93. A. Scott and V. Sokol, "True transient 3D EM/circuit co-simulation using CST studio suite," *Microwave Product Digest*, 2008. [Online]. Available: http://www.euointech.ru/products/CST/CST_MPD_Oct_2008.pdf. [Accessed: 04-Nov-2020].
94. G. A. E. Vandenbosch and A. Vasylychenko, "A Practical Guide to 3D Electromagnetic Software Tools," *Microstrip Antennas*, no. 1, pp. 23–38, 2012.
95. J. A. Narud and C. S. Meyer, "Characterization of Integrated Logic Circuits," *Proceedings of the IEEE*, vol. 52, no. 12, pp. 1551–1564, 1964.
96. F. Overney and B. Jeanneret, "Impedance simulator for automatic calibration of LCR meters over the entire complex plan," *CPEM Digest (Conference on Precision Electromagnetic Measurements)*, pp. 684–685, 2012.
97. J. Nicolas, A. Van Theemsche, and S. A. Awan., "Verification of LCR meters by means of a 4TP 100 Ω linearity test standard over the frequency range 100 Hz to 1 MHz," in *CPEM Digest (Conference on Precision Electromagnetic Measurements)*, 2010, pp. 374–375.
98. A. Pokatilov, A. Satrapinski, T. Kübarsepp, and O. Märten, "Verification of performance of commercial LCR meters," *CPEM Digest (Conference on Precision Electromagnetic Measurements)*, pp. 408–409, 2010.
99. S. Singh, S. Kumar, Babita, and T. John, "Realization of Four-Terminal-Pair Capacitors as Reference Standards of Impedance at High Frequency Using Impedance-Matrix Method," *IEEE Transactions on Instrumentation and Measurement*, vol. 66, no. 8, pp. 2129–2135, 2017.
100. D. Johns, I. Munteanu, and T. Weiland, "Efficient computer simulation of EMC problems with time domain algorithms," *Proceedings of the 2012 ESA*

Workshop on Aerospace EMC 2012, vol. 3, no. 1, 2012.

101. T. Jamneala, P. D. Bradley, and D. A. Feld, "Employing a Ground Model to Accurately Characterize Electronic Devices Measured With GSG Probes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 2, pp. 640–645, 2004.
102. P. F. Freidl *et al.*, "Design of PCB RF probe landing pads for measurements up to 90 GHz," *2016 10th European Conference on Antennas and Propagation, EuCAP 2016*, pp. 15–18, 2016.
103. STMicroelectronics, "USBUF - 2-line EMI filter and ESD protection with R pull-up, for USB interfaces." [Online]. Available: <https://www.st.com/en/emi-filtering-and-signal-conditioning/usbuf.html>. [Accessed: 26-Mar-2020].
104. Texas Instruments, "TFP410 TI PanelBus™ Digital Transmitter," 2014. [Online]. Available: [https://www.ti.com/product/TFP410#:~:text=The TFP410 device combines PanelBus,high-speed digital interface solution](https://www.ti.com/product/TFP410#:~:text=The TFP410 device combines PanelBus,high-speed digital interface solution.). [Accessed: 29-Mar-2020].
105. D. Xu, C. Yang, and W. Gui, "Pinning control of the nearest-neighbor coupled networks based on topology structure," in *Proceedings of the 8th World Congress on Intelligent Control and Automation (WCICA)*, 2010, pp. 3040–3045.
106. D3 Engineering, "TDA3x Automotive Starter Kit," 2018. [Online]. Available: <https://www.d3engineering.com/product/designcore-tda3x-automotive-starter-kit/>. [Accessed: 06-Nov-2020].



APPENDIX A

LIST OF PUBLICATIONS

1. Lik Suong, Ding (2018). “An investigation of experimentally measured S-Parameter as a useful means for impedance characterization of PCB circuitry”, ICESE 2018. 27 August 2018. Submission ID: 3086-6197-1-RV
2. Lik Suong, Ding (2020). “Integrated Circuit Characterisation using Low-cost Coaxial Probe Measurement”, Lecture Notes in Electrical Engineering, vol. 741 LNEE. pp. 61–71, 2021.
3. Lik Suong, Ding (2020). “A More Efficient and Accurate Approach to Characterise an IC into Macro Model”, Lecture Notes in Electrical Engineering, vol. 741 LNEE. pp. 73–85, 2021.



PERPUSTAKAAN UNIVERSITAS TUNJUNG AMINAH

APPENDIX B

VITA

The author was born in February 24, 1991, in Penang, Malaysia. He went to SMJK (C) Chung Ling Butterworth, Butterworth, Penang, Malaysia for his secondary school. He pursued his diploma in Mechatronics at Tunku Abdul Rahman College and his degree at the Manchester Metropolitan University, England, and graduated with the B.Eng. (Hons) in Automation and Control in 2012. Upon graduation, he worked as a design engineer at a jig and fixture company supplying equipment to factories in Penang. Then he pursued his interest in electromagnetic by working as a sales and application engineer in RF Station Sdn. Bhd. While working as an engineer, he admitted into the Ph.D. program in Electrical Engineering at Universiti Tun Hussein Onn Malaysia in 2016. Mr. Ding has authored three papers in area of Electromagnetic Compatibility (EMC).

