FABRICATION, CHARACTERIZATION AND OPTIMIZATION OF IN-HOUSE MOSFET TRANSISTOR USING SPIN ON DOPANT TECHNIQUE

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PERPUSTAKAAN TUNKU TUN AMINAH

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To Mak and Ayah; for your love and support
My bros and sis, together we fight and reach the top
And for me...one step closer to hit

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ABSTRACT

This thesis explains the development and fabrication of first in-house MOSFET device using spin –on dopant technique at KUKUM Microfabrication Cleanroom. The process started with the establishment of process flow, process modules, and process parameters. Four modules were developed. The characteristics prior to the MOSFET device fabrication namely dry and wet oxidation, etching, resist thickness, exposure dose optimization, n-type and p-type spin on dopant and diffusion and also metal thickness characterization were recorded. The data were analyzed and applied in the fabrication of MOSFET devices. The MOSFET fabrication process used blanket-field oxide for isolation, positive resist for lithography process, Boron and Phosphorus for source/drain doping and aluminum for metallization. The whole MOSFET process had four masking process specifically source/drain masking, gate masking, contact masking, and metal masking. The result for each processes are presented in this thesis.

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ABSTRAK

Tesis ini menerangkan mengenai pembangunan modul dan proses fabrikasi peranti MOSFET yang pertama dibina menggunakan teknik "spin –on dopant" di Bilik Bersih, Makmal Mikrofabrikasi, KUKUM. Proses ini bermula dengan membangunkan aliran proses fabrikasi, modul proses and mengenalpasti paramater- parameter yang terlibat. Empat modul telah dibangunkan sebelum proses fabrikasi peranti MOSFET iaitu pengoksidaan basah dan kering serta punaran, ketebalan rintang foto dan pengoptimuman dos dedahan, resapan jenis n dan jenis p serta penglogaman. Setiap data dianalisa dan hasilnya digunakan di dalam proses fabrikasi MOSFET. Proses fabrikasi MOSFET menggunakan pengoksidaan selimut - medan untuk pengasingan transistor, rintang foto positif bagi proses lithografi, boron dan fosforan sebagai dopan untuk proses resapan dan aluminum bagi proses penglogaman. Keseluruhan proses ini melibatkan empat jenis topeng ; topeng telaga (salir dan sumber), topeng get, topeng tingkap sentuhan dan topeng logam. Hasil bagi setiap proses dinyatakan di dalam tesis ini.

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LIST OF SYMBOL

a	Lattice parameter
A	Constant in oxidation law
Å	Symbol for 10^{-10}cm or 10^{-8}m
B	Constant in oxidation law
β	Linear gain
C	Capacitance per unit area
C_{ox}	Oxide capacitance per unit area
D	A dopant (chemical equation only)
D	Diffusion coefficient
g_m	Transconductance
h	Planck's constant
I	Current
I_B	Body current
I_D	Drain current
I_G	Gate current
I_S	Source current
j	Flux
k	Boltzmann's constant
k	Segregation coefficient
l	A length
m	Mass
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

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NMOS	N- Channel Metal Oxide Semiconductor
PMOS	P- Channel Metal Oxide Semiconductor
q	Charge on the electron
Q	Charge per unit area
t	Time
t_{ox}	Oxide thickness
V_B	Body voltage
V_D	Drain voltage
V_{DS}	Drain – Source Voltage
V_G	Gate voltage
V_{GS}	Gate-Source Voltage
V_{TH}	Threshold voltage
W	Work function of metal
x_i	Initial oxide thickness
x_j	Junction depth
x_o	Thickness of oxide film
X	Property of material
ε	Permittivity
ε_o	Permittivity of free space
ε_{ox}	Permittivity of silicon dioxide
μ	Mobility
μ_n	Electron mobility
μ_p	Hole mobility
ρ	Charge distribution
ρ	Resistivity
ρ_s	Sheet resistivity
R_s	Sheet resistance
Ω	Symbol for ohms

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CHAPTER I

PROJECT OVERVIEW

1.1 Overview

This chapter will explain the project overview including objective, scopes, and methodology of project.

1.2 Introduction

The rise of MOS technology is a classic study since it is the most important devices in electronic industry [1] due to its capability. This project is stressed on the fabrication, characterization, and optimization of in-house MOSFET devices. In order to fabricate the devices, the process module development was established and formed backbone of this project.

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The development of the first transistor in 1947 was the start of the microelectronics evolution. The first transistor was the first semiconductor device that made in Bell Laboratory by two scientists, John Bardeen and Walter Brittain and also William Shockley as their supervisor [2, 3] as shown in Figure 1.1. Even though it was not until about the mid-1950s that suitable discrete devices became available for use in industrial equipments.

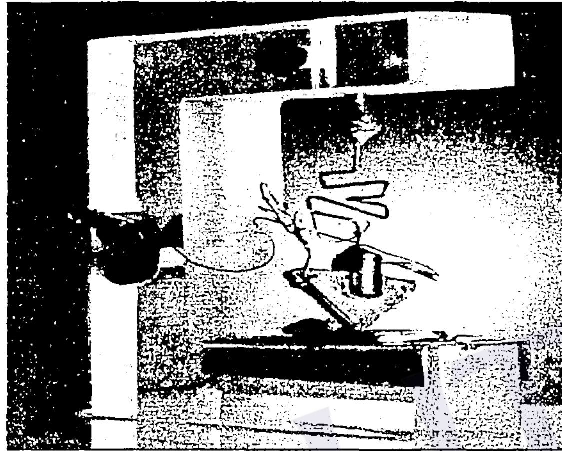

Figure 1.1: The first transistor made by germanium was demonstrated on Dec. 23, 1947, at Bell Labs [3,4].

Early commercial devices were germanium junction transistors, where the collector and emitter regions were diffused from opposite sides into the base region to form the pnp or npn construction. Although germanium has a higher electron and hole mobility than silicon (0.39 and 0.19 m^2 V^{-1} s^{-1}), respectively, for germanium compared with 0.14 and 0.05 m^2 V^{-1} s^{-1} for silicon, thus making it easier to achieve high frequency performance, the poorer temperature characteristics and the inability to protect the critical transistor perimeters (the 'metallurgical junctions') of germanium meant that silicon would become the dominant microelectronic technology from the 1960s onward [5, 8].

The gradual dominance of silicon technology was principally due to the development of planar fabrication, whereby all the fabrication steps were made on one

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surface (plane) of the silicon wafer silicon dioxide providing the key to the protection of the metallurgical junctions as well as providing good isolation between areas where required. Silicon was initially more difficult to process than germanium, which accounted in part for germanium being the first commercially used technology. Since the 1960s the history of silicon technology has been one of continuous and rapid evolution based upon planar techniques.

The starting point of fabrication remains the growing of pure silicon, which has increased from the original pulled-crystal capability which gave wafers of only 10 mm (2/5 inch) in the 1960s to the present wafer size of 300 mm (12 inches) [4,5]. Crystal defects and discontinuities in the silicon which affect the subsequent manufacture of fault-free circuits have also been reduced, and consistency of processing across the whole wafer area, which is vital for good yield, has also been improved [5].

Since the silicon area required for transistors was less than that required for resistors and capacitors, the impact of this evolution on electronic circuit design has been to encourage the use of active rather than passive devices.

The main technologies which have been continuously developed over this period are of course bipolar transistor (BJT) and unipolar transistor (Field Effect Transistor or FET). The FET was then divided into two groups which are JFET (Junction Filed Effect Transistor) and MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

Much of the work leading to the invention of the bipolar transistor involved studies of the effect an applied electric field had on the conductivity of semiconductors. Shockley proposed the junction filed effect transistor (JFET) in 1951, but early attempts at fabrication failed because a stable surface could not be obtained. This difficulty was overcome with the introduction of the planar process and silicon dioxide (SiO_2) passivation. In 1958, the first JFET was produced by Teszner in France. [6]

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The techniques used to make reliable JFETs led to an even more important device, the metal – oxide- semiconductor field - effect transistor (MOSFET). The structure consists of a metallic electrode (the gate) placed on the SiO_2 between two electrodes in the semiconductor (source and drain). The current in the 'channel' between source and drain can be controlled by applying an appropriate voltage between the gate and the semiconductor. Atalla and Kahng (1960) at Bell Laboratories reported the first such device [1].

The use of MOSFETs was immediately attractive because very high component densities are obtainable. Originally, reliable fabrication employed p-channel MOSFET (PMOS) devices – that is, MOSFETs whose operation depended on holes flow. PMOS transistors firstly made at 1960s [4, 6]. Improved fabrication methods led to the use of n – channel metal – oxide –semiconductor (NMOS) devices. This technology was introduced in the mid 1970s [4, 6]. The conductions in these transistors were done by electrons movement and result in higher speed performance. This transistor used ion implantation instead of diffusion technique which applied on PMOS technology. The fabrication process of PMOS using 1960s technology and NMOS with 1970s technology are attached in Appendix A. Presently, NMOS technology is predominant.

The complementary metal oxide semiconductor (CMOS), a circuit configuration employing both p – channel metal oxide semiconductor (PMOS) and n - channel metal oxide semiconductor (NMOS) devices, was first applied in digital watches because of its extremely low power consumption. Recent advances including the use of polysilicon gates and reduction in device size have made CMOS circuits a major digital technology of the 1980s [4]. However, the rapid growth of MOSFET technology gave another implication to the devices such as latch up, hot electron effect and electrostatic discharge (ESD) [6, 7]. But, this reliability implication will not be covered in this project.

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1.3 Problem Aspire

Since the semiconductor industry growth rapidly, competition among companies to fulfill market demands is becoming increasingly intense. Therefore, many data and parameters obtained from researches were not published and kept as a confidential.

Hence, each fabrication laboratories must build their own technologies. The purpose of this project is to build a first MOSFET technology using Micro Fabrication Cleanroom at KUKUM.

Besides, the production of semiconductor is a challenging technological process. The success of operation management and production control technique is critically dependent upon the availability and performance of highly sophisticated, very expensive process equipment.

Manufacturing semiconductors, also called integrated circuits or chips, requires using repetitive sequences of similar processing operations such as photolithography, etch, deposition, diffusion, ion implant, and metallization. The difficulty of doing fabrication process will be taken as a challenge in this project.

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1.4 Objective

Objective of this project are:

1. To optimize and characterize the process parameter and process flow of the MOSFET device.

2. To produce a recipe of MOSFET devices (both NMOS and PMOS transistor).

3. To produce in-house MOSFET device using spin-on dopant technique.

1.5 Project Scope

There are 4 steps that will be done in this project which are :

1. Establishing process module, process parameters, process flow and process run card.

2. Optimizing and characterizing process module.

3. Integrating the process module and starting the fabrication process of MOSFET devices.

4. Analyzing and testing the product.

1.6 Project Workflow

The project flows chart is depicted in Figure 1.2.

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