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Hardware Demonstration of Precoded Communications in Multi-Beam UHTS Systems

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Abstract: In this paper, we present a hardware test-bed to demonstrate closed-loop precoded communications for interference mitigation in the forward link of the multi-beam ultra-high throughput satellite systems. The hardware demonstrator is a full-chain closed-loop communication system with a multi-beam DVB-S2X compliant gateway, a satellite payload and MIMO channel emulator and a set of DVB-S2X user terminals with real-time CSI estimation and feedback. We experimentally show the feasibility of Precoding implementation in satellite communications based on the superframe structure DVB-S2X standard. Using the test-bed we have a possibility to run real-time precoded DVB-S2X communication and benchmark its performance under realistic environment. The hardware demonstrator is suitable to perform realistic benchmarks of Block- and Symbol-level Precoding techniques for multicast and unicast user scheduling scenarios.

1 Introduction

The 5th generation of mobile radio communications systems should provide high level of integration and flexibility between different types of telecommunication networks. Terrestrial and satellite systems historically evolved independently of each other, which results in technological diversity between the networks. The launched 5GPPP research program co-funded by the European Commission is set to work towards a definition of new common standards for 5G networks [1]. The objective of the project METIS 2020 as a part of 5GPPP is to build the foundation for a future mobile and wireless communications system for 2020 and beyond [2]. These standards will allow seamless joint operation of mobile cellular communications and satellite systems as a single service. The use cases of modern satellite communications (SATCOM) systems in 5G networks include increasing coverage of conventional terrestrial cells, facilitating caching through multicast/broadcast data transmission and providing off-load backhauling for unicast user traffic [3, 4].

Although many activities focus on the integration of SATCOM into 5G using higher layers e.g. Software-defined networking (SDN), and network functions virtualisation (NFV), the business potential will be limited unless the raw channel capacity of the satellite systems can be increased proportionally to the terrestrial counterparts. Multi-beam satellites can increase their throughput capacity by utilising channel aided precoding [5–8]. Similar techniques are used in industrial standards in VDSL2 [9] and Long Term Evolution (LTE) [10] communications. In SATCOM the DVB-S2X [11] was developed as a precoding enabling standard.

MIMO Precoding techniques are based on closed-loop approach by employing the retrieved Channel state information (CSI) from the User Terminals (UTs), requiring a feedback channel from UT back to Gateway (GW). Accuracy of the CSI estimations, which are affected by imperfections of the transmitter and all the receivers, and relevance due to the time-varying nature of a wireless channel are not perfect in real communications systems. The inability of acquiring instantaneous CSI at the GW for mobile satellite systems can be very challenging and effect the Precoding performance. However, there is potential for specific types of applications such as aeronautical/maritime systems, where the channel is predictable and there is no direct blockage of the line of sight component [12].

MIMO precoding techniques, which are defined as convex optimisation problems, have to be solved by time-consuming iterative convex optimisation (CVX) or Non-negative least squares (NNLS) solving methods that must fit into relevant time frame. Further research is done on the reduction of the processing times to meet channel requirements [12, 13].

On the other hand, the academic research show that Precoding techniques in SATCOM potentially allow more efficient spectral utilisation and substantially higher service availability [14–16]. To enable the efficient utilisation of satellite transponders, multiple carriers have to be relayed through a single HPA. However, the non-linear nature of the HPA results in adjacent channel interference and increased Peak-to-average power-ratio (PARP), which limits the expected performance gains [17, 18]. In this context, studies on energy efficient on-board predistortion techniques, to maximise performance of HPA by uniformly distributing the power load are conducted [19–21].

In this work, we focus on the implementation of the hardware demonstrator for the closed-loop precoded SATCOM. We describe the design and functionality of the multi-beam DVB-S2X compliant GW, the satellite MIMO Channel Emulator and the set of UTs. We validate the design requirements using reasonable software and hardware resources.

We implemented the physical layer of the DVB-S2X standard by means of software defined radio (SDR) techniques using commercial SDR platforms. Developing on SDR allows to rapidly prototype and deploy the precoded transmission in more realistic environment rather than using only numerical simulations. Authors used the same approach in [22, 23] to benchmark a novel Precoding technique using a small-scale hardware test-bed.

Notation: Upper-case and lower-case bold-faced letters are used to denote matrices and column vectors. The superscripts $(\cdot)^H$ and $(\cdot)^{-1}$ represents Hermitian matrix and inverse operations.

2 Hardware Demonstrator

In this paper, we present a hardware test-bed to demonstrate closed-loop precoded communications for interference mitigation in multi-beam ultra-high throughput satellite (UHTS) systems. We build the test-bed to demonstrate real-time precoded communications under realistic environments. For this matter, we designed a scalable architecture of the gateway and UTs compatible with the DVB-S2X superframe structure. The Fig. 1 shows the block diagram of the demonstrator.

We use the commercially available SDR platform developed by National Instruments (NI). The platform consist of two NI PXI

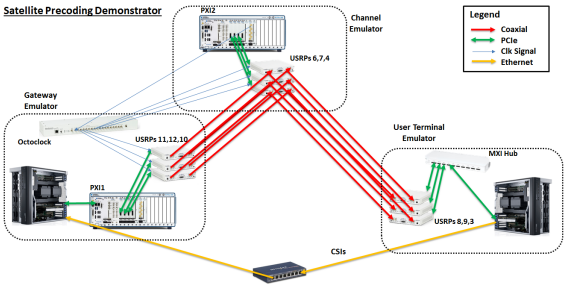

Fig. 1: Block diagram of the Hardware Demonstrator

(PCI EXtension for Instruments) 1085 chassis, which allow centralised connection connection of the set of the NI USRP (Universal Software Radio Peripheral) 2954R and FlexRIO (Reconfigurable IO) 7976R. The NI USRP and FlexRIO have integrated FPGA (Field-Programmable Gate Array) module Kintex-7 from Xilinx.

The gateway simultaneously transmits 6 precoded signals towards 6 user terminals through a 6×6 multi-beam satellite channel emulator. The channel emulator acquires the gateway signals, applies the impairments of the satellite payload, Gaussian noise and the multi-beam interference and transmits the signals to the UTs. The UTs estimate the CSI based on the DVB-S2X standard pilots and report the estimated values to the gateway through a dedicated feedback channel over an Ethernet link. The gateway uses this CSI data to compute a Precoding matrix. The table 1 summaries the current capabilities and the final targets of the demonstrator.

Table 1 Parameters of the hardware demonstrator

Parameter	Current	Target
Gateway IQ channels	6	16
Sampling frequency	1 MHz	80 MHz
Oversampling factor	4	4
Gateway TX freq.	1.21 GHz	-
Channel Emulator RX freq.	1.21 GHz	-
Channel Emulator TX freq.	960 MHz	-
User Terminal RX freq.	960 MHz	-
Filter roll-off factor	0.2, 0.15, 0.1, 0.05	-
Forward Error Correction	no	yes
LDPC code rate	no	1/2, 2/3, 3/4, 5/6

2.1 System Model

We consider a system model, which focuses on the forward link of a multi-beam satellite system. We assume a full frequency reuse scenario, in which all the beams transmit in the same frequency and time. The multi-user interference is mitigated by using the signal Precoding technique. The defined the number of transmitting antenna is equal to the total number of users in the coverage area. In this scenario we consider a 6×6 MIMO channel. In the specified MIMO channel model, the received signal at the i-th terminal is given by $y_i = \mathbf{h}_i^{\dagger} f(\mathbf{x}) + n_i$, where $\mathbf{h}_i^{\dagger}$ is a 1×6 vector representing the complex channel coefficients between the i-th terminal and the 6 antennas of the transmitter, $\mathbf{x}$ is defined as the 6×1 vector of the transmitted symbols of DVB-S2X superframe at a certain symbol period and n_i is the independent complex circular symmetric (c.c.s.) independent identically distributed (i.i.d) zero mean Additive White Gaussian Noise (AWGN) inserted to the i-th terminal's receive signal. The function $f(\mathbf{x})$ represents the non-linear behaviour of the satellite channel.

Looking at the general formulation of the received signal, which includes the whole set of terminals, the signal model is

$$\mathbf{y} = \mathbf{H} f(\mathbf{x}) + \mathbf{n} = \mathbf{H} f(\mathbf{W}\mathbf{s}) + \mathbf{n}, \tag{1}$$

where $\mathbf{y} \in \mathbb{C}^{6\times 1}$, $\mathbf{n} \in \mathbb{C}^{6\times 1}$, $\mathbf{x} \in \mathbb{C}^{6\times 1}$, and $\mathbf{s} \in \mathbb{C}^{6\times 1}$ and $\mathbf{H} \in \mathbb{C}^{6\times 6}$. In this scenario, we define the Block-level Precoding matrix $\mathbf{W} \in \mathbb{C}^{6\times 6}$ as

$$\mathbf{W} = \hat{\mathbf{H}}^H \cdot (\hat{\mathbf{H}} \cdot \hat{\mathbf{H}}^H)^{-1}, \tag{2}$$

where $\hat{\mathbf{H}} \in \mathbb{C}^{6\times 6}$. We consider the data symbols $\mathbf{s}$ to be unit variance complex vectors $|s_k| = 1$ for every $k = 1 \dots 6$.

2.2 Gateway

The gateway operates with a central NI FlexRIO FPGA and 3 NI USRP nodes. The 3 NI USRP nodes connected to the same oscillator reference clock source. A single NI USRP has only 2 RF outputs. In order to transmit 6 independent signals on 6 RF channels simultaneously we need to utilise 3 NI USRP nodes. It is required to have the synchronised frequency and time clocks in all the nodes while performing joint beamforming. The Fig. 2 shows the logical connections between the NI FlexRio, the NI USRP nodes and the controller (NI PXI HOST). Here the upper blue section represent the processes implemented in the host computer and the lower yellow section represents the blocks implemented in the FPGA for fast processing.

The FPGA IP block of the DVB-S2X deployed in the NI FlexRio generates 6 parallel streams of symbols of the DVB-S2X superframe. Each stream carriers terminal specific data. The streams can be independently configured through the dedicated graphical interface as shown on Fig. 3.

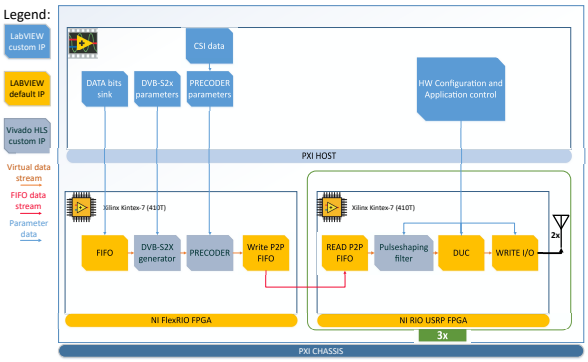

Fig. 2: Block diagram of the DVB-S2X Gateway

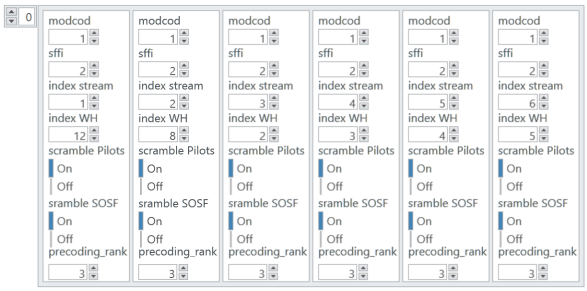

Fig. 3: DVB-S2x Gateway configuration graphical interface

We implemented the configurations, which are covered by the DVB Standards [24, 25], namely: MODulation and CODing Mode (MODCOD), Super-Frame Format Indicator (SFFI), Index Stream, Index of the Walsh-Hadamard (WH) matrix, scramble flag for Pilots

and Start Of Super-Frame (SOSF). We include an extra parameter indicating the Precoding type (). The Precoding type describes the type of the Precoding technique allowed to precode each stream. Rank 0 indicates no Precoding is applied, 1 - Channel based Zero Forcing (ZF) or the Minimal Means Square Error (MMSE) Precodings are used [26], 2 - reserved for the future use, 3 - Symbol-Level Precoding (SLP) techniques [27] are used if possible, otherwise - ZF and MMSE.

The streams are jointly precoded by the PRECODE IP block. The PRECODE IP blocks multiplies 6 symbols from a single time slot with the Precoding matrix $\mathbf{W}$. Additionally, the Precoding Mask controls Precoding behaviour over the segments of the DVB-S2X superframe as illustrated on Fig. 4.

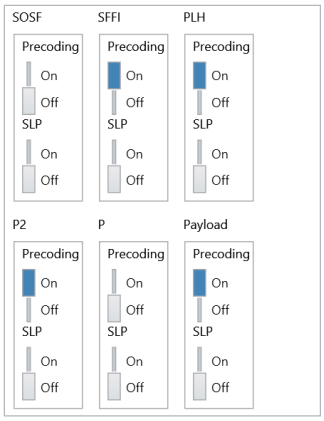

Fig. 4: Precoding configaration for DVB-S2X superframe structure

Through the configuration panel we can enable and disabled Zero-Forcing and SLP Precoding techniques for each segment of the DVB-S2X superframe. We disable Precoding for SOSF and P pilots under normal operation. The SOSF is a known sequence, which can be reliably detected at a user terminal even in high interference environment. The P pilots are not precoded because they are used by UTs to estimate the CSI ($\widehat{\mathbf{H}}$).

The streams with 6 superframes are transferred to the 3 NI USRP nodes, where the signals are oversampled using the Pulshaping filter IP block. The filter's impulse response is given by the Raised-cosine function with different roll-off factors. The roll-off factor of the filter response is configurable according to the DVB-S2X standard. In this iteration of the hardware demonstrator we implemented the roll-off factors of 0.2, 0.15, 0.1 and 0.05. We measured the actual filter's frequency response for these roll-off values as shown on Fig. 5. The oversampled signals are processed by digital up converted (DUC) and transmitted to the RF domain at a desired carrier frequency.

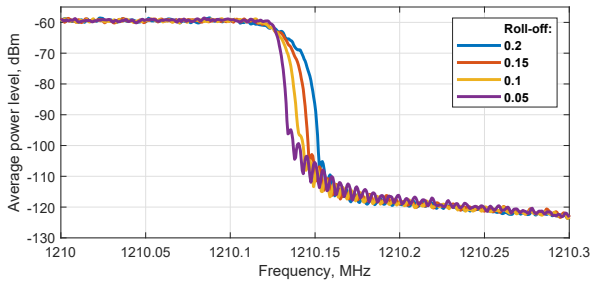

Fig. 5: Frequency characteristics of the transmitted signal

2.3 Channel Emulator

The channel emulator is running on a PXI HOST controller, a NI FlexRIO module for central signal processing and 3 NI USRP nodes for the RF front-end. The nodes are inter-connected as shown on the Fig. 6. Each NI USRP node acquires two streams of the sampled baseband, which are generated by the digital down converter (DDC). Therefore, by utilising 3 synchronised RIO USRP nodes the channel emulator simultaneously samples 6 independent RF baseband streams. The RF inputs and outputs of the NI USRP nodes operate in RF bands of the Low Noise Block (LNB) in the GW and the LNB on the UTs. All the effects that occurs in the actual Ka band are emulated in the channel emulator.

We designed and implemented custom IP blocks into USRP FPGA nodes to emulate the channel impairments in real time. We designed and build an additive white Gaussian noise (AWGN) generator [28] with configurable amplitude. We implemented Input Multiplexing (IMUX) and Output Multiplexing (OMUX) filtering FPGA IP blocks. The input and output characteristics of the filters are shown in Fig. 7.

We developed a custom IP block to emulate Traveling-Wave Tube Amplifier (TWTA) non-linearities. The input and output characteristics of the TWTA IP block correspond to the DVB-S2 standard specifications and are depicted in Fig. 8.

The streams from the 3 USRP nodes are transferred to the FlexRIO FPGA. The channel matrix ($\mathbf{H}$) is jointly applied towards all the streams by the MIMO Channel Emulator IP block. The desired channel matrix is controlled by the PXI HOST. The 6×6 matrix of complex coefficients is based on the realistic satellite beam pattern illustrated on Fig. 9. It is called ESA71 (after the origin and the number of beams). ESA71 makes use of the Ka-band exclusive band 19.7 to 20.2 GHz. We consider a scenario of full frequency reuse, where the same frequency band is applied in every beam. We can simultaneously select up to 6 user terminals in the coverage area and generate realistic channel coefficients.

The resulting signals with added interference are transferred back to the corresponding NI USRP nodes. In every NI USRP node the signal is upsampled in DUC and sent through the RF analogue outputs. The RF inputs and outputs of the channel emulator operate at different carrier frequencies as shown in the Table. 1. Using this configuration we decrease mutual coupling between the transmission and reception links through the RF part of the Channel Emulator to facilitate the accuracy of the designed channel matrix.

2.4 User Terminal

The User Terminals (UT) are the are ground based users which collect the transmitted waveforms and recover the transmitted data bits. The UT are implemented using the same SDR platform used in for the Gateway and the Channel Emulator, the USRP RIO NI2944. We use each of these USRP to implement two independent UTs using the two RF inputs of the device. The FPGA inside the SDR platform performs signal processing for the two UT chains and communicates with the host computer.

Fig. 10 shows an architectural block diagram of the UT implementation. The FPGA interface the RF daughter boards, which down-convert the incoming RF signal using an analog local oscillator. The FPGA reads the ADCs sampled data coming in four sampled streams for the two IQ down-converted pairs. The sampling rate of this particular SDR platform is 200MSPS. After sampling, two DDC blocks take the two IQ sampled streams. Each DDC shifts in frequency the IQ streams using a Numerically Controlled Oscillator, and applies a decimation filter in order to produce a decimated output stream at a selectable sampling rate. The frequency shifting performed in the DDC has the advantage of avoiding the problematic zero-frequency part of the spectrum after analog down-conversion, which usually is corrupted by some leakage of the the local oscillator signal.

After the DDC, the DVB-S2X blocks performs the recovery of the information from the digitally down-converted stream. Fig. 11 shows a simplified functional block diagram of the DVB-S2X Receiver IP block used int the UTs. Due to the efficient FPGA accelerated processing, a single USRP RIO FPGA unit is capable to simultaneously receive two DVB-S2X compliant signals. The DVB-S2X processing chain is capable of recovering the format 2 and 3 super-frames from

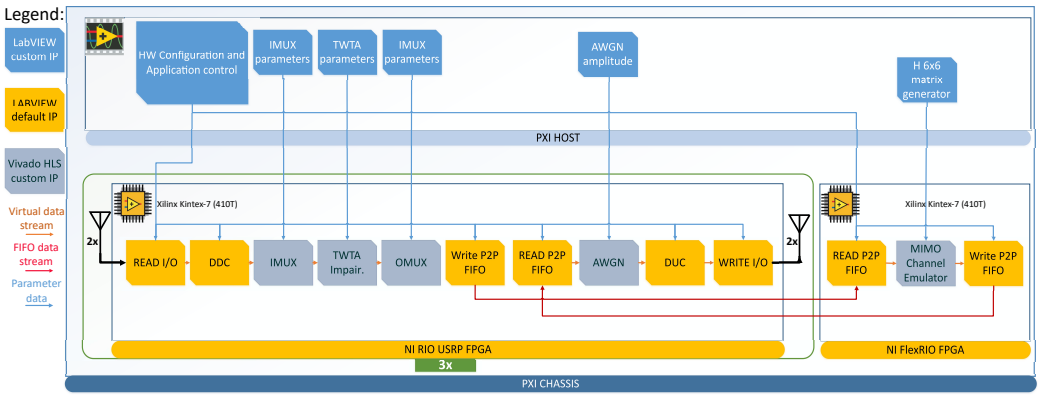

Fig. 6: Block diagram of the channel emulator

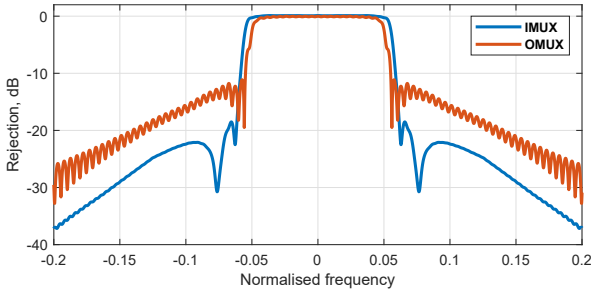

Fig. 7: IMUX and OMUX filter characteristics of the Channel Emulator

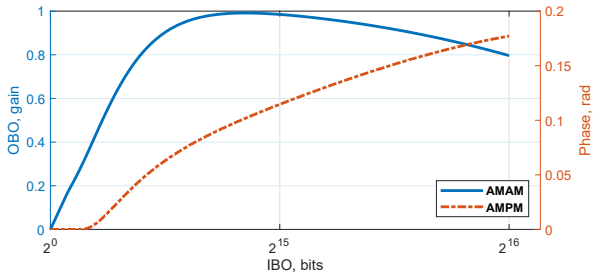

Fig. 8: TWTA AM/AM and AM/PM characteristics of the Channel Emulator

the DVB-S2X standard. These processes include frequency acquisition, matched filtering, time synchronization, frame (including Super-Frame) synchronization, fine phase tracking and CSI estimation. The block labelled Phase Recovery on Fig.11 performs symbol recovery from the input stream with an over-sampling factor of four. The recovered symbols contain the payload data plus the pilot structure of the DVB-S2X framing. All the frame fields and the CSI information are passed to the host computer for their further utilisation. The host computer reports the CSI information to the central Gateway using a custom feedback channel.

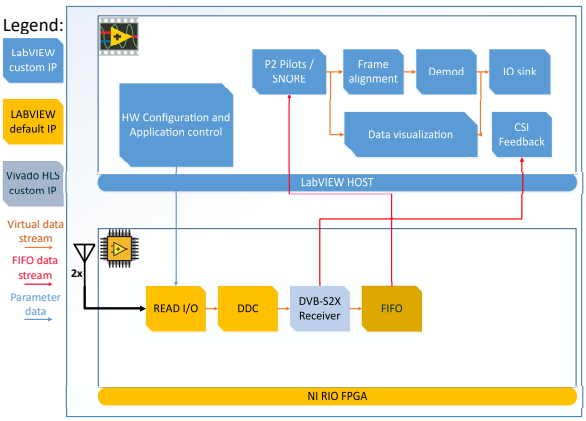

Fig. 10: Architectural block diagram of the User Terminal. Note that two input RF chains are present in a single USRP.

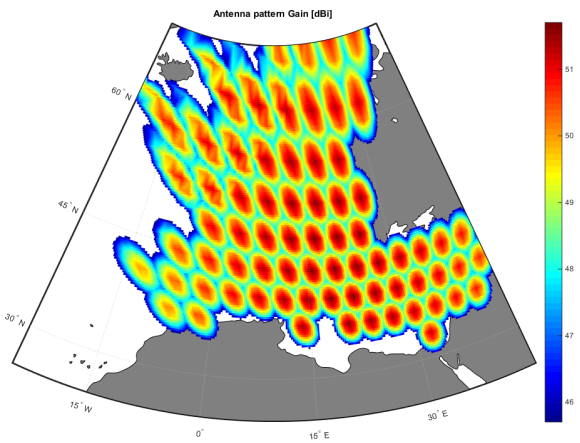

Fig. 9: ESA71 beam pattern, antenna performance

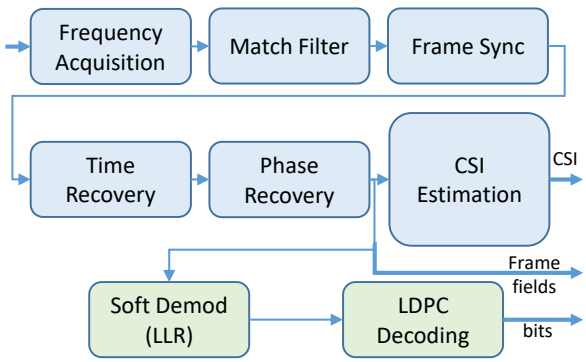

Fig. 11: Functional diagram of the DVB-S2X receiver block in the UT

2.5 Resource Occupation in FPGAs

The described software equipment is heavily based on FPGA code acceleration and parallel computing. The FPGA resources in the used equipment (NI USRP 2954-R and NI FlexRIO 7976R) are limited, thus the design of the functional FPGA blocks is a compromise between the functionality, the resource occupation and the data throughput. The Table 2 is the summary of the actual FPGA resource occupation of each part of the hardware demonstrator. The occupation percentage of the Digital Signal Processors (DSP), Block RAMs (BRAMS), lookup tables (LUT) is manageable for the planned functionality. Hence, we can notice that the Slices (Each slice contains four LUTs and eight flip-flops) occupation is very hight at the user terminal. The complexity of the terminal is much higher than the one with a single receiver. It is evident that if we want to expand the functionality of the terminal we need to deploy only one DVB-S2X receiver per USRP node.

Table 2 FPGA Xilinx Kintex-7 (410TFFG-2) Resource Occupation

	DSP48E	BRAM	LUT	Slices
Gateway node	19%	18%	13%	27%
Gateway FlexRIO	34%	23%	26%	41%
Channel Emu. node	34%	56%	32%	49%
Channel Emu. FlexRio	9%	27%	31%	43%
User Terminal 1 RX	31%	22%	36%	63%
User Terminal 2 RX	40%	23%	57%	83%

3 Conclusion

In this paper we present, to the best author knowledge, the first hardware demonstrator for Precoding in DVB-S2X systems. The hardware demonstrator is a full-chain closed-loop communication system with multi-beam gateway transmitter, MIMO channel emulator and receiver terminals with real-time CSI estimation. With the hardware demonstrator we are able to show experimentally the application of Precoding in satellite communications based on the DVB-S2X standard.

4 Acknowledgments

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