Eighteen-Level Inverter Control with Minimum Switching Losses

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Abstract

A multilevel multistage inverter design and its corresponding control strategy are presented. The hybrid inverter has a high voltage stage composed of the six-switch conventional three phase inverter with its outputs connected in series to the outputs of three-level H-bridge medium and low voltage stages. The voltage ratio has been selected to form 18-level provide maximum number of uniform steps. The suggested control strategy has been developed to ensure minimum switching losses focusing on holding the higher voltage stage state as long as it is feasible. The reference voltage vector has been approximated to the nearest inverter voltage vector. A special definition of state zone has been introduced for the low voltage stage to enable the achievement of the reference vector with minimum error. The proposed control strategy has been tested and its short computational time and low memory requirement has been proven.

Introduction

Multilevel inverters (MLI) have been introduced to enable the construction of inverters of voltage ratings beyond the switching devices capability. Other advantages of this type of inverters are the ability to produce less distorted waveforms and reduced dv/dt. The basic MLI topologies which are the neutral point clamped, flying capacitors and the series connected H-cells enable the construction of inverters with any number of levels theoretically. Due to the increased circuit complexity, number of series connected devices and cost, the number of levels of practical MLIs with the basic topologies is very limited [1].

Modifications have been introduced on the basic topologies. The number of levels of the H-cells symmetrical MLI is linearly proportional to the number of devices. The asymmetrical MLI using different dc input voltages have a number of levels exponentially proportional to the number of devices [2]. The design of the inverter can be further optimized by hybridization, where the MLI is constructed from inverter stages of different types, topologies and/or voltage levels.

It has been shown that when the DC voltages feeding H-bridge cells are related by the ratio of 1:3 the maximum output resolution, i.e. number of levels, can be obtained [3]. The voltage ratio selection rules have been identified in following studies [4], [5] which introduced two conditions for voltage ratios selection; the uniformity of the steps and the modulation condition. The uniformity of the steps is insured if the inverter output voltage levels are evenly spaced. While the modulation condition is satisfied if any two adjacent levels can be achieved by changing the switching state of the lowest voltage inverter only and holding the state of the higher voltage cells. The last condition meant to ensure no high switching frequency at the high voltage stage.

Some studies [6-8] did not consider the condition of the modulation instead the number of levels has been maximized by selecting input voltages of the two or three- stage inverters related by ratio 3. In all these studies, the carrier-based or the space vector PWM control have not been considered, instead selected harmonics elimination [6] or the one switching state per sampling interval [8] has been adopted assuming that the inverter high resolution can ease the need for high frequency PWM control.

The asymmetrical MLI of ratio-3 fed cascaded inverter provides the highest number of levels for a given topology but this design requires high number of isolated DC supplies making DC supply circuit rather complicated, costly and operating with highly reactive current. Also PWM control of this inverter leads to high switching frequency of the high voltage stage [9].

This paper presents a modification of the ratio-3 supplied asymmetrical MLI by replacing the three single-phase H-bridge inverters by a three-phase six switch inverter. This arrangement has been used in the two-stage, 6-level inverter topology presented in [10]. In this paper, novel, one state per sampling interval control algorithm has been developed. The resultant inverter combines the advantages of maximum number of levels and reduced switching losses and the control presented algorithm is based on innovative graphical-based concept.

Inverter Structure, Voltage Vectors and Switching States

The proposed inverter is composed of the "main" high voltage six-switch inverter with each output line connected in series to two cascaded single-phase full bridge inverters as shown in Fig. 1. The main and H-bridge cells are fed by isolated dc sources of a different values related by the ratio 3.

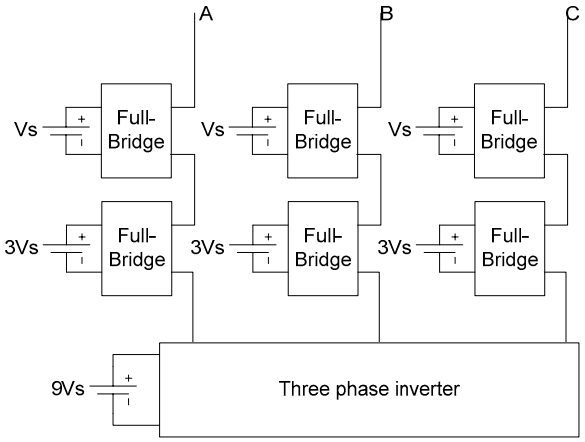

Fig. 1: 18-level inverter topology

The Voltage Vectors and Inverter States

The voltage vectors of the three-stage inverter can be determined graphically by superimposing the vector diagram corresponding to three stages. Fig. 2 shows the voltage vectors corresponding to the high, medium and low voltage stages separately. The full vector diagram can be achieved by positioning vectors corresponding to medium stage at the tip of each of the seven vectors corresponding to high voltage stage. Then, the low voltage vectors are added at the tip of the medium voltage vectors. The resultant vector diagram, with the voltage ratios indicated in Fig.1, is shown in Fig. 3 which shows that ratio-3 sourcing produces uniform step 18-level inverter.

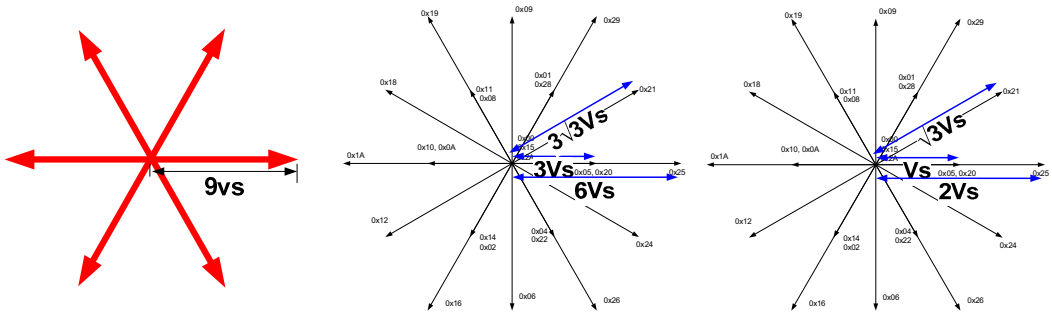

Fig. 2: The voltage vectors corresponding to the high, medium and low voltage stages

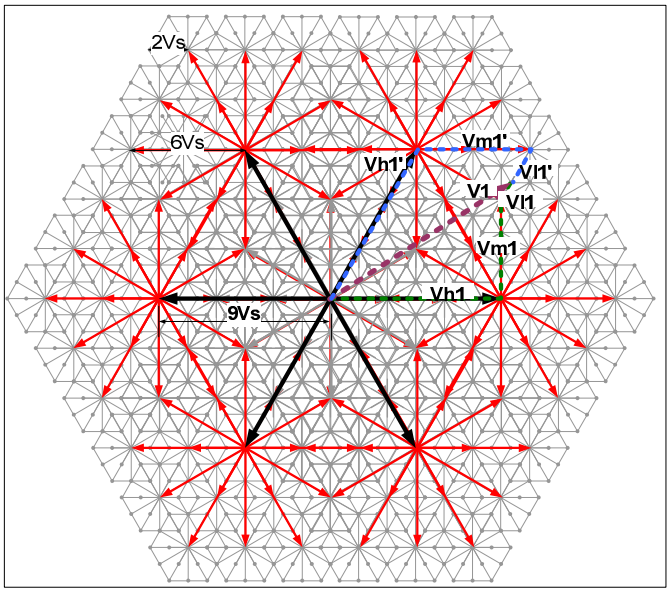

Fig. 3: The voltage vectors of the 18-level inverter as the sum of the three cascaded inverters vectors.

The switching state of the inverter will be denoted by $\{(x_a,x_b,x_c),(y_a,y_b,y_c),(z_a,z_b,z_c)\}$ where x is a binary digit of and y and z are trinary digits. The state of the main inverter is determined by x_{abc} , while y_{abc}, and z_{abc} determine the state of the medium and low voltage stages respectively. The output voltage vector can be represents in terms of the switching state as follows:

$$\begin{bmatrix} v_D \\ v_Q \end{bmatrix} = \frac{V_s}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} v_D \\ v_Q \end{bmatrix} = V_s\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix} \quad (2)$$

The vector corresponding to any inverter state can be determined using equation (2).

High and Medium Voltage Stages Domains

Each of the 919 vectors of the 18-lvel inverter can be represented by the addition of three vectors, one has a norm of 9Vs (or zero) determined by the switching variables x_{abc} , the second has a norm of 6, $3\sqrt{3}$, 3 or 0Vs determined by y_{abc}, and the third has a norm of 2, $\sqrt{3}$, 1 or Vs determined by z_{abc}. Fig. 3 explains this by the example vector V1 which is represented as Vh1+ Vm1+Vl1 and Vh1'+ Vm1'+Vl1'. With the exception of the outmost vectors, most of the vectors can be represented by more than one combination of the high, medium and low voltage vectors.

It is highly desirable for the switching frequency of the high voltage inverter to be minimized. The control algorithm explained in the next section aims to hold the high voltage vector as long as the reference vector can reached through this high voltage vector. We will refer to the hexagonal area marked by the vectors reachable through a given high state vector by its *domain*. The seven domains of the high vectors are shown in Fig. 4. The details shown in the domain of the high state x_{abc}=100 shows that the domain is a hexagon with a side length equivalent to $8V_s$.

The concept of domains has been extended to the middle stage vectors, where 19 hexagons can be drawn within each of the seven high state domains at the tip of the 19 medium voltage vectors. One of the middle state domains hexagons is shown in Fig. 4. If the middle state is y_{abc}=200, then the low voltage stage selection will cover the small hexagon area shown in Fig. 4, which we may refer to as the domain of state [100,200].

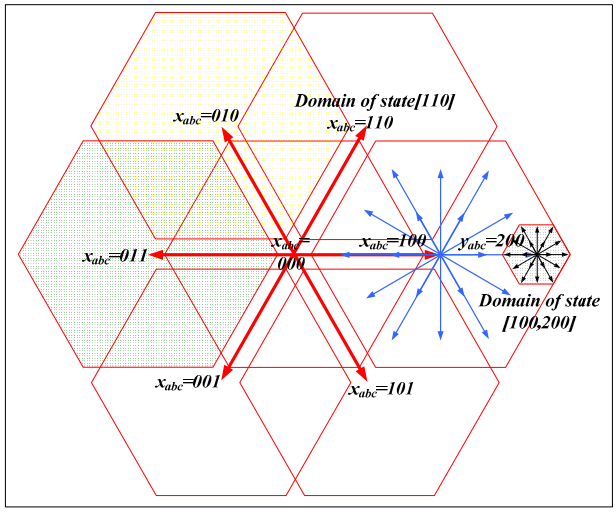

Fig. 4: The seven domains of the high voltage stage vectors

As seen in Fig.4 within the grand hexagon some of the regions are covered by exactly one high state domain forcing the controller to select it when the reference vector is located within it. Other domains are shared by two-or three- high state domains giving freedom in the high voltage state selection. We have exploited this freedom to minimize the switching actions at the higher voltage stages.

The Control Strategy

The Control Concept and General Notations

The flow diagram of the control algorithm is shown in Fig. 5. The controller checks if the reference voltage vector, to be realized in the next sampling interval, is located in the domain of the current high voltage stage vector. If so the inverter will hold the high voltage stage state otherwise it will replace it with the *nearest* state. The *nearest* state is defined as the state that can be reached with minimum number of the switching actions and has the reference vector in its domain.

After selecting the high voltage inverter state, its corresponding voltage vector is subtracted from the reference vector results the middle reference to be realized by the middle and low voltage stages. Much like the high voltage vector selection, if the middle reference is located within its domain the current middle state will be held, otherwise it will be change by the nearest state. Low voltage stage reference is determined by subtracting the voltage vector corresponding to the next middle state from the middle reference. The low voltage stage simply outputs the nearest voltage vector with minimum switching transitions.

High and Voltage Stage State Determination

The calculation of the high and medium voltage state begins by the determination if the reference vector is located in the domain of the current high or medium voltage state, if so the current state is held for the next sampling interval. Otherwise the nearest state is determined by first determining the reference voltage sector and zone according to Figures 6 and 7.

The zones have defined based on the overlap of the domains of adjacent and zero vectors. Table defines the feasible next states for the general sector zones shown in Fig. 6. When there is more than one feasible state the one reachable with minimum switching transition to be selected. A lookup table has been constructed to define the nearest state to all values of initial states for each sector and zone.

The medium stage zones are defined in Fig. 7. The lookup table technique has not been adopted here as the size of table will be large. Instead an four-level (if-then) tree has be written to determine the next medium state.

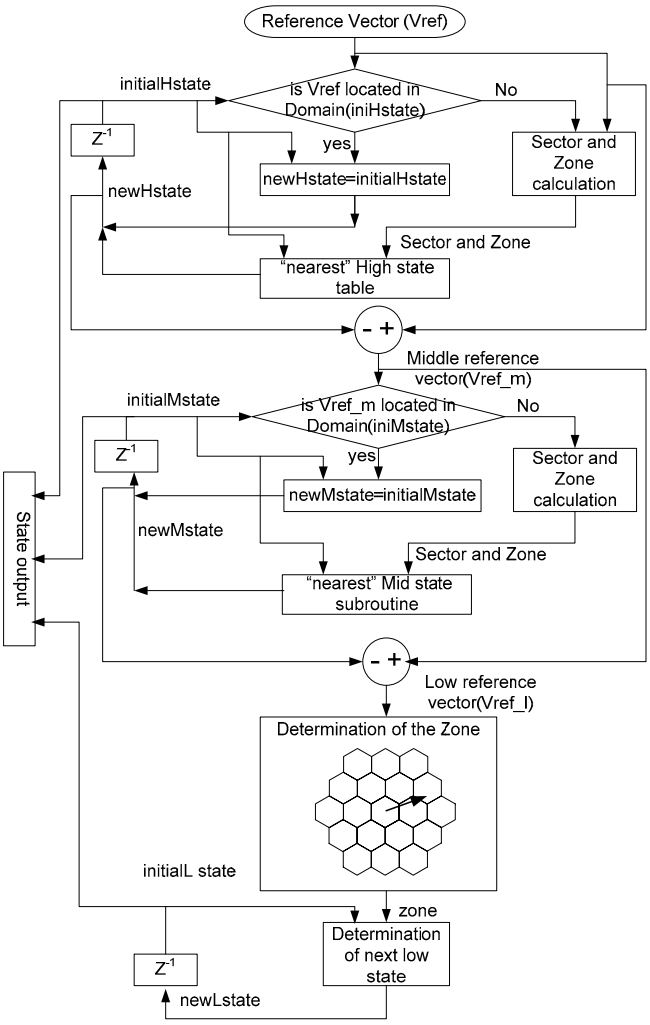

Fig. 5: Flow diagram of the 18 level inverter control algorithm

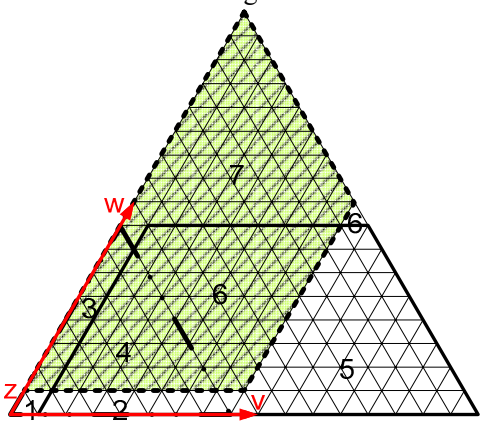

Fig.6: The high state 7 zones defined to determine the high voltage state.

Table I. Feasible next states for the seven high zones

Zone	1	2	3	4	5	6	7
feasible next state(s)	z	v,z,	w,z	v,w,z	v	v,w	w

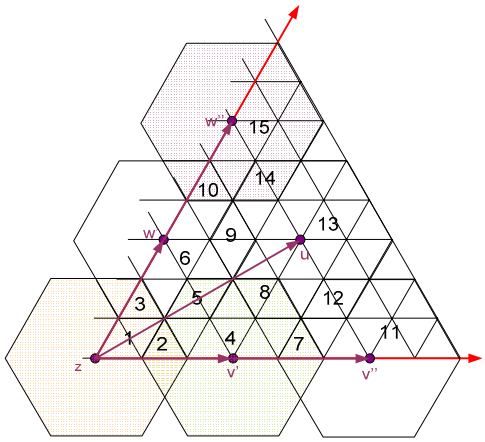

Fig. 7: The medium state inverter sector zones

Low Voltage Stage State Determination

The reference voltage for the low voltage stage is determined by subtracting the medium state vector from the medium stage reference vector as indicated in Fig. 5.

The low stage zone corresponding to each of the low voltage vectors has been defined as the nearest region to that vector as shown in Fig. 8. The control concept is to determine the zone at which the reference vector is located and operate the inverter in the corresponding state. If the vector is associated with two or three switching states, then the initial state will be considered to select the state reachable with minimum switching.

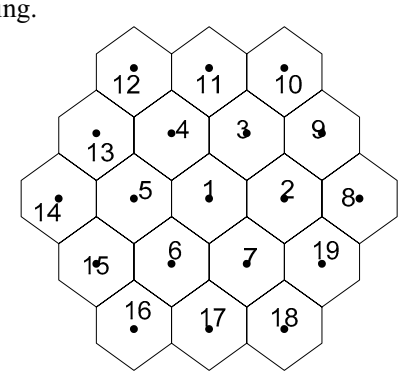

Fig. 8**.** Low voltage stage voltage vector zones.

The determination of the low voltage zone has been carried out by two steps, first axis transformation of the reference vector. Following v-w axis system shown in Fig. 9 the reference vector has been represented by its v-w components according to equation (3).

$$\begin{bmatrix} v_{ref} \\ w_{ref} \end{bmatrix} = \begin{bmatrix} 0.5 & -\frac{\sqrt{3}}{2} \\ 0.5 & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} d_{ref} \\ q_{ref} \end{bmatrix} \tag{3}$$

With this axis transformation we can notice that each zone in Fig. 8 has a unique combination of three parameters (r_d or r_{d2}), (r_w or r_{w2}) and (r_v and r_{v2}). Where $r_{d,v,w}$ is the nearest integer rounding of the d,v or w-dimension and $r_{d2,v2,w2}$ is the nearest integer rounding of the d, v or w-dimension +0.5. These unique combinations are illustrated in Fig. 10 and Table II. The low state zone is determined by the polynomial:

$$LowZone = \sum_{I=1}^{19} I * P_i(\breve{r}_d, \breve{r}_v, \breve{r}_w, \breve{r}_{d2}, \breve{r}_{v2}, \breve{r}_{w2}) \tag{4}$$

where P_i is a product term that produces the value 1 when reference vector axis $\breve{r}_{d,w\ v}$ (or $\breve{r}_{d2,w2\ ,v2}$) matches the values of the I^{th} zone shown in Fig 10, otherwise Pi produces zero. P_i has the following form:

$$P_i = \frac{\prod_{\substack{j=-2 \\ j\neq r_{di}}}^{j=3}(\breve{r}_d - j) * \prod_{\substack{j=-2 \\ j\neq r_{vi}}}^{j=3}(\breve{r}_v - j) * \prod_{\substack{j=-2 \\ j\neq r_{wi}}}^{j=3}(\breve{r}_w - j)}{\prod_{\substack{j=-2 \\ j\neq r_{di}}}^{j=3}(r_{di} - j) * \prod_{\substack{j=-2 \\ j\neq r_{vi}}}^{j=3}(r_{vi} - j) * \prod_{\substack{j=-2 \\ j\neq r_{wi}}}^{j=3}(r_{wi} - j)} \tag{5}$$

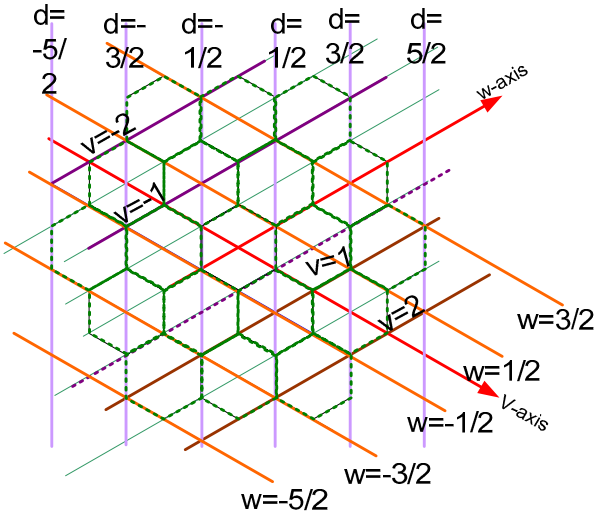

Fig. 9: the unique identification of the 19 low voltage zones in terms of integer values related to the reference voltage vector

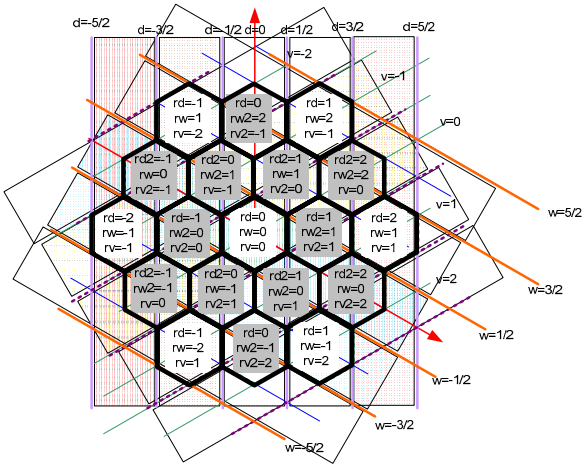

Fig. 10: the unique identification of the 19 low voltage zones in terms of integer values related to the reference voltage vector.

Table II:The integer identifiers of the 19 low state zones shown in figure 11

Zone	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
r_d	0	1	-	-	−1	-	-	2	-	1	0	−1	-	−2	-	−1	0	1	-
r_{d2}	-	-	1	0	-	0	1	-	2	-	-	-	−1	-	−1	-	-	-	2
r_v	0	-	-	−1	-	-	1	1	0	−1	-	−2	-	−1	0	1	-	2	-
r_{v2}	-	1	0	-	0	1	-	-	-	-	−1	-	−1	-	-	-	2	-	2
r_w	0	-	1	-	-	−1	-	1	-	2	-	1	0	−1	-	−2	-	−1	0
r_{w2}	-	1	-	1	0	-	0	-	2	-	2	-	-	-	−1	-	−1	-	-

Implementation

The control algorithm explained in the past section has been implemented by the controller board eZdsp F2812. The 150MHz, fixed point, low cost CPU, ran the algorithm with a sampling frequency acceding 25kHz and using the on-chip memory only reflecting the computational efficiency of the control algorithm.

A 16-bit input port has been allocated for the reference input. The 8 MSBs have been regarded as the reference voltage amplitude where the step dc voltage (Vs) is assumed to be equivalent to $(10)_{16}$. The maximum reference amplitude $(FF)_{16}$ has been set to be corresponding to a reference amplitude of almost 16Vs. This limit is justified by the fact the maximum norm of reference vector that is certain to be within the hexagon must be less than 15.588Vs. The reference vector angle is represented by the 8-LSBs of the input and coded as shown in Fig. 11. Although the resolution of this representation is 1.875°/bit and this is not the maximum resolution permitted by the 8-bit representation but this system allows direct determination of the operating sector as the 3 MSBs of the angle byte which saves computational time. On the other hand, the minimum angle between any two adjacent voltage vectors of the 18-level inverter is about 2.83°.

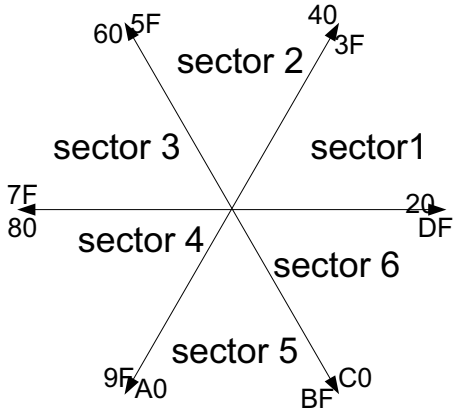

Fig 11: The values of the reference angles at the beginnings and ends of the six sectors

Results

The suggested inverter circuit and the control algorithm have been simulated to verify their validity. With a reference sinusoidal of 50Hz and magnitude control ratio of 80%, the resultant switching signals of the three stages as well as the load phase voltage waveform are shown in Fig. 12. The results show that the high voltage stage basically operates in square wave mode. The medium voltage switching frequency is at least three times that of the high voltage stage. In the particular simulation conditions the low voltage frequency is more than 15 times higher than that of high voltage stage. This number depends, however, on the magnitude control ratio.

The measured waveforms of with same 80% reference amplitude is shown in figure 13. These measurements reflects, besides the quality superiority of the proposed inverter, that the inverter design meets its objectives regarding the switching frequencies at various stages.

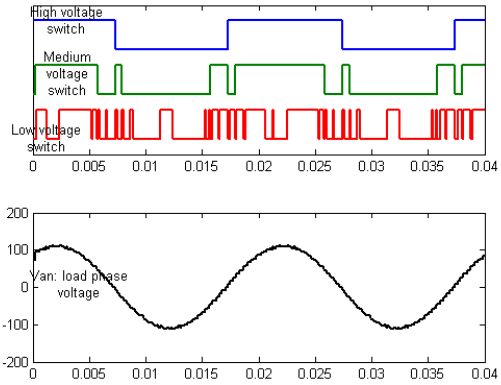

Fig. 12. Three stages switching signals and load phase voltage with 80% reference amplitude.

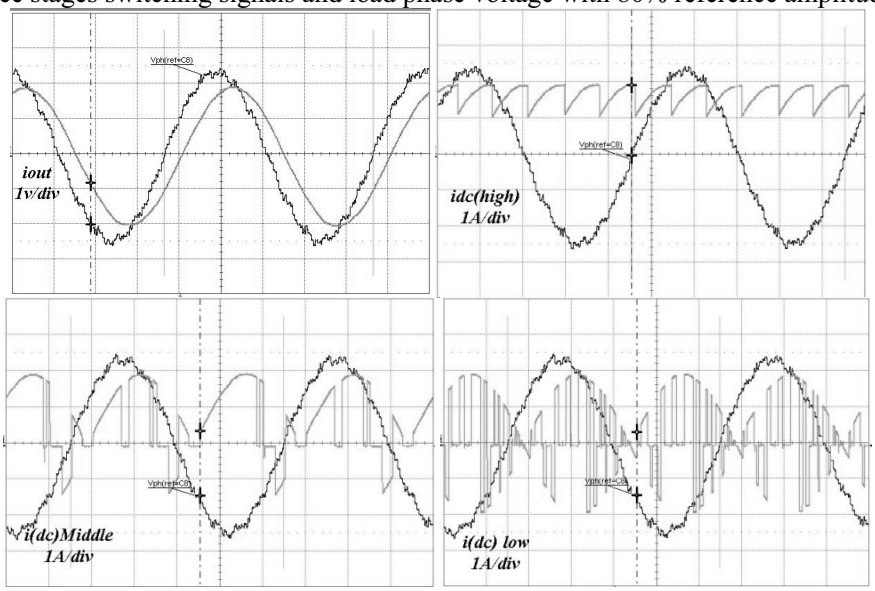

Fig. 13: Measurements with 80% reference supply load phase voltage with , a Load current, b. DC high voltage supply current, c. .DC medium voltage supply current, d. DC low voltage stage currents

Conclusion

In conclusion, we have presented a novel control strategy for the three-stage 18-level inverter. The described strategy exploits the inverters high resolution to approximate any reference vector by one of inverter vectors. The suggested strategy has been tested on low memory, fixed point processor DSP card and some details about this implementation have been given.

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