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Design and Implementation of a Multi Level Three-Phase Inverter with Less Switches and Low Output Voltage Distortion

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ABSTRACT

This paper proposes and describes the design and operational principles of a three-phase three-level nine switch voltage source inverter. The proposed topology consists of three bi-directional switches inserted between the source and the full-bridge power switches of the classical three-phase inverter. As a result, a three-level output voltage waveform and a significant suppression of load harmonics contents are obtained at the inverter output. The harmonics content of the proposed multilevel inverter can be reduced by half compared with two-level inverters. A Fourier analysis of the output waveform is performed and the design is optimized to obtain the minimum total harmonic distortion. The full-bridge power switches of the classical three-phase inverter operate at the line frequency of 50Hz, while the auxiliary circuit switches operate at twice the line frequency. To validate the proposed topology, both simulation and analysis have been performed. In addition, a prototype has been designed, implemented and tested. Selected simulation and experimental results have been provided.

Keywords: Two-level inverter, Multi level inverter, Total harmonic distortion, Three level output waveform inverter

1. Introduction

The high standards applied today to electrical energy increases the requirement of clean sinusoidal waveforms, with minimum harmonics content. Although this can be achieved with the use of conventional inverters with six step modulation control this approach is seldom applied in practice. The output voltage of conventional two-level inverters is far from a sinusoid. The output voltage waveform total harmonic distortion (THD) ratio is approximately 31% [1]. In addition, in the case of high power, the use of the conventional inverters very rare due to the fact that the power switches have to withstand the full network voltage.

There are some proposed solutions in [2] – [6], where these topologies are formed from two cells of the classical two-level inverter topology. The outputs of these cells can be added together using injection transformers [2] - [4] or by directly connecting the output of one cell in series with another [5] – [6]. As a result, the harmonic content of the output voltage is significantly reduced.

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Multilevel inverters (MLIs) can be used to solve these problems. They are built using a number of cells; each cell consisting of switches and capacitor voltage sources. The control of the power switches allows the capacitor voltage sources to be added to obtain the desired output voltage with reduced voltage stress on each individual switch. Also, the resolution of the staircase waveform of the output voltage increases with the number of voltage steps of capacitor voltage sources available in the multilevel inverter. Three different main topologies have been reported for multilevel inverters: 1) diode-clamped or neutral-clamped [7]–[9], where the dc-bus voltage is split into (n+1) levels by n capacitors, where the middle point is called the neutral point and a number of diodes clamp the stress voltage on the power switches; 2) capacitor-clamped or flying capacitors [10]–[12], where additional capacitors are used to clamp the switches' voltage stress; 3) cascaded multi-cell with separate dc sources [3], [13], [14], where each phase leg consists of n similar cells connected in a series with each cell formed from a switched capacitor and four power switches. All these solutions are relatively simple for getting a three-level staircase waveform, but become extremely complicated for getting a higher multilevel staircase waveform.

A well-known example for the three-phase diode clamed MLI is the neutral point clamped inverter [15] which is widely used in industrial applications. It uses four switching elements and two clamping diodes in each leg. It has three-level voltage waveforms. Zero, positive and negative supply dc voltage levels that result in considerable suppression of the harmonic currents when compared with conventional full-bridge two-level inverters. Another well-know 3-level example is the VIENNA Rectifier [16]. It consists of three bidirectional switches, a three-phase full bridge diode rectifier, and a high switching transformer in its structure to get a 3-level boost type rectifier system. This can be called a unidirectional type. A similar topology can be found in [17] with a higher number of switches.

The principle of improving the quality of the waveform of the classical inverter by inserting an auxiliary circuit between the source and the power switches of the full-bridge inverter has been reported in the literature for single phase inverter only in [18], [19], and [20]. In [18], the auxiliary circuit is formed from two switching elements and two diodes, while in [19] the auxiliary circuit contains one switching element and a full bridge of diodes. In [20] a switched capacitor circuit is used which is formed from two diodes, two capacitors and a switching element. As a result, a five-level waveform is obtained at the inverter output which results in significant suppression of the load harmonic currents when compared with the classical three-level full bridge inverter.

Many three-phase loads require a supply of variable voltage at a variable frequency, including fast and high efficiency control by electronic means [21]. The power requirements for these applications range from fractions of kilowatts to several megawatts. It is preferred in general to take the power from a dc source and convert it to three-phase ac using power electronic dc-to-ac converters. The input dc voltage, mostly of constant magnitude, is obtained from a public utility through rectification, or from a storage battery in the case of an electric vehicle drive.

Based on the VIENNA Rectifier II [16], this paper proposes a three-phase inverter topology consisting of three bi-directional switches inserted between the source and the full-bridge power switches of the classical three-phase inverter, where the dc source is taken from the ac utility through rectification. Section 2 describes and explains the proposed inverter general block diagram, the inverter configuration, its operating principles and the control pulses needed for operating the inverter switches. Section 3 subsequently presents an analysis of the total harmonics distortion minimization control method and the inverter output waveform total harmonic distortion THD minimization analysis. To serve as a reference for the inverter's validity, section 4 gives Matlab simulated results and laboratory measurements. These results are used for verifying the performance of the proposed three-level inverter prototype whose analysis is presented in Section 2. Section 5 summarizes the proposed inverter concepts presented in the paper.

2. The Proposed Inverter Topology

The block diagram of the proposed three-phase three-level voltage source inverter system consists of two isolated and regulated dc sources, three-level inverter,

microcontrollers, a data acquisition card PCL-818L, and a personal computer as shown in fig. 1. This system acts as a link between the output of the linear generator and the load, where the linear generator output voltage magnitude is a single phase distorted waveform with its frequency varying from 25 to 50 Hz. Due to that, it is not suitable for many applications, which use a 50 Hz ac. The inverter output voltage can be controlled by controlling the dc inverter bus link voltages, where two dc-dc boost converter circuits with a 10 kHz switching frequency have been used. The measured voltages of the inverter dc capacitor link (two analogue signals) from the sensors are received first by microcontroller1 and microcontroller2 which convert them to 8 bits digital signals for each analogue signal (16 bits total). These 16 digital bits are received by the PC through the PCL-818L card.

The digital data is processed in real time to calculate the duty cycle of each dc-dc converter using a PID controller. The sampling frequency is chosen to be 2 kHz which is fast enough to perform these calculations. These duty cycles are subsequently sent back to the hardware through the PCL-818L card in a digital form. Microcontroller1 and Microcontroller2 receive this digital data from the PCL-818L card and converts it to a duty cycle required by each switch in the dc-dc converter. Microcontroller3 is used to generate the inverter nine controlling pulses. In order to avoid a short circuit during the transition between switches of each leg, a proper time delay has been considered.

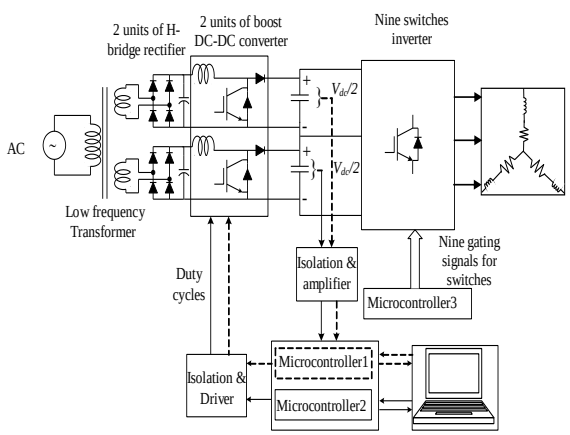


Fig. 1. Block diagram of the proposed inverter and the feedback control circuit.

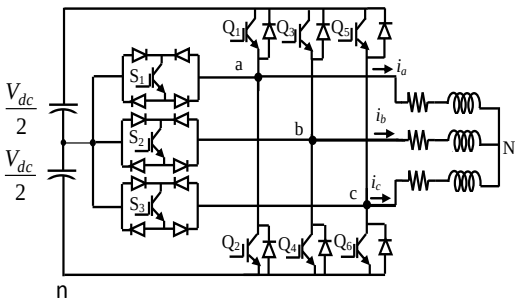


Fig. 2. The proposed nine switch three-level inverter.

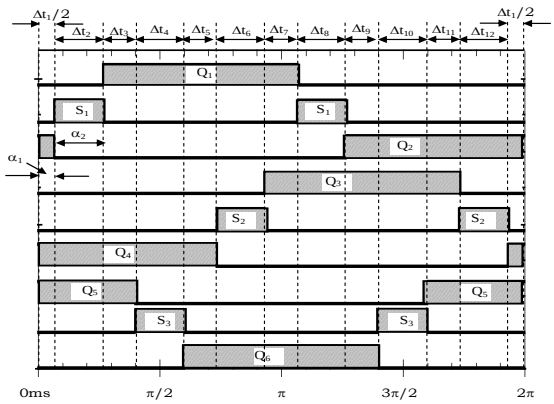


Fig. 3. Switching timing diagram.

Fig. 2 shows the proposed inverter which consists of two isolated H-bridge circuit units, capacitor banks C_1 and C_2 respectively, conventional two-level inverters Q_1 through Q_2 as a main inverter at 50 Hz switching frequency; and an additional circuit which compromises of bi-directional (middle) switches S_1 through S_3, at 100 Hz switching frequency, which allows energy to flow in both directions.

3. The Operational Principals

Fig. 3 shows the proposed controlling pulses of the switches, where the operations can be divided to 12 switching states. The switch on/off states are shown in Table 1 and the operational modes are illustrated in fig. 4(i), (ii), (iii), (iv), (v), (vi), (vii), (viii), (ix), (x), (xi), and (xii). The operational modes can be explained as follows:

Mode i: For switching duration time Δt_1 ($2\alpha_1$), only switches Q_2, Q_4, Q_6 are in the on-state and all the

Table 1. Switching states of switches in each step duration.

Step Duration	Conduction period	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	S_1	S_2	S_3	v_{an}, v_{bn}, and v_{cn}	v_{aN}, v_{bN}, and v_{cN}
Δt_1	$2\alpha_1$	0	1	0	1	1	0	0	0	0	$(0,0,1)V_{dc}$	$\frac{(-2,-2,4)V_{dc}}{6}$
Δt_2	α_2	0	0	0	1	1	0	1	0	0	$(0.5,0,1)V_{dc}$	$\frac{(0,-3,3)V_{dc}}{6}$
Δt_3	$2\alpha_1$	1	0	0	1	1	0	0	0	0	$(1,0,1)V_{dc}$	$\frac{(2,-4,2)V_{dc}}{6}$
Δt_4	α_2	1	0	0	1	0	0	0	0	1	$(1,0,0.5)V_{dc}$	$\frac{(3,-3,0)V_{dc}}{6}$
Δt_5	$2\alpha_1$	1	0	0	1	0	1	0	0	0	$(1,0,0)V_{dc}$	$\frac{(4,-2,-2)V_{dc}}{6}$
Δt_6	α_2	1	0	0	0	0	1	0	1	0	$(1,0.5,0)V_{dc}$	$\frac{(3,0,-3)V_{dc}}{6}$
Δt_7	$2\alpha_1$	1	0	1	0	0	1	0	0	0	$(1,1,0)V_{dc}$	$\frac{(2,2,-4)V_{dc}}{6}$
Δt_8	α_2	0	0	1	0	0	1	1	0	0	$(0.5,1,0)V_{dc}$	$\frac{(0,3,-3)V_{dc}}{6}$
Δt_9	$2\alpha_1$	0	1	1	0	0	1	0	0	0	$(0,1,0)V_{dc}$	$\frac{(-2,4,-2)V_{dc}}{6}$
Δt_{10}	α_2	0	1	1	0	0	0	0	0	1	$(0,1,0.5)V_{dc}$	$\frac{(-3,3,0)V_{dc}}{6}$
Δt_{11}	$2\alpha_1$	0	1	1	0	1	0	0	0	0	$(0,1,1)V_{dc}$	$\frac{(-4,2,2)V_{dc}}{6}$
Δt_{12}	α_2	0	1	0	0	1	0	0	1	0	$(0,0.5,1)V_{dc}$	$\frac{(-3,0,3)V_{dc}}{6}$

other switches are in the off-state; i.e; $v_{an} = v_{bn} = 0$, and $v_{cn} = V_{dc}$, which means that both load nodes 'a' and 'b' are connected to the neutral point of the dc bus, while load node 'c' is connected to the top point of the dc bus as shown in fig. 4(i).

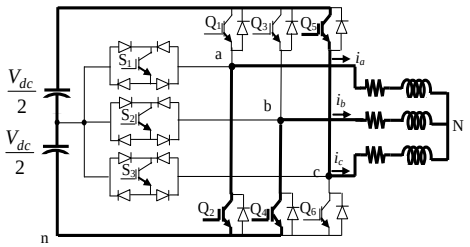
Mode ii: For switching duration time Δt_2 (α_2), only switches Q_4, Q_5, S_1 are in the on-state and the other switches are in the off-state, $v_{an} = \frac{V_{dc}}{2}, v_{bn} = 0, \quad and\ v_{cn} = V_{dc}$. This means that load node 'a' is connected to the middle point of the dc bus, load 'b' is connected to the neutral point of the dc bus, and load node 'c' is connected to the top point of the dc bus as shown in fig. 4(ii).

Mode iii: For switching duration time Δt_3 ($2\alpha_1$), only switches Q_1, Q_4, Q_5 are in the on-state and the other switches are in the off-state, $v_{an} = v_{cn} = V_{dc}$, and $v_{bn} = 0$, and $v_{cn} = V_{dc}$.

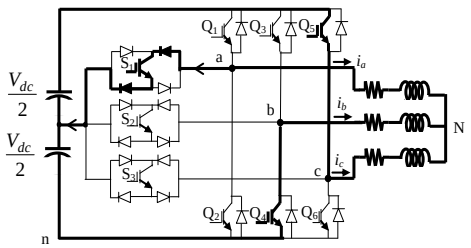
In this case both load nodes 'a' and 'c' are connected to the top point of the dc bus, while load node 'b' is connected to the neutral point of the dc bus as shown in fig. 4(iii).

Mode iv: For switching duration time Δt_4 (α_2), only switches Q_1, Q_4, S_3 are in the on-state and the other switches are in the off-state, $v_{an} = V_{dc}$, and $v_{bn} = 0$, and $v_{cn} = \frac{V_{dc}}{2}$. This means that load node 'a' is connected to the top point of the dc bus, load 'b' is connected to the neutral point of the dc bus, and load node 'c' is connected to the middle point of the dc bus as shown in fig. 4(iv).

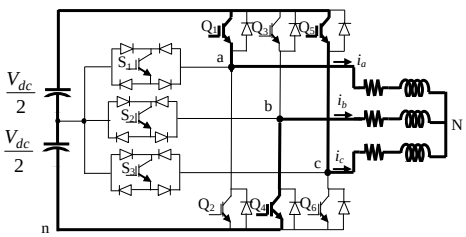
Mode v: For switching duration time Δt_5 ($2\alpha_1$), only switches Q_1, Q_4, Q_6 are in the on-state and the other switches are in the off-state, $v_{bn} = v_{cn} = 0$, and $v_{an} = V_{dc}$. During this switching period, both load nodes 'b' and 'c' are connected to the neutral point of the dc bus, and the load node 'a' is connected to the top point of the dc bus as shown in fig. 4(v).



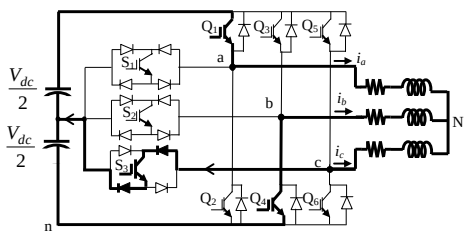
Mode i; $v_{an}=0;\ v_{bn}=0,\ v_{cn}=V_{dc}$



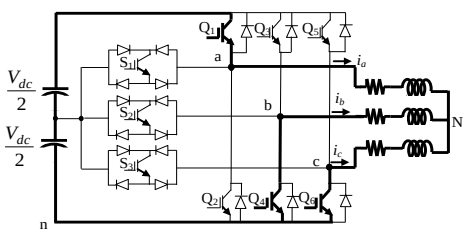
Mode ii; $v_{an}=\frac{V_{dc}}{2};\ v_{bn}=0,\ v_{cn}=V_{dc}$



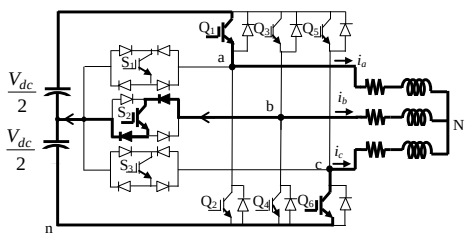
Mode iii; $v_{an}=V_{dc};\ v_{bn}=0,\ v_{cn}=V_{dc}$



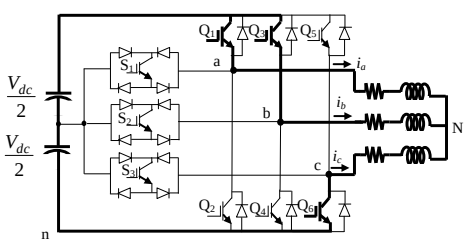
Mode iv; $v_{an}=V_{dc};\ v_{bn}=0,\ v_{cn}=\frac{V_{dc}}{2}$



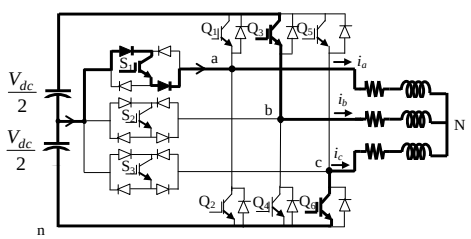
Mode v; $v_{an}=V_{dc};\ v_{bn}=0,\ v_{cn}=0$



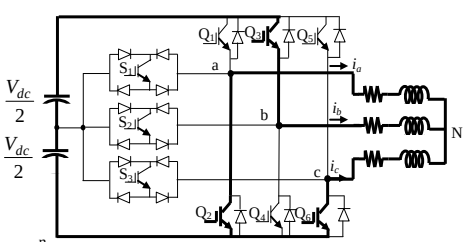
Mode vi; $v_{an}=V_{dc};\ v_{bn}=\frac{V_{dc}}{2},\ v_{cn}=0$



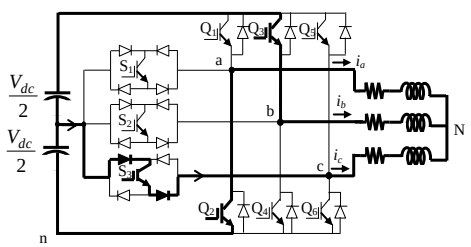
Mode vii; $v_{an}=V_{dc};\ v_{bn}=V_{dc},\ v_{cn}=0$



Mode viii; $v_{an}=\frac{V_{dc}}{2};\ v_{bn}=V_{dc},\ v_{cn}=0$

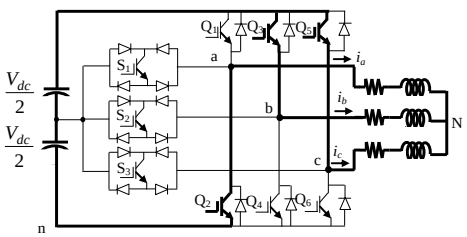


Mode ix; $v_{an}=0;\ v_{bn}=V_{dc},\ v_{cn}=0$

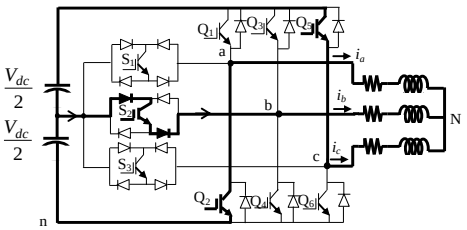


Mode x; $v_{an}=0;\ v_{bn}=V_{dc},\ v_{cn}=\frac{V_{dc}}{2}$

Fig. 4. Operational states of switches according to the switches on-off conditions. (Continued)



Mode xi; $v_{an}=V_{dc}$; $v_{bn}=V_{dc}$, $v_{cn}=V_{dc}$



Mode xii; $v_{an}=0$; $v_{bn}=\frac{V_{dc}}{2}$, $v_{cn}=V_{dc}$

Fig. 4. Operational states of switches according to the switches on-off conditions.

Mode vi: For switching duration time Δt_6 (α_2), only switches Q_1, Q_6, S_2 are in the on-state and the other switches are in the off-state, $v_{an}=V_{dc}, v_{bn}=\frac{V_{dc}}{2}$ and $v_{cn}=0$. This means that load node 'a' is connected to the top point of the dc bus, load node 'b' is connected to the middle point of the dc bus, and load node 'c' is connected to the neutral point of the dc bus as shown in fig. 4(vi).

Mode vii: For switching duration time Δt_7 ($2\alpha_1$), only switches Q_1, Q_3, Q_6 are in the on-state and the other switches are in the off-state, $v_{an}=v_{bn}=\frac{V_{dc}}{2}$, and $v_{cn}=0$. During this duration period, both load nodes 'a' and 'b' are connected to the top point of the dc bus, and the load node 'c' is connected to the neutral point of the dc bus as shown in fig. 4(vii).

Mode viii: For switching duration time Δt_8 (α_2), only switches Q_3, Q_6, S_1 are in the on-state and the other switches are in the off-state $v_{an}=V_{dc}, v_{bn}=\frac{V_{dc}}{2}$, and $v_{cn}=0$. The load node 'a' is connected to the top point of the dc bus, load node 'b' is connected to the middle point of the dc bus, and load node 'c' is connected to the neutral point of the dc bus as shown in fig. 4(vii).

Mode ix For switching duration time Δt_9 ($2\alpha_1$), only switches Q_2, Q_3, Q_6 are in the on-state and the other switches are in the off-state $v_{an}=v_{cn}=0$, and $v_{bn}=V_{dc}$. In this case of switching duration both of the load nodes 'a' and 'c' are connected to the neutral point of the dc bus, and load node 'b' is connected to the top point of the dc bus as shown in fig. 4(ix).

Mode x: For switching duration time Δt_{10} (α_2), only switches Q_2, Q_3, S_3 are in the on-state and the other switches are in the off-state $v_{an}=0$, $v_{bn}=V_{dc}$, and $v_{cn}=\frac{V_{dc}}{2}$. During this switching period, load node 'a' is connected to the pole of the dc bus, load node 'b' is connected to top point of the dc bus, and load node 'c' is connected to the middle point of the dc bus as shown in fig. 4(x).

Mode xi: For switching duration time Δt_{11} ($2\alpha_1$), only switches Q_2, Q_3, Q_5 are in the on-state and the other switches are in the off-state $v_{bn}=v_{cn}=V_{dc}$, and $v_{an}=0$. In this switching period both the load nodes of 'b' and 'c' are connected to the top point of the dc bus, while load node 'a' is connected to the neutral point of the dc bus as shown in fig. 4(xi).

Mode xii: For switching duration time Δt_{12} (α_2), only switches Q_2, Q_5, S_2 are in the on-state and the other switches are in the off-state $v_{an}=0, v_{bn}=\frac{V_{dc}}{2}$, and $v_{cn}=V_{dc}$. In this case load node 'a' is connected to the pole of the dc bus, load node 'b' is connected to the middle point of the dc bus, and load node 'c' is connected to the top point of the dc bus as shown in fig. 4(xii).

In all of the above mentioned modes of operation conditions, while turning on and off the switches; the direction of load currents i_a, i_b, and i_c depends on voltages v_{an}, v_{bn}, and v_{cn}.

The efficiency of the whole converter circuit is high which is attributed to the inverter switches operating at low switching frequencies, (where the total switching times are much less than the period). This will result in the switching losses of the inverter circuit to be negligible [22]. In addition to the boost topology used with a single switch, it has high efficiency [1].

4. Analysis of the Optimized Waveform

By applying the switching patterns given in fig. 3, the node 'a' referred to point 'n' can be defined as follows:

- For voltage level $v_{an} = V_{dc}$, turn on the upper switch $\mathbf{Q_1}$.
- For voltage level $v_{an} = \frac{V_{dc}}{2}$, turn on the middle switch $\mathbf{S_1}$.
- For voltage level $v_{an} = \mathbf{0}$, turn on the lower switch $\mathbf{Q_2}$.

The switches' conduction angles can be calculated from fig. 5 as follows:

- For upper switches $\mathbf{Q_1}$, $\mathbf{Q_3}$, and $\mathbf{Q_5}$

$$\theta_1 = \frac{4\pi}{3} - 2(\alpha_1 + \alpha_2) \quad (1)$$

- For lower switches $\mathbf{Q_2}$, $\mathbf{Q_4}$, and $\mathbf{Q_6}$

$$\theta_2 = \frac{2\pi}{3} + 2\alpha_1 \quad (2)$$

- For bi-directional switches $\mathbf{S_1}$, $\mathbf{S_2}$, and $\mathbf{S_3}$

$$\theta_3 = 2\alpha_2 \quad (3)$$

Therefore from equations (1), (2), and (3), $\theta_1 + \theta_2 + \theta_3 = 2\pi$.

Fig. 5 illustrates the load phase voltages $v_{an}, v_{bn}, and\ v_{cn}$ referred to the neutral point of the dc bus. If neutral point 'n' of the dc bus is not connected to the neutral point of the load 'N', the phase voltages of the load are related to the neutral point of the dc bus 'n' as given in [23] by the following equation:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (4)$$

The line-to-line load voltage v_{ab} can be obtained using the following equation:

$$v_{ab} = v_{an} - v_{bn} \quad (5)$$

From equations (4) and (5), the phase voltage of node 'a' v_{aN} and the line-to-line voltage v_{ab} can be calculated and drawn as shown in fig. 6. The load phase voltage has 7 steps ($\frac{-2V_{dc}}{3}, \frac{-V_{dc}}{2}, \frac{-V_{dc}}{3}, 0, \frac{V_{dc}}{3}, \frac{V_{dc}}{2}, and\ \frac{2V_{dc}}{3}$) and the line-to-line voltage has 5 steps ($-V_{dc}, \frac{-V_{dc}}{2}, 0, \frac{V_{dc}}{2}, and\ V_{dc}$). The line-to-line voltage waveform as shown in fig. 6 (b) is known as a stepped waveform. A Fourier analysis of this waveform gives the magnitudes of the harmonics as a function of α_1 and α_2 as shown in equation (6).

$$V_n = \frac{4\left(\frac{V_{dc}}{2}\right)}{n\pi\{\cos(n\alpha_1) + \cos n(\alpha_1 + \alpha_2)\}}$$

, n=1,3,5,…… (6)

The voltage rating of the upper or lower switch is V_{dc} because it conducts during the total bus voltage while the voltage rating of the middle switch is $\frac{V_{dc}}{2}$ because it conducts during half of the dc bus voltage. The current voltage ratings of these different switches are shown in table 2.

The ideal is to get a clean sinusoidal output voltage, i.e., the content of the harmonics orders greater than one (*n*=3, 5, 7 …) should be zero. The THD of the output voltage is defined as $THD = \frac{1}{V_1}\sqrt{\sum_{3,5,7,..}^{\infty} V_n^2}$, where V_n is calculated from (6). Fig. 7 shows a computer simulation of the *THD* as a function of the parameters α_1 and α_2, where the minimum *THD* (*THD* < 16%) is obtained for $\alpha_1 \approx 12°$ and $\alpha_2 \approx 30°$.

By comparing the proposed inverter which consists of 9 power switches and 12 main power diodes with the

three-level NPC inverter which consists of 12 main power switches and 6 main power diodes[24]–[25] under fundamental frequency modulation, it can be concluded that they produce the same output voltage waveform performance. Also table 3 gives a comparison between the proposed inverter and the well-known 3-level inverters: diode-clamped, flying capacitor, and cascaded inverters.

It can be concluded that the disadvantage of the proposed inverter is that the voltage ratings of the switches have not been reduced. Also, they have different ratings which are similar to the voltage ratings of the diode-clamped inverter switches [10]. Some switches have ratings of V_{dc} while others have voltage ratings of $\frac{V_{dc}}{2}$. In this proposed topology, the switches $Q_1, Q_2, Q_3, Q_4, Q_5, \text{and } Q_6$ have the same voltage and current switch ratings (V_{dc} and load current) and are greater than middle switches S_1, S_2, and S_3 (V_{dc}/2 and 27.2% of the load current).

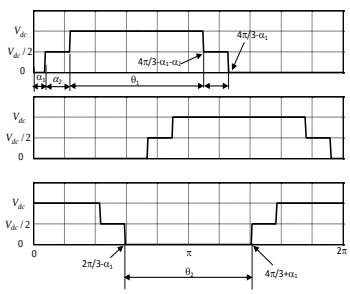


Fig. 5. MATLAB SIMULINK simulated waveforms of the load node voltages v_{an}, v_{bn} and v_{cn}.

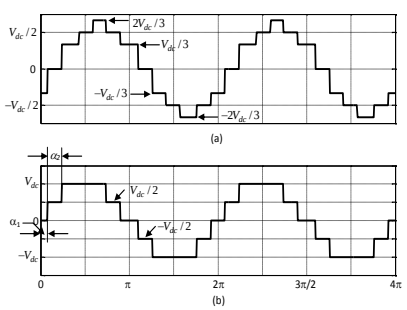


Fig. 6. MATLAB SIMULINK simulated waveforms of: (a) the load phase voltage waveform v_{aN} and (b) the line-to-line voltage waveform v_{ab}.

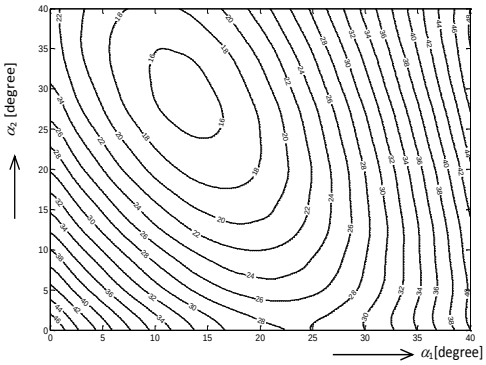


Fig. 7. THD of the output voltage as a function of α_1 and α_2.

Table 2. Current and voltage ratings for inverter switches.

	RMS Current ratings	Max Current ratings
The upper switch	$\%(I_{switch}/I_{Load})_{RMS} \cong 72.5$	$\%(I_{switch}/I_{Load})_{max} = 100$
The lower switch	$\%(I_{switch}/I_{Load})_{RMS} \cong 72.5$	$\%(I_{switch}/I_{Load})_{max} = 100$
The middle switch	$\%(I_{switch}/I_{Load})_{RMS} \cong 27.2$	$\%(I_{switch}/I_{Load})_{max} \cong 50$
	RMS voltage ratings	max voltage ratings
The upper switch	$\%(V_{switch\ RMS}/V_{dc}) \cong 66$	$\%(V_{switchmax}/V_{dc}) = 100$
The lower switch	$\%(V_{switch\ RMS}/V_{dc}) \cong 66$	$\%(V_{switchmax}/V_{dc}) = 100$
The middle switch	$\%(V_{switch\ RMS}/V_{dc}) \cong 43$	$\%(V_{switch\ max}/V_{dc}) = 50$

RMS ≅ root mean square
max ≅ maximum

Table 3. Comparison of the proposed 3L inverter with the well-known 3-level inverters.

Converter type	Proposed inverter	Diode-clamp	Flying-capacitors	Cascaded inverters
Main switching devices	9	12	12	12
Main diodes	18	12	12	12
Clamp-ing diodes	0	6	0	0
DC bus	2	2	2	3
Balanc-ing capacitors	0	0	3	0

5. Results and Discussions

The proposed topology has been simulated using MATLAB/SIMULINK® to verify the performance of the proposed configuration. The dynamic response due to a sudden change in the reference voltage is presented and a Proportional Integral and Derivative (PID) controller has been implemented in order to maintain balanced voltages in the dc bus capacitor. A balanced three-phase star connected RL load with 30Ω resistance, and 50mH inductor per phase was used.

Fig. 8 shows the inverter dc bus voltages of the upper and the lower capacitor banks respectively with controllers, where a step change in the reference voltage from 80V to 110V is shown. Because the voltage of each capacitor is regulated to 80 V or 110 V, the total dc-link voltage is maintained at 160 V and 220 respectively. Fig. 9 shows the inverter output waveforms of the phase voltage v_{aN}, line-to-line voltage v_{ab}, and the line current i_a. The phase voltage exhibits seven levels ($\frac{-2V_{dc}}{3}, \frac{-V_{dc}}{2}, \frac{-V_{dc}}{3}, 0, \frac{V_{dc}}{3}, \frac{V_{dc}}{2}, and\ \frac{2V_{dc}}{3}$), and the line-to-line voltage shows five levels ($-V_{dc}\ \frac{-V_{dc}}{2,0},\ \ \frac{V_{dc}}{2},\ \ and\ V_{dc}$). It is clearly shown that v_{aN}, v_{ab}, and i_a follow the step change in dc capacitor voltage at 100ms.

To validate the proposed inverter, an experimental prototype of the proposed inverter has been built, experimentally tested, and compared with the simulated results. A balanced three-phase star connected load with 30Ω resistance, and 50mH inductor per phase was used. The inverter circuit was built using insulated gate bipolar transistors (IGBTs) as switches, and each bi-directional switch consisting of one IGBT and 4 elements of fast diode rectifiers. The inverter switching frequencies are 50 Hz for the conventional two-level inverter and 100 Hz for bi-directional switches. The control circuit switching frequency is 10 kHz which consists of 2 units of dc-dc boost converters.

Fig. 10 shows a step change in the dc link capacitor voltage, where a step change has been applied from 80V to 110 V in each capacitor bank, thus maintaining 160V and 220V on the dc bus, respectively. Fig. 11 shows the phase voltage v_{aN} with seven steps and the line-to-line voltage v_{ab} with five steps which were obtained in the simulation results. Fig. 12 shows the phase voltage v_{aN} and the line current i_a.

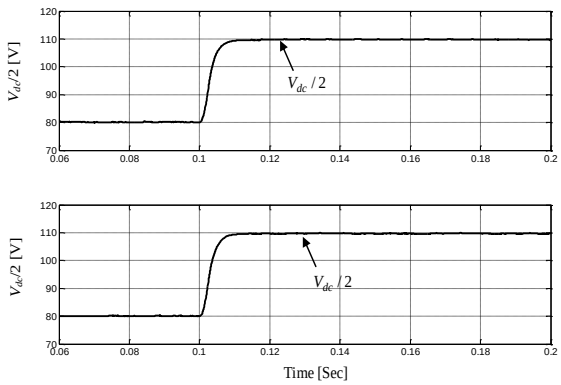


Fig. 8. Simulation results of the upper and lower regulated capacitor banks voltages.

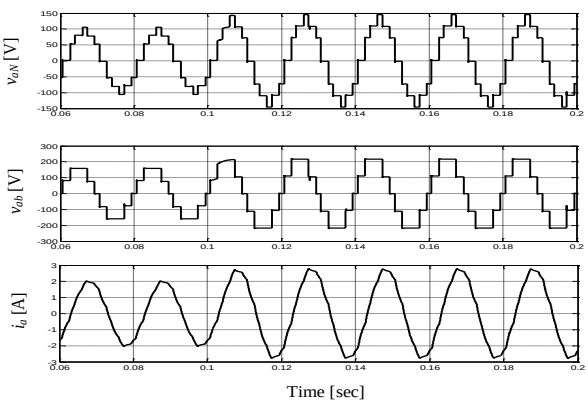


Fig. 9. Inverter output (from top to bottom) phase voltage v_{aN}, line to line voltage v_{ab}, and line (phase) current i_a respectively.

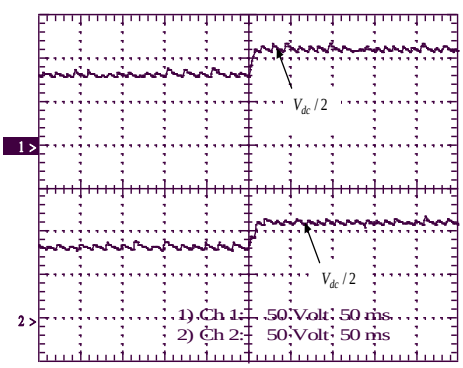


Fig. 10. The inverter dc bus voltages (50V/div, 50ms/div).

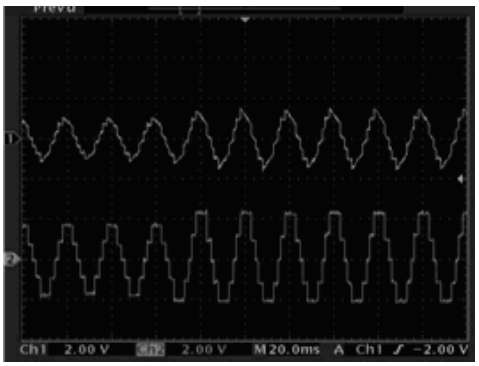


Fig. 11. The load phase voltage v_{aN} and the line to line voltage v_{ab} (200V/ div, 20ms/ div).

Fig.12. The load phase voltage v_{aN} and the line current i_a (150V/ div, 5Amp/ div, 20ms/ div).

6. Conclusions

This paper presents a three-phase three-level nine switch voltage source inverter, where an additional auxiliary circuit which consists of three bi-directional switches has been inserted between the source and the full-bridge power switches of the classical three-phase inverter. As a result, a significant reduction of the load harmonics contents is obtained at the inverter output. Its operating principles and switches timing chart based on harmonic minimization control schemes are analyzed in detail. A prototype has been designed; implemented and tested; also a PID controller has been designed and implemented in the case of a step change in the inverter dc bus voltage. The dynamic responses of load waveforms due to the step change are provided. The simulation and experimental results show that THD of the proposed inverter is considerably improved.

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