Briefs

Application of a Floating Well Concept to a Latch-up-Free, Low-Cost, Smart Power High-Side Switch Technology

M. Bafleur, J. Buxo, M. Puig Vidal, P. Givelin, V. Macary, and G. Sarrabayrouse

Abstract—**The aim of this brief is to present an original design methodology that permits implementing latch-up-free smart power circuits on a very simple, cost-effective technology. The basic concept used for this purpose is letting float the wells of the MOS transistors most susceptible to initiate latch-up.**

I. Introduction

This brief intends to show that for the voltage ratings typically required in automotive applications, it is possible to avoid complex "dielectric-isolation" or "junction-isolated" technologies using a self-isolated, single-epilayer CMOS/DMOS technology. To shield the logic area from the transient voltage disturbances, caused by the ON/OFF switching of the power transistor, it is necessary to find a "design-based" solution. Indeed, CMOS logic circuits have to be employed to achieve low-voltage logic circuitry with very low standby current but are particularly prone to latch-up under such disturbances. As shown in the following, the latch-up immunity requirement can be met by letting float the voltage of the P^--well in which the n-channel transistors of the CMOS control circuitry are sitting.

II. Initiation of Latch-up and Floating Well Concept

A. Static Behavior

In many cases and particularly in VLSI circuits, using grounded body ties in the p-well is the best solution to avoid latch-up initiation. However, in the case of power integrated circuits, the parasitic transient can be such that even with grounded body ties, the p-well does not remain equipotential and activation of the parasitic vertical bipolar (PVB) occurs. The grounded body tie therefore supplies the PVB with as much base current as required and latch-up can be initiated and be fatal for the circuit.

The basic principle of the floating well concept is that, on the one hand, it can follow the voltage transient thus avoiding in most cases the turn-on of the PVB and on the other, even if the PVB is activated, base current is only provided during a limited and layout-controlled time that can be made less than the latch-up regeneration time [1].

Letting float the voltage of the p-well has already been contemplated as a solution to the latch-up problem, particularly for CMOS analog switches [2]. However, numerous drawbacks have been noted. The breakdown voltage BV_{CEo} appears to be reduced and the leakage current of floating-body devices is higher because I_{Ceo} is much greater than the I_{CBo} of devices having fixed reversed-biased body potentials.

However, in the present situation, since the technology includes all the elements that make up a DMOS power device, it is shown that, proper use of the deep p^+ diffusion inherent in this power device, allows producing floating body, n-channel devices with no tendency to display early breakdowns or to initiate latch-up and with conveniently low I_{CEo} leakage currents. Fig. 1 shows that this deep p^+ diffusion is made to properly overlap the n^+-emitter (NMOS source) of the PVB in the floating body arrangement so as to obtain a convenient reduction in the emitter efficiency [3]. Indeed, an n^+/p^+ diode is thus introduced between well and ground. In such heavily doped junction, Auger recombinations are likely to occur and be dominant at low bias voltages and then to yield higher forward currents than in an n^+/p^- diode. Therefore, under a slight forward bias, this diode will provide sufficient conductance to drive the majority-carrier current out of the well without significant bias of the n^+-source associated PVB.

To verify this behavior, an 8 masks metal-gate CMOS technology including an extra deep p^+ diffusion was purposely developed and a specific latch-up test vehicle was designed and produced at the silicon fabrication facility of our laboratory. First, it was shown that, at low bias voltages (≤ 0.5 V), the forward current of a Zener diode (n^+/p^+) can be one decade higher than that of a normal diode (n^+/p^-) thus providing leakage currents with the desired low resistance path. The consequence of this effect is shown in Fig. 2 which compares the I_{CEo} currents of two floating well configurations: unprotected and deep p^+ protected emitter, to the I_{CBo} current. Indeed, in the deep p^+ protected configuration, the I_{CEo} value is as low as the I_{CBo} value and the BV_{CEo} breakdown voltage value is closer to the BV_{CBo} value. A comparison of these two floating well structures under steady-state latch-up conditions (Fig. 3) corroborates that the deep p^+ protected structure has a higher switching voltage and holding current.

The drawbacks of the floating well configuration have then been overcome with the deep p^+ diffusion arrangement that permits to achieve proper self-biasing of the well with little influence on threshold voltage. Indeed, drain current measurements have shown that the kink effect is rejected away from the low-voltage operating range (0–6 V).

B. Transient Behavior

Transient-caused latch-up initiation is the main phenomenon that can jeopardize smart power circuits. Therefore, a protective design methodology aimed at inhibiting, in a transient situation, the activation of the two parasitic vertical bipolar transistors, PVB_D and

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M. Bafleur, J. Buxo, P. Givelin, and G. Sarrabayrouse are with Laboratoire d'Automatique et d'Analyse des Systèmes du C.N.R.S., 31077 Toulouse Cedex, France.

M. P. Vidal is with Laboratoire d'Automatique et d'Analyse des Systèmes du C.N.R.S., 31077 Toulouse Cedex, France, on leave from Universitat de Barcelona, Diagonal 645-647, 08028 Barcelona, Spain.

V. Macary is with Motorola Semiconducteurs, Le Mirail BP 1029, 31023 Toulouse Cedex, France.

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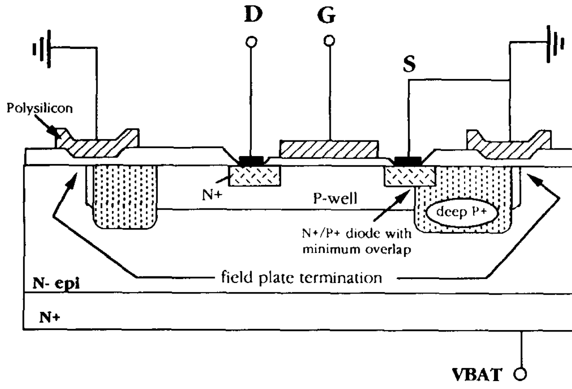

Fig. 1. Deep p^+ protected floating well NMOS transistor.

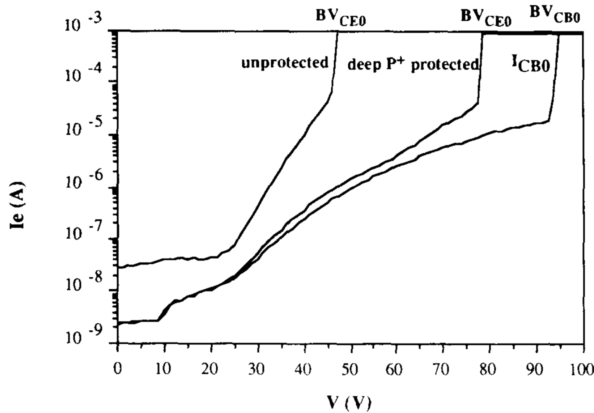

Fig. 2. I_{CE_0} currents in floating well structures.

PVB_S, respectively, related to the drain and source diffusions of the n-channel device has been proposed. Indeed, as a result of capacitive coupling, a negative voltage fluctuation, $\Delta V < 0$, originating in the substrate and transmitted through the parasitic capacitances of the MOS devices, tends to turn on temporarily the PVB_D. The floating well based design methodology should be such that the base current $I(t)$ supplied to PVB_D during the transient is made as small as possible. Since $I(t)$ is provided by the floating well capacitances, this will be achieved by reducing the available amount of charges Q in it, as well as its duration. In these circumstances, this time during which PVB_D remains in the on-state can be made less than the latch-up regeneration time [1].

A limited value and duration of $I(t)$ is practically achieved by introducing in the layout the largest possible value of R_{p^-}, the well resistance under the transistor channel and a minimum value of Cj, the capacitor resulting from the overlap between deep p^+ and grounded n^+ source, which is the most significant contribution to the floating well capacitor (Fig. 1). The expression of $I(t)$ is given by

$$I(t) = \frac{\Delta Vx}{R_p} \cdot \exp\left(-\frac{t}{Cj \cdot R_{p^-}}\right) \quad (1)$$

where ΔVx is the voltage fluctuation on the emitter of PVB_D and with a boundary condition such that

$$\int_0^\infty I(t)\, dt = Q \quad (2)$$

with Q equal to $Cj \cdot \Delta Vx$.

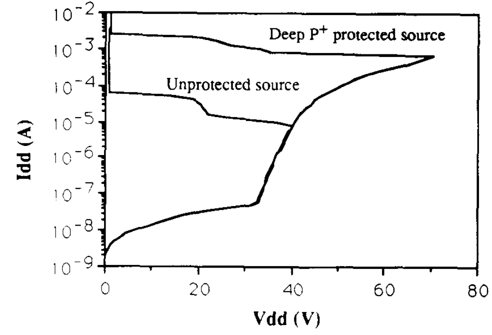

Fig. 3. Steady-state latch-up characteristics.

To achieve maximum R_{p^-}, it is important that in the field oxide region of the transistor, a thick oxide film without field implant underneath be used instead of the classical local oxide technology that uses the p^+ field implant and therefore reduces R_{p^-}. Furthermore, the minimum possible Cj value is required and will only be limited by the necessity of allowing the aforementioned forward conductance in the deep p^+/n^+-source diode that provides proper biasing of the floating well by efficiency driving the majority-carrier current to ground.

Transient electrical measurements were performed on deep p^+ protected structures of the latch-up test vehicle. It was shown that, in the floating case, PVB_D is activated but turns off with an RC time constant after the end of the transient whereas in the grounded case it remains on, its maximum current value being about 20 times higher.

In the case of a positive voltage transient, $\Delta V > 0$, originating in the epilayer, its direct capacitive coupling into the well may activate either PVB_D or PVB_S. In order to avoid this, the deep p^+ diffusion overlapping the n^+-source also surrounds the NMOS transistor (Fig. 1) and plays the role of a capacitive attenuator.

C. Floating Well Design Methodology

On the smart power chip, so as to minimize interaction between the power part and the control circuitry, at least one minority-carrier diffusion length spacing has to be introduced between them, that is about 200 μm.

In order to alleviate the dc situation created as far as BV_{CE_0} and I_{CE_0} that has already been alluded to, the deep p^+-diffusion is not only confined to overlapping the n^+-source of the transistor but is also allowed to surround the device (Fig. 1) or a set of devices completely, so that the current flowing into the p^--well through the various reversely biased junctions is properly conveyed through the low resistance deep p^+-path and eventually to ground through the very slightly fowardly biased deep p^+/n^+ junction. In order to take into account temperature effects, each high-voltage NMOS transistor will be properly protected with its own deep p^+ ring whereas a set of low-voltage NMOS transistors will be allowed to share the same deep p^+ ring.

The source side of NMOS transistors with the n^+/p^+ overlap being the most efficient for transient voltage attenuation, this side has to be implemented towards the power device in order to protect the drain side. Since this attenuating effect is favourable in any transient situation, it is also important to locate the set of NMOS transistors protected with the deep p^+ ring between the set of PMOS transistors and the power device so that the negative transient amplitude, likely to be coupled to NMOS drains via PMOS drains, is reduced.

The elimination of the p^+-implant underneath the field oxide in

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the well does not allow interconnection routing over it and therefore, in order to connect the drain diffusions of two adjacent n-channel transistors, routing paths external to the well have to be implemented.

III. Conclusion

It has been shown that a simple CMOS/DMOS smart power technology can be made latch-up-free using a floating well concept based design methodology. This concept, already studied for VLSI CMOS technologies without great success, takes advantage of the additional diffusions required for the power device to improve smart power circuits latch-up immunity. In standard high-side switch applications, the total die area increase could be less than 10%, hence inducing a small reduction in fabrication yield. However, the proposed methodology permits to produce a high-side switch smart power technology using a single epilayer and only 10 mask levels in contrast to the 15 levels and the multi-epilayers of a junction isolated technology.

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Bright Organic Electroluminescent Devices with Double-Layer Cathode

Junji Kido, Katsutoshi Nagai, and Yoshiyuki Okamoto

***Abstract*—Electroluminescent devices were fabricated using a diamine derivative and Tris(8-quinolinolato)aluminum(III) complex as the hole transport layer and the emitting layer, respectively. The cell structure of glass substrate/anode/hole transport layer/emitting layer/cathode was employed. The anode was indium-tin oxide (ITO) transparent electrode, and the cathode was a double layer consisting of the first layer of Mg, or Li and the second layer of Ag. Intense bright green emission with luminance of 40 400 cd/m^2 was achieved at 18 V with a current density of 330 mA/cm^2 for the cell with the doped Al complex with 1 mol % of coumarin 6 and Li/Ag as the cathode.**

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J. Kido was with the Department of Applied Science, Brookhaven National Laboratory, Upton, NY 11973. He is now with the Department of Materials Science and Engineering, Yamagata University, Yonezawa, Yamagata 992, Japan.

K. Nagai is with the Department of Materials Science and Engineering, Yamagata University, Yonezawa, Yamagata 992, Japan.

Y. Okamoto is with the Department of Chemistry, Polytechnic University, Brooklyn, NY 11201.

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I. Introduction

Electroluminescence (EL) in organic crystals has long been investigated from fundamental as well as practical points of view [1]. The primary reason is that organic materials are known to have extremely high fluorescence quantum efficiencies in the visible region. For example, anthracene single crystal reportedly exhibits blue photoluminescence with a fluorescence quantum yield of 0.99 [2]. Practically, however, electroluminescence from such organic single crystal is less attractive due to their high drive voltage (over 100 V) requirement.

Recently Tang and VanSlyke introduced injection-type EL devices with organic thin films [3], [4]. They demonstrated that the use of a diamine derivative as a hole transport layer for hole injection from the anode into the emitting aluminum complex layer significantly improves the efficiency of the cell. In such double-layer EL devices, the injected holes and electrons each move toward the oppositely charged electrode, and they recombine in the emitting layer. In this case, the hole transport layer plays an important role in transporting holes and blocking electrons, thus preventing electrons from moving into the electrode without recombining with holes, which improves the recombination efficiency. In these devices, the luminous efficiencies are about 1.5 lm/W, which are comparable to those of light-emitting diodes or inorganic ZnS-type EL devices. They also showed that the employment of a low-work-function metal as a cathode provides low drive voltages for the cell.

Since such low drive voltage of the cell promises the practical application such as flat-panel displays, various research activities in this field have been initiated. Adachi and his co-workers later showed the utility of a variety of organic fluorescent dyes as emitter materials in EL devices [5]-[9]. They also developed other types of the cell structures such as a cell with a luminescent hole transport layer and an electron transport layer [7]. In this case, recombination of holes and electrons takes place in the emitting hole transport layer. Another structure consists of three layers of organic thin films in which a luminescent layer is sandwiched between a hole transport layer and an electron transport layer [8], [9]. We have recently demonstrated that the use of a terbium complex as a luminescent material gives extremely sharp green color EL [10] and that a europium complex affords a sharp red color EL [11]. We also demonstrated that polymers such as polysilane and molecularly doped polycarbonate are effective as hole transporting materials in a double-layer-type cell [12], [13] as well as in a single-layer-type cell [14].

Since electroluminescence is generated in all of the above systems by recombination of holes and electrons, it is essential to inject those carriers into luminescent medium. However, the organic materials used in EL devices are insulators or photoconductive. One should employ a low-work-function metal and a high-work-function metal as the cathode and anode, respectively, to reduce drive voltage. Tang *et al.* found that an alloy of magnesium and silver provides good cathode material for this purpose because the alloy system is more stable than magnesium cathode which is subject to oxidation [3]. Other advantages over pure Mg system are that the sticking coefficient of the alloy cathode is better than that of pure Mg and the introduction of Ag reduces the sheet resistance of the cathode. As a result, reproducibility of the cell performance is much improved.

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