

A Reusable Smart Interface for Gas Sensor Resistance Measurement

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Abstract—The advances of the semiconductor industry enable microelectromechanical systems sensors, signal conditioning logic and network access to be integrated into a smart sensor node. In this framework, a mixed-mode interface circuit for monolithically integrated gas sensor arrays was developed with high-level design techniques. This interface system includes analog electronics for inspection of up to four sensor arrays and digital logic for smart control and data communication. Although different design methodologies were used in the conception of the complete circuit, high-level synthesis tools and methodologies were crucial in speeding up the whole design cycle, enhancing reusability for future applications and producing a flexible and robust component.

Index Terms—Circuit synthesis, gas detector, mixed analog-digital integrated circuit.

I. INTRODUCTION

MONOLITHIC integrated gas sensors are mainly known through their use in environmental control, home security and because they are the main component in the development of the well-known electronic noses. These, through trying to mimic the human olfactory system by using an array of chemical sensors and the appropriate circuitry [1], have opened up multiple applications in the food industry, environmental monitoring, medicine, etc.

Gas sensors are one important application of CMOS-compatible microelectromechanical systems (MEMS) technology. Their response consists of a variation in the resistivity of the active material that depends on the mixture of gases present in the environment and on many other factors, especially the structural properties of the sensing film and the temperature of operation [2], [3]. They often need high temperatures to activate the sensing mechanism. Thermally isolated microhotplate structures are commonly used to achieve high temperature with the lowest possible power consumption [4].

Manuscript received June 30, 2003; revised March 17, 2004. This work was supported in part by the European Commission under Contract IST-99-19003 and in part by the Spanish Science Commission CICYT under Contract TIC-2000-1852-CE.

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Digital Object Identifier 10.1109/TIM.2004.831459

Although meeting the minimum requirements in many instances, current gas sensor technology suffers from a number of limitations, in particular poor selectivity and low stability over long periods. Improvement of stability requires fundamental research into material elaboration and characterization [5], [6]. Selectivity, however, can be improved by use of several sensors (an array of sensors) as an entire sensing unit.

With instrumentation electronics, the raw sensor signal can be transformed into a standardized representation. The combination of a sensor or actuator element with local electronics is known as a smart sensor. A smart sensor also checks and calibrates the signal, and transmits the result to its users via a communication protocol. In this framework, a smart gas sensor can be regarded as an electronic control unit (ECU) that is usually embedded in a larger system (for instance, a car, an airplane, an in-house fire detection system, etc.). This approach reduces the complexity of the system.

ECUs often have very tight cost margins, and at the same time there are demanding requirements on their performance, reliability and reusability [7]. These factors make top-down design methodologies, starting from high levels of abstraction that allow the application of high-level synthesis tools, very attractive [8].

In this paper, we present the development of an interface circuit for gas sensor resistance measurement. The paper is organized as follows: after the introduction in Section I, gas sensor structure is described in Section II. The interface circuit of the gas sensor system is proposed in Section III. In Section IV a detailed overview of digital design methodology with emphasis on the role of high-level synthesis tools is given. Section V explains relevant results. Finally, the conclusion is given in Section V.

II. GAS SENSOR STRUCTURE

Adsorption of gas species onto the surface of the sensing layer changes substantially its electrical resistance. In the case of semiconductor gas sensors, the usual range of working temperature for activating the sensing mechanism is between 200°C and 500°C [4]. These temperatures are usually reached by placing the sensing layers on a microhotplate manufactured with CMOS-compatible micromachining technology and distributing a resistance-based heater element around the sensors. By this procedure the central part of the sensor array, which is working at high temperatures, is isolated from the silicon bulk. To keep the microhotplate temperature stable, an efficient heater control scheme is also needed [9].

Gas sensors often respond to a wide range of gas species and are therefore only partially selective. To enhance gas selectivity,

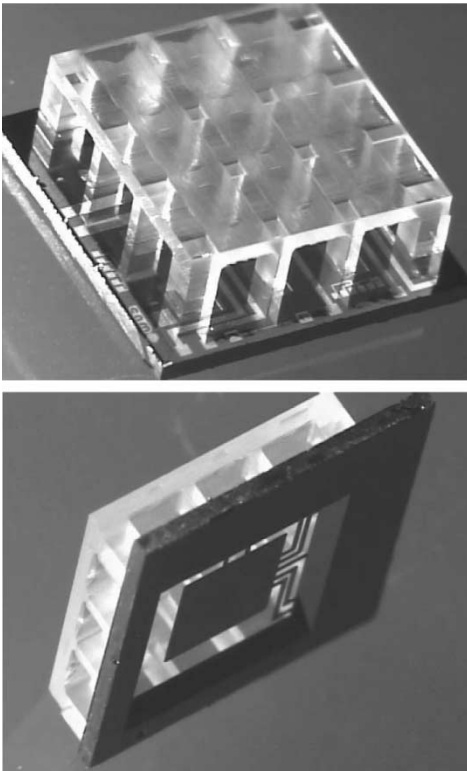


Fig. 1. Top and bottom view of one of the glass/silicon structures with a central platform for a four-sensor array.

multi-sensor structures with different active materials in each sensing resistance can be produced. Each active material has a different nominal resistance that has a specific resistance behavior in gas presence.

Large microhotplates are needed for proper placement and routing of the sensing devices. Their enhanced structure robustness is assured by use of a micromachined glass structure (Fig. 1) described elsewhere [10].

It is desirable to combine an array of gas sensors with integrated electronics to achieve different response signatures for different gases [11]. This requires an efficient interface circuit to select each channel, measure responses and send out the result in standard format.

III. SMART SENSOR ELECTRONICS

In this section, an interface circuit for sensor selection and resistance measurement is described. Although the complete interface design has both analog and digital circuitry, the first step is to fix the sensor readout method.

The nominal resistance of the sensing layers, measured in air at the adequate working temperature (R_{air}), depends on the geometric parameters and resistivity of the sensing layer. This value can range from a few $k\Omega$ to several $M\Omega$ [4]. When the layer is exposed to different gases, its resistance (R_{gas}) varies with gas concentration in air.

For instance, the nominal resistance of a WO_3 gas sensor can rise from $1 M\Omega$ in air to $200 M\Omega$ in air with 2 ppm of NO_2 [12]. SnO_2 films are usually used to detect CO: their resistance can

move from a few $K\Omega$ in air to $200 K\Omega$ when high levels of CO are present [13] (these reported values are of practical interest in environmental monitoring and exhaust ambience applications).

This means that, if an interface circuit is to be reused, it must be able to work under a wide range of nominal resistances (from a few $k\Omega$ to several $M\Omega$) and support relative resistance variations ($R_{\text{gas}}/R_{\text{air}}$) as high as 200 [12]. Accomplishing this huge measuring range is the main challenge in this block design process.

The various solutions in the literature usually work with fixed sensing materials that have known nominal resistances. Najafi *et al.* [14] use a current source to measure the voltage drop at the resistor. This solution is not useful for us, because for resistances of several $M\Omega$, the injected current must be in the range of pA, a level that cannot be controlled with standard CMOS technology. Another solution based on a logarithmic converter is given by Barretino *et al.* [15]. The range achieved with their system runs from a few $k\Omega$ to $100 k\Omega$, which again is too low. A more versatile system for measuring resistors between $5 k\Omega$ and $100 M\Omega$ is proposed by Ruedi *et al.* [16]. The measuring method is based on biasing the sensor at a constant voltage. The current provided by the biasing block is connected to an integrator. The measurement of the integrating time is proportional to the resistance and inversely proportional to the integrator capacitance. To select the resistor measuring range, adequate capacitors must be used.

The use of an oscillator-based interface is another interesting alternative [17]. The measurement signal, i.e., the period, is still essentially analog and related with the voltage across the sensor that causes a current to flow. This current charges the external capacitor, which converts the current back to a voltage. There are many advantages to this solution as follows:

- 1) There are few components, and so the design effort is lower than in the integrator-based circuit;
- 2) The influence of process variations is minimized;
- 3) Its operation is easier to control;
- 4) Output measurement is time-based.

Therefore, there is no need for analog-to-digital converters (ADCs) or other analog components. The oscillator is formed by an RC stage that includes the sensing resistor and an external reference capacitor and an odd number of integrated inverting stages.

A flexible digital block to process the oscillator output and convert the sensor resistance to digital format was designed in parallel. The resulting smart system transfers information to an external controller node using a standard communication protocol. The whole architecture is illustrated in Fig. 2.

A. RC Oscillator

As shown in Fig. 3, the core of the implemented readout circuit consists of a ring-oscillator formed by a chain of three inverter stages and a first-order delay stage made by the sensing resistor and an external capacitor C . By an adequate selection of the reference capacitor, we make the delay at the RC stage longer than the intrinsic delay of the inverting stages. Thus, we obtain an oscillator period with a dominant contribution from the RC stage, which is dependent on gas concentration.

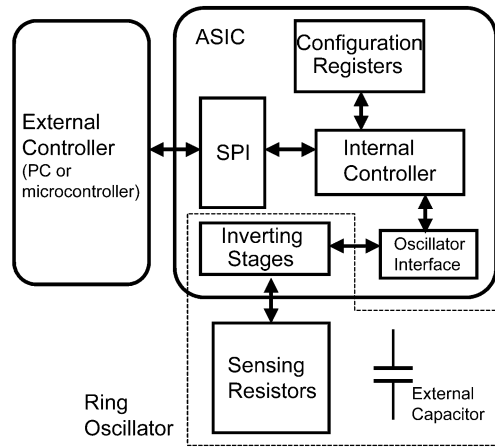


Fig. 2. Architecture of the smart sensor system.

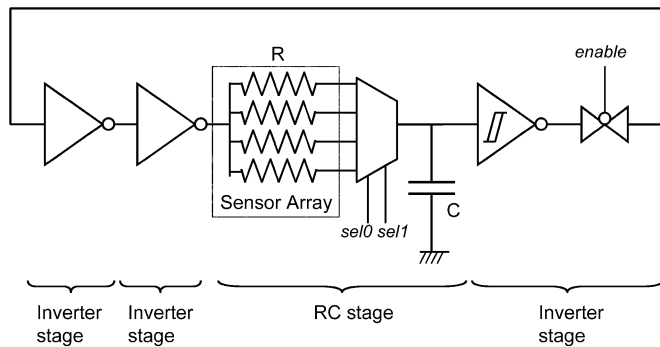


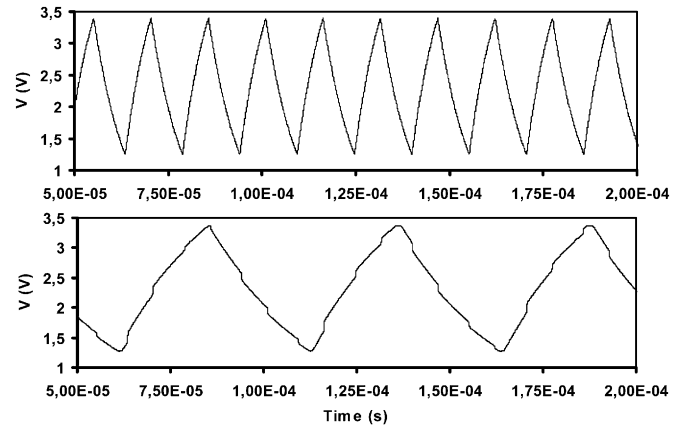
Fig. 3. Block diagram of the RC oscillator.

The inverter stages act as voltage threshold comparators which change the charge/discharge cycle into a time-based measurement. To reduce the delay dependence on the timing performance of CMOS inverters, we placed a Schmidt trigger after the RC stage. The four different resistors of the sensor array can be measured by choosing the value of the control inputs of a switch-based multiplexer. The resistances of these switches are generally three orders of magnitude less than the resistances of the sensing films and thus can be ignored. The advantage of this scheme is that only one ring-oscillator and an external capacitor are needed to measure the resistance changes of all the elements of the array. This block was laid out manually to optimize device matching and performance and to ensure low on-resistance in the switching transistors.

From post-layout simulations we found that the inverting stages introduce a delay of 250 ns. In order to overlook this contribution, the value of the capacitance was chosen to select a period range greater than 10 ms. Fig. 4 shows the output waveform for two different resistances (20 and 100 k Ω) for an external capacitor of 300 pF.

B. Digital Interface

The above results demonstrate that it is possible to interrogate a resistive sensor using an oscillator-based interface. The task now is to exploit the fully digital nature of the oscillator approach and design a cost-effective system for period measurement.

Fig. 4. Simulated oscillator output waveform for two different resistors: 20 k Ω (up) and 100 k Ω (down) ($C = 300$ pF).

The functions of the digital section are: 1) to convert the oscillator output period into an eight-bit digital format; 2) to transmit the resulting digital word; and 3) to receive control and configuration information through Serial Protocol Interface (SPI), a standard communication protocol. Sensor readout and analog-to-digital conversion works as follows:

- The protocol is used to define which sensing resistor will be read.
- The oscillator, properly configured with the desired sensing resistor, is connected to the enabling input of a digital counter. A second counter records the number of successive clock cycles during N periods of the oscillator.
- The resulting eight-bit output value is passed to a buffer that can be read by the SPI unit. To obtain accuracy to under 1% in the resistance value, the number of periods N , of the monitoring window is determined by the external processor (and programmed via SPI).

The system has been partitioned in four blocks:

- Oscillator interface:** This digital block is dedicated to processing the analog RC oscillator output signal. It captures the period of the oscillator in order to compute the sensing resistance. It is also used to switch to the target sensing resistance.
- SPI:** This block performs a serial peripheral interface (SPI) communication between the system and an external component. The SPI is essentially a three-wire serial bus for 8- or 16-bit data transfer applications. The three wires carry information between devices connected to the bus. In this application it runs in slave mode, but the design can be reused to run as a master.
- Internal Controller:** This block provides local control signals to the other blocks.
- Configuration Registers:** This is the memory used to store the SPI data and other signals relating to the sensor readout algorithm. Although in the version of the circuit shown, this block was implemented using D-type flip-flops (from the available standard-cell library), it is considered a RAM block in order to allow future upgrades.

C. Design Methodology

The digital block was designed using a top-down methodology starting from a high-level circuit description. This design strategy was chosen to enable the performances obtained with a given architecture to be evaluated, different solutions to be compared, and block reuse in future designs to be posed as a real possibility.

In addition, use of hardware description languages for design definition increases design flexibility, and the resulting system can be easily upgraded, for instance by adding new control or communication features.

This high-level design methodology can be seen as a set of successive refinement steps from a level of abstraction as high as possible to the details needed for the final implementation [18]. An overview of the design process for this specific system is now described.

First of all, the digital system was partitioned in four blocks. These blocks were designed at a behavioral level with Signal Processing Workbench of Cadence (SPW).

Once all functions were implemented at functional level, a behavioral simulator ensured that the whole system fulfills the desired specifications. At this point, the decision to implement the circuit in an ASIC was taken. (This circuit will be composed by digital standard-cells, full-custom analog blocks and analog library blocks). An RTL-level description of the system functions was designed and simulated using SPW.

Then, a Verilog RTL description of the digital system was extracted from SPW. A structural Verilog description at logic level was obtained using Synopsys. This description consists of a set of standard cells of the selected target technology.

The process concludes with the physical design: 1) The layout of the digital block of standard cells is obtained with automatic place-and-route tools of Cadence Cell Ensemble and 2) the resulting block is connected to the analog circuitry with a full-custom layout editor.

To sum up, a high-level design method was used to implement monolithically the smart sensor. A functional version of the design was simulated and validated at a high level of abstraction, and then a process involving various synthesis tools was followed to obtain the final implementation automatically. In this way, the digital part of the proposed system can be easily retargeted to an FPGA or executed by a microcontroller or a DSP.

IV. EXPERIMENTAL RESULTS

The final device, including the interface circuit and the heater controller to maintain the temperature of the sensing compound stable, was implemented using a $0.8\text{-}\mu\text{m}$ CMOS process of Aus-triamicrosystem. This technology incorporates the possibility of using bipolar and high-voltage devices. The circuit photograph is shown in Fig. 5. The circuit, in a JLCC68 package, occupies an area of 9.89 square millimeters and has 53 I/O pins.

The standard-cell digital block was successfully tested using a logic analyzer and a pattern generator. The voltage measured across the sensing resistor terminal is shown in Fig. 6. When the voltage across the sensing resistor achieves the threshold of the Schmitt trigger, a logic transition in the trigger occurs.

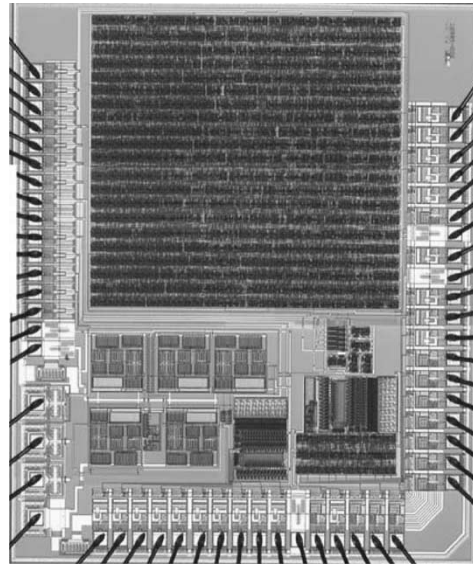


Fig. 5. Micrograph of the integrated prototype.

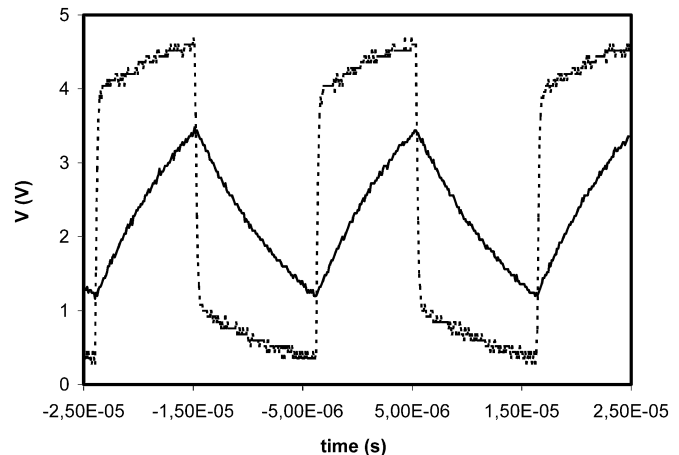


Fig. 6. Experimental measurements showing the voltage across the resistor (solid line) and the Schmitt trigger output (dashed line).

The oscillation period lasts for the delay of all the inverting stages plus the RC delay. As is seen in Fig. 7, the delay related to the inverter stages is 250 ns. Fig. 8 gives the oscillation period vs. resistance for an external capacitor of 330 pF and a resistance range of 10 k Ω –1.5 M Ω . An external capacitor of 3.3 pF is required to work in the range between 1 and 200 M Ω with a resolution lower than 1%.

V. CONCLUSION

We have discussed design methodologies and issues involving the conception of a smart gas-sensing system. In consequence, a specific mixed-mode integrated circuit containing the analog front-end electronics for measure of gas sensor arrays was developed.

Design partition led to well-specified individual blocks that can be easily reusable in future variations of sensing material composition or under different measurement scenarios. After consideration of alternatives for the measurement of sensing

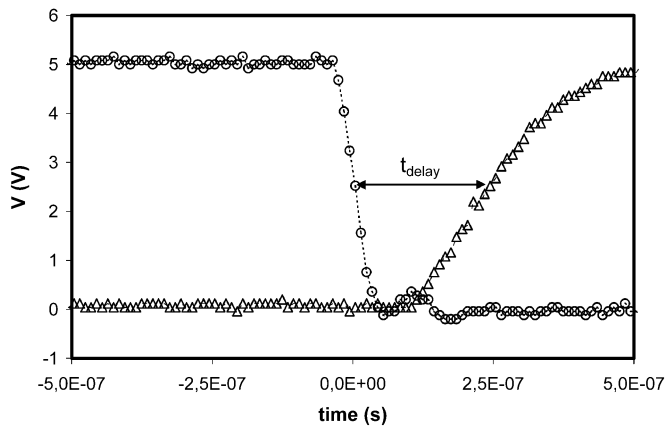


Fig. 7. Measurement of the delay related with an internal inverting stage. (o) Inverter input voltage, (Δ) output voltage. $t_{\text{delay}} = 250$ ns.

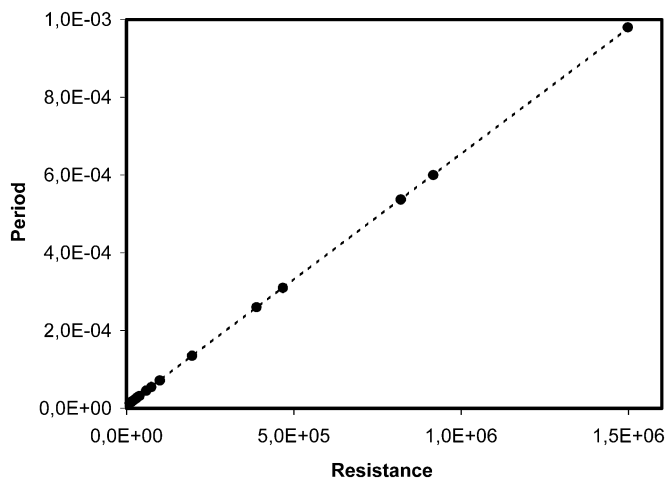


Fig. 8. Oscillator period vs. sensor resistance. Dots correspond to experimental result obtained with an external capacitor of 330 pF. The dashed line represents a lineal fitting: $P = 6.49 \cdot 10^{-10} R + 6.92 \cdot 10^{-6}$.

devices, a method based on the RC oscillator was chosen. This ensures measurement under almost all possible working conditions.

A digital interface based on SPI bus was chosen, allowing the control of the smart sensor by an external processor. This interface was designed using high-level techniques that allow block reuse and system upgrading. In addition, it has the advantage of creating as much of the design in the digital domain as possible. In this domain signal processing can be designed more quickly than in the analog domain, with robust behavior tools and without the influence of manufacturing process variation.

The component was manufactured in commercial high-voltage CMOS technology. Setting the oscillation period at around 1 μs with the help of an external capacitor made it possible to monitor resistance changes of two orders of magnitude with a resolution lower than 1%.

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