High Frequency Power Converter with ZVT for Variable DC-link in Electric Vehicles

By

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ABSTRACT

The most important metrics considered for electric vehicles are power density, efficiency, and reliability of the powertrain modules. The powertrain comprises of an Electric Machine (EM), power electronic converters, an Energy Management System (EMS), and an Energy Storage System (ESS). The power electronic converters are used to couple the motor with the battery stack. Including a DC/DC converter in the powertrain module is favored as it adds an additional degree of freedom to achieve flexibility in optimizing the battery module and inverter independently. However, it is essential that the converter is rated for high peak power and can maintain high efficiency while operating over a wide range of load conditions to not compromise on system efficiency. Additionally, the converter must strictly adhere to all automotive standards.

Currently, several hard-switching topologies have been employed such as conventional boost DC/DC, interleaved step-up DC/DC, and full-bridge DC/DC converter. These converters face respective limitations in achieving high step-up conversion ratio, size and weight issues, or high component count. In this work, a bi-directional synchronous boost DC/DC converter with easy interleaving capability is proposed with a novel ZVT mechanism. This converter steps up the EV battery voltage of 200V-300V to a wide range of variable output voltages ranging from 310V-800V. High power density and efficiency are achieved through high switching frequency of 250kHz for each phase with effective frequency doubling through interleaving. Also, use of wide bandgap high voltage SiC switches allows high efficiency operation even at high temperatures.

Comprehensive analysis, design details and extensive simulation results are presented. Incorporating ZVT branch with adaptive time delay results in converter efficiency close to 98%. Experimental results from a 2.5kW hardware prototype validate the performance of the proposed approach. A peak efficiency of 98.17% has been observed in hardware in the boost or motoring mode.

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TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Chapter 1

INTRODUCTION

1.1 Electric Vehicle Systems

In recent years, the automobile market has experienced a paradigm shift in favor of vehicles that have incorporated some degree of electrification. Electric Vehicles (EV) and Plug-in Hybrid Electric Vehicles (PHEV) have experienced a dramatic surge in sales over the past few years reaching over a million units sold globally in 2017, depicting a near four-fold increase since 2014. Of which, the share of new EV sales is nearly twice that of PHEV sales [1]. This dramatic increase in EV sales can be ascribed to growing concern for global climate change and conscious effort to reduce carbon dioxide (CO_2) emissions. The transportation industry accounted for 14% of global greenhouse gas emissions in 2010 that encouraged car manufacturers to push for electrification of the auto industry [2]. This chapter provides an overview of the modern EV powertrain architecture followed by a brief description of the stringent requirements for automotive DC/DC converters and a comparison of three different DC/DC topologies.

1.1.1 EV Powertrain Architecture

The typical block diagram of an EV powertrain is shown in Figure 1.1. An EV generally uses Fuel Cells, Batteries, Supercapacitors or a combination of these in place of an internal combustion engine (ICE) to provide energy to the drive system [3]. Generally, a Lithium-Ion (Li-Ion) battery pack is preferred as the primary source of energy in the Energy Storage

System (ESS) as described in [4] and [5]. The power electronics module includes a 3-phase inverter that converts the DC voltage supplied by the DC-link to 3-phase AC supplying the Electric Machine (EM). The most widely used electric machines are the permanent magnet synchronous motor (PMSM) and induction motor (IM). Permanent magnet machines are preferred in traction applications owing to advantages in high power density, compact size, and ease of control using existing power electronics technology for effective operation [6].

A simple drivetrain configuration can be achieved by directly connecting the battery to the DC/AC inverter to supply the motor, however, this approach results in various challenges including uncontrolled output voltage of the ESS with varying load and maintaining high DC-link voltage in the traction drive. A simple and highly efficient solution is to incorporate a DC/DC converter in the power electronics module that couples the ESS to the inverter stage. In doing so, the DC-link voltage can be optimized and controlled at various motor load conditions to achieve optimum efficiency that is completely independent of the state of charge (SOC) of the battery stack. Consequently, switching losses in the inverter can be reduced significantly by dynamically lowering the DC-link voltage under low load conditions. This is because, the voltage needed to control the motor at low speeds is much lower than the rated voltage level due to the speed-dependent back electromotive force. Lower voltages will reduce switch stress in the inverter and thus aid in minimizing switch losses. At high speeds, the voltage level can be boosted to a higher level to avoid field-weakening operation and reduce conduction losses due to negative d-axis currents in the motor windings [7]. The power flow occurs from

battery to the EM in motoring mode and vice versa during regenerative braking. Thus, power flow is bidirectional in the EV drivetrain.

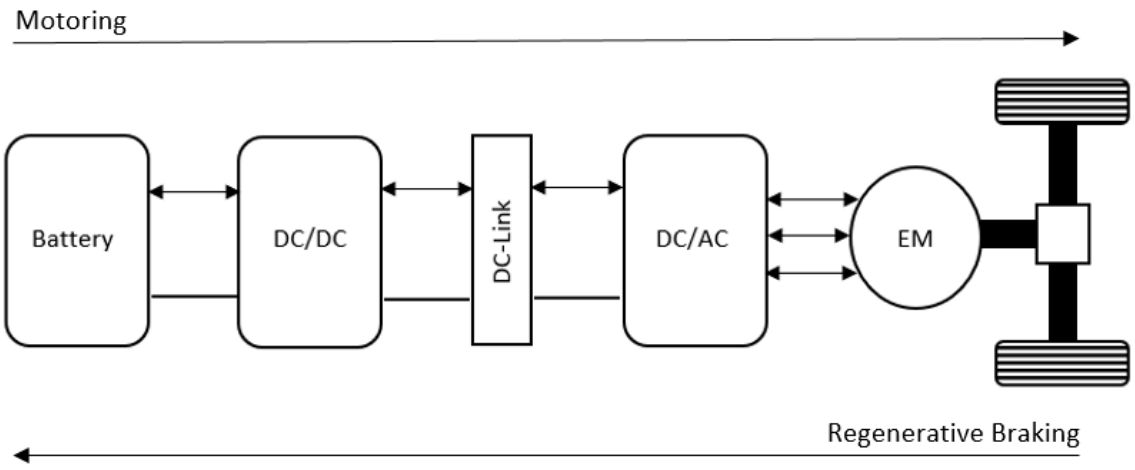


Figure 1.1: Block diagram of a typical EV powertrain

1.2 Automotive DC/DC Converter Requirements

Power electronic converters need to meet strict requirements to qualify for use in automotive applications. Some of the essential design constraints as outlined in [3] are listed below:

a. Light-weight and small volume

An important requirement for converters used in automotive applications is that they are light-weight and compact in size. This is essential because in EVs, the space for power electronics is often limited. Modern automobiles can have excess of 200 individual electrical loads including functions like headlamps, tail lamps, wipers, seat heaters, lighter, cruise control, engine control unit etc. [8]. These are generally supported by increasing number of point of load converters. With increasing number of functionalities, it is highly

advantageous to have a compact DC/DC converter occupying small volume in the EV. Furthermore, a converter that is light-weight is desired as it adds to the overall weight of the EV affecting range and efficiency of the vehicle. Thus, to meet size and weight requirements, high switching frequency is preferred in order to shrink the size of converter components.

b. High efficiency/high temperature requirements

The converter must withstand extreme temperature limits to ensure reliable operation under varied environmental conditions. The power electronic modules in EVs are required to tolerate high ambient temperatures often exceeding 125^{o}C and also temperatures dropping to as low as -40^{o}C depending on the mode of operation and geographical location [9]. In addition to ambient temperature, the operation of the converter at high power levels generate additional heat. This leads to rising junction temperature of the semiconductor devices that can result in damage to the operating devices. All components must be rated to endure these temperatures as well as retain the ability to operate reliably under harsh environmental conditions. Utilizing wide bandgap (WBG) devices such as Silicon Carbide (SiC) or Gallium Nitride (GaN) semiconductors that are capable of operating in extreme temperatures is desired. These WBG devices possess higher maximum operating junction temperature, higher breakdown strength, and better thermal conductivity when compared to traditional Silicon (Si) MOSFETs [10]. These WBG MOSFETs are able to achieve high efficiency even under hard switching conditions that helps reduce power dissipation in the switches and thus reduce the amount of heat generated. Nevertheless, utilizing soft-switching methods to further boost the efficiency is always sought after.

c. Low electromagnetic interference (EMI)

Another important constraint is the amount of EMI that the power electronic converter is allowed to generate. The Society of Automotive Engineers (SAE) have set strict limits on conducted EMI specified under standard J1113/41 that limit the ripple injected by the converter on to the voltage bus over the frequencies from 150kHz to 108MHz [8]. There are ways to tackle the conducted EMI issues through incorporating appropriate input EMI filters such as common mode chokes and proper attention given during design and circuit layout of the converter. Additionally, designing suitable low pass filters, proper grounding, and shielding all contribute to meeting the stringent EMI specifications.

d. Wide input and output voltage range

The converter will be connected to a battery stack whose typical voltage will range between 200V to 400V. The converter must be able to maintain constant output voltage at the DC-link, to supply the inverter with a steady voltage in spite of varying input battery voltage that will occur with changing SOC to ensure smooth operation. Furthermore, a variable DC-link dictates that the converter must be able to supply an output voltage ranging between a minimum of battery voltage up to a maximum of about 800V. The output voltage will be dependent on motor operating speed and the generated back electromotive force (emf). As the speed of the motor increases, the converter will need to supply a voltage that is higher than the generated back-emf to ensure high efficiency operation. All the power electronic components such as the switches and diodes in the converter must be rated for expected high voltage operation.

In addition to the requirements mentioned above, the converter is also expected to draw low input current ripple from the battery and have easy control corresponding to variations in input voltage and varying load conditions. The converter must be bi-directional, capable of operating in both boost mode during motoring and buck mode for regenerative braking to increase overall converter efficiency. Lastly, the converter must also have flexibility in interleaving that allows for easy power scaling. If a single converter is to be used for high power conditions, the size of the components increases and will also require a large heatsink leading to a big, bulky, and heavy converter. Interleaving allows for dividing the total power stress among multiple phases which leads to smaller components with lower current rating due to effective increase in switching frequency and splitting of the total input current.

1.3 Comparison of Different DC/DC Converter Topologies

A brief comparison of three different topologies for the converter is provided below. The benefits and drawbacks of each topology in relation with the mentioned requirements for automotive application is highlighted. The topologies under consideration are a synchronous boost converter, a full bridge converter, and the proposed interleaved bidirectional boost converter.

1.3.1 Synchronous Boost Converter

A conventional boost converter is modified by adding an additional switch in place of the main diode to achieve bi-directionality and potentially increase efficiency to obtain a synchronous boost converter. The advantages of this converter include low component count, easy control implementation, and no limitations on duty cycle range. However, this

topology requires that the output voltage is greater than the input voltage placing limitations on the DC-link range. Also, large variance between input and output voltage magnitude can impose severe stress on the MOSFETs leading to high current and voltage ripple issues [11]. This topology also requires large passive components leading to increased size and weight.

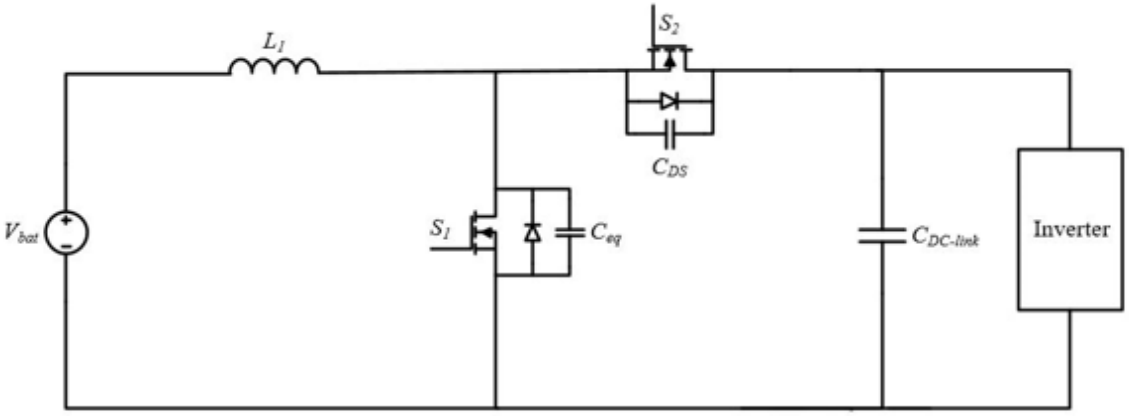


Figure 1.2: Schematic of synchronous boost converter

1.3.2 Full Bridge Converter

A full bridge topology is a common choice for EV DC/DC converter. It consists of four switches with additional switches added for bi-directionality on the secondary side of a high frequency transformer. This topology can both step up and step down the input voltage and thus does not restrict the DC-link range to a battery voltage minimum. This converter can also support a high conversion ratio. Electrical isolation is achieved with the addition of a transformer. However, the leakage inductance of the high frequency transformer resonates with the output capacitance of the transistor/diode causing ringing leading to high voltage stress across the semiconductor devices [10]. The number of switches in the

converter is also increased resulting in larger converter volume, more weight, and higher cost.

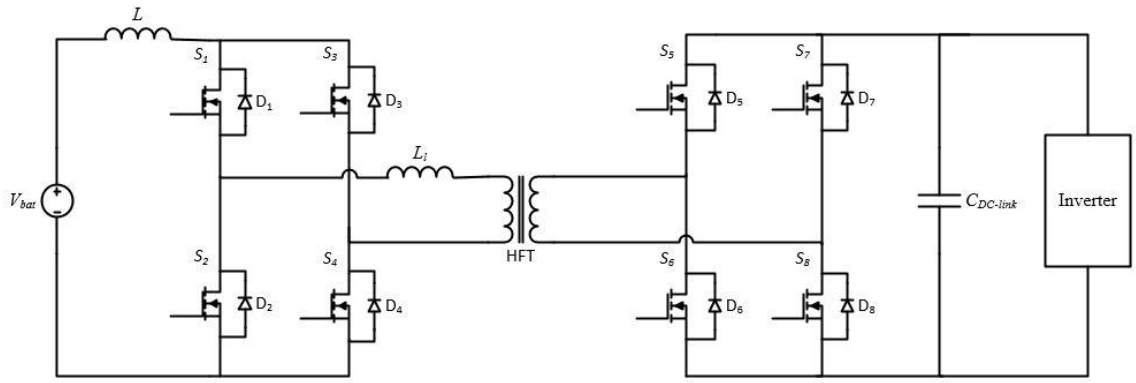


Figure 1.3: Schematic of bi-directional full-bridge converter

1.3.3 Interleaved Bi-directional Boost Converter

The proposed topology adheres to size, weight, and cost constraints along with maintaining flexibility for power scaling through interleaving and enhancing efficiency by utilizing WBG devices and soft-switching techniques. Interleaving synchronous boost converters reduces input and output current and voltage ripples, therefore minimizing the size and weight of the main inductors and DC-link filter capacitor. The low component count aids in reducing the cost of the converter while simplifying the control strategy. This robust topology is suitable to achieve a wide output voltage range and functions effectively for varying input voltages. Detailed analysis of the working principle with key waveforms is provided in Chapter 3.

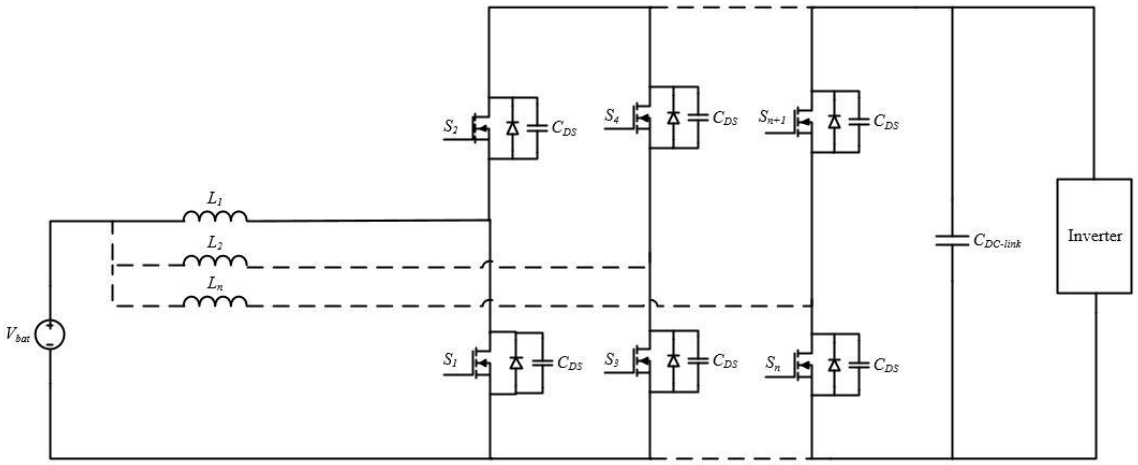


Figure 1.4: Schematic of interleaved bi-directional DC/DC converter

1.4 Review of Soft-Switching Converters

It is clear that DC/DC converters used in the powertrain of an EV face significant design challenges to achieve high power density and high efficiency under harsh environmental conditions while keeping costs low. The main inductor and capacitor are the primary energy storage components accounting for a significant share in the overall size and weight of the converter. The size or value of these components is inversely proportional to the switching frequency. Many conventional DC/DC topologies using hard switching, resort to high switching frequencies in an effort to reduce the size of the converter and increase power density. However, as switching frequencies get higher, so do switching losses leading to lower efficiency. Figure 1.5 shows the overlap of high voltages and currents causing switching loss in the converter. The relationship between switching loss and switching frequency is given in (1.1).

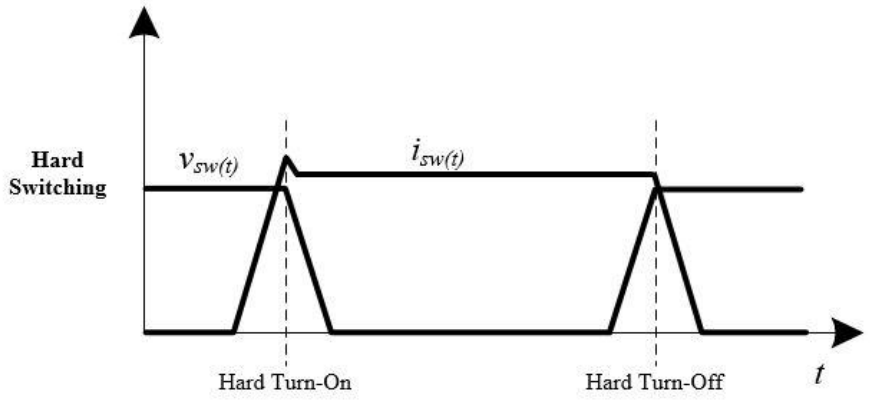


Figure 1.5: Hard-switching voltage and current waveforms

$$P_{sw} = \frac{1}{2} V_{DS} I_{DS} (t_{on} + t_{off}) f_{sw} \tag{1.1}$$

$V_{DS}\ (V)$: Drain-to-Source voltage across the switch
$I_{DS}\ (A)$: Drain-to-Source current flowing in the switch
$t_{on}\ (s)$: Rise time of the switch
$t_{off}\ (s)$: Fall time of the switch
$f_{sw}\ (Hz)$: Switching frequency

At switch turn on, the full load current is diverted into the switch under full blocking voltage. The diode reverse recovery current is also added at the trailing edge before the diode withstands the full reverse voltage and the switch fully turns on. During turn off transition, the switch voltage builds up at full current until the bypass diode of another switch picks up the current and the switch turns fully off. The overlapping voltage and current cause a large switching loss in accordance with (1.1). Additionally, device stress increases under hard switching and prolonged operation can lead to lowered switch reliability. Lastly, high dv/dt, di/dt and parasitic ringing under high switching frequencies create severe EMI issues that may interfere with control circuitry or sensitive components located in close proximity [12].

There are several possible solutions to tackle the problems of hard switching. Snubber circuits can be used to lower dv/dt and di/dt variations. This can result in some decrease in semiconductor device stress by limiting the rate at which the voltage rises across the switch or current falls through the switch to avoid overlap at peak values. This is achieved through RC or RL combination circuits and does not reduce the switching loss but simply transfers the loss to passive elements like a resistor rather than the switching device. A better and more efficient solution is realized through soft switching.

Soft switching methods can be classified as: (1) converters with resonant switches (quasi-resonant converters), (2) resonant transition converters including zero voltage transition (ZVT) and zero current switching (ZCS) and (3) load resonant converters. In resonant transition converters, resonance occurs only during the transition switching period. This resonance ensures that either the voltage across the switch or the current through the switch is brought to zero before the gate pulse is provided. Control for this class of soft switching can be achieved through fixed frequency. Quasi-resonant and load resonant converters have mostly sinusoidal voltage and current waveforms, i.e., resonance exists. This is generally undesirable. Additionally, these converters utilize frequency control which means the filters must be designed for low frequency which is the worst-case scenario, thus also undesirable. Therefore, the resonant transition converters are most favorable for high frequency switching DC/DC converters in automotive applications.

Soft switching techniques such as ZVT and ZCS ensure that turn-on and turn-off transitions occur under favorable conditions as mentioned above. This can be accomplished in many ways that generally include adding an auxiliary branch to the power stage. This

auxiliary branch will contain additional resonant circuitry like inductors, switches, and diodes that enable resonance between the auxiliary branch and parasitic output capacitances of the switches to realize ZVT and ZCS. This reduces switching losses, switch stress, can lead to lower EMI, and improve thermal management. Higher efficiencies and lower losses can be realized resulting in smaller heatsinks required for thermal dissipation. Consequently, the converters can be made smaller and lighter. Figure 1.6 shows switch voltage and current waveforms under soft switching condition.

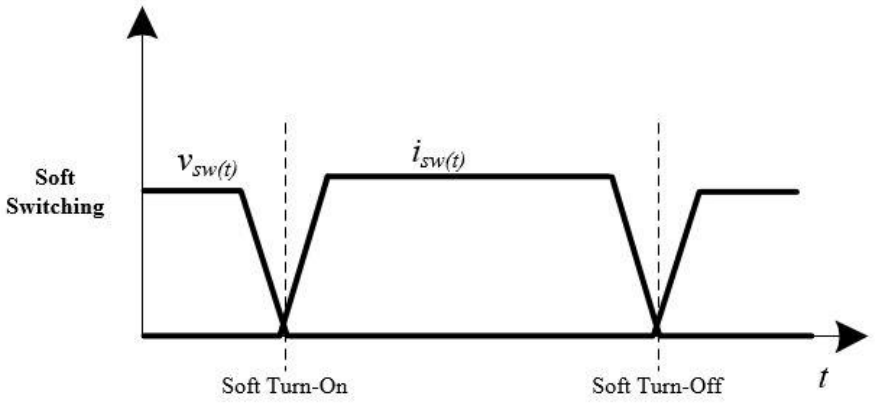


Figure 1.6: Soft-switching voltage and current waveforms

1.5 Objective and Organization of the Thesis

The objective of this work is to design and develop a high efficiency, bi-directional DC/DC converter for interfacing EV battery to an optimal variable voltage DC-link to supply a 3-phase inverter in the electric drivetrain. Careful consideration is given to achieving high power density and maximize efficiency by employing high switching frequency of 250kHz for a single phase of the DC/DC converter. Hardware prototype of 2.5kW is built using high voltage SiC switches to achieve efficiencies >98%. A new bi-directional ZVT circuit is implemented.

In Chapter 2, detailed literature review and analysis is presented outlining the benefits of incorporating a DC/DC converter in the electric drivetrain of the EV that can supply a variable DC-link voltage to the inverter. Referenced work supporting the optimization of the battery stack voltage, 3-phase inverter, and EV motor considering various drive cycles is provided.

In Chapter 3, a bi-directional boost DC/DC converter with soft-switching is proposed to interface the ESS with the inverter in the EV powertrain. The converter features include: (1) wide output voltage range, (2) bi-directional operation in both buck and boost mode, (3) single power pole for each phase leading to low parts count, (4) high power density, (5) easy power scaling and control, (6) ZVT for main and synchronous switch, and ZCS for auxiliary switches, (6) WBG devices with low on-state resistance switching at high frequency for maximized efficiency, and (7) short resonant current pulses in the ZVT circuit to keep conduction losses at a minimum. The working principle of the converter is outlined. The design process and loss analysis are presented for worst-case operating condition. Simulation results for boost and buck mode of operation are also provided.

In Chapter 4, a 2.5kW hardware prototype with the defined specifications is constructed and tested. The results for half power load and full power load are shown along with a summary of the performance obtained from the power analyzer. Soft-switching gate pulses are also displayed.

Lastly, the conclusion of the thesis work is presented in Chapter 5 along with suggestions for future work.

Chapter 2

OPTIMIZATION OF EV COMPONENTS WITH DC/DC CONVERTER AND VARIABLE DC-LINK

2.1 Introduction

In the previous chapter, the advantages of interfacing a DC/DC converter in the electric drivetrain of EVs was briefly outlined. This chapter delves into more detail of how the added degree of freedom helps in optimizing the battery stack voltage, the inverter, and the motor independently. Relevant literature has been reviewed advocating the various advantages which include the possibility of increasing system efficiency through a variable DC-link voltage and stepping up the battery voltage to a higher value that can potentially decrease conduction losses in the inverter and motor.

2.2 Variable DC-Link Voltage Range

The efficiency of the powertrain in an EV can be improved by augmenting the power electronics module between the battery stack and the motor with a DC/DC converter to ensure a stable voltage level at the input of the inverter for various different operation regions [13]. This configuration has been shown through multiple simulation results in [13] to improve system efficiency by controlling switching losses in the power electronic converters and iron core losses in the PMSM motor.

A power train with a variable battery voltage of 235 V to 350 V was designed. To reach the best compromise between the power electronic converter switching and machine losses, the requirement on the DC-link voltage is that it should be higher than the battery voltage

but at the same time, low enough to ensure that it does not significantly impact the machine core losses. For the selected battery voltage range mentioned above, a DC-link voltage of 600V was chosen in [13]. Having the DC/DC converter between the battery stack and the inverter is advantageous as it relaxes the design requirements for the PMSM machine. With the DC/DC converter in place, the machine does not have to be designed for the minimum battery stack voltage and the number of winding turns of the machine can be optimized to a wide range of phase voltages occurring because of the variable DC-link. Having the variable DC-link is also an advantage as it can dynamically vary the voltage supplied to the inverter based on the load requirements and thereby optimize system efficiency for a wide range of motor speeds.

A control strategy is developed in [13] based on the interaction of the DC/DC converter and the machine inverter to extract the optimum results from the Integrated Power Unit. The machine inverter has two defined regions of unique control regimes. For the base speed region, the Maximum Torque Per-Ampere (MTPA) methodology is followed while for higher voltage levels and thereby speeds, the field-weakening regime is followed. The control methodology for the DC/DC converter is such that it regulated both the inductor current of the boost converter and the output voltage across the DC-link capacitor. A cascaded control is used wherein the inductor current is controlled in the inner loop while the output voltage is controlled in the slower, outer loop. The symmetrical optimum regime for the control of the DC/DC boost converter is followed. Through this control scheme, it is made sure that the DC-link voltage operates within a pre-defined range governed by the battery voltage and the machine characteristics. Efficiency of the proposed system for low

speeds was tested in [13] and it was shown that low DC-link voltages at low speeds resulted in the least system losses. The tabulated results are as follows:

Table 2.1: Motor and inverter efficiency improvement through reduced DC-link [13]

Efficiency at low speeds	**DC-link Voltage**		
	400V	**300V**	**200V**
Machine	95.8%	96.1%	96.9%
Inverter	86.3%	86.9%	87.4%

This approach is further tested in [14] that compares the performance of two EV powertrains; one with a variable DC-link voltage, and the other with a constant DC-link voltage for a number of different operating conditions. In this case, the EM used is an induction motor as opposed to a permanent magnet motor and the difference between the drive train topologies is that the first configuration P1 uses a constant DC-link voltage and configuration P2 employs a DC/DC converter with variable DC-link voltage. The second configuration is similar to the setup in the experiments carried out in [13]. This test provides quantitative results supporting the concept that higher system efficiency can be achieved if the DC-link voltage is variable and is lowered for low speed operation and then increased for high speed operation. The calculation of the DC-link voltage, as carried out in [14], is based upon the motor synchronous speed (ω_s) in rad/sec, the number of poles of the machine (p), the stator flux linkage (φ_s) and a marginal voltage (V_m) to adapt the relationship from a PMSM to an induction motor. The equations described in [14] are given below:

$$V_{DC} = \sqrt{3}(\omega_s p \varphi_s + V_m) \tag{2.1}$$

$$V_m = I_s R_s \tag{2.2}$$

To set up the experiment, a 1.1kW induction motor is in one case driven by a constant DC-link voltage of 320V to mimic a battery through an inverter (P1) and in the second case (P2), a Cuk converter shown in Figure 2.1 with the specifications reproduced in Table 2.2 is added between the constant voltage source and the inverter.

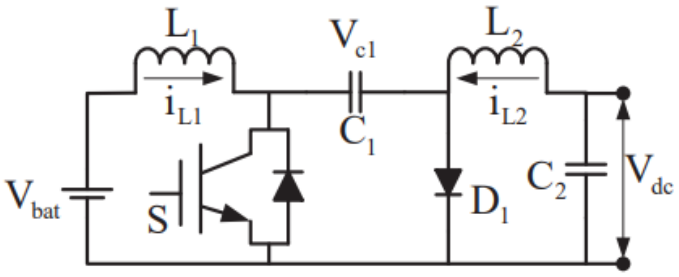


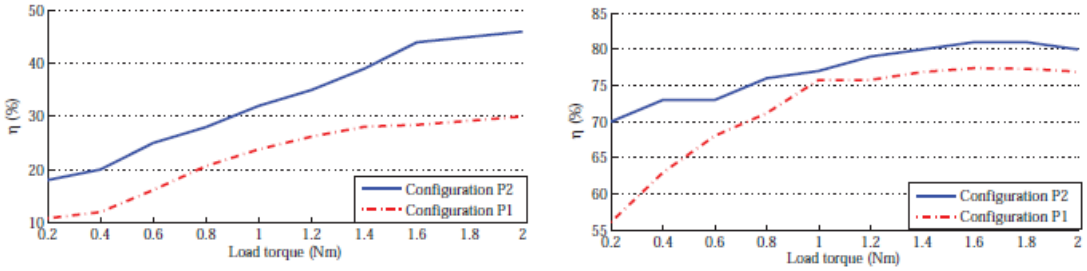
Figure 2.1: Schematic of Cuk converter [14]

Table 2.2: Cuk converter design specifications [14]

Parameters	**Value**
Switching Frequency	50kHz
Inductor (L_1)	1mH
Inductor (L_2)	1mH
Coupling capacitor (C_1)	0.6
Output filter capacitor (C_2)	8μF

The results obtained from the experiment show that the minimum efficiency improvement for the inverter from P1 to P2 was from 50% to 78% at speeds lower than 500RPM and low torque condition, while the maximum efficiency increased to 97.3% from 88.3% at high load torque and high speeds over 1500RPM [14]. The main factor contributing to these results is the reduction in the losses associated with the switching and conduction of the switches as reduced controlled voltages appear across the switches in the second configuration, P2. The efficiency of the induction motor was shown to improve

from 81.6% to 88.7% for speeds greater than 1750RPM. Again, as in [13], the greatest efficiency impact is for low speed operating points as the variable DC-link voltage can be lowered to ensure that the iron core losses are minimized for lower speeds. The individual improvements in efficiency for the inverter and the motor are then also reflected in the overall system efficiency which improves from 71% to 76% for high speeds over 1800RPM. The experiments performed in [14] also make a comparison between efficiency improvements with a variable DC-link at low speeds versus high speeds. It is shown that efficiency of all system components increases with an increase in motor speed and torque as the output power becomes dominant with respect to system losses. Two unique cases of 250RPM and 2500RPM are tested to establish concrete results supporting this theory.



(a) (b)

Figure 2.2: Comparison of system efficiencies for powertrains P1 and P2 at (a) 250RPM (b) 2500RPM [14]

In [15], Tenner et al further the discussion and include additional advantages of including a DC/DC converter in the powertrain other than improvement of system efficiency. These include energizing the motor of a given rated voltage from a battery of a much smaller voltage, a reduction in the series connected cells and balancing network of the battery stack and an adjustment of the output voltage of the battery corresponding to

the state of charge and the operating condition of the machine. To reduce the system losses, an algorithm is proposed to calculate the optimal values for motor reference currents I_d and I_q and the DC-link voltage. These optimal values are generated for varying operating conditions such as speed and torque as well as the SOC of the battery.

When the motor is supplied from a constant DC voltage source through an inverter, the line to line voltage limit of the motor is exceeded for high speeds when the optimized current reference values described above are used. This results in unnecessary high voltage stress on the machine and the inverter which, subsequently results in higher losses. One way to reduce this stress during high speed operation is to select a battery with a lower output voltage while the more practical and flexible approach is to add a DC/DC converter in the powertrain. The DC/DC converter does not only reduce the voltage stress on the system during high speed operation but also makes such an operating point achievable in case the battery voltage drops below a certain threshold as a result of a reduction in the SOC. The control strategy proposed in [15] is based on the conventional field-oriented control. The motor reference currents are generated for a given value of torque, machine speed and battery voltage. A non-linear optimization problem is applied to the relationship between the reference motor currents, as well as the DC-link voltage as an additional degree of freedom, and the reference torque to get the minimum solution to the objective function and the associated constraints. The authors in [15] have used the Monte Carlo algorithm to solve the stated minimization problem. Results for the losses of a traction drive with and without the DC/DC stage have been plotted.

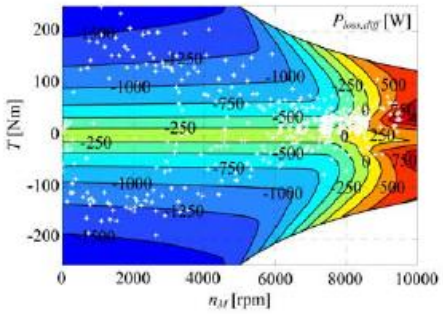


Figure 2.3: Loss difference between a system with and without DC/DC converter: $P_{loss,diff} = P_{loss}(300V) - P_{loss}(400V)$ [15]

The battery voltage used for the test cases was 300 V. As concluded in the previously reviewed papers, experiments with the DC/DC converter show significant reduction in losses for lower speed operating points. This is primarily due to reduced switching losses. For higher speeds, however, since the given battery voltage is insufficient, the voltage must be boosted by the DC/DC converter which incurs greater switching losses leading to a reduction in system efficiency. Therefore, the area of efficiency advantage shifts to lower speeds in a scenario when the battery voltage must be boosted with a significant duty cycle to provide higher DC-link voltage for high speed operation. Consequently, a method to determine the optimal battery voltage to increase the number of operating points occurring within a region of improved efficiency operation is proposed in [15].

Jia et al have proposed a control strategy for a bi-directional DC/DC converter for EV applications in [16]. Compared to the previous control strategies where the detection of the operating mode is necessary to determine the control loop, [16] proposes and then sets up a prototype that controls the DC-link voltage independent of whether the vehicle is in driving or regenerative braking mode

As with previous cases, the outer loop is the DC-link voltage loop while the inner loop is the inductor current loop. Both controllers are realized using conventional PI regulators. Using the same scheme in both modes of operation makes it easy to realize the control design. The voltage stress on the power electronic devices is always clamped as well as the DC-link voltage is always adjusted to suppress any variations during transients. The results obtained in [16] show that the proposed control strategy is a viable solution for multimode operation of the electric vehicle in terms of system stability with the only drawback being minor fluctuations in the DC-link voltage for a period on the order of milliseconds when the operating mode changes between the driving mode and the regenerative braking mode.

Furthermore, having a variable DC-link not only improves the overall system efficiency by limiting the losses within the system, especially the switching losses in the power electronic devices, but also contributes to a more durable system at higher torque operating points by improving the thermal reliability of the switching devices [7]. The control strategy presented in [7] aims to achieve active thermal management by maximizing torque output as well as system efficiency while having electro-thermal constraints.

The motivation for active thermal management comes from the fact that in urban traffic, the electric vehicles are expected to be operated at high torque and low speeds for prolonged periods of time. This decreases the modulation frequency for equal torque outputs and therefore power cycling becomes more apparent. The IGBTs are provided with a large chip surface and thereby a smaller junction-to-case thermal resistance to withstand the thermal impact but the body diodes can be undersized and become problematic at low

speed operation when the dominant load is on the diodes and not the switches. The diodes in such a case are most prone to failure as they continuously conduct the largest DC phase current [7]. A simple remedy to this problem is to set a static limit on the current in the motor controller, however, since this current will correspond to the worst-case load conditions, the performance of the system for non-worst-case loads will be affected as the torque will be restricted in such cases without the thermal limits actually being breached. On the contrary, setting a dynamic current limit in the motor controller by taking actual temperature feedback can ensure that system torque limits are not restricted when diode or IGBT thermal limits are not reached and therefore system performance is not compromised when catering to reliability needs at low speeds and high torques. It is concluded that a dynamically varying DC-link has significantly reduced losses in the inverter and motor compared to a conventional fixed DC-link topology. The reduced losses imply lower switching device temperatures facilitating high torque operation with increased reliability [7].

2.3 Li-Ion EV Battery Stack Voltage

An analysis of the EV battery stack voltage has shown about a 40% reduction in the battery stack voltage due to cumulative discharge and vehicle acceleration for a vehicle operating in the US06 operating range for just over 50 miles [17]. This will impact the performance of the traction system. This is illustrated in Figure 2.4.

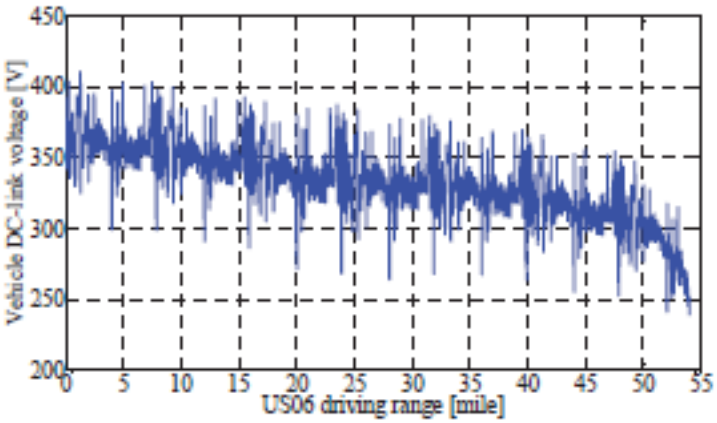


Figure 2.4: Reduction in battery voltage under US06 drive cycle [17]

The field weakening capability of a machine is severely limited at low voltages and for a given case, i.e. 240V, even adjusting the phase current magnitude does not render the machine capable of satisfying the requirements on torque and power during high speed operation at 10000RPM [17]. The Nissan Leaf traction machine is used as a benchmark EM to assess performance variations under changing DC-link voltages and temperatures. If the Nissan Leaf IPM operates at the lowest DC-link voltage that is connected directly to the battery, then the machine torque is limited to less than half of the rated value at high speed operation. However, the inclusion of a boost DC/DC is successful in maintaining the DC-link voltage at a constant value meeting the requirements even when the resultant back-emf is higher than anticipated due to temperature variations [17]. In addition to the primary objective of this work, it is also therefore imperative to have a DC/DC converter in place between the battery stack and the inverter to ensure the system meets the performance requirements at all operating points while a noteworthy reduction in system losses is achieved.

The battery stack voltage in the ESS can thus be selected based on different criteria. If a lower battery voltage is selected, higher efficiencies can be achieved at low speeds. And, a conventional boost converter with just a step-up operation can be utilized to step up the battery voltage when the motor is operating at or above base speed. The advantages of this converter include: low component count, lower switching losses, and easier control. Furthermore, this option allows to reduce the battery size while independently controlling the inverter supply voltage according to the operating point of the motor [18]. On the other hand, if a battery voltage close to the system rated voltage is chosen, then maximum efficiency is achieved at high speed values. In this case, using a conventional boost converter will be unable to fully utilize the DC-link range as it will be limited by battery voltage. A different topology capable of both step-up and step-down voltage operation will have to be selected. This may lead to increased size, cost, and complexity. This thesis considers the former approach of using a bi-directional boost converter.

A reasonable conclusion that the system voltage (inverter input voltage) needs to be proportional to the back EMF generated by the PMSM has been made in [18]. This relationship ensure that the system losses are kept to a minimum for the given operating condition which is dictated by the back EMF generated by the motor. The following Figure 2.5, reprinted from [18], shows how the system operating voltage varies in accordance with the mechanical speed of the motor.

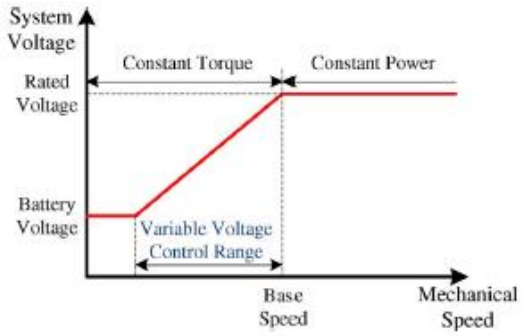


Figure 2.5: Required system voltage with variable-voltage control [18]

For low motor speeds up until a threshold value, the output voltage from the DC/DC converter will be the same as the battery stack voltage to minimize system losses by ensuring lower switching losses in the inverter and significantly lower core losses in the motor as opposed to the condition where a higher voltage is supplied to the inverter. During the constant torque region and for speeds lower than the base speed value, the DC/DC converter linearly increases the supply voltage of the inverter along with an increase in speed. Once the base speed is reached, the constant power region begins, and the inverter supply voltage is now the rated system voltage.

An added layer of efficiency improvement can be implemented within the same topology if the motor load level is taken into consideration when developing the control strategy for the inverter supply voltage, or the DC/DC converter output voltage. According to [18], if the inverter space vector PWM modulation index is used to determine the system voltage, thereby ensuring that the DC/DC converter outputs a voltage value that maintains the inverter modulation index at a predefined reference value for the least amount of losses, the system efficiency can be improved even further. This is possible as the control strategy

will allow for the system voltage to be controlled dynamically and with greater precision depending on the motor operating conditions.

Other important factors to consider are the driving profile of the EV and the motor's torque-speed characteristics. By correlating these along with the corresponding line-to-line voltage required at different operating points, a useful range of DC-link voltages can be determined. For example, reference [15] provides a graph of optimal peak line-to-line voltages for an IPMSM system that is directly connected to a 400V battery stack shown in Figure 2.6. It is evident from the graph that the required input voltage to the electrical machine for increasing speeds varies from $50V_{LL,pk}$ to $400V_{LL,pk}$, at which the voltage limit of the inverter is reached.

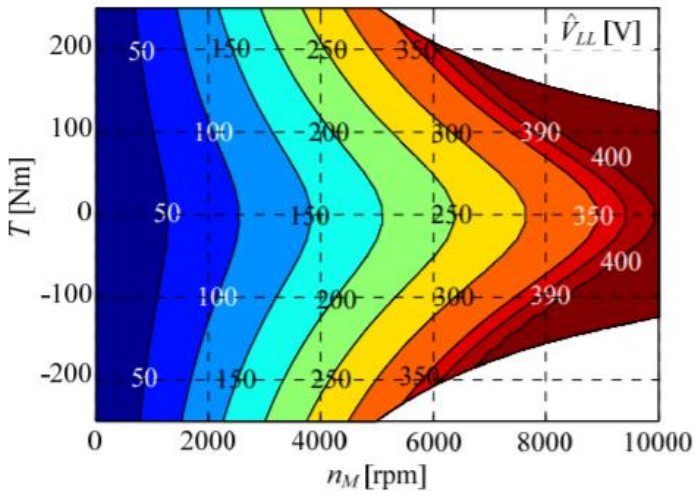


Figure 2.6: Optimal line-to-line voltage of the IPMSM for a system without DC/DC converter and V_{Bat} = 400V [15]

Thus, the battery voltage can be selected to reduce the total losses of the drive system for a given driving cycle. The resulting improvement in efficiency increases the

EV's cruising range as well. Most urban driving cycles reside in the low line-to-line voltage area of operation representing low speeds and stop-and-go traffic, while the US06 Supplemental Federal Test Procedure represents more aggressive driving behavior in the higher voltage range (highway cycle) at high speeds with high acceleration as shown in Figure 2.7. Reference [15] provides the required operating battery voltage for various driving cycles. Here, it is shown that 300V battery voltage is optimum for US06 driving profile. For other driving cycles represented by FTP-75 and NEDC for city driving conditions, using a boost DC/DC converter to reduce the battery voltage level needed has led to energy savings of 16.78% and 13.43% respectively. A battery voltage of 125V was chosen for NEDC and FTP-75 driving cycles, although, higher speed driving profiles result in larger currents and losses. Therefore, battery voltage must be picked to balance both drive cycle extremes with due consideration given for the worst-case condition. Consequently, a maximum battery stack voltage of 300V was chosen for the purposes of this thesis work.

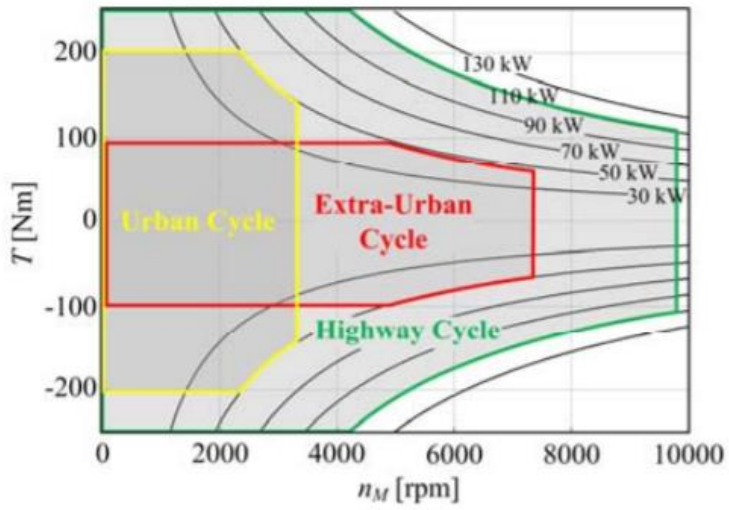


Figure 2.7: Operating points of different driving cycles [15]

2.4 Inverter Optimization

The main traction inverter in the electric drivetrain of an EV is a key component as it controls the electric motor and determines driving behavior. It is also responsible for capturing energy released through regenerative braking and feeding it back to the battery. Consequently, the efficiency of the inverter plays a crucial role in governing the range of the vehicle. Therefore, the inverter should be designed to minimize switching losses and maximize thermal efficiency.

A majority of traction inverters in EV/HEV use IGBT devices with antiparallel diodes due to their high voltage and current capability, low on-state resistance, and low thermal impedance. The total power losses of the semiconductor device can be categorized under conduction losses and switching losses. Conduction losses arise as a result of the IGBT's DC electrical characteristics while the device is in the on-state. These losses are a function of the current passing through the device. Switching losses are a function of the switching

frequency, the current in the device, and the device's dynamic characteristics [19]. Thus, the power losses to a large extent depend on the modulation techniques used to control the traction inverter.

The primary objective of the work detailed in this thesis is to show how a DC/DC converter providing a variable DC-link voltage for different modes of operation of the traction motor can lower the total losses and consequently increase the system efficiency. However, the inverter, which takes this variable DC-link voltage as the input and then generates a three-phase output for the IPMSM must be modelled and then verified to ensure that the total system losses, including the inverter losses, decrease under the proposed strategy. For this analysis, a benchmarked system derived from the Oak Ridge National Laboratory's Annual Merit Review establishing several performance parameters for the inverter and the motor in Nissan Leaf's drivetrain is used as base reference [20].

Figure 2.8 shows the overall drivetrain starting from the battery stack, including the DC/DC converter, the three-pole inverter and the electric motor.

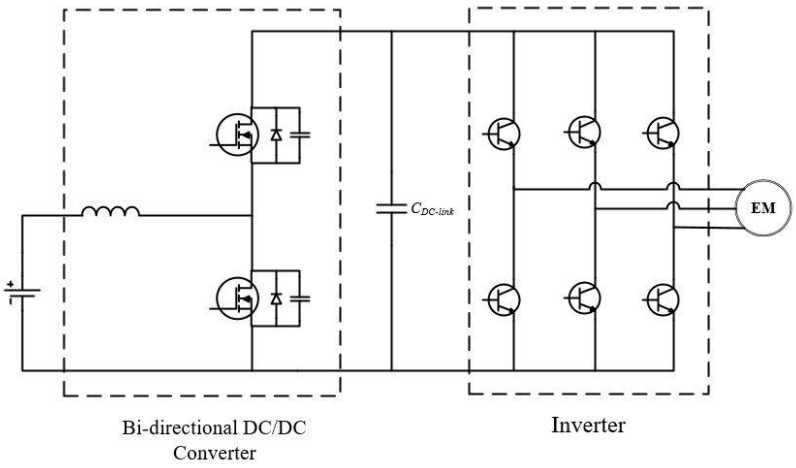


Figure 2.8: Electric drivetrain of EV consisting of battery pack, DC/DC converter, inverter, and motor

In this calculation, it is assumed that Sinusoidal Pulse Width Modulation (SPWM) technique is used to control the switching action of the three-phase inverter. This method treats each 'leg' of the inverter as an independent phase consisting of a pair of IGBT switches and diodes. Each leg is then pulse width modulated using a sine wave function compared to a high frequency triangle wave carrier. In this case, the carrier frequency is set to be 5 kHz. The phase current for the motor and duty cycle are given by the following equations:

$$I_{\phi} = I_{\phi,pk} \sin(\theta) \tag{2.3}$$

$$d(\theta) = \frac{1}{2}[1 + m_a sin(\theta + \phi)] \tag{2.4}$$

Where, m_a is the modulation index varying between 0 and 1. The phase current for the motor lags the phase voltage by angle ϕ.

Conduction losses:

The conduction losses ($P_{cond,inv}$) for the IGBT (P_{CT}) and the diode (P_{CD}) are described by the following equations:

$$P_{CT} = u_{CE0} I_{\phi,pk} \left(\frac{1}{2\pi} + \frac{m_a \cos(\phi)}{8}\right) + r_C I^2_{\phi,RMS} \left(\frac{1}{8} + \frac{m_a \cos(\phi)}{3\pi}\right) \tag{2.5}$$

$$P_{CD} = u_{D0} I_{\phi,pk} \left(\frac{1}{2\pi} - \frac{m_a \cos(\phi)}{8}\right) + r_D I^2_{\phi,RMS} \left(\frac{1}{8} - \frac{m_a \cos(\phi)}{3\pi}\right) \tag{2.6}$$

$$P_{cond,inv} = P_{CT} + P_{CD} \tag{2.7}$$

$u_{CE0}\ (V)$: IGBT collector-emitter forward voltage
$I_{\phi,pk}\ (A)$: Peak amplitude of sinusoidal current
$I_{\phi,RMS}\ (A)$: RMS of sinusoidal current
m_a: Amplitude modulation ratio
$\phi\ (rad)$: Phase shift angle between the sinusoidal current and voltage
$r_C\ (\Omega)$: IGBT on-state resistance
$u_{D0}\ (V)$: Diode forward voltage drop

r_D (Ω): Diode on-state resistance

Switching Losses:

The switching losses ($P_{sw,inv}$) for the IGBT during turn-on ($P_{sw,on}$), turn-off ($P_{sw,off}$), and reverse recovery for the anti-parallel diode (P_{rec}) are given by:

$$P_{sw,on} = \frac{1}{2} E_{on} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.8)$$

$$P_{sw,off} = \frac{1}{2} E_{off} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.9)$$

$$P_{rec} = \frac{1}{2} E_{rec} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.10)$$

$$P_{sw,inv} = P_{sw,on} + P_{sw,off} + P_{rec} \quad (2.11)$$

E_{on} (J): IGBT on-switching losses at nominal voltage and rated current
V_{dc} (V): DC-link voltage
V_{nom} (V): Nominal voltage at which E_{on} is defined
f_{sw} (Hz): Switching frequency
E_{off} (J): IGBT off-switching losses at nominal voltage and rated current
E_{rec} (J): Reverse recover energy for diode

Total Inverter Losses:

$$P_{total,inv} = 6(P_{cond,inv} + P_{sw,inv}) \quad (2.12)$$

To calculate the inverter losses, Infineon FS820R08A6P2B IGBT module is used. This module has a current rating of 820A which meets the 615A peak phase current of the Nissan Leaf IPM motor. The IGBT's specifications are summarized in Table 2.3. IGBT voltage U_{CE0} and body diode voltage U_{D0} are obtained from IGBT characteristic curves I_C vs V_{CE} and I_f vs V_f in the datasheet respectively. The device resistances r_c is calculated from the slope of the I_C vs V_{CE} characteristic curve and r_d is obtained from the slope of the I_f vs V_f characteristic curve. Using the inverter loss equations stated above, the speed of the motor

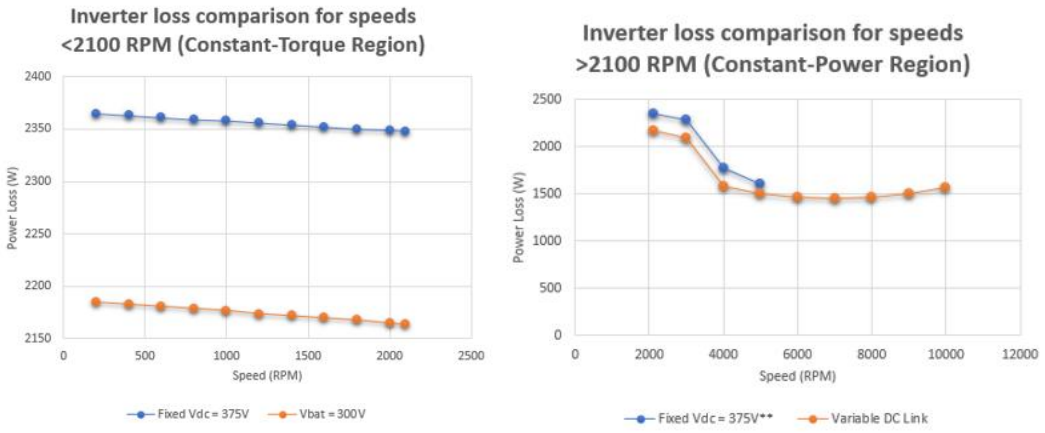
is manipulated by varying the amplitude of the input voltage waveform to the motor. The modulation index, m_a is calculated accordingly for varying DC-link voltages to generate the required voltage at the output of the inverter for different speeds. The modulation index is limited to 1, therefore input voltage to the inverter is supplied accordingly to avoid over-modulation. The losses obtained by variable DC-link of 300V to 470V condition are compared with losses incurred for a constant DC-link voltage of 375V. The results depicting the reduction in inverter losses under the variable DC-link case are shown in Figure 2.9.

Table 2.3: Datasheet parameters of IGBT FS820R08A6P2B

Parameter	IGBT FS820R08A6P2B
V_{CE}	750V
I_C	820A
V_{GE}	15V
U_{CE0}	0.7595V
r_c	8.493e-4Ω
U_{D0}	1.06V
r_d	6.6925e-4Ω
E_{on}	17.5e-3J
E_{off}	29e-3J
V_{nom}	400V
Q_{rr}	40e-6C

The loss analysis of the inverter in Constant Torque region shows that at speeds below the motor's base speed, the required line-to-line voltage to be supplied to the motor are well below the constant DC-link voltage of 375V. Therefore, using the battery voltage to operate the motor results in lower losses in the inverter. As the speed increases beyond 5000 RPM, the required motor voltage increases beyond the supply capability of 375Vdc. Operation at high speeds of 6000 to 10000 RPM will require the original drivetrain

topology to resort to flux weakening schemes. This however, leads to increased losses in the motor windings. In this mode of operation, many harmonics arise on the motor teeth causing a significant increase in iron losses. This is mainly a result of increased Eddy current losses which becomes predominant in field weakening mode [21].



(a) (b)

**Beyond 5000 RPM, Fixed DC-link of 375V is unable to supply the required voltage to the motor and field weakening schemes have to be employed
* Motor (280 Nm, 80 kW) data from ORNL report

Figure 2.9: Inverter loss comparison with variable DC-link of 300V to 470V and constant DC-link of 375V in (a) constant-torque region (b) constant-power region

2.5 Motor Optimization

A summary of results from literature that show how EMs respond to changes in voltage levels at the same output power in terms of motor losses is covered in this section. In a PMSM machine, the field produced by the magnet poles on the rotor is constant. Once the motor is excited, current will flow through the stator which will induce an additional magnetic field onto the rotor through the air gap flux between the rotor and stator. The strength of this magnetic field will depend on Faraday's law of magnetic induction and will result in direct axis currents in the rotor. The reference value of this direct current in the

field weakening method is kept at zero to minimize reactive power and maximize the torque per ampere (MTPA) utilization. Therefore, MTPA ensures that the required torque level for a given mode of operation of the PMSM is generated at the lowest possible stator current magnitude. However, negative direct axis currents must be injected into the stator to run the motor above rated value when the input phase voltage to each stator winding is limited. The direct current should therefore be negative as the total field inside the PMSM equals the sum of the induced field or the induced direct axis currents in the stator and the constant permanent magnet fields [22]. Figure 2.10 shows how the system voltage, operating point and stator current vary for increasing motor speed [22].

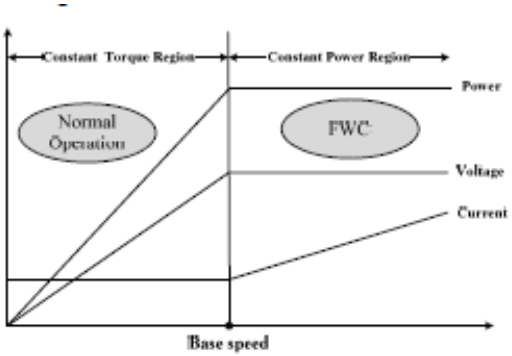


Figure 2.10: Motor parameters in relation with varying speed [22]

The Figure 2.10 describes the ratings of the machine at fixed load torque. During the constant torque operating region, the output power can be increased with an increase in the system voltage which in turn increases the speed of the machine. However, once the base speed is reached, the EM enters constant power region of operation and an increase in voltage can no longer be made as the rated value of battery voltage has been reached. To operate the motor at speeds higher than the base speed, field weakening is exploited by injecting negative d-axis currents into the stator. With this method, the torque can no longer

be expected to be maintained at the base level. By boosting the DC-link voltage at higher speeds, motor efficiencies were shown to increase from 55.13% to 78.46% at 4000RPM and from 42.2% to 79.15% at 5000RPM [22].

Similarly, for this thesis work, a Nissan Leaf Interior Permanent Magnet (IPM) motor is used as a representative benchmark EM. There is vast amount of public data available on this EV's motor that is used to aid in analysis. Motor specifications, torque-speed characteristics, and other performance metrics are obtained from reports by Oak Ridge National Laboratory. The maximum torque of the IPM motor is 280Nm at 2100RPM, and maximum power of 80kW is obtained at 3000RPM. The maximum speed of the motor is 10,000RPM [20]. The appropriate DC-link voltages that needs to be supplied to the motor to operate at speeds higher than the base speed without resorting to flux weakening regime are provided in Table 2.4. As long as the DC/DC converter can boost up the voltage to meet the minimum required line-to-line motor voltage while maintaining a respective margin over the generated back-emf, motor efficiencies can be increased by avoiding conduction losses due to the negative d-axis currents in its windings [23].

Table 2.4: Generated back-emf and required line-to-line voltage with varying speed of Nissan Leaf motor [23]

Speed (RPM)	Generated back-emf (V)	$V_{ll,pk}$ (V)
3000	122.98	230.17
4000	164.54	288.05
5000	206.11	333.50
6000	247.68	377.69
7000	287.52	427.85
8000	329.09	426.13
9000	370.66	444.42
10000	412.23	469.40

Chapter 3

HIGH FREQUENCY BI-DIRECTIONAL DC/DC CONVERTER WITH ZVT FOR AUTOMOTIVE HIGH VOLTAGE SYSTEM

3.1 Introduction

In this chapter, a bi-directional synchronous DC/DC converter with ZVT and high frequency switching is proposed for coupling the 200V-300V EV battery stack to the 3-phase PWM inverter in the EV powertrain. The wide output voltage range of the proposed converter can supply up to 800V to the inverter in the motoring mode of operation. The circuit diagram of the converter is shown in Figure 3.1. The converter consists of two main switches S_1 and S_2, two auxiliary branch switches S_{aux1} and S_{aux2} to facilitate ZVT in both buck and boost modes of operation, a main inductor L_1, and a DC-link capacitor C_1 connected in parallel with load resistance R_1. The equivalent capacitance C_{eq} combines external drain to source capacitance C_{DS} and output capacitance of the main switches. This capacitor is responsible for resonance with the auxiliary inductor L_{aux} during soft-switching operation [24]-[27].

For simplicity of analysis, the parallel combination of DC-link capacitor and load resistor is modeled as a constant DC source V_{DC} that supplies the required DC voltage to the 3-phase inverter in the EV powertrain. All switches are implemented with SiC MOSFETs with anti-parallel body-diodes to enable high efficiency at high switching frequencies of 250kHz per phase. In addition, SiC Schottky diodes are placed in parallel

with the body-diodes of the MOSFETs to decrease reverse recovery losses and further increase converter efficiency. The equivalent circuit is shown in Figure 3.2.

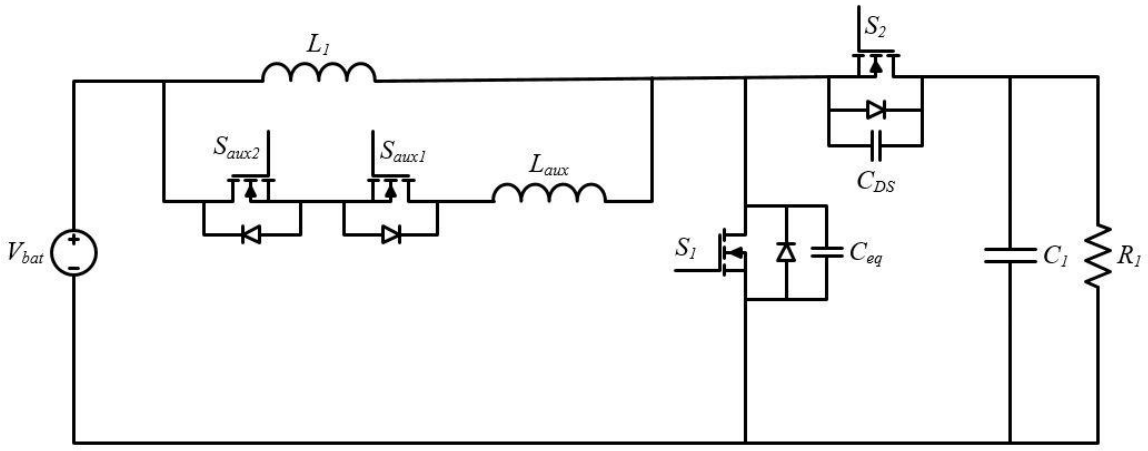


Figure 3.1: Circuit diagram of the proposed bi-directional DC/DC converter with ZVT

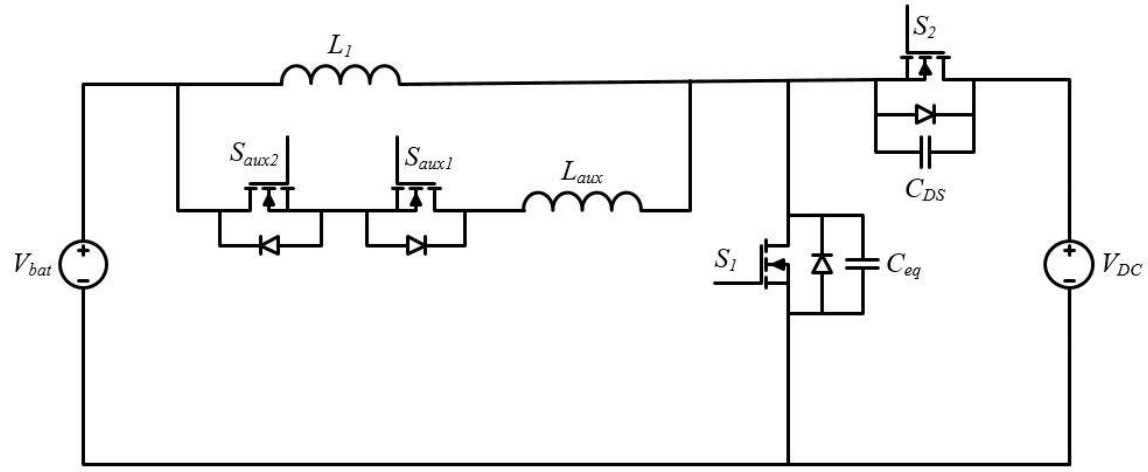


Figure 3.2: Equivalent circuit schematic

3.2 Operating Principle Analysis

As the operating principle of the converter in the buck mode of operation during regenerative braking is simply the dual of the boost mode of operation during motoring, only the boost operation of the converter is presented in detail. It is also assumed that all

the components are ideal, and the circuit is operating under steady-state condition. The key waveforms for boost and buck operation are shown in Figure 3.3 and Figure 3.4 respectively. The direction of current flow is indicated by the arrows in Figure 3.1. It should be noted that, in the key waveforms of buck mode, the high voltage side is still labeled V_{DC} and the low voltage output side is V_{in}. In steady-state operation, the analysis can be divided into eight intervals described in detail below. The topological states of the circuit in these eight intervals are also explicitly displayed in Figure 3.5.

Interval 1 ($t_0 - t_1$):

In this interval, main switch $S_1$is turned off while switch S_2 acting as the synchronous rectifier in boost mode is turned on and conducting inductor current I_L. Auxiliary switch S_{aux1} and S_{aux2} are both off with S_{aux1} blocking a voltage of $V_{DC} - V_{bat}$ and S_{aux2} blocking zero voltage. Therefore, there is no current present in the auxiliary branch. This is the conventional off interval of a boost converter when the stored inductor energy is being supplied to the load.

Interval 2 ($t_1 - t_2$):

At time t_1, the auxiliary switch S_{aux1} is turned on prior to turn on of main switch S_1, while S_{aux2} remains off. Current begins to flow in the auxiliary branch charging the auxiliary inductor L_{aux} by $V_{DC} - V_{bat}$ through switch S_{aux1} and the body diode of S_{aux2}. Auxiliary branch current $i_{Laux}(t)$ is given by (3.1).

$$i_{Laux}(t) = \frac{V_{DC} - V_{bat}}{L_{aux}} \cdot (t - t_1) \qquad (3.1)$$

Meanwhile, the current through synchronous switch S_2 decreases proportionally by:

$$i_{S2}(t) = I_L - \frac{V_{DC}-V_{bat}}{L_{aux}} \cdot (t - t_1) \quad (3.2)$$

Interval 3 ($t_2 - t_3$):

At t_2, the auxiliary branch current i_{Laux} has become equal to the main inductor current I_L soon after which the synchronous switch S_2 is turned off to keep switching loss as low as possible. As i_{Laux} increases greater than I_L, resonance between the equivalent capacitance C_{eq} at the switching pole and L_{aux} is initiated. Mathematical expression for $i_{Laux}(t)$ and $v_{S1}(t)$ during resonance are provided in (3.3) and (3.4) respectively. The peak of the auxiliary current is dependent on the voltage across the auxiliary inductor, which varies between $V_{DC} - V_{bat}$ and $-V_{bat}$, with characteristic impedance $Z = \sqrt{\frac{L_{aux}}{C_{eq}}}$, and $\omega = \frac{1}{\sqrt{L_{aux}C_{eq}}}$.

$$i_{Laux}(t) = I_L + \frac{(V_{DC}-V_{bat})\cdot\sin(\omega t)}{Z} \quad (3.3)$$

$$v_{S1}(t) = V_{DC} + (V_{DC} - V_{bat}) \cdot \cos(\omega t) \quad (3.4)$$

Interval 4 ($t_3 - t_4$):

At t_3, the drain to source voltage across main switch S_1 has been brought to zero with the current in C_{eq} now transferred to the body diode of the switch. Since the capacitor no longer carries any charge, the voltage across it has been effectively reduced to zero and therefore the switch S1 needs to be gated on within this interval to ensure zero voltage switching. The current difference between the main inductor current and the aux inductor current is

what recharges the capacitor C_{eq} and therefore switching should be carried out before this difference takes on a positive value and begins to recharge the capacitor.

Interval 5 $(t_4 - t_5)$:

In this interval, the current through the main switch begins to rise and it is given by the difference between the main inductor current and the auxiliary inductor current. Once the aux inductor current reaches zero, that is when the auxiliary switch can be turned off to achieve zero current switching in the auxiliary branch. The endpoint of this interval is when the auxiliary inductor current drops to zero and the auxiliary switch can be turned off without incurring any switching losses.

Interval 6 $(t_5 - t_6)$:

During this interval, conventional boost converter operation is expected and observed as the main switch is turned on and there is no current flowing through the auxiliary branch. The auxiliary switch is turned off in this interval under ZCS. The main inductor is charged and the DC-Link capacitor discharges to support the load.

Interval 7 $(t_6 - t_7)$:

During this interval, the main switch goes through a turn-off transition as the gate drive to S1 is removed. Due to the switch capacitance, the current through the switch drops linearly during this period. The current transient results in voltage build up within the switch capacitance which leads to switch off losses. However, a large value of the capacitance can significantly reduce the value of this voltage and thereby reduce the switch off losses.

Interval 8 ($t_7 - t_8$):

The low side switch S_1 has completely turned off and blocks the DC-link voltage. The drain-to-source voltage across the synchronous switch S_2 has dropped to zero and can be gated on at this time for ZVS. Inductor energy is transferred to the load through switch S_2 and the circuit state goes back to that of Interval 1.

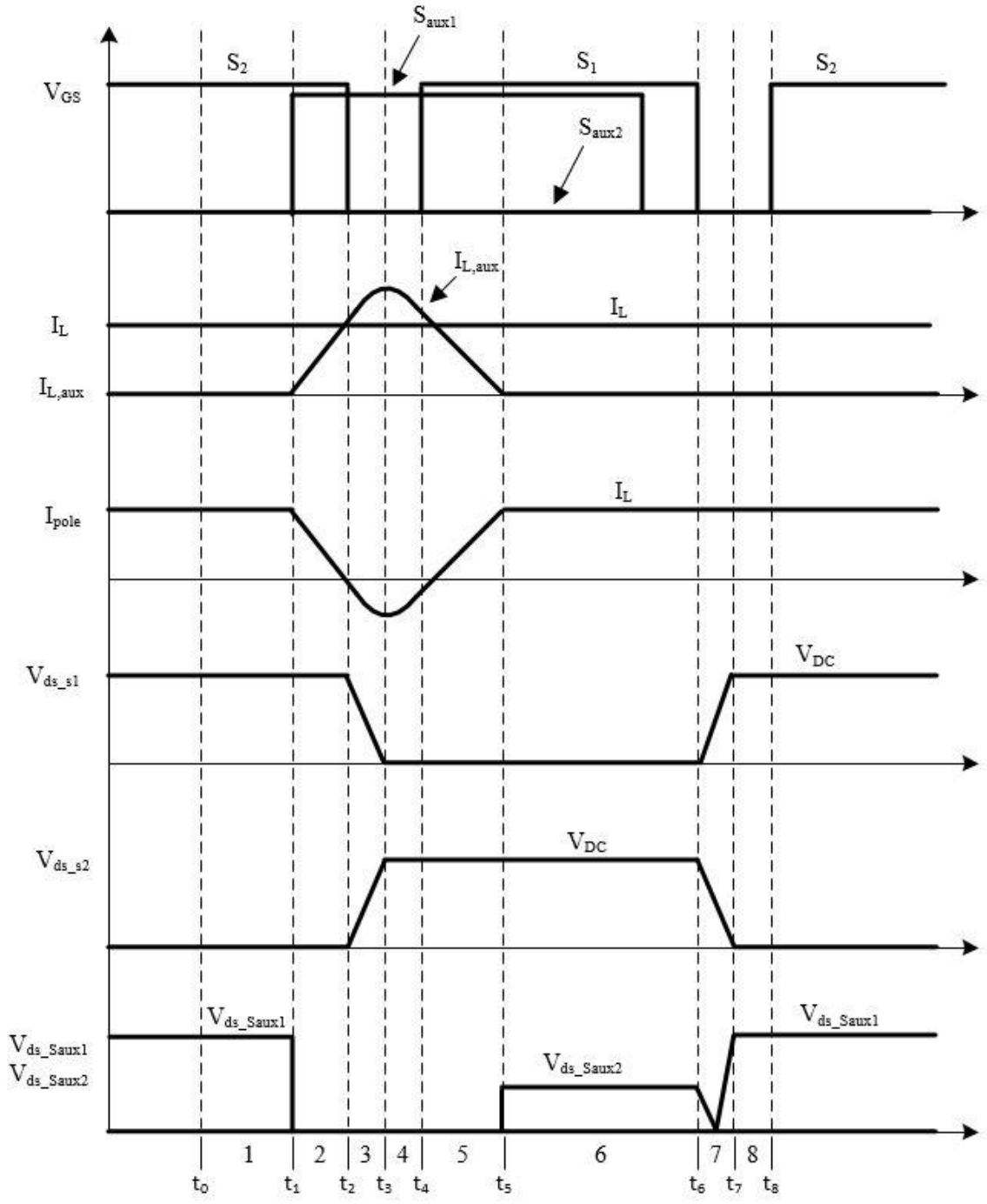


Figure 3.3: Key operating waveforms in boost mode

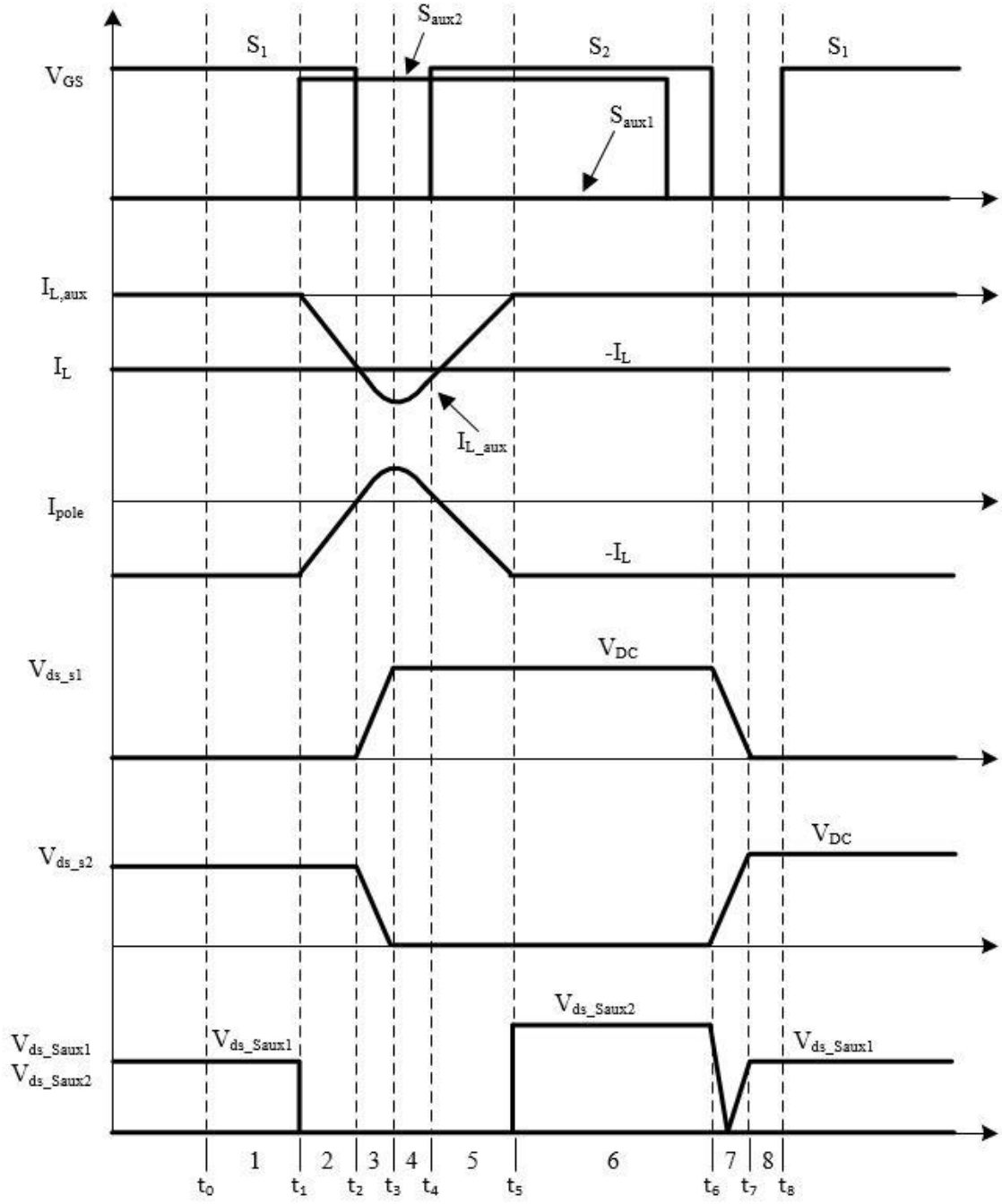
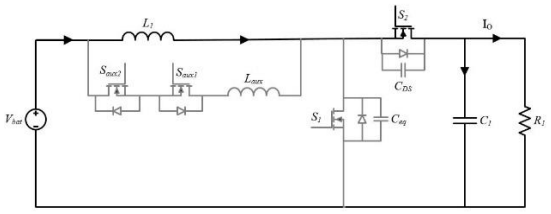
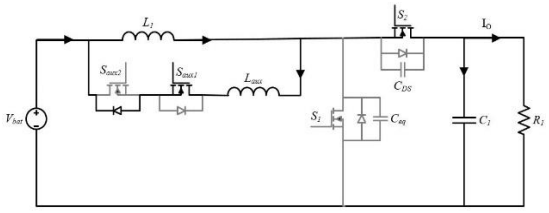


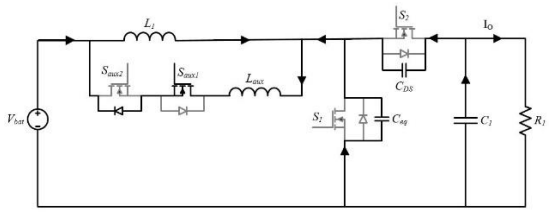
Figure 3.4: Key operating waveforms in buck mode



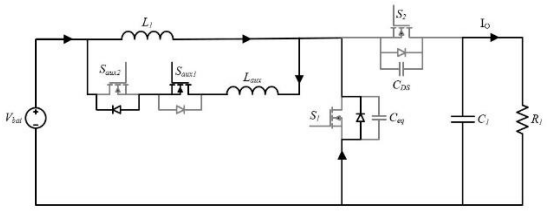
(a) Interval 1



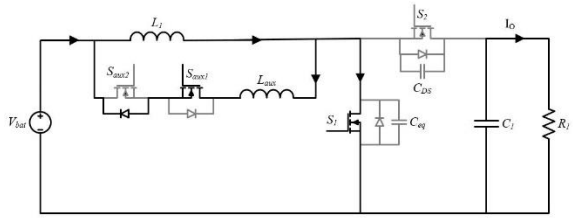
(b) Interval 2



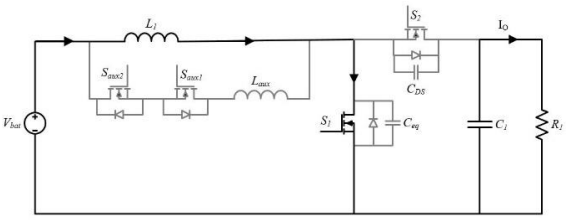
(c) Interval 3



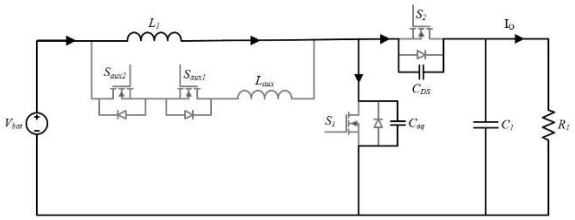
(d) Interval 4



(e) Interval 5



(f) Interval 6



(g) Interval 7

Figure 3.5: Topological state in each interval of operation in the boost mode

3.3 Converter Features

The working principle of the converter explained in the previous section evidently points out key features of the converter that are advantageous for its use in the automotive powertrain. The following features complement the general requirements of power electronic converters in automotive applications as outlined in Section 1.2.

a. Soft-switching for all switches

The operation of the proposed converter is such that the main switches S_1 and S_2 are operated under ZVS while the auxiliary branch switches S_{aux1} and S_{aux2} are switched under ZCS. This ensures high efficiency switching and low EMI even when operated at high switching frequencies.

b. Minimal auxiliary branch losses

An additional auxiliary branch is needed to reduce switching losses in the main switches. However, if the conduction losses incurred in the auxiliary branch are significant then it would defeat its intended purpose of increasing efficiency. The proposed topology accounts for this by limiting the duration of auxiliary current conduction to few 100s of nanoseconds and restricting the current peak required to realize ZVS.

c. Flexible ZVT implementation

The topology presented can achieve soft-switching for a wide range of operating conditions. The adaptive time delay calculates the required phase shift for the auxiliary gate pulse and ensures that the auxiliary current is sufficiently large enough to discharge

the switch resonant capacitors. In this way, ZVT is achieved for varying load as well as input voltage conditions.

3.4 Converter Design

A DC/DC converter for EV generally has a power rating in the tens of kilowatt range. As stated earlier, the proposed topology employs interleaving to minimize the size of filter components making the converter more compact, reducing the current rating of components, better thermal management, and consequently increase efficiency. The flexibility of interleaving allows easy power scaling depending on the power requirement of the EV motor. The power rating for a single phase of such a converter must be determined based on which, a single module prototype can be designed and tested. The power rating for the phase is a tradeoff between reducing losses per phase and reducing total number of phases. A compromise between the two is made and a power rating of 2.5kW for a single phase of the proposed bi-directional DC/DC converter is determined. The prototype design specifications are summarized in Table 3.1. Hardware prototype with the stated specifications is built and tested. The results are presented in Chapter 4.

Table 3.1: Proposed bi-directional DC/DC converter specifications

Rated Power	2.5kW
Input Voltage	200-300V
Output Voltage	310-800V
Switching Frequency	250kHz

3.4.1 Inductor Design

With the above specificatons, the boost inductor was designed based on the following four parameters:

a. The inductance value, L (H):

The inductance of the boost inductor was selected to limit the maximum input current ripple to 10% of the maximum expected input current of 12.5A for worst-case condition. This occurs for boosting an input voltage of 200V to a DC-link voltage of 800V. To maximize the inductance value, the worst-case duty ratio of 0.5 is used. Figure 3.6 shows that the maximum inductor current ripple of 1.25A occurs when the duty cycle is set to 50%. (3.5) gives the calculated inductance value.

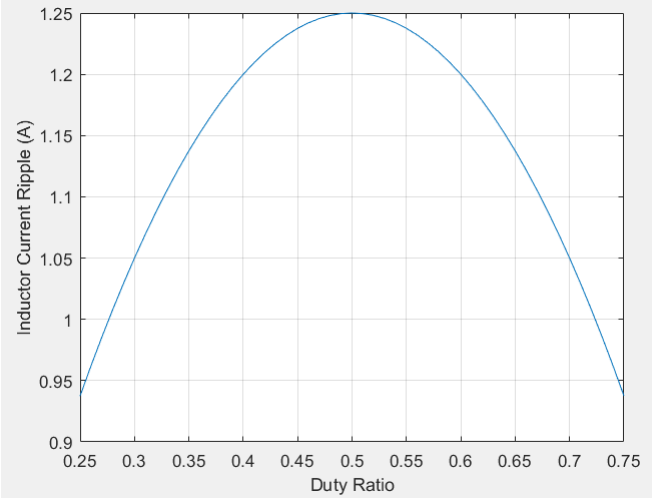


Figure 3.6: Varying inductor current ripple with duty ratio

$$L = \frac{V_o D(1-D)}{\Delta I_L \cdot f_{sw}} = 640\mu H \tag{3.5}$$

b. The maximum peak inductor current is given by:

$$I_{L,peak} = I_{in,max} + \frac{\Delta I_L}{2} = 13.75A \tag{3.6}$$

c. The RMS current rating of the inductor is given by:

$$I_{L,RMS} = \sqrt{I_{in,\max}^2 + \frac{(\Delta I_L)^2}{12}} = 12.5A \quad (3.7)$$

d. The DC bias of the inductor is given by:

$$I_{in,max} = \frac{I_{o,max}}{1-D_{max}} = 12.5A \quad (3.8)$$

Inductor Magnetics Design:

Based on the design parameters, the inductor core material, shape, core size, number of turns, wire gauge, and air gap required can be calculated. High frequency designs are generally limited by core loss. The design values used for flux density (B_{max}), current density (J_{max}), and window utilization factor (k_w) are provided below:

$B_{max} = 0.2T$, $J_{max} = 4\frac{A}{mm^2}$, $k_w = 0.4$

a. Area product:

$$A_p = \frac{L \cdot I_{pk} \cdot I_{RMS}}{B_{max} \cdot J_{max} \cdot k_w} = 2.167 \times 10^5 mm^4 \quad (3.9)$$

A ferrite E-core of dimensions 70/33/32 is selected whose area product is $3.85 \times 10^5 mm^4$ and so meets the minimum requirement calculated above.

b. Number of turns:

The number of turns required to obtain the desired inductance value is dependent on the expected current peak, maximum flux density, and minimum core area (A_c) obtained from the datasheet.

$$N = \frac{L \cdot I_{pk}}{A_c \cdot B_{max}} = 52 \quad (3.10)$$

c. Wire gauge:

The minimum wire gauge requirement is dependent on the expected RMS current rating through the inductor and the maximum current density.

$$A_{cu} = \frac{I_{RMS}}{J_{max}} = 2.5mm^2 \quad (3.11)$$

Litz wire of AWG No. 40 is selected with 435 strands and conductor diameter of 0.079mm.

d. Air gap:

The discrete air gap in the ferrite E-cores can be calculated using the permeability constant (μ_o), number of turns, minimum core area, and inductance:

$$l_g = \frac{\mu_o N^2 A_c}{L} = 3.38mm \quad (3.12)$$

3.4.2 Capacitor Selection

The DC-link capacitor is primarily selected based on the RMS current requirement and voltage rating.

a. RMS current rating:

$$I_{C,RMS} = I_{o,max} \cdot \sqrt{\frac{D_{max}}{1-D_{max}}} \cdot \sqrt{1 + \frac{(1-D_{max})^2}{D_{max}} \cdot \frac{\Delta I_L^2}{12 \cdot I_{o,max}^2}} = 5.42A \quad (3.13)$$

b. Output voltage ripple:

The minimum capacitance required to restrict the output voltage ripple to 10% of the minimum output voltage expected is given by:

$$C \geq \frac{I_{o,max} D_{max}}{\Delta V_o \cdot f_{sw}} = 0.12\mu F \quad (3.14)$$

c. Equivalent series resistance (ESR) limit:

To reduce the conduction loss, it is desired to pick a capacitor with very low ESR. The selected capacitor must have an ESR that is less than the value given in below:

$$ESR \leq \frac{\Delta V_o}{I_{in,pk}} = 2.25\Omega \quad (3.15)$$

d. Voltage rating:

The DC-link capacitor must be able to withstand the maximum output voltage expected plus a sufficient margin to account for voltage ripples and transients.

$$V_{o,max} = 800V + margin \quad (3.16)$$

3.4.3 Switch and Diode Selection

The switch and diode ratings are given as follows:

MOSFET Ratings:

a. Voltage rating:

$$V_{o,max} = 800V + margin \quad (3.17)$$

b. Peak current rating:

$$i_{sw,pk} = I_{in,max} + \frac{\Delta I_L}{2} = 13.125A \quad (3.18)$$

c. RMS current rating:

$$i_{sw,RMS} = I_{in,max}\sqrt{D_{max}} = 10.825A \quad (3.19)$$

Diode Ratings:

a. Voltage rating:

$$V_{o,max} = 800V + margin \quad (3.20)$$

b. Peak current rating:

$$i_{D,pk} = I_{in,max} + \frac{\Delta I_L}{2} = 13.125A \quad (3.21)$$

c. RMS current rating:

$$i_{D,avg} = I_{o,max} = 3.125A \quad (3.22)$$

3.4.4 Auxiliary Branch Design

The auxiliary branch inductor L_{aux} must be optimized to keep ZVT branch losses at a minimum. The auxiliary inductor determines the rate of rise of the ZVT branch current when the auxiliary switch is gated on. The equivalent capacitance at the switching pole is denoted by C_{eq} and is the summation of the output capacitances of the main and synchronous switches. This capacitance is responsible for resonance with the auxiliary inductor and affects the rate of energy transfer between the resonant devices. By setting a limit to the auxiliary current peak, the required inductance value can be calculated from (3.23). Where, Z is the characteristic impedance that can also be related to the voltage across the auxiliary branch $V_{DC} - V_{bat}$ and the determined auxiliary inductor current peak.

$$Z = \sqrt{\frac{L_{aux}}{C_{eq}}} \quad (3.23)$$

The time delay required to switch on the main MOSFET is a combination of the linear rise time, the quarter resonant period, and the linear fall time [b]. A simplified equation is given by:

$$t_{delay} = t_{rise} + t_{res} = \frac{\pi\sqrt{L_{aux}C_{eq}}}{2} + \frac{L_{aux}i_L}{V_{DC}-V_{bat}} \tag{3.24}$$

Once the auxiliary switch is gated on, the current is diverted from the synchronous switch into the auxiliary branch. This leads to pre-charging of the auxiliary inductor before the resonant period begins at turn-off of the synchronous switch. After this, the main switch is turned on causing resonance with the auxiliary inductor pre-charged to a certain level allowing for a wide soft-switching operating range.

3.5 Converter Loss Analysis

3.5.1 Output Capacitance Loss (P_{OSS})

The output capacitance loss of each switch is reliant upon the energy dissipated in the capacitance of each MOSFET during switching transitions. The output capacitance is dependent upon the voltage across each switch which is the DC-link voltage occurring in complementary intervals for the main and synchronous switch. The energy loss E_{OSS}, corresponding to the output switch capacitance obtained from the datasheet can be used in (3.25) to calculate the capacitance loss.

$$P_{OSS} = 2 \cdot E_{OSS} \cdot f_{sw} \tag{3.25}$$

3.5.2 Gate Loss (P_G)

The magnitude of gate losses is significantly lower than the switching losses. The parameters required to calculate gate losses include Q_{GD} and Q_{GS2} which refer to charges required to reduce the gate voltage to zero and the charge required to increase the gate voltage beyond the threshold value to a plateau for conduction respectively. The operating plateau voltage values and corresponding drain-to-source current are read from MOSFET datasheets. The total charge required to increase gate voltage to the plateau voltage is denoted by Q_{GS}. Another important parameter required to calculate the gate losses is the $m_{QGslope}$ which gives the slope of the region between the plateau voltage and the final gate voltage which is 20V for the switches used in this design. Using these parameters, the total charge required to drive a gate voltage from the starting value to the value required to conduct for a given operating condition can then be found. This charge is necessary to carry out loss analysis of the switch and is referred to as $Q_{G(op)}$. The final gate losses are a product of the operating gate charge, switch gate drive voltage and switching frequency.

$$Q_{G(op)} = (Q_{GS} + Q_{GD}) + (m_{QGslope} \cdot (V_{DR} - V_{pl})) \tag{3.26}$$

$$P_G = Q_{G(op)} \cdot V_{DR} \cdot f_{sw} \tag{3.27}$$

3.5.3 Body Diode Conduction Loss (P_{SD})

To calculate the conduction loss of body diodes, the key parameters are the effective conduction time of the diodes. This is given by a difference between the effective deadtime between the switching of the main and the synchronous switch and the fall time of each

diode. Once the t_{diode} is known, the conduction losses through the diodes, both when the main switch is on and off can be calculated. This is shown below:

$$P_{SD,off} = V_{SD,off} \cdot I_{off} \cdot t_{diode} \cdot f_{sw} \tag{3.28}$$

$$P_{SD,on} = V_{SD,on} \cdot I_{on} \cdot t_{diode} \cdot f_{sw} \tag{3.29}$$

3.5.4 Switching Loss (P_{SW})

The main switch experiences both turn-on and turn-off hard switching while the synchronous switch experiences very small switching loss since every switching transition is only to and from a diode voltage drop. The losses are dependent on external gate resistances R_{Gon} and R_{Goff}, the plateau voltage, the gate drive voltage, the threshold voltage, and the gate charge Q_{GD} and Q_{GS}. The losses are calculated using the following formulae:

$$P_{on} = \frac{(V_{out} \cdot I_{on} \cdot f_{sw} \cdot R_{Gon})}{2} \cdot \left(\frac{Q_{GD}}{V_{DR} - V_{pl}} + \frac{Q_{GS}}{V_{DR} - \frac{(V_{pl} + V_{th})}{2}} \right) \tag{3.30}$$

$$P_{off} = \frac{(V_{out} \cdot I_{off} \cdot f_{sw} \cdot R_{Goff})}{2} \cdot \left(\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS}}{\frac{(V_{pl} + V_{th})}{2}} \right) \tag{3.31}$$

3.5.5 Switch Conduction Loss (P_{cond})

Since the conduction time for each switch is based on the duty ratio, calculation of the losses requires the duty ratio for each switch to be determined. Once the duty ratios are known, the conduction losses are calculated similarly to the conduction losses through diodes, the difference being that in the case of a switch, the $R_{DS,on}$ is used instead of the forward voltage drop to evaluate the losses.

$$P_{cond} = I_{sw,RMS}^2 \cdot R_{DS,on} \cdot D \tag{3.32}$$

3.5.6 Inductor Loss (P_{ind})

The inductor loss is a combination of the copper loss in the winding and the losses in the inductor core. The copper losses are given by the product of the inductor DC resistance and the square of the RMS current through the inductor. The core losses are small for an unsaturated core and can be calculated using proprietary core loss calculators associated with each make and model of inductors [28]. The coefficients given in (3.34) are obtained from Ferroxcube which gives the power loss per core volume denoted by P_v. The product of P_v and the inductor core volume V_e comprises of the total inductor core losses.

$$P_{ind} = I_{L,RMS}^2 \cdot R_{dc} \tag{3.33}$$

$$P_v = C_m \cdot f_{sw}^x \cdot B^y \cdot \frac{Ct_2 \cdot T^2 - Ct_1 \cdot T + Ct}{1000} \tag{3.34}$$

$$P_{core} = P_v \cdot V_e \tag{3.35}$$

3.5.7 Capacitor Loss (P_{cap})

The capacitor loss is due to the equivalent series resistance of the selected capacitor and is given as follows:

$$P_{cap} = I_{C,RMS}^2 \cdot ESR \tag{3.36}$$

Using the above equations, the calculated loss breakdown for 1.35kW and 2.5kW operating conditions is given in Figure 3.7 and Figure 3.8 respectively for hard-switching and soft-switching case.

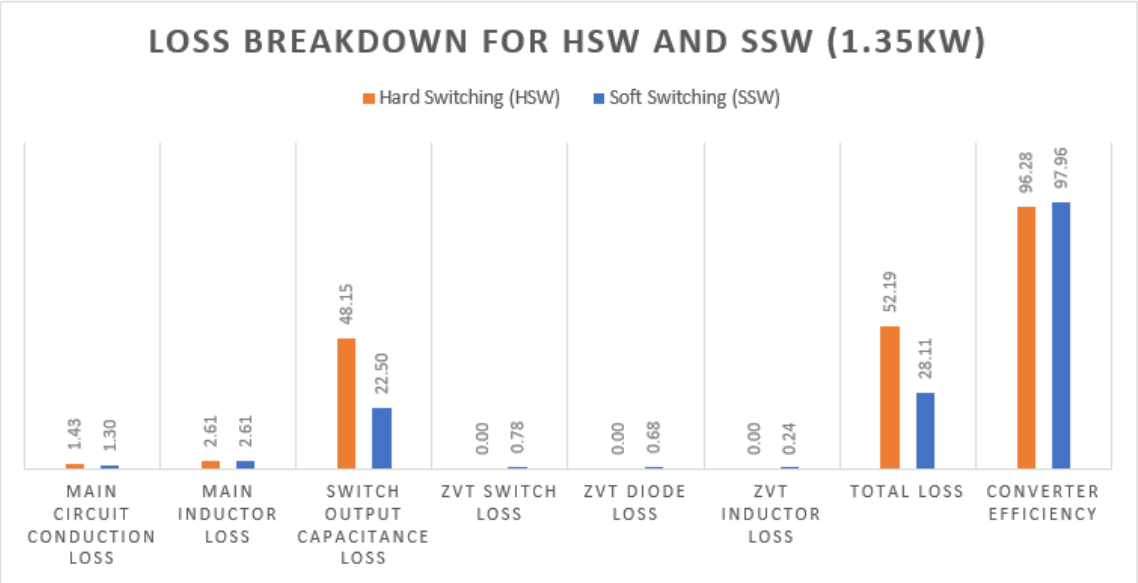


Figure 3.7: Loss breakdown of proposed converter for 1.35kW operating condition

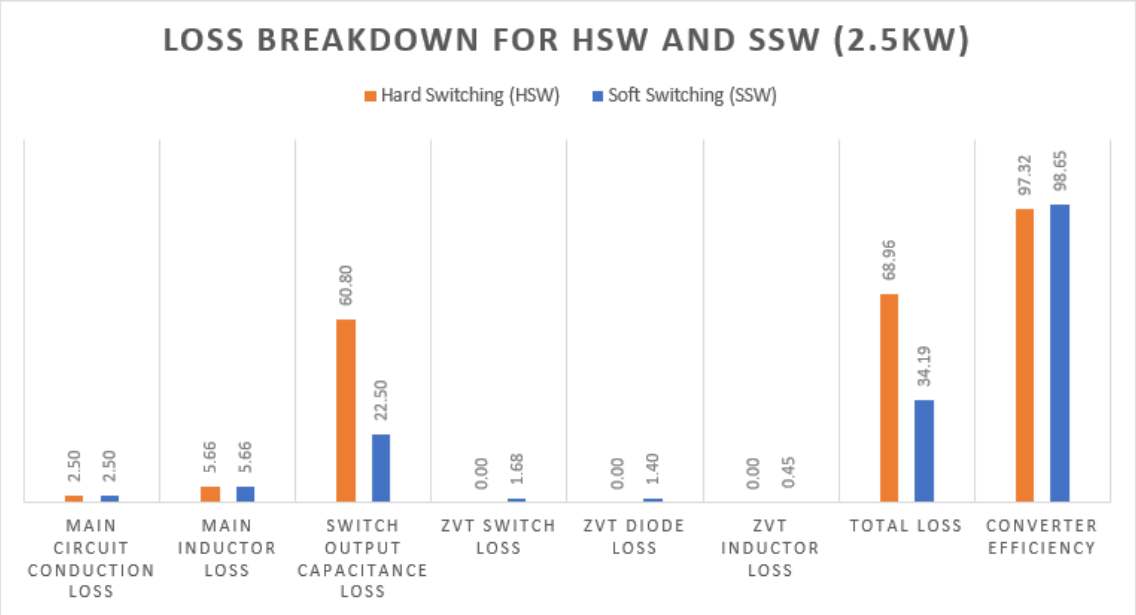


Figure 3.8: Loss breakdown of proposed converter for 2.5kW operating condition

3.6 Converter Simulation

With the design values specified in Section 3.4, the proposed DC/DC converter operation is simulated using PLECS for various test cases. The circuit simulation model used is shown in Figure 3.9. The resultant key waveforms are simulated to verify converter operating principles as discussed in Section 3.2. These waveforms in boost or motoring mode of operation are shown in Figure 3.12 and buck or regenerative braking mode are shown in Figure 3.13.

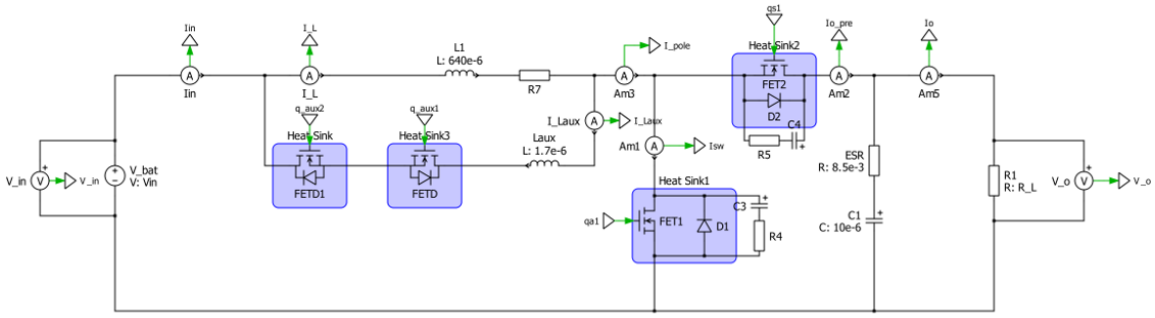


Figure 3.9: PLECS schematic used for simulating the proposed converter topology

The control scheme for the proposed DC/DC converter dictates the direction of power flow and maintains the magnitude of power transferred to and from the EV battery. Current control using the K-factor method is implemented in PLECS simulation to regulate the main inductor current to a reference value.

The plant transfer function for the high speed current control loop is given by (3.37). The transfer function is dependent on load resistance R_L given by V_o^2/P, where V_o is the maximum output voltage of 800V and P is the rated power of 2.5kW. The bandwidth of the controller is set at 25kHz which is 10% of the switching frequency.

$$G_{plant}(s) = \frac{V_{in}}{R_L} \cdot \frac{1+sC(R_{ESR}+R_L)}{1+s\left(\frac{L}{R_L}+CR_{ESR}\right)+s^2LC\left(1+\frac{R_{ESR}}{R_L}\right)} \tag{3.37}$$

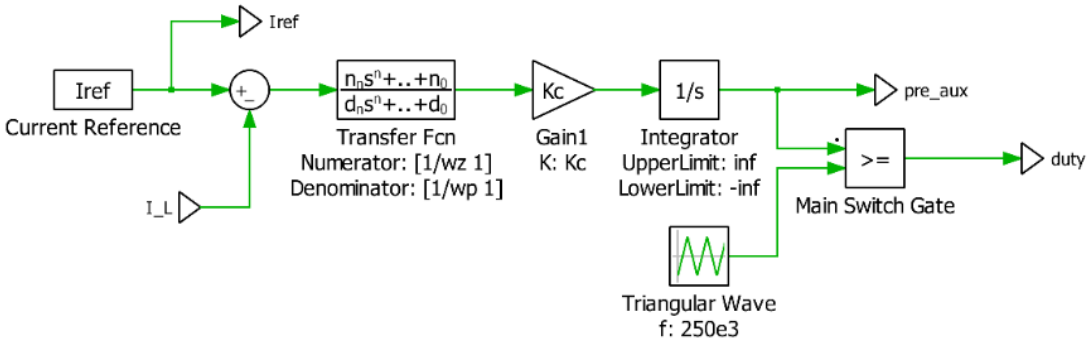
The desired phase margin to safeguard controller stability is 60^o. As the required phase boost is 55^o, a type-II controller is implemented whose transfer function is given in (3.38).

$$G_c(s) = \frac{K_c\left(1+\frac{s}{\omega z}\right)}{\left(1+\frac{s}{\omega p}\right)} \tag{3.38}$$

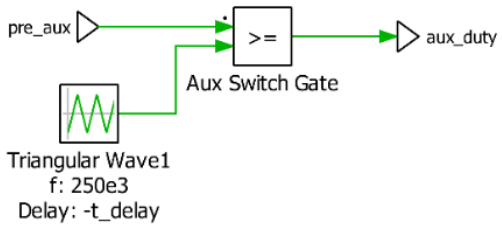
The resulting gain (K_c), zero (ωz) and pole (ωp) values are as follows:

$$K_c = 2.461 \cdot 10^4$$
$$\omega z = 4.909 \cdot 10^4$$
$$\omega p = 5.027 \cdot 10^5$$

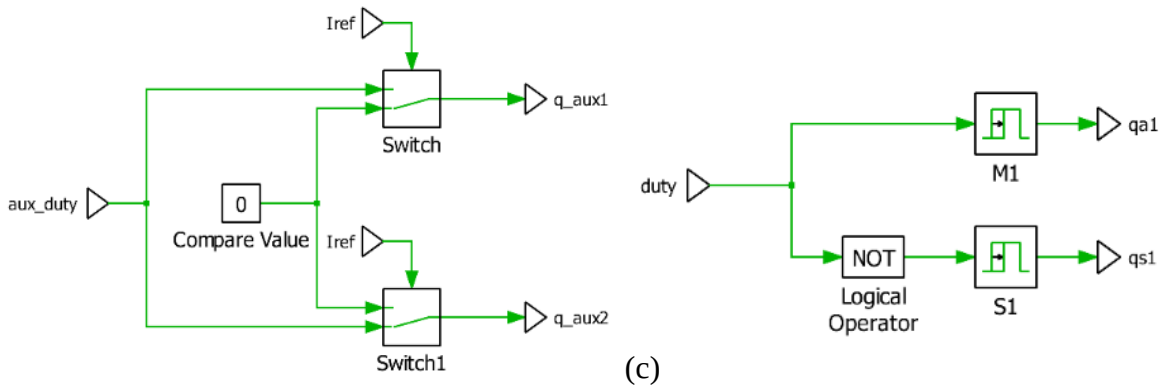
The controller implementation in PLECS is shown below:



(a)



(b)



(c)

Figure 3.10: (a) PLECS current control transfer function implementation and main switch duty cycle calculation (b) auxiliary switch duty cycle calculation (c) auxiliary (left) and main switch (right) gate supply

The adaptive time delay between auxiliary switches and main switches is provided as a negative phase shift of the triangle wave comparator for the auxiliary switches as shown in Figure 3.10(b). In boost mode of operation, S_{aux1} operates ahead of main switch S_1 with a specified time delay and in the buck mode of operation, S_{aux2} switches on ahead of synchronous switch S_2. The calculated auxiliary duty cycle must be provided to the appropriate switch in either case. This gate driver logic is accomplished with a simple comparison to the current reference provided as shown in Figure 3.10(c).

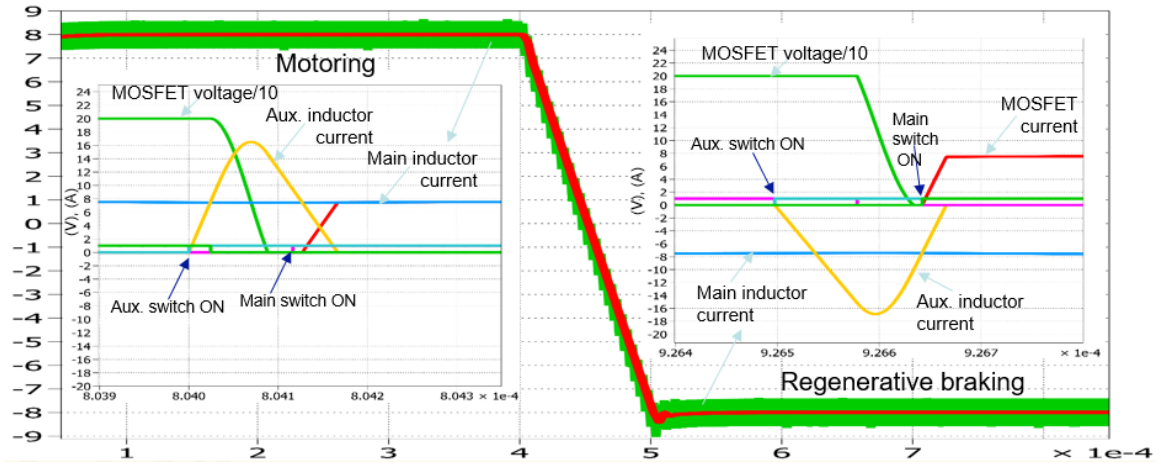


Figure 3.11: Soft-switching operation under motoring and regenerative braking mode

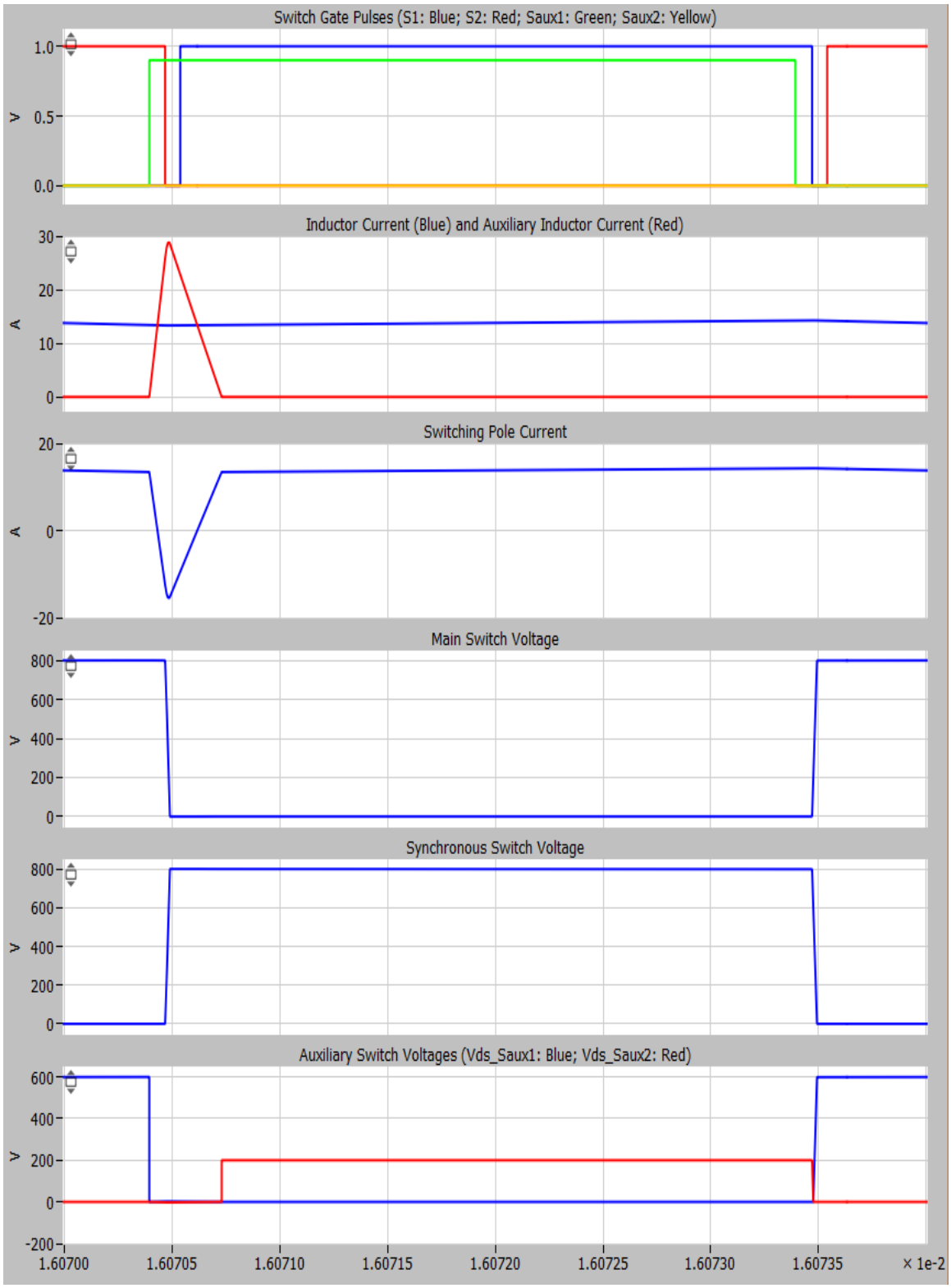


Figure 3.12: Simulated key operating waveforms in PLECS for boost mode

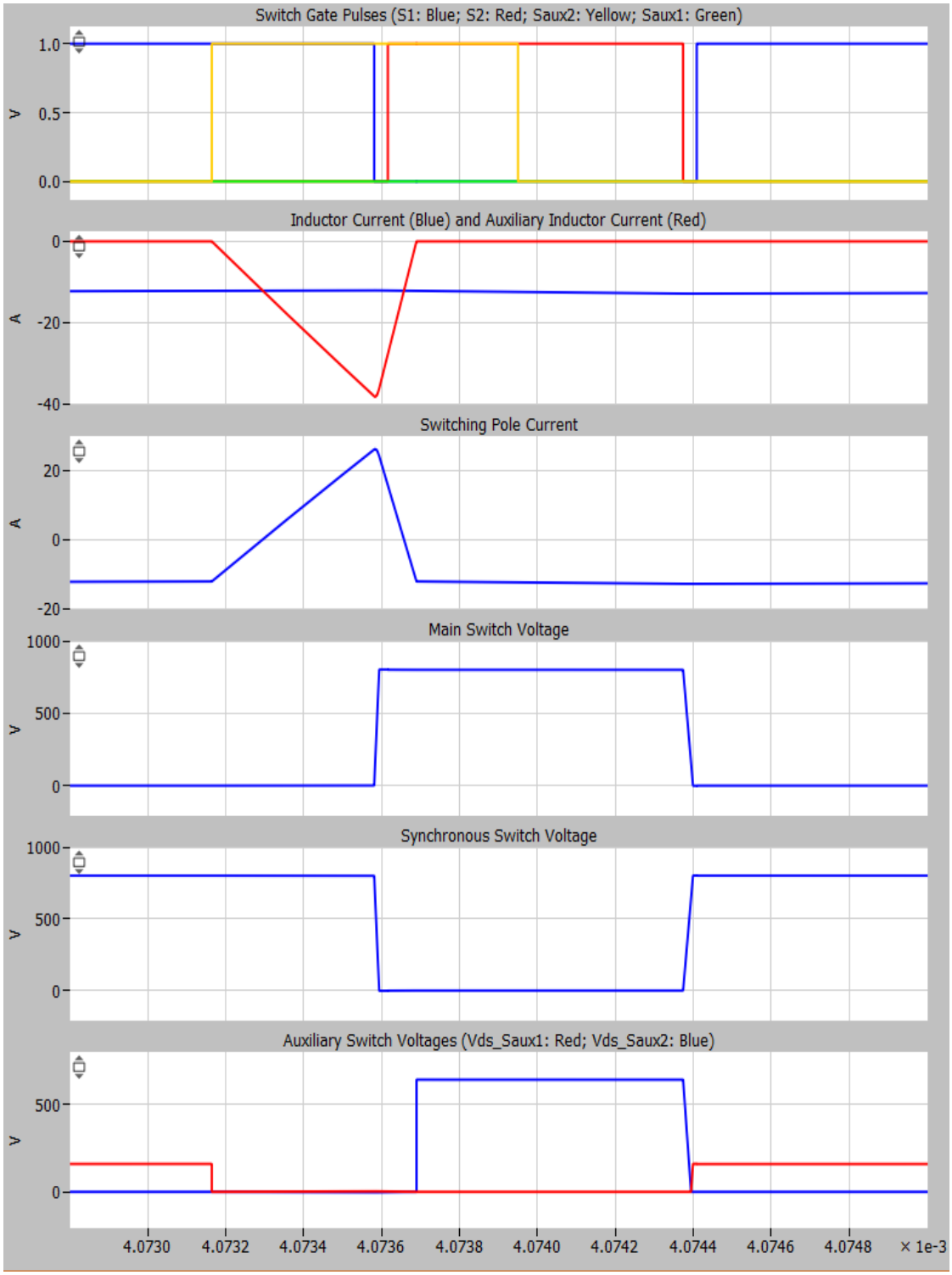
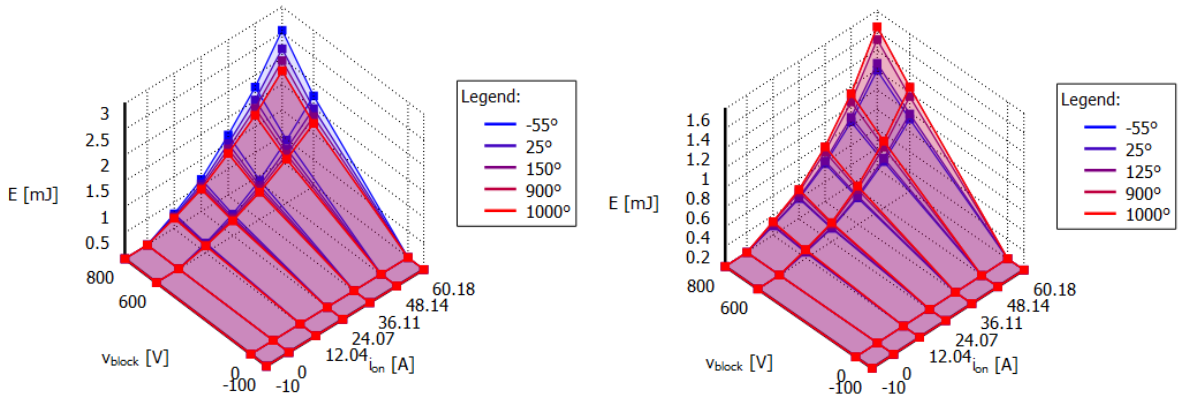


Figure 3.13: Simulated key operating waveforms in PLECS for buck mode

The salient waveforms simulated for both operating modes with ZVT is provided in Figure 3.11. A current reference of +8A dictates power flow from battery to the motor and a reference of -8A simulates the regenerative braking condition with energy from the motor put back into the battery.

To verify the analytically calculated losses incurred in the converter through simulation, the MOSFET and diode PLECS models are obtained from Wolfspeed [29]. The turn-on, turn-off and conduction loss look-up table and corresponding graphs provided in the model are included in the thermal description of the MOSFET and diode used in PLECS simulation. These models along with related loss equations are used to obtain the loss characteristics of the devices. The turn-on and turn-off loss characteristics for C2M0025120D MOSFETs used as main and synchronous switch in the converter are provided in Figure 3.14. The conduction loss characteristic curves are provided in Figure 3.15.



(a) (b)

Figure 3.14: C2M0025120D MOSFET (a) turn-on loss (b) turn-off loss

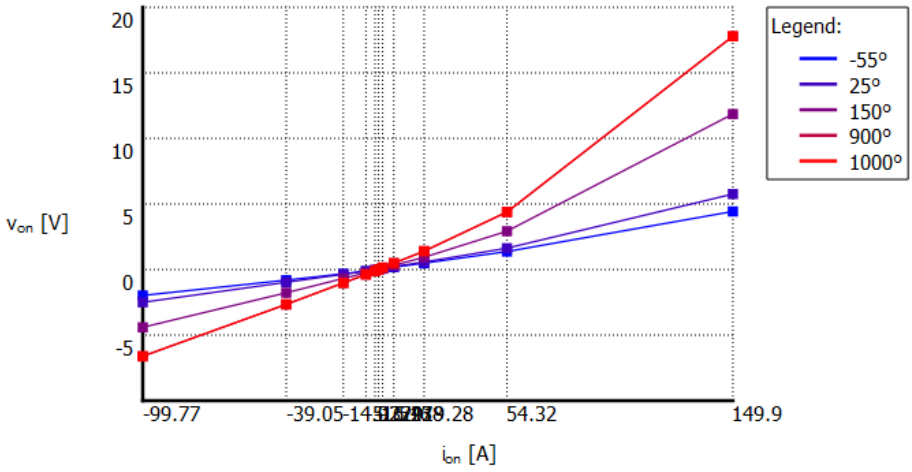


Figure 3.15: Conduction loss characteristic curves for C2M0025120D MOSFET

The obtained converter loss analysis through simulation is compared with the analytical loss calculations presented in Section 3.5. These results are summarized in Figure 3.16. It is evident that simulation and analytical converter losses agree with very little margin of error.

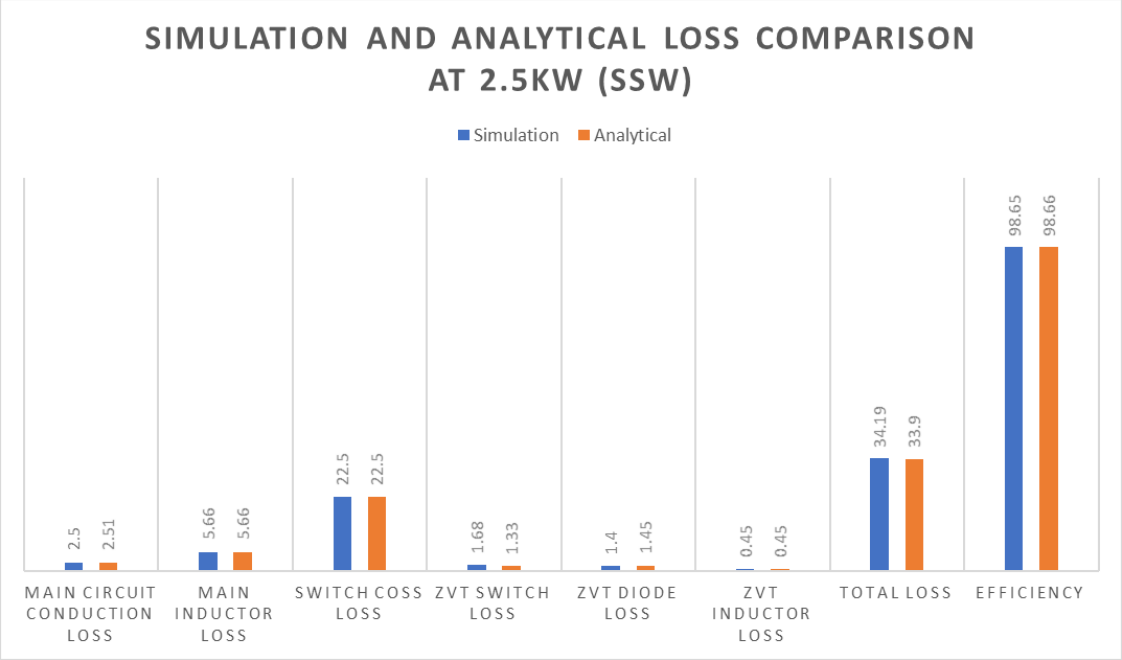


Figure 3.16: Comparison of losses obtained through simulation and analytical methods

Chapter 4

HARDWARE PROTOTYPE IMPLEMENTATION AND RESULTS

4.1 Hardware Implementation

With the design metrics calculated in Section 3.4, the selected components for the proposed converter are summarized in Table 4.1. For the main and synchronous switches, CREE N-Channel Enhancement Mode SiC Power MOSFET C2M0025120D with a blocking voltage of 1200V and on-state resistance of 25mΩ are used [30]. The auxiliary switches use MOSFETs from a similar CREE series C2M0080120D with voltage rating of 1200V and on-state resistance of 80mΩ [31]. These switches are selected because of their lower switch drain-to-source capacitances that help reduce undesired resonance in the auxiliary branch. The DC-link capacitor is selected to meet the voltage and RMS current rating while having the lowest available ESR. A $10\mu F$ capacitor is chosen from AVX Corporation with ESR of 8.5mΩ [32].

All the gate pulses in the system are implemented using Texas Instruments™ TMS320F28335 Digital Signal Processor (DSP). Code Composer Studio (CCS) by TI is an integrated development environment that supports the selected DSP and is used to develop the control for this converter application. The C-script written in CCS is built and loaded on to the DSP through the eZdsp™ F28335 stand-alone module. A Spectrum Digital C2000 XDS510LC Emulator is used to interface code written in CCS to the eZdsp evaluation board [33].

The TMS320F28335 DSP has on chip 12-bit Analog-to-Digital (A/D) converter with 16 input channels used to sense input voltage V_{in}, output voltage V_{out} and main inductor current i_L. The Analog-to-Digital Converter (ADC) module is capable of conversions as fast as 80ns per sample which is instrumental for implementing efficient control. It also has 6 independent, enhanced PWM channels (ePWM) that provide high resolution gate signals to the MOSFETs. Proper ZVT operation is largely dependent on executing time delays for gate pulses within tens of nanosecond accuracy which can be effectively supplied using this DSP.

Table 4.1: List of selected components for the converter

Component Selection	
Main Inductor Magnetics	
Selected Core	E 70/33/32
Core Material/Shape	Ferrite/E-Core
Number of Turns, N_t	52
Air Gap, l_g	3.382mm
Wire Gauge	AWG No. 40
Number of Strands, n_s	435
Capacitor	
Capacitance	10µF
ESR	8.5mΩ
Voltage Rating	1200V
RMS Current Rating	11A
Main Switch + Synchronous Switch	
Selected Switch	1200V/90A SiC C2M0025120D
$R_{DS,on}$	25mΩ
Auxiliary Switches	
Selected Switch	1200V/36A SiC C2M0080120D
$R_{DS,on}$	80mΩ

The fabricated prototype of the PCB is shown in Figures 4.1 and 4.2. The wound main inductor is connected externally to the board. The auxiliary branch is also connected through an external wire (red wire in Figure 4.1) to allow access for sensing auxiliary

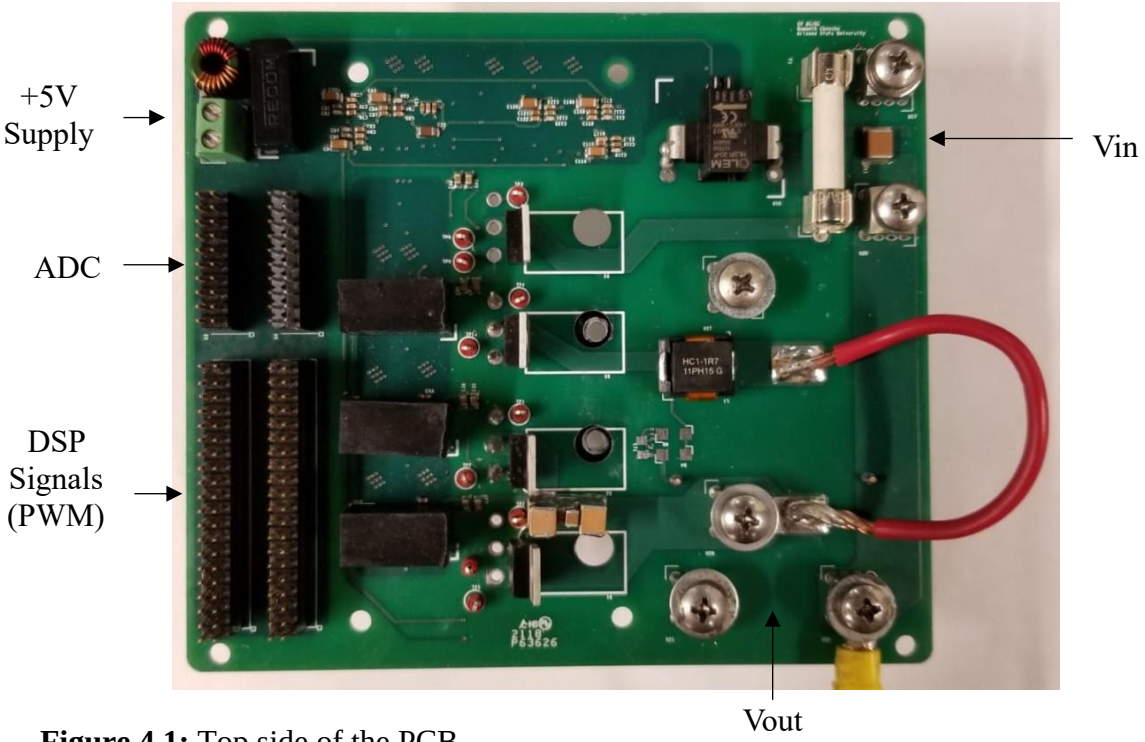


Figure 4.1: Top side of the PCB

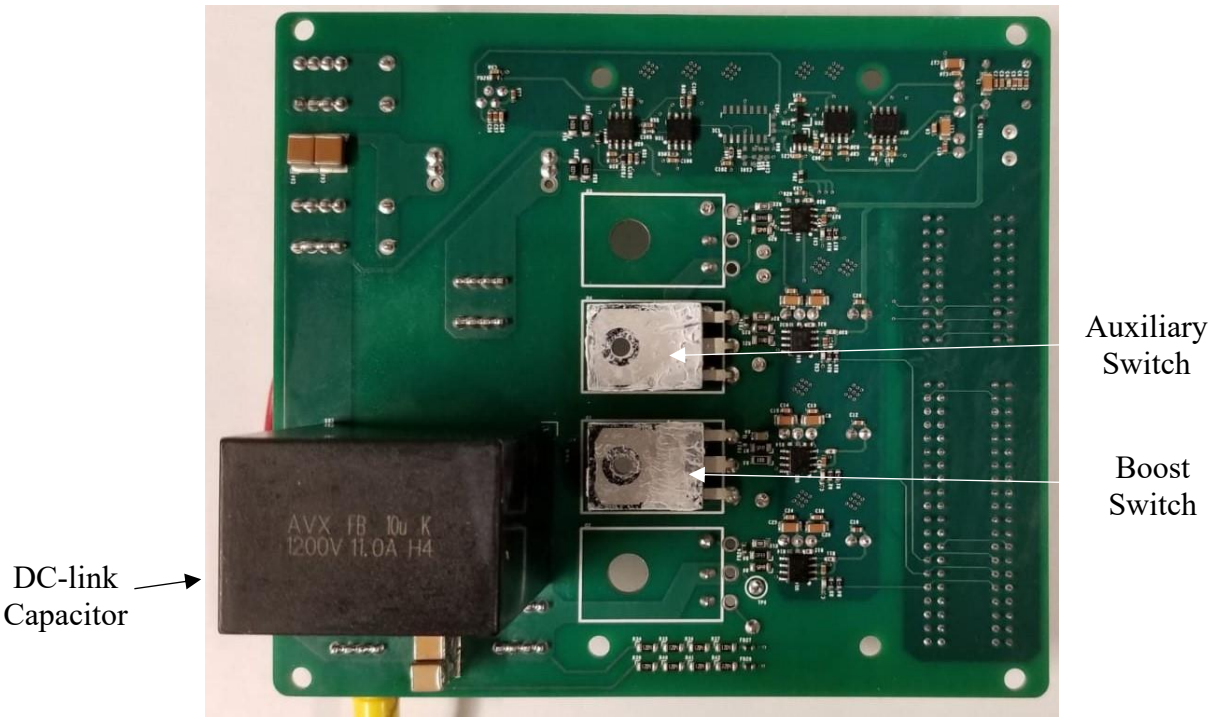


Figure 4.2: Bottom side of the PCB

branch current using a probe. The experimental setup used for testing is shown in Figure 4.3(a). The load used is a series of 8 light bulbs (rated 120V, 250W) connected in parallel with another set of 8 light bulbs connected in series. The maximum rating of the load is 4kW operating at 960V.

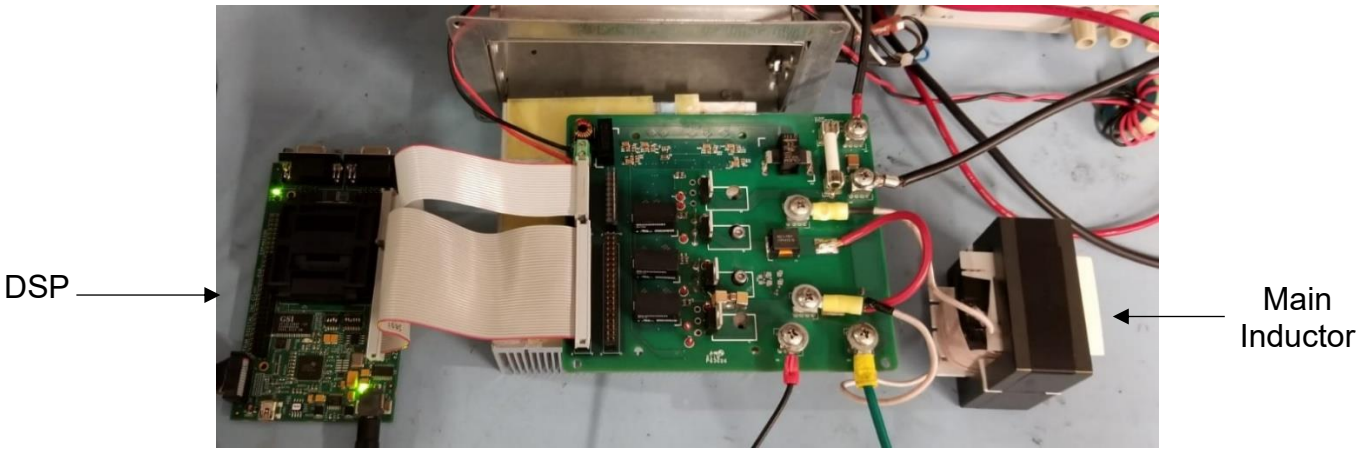


Figure 4.3: Experimental setup of the hardware prototype

4.2 Experimental Results

Hard switching waveforms for 1.35kW boost operation stepping up the voltage from 200V to 400V with a duty cycle of 50% is shown in Figure 4.4. It is evident that under hard-switching, the gate voltage to the main switch is supplied while the switch blocks the entire DC-link voltage. Once the gate-to-source voltage reaches the switch threshold voltage, current through the switch begins to ramp up overlapping the corresponding drop in its drain-to-source voltage leading to high switching loss. The efficiency observed through the power analyzer under this condition is 96.496%.

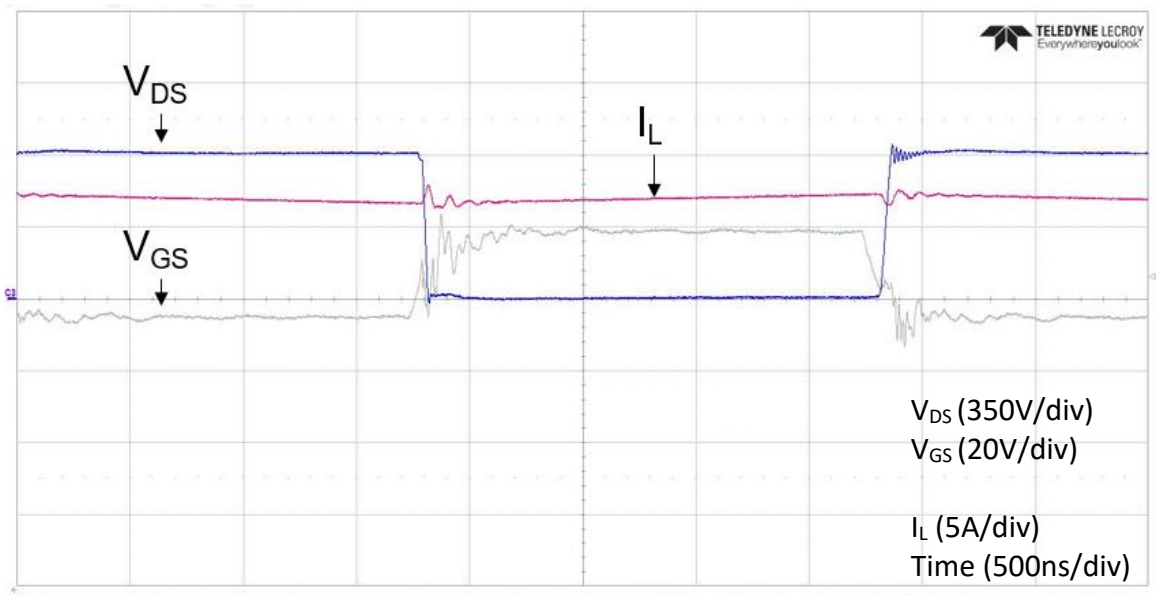


Figure 4.4: Hard-switched test waveforms for 1.35kW power rating

By incorporating the ZVT branch under the same 1.35kW test conditions, the efficiency can be improved considerably. Figure 4.5 shows the resultant waveforms obtained under soft-switching condition. Here, the auxiliary switch is gated on prior to the main switch allowing the drain-to-source voltage across the main MOSFET to drop to zero before the

main switch is turned on. The auxiliary inductor current (green) rises above the main inductor current (maroon) diverting the main inductor current into the auxiliary branch and facilitating soft-switching. The efficiency improved to 98.174% with ZVT.

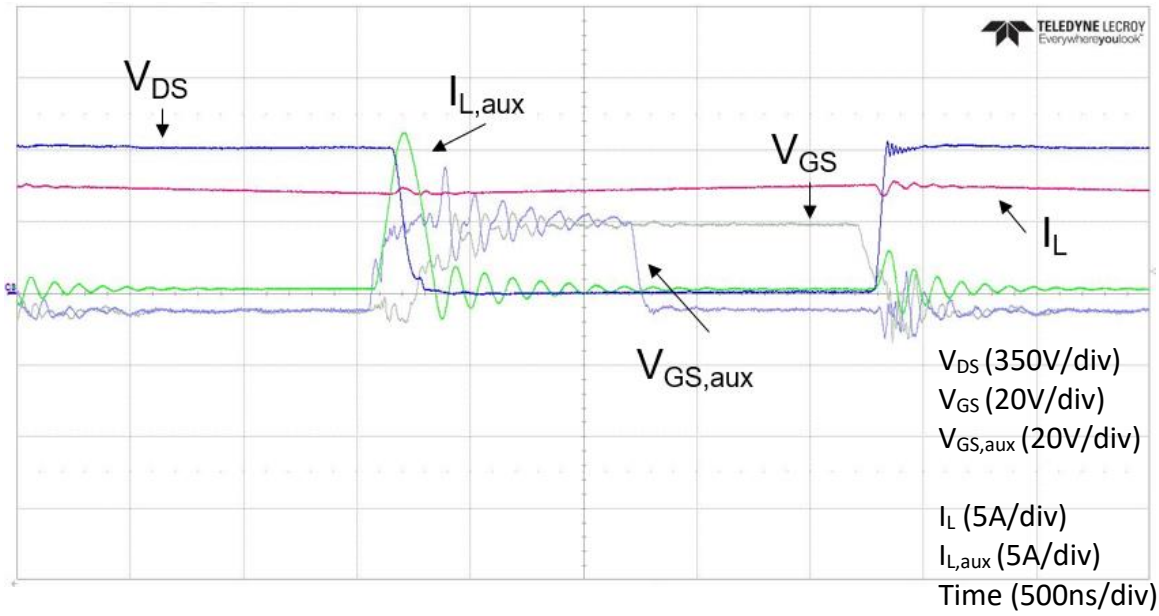


Figure 4.5: Soft-switched test waveforms for 1.35kW power rating

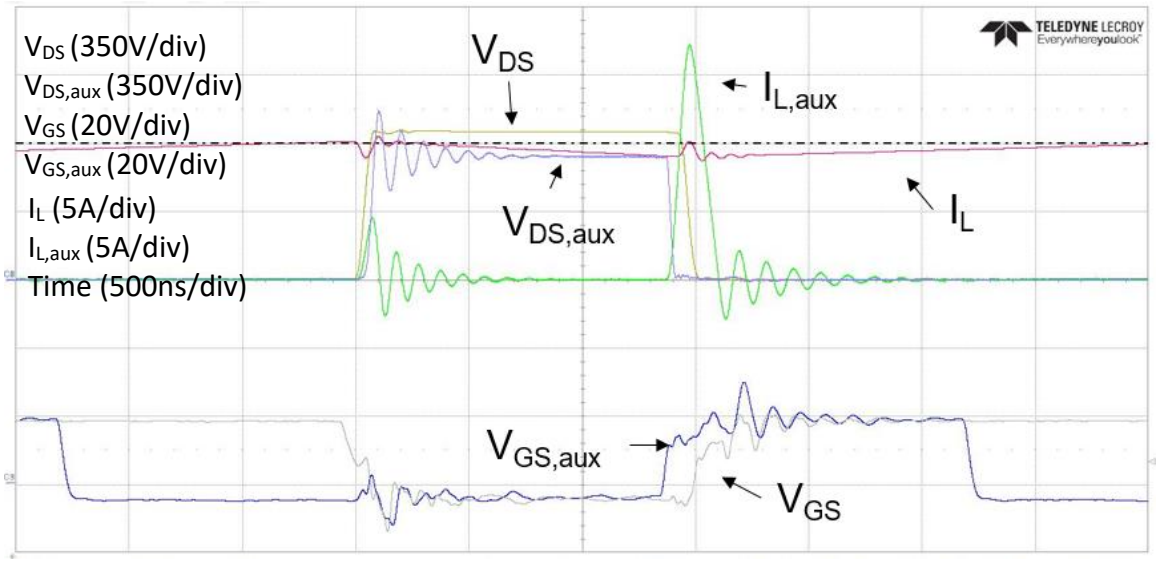


Figure 4.6: Soft-switched test waveforms for 2.5kW operating condition

Hardware test results for rated power of 2.5kW with soft-switching are shown in Figure 4.6. It can be seen that the drain-to-source voltage (yellow) ringing has been damped well with the use of multiple ceramic capacitors placed close to the switching power pole. However, ringing in the voltage waveform across the auxiliary branch is significant with the initial transient reaching 840V before settling to 630V. This intial spike is well under the voltage rating of the MOSFET.

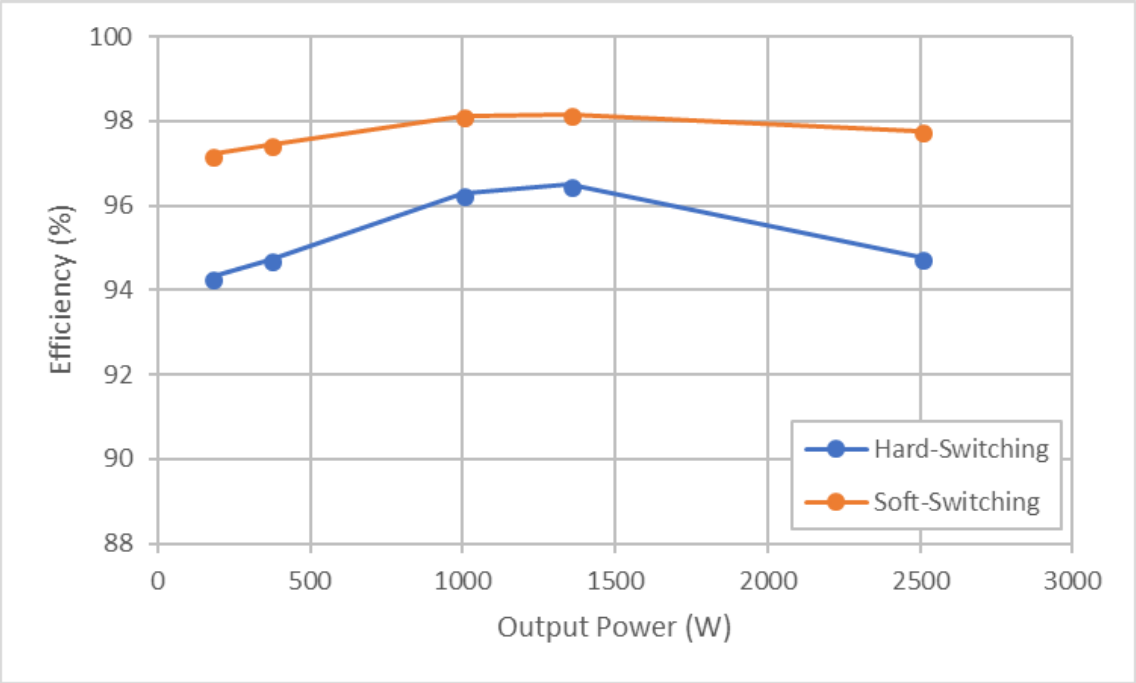


Figure 4.7: Efficiency of the DC/DC converter under hard and soft-switching operation

Converter performance under hard-switching and soft-switching configurations for different load test conditions is provided in Figure 4.7. It is observed that for the conducted hardware tests at a switching frequency of 250kHz, peak efficiency of 98.17% is obtained at 1.35kW load condition.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, a general overview of the EV powertrain architecture is provided with the idea of optimizing each independent module to improve overall system efficiency. The benefits of interfacing the EV battery to the three-phase inverter through a DC/DC converter is discussed, followed by an outline of the requirements of such a converter in automotive applications. A comparison of three different converter topologies revealed that an interleaved synchronous boost converter is preferable for this application. The advantages of this converter include: (1) low component count, (2) flexibility for power scaling, (3) compact size and (4) easy control. Next, to further improve proposed converter efficiency, WBG devices such as SiC and GaN are considered as an alternative to conventional Si switches. Then, soft-switching concepts are reviewed. The proposed converter features SiC MOSFETs with a new ZVT branch that functions in both boost as well as buck mode of operation.

The prototype specifications for a single phase of the DC/DC converter module are defined. A 2.5kW, bi-directional DC/DC converter that operates under input battery voltage range of 200-300V and outputs a wide output DC-link voltage of 300-800V with soft-switching is designed, built, and tested. The proposed converter's design process is covered in detail. Loss analysis of individual components in the converter is performed and presented showing 97% efficiency under hard-switching condition for the worst-case

occurring for duty ratio of 0.75, and >98% under soft-switching for rated power. Hardware results show agreement with analytical and simulation results achieving peak efficiency of 98.17% at half power load and efficiency of 97.75% achieved at rated power with ZVT.

5.2 Future Work

The efficiency achieved at 2.5kW under soft-switching test condition can be improved to >98% with the incorporation of the synchronous switch and fine tuning the auxiliary branch ZVT timing. Buck mode power flow for regenerative braking operation needs to be tested. For the next phase of the project, seamless bi-directional control of the converter is to be realized. Power rating of the converter can be scaled up by integrating 4 to 5 additional phases and testing the interleaved converter module to attain >10kW power level.

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