Advanced Control of the Dynamic Voltage Restorer for Mitigating Voltage Sags in Power Systems

Dung VO TIEN[1], *Radomir GONO*[1], *Zbigniew LEONOWICZ*[2], *Trinh TRAN DUY*[3], *Luigi MARTIRANO*[4]

[1]Department of Electrical Power Engineering, Faculty of Electrical Engineering and Computer Science, VSB–Technical University of Ostrava, 17. listopadu 15/2172, 708 33 Ostrava-Poruba, Czech Republic
[2]Faculty of Electrical Engineering, Wroclaw University of Science and Technology, Wybrzeze Stanislawa Wyspianskiego 27, 50-370 Wroclaw, Poland
[3]Faculty of Electric Power Systems, Vinh University of Technology Education, Hung Dung street, Vinh, Vietnam
[4]Department of Electrical Engineering, Sapienza University of Rome, Piazzale Aldo Moro 5, 00185 Rome, Italy

dung.vo.tien.st@vsb.cz, radomir.gono@vsb.cz, zbigniew.leonowicz@pwr.edu.pl, duytrinhktv@gmail.com, luigi.martirano@uniroma1.it

DOI: 10.15598/aeee.v16i1.2350

Abstract. *The paper presents a vector control with two cascaded loops to improve the properties of Dynamic Voltage Restorer (DVR) to minimize Voltage Sags on the grid. Thereby, a vector controlled structure was built on the rotating dq-coordinate system with the combination of voltage control and the current control. The proposed DVR control method is modelled using MATLAB-Simulink. It is tested using balanced/unbalanced voltage sags as well as fluctuant and distorted voltages. As a result, by using this controlling method, the dynamic characteristics of the system have been improved significantly. The system performed with higher accuracy, faster response and lower distortion in the voltage sags compensation. The paper presents real time experimental results to verify the performance of the proposed method in real environments.*

Keywords

Current controller, dynamic voltage restorer, power quality, voltage controller, voltage sags, Voltage Source Converter (VSC).

1. Introduction

Voltage sags are one of the most common events that affect power quality in the distribution system. The major causes of voltage sags are faults of a grid, such as a single line to the ground, phase to phase, two-phase to the ground, three-phase faults due to accidents, lightning, wind, animals, and other causes. Other causes include transformer energizing, switching capacitor banks, and the starting of large induction motors [6] and [12]. Voltage sags can be symmetric or asymmetric depending on the causes of sags.

Although voltage sags occur in a short time (from 0.5 cycle to 1 minute) [11], it may affect the operation of equipment (stalling of motors, tripping of sensitive loads, and inaccuracy of control devices). These effects can give a rise in serious production problems, causing huge economical losses for consumers. According to an investigation of Schneider Electric in [13], voltage sags were the largest power quality problems in US distribution system, as shown in Fig. 1. It is also a serious problem in Vietnam electric power system.

There are many methods for mitigating voltage sags, such as UPS (Uninterruptible Power Supply), SVC (Static VAR Compensator), DSTATCOM (Distribution-Static Compensator), DVR (Dynamic Voltage Restorer). The structure of SVC is simpler than DVR but it has the incapability to control active power flow. The energy capacity of the DVR is higher than that of the UPS which has the same power rating. Additionally, the size of a DVR is smaller than that of the DSTATCOM. Furthermore, it is the cheapest in comparison with the UPS and the DSTATCOM

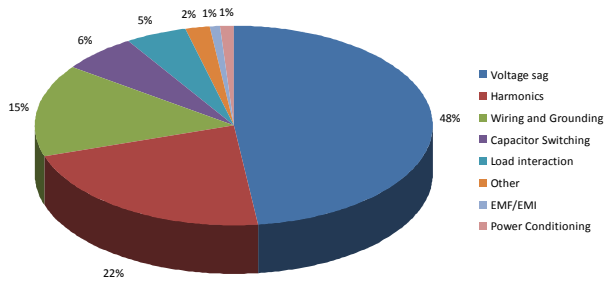

Fig. 1: Most common power quality issues (U.S.).

[1], [7]. Therefore, DVR is widely considered as an effective device in mitigating voltage sags.

This paper is arranged as follows. The proposed vector control with two cascaded loops method is discussed in details in Sec. 2. In Sec. 3. the simulation model using MATLAB-Simulink is illustrated for this control strategy. One part of the real time experimental result is represented in Sec. 4. Finally, conclusions are given in Sec. 5.

2. Proposed Control Method

2.1. Configuration of DVR

The general structure of a DVR consists of a booster transformer, a harmonic filter, a Voltage Source Converter (VSC), an energy storage and a control system. The control system is responsible for creating the injected voltage $u_{inj}(t)$ that can be restored the voltage at the Point of Common Coupling (PCC) with a preset value during the voltage sags. Detailed discussion of principles and operations of the DVR can be found, e.g., in [2] and [3].

The three-phase diagram of a grid with DVR is shown in Fig. 2. Where:

- $u_{sa}(t), u_{sb}(t), u_{sc}(t)$ are the three-phase voltages of the source.
- $u_{ga}(t), u_{gb}(t), u_{gc}(t)$ and $i_{ga}(t), i_{gb}(t), i_{gc}(t)$ are the grid voltages and the grid currents at PCC, respectively.
- $u_{inv,a}(t)$, $u_{inv,b}(t)$, $u_{inv,c}(t)$ and $i_{fa}(t)$, $i_{fb}(t)$, $i_{fc}(t)$ are the three-phase voltages and currents of the VSC, respectively.
- $u_{Ca}(t), u_{Cb}(t), u_{Cc}(t)$ and $i_{Ca}(t), i_{Cb}(t), i_{Cc}(t)$ are the filter capacitor voltages and currents, respectively.
- $u_{inj,a}(t), u_{inj,b}(t), u_{inj,c}(t)$ and $i_{inj,a}(t)$, $i_{inj,b}(t)$, $i_{inj,c}(t)$ are the voltages and currents injected by the DVR, respectively.
- $u_{dc}(t)$ is the DC-link voltage.
- $u_{La}(t), u_{Lb}(t), u_{Lc}(t)$ are the load voltages.

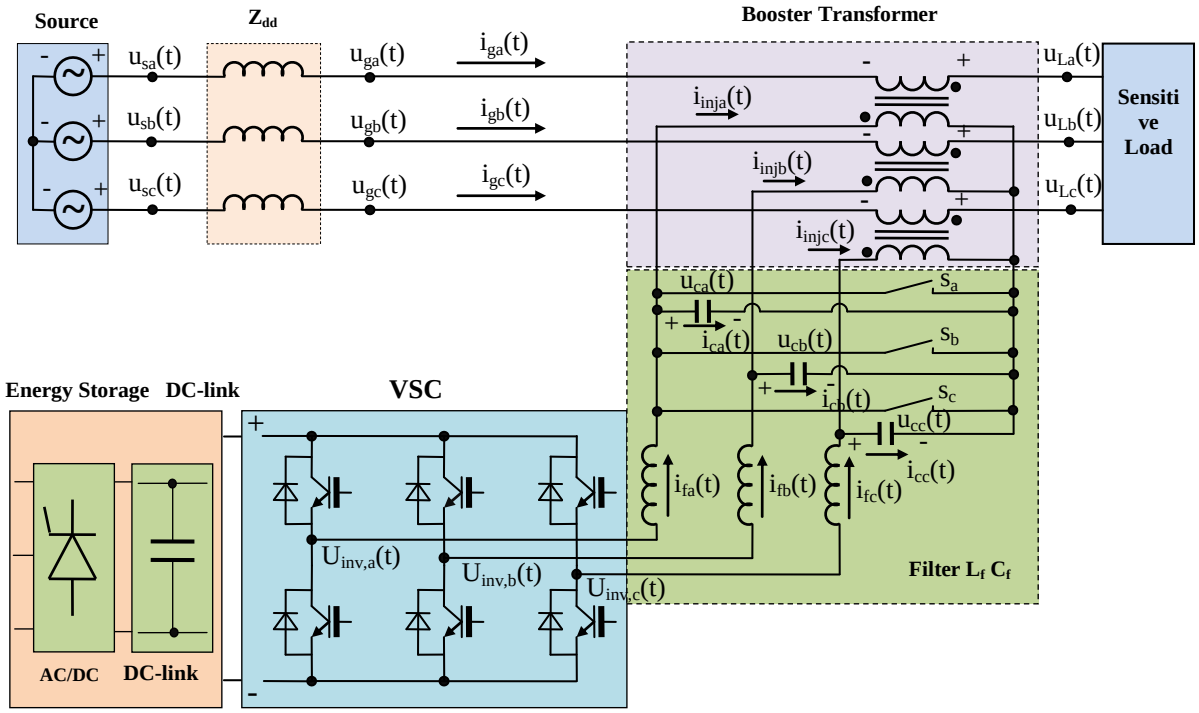

Fig. 2: Three-phase diagram of a grid with the dynamic voltage restorer.

The DVR functions by transferring the voltage sags compensation value from energy source through the booster transformer after the filter to restore the nominal voltage. This means that the differential voltage between PCC and reference voltage is appeared when the voltage disturbance occurs in the grid caused by any events, an equivalent voltage generated by the VSC should be compensated and injected through the booster transformer. The possibility of compensating voltage sags of a particular DVR depends on many factors including different types of voltage sags, different load conditions and the power rating that is supplied to the DVR.

2.2. Mathematical Modelling of DVR

From structural diagram of DVR, to reduce the complication of modeling, assuming the injection transformer is considered ideal with a 1:1 turn ratio. The one phase diagram of the grid connected VSC is shown in Fig. 3, where u_{invx} and i_{fx} are voltage and current of VSC, u_{Cx} and i_{Cx} are voltage and current of the filter, u_{injx} and i_{injx} are injected voltage and injected current. Applying Kirchhoff's law:

$$i_{fx}(t) = i_{Cfx}(t) + i_{injx}(t) = C_f \frac{\mathrm{d}}{\mathrm{d}t} u_{injx}(t) + i_{injx}(t), \quad (1)$$

$$u_{invx}(t) - u_{injx}(t) - R_f i_{fx}(t) - L_f \frac{\mathrm{d}}{\mathrm{d}t} i_{fx}(t) = 0. \quad (2)$$

By applying Clarke's transformation, Eq. (1) and Eq. (2) can be written in the α, β - coordinate system as:

$$\frac{\mathrm{d}}{\mathrm{d}t} i_f^{(\alpha\beta)}(t) = \frac{1}{L_f} u_{inv}^{(\alpha\beta)}(t) - \frac{1}{L_f} u_{inj}^{(\alpha\beta)}(t) - \frac{1}{L_f} R_f i_f^{(\alpha\beta)}(t), \quad (3)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} u_{inj}^{(\alpha\beta)}(t) = \frac{1}{C_f} i_f^{(\alpha\beta)}(t) - \frac{1}{C_f} i_{inj}^{(\alpha\beta)}(t). \quad (4)$$

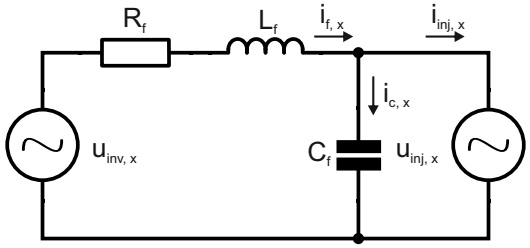

Fig. 3: One phase diagram of the grid connected VSC.

After manipulation of these equations, the following state-space model is obtained:

$$\frac{\mathrm{d}}{\mathrm{d}t} x(t) = Ax(t) + Bu(t) + Ed(t), \quad (5)$$

$$y(t) = Cx(t), \quad (6)$$

where

$$x(t) = [i_f^{\alpha}, i_f^{\beta}, u_{inj}^{\alpha}, u_{inj}^{\beta}]^T, u(t) = [u_{inv}^{\alpha}, u_{inv}^{\beta}]^T,$$

$$d(t) = [i_{inj}^{\alpha}, i_{inj}^{\beta}]^T, y(t) = [u_{inj}^{\alpha}, u_{inj}^{\beta}]^T,$$

$$A = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ -\frac{1}{C_f} \end{bmatrix},$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}.$$

The block diagrams for Eq. (5) and Eq. (6) are shown in Fig. 4.

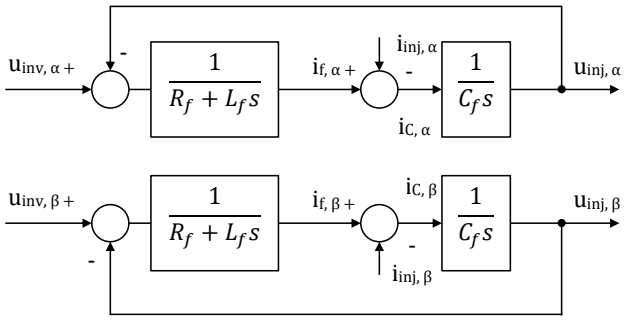

Fig. 4: Block diagrams of controller in the $\alpha\beta$ - coordinate system.

Re-writing the Eq. (5) and Eq. (6):

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_f^{(\alpha\beta)} \\ u_{inj}^{(\alpha\beta)} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_f^{(\alpha\beta)} \\ u_{inj}^{(\alpha\beta)} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} [u_{inv}^{(\alpha\beta)}] + \begin{bmatrix} 0 \\ -\frac{1}{C_f} \end{bmatrix} [i_{inv}^{(\alpha\beta)}], \quad (7)$$

$$u_{inj}^{(\alpha\beta)} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_f^{(\alpha\beta)} \\ u_{inj}^{(\alpha\beta)} \end{bmatrix}. \quad (8)$$

By transforming coordinate system from $\alpha\beta$ - to dq - with a PLL (Phase-Locked Loop) synchronized with the grid voltage vector, Eq. (3) and Eq. (4) becomes:

$$\frac{\mathrm{d}}{\mathrm{d}t} u_{inj}^{(dq)}(t) = \frac{1}{C_f} i_f^{(dq)}(t) - \frac{1}{C_f} i_{inj}^{(dq)}(t) \pm j\omega \cdot u_{inj}^{(dq)}(t), \quad (9)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_f^{(dq)}(t) = \frac{1}{L_f} u_{inv}^{(dq)}(t) - \frac{1}{L_f} u_{inj}^{(dq)}(t) - \frac{1}{L_f} R_f i_f^{(dq)}(t) \mp j\omega . L_f i_f^{(dq)}(t), \quad (10)$$

where:

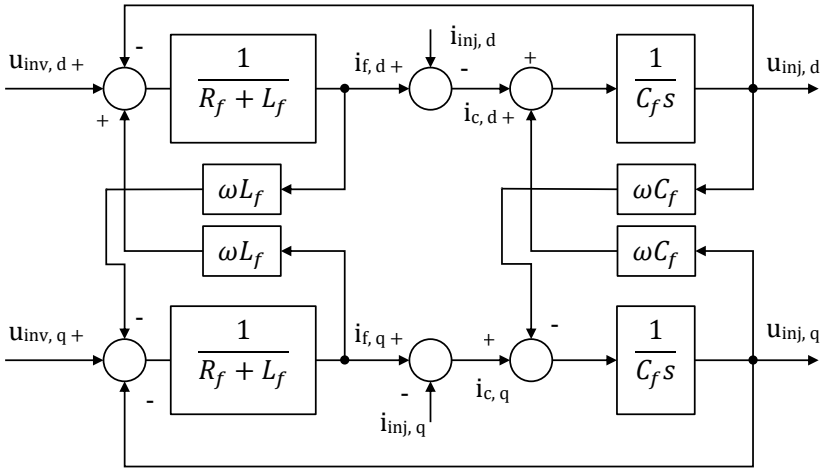

Fig. 5: Block diagrams of controller in the dq - coordinate system.

- $i_f^{(d)}, i_f^{(q)}$ are d and q components of current of the VSC;
- $u_{inj}^{(d)}, u_{inj}^{(q)}$ are d and q components of injected voltages;
- $u_{inv}^{(d)}, u_{inv}^{(q)}$ are d and q components of voltages of VSC in dq-coordinate system;
- $i_{inj}^{(d)}, i_{inj}^{(q)}$ are d and q components of injected current in dq-coordinate system.

Equation (9) and Eq. (10) can be rewritten as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_f^{(d)} \\ i_f^{(q)} \\ u_{inj}^{(d)} \\ u_{inj}^{(q)} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & \omega & -\frac{1}{L_f} & 0 \\ -\omega & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 & 0 & \omega \\ 0 & \frac{1}{C_f} & -\omega & 0 \end{bmatrix} \begin{bmatrix} i_f^{(d)} \\ i_f^{(q)} \\ u_{inj}^{(d)} \\ u_{inj}^{(q)} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_{inv}^{(d)} \\ u_{inv}^{(q)} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -\frac{1}{C_f} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix} \begin{bmatrix} i_{inj}^{(d)} \\ i_{inj}^{(q)} \end{bmatrix}. \tag{11}$$

The block diagrams for Eq. (11) are shown in Fig. 5.

To derive the voltage controller to be implemented in a digital controller, it is necessary to discretize Eq. (9) and Eq. (10). This is done by integrating the equation over one sample period T_s and then dividing by T_s, thus obtaining:

$$\frac{1}{T_s}(u_{inj}^{(dq)}(k+1) - u_{inj}^{(dq)}(k)) = \frac{1}{C_f} i_f^{(dq)}(k) - \frac{1}{C_f} i_{inj}^{(dq)}(k) \pm j\omega u_{inj}^{(dq)}(k), \tag{12}$$

$$\frac{1}{T_s}(i_f^{(dq)}(k+1) - i_f^{(dq)}(k)) = \frac{1}{L_f} u_{inv}^{(dq)}(k) - \frac{1}{L_f} u_{inj}^{(dq)}(k) - \frac{1}{L_f} R_f i_f^{(dq)}(k) \mp j\omega u_{inj}^{(dq)}(k). \tag{13}$$

Vector controller analysis and designs, its problems and possible solutions can be found, e.g., in [4], [8], [9], [10] and [14].

3. Control Strategy of the DVR

Figure 6 shows the proposed control strategy is developed based on vector controller method performed on dq- and $\alpha\beta$ - coordinates system with double loops, the outer loop is voltage controller and the inner loop is current controller. Both voltages and currents are analyzed by their sequence components and two separated controllers are used, the voltage controller can restore the load voltage both under balanced and unbalanced conditions of the grid voltage, the current controller can regulate the injected currents and improve response and operate properly of DVR.

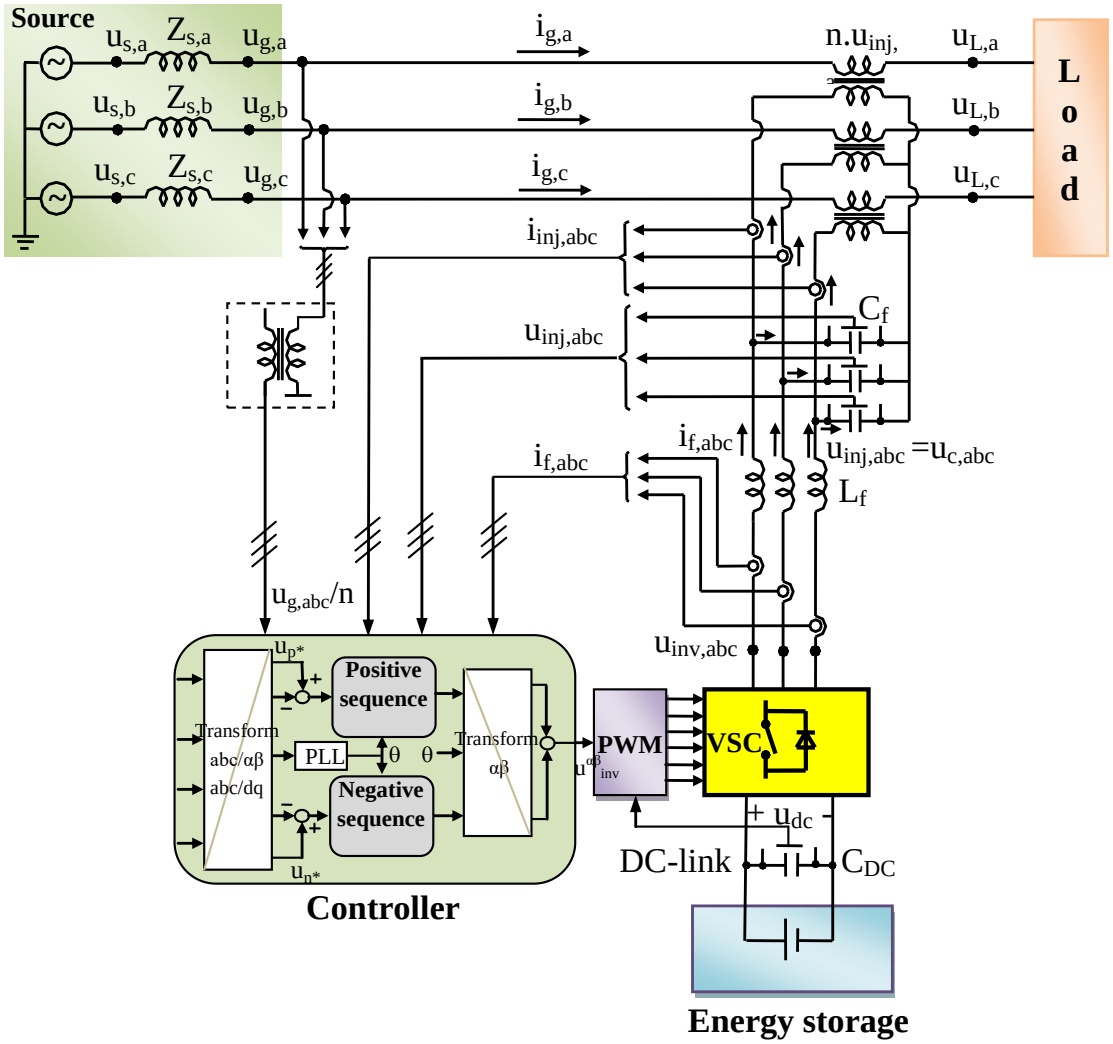

Fig. 6: Control scheme of DVR applications for mitigating voltage.

3.1. Voltage Controller - Outer Loop

Using PI controller, Eq. (12) can be written as follows:

- with positive components:

$$i_f^{(dq+)}(k+1) = i_{inj}^{(dq+)}(k) + G_{PI}^{P}\frac{C_f}{T_s}(u_{inj}^{(dq*+)}(k) - u_{inj}^{(dq+)}(k)) + j\pm\omega C_f u_{inj}^{dq-}(k), \quad (14)$$

- with negative components:

$$i_f^{(dq-)}(k+1) = i_{inj}^{(dq-)}(k) + G_{PI}^{N}\frac{C_f}{T_s}(u_{inj}^{(dq*-)}(k) - u_{inj}^{(dq-)}(k)) + j\mp\omega C_f u_{inj}^{dq+}(k), \quad (15)$$

where G_{PI}^{P} and G_{PI}^{N} are integral gain of the voltage controller for positive and negative components, respectively. The output of the voltage controller is the reference current i^{dq*}. Figure 8 shows the schematic structure of voltage controller.

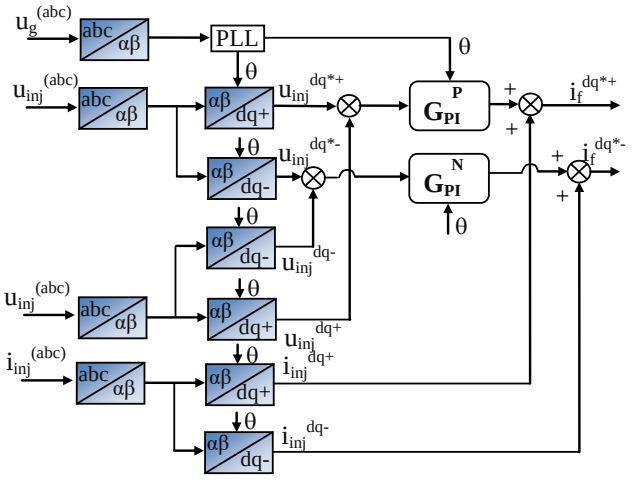

Fig. 8: Schematic structure of voltage controller in the rotating dq-coordinate system.

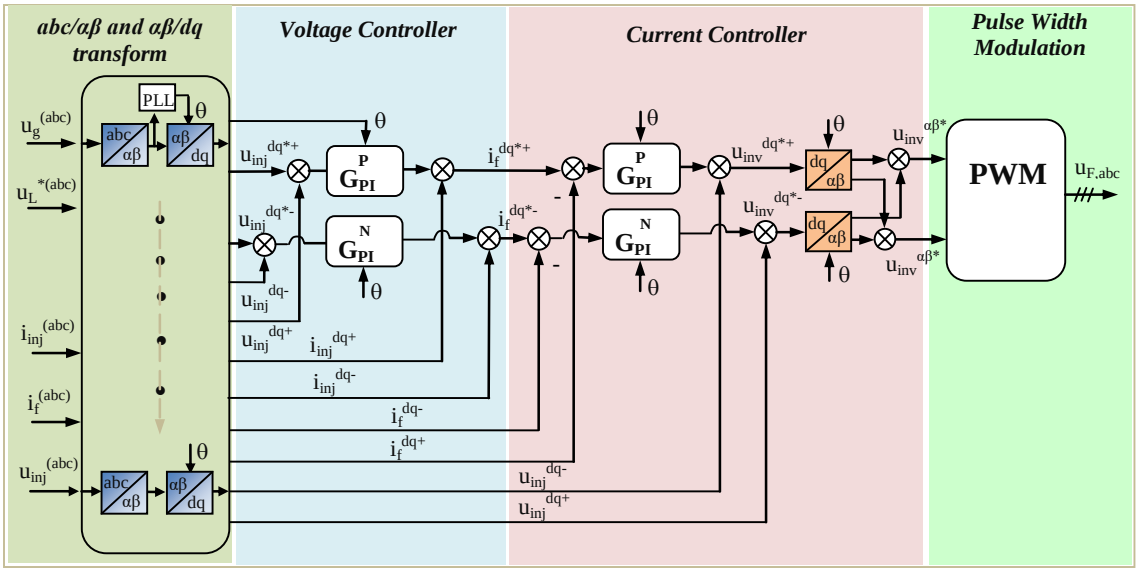

Fig. 7: Schematic structure of DVR in the rotating dq-coordinate system.

3.2. Current Controller - Inner Loop

Using PI controller, Eq. (13) can be written as follows:

- with positive components:

$$u_{inv}^{(dq+)}(k) = u_{inj}^{(dq+)}(k) + R_f i_f^{(dq+)}(k) \mp j\omega L_f if^{(dq-)}(k)$$

$$+G_{PI}^{P}\frac{L_f}{T_s}(i_f^{(dq*+)}(k+1) - i_{inj}^{(dq+)}(k)), \qquad (16)$$

- with negative components:

$$u_{inv}^{(dq-)}(k) = u_{inj}^{(dq-)}(k) + R_f i_f^{(dq-)}(k) \pm j\omega L_f if^{(dq+)}(k)$$

$$+G_{PI}^{N}\frac{L_f}{T_s}(i_f^{(dq*-)}(k+1) - i_{inj}^{(dq-)}(k)). \qquad (17)$$

The output of the current controller is the reference voltage u^{dq}. The schematic structure of the current controller is shown in Fig. 9.

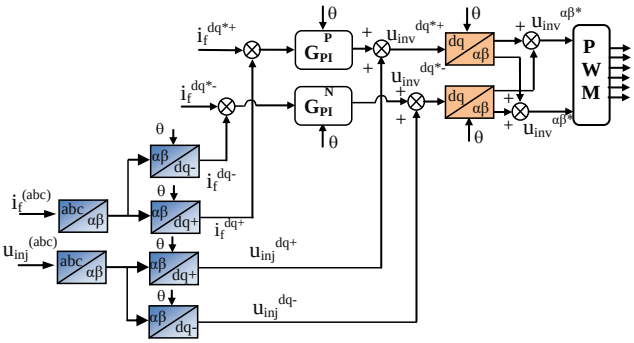

Fig. 9: Schematic structure of Current controller in the rotating dq-coordinate system.

Finally, cascaded double loop vector controller based on combining two separated controllers implemented in the positive and negative sequence, respectively, as shown in Fig. 7. This means that voltage and current on dq- and $\alpha\beta$ - coordinates system are separated into positive and negative sequences, the voltage controller and current controller are used independently, after that by transforming them into the fixed $\alpha\beta$ – coordinate system.

4. Simulation and Discussion

Three cases of distribution system based on real data are simulated using MATLAB-Simulink. The numerical data are taken from case study of co-author in an existing publication [5]. The cases of study can be represented as follows:

- Case I: Balanced voltage sags.
- Case II: Unbalanced voltage sags.
- Case III: Fluctuations and distortion voltages caused by Switching capacitor ON or OFF.

4.1. Case I: Balanced Voltage Sags

The balanced voltage sag occurs while three phases fault in the grid, during the period from 2 to 2.1 second. The voltage of the sensitive load is reduced by 50 % with respect to the reference voltage. Figure 10, shows grid voltage, injected voltage and load voltage respectively in three phase and d, q components in rotating dq - coordinate system. The error between d

and q components of designed injected voltage and real time experimental injected voltage is shown in Fig. 11. The information of voltage at PCC and load voltage in this case is presented in Tab. 1. It can be clearly seen that the DVR is doing nothing during normal operation but it quickly injects voltage components to restore the load voltage during voltage sag.

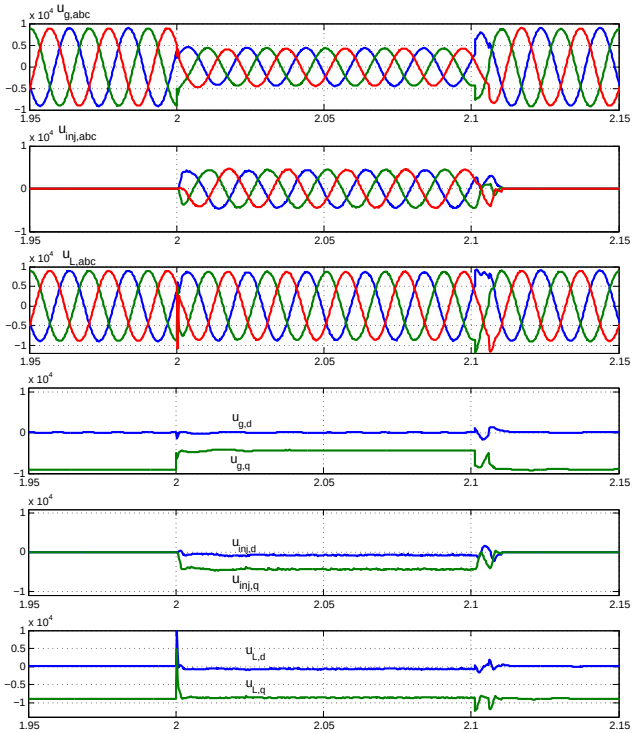

Fig. 10: Case I-The voltage in three phases and in the dq-coordinate system: from top to bottom traces are grid voltages, injected voltages, and load voltages.

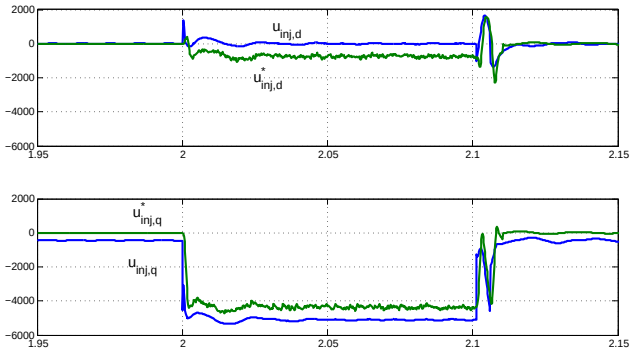

Fig. 11: Case I-The difference of d, q components between designed injected voltage and real time experimental injected voltage.

Tab. 1: RMS voltage of case I.

Voltage at PCC before sag (V)	Balanced Voltage sag at PCC (V)	Load voltage during sag (V)
6320	3180	6220

4.2. Case II: Unbalanced Voltage Sags

The unbalanced voltage sags are simulated and the results are shown in Fig. 12 and Fig. 13. The voltage sags due to unsymmetrical fault in transmission line started at 2 second and kept until 2.1 second, the period of voltage sags is 0.1 seconds. The voltage at the sensitive load is reduced 28 % in phase A, 35 % in

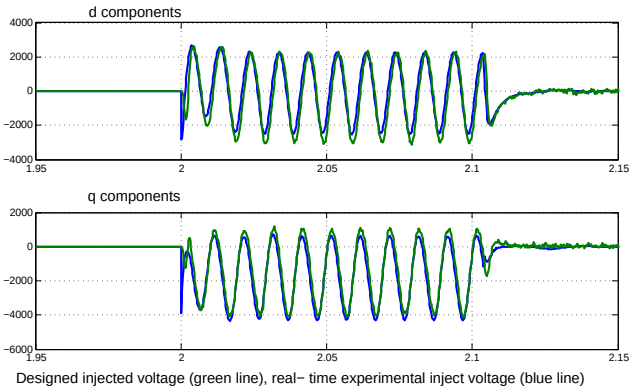

Fig. 12: Case II-The difference of d, q components between designed injected voltage and real time experimental injected voltage.

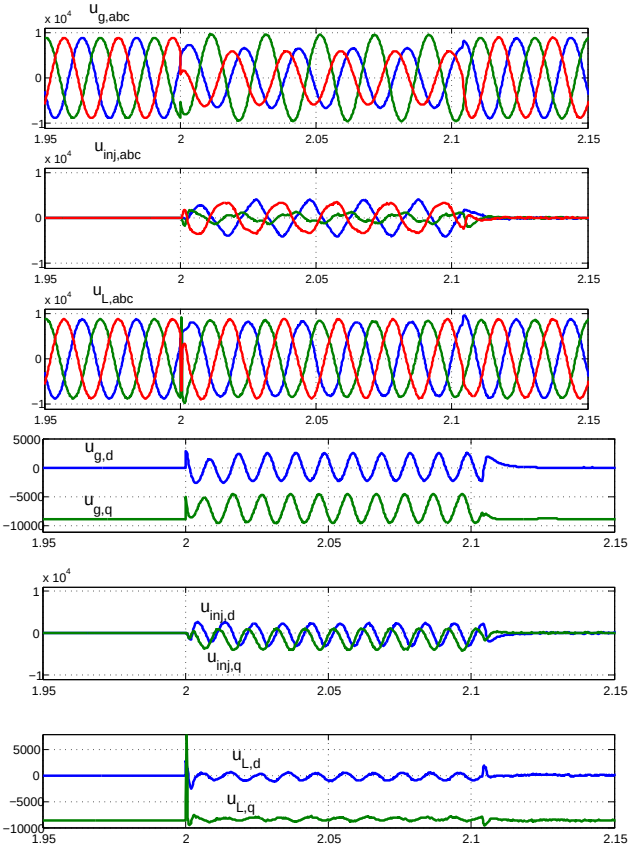

Fig. 13: Case II-The voltage in three phases and in the dq-coordinate system: from top to bottom traces are grid voltages, injected voltages, and load voltages.

phase C and little increased 10 % in phase B with respect to the reference voltage (see Tab. 2). Observing that, the injected voltage was produced by DVR can restore balanced voltage at the PCC despite of unbalanced voltage sags occurring in the grid.

Tab. 2: RMS voltage of case II.

Voltage at PCC (V)	Unbalanced voltage sag in phase			Load Voltage in phase		
	A (V)	B (V)	C (V)	A (V)	B (V)	C (V)
6320	4600	6750	4200	5900	5850	5940

4.3. Case III: Fluctuations and Distortion Voltages

Fluctuations and distortions voltages can occurred by switching the capacitor ON and OFF at the station. In this simulation, the capacitor was switched ON at 2 second and switched OFF at 3 second, the period of fluctuations and distortions is 1 second. The result of simulation is shown in Fig. 14 and Fig. 15 where

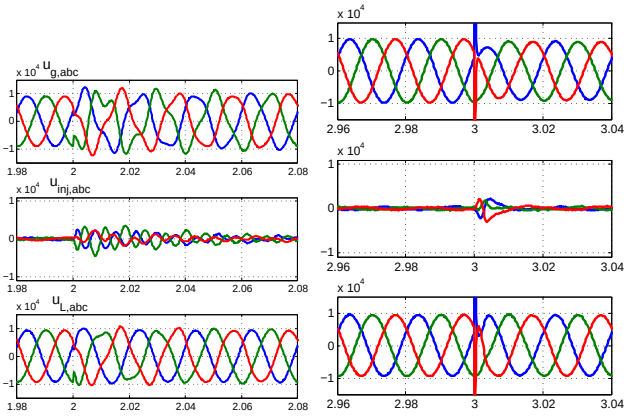

Fig. 14: Case III-The voltage in three phases: from top to bottom traces are grid voltages, injected voltages, and load voltages.

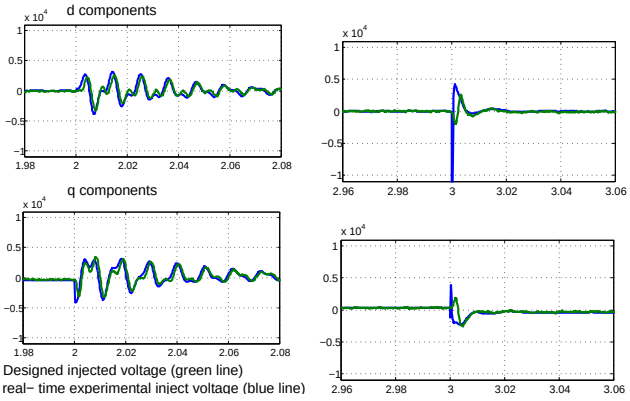

Fig. 15: Case III-The difference of d, q components between designed injected voltage and real time experimental injected voltage.

Fig. 14 shows source voltage, injected voltage and load voltage respectively in three phase and d, q components in rotating dq - coordinate system, Fig. 15 shows the difference between d and q component of designed injected voltage and real time experimental injected voltage. It can be seen that the DVR is capable to nearly maintain normal operation of load voltage after about 0.04 second (see Tab. 3).

Tab. 3: RMS voltage of case III.

Voltage at PCC before sag (V)	Fluctuations and Distortions voltage (V)	Load voltage during sag (V)
6320	6950	6450

5. Experimental Results

The experiment of proposed methods for mitigating balanced voltage sags was performed at the laboratory. Fig. 16 and Fig. 17 show the experimental setup and its elements. In this experiment, voltage at the sensitive load reduced by 50 % due to three-phase fault, during the period from 1.68 to 3.21 seconds. The result of experimental is shown in Fig. 18 and Fig. 19 where Fig. 18 shows source voltage, injected voltage and load voltage respectively in three phases, Fig. 19 shows d, q components in rotating dq - coordinate system.

Fig. 16: The picture of experiment setup.

6. Conclusion

In this paper, the summary of the mathematical representation and configuration of DVR for mitigating balanced voltage, unbalanced voltage sags, fluctuant voltage and distorted voltages was presented. The paper discussed the vector control with two cascaded loops technique to improve the properties of DVR.

Fig. 17: The VSC converter using Baumuller Servo-Power-Unit BUS 621, 622, 623, 624; nominal voltage 600V, nominal current 20 A.

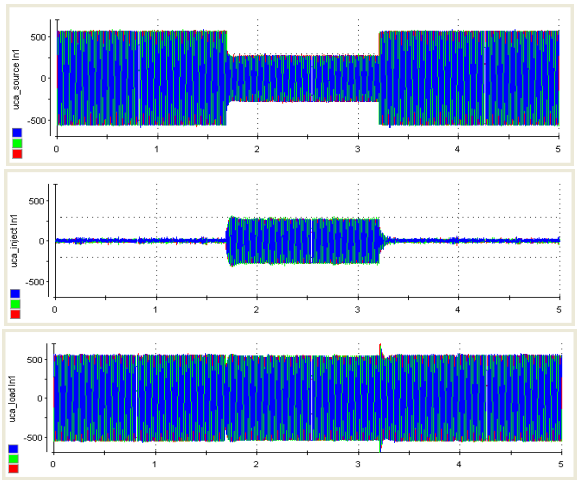

Fig. 18: Experimental results for balanced voltage sags: from top to bottom traces are source voltages, injected voltages, and load voltages.

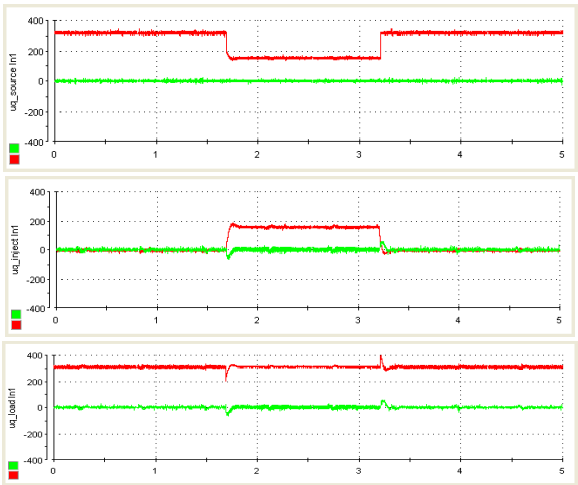

Fig. 19: Experimental results for balanced case: from top to bottom traces are voltage components on the *dq* - coordinate system of source, injected and load.

The proposed DVR control method was modeled using MATLAB-Simulink and tested in balanced, unbalanced voltage sags and fluctuant voltage and distorted of voltages. As a result, the system performed with higher accuracy, faster activated ability and lower distortion in the sags voltage compensator.

Experimental results from laboratory proved the correctness and effectiveness of proposed solutions.

Acknowledgment

Support by the University La Sapienza, Rome, Italy for Zbigniew Leonowicz is gratefully acknowledged.

This research was partially supported by the SGS grant from VSB–Technical University of Ostrava (No. SP2018/61) and by the project TUCENET (No. LO1404).

References

[1] DEVARAJU, T., V. C. VEERA REDDY and M. V. KUMAR. Performance of DVR Under Different Voltage Sag and Swell Conditions. *ARPN Journal of Engineering and Applied Sciences*. 2010, vol. 5, iss. 1, pp. 55–64. ISSN 1819-6608.

[2] RAJASEKARAN, D. and S. S. DASH. Mitigation of Voltage Sags and Voltage Swells by Dynamic Voltage Restorer. *International Journal of Electrical and Power Engineering*. 2011, vol. 5, iss. 3, pp. 139–143. ISSN 1990-7958.

[3] DASTAGIR, R., M. KHEMARIYA and A. BARVE. Simulation of the DVR for the Mitigation of Power Quality Problems. *International Journal of Electrical, Electronics and Computer Engineering*. 2015, vol. 4, iss. 2, pp. 30–33. ISSN 2277-2626.

[4] WANG, F., M. C. BENHABIB, J. L. DUARTE and M. A. M. HENDRIX. Sequence- Decoupled Resonant Controller for Three-phase Grid-connected Inverters. In: *Applied Power Electronics Conference and Exposition*. Washington: IEEE, 2009, pp. 121–127. ISBN 978-1-4244-2811-3. DOI: 10.1109/APEC.2009.4802643.

[5] DUY, T. T., D. V. TIEN, R. GONO and Z. LEONOWICZ. Mitigating Voltage Sags due to short circuits using Dynamic Voltage Restorer. In: *IEEE International Conference on Environment and Electrical Engineering*. Italy: EEEIC,

2016, pp. 2671–2676. ISBN 978-1-5090-2320-2. DOI: 10.1109/eeeic.2016.7555868.

[6] BOLLEN, M. H. J. *Understanding power quality problems - voltage sags and interruptions*. New York: IEEE Press, 2015. ISBN 0-7803-4713-7.

[7] GHOSH, A. and G. LEDWICH. *Power Quality Enhancement Using Custom Power Devices*. Boston: Kluwer Academic Publishers, 2002. ISBN 1-4020-7180-9.

[8] STRZELECKI, R. and G. BENYSEK. *Power Electronics in Smart Electrical Energy Networks*. London: Springer - Verlag Publishers, 2008. ISBN 978-1-84800-317-0.

[9] KAZMIERKOWSKI, M. P., R. KRISHNAN and F. BLAABJERG. *Control in Power Electronics*. New York: Elsevier Science Publishers, 2002. ISBN 0-12-402772-5.

[10] NIELSEN, J. G. *Design and Control of a Dynamic Voltage Restorer*. Aalborg: Aalborg University, Denmark Publishers, 2002. ISBN 90-77017-83-6.

[11] Recommended Practice for Monitoring Electric Power Quality. *IEEE Std 1159-1995*. 1995. DOI: 10.1109/IEEESTD.1995.79050.

[12] Testing and Measurement Techniques— Power Quality Measurement Methods. *IEC 61000-4-30*. 2003.

[13] Report of Schneider Electric. In: *Schneider Electric* [online]. 2017. Available at: `https://blog.schneider-electric.com/power-management-metering-monitoring-power-quality/`.

[14] BONGIORNO, M. *Control of Voltage Source Converters for Voltage Dip Mitigation in Shunt and Series Configurations*. Goteborg, 2004. Thesis. Chalmers University of Technology. Supervisor: Ambra Sannino and Jan Svensson.

About Authors

Dung VO TIEN received the M.Sc. degree in Electric Power Systems from HaNoi University of Science and Technology (HUST), Vietnam in 2007. He has been with the Department of Electrical Power Engineering, Vinh University of Technology Education, Vietnam. Since 2015, he has been pursuing a Ph.D. degree in Electrical Engineering at Technical university of Ostrava, Czech Republic. His current research interests are in the areas of power system analysis, reliability of electric power systems and power quality.

Radomir GONO (IEEE M'12-SM'16) received the M.Sc., Ph.D. and Habilitate Doctorate degrees, all in Electrical Power Engineering, in 1995, 2000, and 2008, respectively. He has been with the Department of Electrical Power Engineering, VSB–Technical University of Ostrava, Czech Republic, since 1999 where he currently holds the position of Associate Professor and Vice-head of the department. He works also as a Senior researcher of the research centre - Energy Units for Utilization of non Traditional Energy Sources at the same university. His current research interests are in the areas of electric power systems reliability, optimization of maintenance and renewable energy sources.

Zbigniew LEONOWICZ (IEEE M'03–SM'12) received the M.Sc., Ph.D. and Habilitate Doctorate (Dr Sc.) degrees, all in Electrical Engineering, in 1997, 2001, and 2012, respectively. He has been with the Department of Electrical Engineering, Wroclaw University of Science and Technology, Poland, since 1997 where he currently holds the position of Associate Professor. His current research interests are in the areas of power quality, control and protection of power systems, renewables, industrial ecology and applications of advanced signal processing methods in power systems.

Trinh TRAN DUY received the M.Sc. and Ph.D. degrees, all in Electrical Engineering, in 2006 and 2014, respectively. He has been with the Department of Electrical Power Engineering, Vinh University of Technology Education, Vietnam, since 2008 where he currently holds the position of Head of the department. His current research interests are in the areas of power quality, control and automation of power systems and renewable energy sources.

Luigi MARTIRANO (IEEE M'02–SM'11) received the M.Sc. and Ph.D. degrees, in Electrical Engineering, in 1998 and 2003, respectively. He has been with the Department of Electrical Engineering, Sapienza University of Rome (Italy), since 2000 where he currently holds the position of Associate Professor. His current research interests are in the areas of power systems design, planning, safety, lightings, home and building automation, energy management. He is a senior member of the IEEE/IAS, member of the CEI (Italian Electrical Commission) Technical Committees CT205 (Home and Building Electronic Systems) and CT315 (Energy Efficiency) and member of the European CENELEC Joint Working Group CEN/CLC JWG9 "Energy measurement plan for organizations".