DESIGN OF A SCALABLE NANO UNIVERSITY SATELLITE BUS
(ILLINISAT-2 BUS)
COMMAND AND DATA HANDLING SYSTEM AND POWER SYSTEM

BY

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THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Aerospace
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2018

Urbana, Illinois

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ABSTRACT

IlliniSat-2 bus is the second generation of a general model on which multiple-production of CubeSats are based upon. The IlliniSat-2 bus consists of Command and Data Handling system, Power Generation and Distribution system, Attitude Determination and Control system and Radio system. The IlliniSat-2 is required to be capable of operating a nanosatellite from size 1.5U (10x10x17cm) to 6U (10x22.6x36.6cm) and carrying up to three science payloads. The challenge with IlliniSat-2 bus is the requirement for the wide-range scalability. The major contribution of this work includes the requirements, design, testing, and validation of two parts of the IlliniSat-2 bus systems: Command and Data Handling system and Power Generation and Distribution system. This work also contributes the lessons learned throughout the implementation of the flight hardware. So far, five missions are using IlliniSat-2 bus to carry their science payloads: LAICE, CubeSail, SpaceICE, SASSI^2 and CAPSat. CubeSail satellite was fully constructed and delivery to the launcher on April 12th, 2018. The tentative launch date as of this publication is August 31st, 2018. SpaceICE, SASSI^2 and CAPSat are three missions developed as parts of the NASA Science Mission Directorate's (SMD) Undergraduate Student Instrument Program (USIP). Those three satellites are being constructed as of this publication and will be delivered to perspective launchers by the end of August. LAICE satellite was constructed and is awaiting to be delivered to the launch in November 1st, 2018.

ACKNOWLEDGEMENTS

The following work would not be possible without the guidance and persistent help from my advisor, Professor Alexander Ghosh. He introduced me to CubeSat four years ago, since then he has been a guiding light in the path of my career development. His constant encouragement built my confidence as an electrical and systems engineer for spacecrafts. I am eternal grateful to have Alex looking after me over the past four years, not only my academic and research performance, but also my overall well-being.

I would also like to thank Professor Gary Swenson for offering continuous support throughout my CubeSat experience. He took me under his wing after my undergraduate degree and hired me to work on the LAICE CubeSat for a year. That year was one of the happiest years of my life. Gary, you changed my life for the better.

The work presented would not have been possible without the efforts of the three generations of students that I had the honor to work with. I want to especially thank the entire USIPs team, who right now are probably working hard to get the three satellites delivered to NASA: I had such a great time working with you guys during this summer. I am so proud of what we accomplished together in these short two months. You are the future of University of Illinois' CubeSat project. I wish you all the best.

Finally, I would like to recognize the unending support of my parents and my girlfriend. Mom and dad, I know it must be hard having your son away from you in a different continent for seven years, thank you for giving me this opportunity; thank you for never losing faith in me; thank you for raising me up to be an honest, loyal and hardworking person. Ashley, thank you for reviewing my thesis; thank you for being a constant voice of encouragement. This work, I dedicate to you all!

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION & BACKGROUND

This work describes the second-generation design of the electrical system of a satellite bus for University of Illinois at Urbana-Champaign. The bus is given the name IlliniSat-2. IlliniSat-2 bus is designed to be 10x10x7.5cm(0.75U) in size. It is designed to be scalable from 1.5U to 6U in size according to CubeSat Standard[1][2] and capable of providing power and data communication up to three scientific payloads.

Currently, five missions are flying with IlliniSat-2 bus carrying their scientific payloads: LAICE, CubeSail, SpaceICE, SASSI^2 and CAPSat. CubeSail was already constructed and delivered to the launcher, the tentative launch date is later in 2018. SpaceICE, SASSI^2 and CAPSat CubeSats are being developed as a part of the NASA Science Mission Directorate's (SMD) Undergraduate Student Instrument Program (USIP). They are finishing testing and construction as the thesis is getting deposited. Those three missions will be delivered to NASA at the end of August. LAICE is constructed and currently in the process of acquiring an FCC license and the tentative delivery date is November 1st 2018.

This work discusses the requirements, design, testing, and validation of two parts of the IlliniSat-2 bus systems: Command and Data Handling (C&DH) system and Power Generation and Distribution system (Power System). Further, multiple bus software or firmware systems will be developed herein, including validation of the C&DH Linux kernel and the power distribution and monitoring firmware. The work also discusses the software used to design flight hardware and manufacturers used to manufacture flight hardware.

This thesis is dedicated to IlliniSat-2 bus hardware. From C&DH system, to Power Generation and Distribution system involving solar panels, battery pack and Power Board. The

thesis will first present the overall IlliniSat-2 bus architecture, then it goes over descriptions of each mission and the requirements for the IlliniSat-2 bus's C&DH and power system, then it will dig into the methods involved to implement a common hardware design which can meet the needs of multiple missions with very little variation. Each of the subsequent chapters are dedicated to a specific system or subsystem's design, implementation and testing. Finally, the thesis will discuss the processes used to design and manufacture IlliniSat-2 hardware and software, as well as the lessons learned from the development of C&DH system and power system.

CHAPTER 2: IlliniSat-2 BUS AND MISSION OVERVIEW

2.1 IlliniSat-2 Overview

The IlliniSat-2 bus is broken down into 4 main electrical systems: Command and Data Handling (C&DH) system, Power Generation and Distribution system, Attitude Determination and Control System (ADCS) and Radio system. The Power Generation and Distribution system is broken down into power generation, power storage, power regulation and distribution subsystems. The ADCS system is broken down into determination, control, and interface subsystems.

2.2 Service Stack
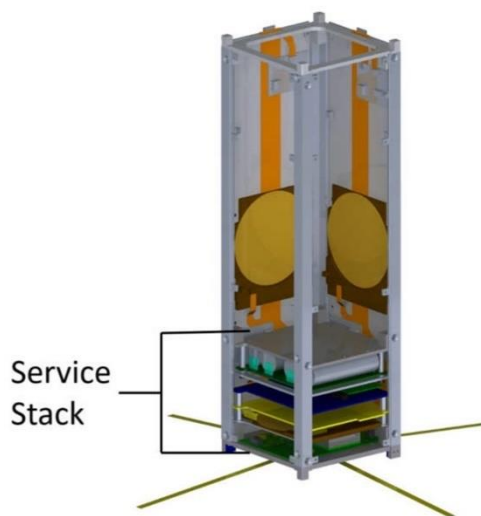
Figure 1: IlliniSat-2 Service Stack

The four IlliniSat-2 main systems form a satellite service stack. The service stack is installed in the bottom-most unit of the satellite structure. The service stack is comprised of (from top to bottom) the Battery Pack Printed Circuit Board (PCB), command and data handling board, Power Board, 2 Z-axis Torque Coil boards, radio mounting board, and various harnesses for each of these subsystems. A flexible circuit interfacing and magnetometer board, a Torque Coil board

and a gyroscope board are assembled behind each solar panel and plugged in to the Power Board. The total size of the service stack is 90 x 90 x 75mm excluding the structures, which is the size of 0.75U satellite. A completed service stack is depicted in Figure 1. The orientation of the IlliniSat-2 is defined in Figure 2. The long wall of the satellite is defined as the wall with one solar panel chain attached.
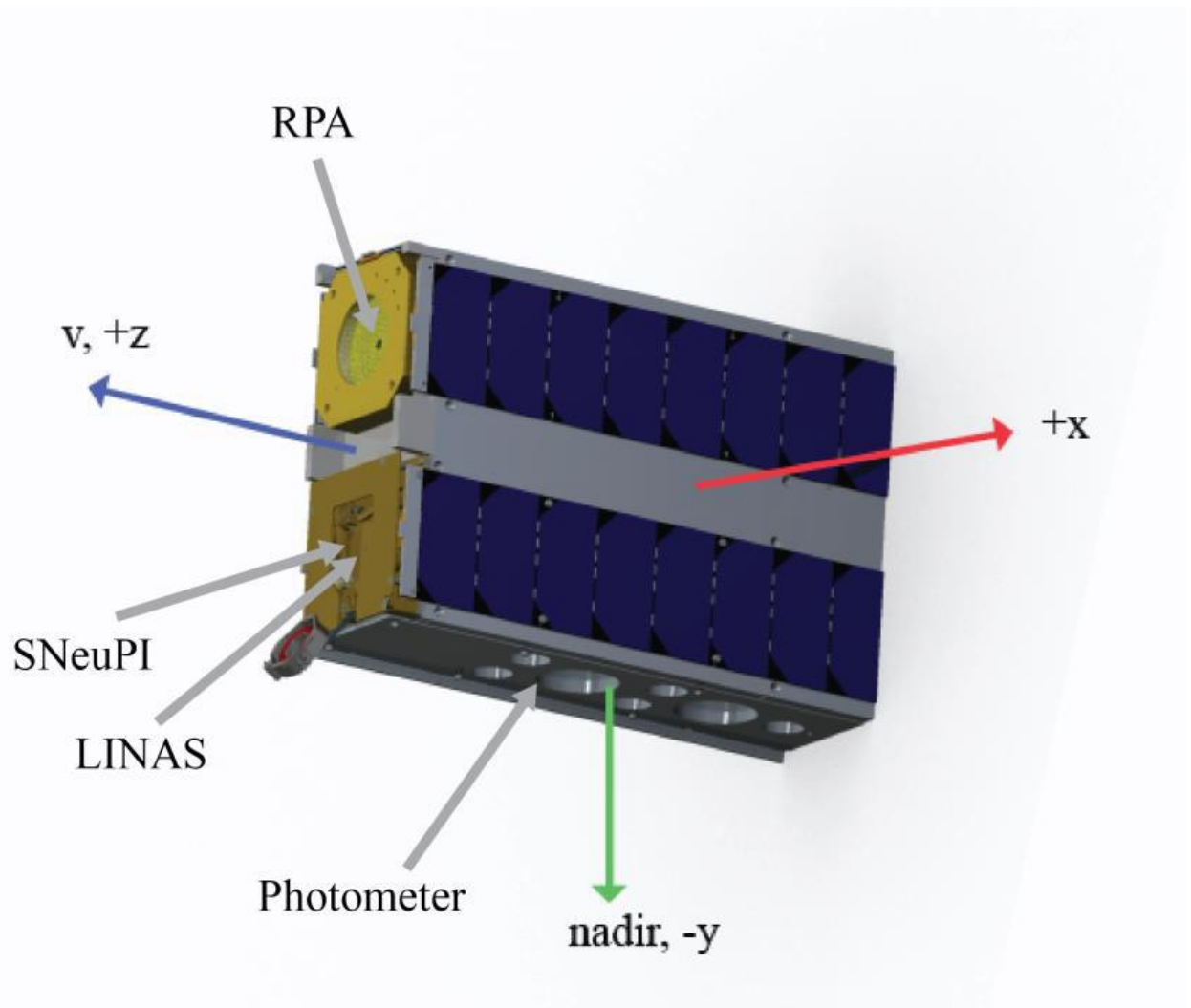
Figure 2: IlliniSat-2 Orientation

2.2.1 Command and Data Handling (C&DH)
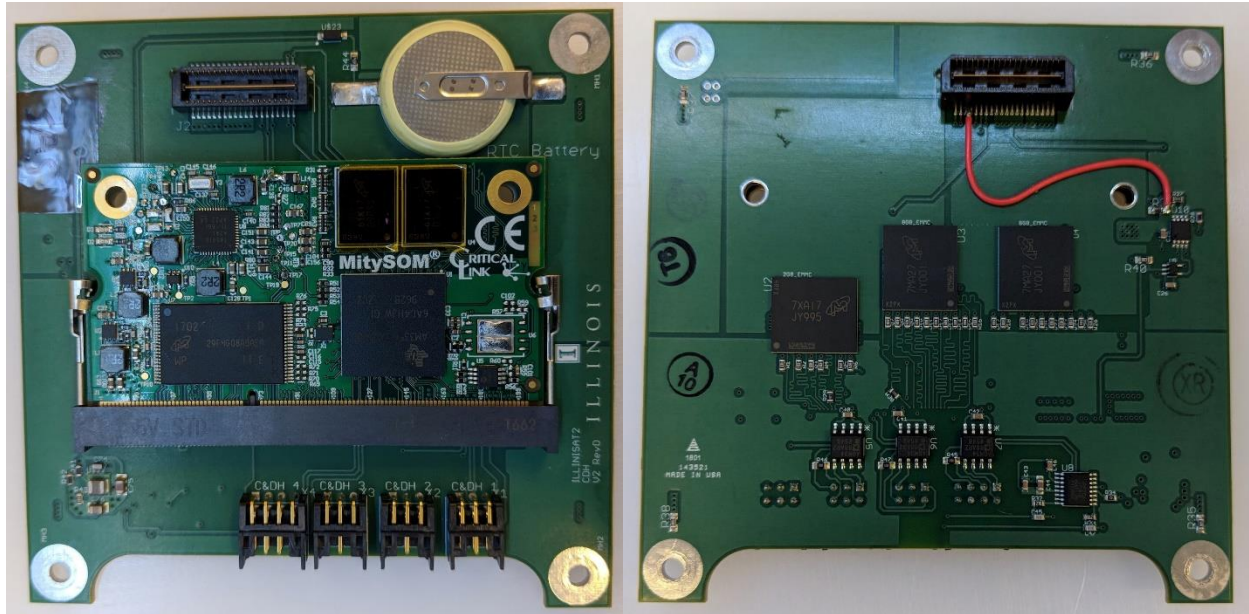
Figure 3: C&DH PCB Top (left) and Bottom (right)

The Command and Data Handling system is the brain of the satellite. In terms of data management, the C&DH collects and processes information about all subsystems and payloads. In terms of attitude determination and control, the C&DH calculates the spacecraft's attitude and carries out maneuvers to change the attitude. In terms of radio communication, The C&DH carries out commands sent from earth and prepares data for transmission to earth. The key parts of the system are the space flight computer, data storage units and flight software. Pictures of the C&DH system is shown in Figure 3.

2.2.2 Power Generation and Distribution

The Power Generation and Distribution system, short for power system, is the power plant of the satellite. This system generates power from solar photovoltaic cells. It then regulates the solar-cell-generated power into a level acceptable to charge a lithium-ion battery pack and stores the energy into the battery pack. The power system further distributes the regulated battery power

into rest of the subsystems and payloads while monitors the current consumption of the power distributions. Routinely, the power distribution subsystem will calculate the current percentage of the battery pack and enters the satellite into different power modes suitable for the battery level.

2.2.2.1 Power Generation - Solar Panel
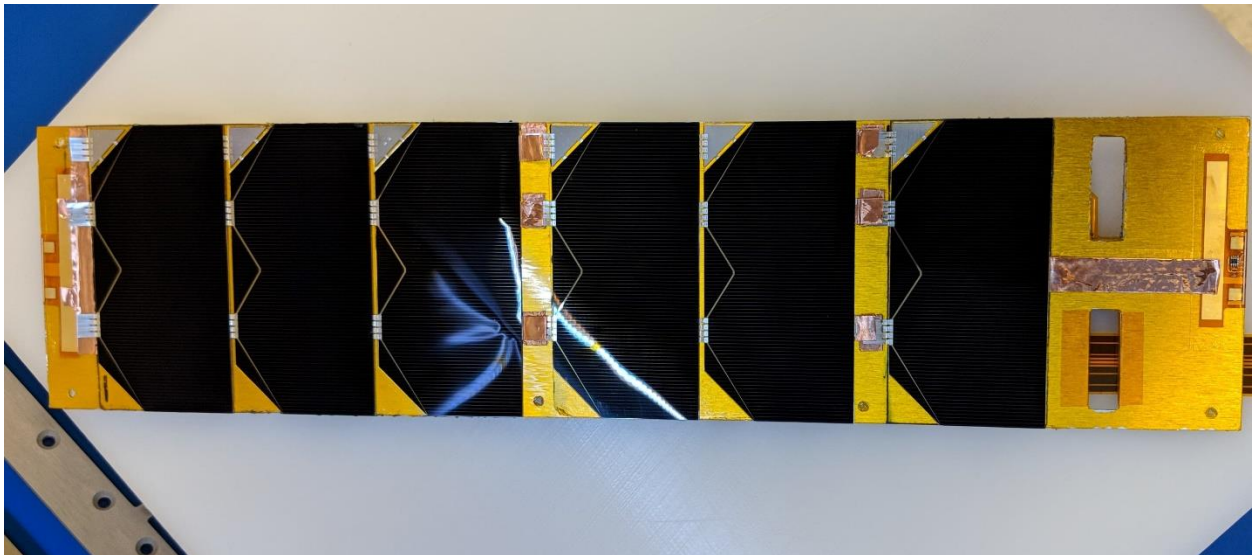
Figure 4: Constructed Solar Panel

IlliniSat-2 generates power through the use of solar photovoltaic cells (often called solar cells). these cells are a class of electrical device that converts the energy of light into electricity by the photovoltaic effect. The solar cells are constructed together into a solar cell chain and mounted onto the satellite wall to form a solar panel. A picture of a complete solar panel is shown in Figure 4.

2.2.2.2 Power Storage - Battery Pack
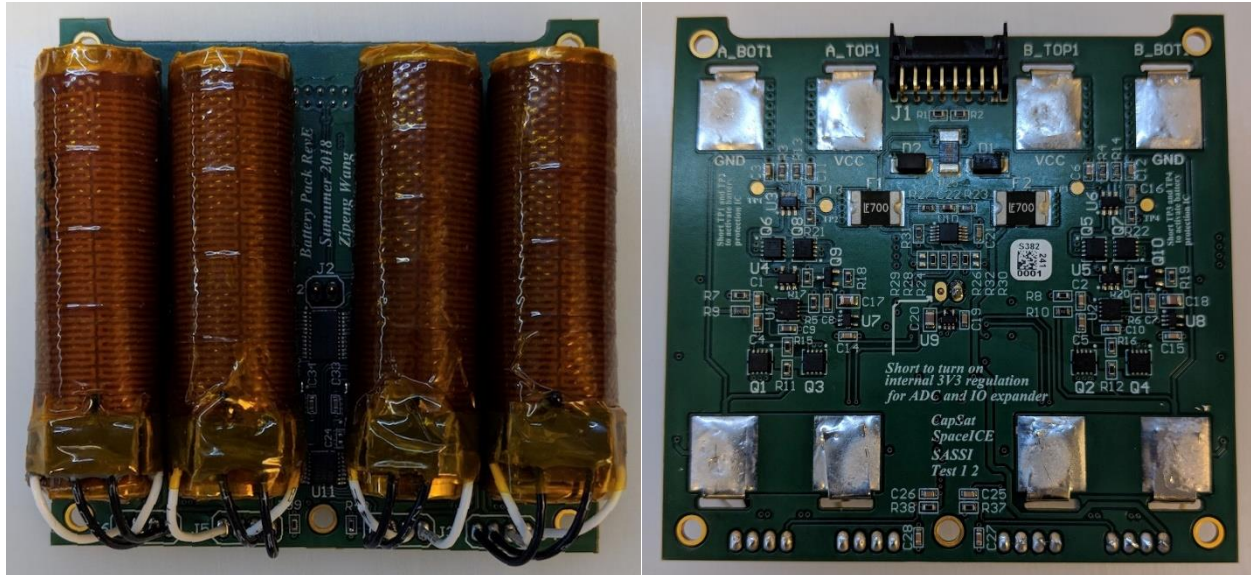
Figure 5: Assembled Battery Pack Top (left) and Bottom (right)

IlliniSat-2 bus stores solar-generated energy into a lithium ion battery pack. Each of the batteries are assembled to include a Kapton heater for temperature regulation. The battery pack contains over-charge, under-charge and external-short protection to ensure the safe operation of the battery cells. The battery pack also maintains the balancing of cell's State of Charge (SoC) to maximize the charge/discharge efficiency. Several digital measurement and control Integrated Circuits (ICs) are included in the battery pack to communicate with the Power Board. Pictures of the Battery Pack is shown in Figure 5.

2.2.2.3 Power Regulation and Distribution - Power Board
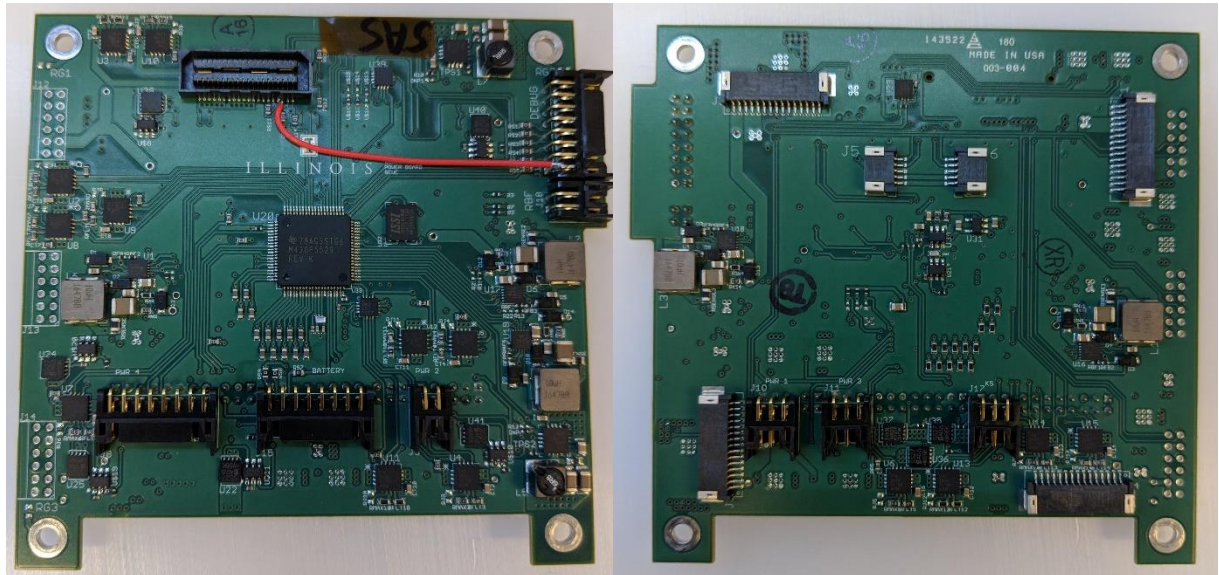
Figure 6: Power Board Top (left) and Bottom (right)

IlliniSat-2 bus regulates and distributes all the power through the Power Board. The Power Board regulates the solar power into battery power, then further regulate the battery power into 3.3V power. The Power Board distributes the battery power and 3.3V power to the rest of the subsystems and monitors the current consumption on each of distribution line.

On the Power Board, there is a microcontroller that runs software to control the initial power state of the satellite after deployment. The software communicates with C&DH's for the purpose of health monitoring. It also answers C&DH's commands to turn on/off subsystems and payloads. The software detects overcurrent fault situations on the subsystems and payloads. It routinely updates the battery's state of charge then enter the satellite into different power states.

The Power Board mates with C&DH to form part of the service stack. Pictures of the Power Board is shown in Figure 6.

2.2.3   Attitude Determination and Control System (ADCS)

The Attitude Determination and Control System is the arms and legs of the satellite. The ADCS determines the satellite's attitude or orientation and points the satellite towards the desired position for charging or scientific or ground communication purpose.

2.2.3.1 Attitude Control - Torque Coil
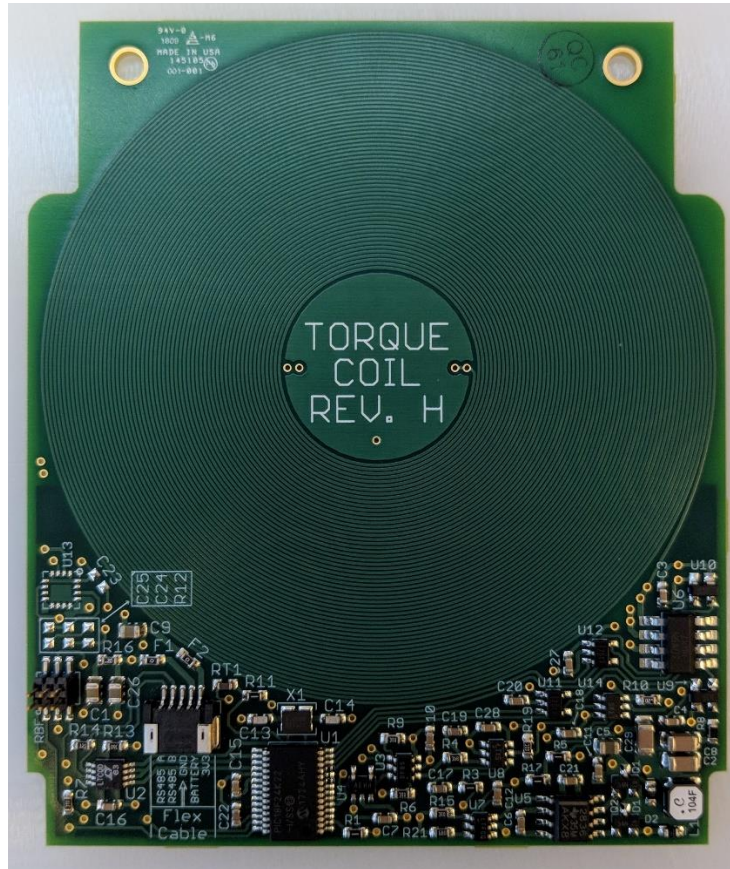
Figure 7: Torque Coil PCB

The Torque Coil controls the satellite's attitude by generating a magnetic moment that interacts with earth's magnetic field, creating a torque. The Torque Coil sets the current level and direction through the command of C&DH and passes that current into a coil to generate the

desired magnetic moment. The Torque Coils are included in the X, Y and Z directions for 3-axes attitude control. A picture of the Torque Coil is shown in Figure 7.

2.2.3.2 Attitude Determination – Magnetometer
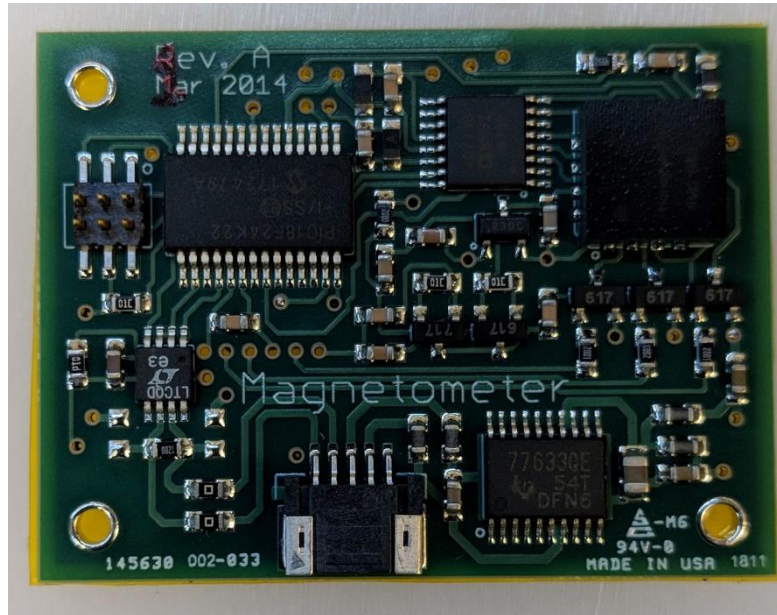
Figure 8: Magnetometer PCB

The Magnetometer is part of the attitude determination system of the satellite. It measures the magnetic field strength in X, Y and Z directions. The Magnetometer passes the measured data on to the C&DH for the purpose of attitude determination. A picture of the Magnetometer is shown in Figure 8. While each magnetometer can measure all three axes, a standard Illinisat-2 bus has multiple of them for redundancy.

2.2.3.3 Attitude Determination – Gyroscope
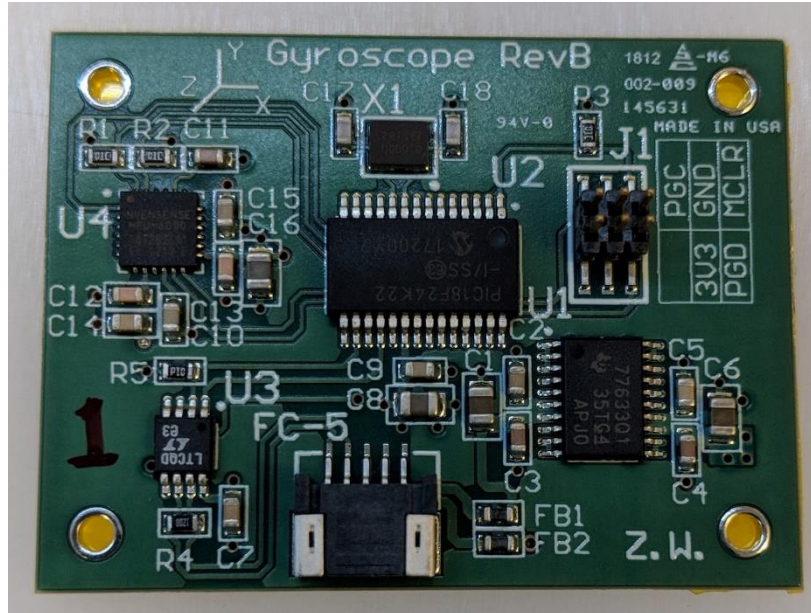
Figure 9: Gyroscope PCB

The Gyroscope is part of the attitude determination system of the satellite. It contains an

Inertial Measurement Unit (IMU) that measures the rotation rate of the satellite as well as

acceleration in X, Y and Z axes. The Gyroscope passes the measured data on to the C&DH for

the purpose of attitude determination. As with the magnetometer, redundant backups are flown.

A picture of the gyroscope is shown in Figure 9.

2.2.3.4 ADCS Interface - Flex Cable
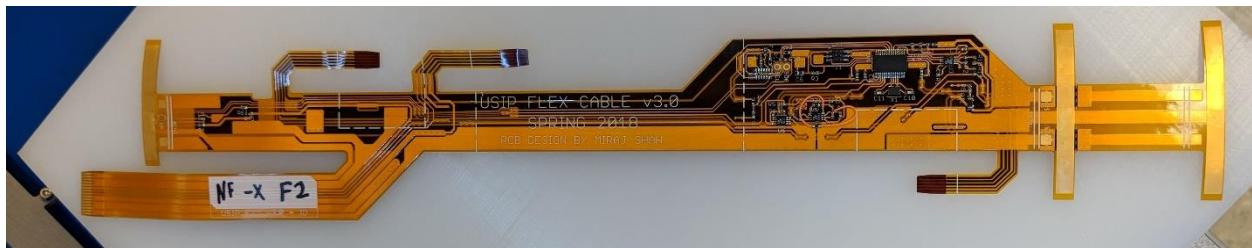
Figure 10: Flex Cable PCB

Figure 11: Flex Cable assembled with ADCS devices, and glued to the solar panel

The Flex Cable acts like an interconnect between the service stack and the ADCS system. Each Flex Cable connects a torque coil, a magnetometer and a gyroscope to distribute power from the power board and commands from C&DH. A picture of the Flex Cable is shown in Figure 10.

Besides having the purpose of interfacing ADCS devices. The Flex Cable is also in charge of delivering solar panel power to the power board and monitoring the health of satellite wall. In 1.5U CubeSat (CubeSail)'s case, the Flex Cable has a more important role of regulating the solar voltage to a level acceptable by the solar charger.

The Flex Cable is glued to the backside of the solar panel along with the attached ADCS devices. Together, the assembly forms the final solar panel design. A picture of the backside of the assembled solar panel is shown in Figure 11.

2.2.4 Radio

Figure 12: Radios Selected for IlliniSat-2: From left to right, AstroDev Lithium Radio, GlobalStar EyeStar D-2 Radio, GOMSpace NanoCom AX100 Radio

The Radio subsystem is the mouth and ear of the satellite. The Radio subsystem is in charge of establishing communication between the earth ground station and the satellite. The ground station uplinks commands through the Radio subsystem to the C&DH. The C&DH performs the received commands and downlink the data through the Radio subsystem to the ground station. The three radios shown in Figure 12 are the radios used for different missions that flew with IlliniSat-2 bus.

2.3   Mission Descriptions

As Illinisat-2 is designed to support generic science with very little hardware change, it is important to understand the practical needs of the existing five missions, and how they influenced the requirements for each system. To that end, the following sections will talk about each mission and their scientific goals.

2.3.1 LAICE

Figure 13: LAICE Pictures After Construction.

The Lower Atmosphere/Ionosphere Coupling Experiment (LAICE) is the first Earth satellite to exclusively investigate the energy and momentum of waves produced by low-atmosphere weather system. Pictures of assembled LAICE satellite is shown in Figure 13. LAICE is built into a 6U CubeSat, and be compliant with NASA Educational Launch of Nanosatellites(ELaNa) launch standards and procedures[3]. The LAICE CubeSat will be delivered to International Space Station and launched into a near circular orbit between 350 and 450 km, depending on International Space Station altitude at the time of release. The desired mission duration is approximately two years in order to provide adequate longitudinal and local time coverage over four different seasons.

LAICE is a collaborated effort between University of Illinois and Virginia Tech. There are two primary science goals for the LAICE mission:

1. Systematically observe gravity waves with large vertical wavelengths at lower F-region heights, and correlate on a global scale remotely-sensed wave-induced airglow perturbations in the upper mesosphere with in-situ measurements of ion and neutral density fluctuations at higher altitudes.

2. Produce global maps of active gravity wave regions in the mid- and low-latitude ionosphere over multiple seasons at all local times, so that global patterns and climatological variations can be quantitatively compared to and correlated with terrestrial weather systems via ray-trace modeling.[4]

LAICE satellite is required to carry three payloads: University of Illinois Photometer Payload, Virginia Tech Payloads(LIIB, LINAS, SNeuPI and RPA) and Cadet L-3 Radio. The Photometer Payload requires 2.7W power during active science operations. The Virginia Tech Payloads require 4.16W power during active science operations. The Cadet Radio requires 9W of power during transmit. Each payload require a dedicated communication with C&DH.

The satellite size is 6U, 10 x 22.6 x 36.6cm.

The expected delivery date for LAICE is November 1st, 2018.

2.3.2 CubeSail
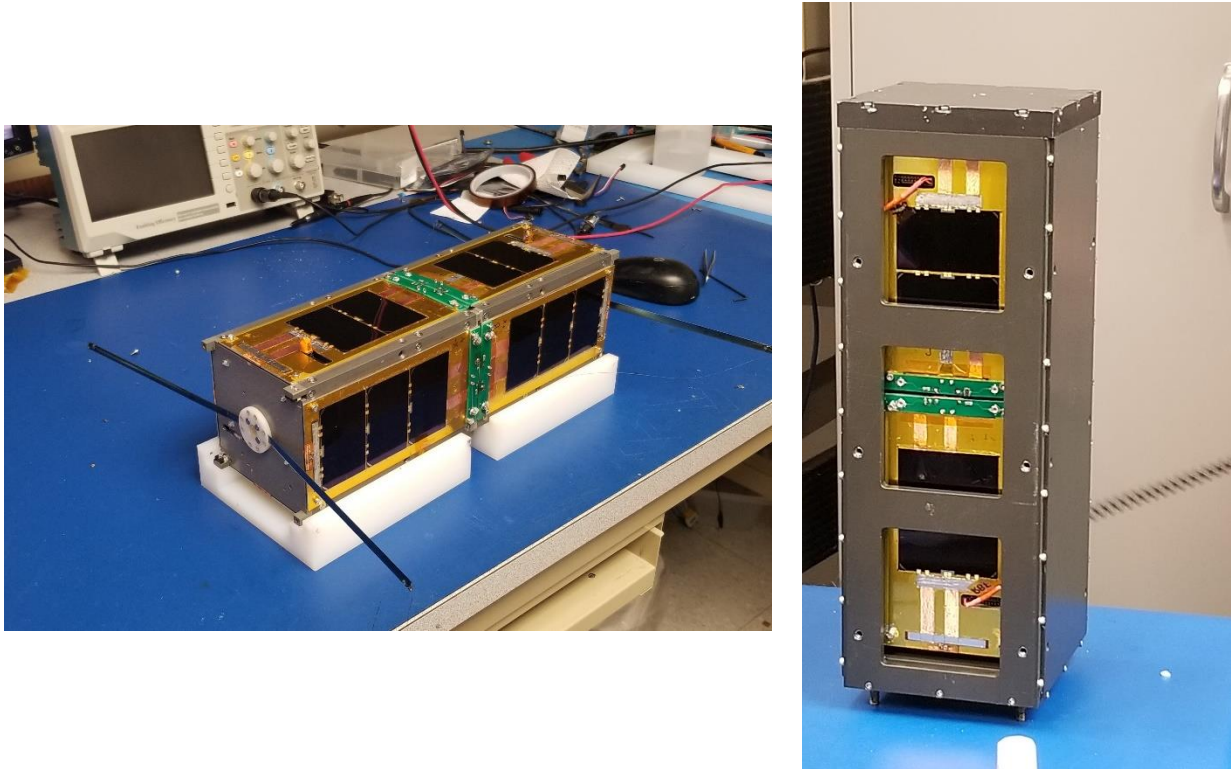
Figure 14: CubeSail Pictures. Shown left is the mated, fully constructed CubeSail satellite. Right is the satellite assembled into launcher's pod.

CubeSail is a CubeSat mission to demonstrate in-space deployment of solar sail technology. Pictures fully assembled CubeSail satellite is shown in Figure 14. CubeSail is 3U in size. During its operation, it will separate into two 1.5U CubeSats with a 250-meter-long, 8-centimeter-wide solar ribbon deployed between them. The orientation of the 1.5U CubeSat at either end will be used to control the orientation of the sail and achieve "propellant-less" solar sail. CubeSail is a collaborated effort between University of Illinois and CUAerospace. CubeSail mission goals are successful sail deployment, attitude control and deorbit.

Each unit of CubeSail carries one science payload for solar sail deployment and a 320x240 camera to record the event. The payload consumes 4W of power during its one-time deployment

event. The camera consumes 0.2W during recording. The payload and camera both require their own dedicated UART channel for communication.

The satellite size is 3U, 10 x 10 x 34.5cm.

CubeSail was delivered to Rocket Lab on April 12th, 2018. The tentative launch date as of this publication is August 31st, 2018.

2.3.3 SpaceICE

Figure 15: SpaceICE CAD Model

Interface Convective Effects (SpaceICE) is a 3U CubeSat mission designed to investigate freeze-casting in the microgravity environment of Low Earth Orbit (LEO). A complete CAD model for SapceICE is shown in Figure 15. Freeze-casting is a directional solidification technique that is used to fabricate porous materials with anisotropic, aligned pore structures. The SpaceICE mission aims to improve terrestrial fabrication of these materials by better understanding the role of gravity during the solidification process.

SpaceICE is a collaborated effort between University of Illinois and Northwestern University. There are two primary science goals for the SpaceICE mission:

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1. Improve Earth-based processing by building a better fundamental understanding of processing/microstructure relationships in freeze-casting materials and producing benchmark data to improve modeling efforts of the solidification process; and

2. Advance the freeze-casting technique as an in-situ resource utilization (ISRU) technology.[5]

SpaceICE will carry one science payload and a vibration motor. Specification for those payloads are unknown as of now due to redesigns.

The satellite size is 3U, 10 x 10 x 34.5cm.

The expected delivery date as of this publication for SpaceICE is August 6th, 2018.

2.3.4   SASSI^2
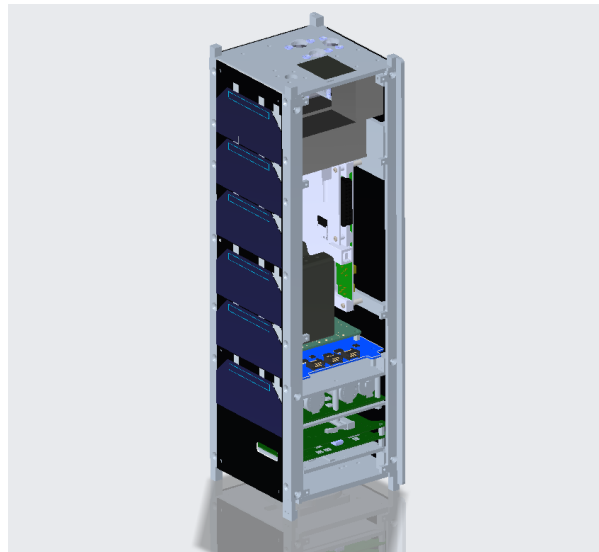
Figure 16: SASSI^2 CAD Model

Student Aerothermal Spectrometer Satellite of Illinois and Indiana (SASSI^2) is a small satellite mission scheduled to be flown in 2018. This mission is being developed as a part of the NASA Science Mission Directorate's (SMD) Undergraduate Student Instrument Program (USIP). A complete CAD model for SASSI^2 is shown in Figure 16. The goal of the mission is to

characterize the flow field and radiation generated by the diffuse bow shock formed during high-speed flight through the upper atmosphere. Optical spectrographic measurements of the radiation will be taken to provide data for fundamental flow, radiation, and materials modelling, resulting in improved prediction of the aerothermodynamic environment encountered by bodies during atmospheric entry.[6]

SASSI^2 is required to carry three payloads: STS-VIS Spectrometer, STS-UV Spectrometer and Purdue Sensor Payload. The three payloads share the same power interface and data interface, but are required to provide one extra power channel and one extra data channel for redundancy purpose. The maximum power consumption of SASSI^2 payload is 1.38W.

The satellite size is 3U, 10 x 10 x 34.5cm.

The expected delivery date as of this publication for SASSI^2 is August 15th, 2018.

2.3.5 CAPSat

Figure 17: CAPSat CAD Model

The Cooling, Pointing, Annealing Satellite (CAPSat) is a 3U CubeSat under development by the University of Illinois as a part of the Undergraduate Student Instrument Program (USIP). A complete CAD model for CAPSat is shown in Figure 17. CAPSat is expected to operate with one year of lifetime. It encompasses three technology demonstrations, each advancing the technology readiness level of NASA roadmap technologies. The experiments are: strain-actuated deployable panels for improved pointing control and jitter reduction, an active thermal control system, and single-photon avalanche detectors (SPADs) to test methods of mitigating space radiation damage.[7]

CAPSat is required to carry three scientific payloads, namely the cooling, pointing and annealing payloads. Each payload will have its own dedicated power and data channel. The cooling payload consumes 6.505W of power during its active operation. The annealing payload consumes 9.755W of power during its active operation. The pointing payload consumes 5W of power when it is active.

The satellite size is: 3U, 10 x 10 x 34.5cm.

The expected delivery date as of this publication for CAPSat is August 25th, 2018.

2.4 Electrical Master Requirements (for IlliniSat-2 Bus Design)

1. IlliniSat-2 bus shall be 0.75 U in size, meaning 10 x 10 x 7.5cm. IlliniSat-2 bus shall be able to support CubeSat missions with different form factors, from size 1.5U to 6U.

Mission	Payloads	Power Channel	Estimated Power Consumption(W)	Communication Channel
LAICE	UIUC Photometer	1	2.7	1
LAICE	Virginia Tech	1	4.16	1
LAICE	Cadet Radio	1	9	1
CubeSail	Solar Ribon Deployment	1	4	1
CubeSail	Camera	1	0.2	1
SpaceICE	Science	1	N/A	1
SpaceICE	Vibration Motor	1	N/A	0
SASSI^2	STS-VIS	2(Redundancy)	0.75	2(Redundancy)
SASSI^2	STS-UV		0.75	
SASSI^2	Purdue Sensor		1.38	
CAPSat	Cooling	1	6.505	1
CAPSat	Annealing	1	9.755	1
CAPSat	Pointing	1	5	1

Table 1: Science Payloads for Each Mission and Their Power and Communication Requirement

2. IlliniSat-2 bus shall be capable of providing power and communication interfaces to support up to three scientific payloads in accordance to Table 1.

3. IlliniSat-2 bus shall provide connector interfaces that are physically resistant to 10 root mean square acceleration (gmrs) level of vibrational damage[8].

4. IlliniSat-2 bus shall provide a central computer that communicates with all the subsystems, collect data, control the satellite's orientation, and control the radio to uplink and downlink data.

5. IlliniSat-2 bus shall provide at least 4GB of storage space for science data, and 4GB of storage space for redundancy.

6. IlliniSat-2 bus shall be capable of recharging the batteries on board the spacecraft using solar panels.

7. IlliniSat-2 bus shall be capable of protecting each Lithium Ion's battery from over-charge(4.25V), under-charge(2.5V), over-temperature(50C), under-temperature(10C) and external short conditions.

Channel	Max Load Current(A)
3.3V_Flex_Cable	1
3.3V_C&DH	1.5
3.3V_Payload_1	1
3.3V_Payload_2	1
3.3V_Radio	1
3.3V_Payload_3	1
Battery_Pyro	3
Battery_Flex_Cable	2
Battery_C&DH	1
Battery_Payload_1	1.5
Battery_Payload_2	2
Battery_Radio	1.5
Battery_Payload_3	1
Battery_Payload_4	1.5

Table 2: IlliniSat-2 Power Channel Distribution Requirement Table

8. IlliniSat-2 bus shall provide 14 total channels of power generation and distributions in accordance to Table 2.

9. IlliniSat-2 bus shall detect fault conditions of subsystems and payloads.

10. IlliniSat-2 bus shall include 3 switches that shut down the satellite when it is assembled in the P-POD.

11. IlliniSat-2 bus shall provide a remove before flight interface to cut the power to the rest of the satellite system once activated while still allow the batteries to be charged.

12. IlliniSat-2 bus shall provide externally-accessible debugging interfaces for its flight computer and power system.

CHAPTER 3: POWER AND DATA INTERFACES

3.1 Introduction

IlliniSat-2 design incorporates certain standard components such as harness connectors, mating connectors, and communication protocol transceiver ICs. The IlliniSat-2 has a standardized board stacking scheme called service stack, and a grounding scheme. This chapter will discuss the architecture of the satellite bus.

3.2 DF-11 connector

Figure 18: 6-pin DF-11 connector

DF-11 connectors are responsible data and power delivery from the service stack to the rest of the system. For data communication, the payloads and the radios connect to the C&DH board via right angled Hirose DF-11 connectors positioned along the cable trench. For power delivery, the battery, payloads and the radios connect to the Power Board via right angled Hirose DF-11 connectors positioned in the middle of the PCB facing the cable trench. Figure 18 shows a 6-pin DF-11 connector.

DF-11 series connector was chosen as the sole harness connector for IlliniSat-2 for two reasons: Firstly DF-11 has multiple features that target safe mating of the harness to the connector.

DF-11 connectors incorporate a simple lock system that locks the mated connectors. DF-11 connectors have ribs on 3 sides to indicate the correct insertion, and to prevent contact miss insertion as well as dissimilar contact insertion[9]. The second reason for choosing DF-11 is: they are space saving while still maintaining an acceptable current delivery rating. DF-11 connectors are double rows with 2mm pitch contact with a width of 5mm. Compared with standard 2.54mm pin header connectors, DF-11 saves 61% of space. Each pin on DF-11 is rated for 2A when the wire size is 22 to 26 AWG. While standard 2.54mm spaced pin headers have a current rating of 3A on each pin.

The downside of DF-11 is that the outgassing of insulating material outgasses. The general requirement for materials outgassing is Recovered Mass Loss (RML)<1.0% and Collected Volatile Condensable Materials (CVCM) < 0.1 % as per ECSS-Q-70. DF-11's insulating material is polyamide which is a water absorbing material. The Total Mass Loss (TML) for polyamide is often above 1%[10]. However, the water absorption is always reversible, and can be controlled by baking out the satellite before launch.

All the PCBs in the IlliniSat-2 bus use male-pin through-hole DF-11connectors with gold-plated pins. All the harnesses in the satellite use female-socket DF-11 mating connectors with gold plated crimps. Having gold-plated pin and crimps increases the lifetime of the connector. The usage of through-hole connectors on a PCB ensures structural rigidity.

3.3   Backbone connector

Figure 19: Backbone connector

The backbone connector provides standardized IlliniSat-2 interface between the Power Board and C&DH system. Figure 19 shows a picture of the backbone connector. On the C&DH board, the QTE-020-02-L-D-A connector sticks off the bottom of the carrier board and mates with the Power Board's QSE-020-02-L-D-A connector. The total mating height is 8mm which ensures the compactness of the service stack. The backbone connector passes along 3.3V and battery power, as well as 3 UART signal lines on the side pins. The ground connection is provided through the middle pin.

The backbone connector has 22 un-used pins, which are allocated for future expansion of the C&DH and Power Board. A mating connector QSE-020-02-L-D-A is also soldered on the top of the C&DH board to ensure versatility for future missions. This expansion feature is currently not in use for any of the missions.

3.4   Data communications
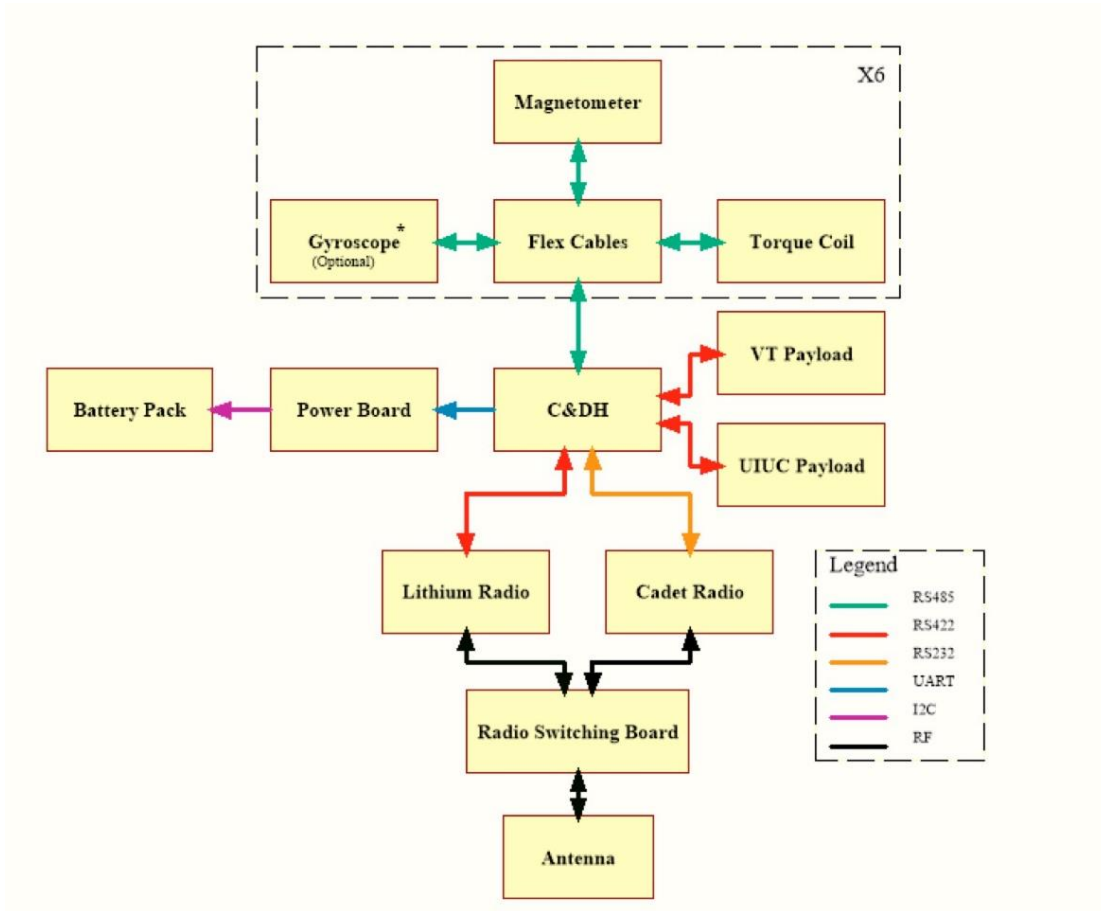
Figure 20: IlliniSat-2 Subsystem Communication Method

The flight computer communicates with the rest of the subsystems through 2-wire UART protocol. UART signals can be transferred with four choices of communication standards, TTL, RS232, RS422 and RS485, all of which are used in the IlliniSat-2 design. Among those four standards, only TTL is used for short range communication and involves no transceiver ICs. The other three are used for long distance communication and require dedicated transceiver ICs. Table 3 shows a rough comparison between RS232, RS422 and RS485 communication methods. Figure 20 shows the design of IlliniSat-2 communication system.

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3.4.1   Transistor-Transistor Level (TTL)

TTL is used on IlliniSat-2 for short communication between the flight computer and Power Board and between flight computer's debug port and the host computer. TTL performs direct communication between two devices at logic voltage level, which is 3.3V or 5V. The low communication voltage level means that the TTL communication distance is short, an estimation is that at maximum communication speed, 115200 bps. The data can be reliably transferred when the cable is less than half a meter. The voltage level for IlliniSat-2 TTL bus is 3.3V. Any voltage above 3.3V through the TTL channel could cause malfunction of the flight computer. TTL is not the most reliable standard for communication. It will likely be replaced by RS232 in the future.

3.4.2   RS232

RS232 is used to communicate between the flight computer and radio. RS232 is the oldest and best-known standard for communication. RS232 standard has been commonly used in computer serial ports. It performs communication between two devices at voltages higher than logic level voltages. By the RS232 standard a logic high ('1') is represented by a negative voltage – anywhere from -3 to -25V – while a logic low ('0') transmits a positive voltage that can be anywhere from +3 to +25V. The high voltage communication voltage level makes the signal less susceptible to noise, interference, and degradation[11]. This means that an RS232 signal can generally travel longer physical distances than their TTL counterparts, while still providing a reliable data transmission. RS232 also offers isolation between the master and slaves to protect them from overvoltage damage. For IlliniSat-2, the RS232 bus operates at 3.3V. The transceiver used for RS232 in IlliniSat-2 bus is Texas Instrument's MAX-232.

3.4.3 RS422

RS422 is used to communicate between the flight computer and all the payloads. RS422 is a balanced, differential serial standard that further reduces the signal noise and reliable communication distance, with the communication speed at 115200 bps. RS422 requires transceiver ICs between master and slave. ADM3488 is used throughout the spacecraft for IlliniSat-2 RS422 bus.

3.4.4 RS485

RS485 is used to communicate between the flight computer and the attitude determination and control system. RS485 is a single-master-multi-slave protocol with balanced differential serial output. It supports up to 32 slaves with a single master. In the extreme case of 6U satellite like LAICE, where there are 17 ADCS slaves on board. RS485 is the perfect fit to handle the communication. RS485 operates by toggling the DE and RE pins to determine whether the transceiver is in transmit mode or receive mode. When the DE and RE pins are both high, the transceiver is in transmit mode; when the DE and RE pins are both low, the transceiver is in receive mode. During the communication, all the devices should be in receive mode at idle state and toggle to the transmit mode if there is data to transmit. All the devices need to have their own individual address and command addresses so that no two devices will share a single command. RS485 requires transceiver ICs between master and slave. LTC2850 is used throughout the spacecraft for IlliniSat-2 RS485 bus.

Characteristics of RS232, RS422, RS423 and RS485

	RS232	RS423	RS422	RS485
Differential	no	no	yes	yes
Max number of drivers Max number of receivers	1 1	1 10	1 10	32 32
Modes of operation	half duplex full duplex	half duplex	half duplex	half duplex
Network topology	point-to-point	multidrop	multidrop	multipoint
Max distance (acc. standard)	15 m	1200 m	1200 m	1200 m
Max speed at 12 m Max speed at 1200 m	20 kbs (1 kbs)	100 kbs 1 kbs	10 Mbs 100 kbs	35 Mbs 100 kbs
Max slew rate	30 V/µs	adjustable	n/a	n/a
Receiver input resistance	3..7 kΩ	≥ 4 kΩ	≥ 4 kΩ	≥ 12 kΩ
Driver load impedance	3..7 kΩ	≥ 450 Ω	100 Ω	54 Ω
Receiver input sensitivity	±3 V	±200 mV	±200 mV	±200 mV
Receiver input range	±15 V	±12 V	±10 V	−7..12 V
Max driver output voltage	±25 V	±6 V	±6 V	−7..12 V
Min driver output voltage (with load)	±5 V	±3.6 V	±2.0 V	±1.5 V

Table 3:RS232, RS423, RS422 and RS485 Comparison[12]

3.5 Grounding Scheme

Correct grounding is important for the correct operation of a spacecraft. Correct grounding will reduce ground loops in the spacecraft. Ground loops can be troublesome because they can both radiate and receive magnetic field noise. AC magnetic field noise can couple into and disturb other circuits. DC magnetic fields can disturb onboard dc magnetometers. The key to minimizing the effects of ground loops is to minimize the enclosed area around which the current flows. Correct grounding can also reduce the chance of mission failures. NASA has reported failure cases of their spacecrafts due to high voltage rails accidentally touching the chassis and the direct grounding methods caused high current spikes in the spacecraft system, resulting in a 100% mission loss.

According to NASA-HDBK-4001 reference handbook for grounding, there are two preferred strategies when it comes to grounding a spacecraft: single point "star" ground and multiple point ground. In both cases, the ground is a reference to the chassis. Single point star

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ground ensures that there is one and only one DC ground reference path for each assembly; however, if the wires between the chassis and subsystems are too long or the frequency is too high, significant inductance can be induced through the wires. The system may no longer have a zero-potential reference with respect to chassis. Multiple point ground strategy has each circuit common grounded directly to the chassis. Multiple point ground is typical for radio frequency subsystems but shall not be used when signal is lower than 1MHz frequency[13].

IlliniSat-2's grounding scheme combines single point grounding and multiple point grounding. The radio is grounded at multiple points to the chassis to achieve multiple point grounding. The rest of the system is treated as a unit, with all the ground tied to the Power Board in a star fashion. Power Board has a single direct ground connection to chassis through one of its mount holes to achieve single point star ground. IlliniSat-2's grounding complies with NASA's standard for small/simple spacecraft in Table II[13]. A complete grounding diagram in the example of LAICE is shown in Figure 21.
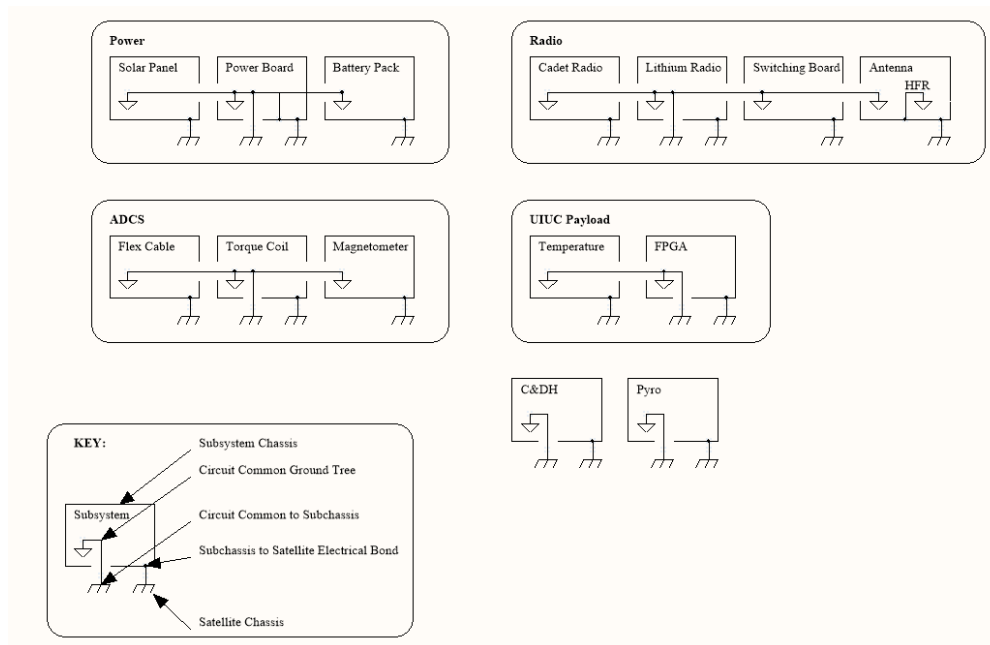
Figure 21: IlliniSat-2 Grounding Scheme

CHAPTER 4: COMMAND AND DATA HANDLING SYSTEM

4.1 Introduction

The Command and Data Handling (C&DH) system in a spacecraft is responsible for data gathering and commanding for the rest of the system. The Command and Data Handling system has several responsibilities: query the power system to gather battery health data of the satellite; query data from the Attitude Determination System to determine satellite's attitude; command the Attitude Control System to control satellite's attitude; query the Flex Cable interconnects to gather temperature data; communicate with the radios for beacon, handshake with the ground station and transfer the data; and lastly, communicate with the scientific payloads to perform science experiments and gather the results.

4.2 Requirements

1. The Command and Data Handling system shall correctly boot up the Linux kernel, and shall not have accidental re-boot during the mission operation.

2. The Command and Data Handling system shall provide a second method for booting up the Linux system when the first boot method malfunctions.

3. The Command and Data Handling system shall have an on-board backup battery system to provide power to the Real Time Clock in order to keep the timer going, even when the system is off. The backup battery shall include protection circuitry to prevent damage to the battery.

4. The Command and Data Handling system shall have 7 channels of communication. Among these 7 channels is a TTL debug interface to print out kernel messages. Another is a TTL interface between C&DH and the Power Board. There is also a RS485 interface between

C&DH and ADCS system. Lastly there is a RS422 interface between C&DH and the radio system. The remaining 3 communication interfaces can be chosen between RS232 and RS422 for the payload. Having 7 channels of communication ensures expandability of the IlliniSat-2 bus to being able to carry 3 science payloads.

5. The Command and Data Handling system shall provide at least 4GB of storage for science and housing data, and another 4GB of storage space for data backup.

6. The Command and Data Handling PCB shall have the dimension of 90 x 90mm with a maximum height of 12 mm once the daughter card is mated with the carrier board.

7. The Command and Data Handling system shall comply with the Illinisat-2 grounding scheme.

8. The Command and Data Handling system shall use DF-11 connectors as per the data interface design between subsystems and payloads.

9. The Command and Data Handling system shall use backbone connector to interface with the power board.

4.3   C&DH Revision History

The first generation of C&DH was designed for ION-1 satellite. The system was an off the shelf Small Intelligent Datalogger (SID) system developed by Tether Application. The SID system is radiation hardened for LEO operation with latch-up protection circuitry, watchdog timer, thermal and EMI repression.

After University of Illinois acquired funding for IlliiSat-2 bus through LAICE and CubeSail satellite projects, it was determined that we should start making our own C&DH circuitry for cheaper manufacture pricing and better customer support. The second generation of C&DH is designed based around embedded Linux operating system. Compared with Eclipse based

embedded microcontroller software development environment, embedded Linux offers more complete device driver support, a wide variety of toolchains, packages and libraries to ease the process of development. The first attempt to design the C&DH was around a Texas Instrument OMAP microprocessor. The C&DH has a 400MHz processor, 64MB of 166MHz SRAM, 2 32MB of external SPI Flash, and 4 UART output ports for communication with the rest of the system. The design for the C&DH circuit was offloaded to an independent contractor, the circuit was designed, underwent the final design review and final mass production of 10 units. However, because of a lack prototyping and looseness of the design review, the final C&DH units have the RAM's connection flipped and mirrored, causing un-fixable failure of the second revision of C&DH. The lesson learned from the costing experience was that prototyping a circuit before mass production is necessary to catch all potential design production errors.

After the failure of designing our own in-house C&DH board, the upper management realized how expensive it is to prototype and manufacture a Linux system and how easy it is for a designer to make a mistake on a complex high-layer count Linux PCB. The focus was shifted to avoid designing a Linux computer. Instead, the designer should choose an already-existing professionally-designed-and-tested off-the-shelf Linux daughter module, and design a carrier PCB around the daughter module to extend the functionalities to fit the needs of the IlliniSat-2 system. Through researching on different websites and comparing different Linux modules, Critical Link's MitySOM-335x system on module card was chosen as the daughter cad for C&DH. MitySOM-335x is based on Texas Instrument's OMAP2 series AM3358 microprocessor. AM3358 is the series of processor used in the well-known BeagleBone series of hobbyist Linux modules, which has a good amount of design and debugging support around the internet. The system-on-module also has well-supported documentations on carrier board design and custom Linux Kernel

modifications, which ease the engineer's design process. The third generation of C&DH's design work was carried out by Fall 2014 ECE senior design team. The carrier board offers power-sequencing for the daughter card, two 4GB NAND storage expansion and 6 UART expansions for communication with the C&DH. The third revision booted up the SOM daughter card. The students claimed to have verified the UART communications through loop testing, but it was later found that their test code was buggy and couldn't verify the UART communication. SPI to UART expansion was also tested to be non-functioning. Upon further testing, the NAND flash along with the NAND flash controller also couldn't be recognized by Linux Kernel. Revision 3.1 was later designed by ECE student ZheJi to address all the issues, and the effort did not result in a fully functioning C&DH.

Due to the failure of NAND flash and SPI-to-UART controller, the decision was made to shy away from externally controlled NAND flash and to use ICs close to SD card that is NAND but with internal management circuitry instead. SD cards are not suitable for space due to the shell and holder material outgassing. Through research, embedded Multimedia Card, eMMC was found to be the alternative option to an SD card. Revision four was designed to replace the NAND with eMMC and SPI-to-UART with USB-to-UART. Revision 4 was a success after kernel modifications. It was used for CubeSail satellite. A more updated Revision 4.1 was later produced to address mechanical fitting error, as well as high-speed signal integrity issues. Revision 4.1 was used for LAICE, SpaceICE, CAPSat and SASA missions. Revision 4 design is what will be discussed in the next sections. The PCB layout for C&DH Revision 2 to Revision 4 are attached in Appendix B.

4.4 C&DH Hardware Function Overview
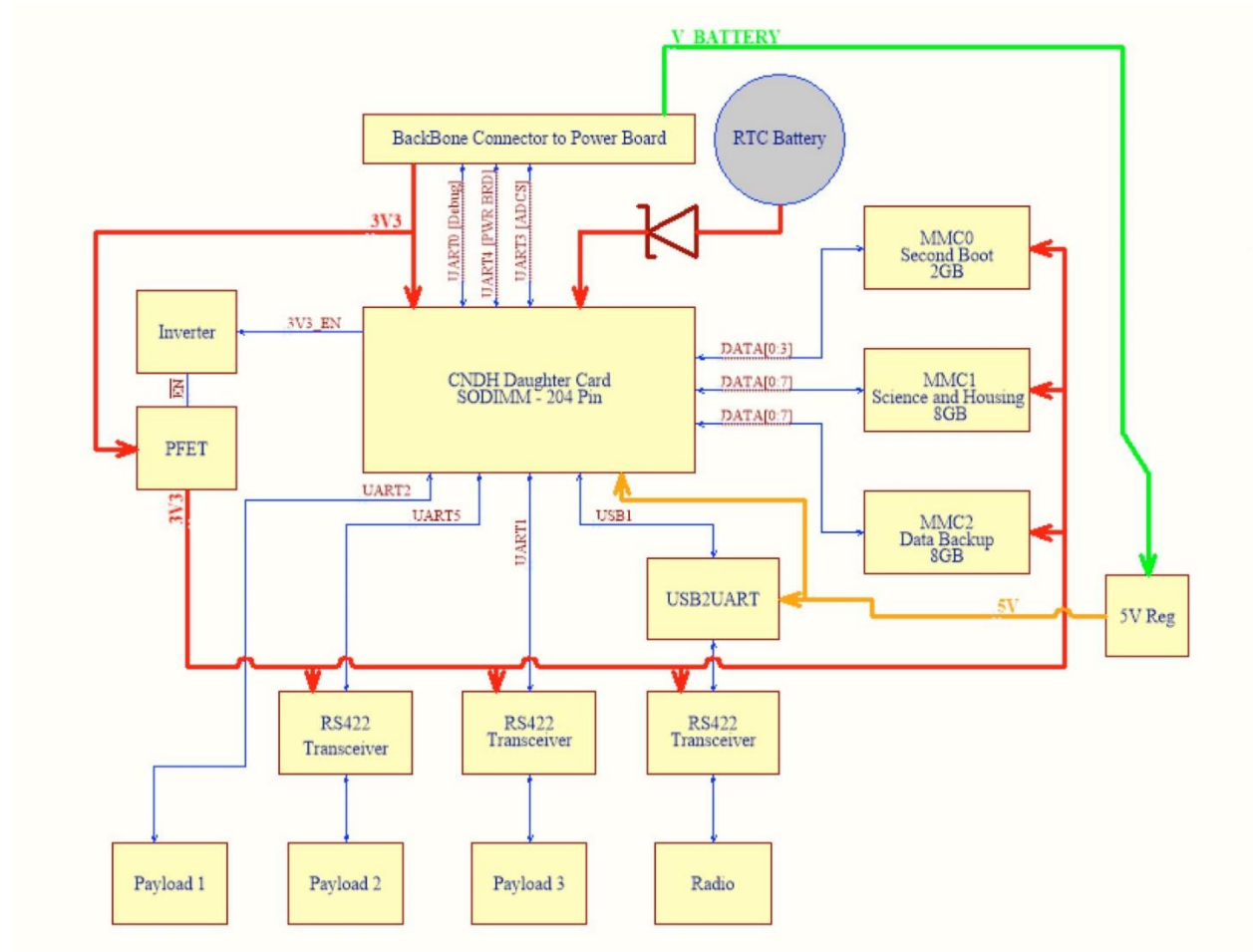
Figure 22: C&DH Block Diagram

The Command and Data Handling system consists of system-on-module daughter card with the core embedded Linux circuitry; a boot-sequencing circuitry to correctly power sequence the daughter card with rest of the peripherals; 3 eMMCs to add in secondary boot, science and housing data collection and data backup; USB to UART driver to add an extra UART line, bringing to a total of 6 UART communication line for communication with the rest of the satellite; and an external coin cell battery to supply power to keep the timer alive. Figure 22 shows a complete

block diagram of the C&DH system. The C&DH circuit fits in a 90 x 90 mm PCB with 7.7mm height once the daughter card is plugged into the spacecraft which complies with requirement six.

C&DH PCB carries four DF-11 connectors that are used to communicate with one radio and three payloads. The PCB also contains a backbone connector. The backbone connector mates with the power board to receive power and distribute commands to power board, ADCS and debug console. This setup is shown in Figure 23 meets requirement eight.

To satisfy requirement nine in terms of grounding, the C&DH PCB offers direct connection to the Power Board's ground through the middle pin of the backbone connector. A 3MOhm resistor is connected between chassis and C&DH's ground for the four mounting holes of CNDH. The grounding scheme is shown in Figure 23.
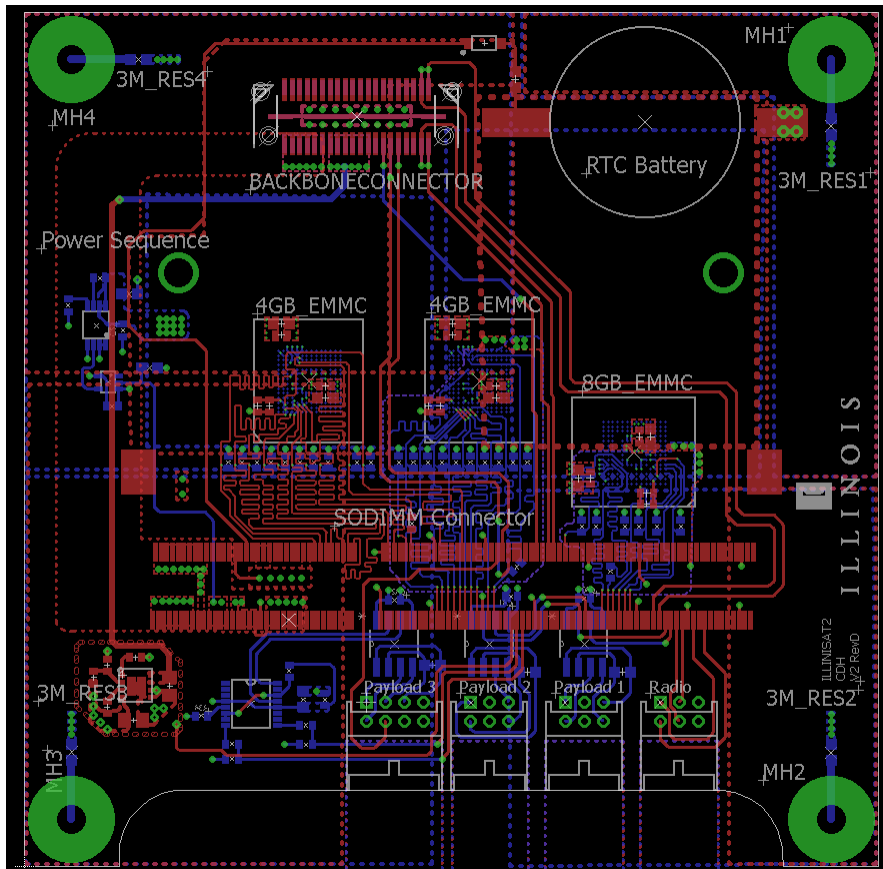
Figure 23: C&DH PCB Design

4.5   Hardware Description

4.5.1   System-on-Module Daughter Card

Figure 24: MitySOM-335x Card

The System-on-Module card is the core of the C&DH system. The SOM is a board-level circuit that integrates a full embedded Linux circuitry. The SOM was designed on a 38.1 x 67.6mm PCB with the shape of a DDR3 RAM module. Through a 204-pin SODIMM connector, the SOM is mated with the carrier board for system booting, peripheral expansion and kernel debugging. Due to the cost and complexity of designing and fully testing a high-speed embedded system, off-the-shelf MitySOM-335x series SOM cards from Critical Link were chosen as the flight daughter card. A picture of the daughter card is shown in Figure 24. MitySOM-335x is based on 1GHz 32-bit Texas Instrument AM335x family of embedded Linux Microprocessor, with 1GB of DDR3 RAM and 512MB of NAND storage. MitySOM-335x SOM card offers expansions of 6 channels of UARTs, 2 USBs and 3 MMC/SD/SDIO storage expansion channels[14]. The Linux kernel can be debugged through UART0 line, where all the boot message can be printed out to an external Linux system running Minicom or Screen.

4.5.2   Carrier Board

The MitySom-335x SOM Card requires a carrier board to supply power and expand the peripherals per design needs. The carrier board designed includes a boot-up sequence to correctly provide power to the SOM card and boot-option select to provide two boot methods. The carrier board carries a coin cell battery as a backup supply to the Real Time Clock (RTC). The carrier board includes a 8GB embedded multi-media card (eMMC) to hole secondary Linux Image file and two 4GB eMMCs for science data storage with redundancy. Lastly, the carrier provides seven channels of communications to the rest of the subsystems. A 204-pin SODIMM connector is used to provide electrical connections between the SOM card and the carrier board and is shown in Figure 23.

4.5.2.1 Boot-up Sequence

Based on AM335x's datasheet, it is recommended that the Linux Computer be powered-up first before powering the rest of the peripheral circuitry[15]. The Linux core voltage line is a big inductive circuit that usually consumes a lot of current, which can cause ripples on the power supply line when it is being powered up. By waiting for the core to power up first, then power up the rest of the circuit, we can get cleaner power line during the boot up and avoid potential resonation of the loads. There are two power sequencings on the C&DH board, SOM Power Management Integrated Circuit (PMIC) power sequencing and carrier board power sequencing. The SOM PMIC sequencing is implemented on the SOM. The PMIC sequences the power supplies for the Linux to boot up the processor. The last powerlines in the SOM powering sequence will be 3.3V out. Once the power sequencing is complete on the SOM side, the carrier board will get the indication from the 3.3V output that the AM335x is correctly powered, then the carrier board will power on the rest of the peripherals.
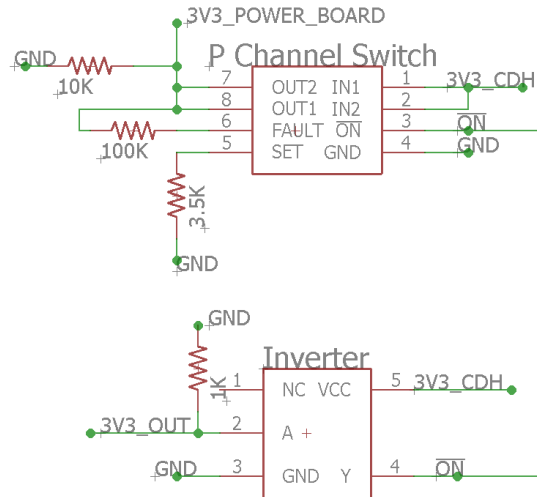
Figure 25: C&DH Carrier Board Boot-up Sequencer Circuit

The boot-up sequence circuit on the carrier board consists of a P-Channel Switch and an inverter and is shown in Figure 25. The inverter is needed because the P-Channel switch is low enable. When the 3V3_OUT from the SOM is at 3.3V indicating that the Linux core is correctly booted up, the inverter will output 0V, which enables the P-channel switch and turns on rest of the circuit on the carrier board. MAX892L P-Channel Switch[16] is chosen for its low on-resistance and thermal shutdown to prevent overcurrent situation. The correct boot sequence result is attached in Figure 26. The design of boot sequence partially satisfies requirement one.
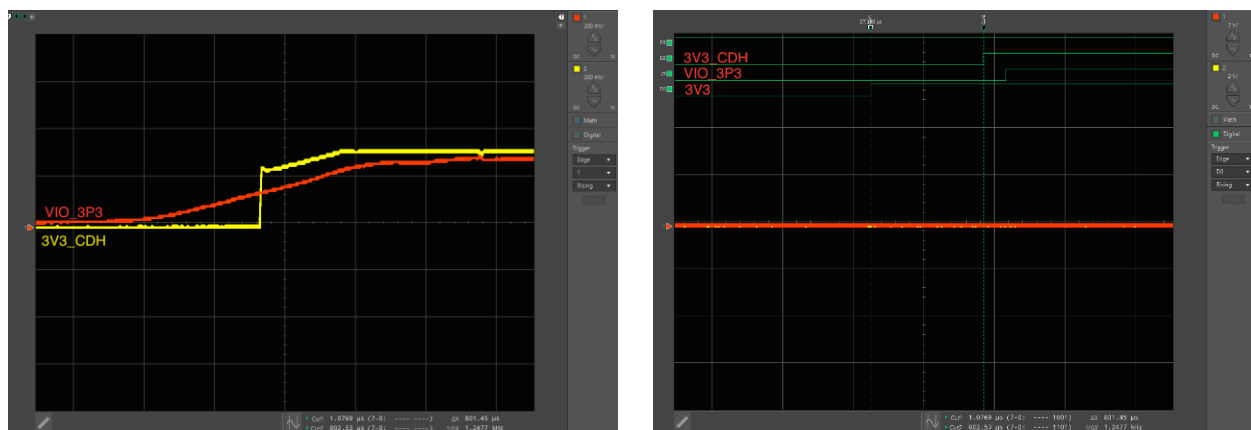
Figure 26: C&DH Boot-up Sequence

4.5.2.2 Boot Option

Linux is capable of booting from different peripherals of different storage devices, namely: NAND, SPI, USB, UART, SD and Ethernet[17]. The sysboot (mapped to LCD_DATA) pins [15:0] configure the boot order by being pulled to logic high or low with 10K Ohm resistor.

To meet the requirement of having two ways of booting the C&DH as a fail-safe measure towards radiation damage, The IlliniSat-2 C&DH's LCD_DATA [11:0] is configured to
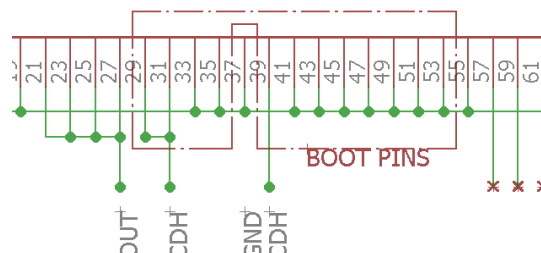
Figure 27: C&DH Boot Option Configuration

Boot Config LCD_DATA[11:0]: 0000000 10011⁺

0x000000010011 to have a boot sequence of NAND->NANDI2C->MMC0->UART0, shown in Figure 27. Out of the four boot methods, only the NAND and MMC0 boot methods are implemented. As a result, during the boot process, C&DH will look for boot files in NAND first. If NAND boot fails, C&DH will look for boot files in MMC0. The boot order is also implemented in the uboot's uenvironment.txt file. The design for the boot option satisfies requirement two.

4.5.2.3 RTC Battery

Correct timing is important for a spacecraft, especially when the central computer is Linux-based. For IlliniSat-2, Linux scheduler daemon was timing based. If the time of the satellite is incorrect, the scheduled tasks will be run at the wrong time. For example, when running the attitude determination and Control System at incorrect kernel time, the satellite might issue a re-orientation at the wrong time, causing the satellite to rotate when it is not desired. When running the

communication system at the wrong time, passes through the ground station will be scheduled at the wrong time. The C&DH system's power is controlled by the Power Board. In the case that the power is cut out of C&DH from the Power Board, the SOM module will not be getting power and the Real Time Clock timer will be reset to the default value. To prevent the clock from being reset and satisfies requirement three, C&DH carrier board includes a non-rechargeable Lithium Ion coin cell battery feeding into the VBACKUP pin to keep the timer IC alive even when the power is cut off. The protection circuit for the RTC battery is a diode in forward-biased configuration to avoid reverse current going into the battery, and a 4.7K Ohm resistor in series to limit the current.

Based on the datasheet of MitySOM-335x, when the PMIC RTC is active, it consumes 10.2uA. By the recommendation of MitySOM-335x's design guide, the RTC battery chosen is Panasonic BR1225 coin cell battery with 48mAh capacity. By calculation, the RTC battery can operate for 4706 hours, the equivalent of 196 days. The 196 days of RTC operation time will account for the off time of the satellite from delivery to launch; for certain missions, from delivery to International Space Station to deployment; as well as low power stage C&DH is shutdown during satellite operation.

It is recommended to replace the coin cell battery during final assembly so that the spacecraft will be delivered to the launcher with the battery in a full state of charge.

4.5.2.4 EMMC

EMMC is a NAND based memory storage device. Unlike NAND memory, which needs hardware or software controller for ease of read/write/formatting/mounting, bit-flip and bad block handling[18]. EMMC memory has internal controller circuit integrated with the NAND memory cells to offer reliable storage expansion for the daughter card. The eMMCs chosen for C&DH carrier board is Micron MTFC series[19]. The MTFC series has low standby current at 100uA,

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which offers defect and error management and data-loss through power-loss prevention, making the chip ideal for satellite operation.

The C&DH carrier board carries 3 eMMC ICs. For C&DH REV C, eMMC0 has 2GB of storage that will solely be used as a second boot method, eMMC1 has 8GB of storage for science and house-keeping data, eMMC2 has 8GB of storage and is used as a backup for the science and house-keeping data. For C&DH REV D, due to a lack of available eMMC IC, the eMMC0 slot is assembled with 8GB EMMC. The eMMC1 and eMMC2 are assembled with 4GB EMMC. The eMMC0 will have 2GB of boot space, 3GB of science plus house-keeping data space and 3GB of backup space. eMMC1 will storage 4 GB of science and house-keeping data, eMMC2 will be the backup storage. This design satisfies requirement five.

EMMCs were chosen as the storage expansion because they are closely related to the architecture of SD cards. They are relatively easy to implement since there is no need for an additional NAND controller. To implement a NAND based system, the designer needs to route the 16 data pins, 8 command pins, 6 indication pins as well as the corresponding NAND controller's data and command pins. To implement an eMMC based system, all the designer needs to route are the data, command and clock line. However, there are downsides of using eMMCs: the manufacturability of the PCB. The Ball Pitch between each eMMC Ball pins is 0.5mm. The diameter of each ball pad is 0.3mm, which leaves 0.2mm space for routing traces and 0.4mm space for routing vias. The standard PCB manufacturing capability is 6mil trace width, 6mil clearance between copper, 12mil via hole size and 12mil via plating. For the eMMC section of the C&DH design, trace width is 6mil, via hole size is 5mil with 5mil of plating, and the clearance is 3mil. The small via size, the small trace size and clearance, together, brought signal integrity issues on the eMMC data trace, as well as increased manufacturing cost.

4.5.2.5 Data Communication

Channel	Protocol	Functionality
UART0	TTY	Debug
UART1	RS422	Communication to Payload 1
UART2	RS232	Communication to Radio
UART3	RS485	Communication to ADCS
UART4	TTY	Communication to Power Board
UART5	RS422	Communication to Payload 2
USB0	RS422	Communication to Payload 3

Table 4: C&DH UART Channel Assignment

The requirement states that the C&DH needs 6 UART channels to communicate with rest of the subsystems on the satellite. MitySOM335x supports 6 independent UART and 2 USB communication channels, with the UART0 being the debug port to print out kernel messages. The final design of the communication channels is shown in Table 4, with all 6 UARTs and 1 USB port used. UART0 goes through Power Board into the debug header for kernel debugging. UART1 and UART5 goes through RS422 transceivers for payload RS422 communication. UART2 is RS232 communication for the radio. UART3 is RS485 bus for the single-master-multi-slave bus of ADCS. UART4 is TTY communication between C&DH and Power Board's MSP430. USB0 goes through a USB to UART converter, then RS422 transceiver for payload communication. The USB to UART expansion requires the corresponding USB1_VBUS pin on the SOM which needs to be powered up with a 5V. As a result, a buck regulator was added to convert the battery voltage to 5V to power up the USB1 line. This design satisfies the requirement five for the subsystem and payload communication interfaces.

4.6   Kernel Driver Modification

During the testing of the C&DH PCB, several modifications were implemented in the Linux kernel to add in support for the carrier board and enable desire peripherals:

1. To satisfy requirement one, the Linux kernel is upgraded from 3.1 to 3.2 for 512MB+ NAND support. The Linux kernel version 3.1 only supports up to 256MB of NAND for UBI filesystem. When the NAND size is bigger than 256MB, kernel 3.1 will fail to detect the NAND and choose the correct partition table. The issue is addressed in kernel version 3.2.

2. To satisfy requirement one, the baseboard-mityarm335x-laice.c and mux33xx.c for C&DH is modified. The mux33xx.c file is a pin-mux file for C&DH that lists the functionalities of each BGA pin. In the baseboard file, the designer will choose the functionality of each pin based on the carrier board design. In the baseboard file, two extra MMC pin-mux selections were added along with initialization, several UART pin-mux were added, and the LCD display was disabled to lower the current draw. The files can be found in /arch/arm/mach-Omap2/.

3. To satisfy requirement four, the FT230x USB to UART driver support was added to the Linux kernel. Linux 3.2 kernel does not support FT230x series USB to UART transceiver, which results in the kernel not recognizing the FT230 transceiver. The driver was manually implemented in ftdi_sio.c and ftdi_sio_ids.h in /drivers/usb/serial/, and enabled in menuconfig.

4. To satisfy requirement four, RS485 driver was further modified to include delay timing. During the ADCS software testing, it was noted that the RS485 bus's enable line was toggled right after the command was sent, which caused the RS485 communication

line to be locked up. Changing the rts_delay_before and rts_delay_after variable in the RS485 ioctl struct during initialization had zero effect on the enable line delay time. Upon further investigation, we noticed that the RS485 enabled a delay that was never implemented in MitySOM Linux 3.2 kernel. The delay implementation was then added to /drivers/tty/serial/omap-serial.c.

5. The eMMCs on the carrier board has signal integrity issue from impedance mismatching. To address the signal integrity issue and satisfy requirement five, the communication clock speed is lowered in /drivers/mmc/core/mmc.c from 50MHz to 20MHz. For C&DH Rev D, the eMMCs are of higher revision, which didn't fall through the Linux revision check. The revision check in mmc.c is also by-passed to allow the newer eMMCs to be recognized.

4.7   C&DH Boot Log

The Appendix A showed a complete boot log of the CNDH mother board. The boot log demonstrates that the CNDH is capable of correctly loading its 3.2 Linux Kernel from the 512MB NAND Flash which meets the first requirement of successful booting. The boot log also demonstrates the correction creation of UART0 to UART6 channels and USB1 channel, partially fulfilling the fourth requirement about providing sufficient communication channels. Finally, the boot log showed the detection and creation of the 3 eMMC devices with the correct version number and storage size, fulfilling requirement five.

4.8   Remaining Issues and Suggestion for Next Revision

There are certain remaining issues with the current C&DH Carrier Board PCB design. The issues are listed below and multiple recommendations are made to improve the C&DH carrier board design for the next revision.

The first issue is the signal integrity issue with the eMMC high speed traces. The eMMC data, command and clock traces can potentially run at 50MHz speed. In Rev C, impedance mismatch, trace length mismatch, and close trace coupling caused signal integrity issues which limited reliable communication speed to 10MHz. Rev D re-organized the eMMC traces to avoid close trace coupling and trace length mismatch, yet the eMMCs still cannot reliably operate at 50MHz maximum communication speed. In both revisions, the communication errors occur at MMC0. For the future revision, it is beneficial to look into a way to route the eMMCs through unused pin instead of fanning out the pins through tiny vias which are prone to signal coupling. If possible, the future designer should look into space-safe SD card holder and SD card with low outgassing property, conformal coat and epoxy the SD card slots to prevent the SD card from ejecting during vibration.

The second issue is the daughter card malfunctions and burns out when testing the fully-integrated satellite. During service stack subsystem modular testing using the standard Power Board, C&DH and EGSE setup, damage to the daughter card was never observed. The SOM could always boot up and print out messages through the debug UART channel. However, throughout the final integration of LAICE CubeSat and CubeSail CubeSat, the daughter card was permanently damaged 4 times. All 4 times were under correct testing setup. The tester removed the Remove-Before-Flight tag to boot up C&DH, the Linux processor got hot, beeped and refused to show any boot message. The damages were permanent and the only course of action was to replace the daughter card. Upon investigation, the root cause was found to be that the design guideline were not followed correctly. It is specified in the design guide that all external peripherals should be powered up after the Linux core is powered up, hence the boot sequence described in the previous section[26]. The UART0 debug line has an USB to UART module for communication with the
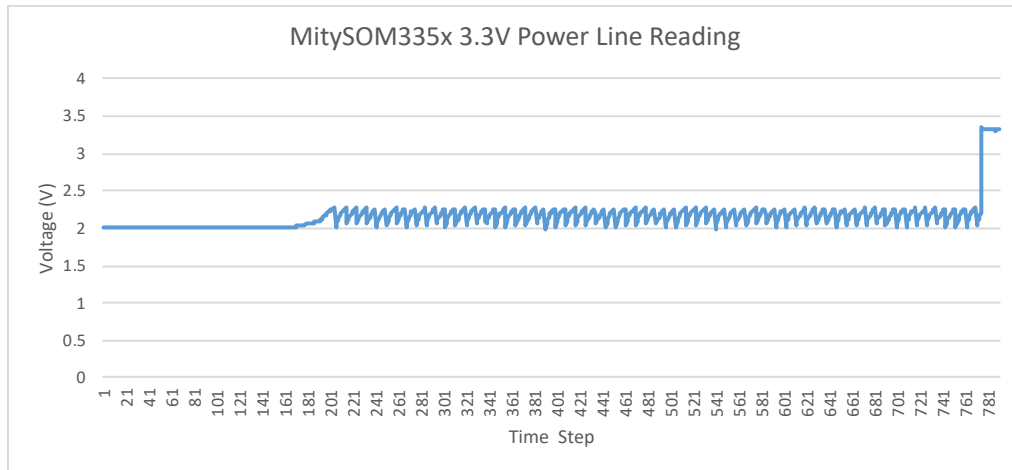
Figure 28: C&DH 3V3 Line Voltage Measurement

host Linux computer. Ideally, when the C&DH is powered down, all the pins going into the C&DH should be pull to GND level. But in this case, a powered-up idle UART line will have its RX and TX lines raised high. As a result, the C&DH will have two 3.3V signals going into its GPIO pins when it is not powered off. Those GPIO pins are non-fail-safe pins that can only receive signals from -0.3V ~ 0.5V when the power is off. Measurements were taken on the 3V3 power line when the C&DH is off and UART0 on. A noisy signal in the power line with lots of ripples was observed, shown in Figure 28. It is believed that the ripple could potentially cause resonation on the SOM card and cause irreversible damage. The current solution to the problem was to use RS232 transceivers in the UART0 line, and only have the RS232 be powered up when the power sequencing indicates that the SOM is powered up. The fix involves soldering a 3V3 line from the output of the power sequencing P-FET to the backbone connector, then guide that 3V3 line to the debug header on the Power Board into EGSE's RS232 line. For the future revision, the RS232 circuit should be added on to the carrier board with correct power sequencing.

The third issue is a lack of method to debug C&DH user software. To be able to use gdbserver to debug C&DH software, one extra communication line is needed. The current C&DH

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carrier board design does not have extra UART line for debugging. It is recommended that the next revision should incorporated another USB to UART converter on the USB0 line for the sake of debugging.

The next issue is the slow software uploading speed. The C&DH software are uploaded through UART0 debug line which has the upload speed to 115200bit-per-second. The uploading is a slow process and a normal 4MB software takes around 5 mins to upload. For the future revision, it is advised to enabled ethernet support on the carrier board so that the programmers can upload the code through ethernet which are much faster.

The last issue is the RTC battery life time. Currently the RTC battery can only support 196 days of backup power. If a CubeSat were to sit on the bench for longer than 196 days, the RTC battery will have to be replaced before flight. A rechargeable coin cell battery with charging circuitry should be implemented for the next generation of C&DH. The coin cell battery should be able to be recharged off the main battery, thus providing longer satellite shelf life.

4.9 Summary of Contributions

The C&DH design fulfilled all the requirements. The carrier board is able to successfully boot the daughter card with Linux 3.2 Kernel. All the required UART and USB channels are recognized and created. All three eMMCs are correctly detected and communicated, providing a method of second boot through eMMC0. An RTC battery is chosen to supply power to Linux Clock Driver when the main power is turned off as a method to keep the correct timing. Lastly, the C&DH design fit the mechanical requirement. It is able to mate with the power board through the backbone connector and fit inside the satellite service stack, as shown in service stack picture in Figure 1.

CHAPTER 5: POWER GENERATION AND DISTRIBUTION SYSTEM

5.1   Introduction

The Power Generation and Distribution System, is responsible for the generation, storage, distribution and monitoring of electrical power. The IlliniSat-2 Power System generates electrical power by converting sunlight into electrical current through solar panels. By using technology called Maximum Power Point Tracking (MPPT), the system can regulate the raw solar electrical power to a level suitable for the satellite's electrical system. The excess electrical power will be stored in a battery pack consisted of four 18650 Lithium Ion batteries. The raw battery power will be further regulated and then distributed through Hot-Swap switches controlled by a central microcontroller MSP430. The overview of the power system is shown in Figure 29. In this chapter, the power system is broken into 3 subsystems: Solar Panel subsystem for power generation, Battery Pack subsystem for power storage, and Power Board subsystem for power regulation, distribution and monitoring.
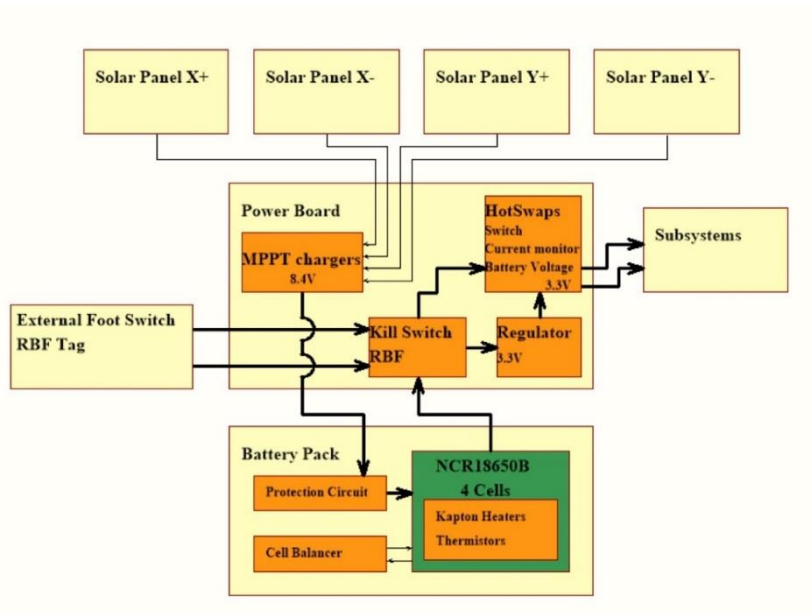
Figure 29: IlliniSat-2 power System Overview

5.2   Requirements

1. The Power Generation and Distribution system shall generate enough power from the solar panel to operate the payloads during the mission operation time.

2. The Power Generation and Distribution system shall be able to charge the batteries with different length of solar array from size 1.5U to 6U.

3. The Power Generation and Distribution system shall comply with Nanoracks' NR-SRD-139 document regarding battery safety[22].

4. The Power Generation and Distribution system shall disconnect power from the satellite upon the insertion into a Remove Before Flight (RBF) connector or pressing of the switches on the bottom of the satellite.

5. The Power Generation and Distribution system shall initiate a 50min countdown upon the release of foot switches.

6. The Power Generation and Distribution system shall communicate with C&DH.

7. The Power Generation and Distribution system shall monitor the batteries' state of charge and enter satellite into corresponding power state.

8. The Power Generation and Distribution system shall distribute power through battery and 3.3V lines.

9. The Power Generation and Distribution system shall have control over the distribution of power to the rest of the subsystems.

10. The Power Generation and Distribution system shall comply with the Illinisat-2 grounding scheme.

11. The Power Generation and Distribution system shall use DF-11 connectors as per the power and data interface design.

5.3 Power Generation – Solar Panel

5.3.1 Introduction

IlliniSat-2 bus generates power through the use of solar cells. Solar cells were chosen because of their relatively small size, easy assembly, relatively high efficiency and long operation life time. The Solar cells are assembled in series to form a higher voltage solar cell chain; the solar cell chain is attached to one side of the aluminum radiation shield to form the solar panel.

5.3.2 Requirements

1. The Power Generation system shall generate enough power to operate the payloads during the mission operation time.

2. The Power Generation system shall adapt to different lengths of solar array from size 1.5U to 6U.

3. The Power Generation system shall protect the solar panels from reverse-current situation.

4. The Solar Panel shall still be functioning even with the presence of a broken cell.

5.3.3 Design

Configuration	Avg Bus Power Generated (W)(W)	Avg Bus Power Required (W) (W)	Avg Payload Power Allowed (W) (W)
1.5U	2.85	1.5	1.35
2U	3.8	2	1.8
3U	6.65	2	4.65
6U	9.3	2.5	6.8

Table 5: Average Power Generation and Allowed Consumption Based on Spacecraft Size

Depending on the size of the spacecraft, the solar cell count for each will change. Table 5 includes the averaged power generation of the solar panel depending on the size of the satellite. Table 5 is the verification of the first requirement.

The IlliniSat-2 bus supports solar panels on four sides of its wall, up to six panels in total. The 6U CubeSat has two panels on the wide side of the long walls, bringing the total panel count to six. The 6U CubeSat is longer than a 3U CubeSat, allowing extra solar cell to be attached. Unless the payload specifically requires one side of the wall to not have solar panels on, all four long walls should have solar panel covered. The cells on each wall are configured in a serial to increase the overall output voltage. Usually, the +Y solar panel will have one less solar cell to accommodate for the Debug and RBF port from the Power Board. Table 6 shows averaged panel number and cell count for each spacecraft's configuration, satisfying the second requirement.

Configuration	Solar Cell Count on one side	Number of Solar Panels	Estimated total number of cells
1.5U	3	4	11
2U	4	4	15
3U	7	4	27
6U	8	6	47

Table 6: Average Solar Cell Configuration Based on Spacecraft Size

For an individual solar cell, a corresponding IV curve is generated to analyze the cell's functionality and efficiency. To generate an IV curve in a lab environment, a solar simulator was used. The solar simulator consists of two sub-components, a sun light generation unit and a data collection unit. The sunlight generation unit warms up a cold started lamp and generates light with intensity corresponding linearly to that of the sun. The data collection unit behaves like a programmable digital load operating in constant current mode, an IV curve software sweeps through the current and measures the output voltage. The result of one solar cell's IV curve is shown in Figure 30. The peak point of the red curve indicates the peak point operation of the solar cell.
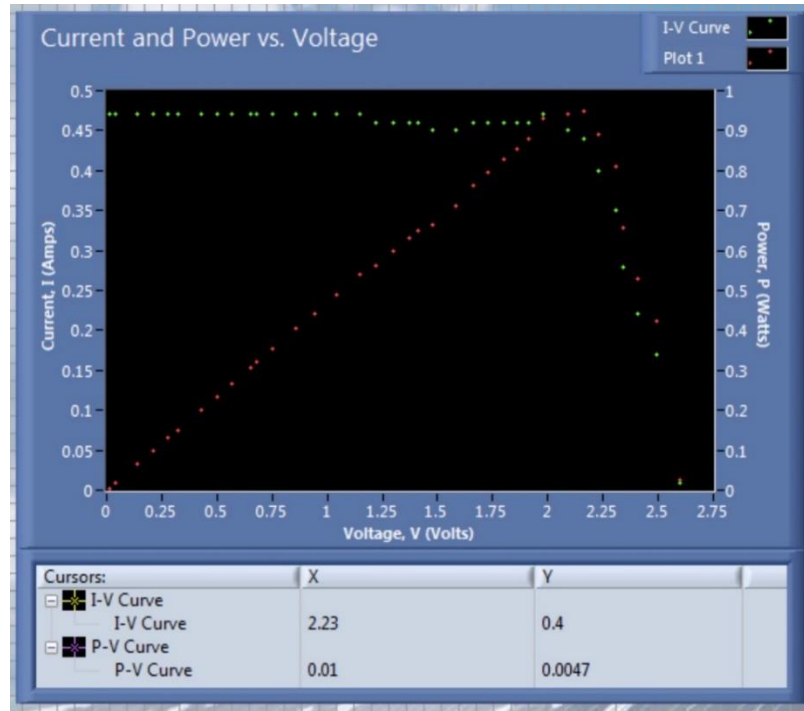
Figure 30: Solar Cell IV Curve

The spacecraft grade triple junction GaAs solar cells used usually have around 28~30 percent efficiency[20]. The discrepancy of the efficiency is due to slight differences in the manufacturing process. To select the solar cells for each panel, estimate which wall will collect the most amount of sunlight and put the solar cells of the highest efficiencies on that side.

For each solar cell, there is a bypass diode connected in reverse biased fashion between the positive and negative output terminal shown in

Figure 31. The bypass diodes allow the series of connected cells to continue supplying power at a reduced voltage rather than no power at all. Having a bypass diode also prevents one broken solar cell from disconnecting the rest of the solar cell chain[21].

A blocking diode is also incorporated on the positive terminal of each solar panel. The block diode prevents the current from flowing back into the solar arrays. The diode configuration of the solar panels satisfies requirements three and four.
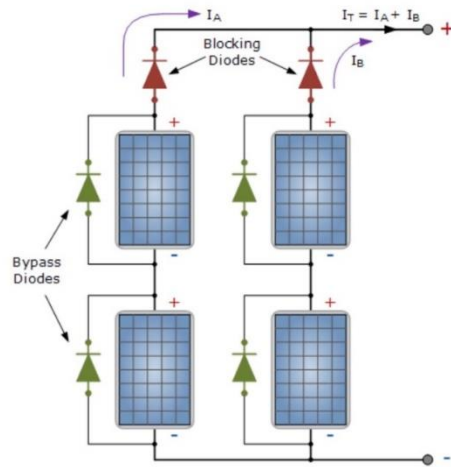
Figure 31: Solar Panel Diode Configuration

After the construction of the solar panel, the solar cell chain will be recharacterized under the solar simulator. The load used to generate the IV curve can only operate when the input voltage from the solar panel is below 10V, due to a limitation of the solar simulator and associated test equipment as it was acquired from the manufacturer. A 6-cell, 14V solar panel will not operate correctly under the IV curve load. As a result, a dedicated programmable load LD400i and custom IV curve LabView software is used when the panel voltage is above 10V. The IV curve of a solar cell chain is shown in Figure 32.
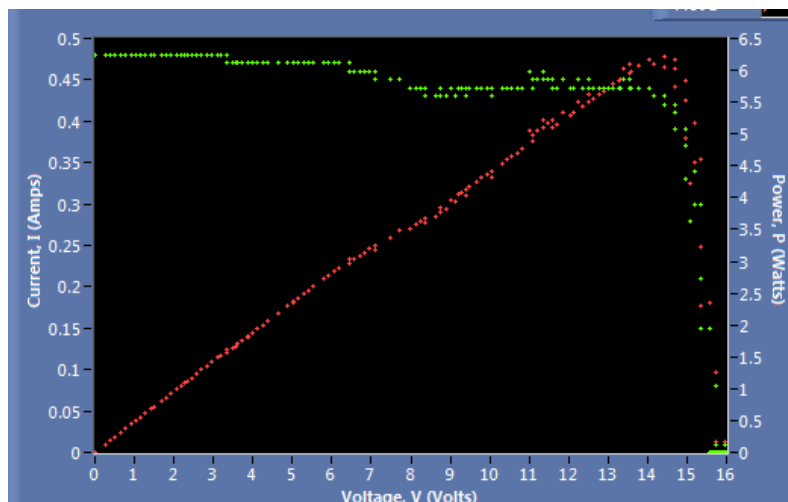
Figure 32: Solar Cell Chain Characterization

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5.4   Power Storage - Battery Pack

5.4.1   Introduction

For illiniSat-2 bus, Lithium-Ion 18650 rechargeable battery cells are used to store the energy generated by the solar panels, as well as supplying power to the rest of the system when the satellite is not receiving sunlight. The battery pack contains two sub battery packs in parallel with each sub pack made up of two cells in series, for a total of four cells. The configuration brings the nominal battery voltage to 7.4V, and nominal battery capacity to 6400mAh[1]. The battery pack contains battery protection ICs to prevent the over-voltage, under-voltage, and over-current scenario; voltage and current measurement to estimate battery state of charge; Kapton heater and NTC thermistor for battery temperature regulation; and a cell balancer to prolong battery's operation time. The battery pack went through six iterations of design, with Rev F passing NanoRacks' NR-SRD-139 Flight Acceptance Test Requirements[22] for Li-ion Cells and Battery Packs.

5.4.2   Requirements

1. All battery pack subsystems shall function at any battery pack voltage in the range of 5V to 8.4V.

2. The battery pack shall ensure that no individual battery cell be charged higher than a voltage of 4.25 V (or maximum charge voltage as specified by specific battery vendor)

3. The battery pack shall ensure that no individual battery cell be discharged below a voltage of 2.75 V (or minimum discharge voltage as specified by vendor)

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[1] This number varies based on the quality of cell purchased, age of the cell, and practical manufacturing quality of the cells

4. The battery pack shall cut off the flow of current through the batteries in the event of a short circuit.

5. The battery pack shall be operating within the temperature range of 10C to 50C.

6. The battery pack shall survive vibrational testing when assembled. The vibration intensity is specified in Nanoracks' NR-SRD-139 document[22].

7. The battery pack shall be capable of operating in vacuum.

8. The battery pack shall be capable of balancing all battery cell voltages within 10 mV of each other.

9. The battery pack shall make battery voltage and load/charge current data readily available to the Power Board.

10. The battery pack shall make battery temperature data readily available to the Power Board.

11. The battery pack shall be capable of heating the batteries at a rate between 0.5W and 1.5W per battery cell.

12. The battery pack shall have the dimension 84 x 86mm with maximum height 21mm when assembled.

13. The battery pack shall comply with the Illinisat-2 grounding scheme.

14. The battery pack shall use DF-11 connectors as per the power and data interface design.

5.4.3 Revision History

Revision A to Revision D of the battery pack was designed by Carl Haken between fall 2013 and summer 2015[23]. All four revisions were tentative approaches towards achieving a functioning cell protection and balancing circuitry. Revision D was deemed the flight version battery pack for LAICE and CubeSail missions. However, during the certification of the battery pack for the launcher NanoRacks performed as part of this work, several electrical errors were

noted. Firstly, the battery protection IC does not cut off the batteries from the satellite power system when the batteries are under-discharged. Secondly, due to the enable voltage being lower than the IC threshold, the cell balancer can only be balance in one direction. And lastly, the cell balancer is at extremely low efficiency with almost all the energy lost as heat through the inductor. Due to time constraint on mission delivery of CubeSail, Revision D was flown with Power Board-controlled battery under-voltage cutoff, and cell-balancer disabled.

Revision E was designed by Dillon Vadgama in spring 2018 for the 3 USIP missions. Revision E was an attempt to fix all the remaining issues on the battery pack. Revision E replaced the single-cell protection IC with dual-cell protection IC, the dual low-side MOSFET drivers with a high-side low-side MOSFET driver, and Revision E also added a bi-directional current sensor. However, the cell balancer still overheats, the battery still won't get cut off when the cells were at under-discharged condition.

Revision F was designed as one of the concluding stages of this work during the summer of 2018 as an attempt to address all previous design flaws. the battery pack's cell balancing system is completely revamped. By using bleeding-based cell balancing, as well as different grounding scheme referencing battery minus instead of satellite ground, the remaining issues with the battery pack have all been fixed. Revision F has been installed on SpaceICE, SASSI^2 and CAPSat missions. Due to how long the original Rev D batteries have sat within LAICE, it will be retrofit with a Revision F prior to delivery for launch. The PCB layout for Battery Pack Revision A to Revision F are attached in Appendix B.

5.4.4 Hardware Function Overview
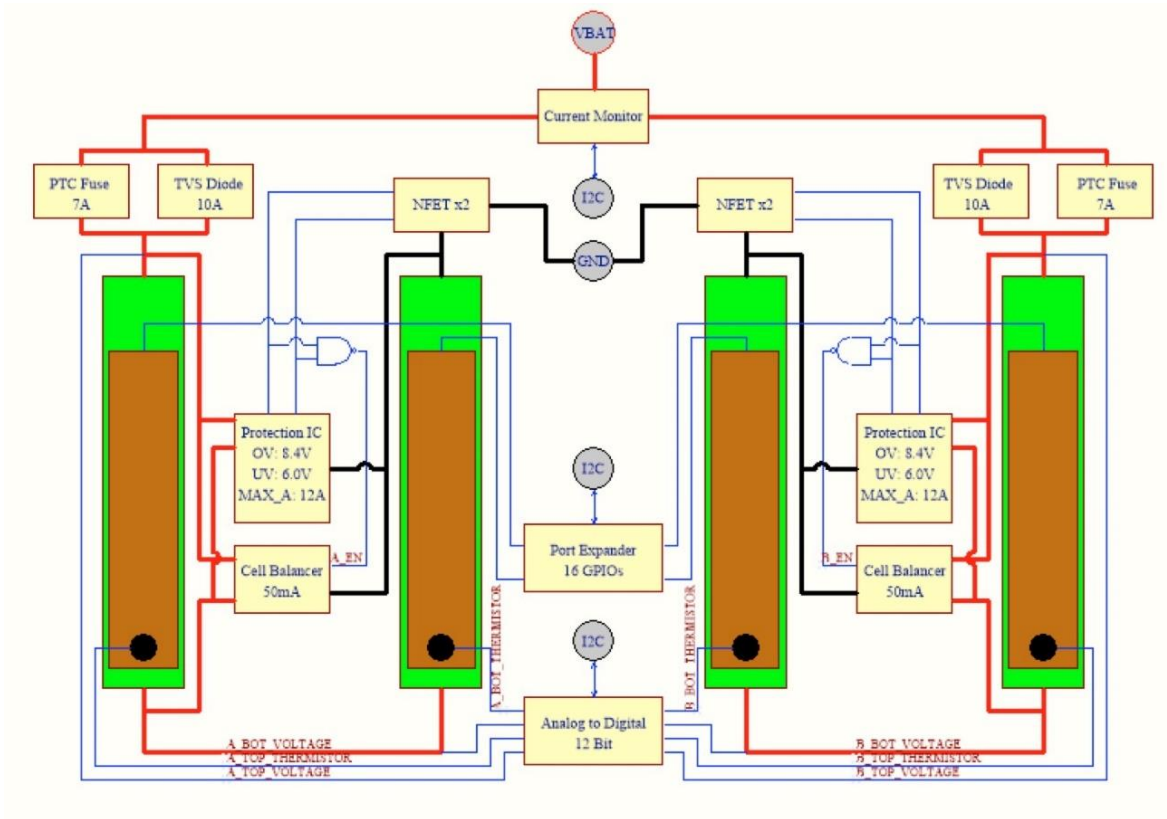
Figure 33: Battery Pack Block Diagram

The battery pack consists of four Lithium Ion 18650 batteries. Each battery needs to be assembled to have a 0.5W Kapton heater and negative temperature coefficient (NTC) thermistor attached to satisfy requirement five. Next, the cells are soldered on the battery pack PCB. The battery pack is constructed with two parallel batteries sub-pack. Each sub-pack contains two 18650 batteries connected in series, passive protection circuit, a battery protection IC and a cell balancer. The battery pack communicates with the Power Board for heater control and passing along voltage and current data for state-of-charge estimation. The assembled battery pack is of size 84x86mm with 20.3mm height which satisfies requirement twelve.

Battery Pack PCB carries one DF-11 connector that is used to transfer raw battery power and I2C communication lines to the power board. Each of the "Battery plus" and "Battery minus"

lines use 6 pins on the DF-11 connector, making the maximum rate current to be 15A. This DF-11 setup is shown in Figure 34 and it meets requirement fourteen.

To satisfy requirement thirteen in terms of grounding, the battery pack PCB offers direct connection to the Power Board's battery minus through the DF-11 connector. The mounting holes are isolated from the battery minus. The grounding scheme is also shown in Figure 34.
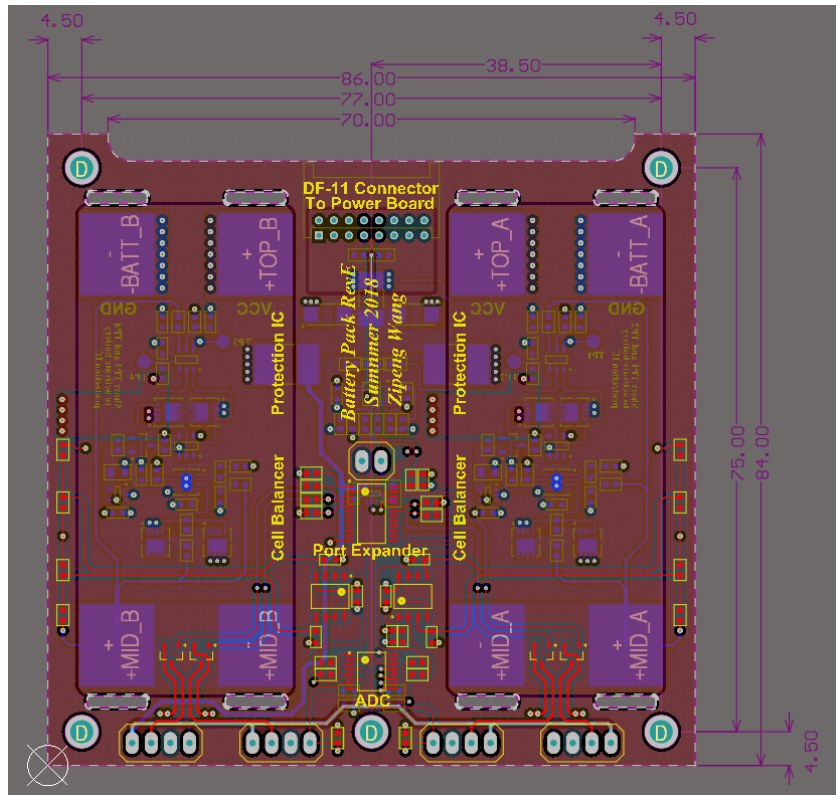
Figure 34: Battery Pack PCB

5.4.5   Hardware Description

5.4.5.1 Lithium Ion Battery

Lithium Ion batteries are common in home-electronics, they are one of the most popular types of rechargeable batteries for portable electronics[24]. Lithium Ion batteries have high energy density, low memory effect, and fast charging speed[25], which makes them ideal for small satellite when space and power generation is of constraint.

Lithium Ion batteries come with their downsides: each individual cell cannot be charged beyond a maximum voltage threshold of 4.2V, the batteries cannot be discharged below a minimum voltage threshold of 2.6V. The batteries can only operate safely in a certain temperature range of between 10C and 50C. If the battery is discharged with the current higher than 2 times the battery capacity, there is a potential of the Lithium Ion battery exploding. None of the conditions above are desirable.

Another problem with Lithium Ion batteries is that no two batteries are alike, each battery has its unique internal chemical composition. Due to the differences, when batteries are connected in a series, they will charge and discharge at different rates. Over time, the two batteries in series will have differences in voltages, which may result in premature charging and discharging cutoff.

IlliniSat-2's battery pack system addresses the disadvantages of the Lithium Ion batteries. Over-voltage, under-voltage and short protection is implemented on the Battery Pack PCB. Each battery cell has its own dedicated thermistor and Kapton heater to regulate the cell temperature. Each two-cell pack includes a bi-directional cell balancer to regulate even charge discharge.

5.4.5.2 Battery Configuration

The battery pack consists of two parallel sub-pack with each pack containing 2 cells. In the event of a battery cell failure, the sub-pack containing the faulty cell will be disconnected while the non-faulty sub-pack continues to operate. The two cells in series bring the pack voltage to be nominal 7.4V. The two packs in parallel bring the pack capacity to 6400mAh. The specifications for individual cell and the entire battery pack[2] is shown in Table 7.

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[2] The specifications is subject to change depending on the choice of Lithium Ion 18650 battery cells.

Specification	Individual Cell	Entire Battery Pack
Nominal Voltage	3.6V	7.2V
Minimum Discharge Voltage	2.5V	5V
Maximum Charge Voltage	4.2V	8.4V
Rated Capacity (Min)	3200mAh	6400mAh
Capacity (Typical)	3350mAh	6700mAh
Charge Current (C/2)	1625mA	3250mA
Discharge Current (C/2)	1625mA	3250mA
Over-charge Current (1C)	3250mA	6500mA
Over-charge Discharge Current (C/5)	650mA	1300mA
Over-discharge Current (1C)	3250mA	6500mA
Over-discharge Charge Current (C/5)	650mA	1300mA

Table 7: Battery Cell and Pack Specifications

5.4.5.3 Battery Protection
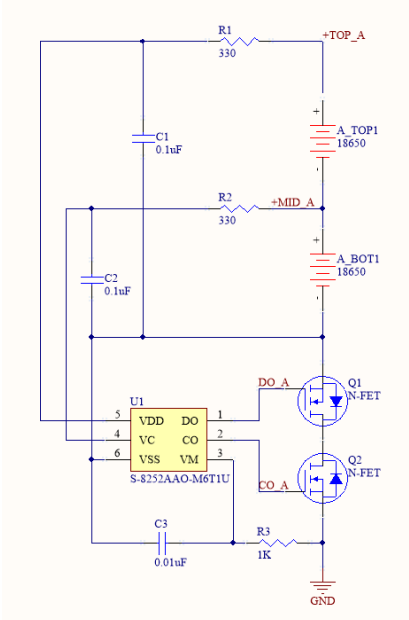
Figure 35: Battery Protection IC Schematic[26]

The battery pack is protected against cell over-voltage conditions through 2 methods: transient voltage suppression (TVS) diode and Battery Protection IC. The TVS diode has a breakdown voltage of 11.1V for the pack and the Battery Protection IC protects single cell against charging over 4.25V. The set up means that when the one individual cell is above 4.25V during

normal charging, the cell protection IC will pull the CO pin to low, which puts the N-FET into non-conducting mode and cut off the faulty cell from the battery pack. The protection IC will reconnect the battery once the battery is in charging condition. If in the case of a high voltage rail accidentally conducts to the battery pack and raises the pack voltage instantly above 11.1V, the TVS diode will limit the voltage to 11.1V to prevent further damage.

The battery pack is protected against under-voltage conditions through the Battery Protection IC. A complete circuit depicting the protection IC is shown in Figure 35. The Battery Protection IC protects single cell against discharging below 2.5V. When an individual cell is below 2.5V, the cell protection IC will pull the DO pin low, which puts the N-FET into non-conducting mode and disconnects the battery from the satellite. The protection IC will reconnect the battery once the battery is put into discharge mode.

The battery pack is protected against overcurrent and external short condition through 2 means: positive temperature coefficient (PTC) resettable fuse and Battery Protection IC. The PTC fuse has a hold current of 7A, trip current of 14A and trip speed of 0.2s. The Battery Protection IC protects single cells against over-current of above 16A with a trip speed of 8ms. During faulty operations of the spacecraft in which the current draw slowly raises to exceed 14A, the PTC fuse will disconnect the battery's plus side from the spacecraft's power line and reset only if the current draw returns to below 7A. During an external short or high transient in-rush current situation, the battery protection IC will instantly toggle DO and CO low to disconnect the battery minus the spacecraft's ground and will reset if such fault conditions are removed.

It is vital that the batteries remain above -10 Celsius at all times and are not re-charged when they are below 0 Celsius. Thus, each battery cell has an NTC thermistor and a 0.5W Kapton heater attached to it to perform thermal regulation in prevention of overheating or freezing the

cells. The Power Board microcontroller is responsible for turning the heaters on/off to make sure requirement five for operation temperature range are fulfilled. The Power Board will read the voltages across the thermistors to determine the temperature of each cell. Depending on the batteries' state of charge, the Power Board will issue the on/off of the Kapton Heaters. The optimal battery operating temperature is around 25 Celsius, so the battery should be kept as close to 25C as possible. If the batteries are below 0 Celsius when the satellite gets solar power, the power must be cut off and transferred to the heater to heat up the battery before charging.

Aside from internal cell protection, the Power Board is also incorporated as a means of external voltage protection. The Power Board reads battery voltages and charge/load current to derive the percentage state of charge of the battery pack. Based on the state of charge of the pack, the Power Board will issue different power states for the satellite to enter. This acts as a method of further protection of the battery and will be further discussed in later sections.

5.4.5.4 Cell Balancing

No two batteries are identical, even the cells that come out of the same batch of manufacturing exhibit slightly different states of charge, capacitance, impedance, self-discharge rate and temperature dependence. As a result, the voltages of two battery cells in a series will diverge over time under the same charging or loading environment, and will potentially cause over-voltage cutoff when the batteries are not fully charged or under-voltage cutoff when the batteries are not fully depleted[27]. A cell balancer in place of cells in a series will minimize the differences of cell's state of charge, thus prolong the battery lifetime.

Among the methods of cell balancing, two practices are the most popular for a battery system, passive bleeding-based cell balancing and active switching-based cell balancing. In passive bleeding-based method, any excess energy from the cell with higher state of charge will

be bled out as heat through a resistor, so that eventually the two cells will have same energy stored. To achieve bleeding cell balancing, the user needs an op-amp to compare two battery cell's voltages and one resistor for each battery cell for the excess power to bleed through. The Op-Amp comparator enable connections to the corresponding resistor with voltage differences beyond a certain threshold is detected. The downside of resistive cell balancing is the low efficiency of this technique due to all the excess power difference being wasted as heat. Bleeding based cell balancing is not recommended when the system has a tight energy constraint.

Net current flow for case when lower voltage > upper voltage shown in red

When FET not conducting

PFET switched at 100 kHz if upper voltage > lower voltage

Li-Ion 3.7V

inductor

NFET switched at 100 kHz if lower voltage > upper voltage

Li-Ion 3.7V

When FET is conducting
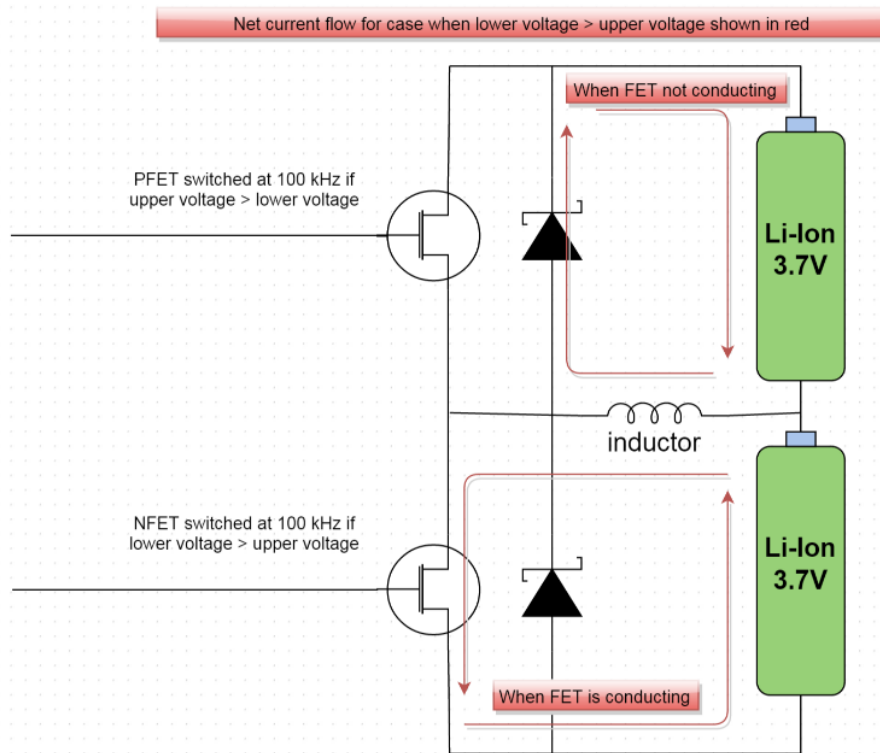
Figure 36: Active Switching Cell Balancing Topology

The active cell balancing system is more complicated than bleeding-based cell balancing. It involves actively transferring power from the cell with higher energy to the cell with lower energy. The approaches for active cell balancing can be capacitive or inductive, with the principle of storing energy from the higher energy cell to a passive device, then transfer that energy from

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the passive device to the lower energy cell. The typical solution for active cell balancing is inductive based balancing based on a buck-switching-regulator topology. The balancing architecture is significantly more efficient because energy is transferred to where it is needed instead of being bled off. Based on Figure 36, if the upper cell is charged/discharged to a higher voltage than the lower cell and the upper MOSFET are switched at 100kHz while the lower MOSFET is turned off. During the switching of the upper MOSFET: when the MOSFET is turned on, the current flows from the upper battery into the inductor; when the upper MOSFET is turned off, the inductor draws current up through the lower diode and charges the lower cell. This process works vise-versa if the lower cell is charged to a higher voltage.

The IlliniSat-2 battery pack system went through six iterations of prototypes with the first five iterations focusing on developing a functioning active switching cell balancing system and the last flight iteration being passive bleeding cell balancing due to time constraint on prototyping the active cell balancer. The first five revisions all had major problems with switching the cell balancing circuit. When the balancer is turned on, the cells lose majority of the power through the inductor instead of transferring the power to lower energy cell. The first five revisions of the design also made use of the wrong negative reference for the cell balancing. They all use spacecraft ground as ground reference instead of battery minus, leaving a conductive path even when the battery is cut off from the rest of the system. The sixth revision of the battery pack uses BQ29209 IC[28] for each two-cell pack with the ground referencing the battery minus. Revision F implemented an automatic battery balancing control to relieve software scheduler burden from the Power Board. Revision F also implemented logic such that when the battery protection IC disconnects the battery from the satellite, the cell balancer also turns off. Revision F is a simpler design and was proven to be functioning for balancing a set of unbalanced batteries.

Figure 37 demonstrates a testing of the resistive-bleeding based cell balancing technique used in Battery Pack Revision F. When the test began, the two batteries in series had 0.3V difference. After two days of idling, the battery cell with higher voltage is balanced to the cell with lower voltage at around 3.46V. Then the two cells stay balanced over the remainder of six days. This test is a validation of requirement eight.
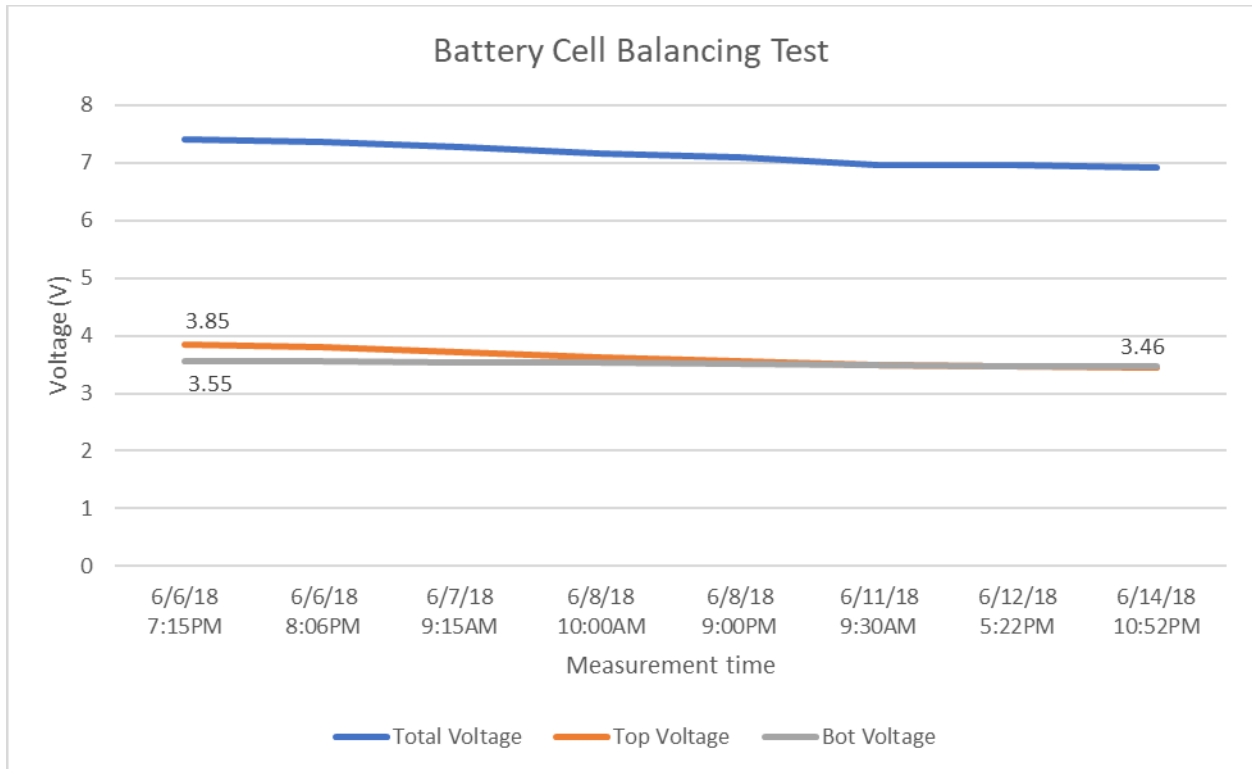
Figure 37: Battery Cell Balancing Test Result

5.4.5.5 Control and Measurement ICs

The battery pack contains three I2C interfaced ICs which are controlled directly by the Power Board's microcontroller. The I2C lines are routed from Power Board's DF-11 connector, through the battery harness into battery's DF-11 connector.

GPIO port expander

A sixteen-channel GPIO chip was used to control heaters. The GPIO chip's pins default as high impedance input on start-up, and they will remain so until the Power Board instructs otherwise. The pin assignment for the port expander is shown in Table 8.

Name	Pin#	When output logic 1	When output logic 0	Default
Upper heater enable (A)	4	Heater for upper cell A is turned on	Heater for upper cell A is turned off	Low
Lower heater enable (A)	5	Heater for lower cell A is turned on	Heater for lower cell A is turned off	Low
Upper heater enable (B)	20	Heater for upper cell B is turned on	Heater for upper cell B is turned off	Low
Lower heater enable (B)	19	Heater for lower cell B is turned on	Heater for lower cell B is turned off	Low

Table 8: Port Expander GPIO Assignment

Analog to Digital Converter

An eight-channel ADC IC is used to measure battery temperatures and voltages with 12-bit precision. Measurements are sent to the Power Board microcontroller with the pin assignment shown in Table 9. Voltage measurements are made at the midpoint of each battery pack half and the top of each battery pack half. The ADC IC is only able to measure voltages in the range of 0~3.3V, the battery mid voltage usually has the range of 3V~ 4.2V, and the battery top voltage usually has the range of 6V~8.4V. As a result, a 2:1 voltage divider for a battery mid voltage measurement, a 4:1 voltage divider for a battery top voltage measurement. All the dividers also undergo buffering with rail-to-rail, unity gain stable AD8607 op-amps.

Name	Pin#	Description
Voltage (top point B)	7 (IN1)	12-bit value corresponding to top point B voltage 0 = 0V, 4095 = 8.4V, resolution: ~4 mV
Voltage (top point A)	14 (IN2)	12-bit value corresponding to top point A voltage 0 = 0V, 4095 = 8.4V, resolution: ~4 mV
Voltage (midpoint B)	8 (IN3)	12-bit value corresponding to midpoint B voltage 0 = 0V, 4095 = 4.2V, resolution: ~2mV
Voltage (midpoint A)	13 (IN4)	12-bit value corresponding to midpoint A voltage 0 = 0V, 4095 = 4.2V, resolution: ~2mV
Temperature (lower cell B)	9 (IN5)	12-bit value corresponding to lower cell B temperature Higher value = higher temperature, nonlinear, needs calibration
Temperature (lower cell A)	12 (IN6)	12-bit value corresponding to lower cell A temperature Higher value = higher temperature, nonlinear, needs calibration
Temperature (upper cell B)	10 (IN7)	12-bit value corresponding to upper cell B temperature Higher value = higher temperature, nonlinear, needs calibration
Temperature (upper cell A)	11 (IN8)	12-bit value corresponding to upper cell A temperature Higher value = higher temperature, nonlinear, needs calibration

Table 9: Battery Pack ADC Channel Assignment

Current Reader

Revision A to D battery pack designs only use voltage to estimate the state-of-charge of the battery pack. Using voltage to measure capacity is not accurate and usually results in 10~20% of estimation error. Revision E and F designs incorporated a current sensor on the high side of the battery pack to measure the load/charge current going in/out the battery pack. The current sensor measures voltage across a 5 mOhm shunt resistor, returns the voltage in two's compliment fashion with 2.5uV of resolution. The 5 mOhm shunt resistor is connected in a four-wire Kelvin fashion to avoid additional resistance.

5.4.6 Battery Pack Assembly

The flight battery pack circuit boards are professionally manufactured and assembled by Sierra Circuit under class two standard. The battery pack circuit boards come without Li-ion batteries attached. To assemble the battery pack for flight configuration, the following procedures are followed:

1. Peel the plastic skin off battery with an x-acto knife. Measure the battery's physical dimension. Visually analyze the battery cell for any physical defect.

2. Cut the battery tab to be 15mm and shield the battery tab with Kapton to avoid accidental shorting.

3. Shorten the Kapton heater and thermistor cable length to 15mm. Apply Pressure Sensitive Adhesive to the back side of the Kapton Heater. Without peeling off the release layer, apply pressure to activate one side of the PSA.

4. Peel off the release layer and attach the Kapton heater onto the battery, apply pressure to activate the PSA on the other side. Wrap Kapton tapes around the battery cell to secure the heater. A assembled battery cell is shown in Figure 38.
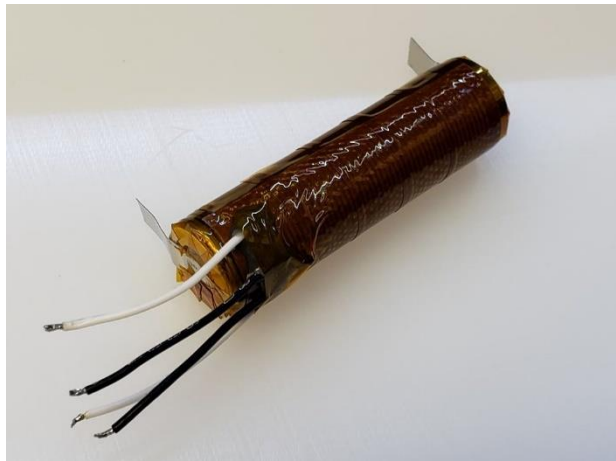
Figure 38: Assembled Battery Cell

5. Solder the assembled battery to the battery pack PCB through the taps attached at the positive and negative sides.

6. Plug the heater wires to the corresponding heater holes in the battery pack PCB and solder the wires in place.

7. Remove the no-clean flux using flux cleaner and 91% isopropyl alcohol.

5.4.7   Battery Verification through Testing

To certify the battery pack for spacecraft flight's safety standard, especially storage on board the International Space Station in the example of LAICE CubeSat, the battery pack needs to undergo six tests: electrochemical test, charge cycling test, over-voltage test, under-voltage test, external short test, vacuum test, and vibration test. The next few subsections will go through each individual test and result of testing.

In Revision A to E, the battery's control and measurement ICs can only be powered by internal 3.3V power line on the battery pack. Such an approach has two short comings: Firstly, there is no way to power-off those ICs without physically or electrically removing the battery pack; Secondly, when the battery is cutoff at faulty conditions, those ICs will also be powered off which results in blank readings. In Revision F, a two-pin pin header is added, so that the tester can have the option to either use the internal 3.3V supply or external supply. This small change resulted in more reliable readings and provides a way to reset the measurement ICs without removing the battery cells. For final flight configuration, the two pins on the pin header will be connected through a blob of solder.

All the batteries verification tests are automated using a Visual Studio C++ Software. The software controls the setting of a power supply and a programmable to put the battery pack into charge or discharge mode. The software also communicates with a MSP4305229 Launchpad running Power Board Software to gather voltage, temperature and current data regarding the battery pack. The software saves all the acquired data into a .csv file.

5.4.7.1 Charge Cycling test

The battery charge cycling test charges and discharges the battery 5 times to determine the capacity of each battery. The objective of the cycling test is to ensure the batteries don't have internal defects. If the cell capacity does not drop below 5% throughout the test, the battery pack pass the charge cycling test.

Testing Steps

1) Charge the batteries to 4.2V using a current of 3250mA.
2) 10 minutes rest period.
3) Discharge the batteries to 3.0V using a current of 3250mA.
4) 10 minutes rest period.
5) Charge the batteries to 4.2V using a current of 3250mA.
6) 10 minutes rest period.
7) Discharge the batteries to 3.0V using a current of 3250mA.
8) 10 minutes rest period.
9) Charge the batteries to 4.2V using a current of 3250mA.

Recording Elements

1) Individual cell voltage readings through Battery Pack's 12-bit ADC.
2) Charge and discharge current through Battery Pack's current reader.
3) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.

Result and Analysis
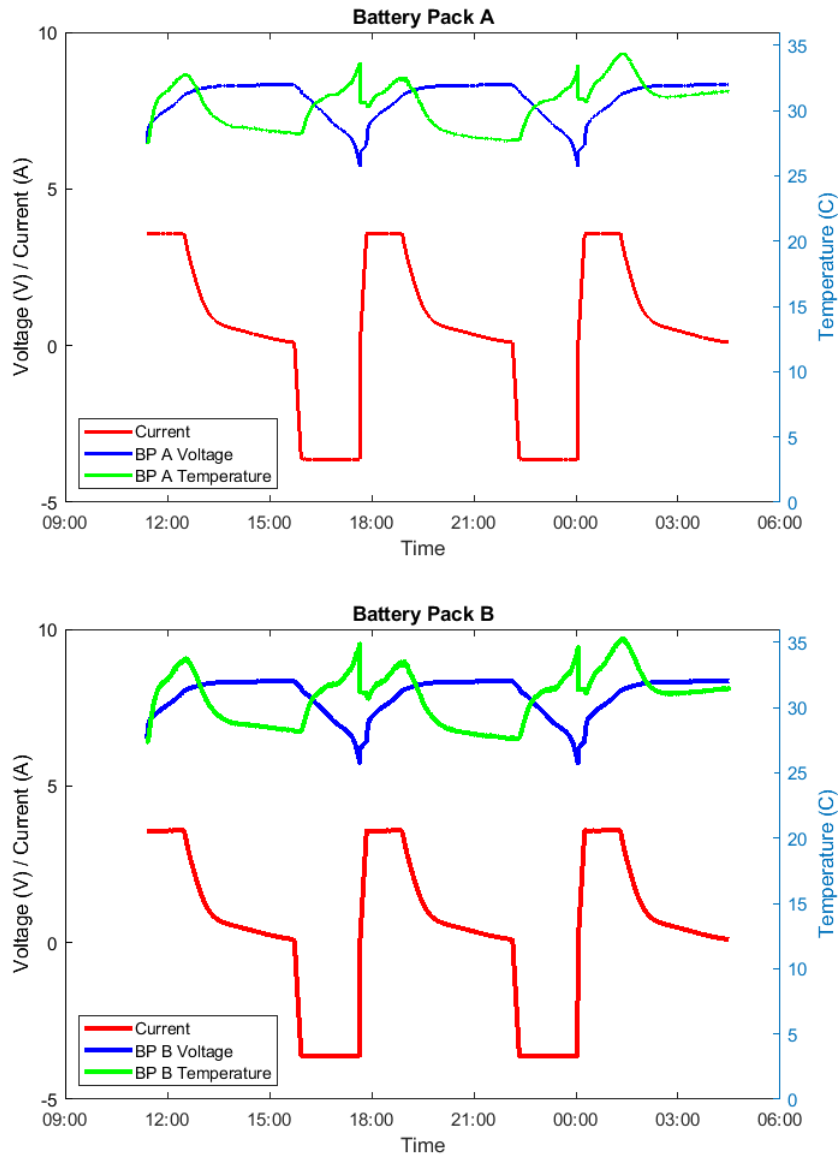
Figure 39: Battery Charge Cycling Result of Pack A and B

Based on the data collected and plotted in Figure 39, the total battery pack has a totally capacity of 6295mAh. The total capacity didn't change during the two charge cycles and the temperature didn't increase above 50C. indicating healthy batteries. This result satisfies requirement one.

5.4.7.2 Cell Over-charge Test

The cell over-charge test tests the battery pack's ability to handle a situation where the batteries are charged to a voltage beyond the rated maximum charge voltage. When a Lithium Ion battery is fully charged, any additional charge will cause the plating of metallic lithium and compromise the safety[29]. The protection will cut the battery from the satellite power line when the pack voltage is above 8.4V, resulting in 0A charge current. The battery pack will be reconnected once the batteries are put into a discharging state.

Testing Steps

1) Over-charge the batteries using a current of 6500mA when the battery pack is at 7.4A.
2) Wait until the charging current is 0A. Record the voltage at which the protection activates and the MOSFET opens the circuit.
3) Discharge the batteries, using a current of 1300mA and record the voltage at which MOSFET closes the circuit.
4) Wait until the MOSFET is closed, which means the discharge current is at 1300mA. Record the voltage when the MOSFET is closed.
5) Discharge the batteries to 3.0V using a current of 3250mA.
6) 10 minutes rest period.
7) Charge the batteries to 4.2V using a current of 3350mA. Record the capacity of the battery pack.

Recording Elements

1) Individual cell voltage readings through Battery Pack's 12-bit ADC.
2) Charge and discharge current through Battery Pack's current reader.
3) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.

Result and Analysis
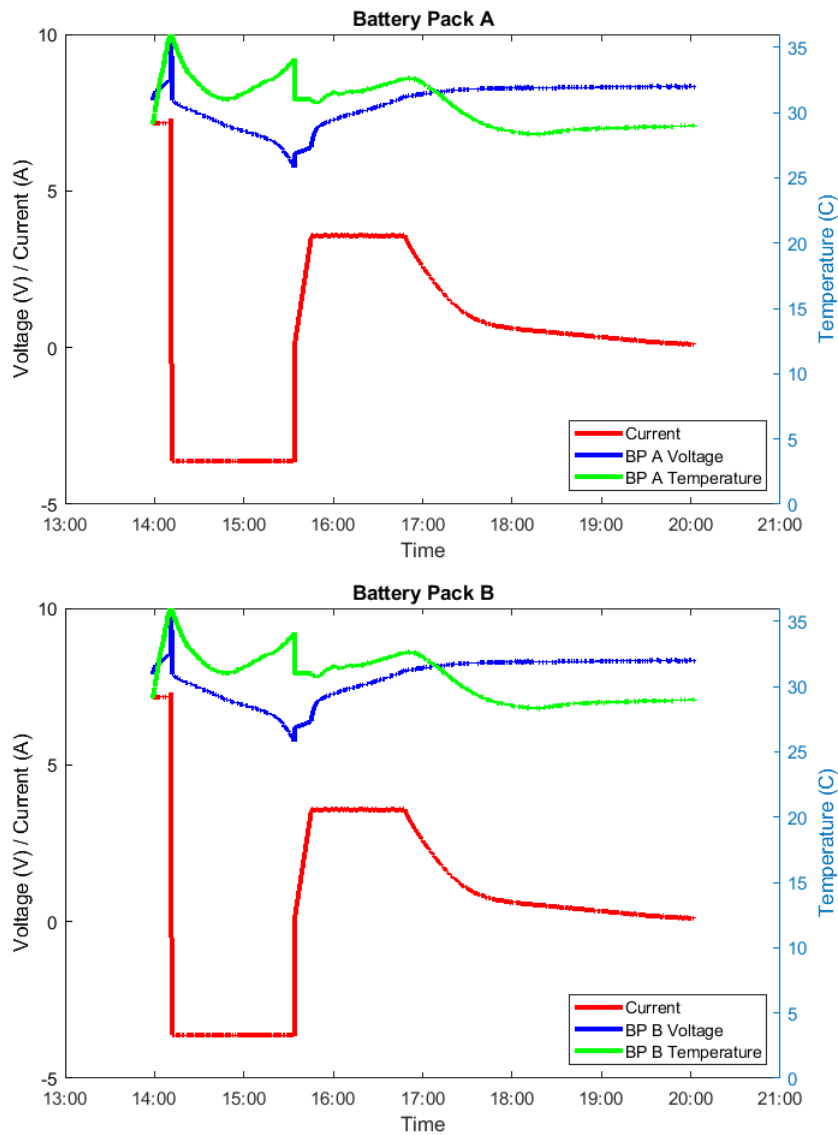
Figure 40: Battery Overcharge Result of Pack A and B

Based on the data collected and plotted in Figure 40, the battery pack gets cut off from the main power supply when the pack voltage is at 8.6V. The MOSFET reconnects the battery to the circuits during when the battery pack is discharging and the pack voltage is 8.1V. The total pack capacity after overcharging test is 6272mAh which is 0.35% lower than the capacity derived from the charge cycling test. The overcharging test is a success and it satisfies requirement two.

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5.4.7.3 Cell Over-discharge Test

The cell over-discharge test examines the battery pack's ability to handle a situation where the batteries are discharged to a voltage beyond the rated minimum discharge voltage. When a Lithium Ion battery is discharged below 2.5V, any additional discharge current will cause copper in the anode to dissolve into the electrolyte. When the battery is charged from an over-discharged situation, the dissolved copper can create dendrites that might cause a short circuit inside the battery that may cause venting of the electrolyte[30]. The protection will cut the battery from the satellite power line when the pack voltage is below 5V, resulting in 0A discharge current. The battery pack will be reconnected once the batteries are put into a charging state.

Testing Steps

1) Over-discharge the batteries using a current of 6500mA when the battery pack is at 7.4A.
2) Wait until the discharging current is 0A. Record the voltage at which the protection activates and the MOSFET opens the circuit.
3) Charge the batteries, using a current of 1300mA.
4) Wait until the MOSFET is closed, which means the charge current is at 1300mA.
5) Charge the batteries to 4.2V using a current of 3250mA.
6) 10 minutes rest period.
7) Discharge the batteries to 3.0V using a current of 3250mA.
8) 10 minutes rest period.
9) Charge the batteries to 4.2V using a current of 3350mA. Record the capacity of the battery pack.

Recording Elements

1) Individual cell voltage readings through Battery Pack's 12-bit ADC.
2) Charge and discharge current through Battery Pack's current reader.
3) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.

Result and Analysis
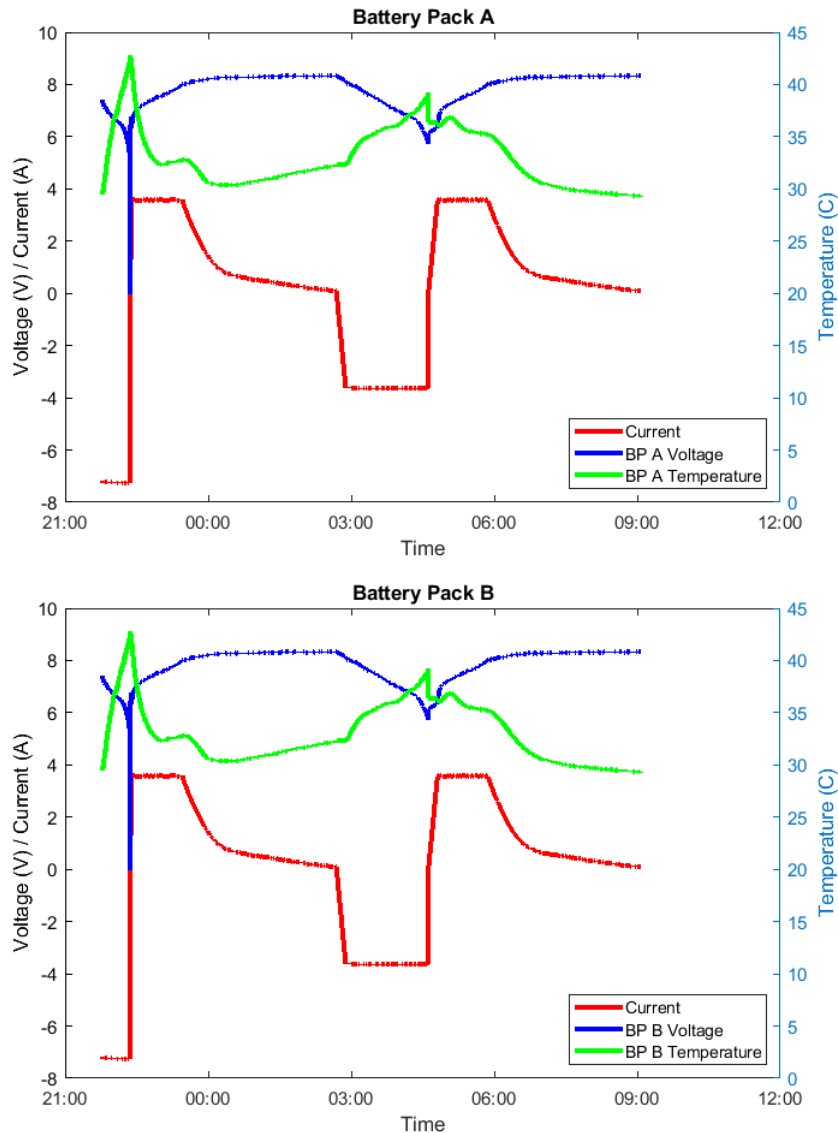
Figure 41: Battery Overdischarge Result of Pack A and B

Based on the data collected and plotted in Figure 41, the battery pack gets cut off from the main power supply when the pack voltage is at 5V. The MOSFET reconnects the battery to the circuits during when the battery pack is charging and the pack voltage is 6.4V. The total pack capacity after overdischarging test is 6315mAh which is 0.33% higher than the capacity derived from the charge cycling test. The overdischarging test is a success and it satisfies requirement three.

5.4.7.4 External Short Test

The cell external short test checks the battery pack's ability to handle a situation where the batteries are shorted. When a short is created external to the battery, a large amount of current will flow from the batteries into the area shorting, generating a lot of heat and can cause hyper-venting of the electrolyte. The protection will cut the battery from the satellite power line when the discharge current is above 8A. The battery pack will be reconnected once the short is removed and the battery is put into a charging state.

Testing Steps

1) Externally short the batteries using a 10mOhm, 100W Chassis mount resistor.
2) Record the current at greater than 1KHz rate for the first 3 seconds of the test. Record the current when the MOSFETs disconnects the circuit.
3) Charge the batteries, using a current of 1300mA. Record the voltage at which the MOSFET reconnects the circuit.
4) Discharge the batteries to 3.0V using a current of 3250mA.
5) 10 minutes rest period.
6) Charge the batteries to 4.2V using a current of 3350mA.

Recording Elements

1) Individual cell voltage readings through Battery Pack's 12-bit ADC.
2) Charge and discharge current through Battery Pack's current reader.
3) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.

Result and Analysis
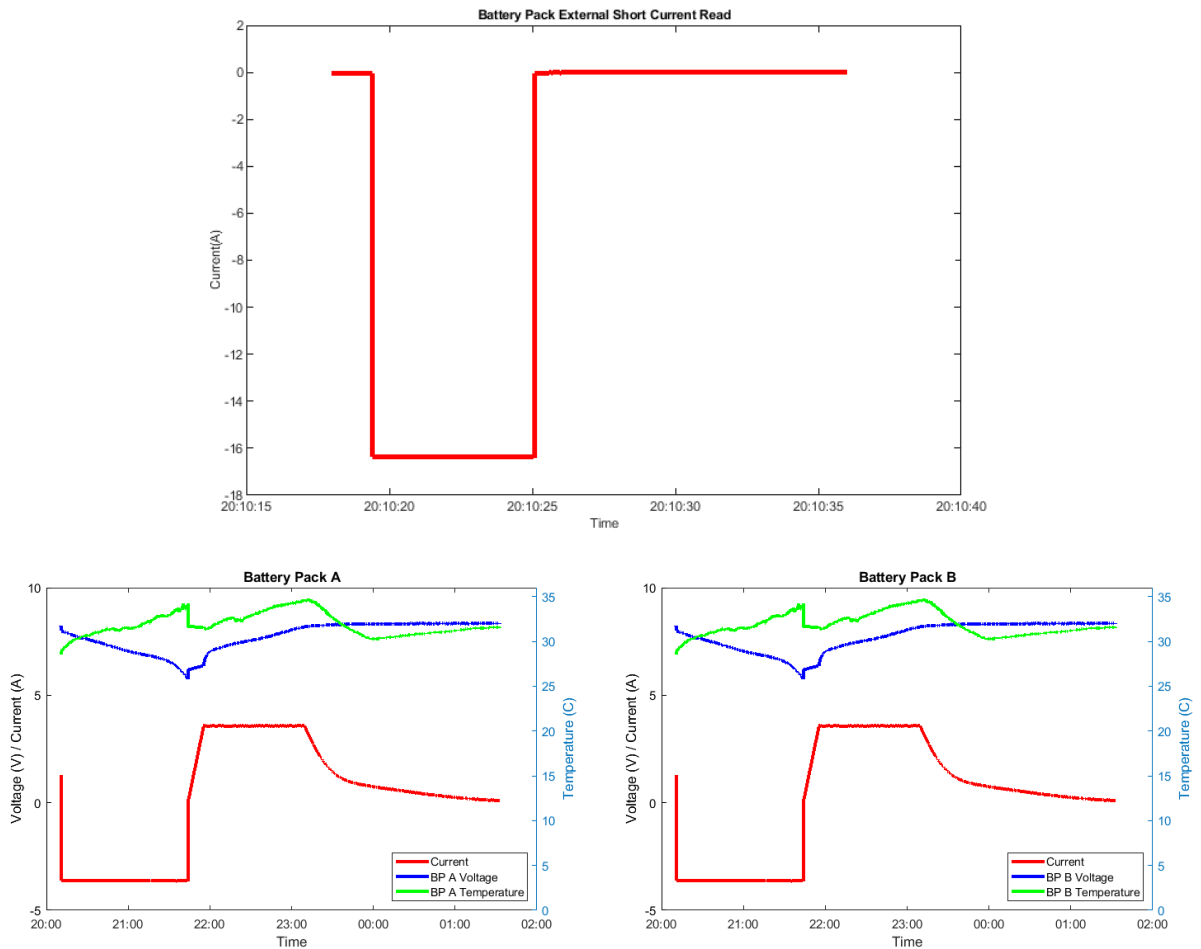
Figure 42: Battery External Short Result of Current Reading, Pack A and B

Based on the data collected and plotted in Figure 42, the battery pack disconnects the battery cells from the satellite two seconds after the cells are shorted. The MOSFET reconnects the battery pack once the short is removed and battery started discharging. The battery pack's capacity after external short test is 6284mAh which is 0.15% lower than the capacity derived from the charge cycling test. This test demonstrated the battery pack's ability to handle external short situation and thus satisfies requirement four.

5.4.7.5 Battery Vibration Test

The vibration test examines the battery pack's ability to handle a vibrational situation like a rocket launch. Vibration can potentially cause breaking of electrical traces around the mounting holes or cracking the internal structures of capacitors and resistors causing shorts. The Battery Pack mitigates the vibration damage by adding a battery plate to hold the bottom of the battery pack, the battery cells are pressed against the middle plate for additional mechanical support.

Testing Steps

1) Assemble the battery pack onto the vibration plate according to NASA mechanical spec[31].
2) Before Vibration test, perform one charge cycling to determine the Battery Pack's capacity.
3) Bolt the battery pack onto a vibration table at Engineered Testing System at Indianapolis, IN.
4) Record the OCV for each cell on the battery pack before the vibration starts.
5) Vibrate the battery according to NR-SRD-139 table 1[22]. Measure OCV for each battery before vibration testing and between each axis of vibration testing.
6) After the vibration, perform one charge cycling to determine the Battery's capacity.

Recording Elements

1) Multimeter with 0.001V precision.
2) Individual cell voltage readings through Battery Pack's 12-bit ADC.
3) Charge and discharge current through Battery Pack's current reader.
4) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.
5) Accelerometer attached externally to the battery pack, to analyze for the resonance point.

Result and Analysis

	A Top (V)	A Bottom (V)	B Top (V)	B Bottom (V)
Pre-Vibration	4.155	4.148	4.162	4.141
Post-X- Vibration	4.155	4.148	4.162	4.140
Post-Y- Vibration	4.154	4.148	4.162	4.141
Post-Z- Vibration	4.155	4.148	4.162	4.141

Table 10: Vibration Test Voltage Measurement result

The results were generated using the battery pack revision D for LAICE mission. The voltage measure of each cell was shown in Table 10, indicating that the cells remain intact after vibration on each axis. The capacity of the battery pack before vibration test is 6090mAh.The capacity of the battery pack after vibration test is 6050mAh. The battery performs well after vibration test satisfying requirement six.

5.4.7.6 Vacuum Test

The battery pack vacuum test tests the battery's response for long term operation in a vacuum. If the Lithium Ion battery is not sealed correctly, operating in a vacuum may cause leaking from the battery cell. The vacuum test uses on the physical parameters of the battery before and after being in a low-pressure vacuum, as well as the battery capacity to determine if any damaged is caused to the batteries during vacuum operation.

Testing Steps

1) Measure battery pack's length, width, height, mass and voltage before vacuum test, the measurements should be recorded with 0.1mm/0.1g/0.001V precision.
2) Perform charge cycling test on the battery pack before vacuum test.
3) Place the fully charged batteries into the vacuum chamber at atmospheric pressure and pull vacuum at approximately 8psi/minute. Maintain vacuum at approximately 0.1 psia for 6 hours, re-pressurize the chamber to ambient at a rate of 9psia/s.
4) Perform charge cycling test on the battery pack. The change in capacity should be less than 5%.
5) Perform visual inspection for indication of leaks.
6) Measure battery pack's length, width, height, mass and voltage. The change in those parameters should be less than 0.1%.

Recording Elements

1) Scale with 0.1g precision.
2) Caliper with 0.1mm precision.
3) Multimeter with 0.001V precision.
4) Individual cell voltage readings through Battery Pack's 12-bit ADC.
5) Charge and discharge current through Battery Pack's current reader.

6) Individual cell temperature readings of 50K Ohm NTC thermistor through Battery Pack's 12-bit ADC.

Result and Analysis

	Pack A	Pack B
Length	65.52mm	64.94mm
Width	38.79mm	38.44mm
Height	20.35mm	20.40mm
Mass	227.2g	
Voltage	Top(4.22V), Bot(4.18V)	Top(4.23V), Bot(4.18V)
Capacity	6110mAh	

Table 11: Battery Parameters Before Vacuum Test

	Pack A	Pack B
Length	65.53mm	64.93mm
Width	38.60mm	38.46mm
Height	20.38mm	20.42mm
Mass	227.2g	
Voltage	Top(4.20V), Bot(4.17V)	Top(4.21V), Bot(4.16V)
Capacity	6134mAh	

Table 12: Battery Parameters After Vacuum Test

The battery pack survive the vacuum operation with almost no parameter change, thus satisfies requirement seven.

5.4.8 Remaining Issues and Potential Fix for Next Revision

So far, no issues were found with Revision E. However, there are several suggestions for the next revision of the battery pack.

For next revision of the battery pack, the correct move is to switch back to the active switching-based cell balancing. Revision F used passive cell balancing mainly due to time constraint of the mission delivery date. When time is not an urgent factor, developing an active cell balancing with much higher theoretical efficiency compared is more desired for a small spacecraft. The low efficiency in our current design could just be an inductor selection issue. The current selection of the 68uH inductor has 0.95Ohm to DC resistance, while the current Digi-key

selection has 68uH inductor with 89mOhm DC resistance. This means the inductor could be wasting 10 times more heat. For the next revision, the ground of the cell balancing should be referenced to the battery minus.

5.4.9   Summary of Contribution

The battery pack design can be successfully charged and discharged with no observed damage or overheating. The battery pack PCB can protect the batteries from overcharge, overdischarge and external short conditions while maintain the state of charge balance of the battery cells. The battery pack can operate in vibrational environment as well as vacuum environment with no observed parameter change. Lastly, the battery pack is capable of communicating with the power board to delivery its current, voltage and temperature measurement, as well as letting the power board control battery's heaters to maintain the safe operating temperature. In conclusion, the battery pack revision F design satisfies all the requirements listed in the section 5.3.2.

5.5 Power Distribution and Monitoring - Power Board

5.5.1 Introduction

The Power Board is responsible for ensuring safe operation of the CubeSat by managing the batteries as well as monitoring current consumption of the subsystems. The Power Board is in charge of charging the batteries through the solar panel. It monitors the battery's state of charge to determine different power states. Power Board also answers to commands from C&DH that perform health monitoring, provide debugging interface for its on-board microcontroller and C&DH's Linux processor, RBF and KS interfaces for turning off the satellite, as well as controls and monitors the power delivery to the rest of the system. All the power is run through the Power Board so that no system can be turned on unless we determine it is safe for them to be on.

5.5.2 Requirements

5.5.2.1 Hardware requirements

1. The Power Board shall incorporate a low power central microcontroller for communication with C&DH, power delivery control and monitoring.

2. The Power Board shall convert the power from the solar panel into battery level power to distribute to the system or charge the batteries.

3. The Power Board shall support physical mounting and electrical connection of a maximum of 6 solar panels

4. The Power Board shall control the power delivery to the rest of the system.

5. The Power Board shall monitor the power delivery to the rest of the system.

6. The Power Board shall have a safety factor of 2 in terms of high current trace width.

7. The Power Board shall disconnect power from the satellite upon the insertion into a Remove Before Flight connector or pressing of the switches on the bottom of the satellite. The disconnection shall happen at 3 locations on the power line.

8. The Power Board shall be capable of charging the battery with the RBF plugged in.

9. The Power Board shall provide control and electrical interface for the thermal knives.

10. The Power Board shall provide 3.3V voltage rail to the rest of the system with back up.

11. The Power Board shall carry a RS485 transceiver to deliver communication to the ADCS system**.**

12. The Power Board shall comply with the Illinisat-2 grounding scheme.

13. The Power Board shall use DF-11 connectors as per the power and data interface design.

5.5.2.2 Software Requirements

1. The Power Board software shall initiate a 50min countdown upon the release of foot switches. The countdown shall be a one-time event that shall not restart upon future reboot of the Power Board.

2. The Power Board software shall communicate with the sensors on the battery pack to acquire voltage, temperature and current information.

3. The Power Board software shall control battery pack's heater based on the temperature reading.

4. The Power Board software shall estimate battery pack's state of charge and enter the satellite into corresponding power state.

5. The Power Board software shall correctly respond to commands from C&DH with 115200 bit-per-second baudrate.

6. The Power Board software shall monitor current consumption from rest of the subsystem and turn off ones that are in the faulty stage.

7. The Power Board software shall act like C&DH's watchdog to determine if the C&DH is at false state. The Power Board shall reboot C&DH if C&DH is at a false state.

5.5.3 Revision History

The first revision of the Power Board was design by Nathan Poland in fall 2014, as a prototype testing board. The first revision of the Power Board had a faulty kill switch system that did not cut off the batteries from the satellite when pressed. The first revision also included eight RS485 transceivers for each of the Flex Cable connections, which were later deemed unnecessary.

The second revision of the Power Board was designed by Nathan Poland and the author in fall 2015 and was professionally manufactured by Sierra PCB. Revision B fixed the kill switch issue, implemented kill switch RBF priority circuit. Revision B cut the RS485 transceiver number from 8 to 1. Revision B included additional 3.3V Buck Converter as a fail-safe measure. Several hardware issues were noticed during thorough software implementation of the Power Board. Firstly, the I2C line on the Power Board was flipped. An emergency bit-bang I2C protocol had to be implemented for flipped wire I2C. Secondly, the USB module on the microcontroller was not powered, which disabled the USB module. Thirdly, the grounding scheme of the Power Board was 4 direct grounding on the four mounting holes, which created ground current loops. Fourthly, the UART communication line between C&DH and Power Board was flipped. Lastly, the thermal knife's P-MOSFET lacked a gate driver to full saturate the PFET for conduction. One major mechanical issue was also noticed, the mating connector between Power Board and C&DH was shifted by 1mm. Revision B had the fixes implemented to address above issues and was flown by CubeSail mission.

The third revision of the Power Board was designed as part of this work during fall 2017. Revision C fixed all the previous problems regarding the Power Board. Revision C also added several improvements to the Revision B design. Revision C added pull-down resistors to set the hardware default state of the Hot-swap controllers. Revision C added the option for the user to turn on automatic Hot-swap restart. Revision C changed certain passive components' sizes from 0402 to 0603 for better solderability. Revision C also organized the silkscreen on the PCB for better aesthetic. Revision C Power Board is tested to be fully functional and will be flown by the three USIPs mission and LAICE mission. The PCB layout for Power Board Revision A to Revision C are attached in Appendix B.

5.5.4   Hardware Function Overview
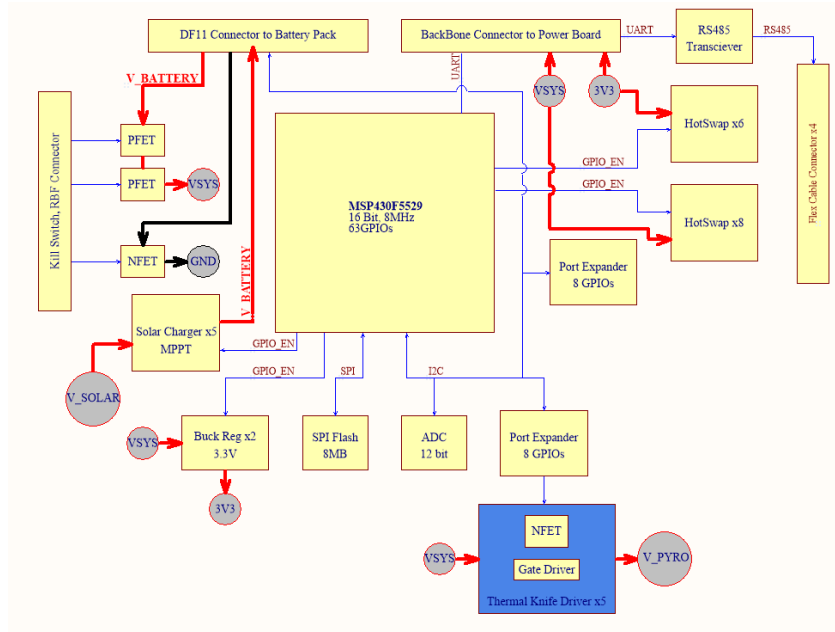
Figure 43: Power Board Block Diagram

The Power Board consists of central microcontroller MSP430F5529 for C&DH command handling, data acquisition and power system autonomous monitoring. The block diagram for the Power Board is shown in Figure 43. The Power Board included 14 Hot-swap controllers to control

delivery of battery and 3.3V power to the rest of the subsystems. The Hot-swap controllers also provide the Power Board with current information of each subsystem. The Power Board converts the solar panel into battery acceptable power and charge the battery through 5 on-board MPPT solar chargers. 5 P-MOSFETs along with their corresponding driver circuits are implemented to control the firing of the thermal knives. Lastly, the Power Board included kill switch and RBF circuits to cut the battery power from rest of the satellite on-demand.

The physical dimension of Power Board is 90 x 90mm in dimension with cable drench cut out for harness pass through. The maximum height of the Power Board is 11.72mm, when mated with the C&DH, the mated height is 21.84mm. The Power Board design PCB consists of 6 layers of 2oz copper, with stacking topology of signal-ground-power-power-ground-signal.

Power Board PCB carries eight DF-11 connectors. Among them, five DF-11 connectors are used to provide power interface to the battery pack, radio and three payloads. One DF-11 connector provides satellite debug interface. The rest two DF-11s serve as the Kill Switch and RBF. The PCB also contains a backbone connector. The backbone connector on the Power Board mates with the C&DH to receive power and distribute commands to power board, ADCS and debug console. This setup is shown in Figure 23 meets requirement thirteen. The Power Board also offers three expansion headers to provide extra power and data interface for 6U configuration.

To satisfy requirement twelve in terms of grounding, Power Board PCB offers three resistors pads RG1 to RG3 near the mounting holes. One of the resistors will be a zero-Ohm resistor shorting the satellite ground to Chassis while the other two be 3MOhm. This configuration forms a single point star ground.
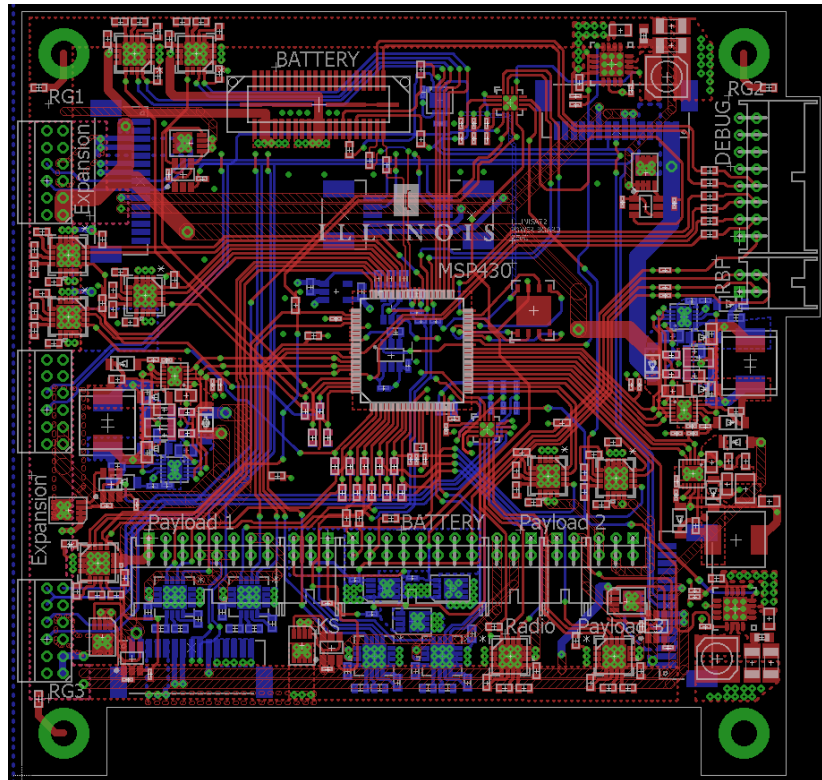
Figure 44: Power Board PCB

5.5.5 Hardware Description

5.5.5.1 Microcontroller – MSP430F5529

The Power Board has several flow-down requirements for the microcontroller. The microcontroller is required to operate at low power consumption because it will always be turned on throughout the mission life time. The microcontroller is required to have high number of GPIO pins to control and monitor all the hot-swaps and solar chargers. The microcontroller is required to have at least one I2C and SPI bus peripheral to communicate with different digital sensors for house-keeping. The microcontroller is required to have one UART interface to communicate with C&DH. The microcontroller is required to run at least 8MHz for less communication latency.

Lastly the microcontroller is required to have at least 14 analog input with at least 10-bit resolution to read current from the hot-swaps.

The microcontroller chosen as the main processor is the Texas Instrument's MSP430F5529[32]. MSP430F5529 fulfills almost all the microcontroller requirements, as well as requirement one in section **5.4.2**. MSP430F5529 has 63 I/O pins with 16 of them being analog inputs, the whole software suite for MSP430 can be ran at 2mA at idle state and it has two I2C, SPI and UART interface peripherals. The only downside is the lack of GPIO pins, the Power Board requires 65 GPIO pins to control and monitors all on-board devices and only 49 pins are available. The lack of GPIO pins was compensated by having 2 I2C port expanders that offer 16 extra GPIOs in total. The most important reason for choosing MSP430F5529 was because of the already existing Texas Instrument's popular evaluation board "MSP430F5529 Launchpad". The popularity of MSP430F5529 among embedded software engineers means a more complete software support for developing embedded drivers, as well as more help from the internet when issues are encountered. Noted that the software development done in MSP430F5529 can be ported to other MCUs within MSP430x5xxx family with minimal change.

MSP430F5529 is powered by an independent 3.3V Low Dropout regulator apart from the rest of the system to ensure that MSP430F5529 remains powered on when the rest of the satellite is powered off during mission lifetime. MSP430 IC has an external 32.768kHz crystal to have a real-time clock with low drift. MSP430F5529 includes an external watchdog timer IC to detect and recover from a Power Board software malfunction. Every 140ms the MSP430 chip will send a 2ms width pulse to the watchdog timer IC, if the 140ms window is missed, the watchdog will toggle the low-enabled reset pin to reset the MSP430 software.

The Power Board can be programmed and debugged using MSP430F5529. MSP430F5529 launchpad includes two circuit parts. The first part is debugging the interface, it has an eZ-FET on-board emulator that enables debugging/programming as well as communication back to the PC. The second part is the actual MSP430F5529 circuit. The designer can disconnect the debugger from the launchpad through the jumpers, connect the debugger to the Power Board's debug port to program and debug the Power Board. Having a cheap launchpad as the debugger compared with an expensive debugger saved a lot on development cost.

5.5.5.2 Maximum Power Point Tracking Solar Charging

Maximum Power Point Tracking, short for MPPT, is a technique to operate the solar cells at the peak power of the IV curve for maximum charging efficiency. Currently, there are two implementation methodologies for MPPT charging: constant operating voltage charging[33] and perturb observe charging[34].

Constant operating voltage charging let the designer set a minimum input voltage threshold to enable the charger. The charger turns on charging when the input voltage is above the set level. If the minimum input voltage is set near the maximum power point of the IV curve, the solar charger will be operating near maximum charging efficiency when charging is at full sunlight. Constant operating voltage charging requires the designer to set the enable voltage through a resistor divider. Once the voltage is set, it cannot be changed for flight, which makes constant operating voltage charging a rigid design. The designer can get with the rigidity by using several resistors dividers. Each resistor divider will have a dedicated MOSFET for the microcontroller to select input voltage. This divider network method will undoubtedly increase the complexity of the PCB as in it will require more components. The selection of which divider to use is also problematic because it will require the microcontroller to know the status of the solar charger,

namely voltage and current, which further increases the complexity. Currently there are many ICs in the market that offers set-point MPPT charging.

The second way of maximum power point tracking charging is called perturb and observe charging. Perturb and observe algorithm falls into the category of hill climbing algorithm, which involves taking steps over sampled data to reach desired level. To achieve such charging methodology, the microcontroller needs to perturb the charging current by increasing or decreasing the PWM wave's duty cycle, record the input power through voltages and currents, compare the power with the previous measure point, until the charger deems the input power to be at maximum. Perturb and observe can be implemented analogously or digitally and is usually complex to design. When designed correctly, buck-boost perturb and observe charging can bring charging efficiency to around 95%. Unfortunately only one commercially available chip exists to support buck-boost perturb and observe charging, the LT8490. A prototype was design to determine its feasibility for Illinisat-2, and due to its complexity, this approach was deemed not sufficiently reliable.

For the IlliniSat-2 bus, Constant operating voltage Maximum Power Point down-regulation charging with single voltage set point is used through LT3652 IC. The LT3652 is a step-down battery charger that operates over a 4.95V to 32V input voltage range. It provides a constant-current and constant-voltage charge characteristic, with maximum charge current externally programmable up to 2A. The charger can set the desired battery float voltage up to 14.4V with a resistor divider. The LT3652 employs an input voltage regulation loop, which reduces charge current if the input voltage falls below a programmed level, set with a resistor divider. When the LT3652 is powered by a solar panel, the input regulation loop is used to maintain the panel at peak output power. When operating at full sunlight charging the battery at highest set charging current, the LT3652 has an efficiency of around 80%[35]. The biggest drawback of using LT3652 is that

if one solar panel malfunctions, the IV curve's maximum operating point will be shifted left-ward while the constant operating voltage point remains the same. As a result, the solar panel will not be operating at maximum point and the charging efficiency is dramatically lowered.

Figure 45: IV Curve of a Solar Panel with Damaged Solar Cell[36]
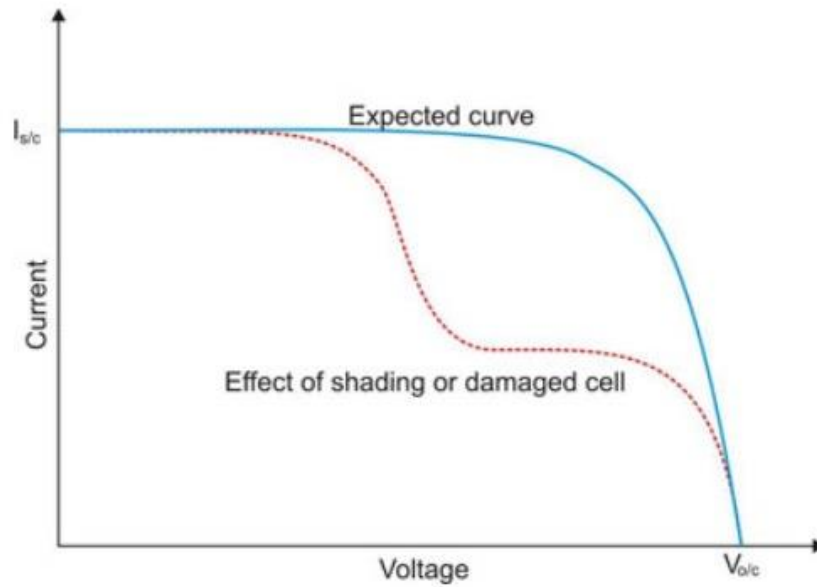
There are five LT3652 circuits on the Power Board, four of them are used for the four solar panel walls of the satellite, and the last one is used to expand the Power Board to 6U configuration in the case of LAICE. The resistor divider going into VIN_REG pin sets the MPPT voltage of the charger. And it should be configured based on the MPPT voltage point of each solar panel. Figure 46 demonstrates that the MPPT charger functioning and output the correct voltage, satisfying requirement two and three.
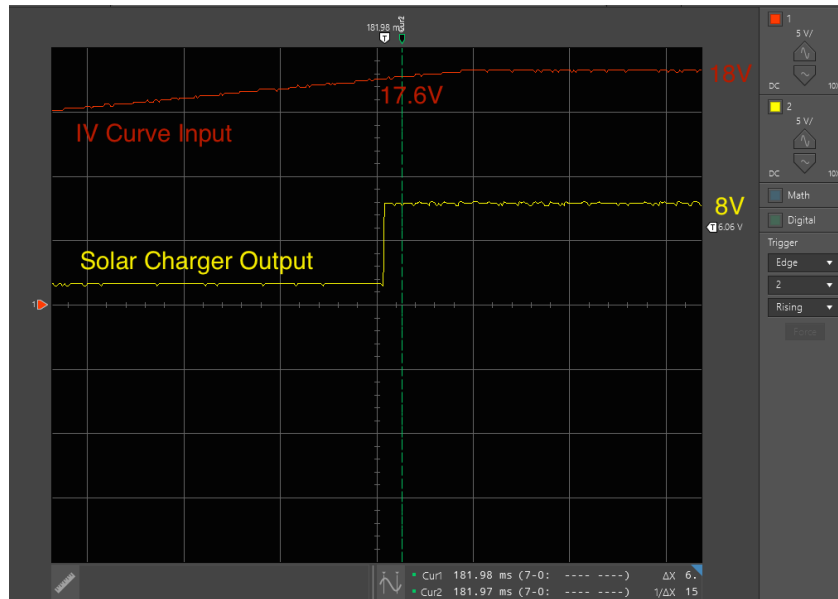
Figure 46: MPPT Charger Testing

Note that for LT3652 solar charger to turn on and charge the batteries, the input voltage must be higher than the battery charging voltage. For 1.5U configuration, there are only 3 cells on each panel, meaning the maximum output voltage is around 7V which is lower than the required input voltage. A constant operating voltage MPPT boost-converter was implemented on the Flex Cable to step up the output voltage with a gain of two in order to turn on the LT3652 charger.

5.5.5.3 Hot-Swap – TPS2420

The Power Board is required to control and monitor the power delivery to the rest of the subsystem. For IlliniSat-2, it is decided to use a family of ICs called Hot-swaps to fulfill the requirement. Hot Swapping is a technique that allows replacing or adding components without stopping or shutting down the host device. Usually a hot-swap has an integrated software-controlled switch with overcurrent protection. TPS2420 was chosen as the hot-swap for its wide range of operation voltage up to 20V, low MOSFET on resistance of 33 mOhm, hardware

configurable overcurrent fault protection, ability to restart the load after a fault condition, and analog output to the microcontroller to indicate the current consumption of the load[37].

Hot Swap #	Channel	fault current(A)	max current(A)	fault time(ms)	max load current(A)
1	3.3V_Flex_Cable	1	2	0.86	1
2	3.3V_C&DH	1.5	2.5	1.83	1.5
3	3.3V_Payload_1	1	2	0.86	1
4	3.3V_Payload_2	1	2	0.86	1
5	3.3V_Radio	1	2	0.86	1
6	3.3V_Payload_3	1	2	0.86	1
7	Battery_Pyro	3	4	0	3
8	Battery_Flex_Cable	2	3	3.89	2
9	Battery_C&DH	1	2	0.86	1
10	Battery_Payload_1	1.5	2.5	1.83	1.5
11	Battery_Payload_2	2	3	3.89	2
12	Battery_Radio	1.5	2.5	1.83	1.5
13	Battery_Payload_3	1	2	0.86	1
14	Battery_Payload_4	1.5	2.5	1.83	1.5

Table 13: Power Board Hot Swap Assignment

The Power Board consists of 14 hot-swaps controlling the power delivery of the battery and 3.3V line to C&DH, ADCS, Radio and Payloads subsystem. The overcurrent threshold level, the overcurrent maximum level, and the fault time for each channel are listed in Table. This satisfy requirement four, five and six.

TPS2420 has two modes to protect the load from an overcurrent situation. Hard Overload and normal overcurrent shutdown. The TPS2420 enters hard overload mode when the load current is 1.6 times the configured maximum voltage. In hard overload mode, TPS2420 will immediately disable the output without waiting for the fault timer to expire. After the shutdown, TPS2420 will re-enter start up mode and attempt to re-powerup the load device. If the hard overload failure continuous to occurs after the restart, the TPS2420 will enter a current limit mode with the fault timer enabled. The device will be shutoff if TPS2420 does not get off the current limit mode before the timer expires. The TPS2420 enters normal overcurrent mode when the load current exceeds

set fault current threshold and the countdown timer will start. If during the countdown, the current

exceeds the maximum fault current, the fault signal will be raised and the load device will be

shutdown. If the load device does not go below set threshold current before the timer expires,

TPS2420 will also shutoff power delivery to the device.
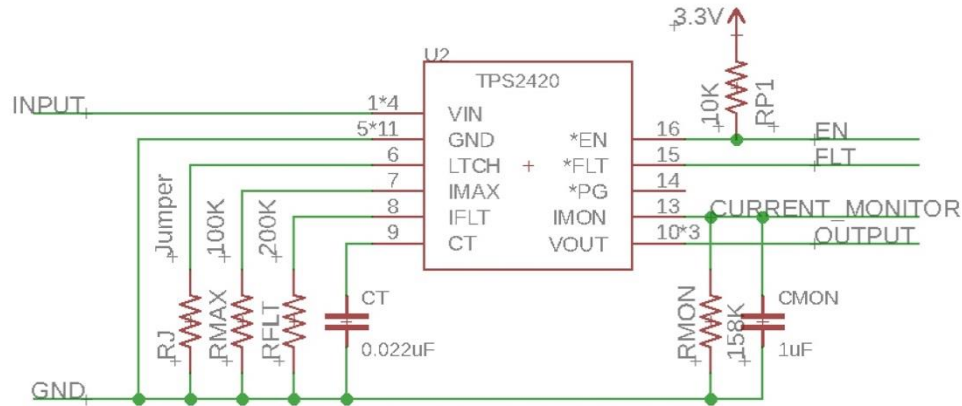
Figure 47: Hot-swap Schematic

TPS2420's maximum load current is set through RMAX and RFLT resistors. The resistor

setting is below in Table 14. The resistors are 0603 in size which are easily solder/de-solder-able

by hand. The user will also have the ability to enable hot-swap's ability to restart the load after a

fault condition. The restart is enabled through soldering a 0 Ohm resistor in RJ's spot.

I_{FAULT} (A)	R_{IFLT} (kΩ)	I_{IMAX} (A)	R_{IMAX} (kΩ)	C_{CT} (μF)	T_{FAULT} (ms)	T_{SD} (ms)	$I_{LOAD(max)}$ (A)	R_{IMON} (kΩ)
1	200	2	100	0.022	0.86	22	1	158
1.5	133	2.5	80.6	0.047	1.83	47	1.5	105
2	100	3	65.5	0.1	3.89	100	2	78.7
2.5	80.6	3.5	56.2	0.22	8.56	220	2.5	63.4
3	65.5	4	49.9	0.47	18.28	470	3	52.3
3.5	56.2	4.5	44.2	0.68	26.45	680	3.5	45.3
4	49.9	5	40.2	1	38.9	1000	4	39.2

Table 14: Hot-swap Configurations

TPS2420 can also measure the load current without the need of an external shunt resistor.

The full scale of the current is set by an external resistor RMON. The output voltage level from

the IMON pin indicates the load current level and is read by the 12 bit Analog-Digital-Converter pins on the MSP430. The current readings from the hot-swaps usually have high zero-current reading, and thus need to undergo calibration. Calibration involves running PB_Cur_Char software. The software sweep through the current from 0A to maximum rated amperage with 50 step points, and returns the raw current read from the Power Board. Figure 48 shows a characterization of a Hot-Swap channel with 2A maximum load current. We can see that the Hot-Swap is able to deliver the rated current to the load and disconnect from the load when the current is above 2A. This satisfies requirement eight.
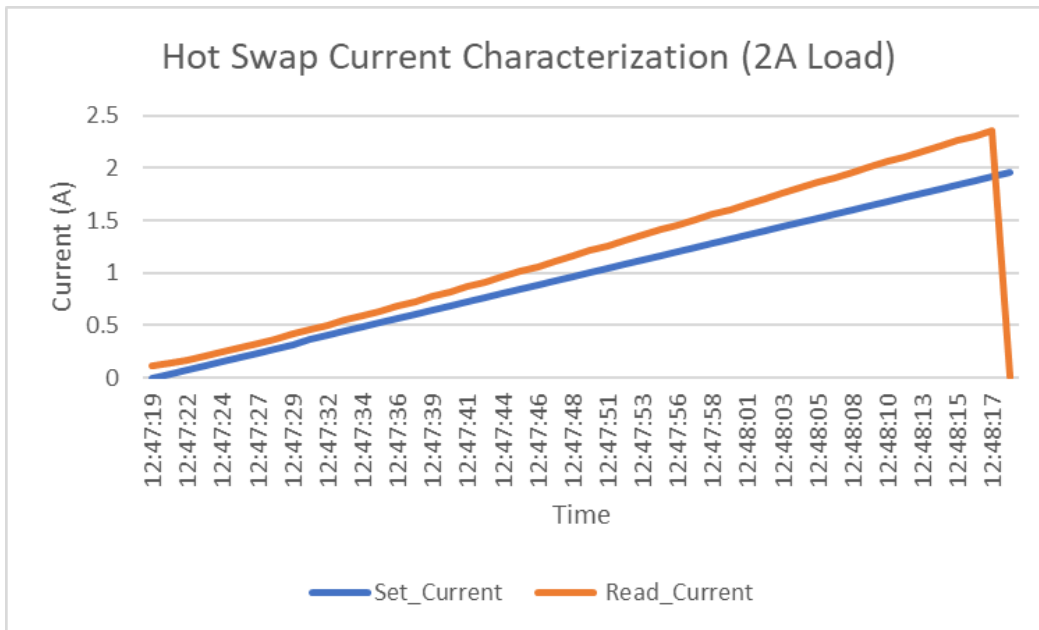
Figure 48: Hot-Swap Current Characterization (2A)

5.5.5.4 Kill Switch and RBF
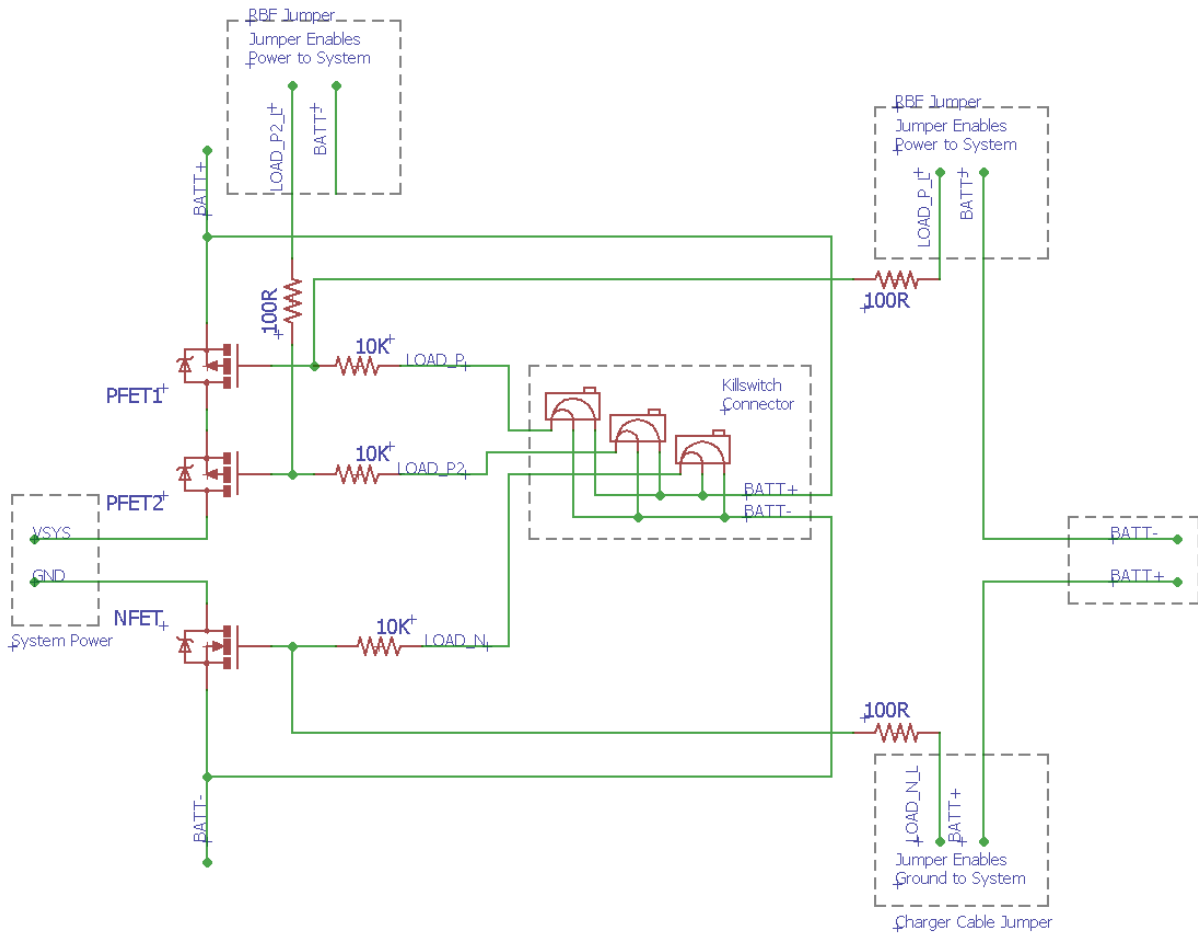
Figure 49: Power Board Kill Switch and RBF system schematic

To satisfy requirement seven, the IlliniSat-2 bus has two sets of mechanical switches to cut off power from the battery to the rest of the system: Remove Before Flight Tag and Kill Switch. RBF is an external tag that plugs into the spacecraft's RBF connector to shutoff the spacecraft and enable charging the battery. The Kill Switch is a set of mechanical switches integrated into the satellite so shut off power to the system and disable charging. The RBF has higher priority over the Kill Switch and will override the Kill Switch if both RBF and Kill Switch are engaged.

The schematic for the Kill Switch and RBF is shown in Figure 49. The Kill Switch and RBF share three MOSFETs among them, two P-MOSFETs on the high side of the battery to control connection between Battery plus and system voltage, and one N-MOSFET on the low side of the battery to control connection between Battery minus and system ground. The MOSFETs are chosen to have low on resistance. The PFETs have 4.5mOhm and NFET has 2.5mOhm resistance.

The priority between Kill Switch and BRF is set through the gate current. MOSFETs have miller effects which introduces capacitance to the gate of a MOSFET. As a result, higher current going into the gate means higher time to switch on/off the MOSFET. RBF's control signal line has a lower serial resistance than Kill Switch's, which gives the RBF control signal higher current, and thus higher priority.

The RBF setup allows the satellite to be charged even when the RBF is plugged into the power board which satisfies requirement eight. The RBF will not connect LOAD_N_L to BATT-, but instead connect to BATT+ to enable the NFET connecting BATT- to satellite ground. This configuration allows charging current to flow from BATT+ to satellite ground to charge the battery, while still disconnecting satellite VSYS from BATT+.

5.5.5.5 Thermal Knife

The thermal knife system on the Power Board is in charge of releasing any folded components that need to be unfolded and deployed, most importantly the antenna. To fit the satellite into the P-Pod from the launcher, the antenna needs to be folded down around the satellite and only to be released through the thermal knife when the satellite is released from the P-Pod. The thermal knife operates by passing 2A current through a low resistance nichrome wire, heating up the wire to around 200C to melt the dyneema wire that holds down the antenna. The thermal

knife consists of through-hole ring test points to mechanically hold the nichrome wire, and serial resistors to limit the current to 2A.

When the thermal knife is turned on to release the antenna, the spacecraft should still be at its initial stage with fully charged batteries. The voltage going into the nichrome wire should be about 8.4V, indicating a full battery. The serial resistance of the thermal knife line is 4 Ohm, which limits the current to 2.1A. Note that the resistors in series will have 2.1A passing through them, which is around 8.8W of power dissipating through each one of them. Choosing resistors with high power rating is crucial for the correct release of antenna. Otherwise, the resistors will be burnt out before the nichrome wire is hot enough to melt the dyneema wire. The current design contains two 25W 2Ohm power resistor in series.

The mechanical challenge with the thermal knife is the thickness of the assembled PCB. The thermal knife is attached to the outside of the solar panel plate and the assembled thermal knife PCB should have maximum thickness of 5mm in order for the satellite to be physically fit into the release POD. As a result, the PCB are manufactured to have 1mm thickness with the resistors' height being 2mm and the test point ring height 2.54mm to have the final assembly to be around 4mm.

The thermal knife subsystem's input power is controlled by a dedicated thermal knife hot-swap that is set to have maximum load current of 3A. If all the thermal knives are fired at the same time, the load current will 8.4A, which will trip the hot-swap as well as the battery protection. As a result, the thermal knife will need to be fired sequentially in order to prevent tripping the hot-swap. The driver circuit for the thermal knife firing consists of P-MOSFET and low-side P-MOSFET gate driver for each thermal knife and the control signal is generated by the

microcontroller. Figure 50 below shows the schematic of one of the PYRO channel driver. This design satisfies requirement nine.
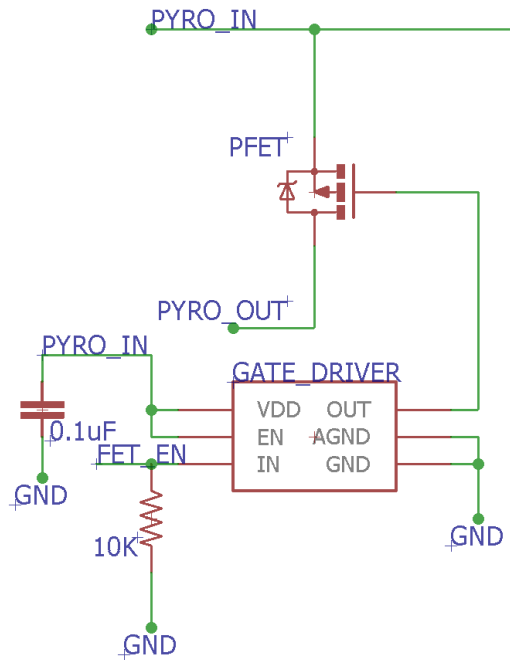
Figure 50: Thermal Knife Driver Schematic

5.5.5.6 3.3V Regulator

The Power Board carries 3.3V switching step-down regulators to supply 3.3V to the digital power lines in the satellite. The 3.3V regulator chosen is Texas Instrument's TPS62111[38]. TPS62111 is capable of regulating battery voltage down to 3.3V at maximum 95% efficiency and supply up to 1.5A on the 3.3V line. The regulator also has the ability to shut itself off when its temperature reaches above 145 Celsius, making it more resistive towards fault situation. Figure 51 shows the output of the 3.3V regulator when the regulator is enabled and the input is 7.4V.
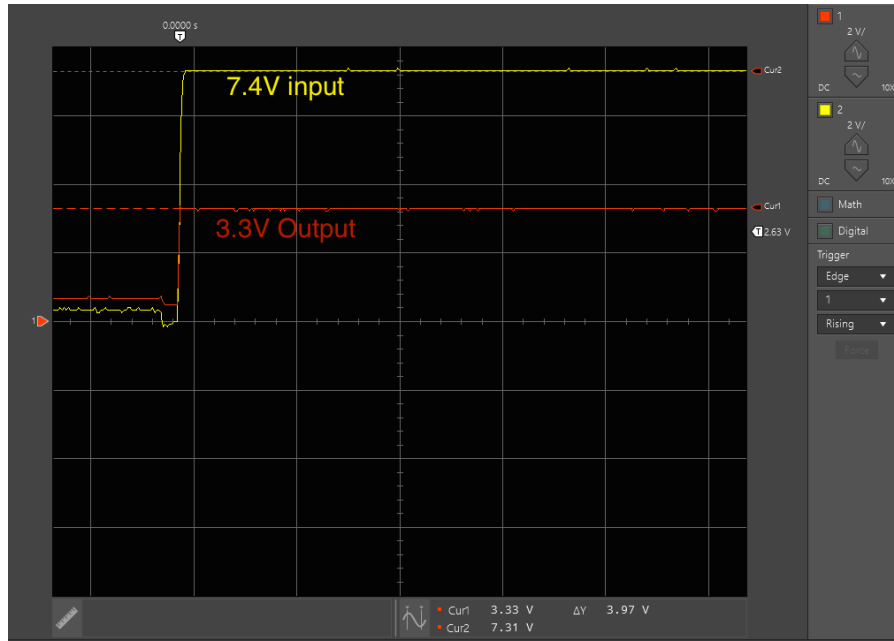
Figure 51: 3V3 Regulator Output

For redundancy purposes, two switching step-down regulators are implemented on the board. The enable is controlled by the MSP430 microcontroller. The MSP430 microcontroller will monitor the "Power Good" pin output on the regulator. If the output voltage is below 98.4% of 3.3V output, the "Power Good" pin will rise to a logic low indicating an issue with the power supply. The microcontroller will catch the issue, turn the faulty regulator off and turn the backup regulator on. This design satisfies requirement ten.

5.5.6 Power Board Software

5.5.6.1 Power Board AIT, and early commissioning concept of operations

The Power Board system remains on throughout the lifetime of the spacecraft. Before the satellite is delivered, a Remove Before Flight tag was plugged into the Power Board to override the Kill Switch and turn off everything on the satellite. When the satellite is assembled into the deployment P-POD for delivery, both the RBF and kill switches are engaged. Before the satellite launch, the RBF tag is removed, but the physical Kill Switch is still pressed by the P-POD to

disable the satellite. After the satellite is released out of the deployment P-POD in space, the kill switch will be depressed and the satellite's Power Board will come online. The Power Board will go through a 45-minute countdown, then it will check the health of the battery pack and turn on the C&DH if the Power Board deems that the battery is healthy. Afterwards, the Power Board will answer commands from C&DH following Table 15. Every minute the Power Board refreshes the battery percentage to determine the current power state and act on it, as well as monitor the current consumption of the subsystems to see if any subsystem is experiencing faulty situation.

Command	Read/Write	Start Byte	Command Address	Data Byte	Return Byte	Function
WDT	W		"CNDH"			Send to power board every 10s to keep C&DH Powered on
PWR_BRD_CHK	R	0xf0	0x0001	0	5 (0x494d474f44)	General Check
HS_EN	W	0xf0	0x0002	2	5 (0x48535f454e)	Enable Hotswaps
HS_DIS	W	0xf0	0x0003	2	5 (0x48535f4449)	Disable Hotswaps
BATT_V_STAT	R	0xf0	0x0005	0	8	Battery Voltage Status
BATT_T_STAT	R	0xf0	0x0006	0	8	Battery Temperature Status
BATT_CUR_READ	R	0xf0	0x0007	0	2	Battery Current Status
BUS_VOL_READ	R	0xf0	0x0008	0	2	Battery Pack Bus Voltage
BATT_HTR_ON	W	0xf0	0x0009	1	5 (0x48545f4f4e)	Turn on Battery Heaters
BATT_HTR_OFF	W	0xf0	0x000A	1	5 (0x48545f4f46)	Turn off Battery Heaters
HS_CUR_STAT	R	0xf0	0x000B	0	28	HotSwap Current Status
HS_FLT_STAT	R	0xf0	0x000C	0	2	HotSwap Fault Status
SC_DIS	W	0xf0	0x000D	1	5 (0x53435f4449)	Solar Charger Disable
SC_EN	W	0xf0	0x000E	1	5 (0x53435f454e)	Solar Charger Enable
SC_STA	R	0xf0	0x000F	0	1	Solar Charger Status
ADS1000_READ	R	0xf0	0x0010	0	3	Battery Voltage from ADS1000
BUCK_STAT	R	0xf0	0x0011	0	1	Buck Regulator Status
TF_FIRE	W	0xf0	0x0012	0	5 (0x544b464c59)	Sequentially Fire all 5 thermal knives

Table 15: Power Board Commands

5.5.6.2 Software Implementation

The Power Board software contains two major sections: peripheral drivers and device drivers. The peripheral drivers contain implementation for internal ADC, flash, I2C, RAM, RTC, SPI, timer and UART peripherals. The device drivers contain implementation of the external devices that are attached to MSP430. Table 16 specifies devices and their corresponding peripherals.

Device	IC	Functionality	Peripheral
Battery Pack	AD7997	Analog to Digital	I2C
	INA226	Current Sensing	
	TCA6414A	Port Expansion	
Buck Regulator	TPS6211	3.3V regulation	GPIO
CNDH	N/A	N/A	UART
Hot Swap	TPS2420	Load Switch, overcurrent protection, current read	GPIO
External NOR Flash	IS25LQ080	8MB Storage	SPI
Port Expander	PCF8574	Port Expansion	I2C
Thermal Knife	SISS23DN	P-MOSFET	GPIO
	MCP14A0151	Gate Driver	
Solar Charger	LT3652	Battery Charging	GPIO

Table 16: Power Board Device Peripheral Summary
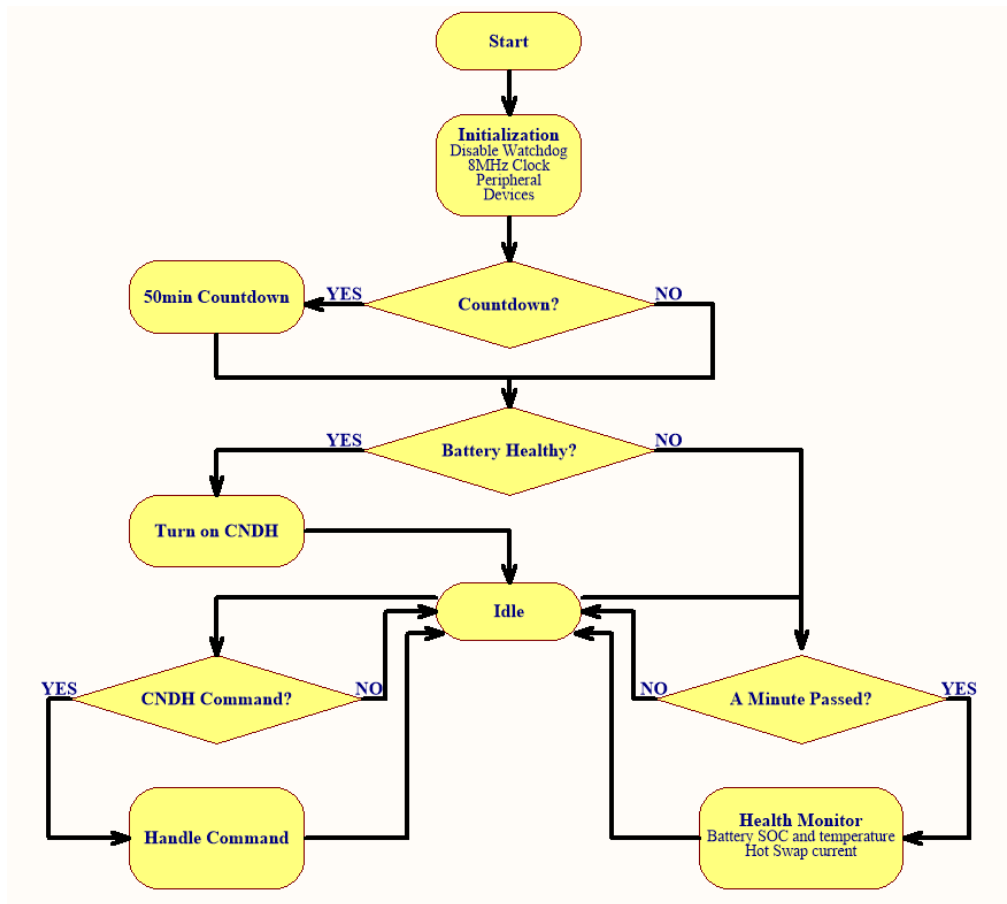
Figure 52: Power Board Software Flow Chart

Figure 52 outlines a flow chart for the operation of the Power Board software. Upon boot, the Power Board will first initialize its internal RC clock generate to generate 8MHz clock signal. Once the oscillator is initialized, the Power Board will go through a peripheral initialization routine to initialize the ADC, I2C Master communication bus, custom-designed file system, Timer A, Timer B, and Real Time Clock. Then the Power Board will initialize the associated hardware by turning off all the hot-swaps, turning on all the solar charger, turning off both the 3.3V buck regulators, and initialize the communication between the Power Board and C&DH. Once the initialization is complete, the Power Board will go through the boot sequence.

During the boot sequence routine, the Power Board checks a specific flash memory location at 0x1C200 to see if it is 0xFF. When reprogramming MSP430 through Code Composer Studio, all the un-used flash will be erased to have the initial value 0xFF. By checking for the initial value of a specific memory location, the software will determine whether it is the first time booting of MSP430. Upon determining the first boot of MSP430, the software will issue a 50min countdown through the RTC timer. After the 50min initial countdown, the Power Board will update the memory location 0x1C200 to 0xAA to disable the 50min timer in future boots. Any interruption of the fifty-minute countdown will not result in 0x1C200 being updated to 0xAA. This software setup satisfies the first requirement on software.

After the initial countdown, the Power Board will execute its battery monitoring routine. The Power Board reads from the analog-to-digital converter to gather raw voltage data of the individual battery cell and convert the raw binary data into battery percentages of each cell. If the battery percentage is above 50 percent, the battery is deemed to be in a healthy state and C&DH will be enabled.

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If the battery is in a good state and the C&DH is powered on. The Power Board will sit in idle waiting for C&DH's commands through the UART channel at 115200 bit-per-second baud rate. The power board responds to commands in 1.25 to 20ms. Figure 53 is a logic analyzer capture of the communication between Power Board and C&DH. C&DH sends the command "0xF0 0x00 0x01", in 1.25ms, power board responds with "0x44 0x4F 0x47 0x4D 0x49" indicating its presence. This validates software requirement six.

Figure 53: Power Board Responds to C&DH commands

To satisfy requirement four, the Power Board checks the batteries' state of charge and temperature every minute to make sure that the battery pack is healthy. The software is the same one used to generate battery reading in section 5.3.7. Following Table 17: IlliniSat-2 Power States, when the battery percentage is between 30 and 50 percent, the battery is deemed to be in low state where the C&DH will only be enabled if the satellite is charging though the solar panel; when the battery percentage is below 30 percent, the battery is deemed to be in emergency state where all the subsystems' hot-swaps will be shutoff including C&DH, the Power Board will go into a low power mode, and check the battery percentage once every minute to see if the satellite is out of the battery emergency state.

Battery Percentage	State	Action
Above 50%	Healthy	Power on CNDH, allow any instrument to operate.
30% to 50%	Low	Only power on CNDH when the solar panel is charging. Disable power to all the payloads
below 30%	Emergency	Power down everything on the satellite including CNDH.

Table 17: IlliniSat-2 Power States

The Power Board software also functions as a watchdog timer for the C&DH. After the first communication between C&DH and Power Board, Power Board will enable its TimerA module and issue a 16s countdown. If no "CNDH" message is received during the 16s, power board will reboot C&DH. If "CNDH" message is received, the 16s timer will be set. Figure 54 shows the watchdog interaction between C&DH and Power Board. C&DH sends Power Board the command "CNDH" every 10 seconds to prevent Power Board from rebooting C&DH. When C&DH stops sending the command, Power Board toggles the line and reboots C&DH. This implementation satisfies requirement seven.
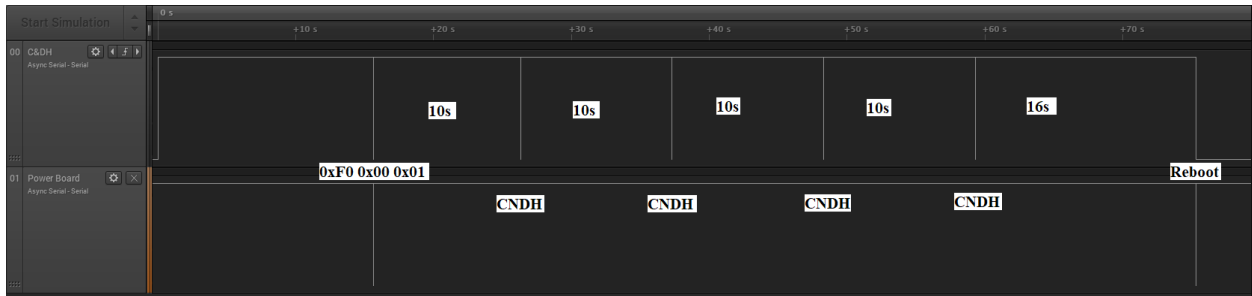
Figure 54: Power Board and C&DH Watchdog interaction:

5.5.7 Remaining Issues and Next Revision

So far, only one issue was noticed for the Power Board Revision C. The 3.3V is supplied to the VUSB pin not VBUS pin for the USB module. As a result, the USB module is not powered on for its extended GPIO function. The current fix is applying a dot of solder to short the VUSB and VBUS pins.

Another fix that was implemented on the Power Board was regarding the burn out issue with the C&DH mentioned above. A wire is guided out from the backbone mating connector to the debug port to supply 3.3V to the RS232 transceivers on the EGSE.

For the next revision of Power Board, it is not recommended to use MSP430 family of microcontrollers as the central processor. But instead use Texas Instrument Hercules Series of microcontrollers. Hercules Series of microcontrollers are designed to operate in safety critical applications. Inside of a Hercules microcontroller, two CPUs are running simultaneously with a lock step between them. Every 2 clock cycles, the CPUs will check their results to ensure they are not malfunctioning. Using Hercules instead of MSP430 for a system that will never be powered off is a safer method.

For the next revision of Power Board, the designer should consider implementing a perturb observe buck boost MPPT charging circuit. As discussed above, perturb and observe is the most efficient way to transfer power from solar panel to battery. The designer does not necessarily need to put 5 of such circuits onto the Power Board because perturb and observe charging circuits are usually much bigger than constant operating voltage charging circuits. The designer can simply put two P&O circuits on the Power Board, with one being the actual charger and the other being the backup charger. The designer needs to figure out which solar panel is charging based on the

UV light sensor's output data on the Flex Cable and electrically connect the sun facing solar panel to the P&O charger.

5.5.8   Summary of Contribution

The Power Board design is capable of controlling the distribution of power to the rest of the subsystems and three payloads through the use of Hot-Swap controller. The Power Board is able to convert the solar panel to charge the battery through constant operating voltage Maximum Power Point Tracking solar charger. The Power Board contains a kill switch and RBF interface to disconnect the battery from the satellite for launch. The Power Board holds five thermal knife firing circuitries to satisfy the need to deploy either antennas or solar panels. The Power Board includes a microcontroller that runs Version 1 of the Power Board Software. The software communicates with C&DH to execute command to control the Hot-Swaps or gathering health monitoring data. The software also determines and enters different satellite power states based on the battery health. When the C&DH is powered on, the software acts like an external watchdog to prevent C&DH from hanging. The Power Board's software and hardware, together, meet all the requirements stated in section 5.4.2.

CHAPTER 6: DESIGN AND MANUFACTURING LESSON LEARNED

6.1 Introduction

This chapter will discuss the software used in: the design process, component sourcing for spacecraft Printed Circuit Boards, PCB manufacturers for prototyping and flight, and the process to professionally manufacture a PCB.

6.2 PCB Design Software

Several PCB design software packages were used during the designing phase of IlliniSat-2 bus and paylaod hardware. Each software has their pros and cons, and their usage was determined based on the respective student designer's expertise, complexity of the PCB, and the need for specific specialty design tools. This section will go over the four PCB design software that were used during IlliniSat-2 development.

6.2.1 OrCAD

OrCAD was used to design Revision one and two of the C&DH PCB. OrCAD is a very powerful software and an industrial standard, used at companies such as Apple, Intel and IBM[39]. It is mainly used for high-speed PCB design, due to its ability to perform full circuit simulation and signal integrity simulation with the drop in PSpice[3] model feature. OrCAD has a steep learning curve because it was targeted towards high density, high speed, mixed signal PCB design. Most of the PCBs for IlliniSat-2 are neither high-speed, nor high density nor mixed signal, with the notable exception of the C&DH support board. OrCAD also split every one of its features into

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[3] PSpice is a SPICE circuit simulator application for simulation and verification of analog and mixed-signal circuits. PSpice is an acronym for Personal Simulation Program with Integrated Circuit Emphasis.

standalone software. The designer has to toggle between multiple software even when doing a simple PCB design. As a result, OrCAD stopped being used for hardware development ever since the departure of the designer who is familiar with it.

6.2.2 Eagle CAD

Eagle CAD was used for the majority of the PCB designs for IlliniSat-2 bus. The Power Board, battery pack, C&DH, 3U and 6U Flex Cables, Torque Coil, Magnetometer and radio mounting board were all designed in Eagle CAD.

Eagle CAD is one of the most popular CAD software among amateurs due to its relatively complete schematic and PCB design interface. Eagle CAD software is low cost, easy to use, and have support from various forums and online communities[40]. On top of that, Eagle CAD was the software of choice for the ECE department, and it was particularly used by the ECE senior design class. The popularity of Eagle CAD within the school means that the software license is already available for use, and many students are trained to use Eagle CAD so the learning curve to apply it to spacecraft design is not steep.

Designing PCBs with Eagle CAD has its short comings. Thus far, four major flaws were noticed throughout author's usage of Eagle CAD. The first flaw is the lack of functionality to facilitate high speed PCB routing, the issue was glaringly noticed during the routing of the high-speed traces[4] for C&DH. Further, unlike Altium and KiCad, Eagle CAD lacks 3D views and 3D PCB export which makes board-to-board mechanical fit checking problematic. The lack of such

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[4] High-speed traces are traces with signal speed of over 50MHz. In C&DH's case, the clock, command and data traces are all rated to be 50MHz. When routing high speed single-ended traces, the trace impedance need to be 50 Ohm, and the trace lengths of a signal group need to be matched within 20mil.

functionality caused misplacement of backbone connector between Power Board and C&DH, as well as difficulties in designing the Flex Cables that required fine mechanical dimension. The third flaw is that Eagle does not provide a more user-friendly interface for PCB routing; the complicated process to switch between layers makes any design or redesign with more than four layers of copper an unpleasant experience, like in the case of the Power Board. The last flaw with Eagle is that it does not have a complete design rule check. This means that certain types of design errors can pass the design rule inspection, allowing flawed or un-manufacturable designs to be released to production companies. This led to problems on multiple occasions. For instance, on one of the Torque Coils' revisions, a via shorting the coil trace passed the design rule check, yet the short meant the Torque Coils of that batch were unusable as delivered. Determining the source of the problem and a fix wasted a lot of debugging time once the PCB was received. Another example relates to one of the Power Board's revisions. In that case, several unterminated wires passed the design rule check and caused electromagnetic interference (EMI) issues with the Power Board.

6.2.3   Altium

Like OrCAD, Altium is also a powerful PCB design software and an industrial standard. For example, Altium is the main software used for SpaceX's PCB designs[41]. Altium is used for designs of the C&DH PCB high speed traces, the radio switching board between Lithium Radio and Cadet Radio needed by the LAICE mission, the 1.5U Flex Cable for CubeSail, and latest revision of Battery Pack.

Altium packs schematic and PCB design into a single software interface. Altium provides an intuitive shortcut system that greatly accelerates the design and learning process. It also provides the designer with a cleaner PCB coloring and design interface to ease the design process of PCBs with more than 4 layers. The biggest highlight for Altium Designer is its superior 3D

viewer for the PCB. Altium can import and export 3D models in step format, which means the mechanical fit check can be done during the design phase, unlike with the other software packages. This feature allows much better systems-level design, and ensures that the PCBs are guaranteed not to interfere with other spacecraft parts. Further, Altium also supports bending of flexible PCBs which is essential for the design of the solar panel Flex Cables.

There are two downsides of using Altium. First downside is that sometimes the software crashes and a lot of design progresses are lost as a result. The issue was occurring a lot during Altium 17 and was improved in Altium 18. The second downside is the pricing of the software. Currently, the school doesn't have Altium licenses. A full life time license is at about $8000 with one-year software update subscription, each year $2000 will need to be paid to subscribe to software updates.

6.2.4 KiCad

KiCad is a complete open source, and free PCB design software. It is maintained by volunteers and paid contributors, and it recently got supported by the engineering team of CERN[42]. KiCad was used to design the entire SASA payload, as well as multiple interconnect circuits for the CAPSat and SASSI^2 payloads. The choice to use KiCad for those designs was made because of hardware engineers' expertise on the software.

KiCad mimics most functionalities of Altium in terms of 3D viewing, shortcut assignment and routing modes, while being completely free. The remaining issue with KiCad is its complicated library linking system, and an incomplete design rule check system which misses PCB errors from time to time. The use of KiCad within the Illinisat-2 family of satellites is relatively new, and further usage, testing and experimentation is necessary before any recommendation to adopt it more generally can be made.

6.3   Embedded Software - Energia vs Code Composer Studio

For MSP430 family microcontroller, the designer can have the option to use Code Composer Studio or Energia to develop the software. Originally, the implementation strategy for the software was to implement the software on top of the Energia framework. Energia framework mimics the popular Arduino framework that runs in Atmel family of microcontrollers. Energia contains all the necessary peripheral drivers and libraries to simplify the functions calls to greatly accelerate the design process. If Energia was used, the developers don't have to spend a lot of time digging into the microcontroller datasheet to learn about different functionalities of each register. The downside of Energia is the reliability of the software's framework. The Power Board's microcontroller is required to always be powered on after the satellite's lifecycle begins. If the software goes through an error situation because of bugs in the driver, the error could potentially latch the microcontroller, freeze the communication between Power Board and C&DH resulting in no control over the satellite's power system. The entire satellite could potentially be locked up and the mission will be over. With the presence of the hardware watchdog, the error could potentially cause repeated reboot of the entire satellite at a rapid rate, which also means the failure of the mission. As a result, the developer for the embedded software must have a thorough understanding of the implementation of the embedded peripheral drivers, as well as a complete debugging interface to analyze the software's reliability to catch any potential errors within the system. Energia and its corresponding IDE is more for hobbyist designers. It cannot guarantee the capability to ensure the prolonged operation of the power system. Energia also lacks a well put-through debugging interface. Traditional embedded software debuggers involve putting breakpoints and pausing the program at specific instructions to analyze the internal registers, expressions and memories of the microcontroller. The debugging in Energia IDE can only be done

through printf() function calls to print out variables through UART. As a result, Energia framework was deemed unable to fulfill the requirements. A lower level software implementation strategy based on Code Composer Studio was chosen.

Code Composer Studio is the integrated development environment to develop software application for the Texas Instrument family of microcontrollers and microprocessors. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features[43]. The user can put the software into debug mode, insert breakpoint into either certain location in the software or specific faulty scenarios like stack overflow. The debug interface will provide information all the internal registers, user declared variables, and most importantly, the memory of the entire internal of the microcontroller. The user can also view the disassembly of the written C/C++ software. The usage of Code Composer Studio can help the programmer trace and fix software bugs more efficiently.

6.4   Component Selection

Selection of components is important to ensure the proper operation of electrical component over the mission life time. Well selected components can ensure around many years of continuous operations of the satellite in the space environment. From a consumer level distributor, the designer is limited to two choices of component categories: general purpose grade and automotive grade components. The difference between general purpose and automotive component is the amount of testing that goes into qualifying the component. Automotive grade components go through a couple of JEDEC based qualification that involved high accelerated stress testing[44]. These tests simulate the component operating in high temperature and humidity, and further with simulated accelerated corrosive environment through input bias voltage. Taking

the example of a capacitor: if the capacitor is selected to be a general-purpose grade capacitor, it might be prone to internal cracking due to physical stress, parameter change through solder heat, etc. If the capacitor is AEC-Q200 standard qualified for automotive components, it will ensure a wide temperature operating range at -40 ~ 150C, moisture resistance at 80% humidity, long operating life, better resistance to solvents, mechanical shock, vibration and solder heat. If applicable[45]. AEC-Q2000 qualified automotive components are always preferred over general-purpose components, especially when the electrical component is passive components such as resistors/capacitors/inductors/diodes. Below is a discussion to help future designer select capacitors and resistors since they are most commonly used in spacecraft electronic design.

For capacitors, the preferred manufacturers are the name-brand Murata, Kemet, Samsung and TDK, since all the satellite capacitors have been sourced from them and no issues were noticed. The stocking for the capacitors fluctuates a lot depending on current market demand, so be prepared to have the capacitor selected obsolete even a week after generation of the Bill of Material. Due to the effect of capacitors losing capacitance in a half-life fashion, the capacitors selected should have their voltage rated twice the maximum operating voltage. It is wise to always have common value capacitors in stock, or to perform "lifetime[5]" purchases of commonly used capacitors that have been proven to meet Spacecraft needs. The tolerance of the capacitor should be 10% to 20%. The temperature rating is preferred to be X7R that ensures operation at -55C to 125C, but any rating above X5R is acceptable.

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[5] A "lifetime" purchase would be a preemptive purchase of extra capacitors expected to meet the manufacturing need for the foreseeable design life of the part, based on expected usage on upcoming missions and the part improvement/redesign cycle.

Electrolytic capacitors are general avoided for space applications. Electrolytic capacitors may undergo parameter changes from either ionizing or burst radiation, depending on dosage. Aluminum electrolytic capacitors can outgas water and organic vapors. The dielectric also can be weakened, and DC leakage may rise as a result of bombardment[46]. Ceramic capacitors should always be the first choice when selecting capacitors. The designer can also select glass film or tantalum capacitors for spacecraft with caution for polarity. A capacitor's lost capacitance can be reset through oven bake-out, the bake-out realigns internal crystal structures of a capacitor, and should be performed before spacecraft delivery to ensure the capacitors can operate with a fresh start[47].

For resistors, the preferred manufacturers are the name-brand Panasonic, Samsung, Stackpole, Vishay Dale and Yageo, since all the satellite resistors have been sourced from them and no issues were noticed. The available stock from distributors for resistors fluctuates but not as much when compared with capacitors. Resistors usually don't suffer from half-life effects like capacitors. When selecting resistors, 1% tolerance is desired, 5% is acceptable. The only big thing to be cautious about is the resistors' power rating. A resistor operating above its power rating can lead to resistors smoking which is not desired for spacecraft.

6.5 Tin Whiskering

For spacecraft operating in a space environment, tin whisker from the tin solder can cause potential damage to the electrical circuit. Tin whiskers are electrically conductive, crystalline structures of tin that sometimes grow from surfaces where tin (especially electroplated tin) is used as a final finish. Tin whiskers were observed to grow to several millimeters and in some extreme cases, exceed 10mm. Tin whiskers can cause shorting of electrical circuits, causing a high surge of current flowing through the whisker, creating metal vapor that cascades out to short more

circuits. To prevent Tin Whiskers from happening, NASA suggested the use of leaded solder as a finish, and conformal coating the printed circuit board[48]. Tin whiskers are dangerous in the case of C&DH's MitySom-335x daughter card. First, the daughter card is an off-the-shelf system module that is European ROHS compliant, meaning that the soldering process of the SOM card is lead free. Second, the BGA pitch for the AM3358 chip is 0.5mm, there is such a small gap between the BGA balls, that even a small growth of Tin whiskers from one pin can easily make it to another pin. As a result, special daughter cards are offered by Critical Link to add lead into the assembly process. This means re-balling the BGA with tin-lead balls, and soldering the entire circuitry with leaded solder paste. The daughter cards also goes through ultrasonic conformal parylene coating to apply coat in between BGA balls.

6.6   PCB Manufacturers for Prototyping and Flight

Prototype PCBs before professionally manufacturing them is a good and cheap way to catch potential errors. Prototyped PCBs don't go through thorough quoting processes, rigorous testing, nor certifications, which dramatically lower the cost. During the prototyping phase of the spacecraft, cheap PCB prototyping companies were used to manufacture PCBs. OSH Park, PCBWay, Golden Phoenix PCB, JLC Circuit, 4PCB, Bay Area PCB were all used at one point or another to manufacture prototype PCBs. Among those companies, PCBWay, Golden Phoenix PCB and JLC Circuit are based in China, OSH Park, 4PCB and Bay Area PCB are based in United State. Producing PCB in China reduces the production speed and cost dramatically while maintaining the same PCB quality as those produced in America. For example, PCBWay offers two-layer PCB that are less than 15 square inches at $5, the PCB can be delivered within a week. OSH Park offers two-layer PCB manufacturing at $5 per square inch, and the delivery is usually two weeks unless an extra $200 is paid. The cost difference and manufacture speed increase as the layer counts goes

up, making Chinese PCB manufacturers more attractive for satellite PCB prototyping. The big downside with using Chinese PCB manufacturers is that China is under ITAR and EAR regulation. Certain PCBs that fall into such category is not allowed to be made in China. If the components are shipped from American suppliers to China for assembly, they have to go through custom checks which can slow down the assembly process.

All the spacecraft hardware was later professionally manufactured and assembled in the United States once they were verified to be functionally flight ready. So far, Advanced Circuits and Sierra were used to produce rigid flight PCBs. FlexPCB was used to produce all the Flex Cables. Issues were noticed with all three companies. With Sierra Circuit being the more reliable company, Sierra Circuit has a great issue tracking system to catch any potential design or assembly errors. However, Sierra Circuits tends not to go through quoting files thoroughly which caused unnoticed quoting mistakes. For example, the Torque Coils and Battery Pack were quoted to be manufactured with leaded solder. Sierra missed that specification in the quote file. They had to confirm with one of the engineers if the boards are Restriction of Hazardous Substances (RoHS) compliant[49] in a section of a relatively long email. The engineer didn't catch that question and answer. Sierra manufactured the boards to be unleaded as a result and caused a lot of troubles. But as long as the engineer is careful and thoroughly analyzes the quotes, such issues can be avoided.

To professionally manufacture and assemble a PCB, the designer has to go through three steps: generating the manufacture and assembly files, getting the quote, and placing the order. The designer needs to generate all the necessary Gerbers to manufacture the boards; solder paste files, component placement file and bill of material files should be generated to assemble the boards. The designer also need to attach a ReadMe file that contains the circuit's specificationand order info. An example of the ReadMe file is shown below in

Figure 55. The files should be zipped together and upload to the manufacturer's website. Once the

quote is generated, the designer needs to go through the quote carefully to spot mistakes. If the

price is acceptable, the order will be placed through the business office. Usually the manufacturer

will give an order tracking number to track the manufacture status of the order.

```
◀▶     ReadMe.txt          ×
 1   Files
 2   Manufacture:
 3   *.GTO — Top Overlay
 4   *.GTS — Top Solder
 5   *.GTL — L1 (Positive)
 6   *.G1 — L2 (Positive)
 7   *.G2 — L3 (Positive)
 8   *.GBL — L4 (Positive)
 9   *.GBS — Bottom Solder
10   *.GBO — Bottom Overlay
11   *.TXT — NC Drill
12   *.GM1 — Board Outline (Including Cutout)
13
14   Assembly:
15   *.GTP — Top Paste
16   *.GBP — Bottom Paste
17   *.GM11 — Bottom Center Location
18   *.GM12 — Top Center Location
19   *.GM15 — Top Component Placement
20   *.GM16 — Bottom Component Placement
21
22   Board info:
23   Dimension — 86 x 84mm
24   Layer Count — 4 layers
25   PCB Type — FR4
26   Min Trace/Spacing — 6/6mil
27   Min Hole Size — 0.3mm
28   Solder Mask — Green
29   Silkscreen — White
30   Surface Finish — Immersion gold
31   Board Cutout — GM1 Layer, the 8 cutouts location      <---- Important
32   Assembly material — Leaded                            <---- Important
33   Assembly Component — Manufacture Sourcing.            <---- Important
34   Assembly BOM — Attached
35   Assembly CPL — Attached
36
37   Order info:
38   Manufacture Quantity — 8
39   Assembly Quantity — 5
40   Manufacture Leadtime — quote 3, 4 and 5 days
41   Assembly Leadtime — quote 3, 4 and 5 days
```

Figure 55: Example ReadMe.txt file for PCB quoting

There are several parameters to stress when producing PCBs for spacecraft flight which

should be listed in the ReadMe file. Any non-circular internal cutout of the circuit needs to have

its own Gerber file and be specified in the ReadMe. The surface finishing is preferably a gold

finish with the process of Eletroless Nickle Immersion Gold (ENIG) to offer longer shelf life, even

soldering surfaces, and through-hole component's structural rigidity[50]. The soldering process

has to be leaded to prevent tin-whiskering. The PCB is preferred to be at least Class 2 tested. A professionally designed PCB needs to meet either Class 1, 2, 3 or 3/A standard. Class 1 is targeted towards general purpose electronics which should not be applied for satellite flight components. Class 2 products are defined as products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Class 2 is usually affordable for CubeSat projects where funding is very limited but reliability is required. Class 3 targets products that demand continued high performance and zero equipment downtime, such as life support systems and other critical systems e.g. pacemaker, satellite, radar signals, etc[51]. Class 3 testing can be several times more expensive than Class 2 testing, thus not economically sensical to run circuits through it. Class 3/A includes Space and Military Avionics and is the highest class for circuit boards. Class 3/A is extremely costly and mostly ITAR restricted, so they are never considered for LEO CubeSat missions.

CHAPTER 7: CONCLUSION

The presented design for IlliniSat-2 electrical bus offers complete solution of a Command and Data Handling system, as well as a Power Generation and Distribution system. All the master requirements are met through the further divided subsystem requirements. The C&DH and Power systems can not only support power and communication to the rest of the IlliniSat-2 subsystems, but also up to three scientific payloads. The IlliniSat-2 bus is capable of generating solar power for CubeSat missions with size from 1.5U to 6U. The IlliniSat-2 bus was designed with reliability in mind and provided redundancy whenever possible to the C&DH and Power system. The capability of the IlliniSat-2 bus is demonstrated by the five missions listed in Chapter Two, with the mission sizes varying from 1.5U to 6U and payload count varying from one to three.

CubeSail satellite was delivered with the presented IlliniSat-2 C&DH and Power systems. When CubeSail is launched and makes communication with the ground station, it will be crucial to analyze the performance of those two systems. The lesson that will be learnt from CubeSail mission can be used to implement better IlliniSat bus.

The subsequent USIP missions and LAICE mission, due to their later delivery dates, will go through more testing compared with CubeSail. Those four missions will further demonstrate and validate IlliniSat-2 bus's capability for space operation.

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APPENDIX A: C&DH BOOTLOG

```
[    0.000000] Linux version 3.2.0-00362-gde97a28-dirty
(mitydsp@mitydsp-dev) (gcc version 4.5.3 20110311 (prerelease)
(GCC) ) #60 Fri Mar 16 16:37:22 EDT 2018
[    0.000000] CPU: ARMv7 Processor [413fc082] revision 2
(ARMv7), cr=10c53c7d
[    0.000000] CPU: PIPT / VIPT nonaliasing data cache, VIPT
aliasing instruction cache
[    0.000000] Machine: mitysom335x
[    0.000000] Memory policy: ECC disabled, Data cache writeback
[    0.000000] On node 0 totalpages: 131072
[    0.000000] free_area_init_node: node 0, pgdat c06f042c,
node_mem_map c073e000
[    0.000000]   Normal zone: 1024 pages used for memmap
[    0.000000]   Normal zone: 0 pages reserved
[    0.000000]   Normal zone: 130048 pages, LIFO batch:31
[    0.000000] AM335X ES2.1 (sgx neon )
[    0.000000] pcpu-alloc: s0 r0 d32768 u32768 alloc=1*32768
[    0.000000] pcpu-alloc: [0] 0
[    0.000000] Built 1 zonelists in Zone order, mobility
grouping on.  Total pages: 130048
[    0.000000] Kernel command line: console=ttyO0,115200n8
root=ubi0:rootfs rw ubi.mtd=8,4096 noinitrd rootfstype=ubifs
rootwait=1 ip=none
[    0.000000] PID hash table entries: 2048 (order: 1, 8192
bytes)
[    0.000000] Dentry cache hash table entries: 65536 (order: 6,
262144 bytes)
[    0.000000] Inode-cache hash table entries: 32768 (order: 5,
131072 bytes)
[    0.000000] Memory: 512MB = 512MB total
[    0.000000] Memory: 512332k/512332k available, 11956k
reserved, 0K highmem
[    0.000000] Virtual kernel memory layout:
[    0.000000]     vector  : 0xffff0000 - 0xffff1000   (   4 kB)
[    0.000000]     fixmap  : 0xfff00000 - 0xfffe0000   ( 896 kB)
[    0.000000]     vmalloc : 0xe0800000 - 0xff000000   ( 488 MB)
[    0.000000]     lowmem  : 0xc0000000 - 0xe0000000   ( 512 MB)
[    0.000000]     pkmap   : 0xbfe00000 - 0xc0000000   (   2 MB)
[    0.000000]     modules : 0xbf000000 - 0xbfe00000   (  14 MB)
[    0.000000]       .text : 0xc0008000 - 0xc0658000   (6464 kB)
[    0.000000]       .init : 0xc0658000 - 0xc0694000   ( 240 kB)
[    0.000000]       .data : 0xc0694000 - 0xc06fc0b8   ( 417 kB)
[    0.000000]        .bss : 0xc06fc0dc - 0xc073d7b4   ( 262 kB)
```

```
[    0.000000] NR_IRQS:396
[    0.000000] IRQ: Found an INTC at 0xfa200000 (revision 5.0)
with 128 interrupts
[    0.000000] Total of 128 interrupts on 1 active controller
[    0.000000] OMAP clockevent source: GPTIMER2 at 24000000 Hz
[    0.000000] OMAP clocksource: GPTIMER1 at 32768 Hz
[    0.000000] sched_clock: 32 bits at 32kHz, resolution
30517ns, wraps every 131071999ms
[    0.000000] Console: colour dummy device 80x30
[    0.000091] Calibrating delay loop... 795.44 BogoMIPS
(lpj=3977216)
[    0.039093] pid_max: default: 32768 minimum: 301
[    0.039215] Security Framework initialized
[    0.039306] Mount-cache hash table entries: 512
[    0.039642] CPU: Testing write buffer coherency: ok
[    0.040344] devtmpfs: initialized
[    0.059661] omap_hwmod: pruss: failed to hardreset
[    0.060821] print_constraints: dummy:
[    0.061157] NET: Registered protocol family 16
[    0.063140] OMAP GPIO hardware version 0.1
[    0.065460] omap_mux_init: Add partition: #1: core, flags: 0
[    0.067321] Configuring I2C Bus 1
[    0.067413]  omap_i2c.2: alias fck already exists
[    0.067596] Configuring I2C Bus 2
[    0.067657]  omap_i2c.3: alias fck already exists
[    0.068481] Registering mcspi 1 [2]
[    0.068511]  omap2_mcspi.1: alias fck already exists
[    0.068695] Registering mcspi 2 [2]
[    0.068725]  omap2_mcspi.2: alias fck already exists
[    0.068969]  edma.0: alias fck already exists
[    0.069000]  edma.0: alias fck already exists
[    0.069000]  edma.0: alias fck already exists
[    0.071899] baseboard_init [MityARM-335x DevKit]...
[    0.072204]  omap_hsmmc.0: alias fck already exists
[    0.072570]  omap_hsmmc.1: alias fck already exists
[    0.072814]  omap_hsmmc.2: alias fck already exists
[    0.095581] bio: create slab <bio-0> at 0
[    0.097534] SCSI subsystem initialized
[    0.099060] usbcore: registered new interface driver usbfs
[    0.099395] usbcore: registered new interface driver hub
[    0.099578] usbcore: registered new device driver usb
[    0.099731] musb-ti81xx musb-ti81xx: musb0, board_mode=0x3,
plat_mode=0x3
[    0.100006] musb-ti81xx musb-ti81xx: musb1, board_mode=0x3,
plat_mode=0x0
[    0.101074] omap_i2c omap_i2c.2: bus 2 rev2.4.0 at 100  kHz
```

```
[    0.119110] omap_i2c omap_i2c.3: bus 3 rev2.4.0 at 100 kHz
[    0.119964] tps65910 3-002d: JTAGREVNUM 0x1
[    0.122314] print_constraints: VRTC:
[    0.123748] print_constraints: VIO: at 1500 mV
[    0.126007] print_constraints: VDD1: 600 <--> 1500 mV at 1262
mV normal
[    0.128265] print_constraints: VDD2: 600 <--> 1500 mV at 1137
mV normal
[    0.129241] print_constraints: VDD3: 5000 mV
[    0.130645] print_constraints: VDIG1: at 1800 mV
[    0.132049] print_constraints: VDIG2: at 1800 mV
[    0.133453] print_constraints: VPLL: at 1800 mV
[    0.134857] print_constraints: VDAC: at 1800 mV
[    0.136260] print_constraints: VAUX1: at 1800 mV
[    0.137664] print_constraints: VAUX2: at 3300 mV
[    0.139099] print_constraints: VAUX33: at 3300 mV
[    0.140502] print_constraints: VMMC: at 3300 mV
[    0.140991] tps65910 3-002d: No interrupt support, no core
IRQ
[    0.141967] Advanced Linux Sound Architecture Driver Version
1.0.24.
[    0.143218] cfg80211: Calling CRDA to update world regulatory
domain
[    0.144287] Switching to clocksource gp timer
[    0.161468] musb-hdrc: version 6.0, ?dma?, otg
(peripheral+host)
[    0.161621] musb-hdrc musb-hdrc.0: dma type: dma-cppi41
[    0.161926] MUSB0 controller's USBSS revision = 4ea20800
[    0.161956] musb0: Enabled SW babble control
[    0.161956] musb-hdrc: ConfigData=0xde (UTMI-8, dyn FIFOs,
bulk combine, bulk split, HB-ISO Rx, HB-ISO Tx, SoftConn)
[    0.161987] musb-hdrc: MHDRC RTL version 2.0
[    0.161987] musb-hdrc: setup fifo_mode 4
[    0.162017] musb-hdrc: 28/31 max ep, 16384/16384 memory
[    0.162017] musb-hdrc.0: bulk split disabled
[    0.162048] musb-hdrc.0: bulk combine disabled
[    0.162506] musb-hdrc musb-hdrc.0: USB OTG mode controller at
e083c000 using PIO, IRQ 18
[    0.162658] musb-hdrc musb-hdrc.1: dma type: dma-cppi41
[    0.162902] MUSB1 controller's USBSS revision = 4ea20800
[    0.162933] musb1: Enabled SW babble control
[    0.162963] musb-hdrc: ConfigData=0xde (UTMI-8, dyn FIFOs,
bulk combine, bulk split, HB-ISO Rx, HB-ISO Tx, SoftConn)
[    0.162963] musb-hdrc: MHDRC RTL version 2.0
[    0.162963] musb-hdrc: setup fifo_mode 4
[    0.162994] musb-hdrc: 28/31 max ep, 16384/16384 memory
```

```
[    0.162994] musb-hdrc.1: bulk split disabled
[    0.163024] musb-hdrc.1: bulk combine disabled
[    0.163085] musb-hdrc musb-hdrc.1: MUSB HDRC host driver
[    0.163146] musb-hdrc musb-hdrc.1: new USB bus registered,
assigned bus number 1
[    0.163269] usb usb1: New USB device found, idVendor=1d6b,
idProduct=0002
[    0.163269] usb usb1: New USB device strings: Mfr=3,
Product=2, SerialNumber=1
[    0.163299] usb usb1: Product: MUSB HDRC host driver
[    0.163299] usb usb1: Manufacturer: Linux 3.2.0-00362-
gde97a28-dirty musb-hcd
[    0.163299] usb usb1: SerialNumber: musb-hdrc.1
[    0.164123] hub 1-0:1.0: USB hub found
[    0.164154] hub 1-0:1.0: 1 port detected
[    0.164794] musb-hdrc musb-hdrc.1: USB OTG mode controller at
e083e800 using PIO, IRQ 19
[    0.165191] NET: Registered protocol family 2
[    0.165344] IP route cache hash table entries: 4096 (order:
2, 16384 bytes)
[    0.165618] TCP established hash table entries: 16384 (order:
5, 131072 bytes)
[    0.165893] TCP bind hash table entries: 16384 (order: 4,
65536 bytes)
[    0.166046] TCP: Hash tables configured (established 16384
bind 16384)
[    0.166076] TCP reno registered
[    0.166076] UDP hash table entries: 256 (order: 0, 4096
bytes)
[    0.166107] UDP-Lite hash table entries: 256 (order: 0, 4096
bytes)
[    0.166259] NET: Registered protocol family 1
[    0.166503] RPC: Registered named UNIX socket transport
module.
[    0.166534] RPC: Registered udp transport module.
[    0.166534] RPC: Registered tcp transport module.
[    0.166534] RPC: Registered tcp NFSv4.1 backchannel transport
module.
[    0.166748] NetWinder Floating Point Emulator V0.97 (double
precision)
[    0.184448] VFS: Disk quotas dquot_6.5.2
[    0.184509] Dquot-cache hash table entries: 1024 (order 0,
4096 bytes)
[    0.184997] msgmni has been set to 1000
[    0.185791] io scheduler noop registered
[    0.185821] io scheduler deadline registered
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[    0.185882] io scheduler cfq registered (default)
[    0.187652] Serial: 8250/16550 driver, 4 ports, IRQ sharing
enabled
[    0.189453] omap_uart.0: ttyO0 at MMIO 0x44e09000 (irq = 72)
is a OMAP UART0
[    0.886596] console [ttyO0] enabled
[    0.890869] omap_uart.1: ttyO1 at MMIO 0x48022000 (irq = 73)
is a OMAP UART1
[    0.898742] omap_uart.2: ttyO2 at MMIO 0x48024000 (irq = 74)
is a OMAP UART2
[    0.906555] omap_uart.3: ttyO3 at MMIO 0x481a6000 (irq = 44)
is a OMAP UART3
[    0.914337] omap_uart.4: ttyO4 at MMIO 0x481a8000 (irq = 45)
is a OMAP UART4
[    0.922149] omap_uart.5: ttyO5 at MMIO 0x481aa000 (irq = 46)
is a OMAP UART5
[    0.939331] brd: module loaded
[    0.947387] loop: module loaded
[    0.950836] i2c-core: driver [tsl2550] using legacy suspend
method
[    0.957336] i2c-core: driver [tsl2550] using legacy resume
method
[    0.963745] at24 2-0050: 256 byte 24c02 EEPROM, read-only, 0
bytes/write
[    0.976593] MitySOM-335x: Part Number = 3354-HX-X38-RI
[    0.981964] MityARM-335x DevKit: factory_config_callback
[    0.988159] No SPI NOR Flash found.
[    0.991790] Configuring 512MB NAND device
[    0.996704] omap-gpmc omap-gpmc: GPMC revision 6.0
[    1.001708] Registering NAND on CS0
[    1.007720] m25p80 spi2.0: m25p64-nonjedec (8192 Kbytes)
[    1.013275] Creating 1 MTD partitions on "spi_flash":
[    1.018615] 0x000000000000-0x000000800000 : "NOR User
Defined"
[    1.026641] omap2-nand driver initializing
[    1.031219] ONFI flash detected
[    1.034637] ONFI param page 0 valid
[    1.038299] NAND device: Manufacturer ID: 0x2c, Chip ID: 0xdc
(Micron MT29F4G08ABAEAWP)
[    1.046722] Creating 8 MTD partitions on "omap2-nand.0":
[    1.052276] 0x000000000000-0x000000040000 : "SPL"
[    1.058837] 0x000000040000-0x000000080000 : "SPL.backup1"
[    1.065826] 0x000000080000-0x0000000c0000 : "SPL.backup2"
[    1.072723] 0x0000000c0000-0x000000100000 : "SPL.backup3"
[    1.079681] 0x000000100000-0x000000300000 : "U-Boot"
[    1.086517] 0x000000300000-0x000000340000 : "U-Boot Env"
```

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[    1.093322] 0x000000340000-0x000000840000 : "Kernel"
[    1.100830] 0x000000840000-0x000020000000 : "File System"
[    1.210357] usb 1-1: new full-speed USB device number 2 using
musb-hdrc
[    1.218841] OneNAND driver initializing
[    1.225158] CAN device driver interface
[    1.229156] CAN bus driver for Bosch D_CAN controller 1.0
[    1.235443] PPP generic driver version 2.4.2
[    1.240295] PPP BSD Compression module registered
[    1.245239] PPP Deflate Compression module registered
[    1.250946] PPP MPPE Compression module registered
[    1.255981] NET: Registered protocol family 24
[    1.260955] usbcore: registered new interface driver
cdc_ether
[    1.267242] usbcore: registered new interface driver
cdc_subset
[    1.273468] Initializing USB Mass Storage driver...
[    1.278808] usbcore: registered new interface driver usb-
storage
[    1.285095] USB Mass Storage support registered.
[    1.290313] usbcore: registered new interface driver
usbserial
[    1.296417] usbserial: USB Serial Driver core
[    1.301116] USB Serial support registered for FTDI USB Serial
Device
[    1.308044] usbcore: registered new interface driver ftdi_sio
[    1.314025] ftdi_sio: v1.6.0:USB FTDI Serial Converters
Driver
[    1.320739] mousedev: PS/2 mouse device common for all mice
[    1.329559] tps65910-rtc tps65910-rtc: Wake up is not
possible as irq = 0
[    1.342498] tps65910-rtc tps65910-rtc: rtc core: registered
tps65910-rtc as rtc0
[    1.350463] i2c /dev entries driver
[    1.354766] Linux media interface: v0.10
[    1.359039] Linux video capture interface: v2.00
[    1.364166] usbcore: registered new interface driver uvcvideo
[    1.370208] USB Video Class driver (1.1.1)
[    1.431396] usb 1-1: New USB device found, idVendor=0403,
idProduct=6015
[    1.438415] usb 1-1: New USB device strings: Mfr=1,
Product=2, SerialNumber=3
[    1.445861] usb 1-1: Product: FT230X Basic UART
[    1.450592] usb 1-1: Manufacturer: FTDI
[    1.454589] usb 1-1: SerialNumber: DN03ZBU3
```

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[    1.462738] ftdi_sio 1-1:1.0: FTDI USB Serial Device
converter detected
[    1.469909] usb 1-1: Detected FT-X
[    1.473480] usb 1-1: Number of endpoints 2
[    1.477752] usb 1-1: Endpoint 1 MaxPacketSize 64
[    1.482574] usb 1-1: Endpoint 2 MaxPacketSize 64
[    1.487426] usb 1-1: Setting MaxPacketSize 64
[    1.492462] usb 1-1: FTDI USB Serial Device converter now
attached to ttyUSB0
[    1.501464] OMAP Watchdog Timer Rev 0x01: initial timeout 60
sec
[    1.510009] cpuidle: using governor ladder
[    1.514739] cpuidle: using governor menu
[    1.526123] usbcore: registered new interface driver usbhid
[    1.531951] usbhid: USB HID core driver
[    1.537048] usbcore: registered new interface driver snd-usb-
audio
[    1.545074] ALSA device list:
[    1.548187]    No soundcards found.
[    1.551727] oprofile: hardware counters not available
[    1.557037] oprofile: using timer interrupt.
[    1.561492] nf_conntrack version 0.5.0 (8005 buckets, 32020
max)
[    1.568267] ip_tables: (C) 2000-2006 Netfilter Core Team
[    1.573913] TCP cubic registered
[    1.577301] NET: Registered protocol family 17
[    1.581970] can: controller area network core (rev 20090105
abi 8)
[    1.588500] NET: Registered protocol family 29
[    1.593139] can: raw protocol (rev 20090105)
[    1.597625] can: broadcast manager protocol (rev 20090105 t)
[    1.603546] lib80211: common routines for IEEE802.11 drivers
[    1.609466] lib80211_crypt: registered algorithm 'NULL'
[    1.609497] lib80211_crypt: registered algorithm 'WEP'
[    1.609497] lib80211_crypt: registered algorithm 'CCMP'
[    1.609497] lib80211_crypt: registered algorithm 'TKIP'
[    1.609527] Registering the dns_resolver key type
[    1.614501] VFP support v0.3: implementor 41 architecture 3
part 30 variant c rev 3
[    1.622528] ThumbEE CPU extension supported.
[    1.627044] mux: Failed to setup hwmod io irq -22
[    1.632507] Power Management for AM33XX family
[    1.637176] pm: Err (-22) setting core voltage setting
[    1.642730] Trying to load am335x-pm-firmware.bin (60 secs
timeout)
[    1.649414] Copied the M3 firmware to UMEM
```

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[    1.653717] Cortex M3 Firmware Version = 0x186
[    1.663665] UBI: attaching mtd8 to ubi0
[    1.907775] mmc0: new high speed MMC card at address 0001
[    1.926239] Hi, Im here: mmcblk0: mmc0:0001 Q2J55L 7.12 GiB
[    1.932250] mmcblk0boot0: mmc0:0001 Q2J55L partition 1 2.00
MiB
[    1.938568] mmcblk0boot1: mmc0:0001 Q2J55L partition 2 2.00
MiB
[    1.957946]  mmcblk0: unknown partition table
[    1.992279]  mmcblk0boot1: unknown partition table
[    2.016815]  mmcblk0boot0: unknown partition table
[    2.207672] mmc1: new high speed MMC card at address 0001
[    2.226104] Hi, Im here: mmcblk1: mmc1:0001 Q2J54A 3.58 GiB
[    2.232116] mmcblk1boot0: mmc1:0001 Q2J54A partition 1 16.0
MiB
[    2.238433] mmcblk1boot1: mmc1:0001 Q2J54A partition 2 16.0
MiB
[    2.257720]  mmcblk1: unknown partition table
[    2.291961]  mmcblk1boot1: unknown partition table
[    2.316436]  mmcblk1boot0: unknown partition table
[    2.507324] mmc2: new high speed MMC card at address 0001
[    2.525726] Hi, Im here: mmcblk2: mmc2:0001 Q2J54A 3.58 GiB
[    2.531738] mmcblk2boot0: mmc2:0001 Q2J54A partition 1 16.0
MiB
[    2.538024] mmcblk2boot1: mmc2:0001 Q2J54A partition 2 16.0
MiB
[    2.559356]  mmcblk2: unknown partition table
[    2.591552]  mmcblk2boot1: unknown partition table
[    2.616119]  mmcblk2boot0: unknown partition table
[    5.902923] UBI: scanning is finished
[    5.923034] UBI: attached mtd8 (name "File System", size 503
MiB) to ubi0
[    5.930175] UBI: PEB size: 262144 bytes (256 KiB), LEB size:
253952 bytes
[    5.937286] UBI: min./max. I/O unit sizes: 4096/4096, sub-
page size 4096
[    5.944274] UBI: VID header offset: 4096 (aligned 4096), data
offset: 8192
[    5.951477] UBI: good PEBs: 2015, bad PEBs: 0, corrupted
PEBs: 0
[    5.957763] UBI: user volume: 1, internal volumes: 1, max.
volumes count: 128
[    5.965209] UBI: max/mean erase counter: 43/21, WL threshold:
4096, image sequence number: 1104463418
[    5.974853] UBI: available PEBs: 0, total reserved PEBs:
2015, PEBs reserved for bad PEB handling: 40
```

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[    5.984649] UBI: background thread "ubi_bgt0d" started, PID
721
[    5.994293] tps65910-rtc tps65910-rtc: setting system clock
to 2000-01-01 01:12:24 UTC (946689144)
[    6.067108] UBIFS: background thread "ubifs_bgt0_0" started,
PID 725
[    6.137145] UBIFS: recovery needed
[    6.506347] UBIFS: recovery completed
[    6.510284] UBIFS: mounted UBI device 0, volume 0, name
"rootfs"
[    6.516571] UBIFS: LEB size: 253952 bytes (248 KiB),
min./max. I/O unit sizes: 4096 bytes/4096 bytes
[    6.526123] UBIFS: FS size: 398704640 bytes (380 MiB, 1570
LEBs), journal size 9404416 bytes (8 MiB, 38 LEBs)
[    6.536499] UBIFS: reserved for root: 0 bytes (0 KiB)
[    6.541778] UBIFS: media format: w4/r0 (latest is w4/r0),
UUID 4884BFB3-1E1C-425E-A654-C75ECDD298E8, small LPT model
[    6.554901] VFS: Mounted root (ubifs filesystem) on device
0:14.
[    6.561492] Freeing init memory: 240K
```

APPENDIX B: PICTURES OF PCB REVISIONS
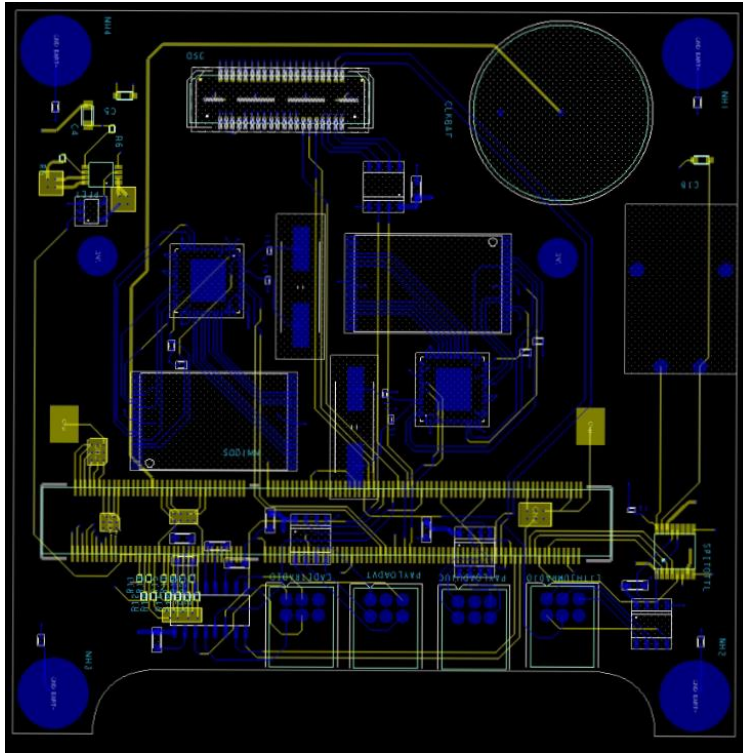
Figure 56: C&DH Revision 2
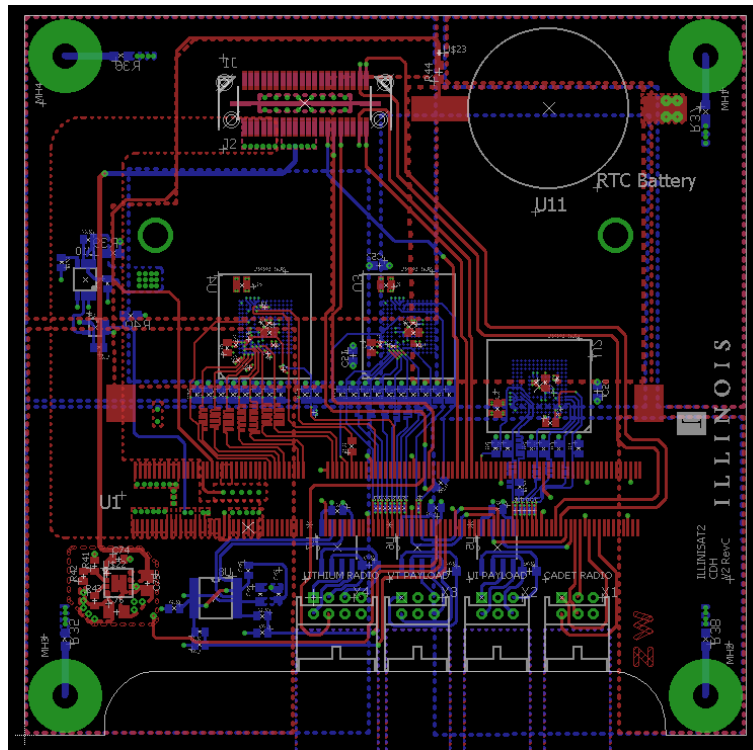
Figure 57: C&DH Revision 3
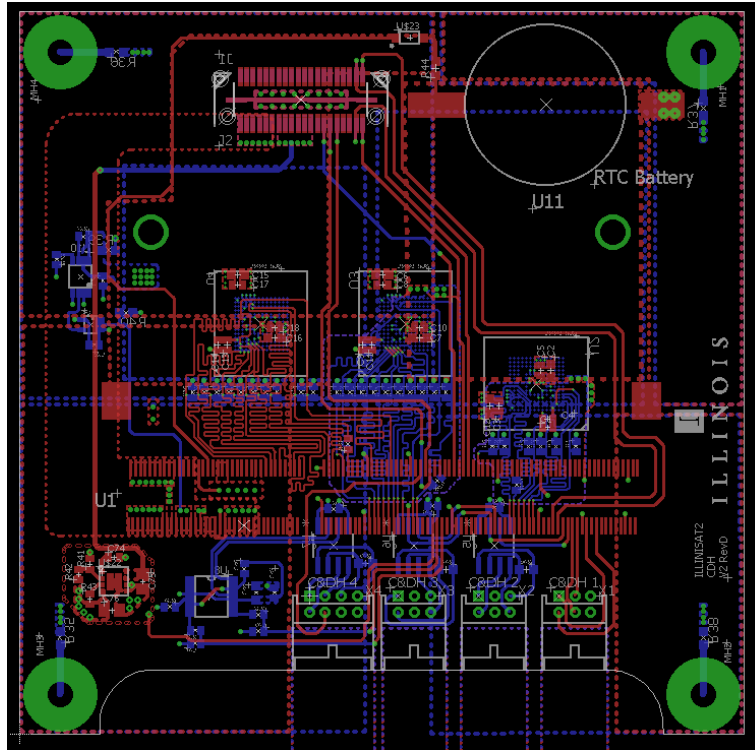
Figure 58: C&DH Revision 4
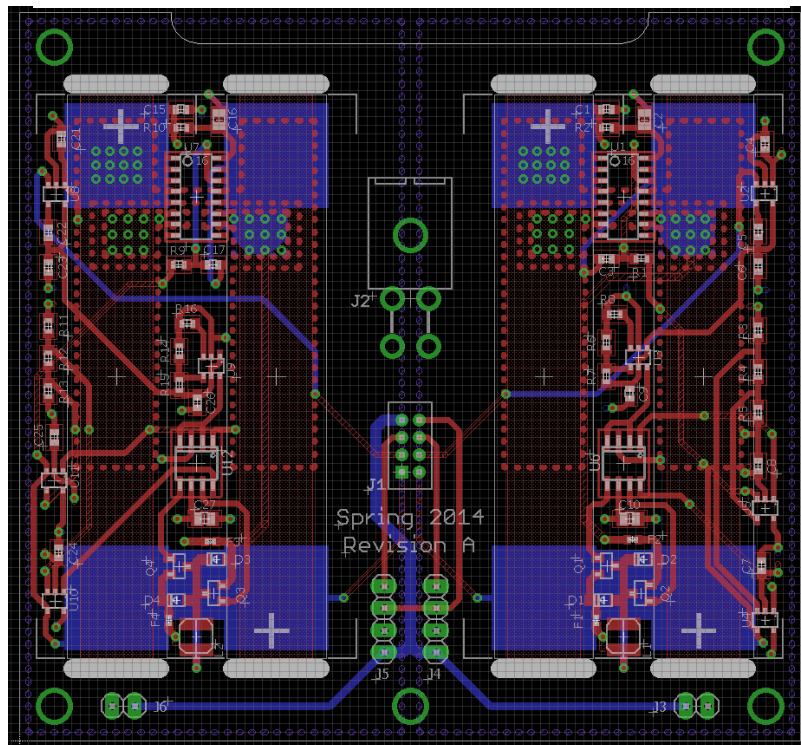
Figure 59: Battery Pack Revision A
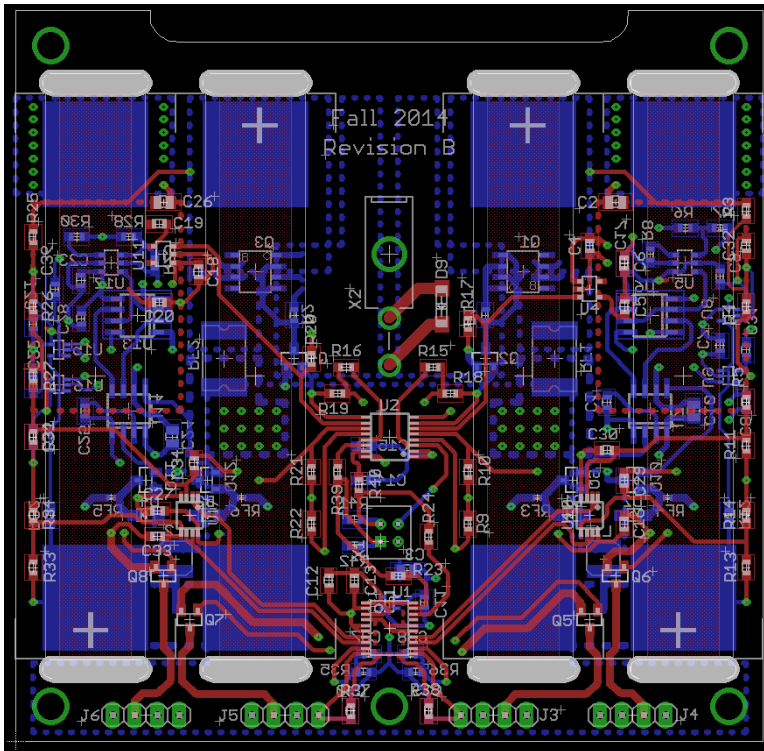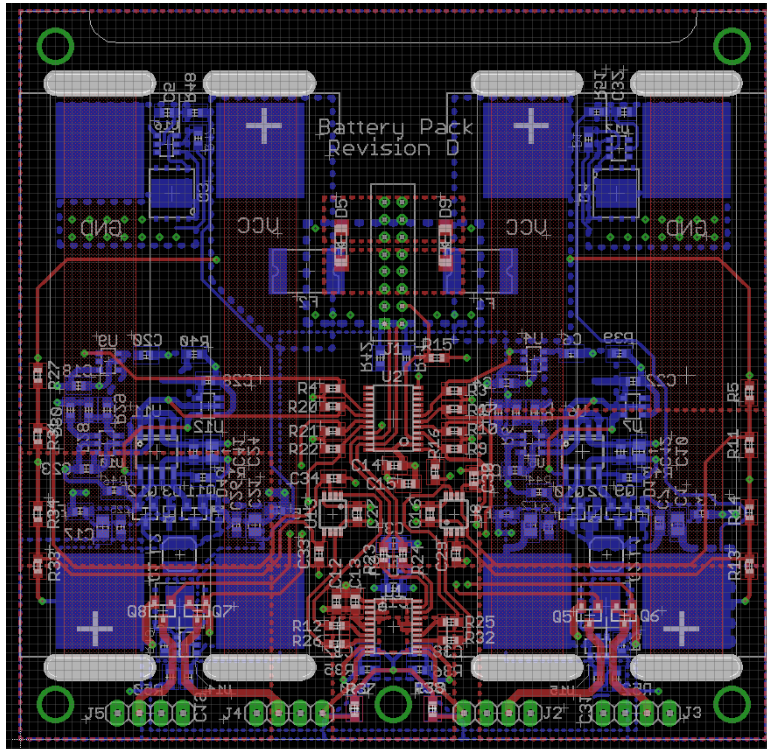
Figure 60: Battery Pack Revision B
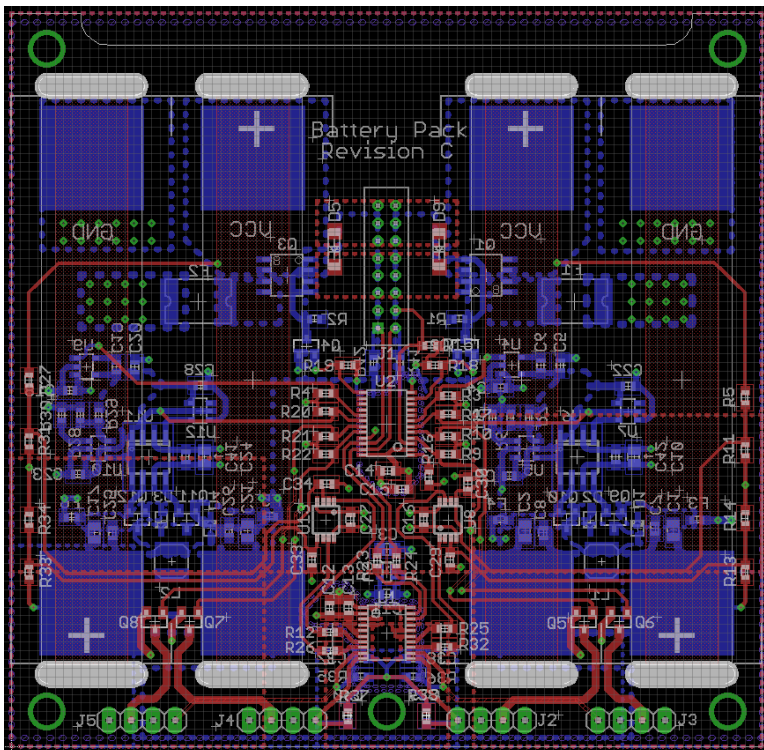
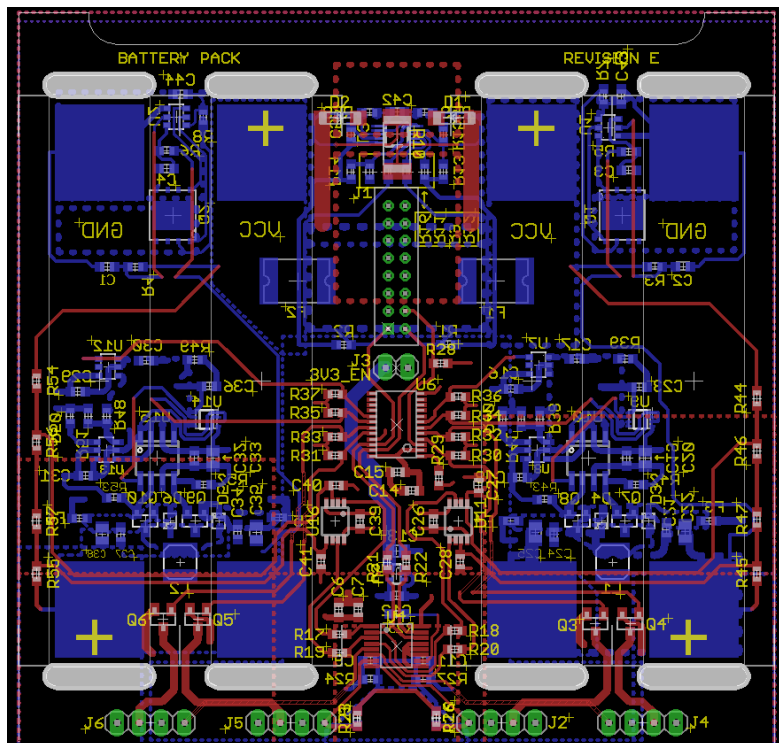**Figure 61: Battery Pack Revision C**
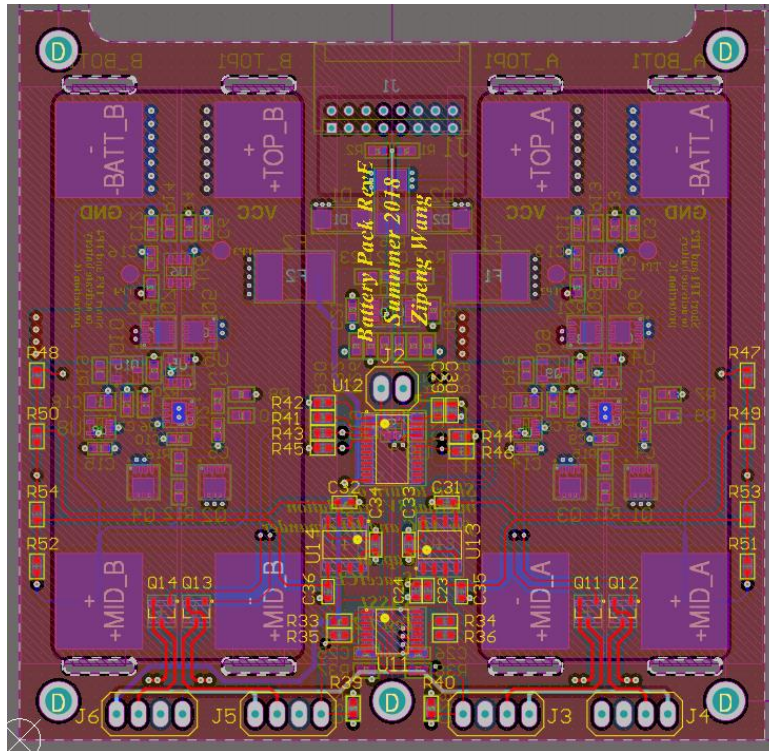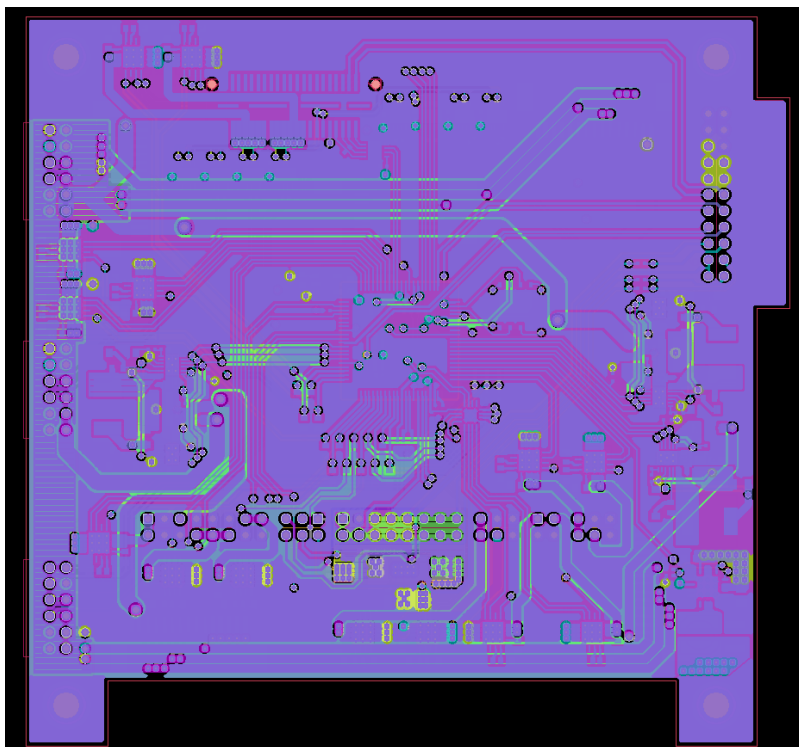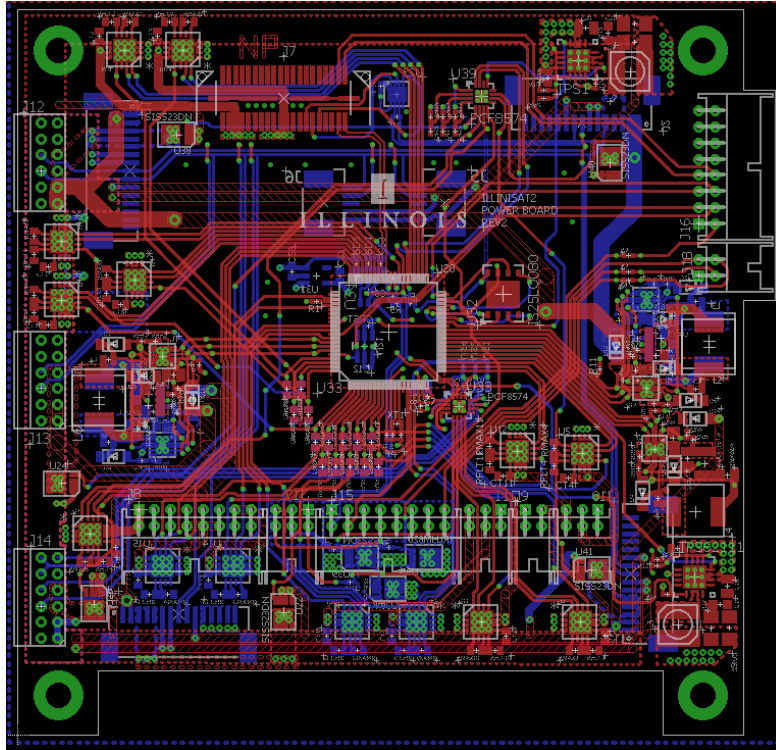
Figure 62: Battery Pack Revision D
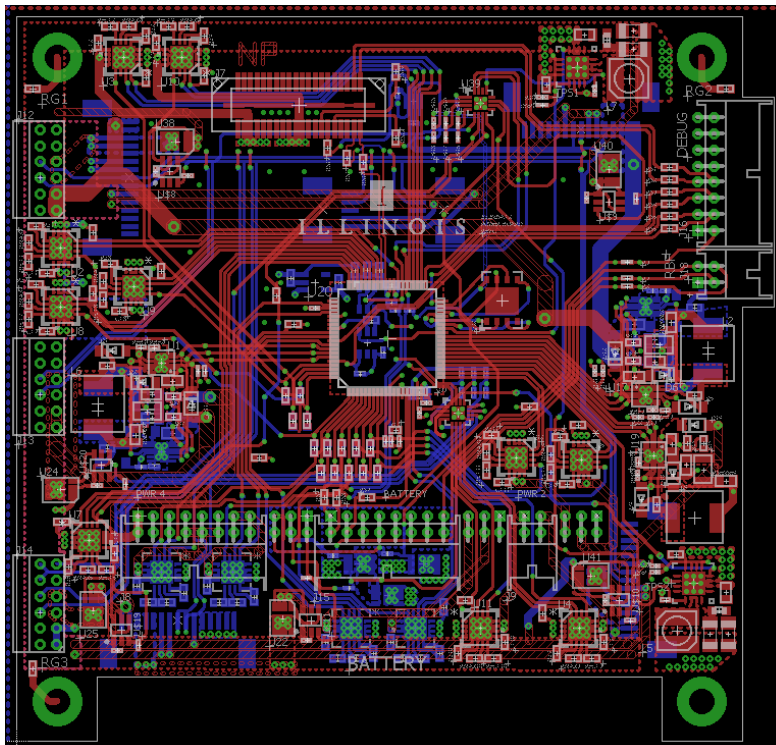

Figure 63: Battery Pack Revision E

Figure 64: Battery Pack Revision F

Figure 65: Power Board Revision A

Figure 66: Power Board Revision B

Figure 67: Power Board Revision C