FAILURES CAUSED BY SUPPLY FLUCTUATIONS DURING SYSTEM-LEVEL ESD

BY

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DISSERTATION

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ABSTRACT

It is necessary to design robust electronic systems against system-level electrostatic discharge (ESD). In additional to withstanding ESD without hard failures (permanent damage), it is important that the system is robust against soft failures (recoverable loss of function or data), which can be caused by ESD-induced noise on signal inputs and power nets. Besides radiation, the current injection into the circuit alone can cause these disturbances, especially the sharp current spike of a high amplitude in system-level ESD. The waveform of this current is similar in various ESD test setups. Circuit models with distributed elements enable accurate modeling of the system-level ESD current in contact discharge. Experiments have shown that ESD-induced noise on signal traces starts to disturb the IO input at very low ESD levels, and the effectiveness of the transient voltage suppressor (TVS) on board is limited. The noise on supply is global to integrated circuit (IC), as it travels across all the power domains. The waveform of the noise depends on the polarity of the ESD current and the type of ESD protection. The experiments have shown that the supply fluctuation can be quite severe, as a strong reverse of the on-chip supply is indicated by monitor circuits starting from the ESD levels below the common required passing level. This poses a requirement of a minimum amount of on-chip decoupling capacitances (decaps) to limit the amplitude of supply fluctuations. This requirement is similar whether the supply voltage is generated on-chip or off-chip, as

long as a large amount of off-chip decap is used and connected to the board ground. If the supply voltage is generated on-chip, the regulator needs to be carefully designed against ESD induced noise. In addition, the rail clamp, if not optimized, deteriorates the power integrity with its instability. The ESD-induced supply fluctuation may cause latch-up without careful attention to the well-bias scheme.

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LIST OF ABBREVIATIONS

APD	antiparallel diode
CDE	cable discharge event
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
decap	decoupling capacitance
ESD	electrostatic discharge
EUT	equipment under test
VDDext	externally generated VDD
FFT	fast Fourier transform
GD	glitch detector
HBM	human body model
HCP	horizontal coupling plane
HMM	human metal model
IC	integrated circuit
VDD_{int}	internally generated VDD
ORED	out-of-range error detector
PCB	printed circuit board
PDN	power delivery network
PSRR	power supply rejection ratio

RBB	reverse body bias
SCR	silicon controlled rectifier
SEED	system-efficient ESD design
SOA	safe operating area
TLP	transmission line pulse
TVS	transient voltage suppressor
VNA	vector network analyzer

CHAPTER 1

INTRODUCTION

Electrostatic discharge (ESD) is a concern for the reliability of all electronic systems. Static electricity can be built up by triboelectrification, which occurs during contact between two materials [1]. The charge is redistributed when the charged object contacts another object at a different electric potential. An integrated circuit (IC) in the discharge path is subject to damage due to heating or over voltage. To protect ICs from such damage, several committees (e.g. JEDEC, ESDA, IEC, ISO, etc.) have published many qualification procedures which specify that ICs must pass certain ESD target levels. These qualifications describe discharges that represent various scenarios in the manufacture, handling and operation of the ICs.

One group of these qualifications is classified as component-level ESD, such as the human body model (HBM) and charged device model (CDM). HBM testing requirements ensure that the IC is not damaged when an operator is handling a packaged IC, and CDM testing requirements ensure the IC is not damaged when a machine is handling the IC. These tests are always done when the IC is not powered. The target levels for component-level ESD have decreased over the years with stricter ESD control in the factory on the maximum amount of charge that can be accumulated in the environment and how the

charge is dissipated. For example, electrically dissipative materials and electrostatic neutralizers are widely used.

System-level ESD describes the possible ESD hazard that occurs in a system. In this context, “system” refers to an electronic product, which is itself a broad category; examples include smart phones, automobile GPS navigation systems, power meters, and computer clusters. Widely used qualifications include IEC 61000-4-2: Electrostatic discharge immunity test, IEC 61000-4-5: Surge immunity test, ISO 10605: Road vehicles – Test methods for electrical disturbances from electrostatic discharge [2]. Each qualification targets a certain group of applications. For example, automobile electronic systems must meet ESD target levels specified by ISO 10605, and ethernet transceivers must survive in the cable discharge event (CDE) [3], [4].

In system-level ESD tests, the reaction of the equipment under test (EUT) is categorized in four classes [5]: A: EUT continues to function normally; B: EUT has an upset condition but recovers automatically; C: EUT has an upset condition and needs manual interference to recover; D: EUT is damaged. In this dissertation, Classes B and C are categorized as soft failures, while Class D is categorized as hard failures. For soft failures studied in this dissertation, it is assumed that they are caused by loss of function or data of the IC.

When the EUT is under a system-level ESD test, it may be powered off or powered on. Since the discharge occurs at the user site, there is less ESD environment control than where the ICs are assembled into the system. The challenge that system-level ESD poses to circuit design other than component-level ESD is that the amplitude of the discharging current is much higher and the system may be in operation. Hard failures to an IC can

occur during system-level ESD even though it passes the component-level ESD test [5]. A power-on system may have different behavior compared to its power-off state during ESD. The power-on system may also experience soft errors, which is not desired but essentially recoverable. A better understanding is necessary for engineers to address potential system-level ESD-related failures in the early design phase.

Efforts have been made to develop a co-design methodology between circuit and system design engineers to address the challenges of system-level ESD [6]. ICs are characterized with transmission line pulse (TLP) measurements and the models derived are used for prediction of the response of the EUT in system-level ESD to estimate the passing level. In the TLP measurement, a square current pulse, usually with a 10-ns rise time and a 100-ns pulse width, is injected to the IC. At the end of the pulse, when the current and voltage are stabilized, the current and voltage are measured as an average from the sampling window. The obtained current-voltage pairs at different pulse amplitudes are plotted as a quasi-static I-V curve of the IC.

However, system-level ESD pulses generally have shorter rise times and pulse widths than the TLP. Since the IC generally contains nonlinear elements with memory, its quasi-static I-V characteristics obtained from pulse measurements may depend on the rise time of the TLP. In addition, the quasi-static I-V characteristics also have self-heating effects [7]. Therefore, even for cases where the current and voltage of the IC are stabilized in system-level ESD, the I-V characteristics obtained in TLP cannot represent the quasi I-V characteristics in system-level ESD. It is not straightforward to predict the hard failure level for system-level ESD from TLP measurements due to pulse-width dependency [8], [9]. A more important concern is that many failures are related to the

transient response at the edges of the ESD pulse, and the transient behavior usually cannot be estimated from quasi-static I-V characteristics. The transient characteristics are affected by elements such as a parasitic capacitor [10]. It is important to gather information about inductances and decoupling capacitances (decaps) in the system to understand the response to system-level ESD.

One of the most commonly used qualification is IEC 61000-4-2 [11], which represents the discharge that occurs when a person holding a metal tool approaches a system that is at a different potential; the charged object may be either the person or the system. For commercial electronic products, only soft failures that do not result in degradation of performance or the performance is degraded to an unacceptable level after the test are allowed for 4 kV contact and 8 kV air discharge [12], [13]. Contact discharge is the test method where the charged electrode of the ESD tester is kept in contact with the conductive surfaces of the EUT or coupling planes; air discharge is the test method where the electrode approaches the EUT until it touches the insulating surfaces of the EUT [11].

The apparatus that is used to generate the stress is an ESD gun. For a contact discharge, the gun tip is kept in contact with a metal part of the system and then a switch is actuated; for an air discharge, the switch is actuated first and then the gun approaches the system —there is a spark when the discharge is initiated. The system is still under stress when there is no spark, since the capacitance between the EUT and the gun, which maintains the potential difference, increases as the gun approaches [14]. The discharge current waveforms resulting from contact discharge display less variability due to the absence of the spark. This dissertation focuses on contact discharge.

The ESD current waveforms obtained when testing a variety of systems may differ dramatically. The EUT constitutes the load seen by the gun, and these systems may present very different loads. Therefore, the ESD current that enters an IC within the EUT will depend on the larger system design, e.g. whether the EUT is battery operated or plugged into a power source, whether the EUT has a well-grounded shield, whether there are filtering elements at the input to the IC, etc. The accurate modeling of system-level ESD currents with different loads requires an understanding of the EUT as well as the ESD test bed.

The ESD protection of an IC affects the IC's response to system-level ESD. Figure 1.1 shows a typical ESD protection scheme for a low-voltage complementary metal-oxide-semiconductor (CMOS) IC. The ESD protection circuit at an IO pin affects whether the ESD current leaves the IC through the power net or the ground net. For positive ESD currents into IO1, the top diode sends current to the power net, while the positive ESD current into IO2 goes through the silicon controlled rectifier (SCR) to the ground net. The rail clamp circuits limit the maximum possible voltage of each power domain during ESD. The reverse diodes between power and ground nets form a current path with smaller effective resistance than the other circuits when the supply is reversed. The ground nets of VDDIO1 and VDDIO2 domains are connected with antiparallel diodes (APDs). These APDs limit the maximum possible voltage for cross-domain circuitry while maintaining isolation between the two ground nets under normal operating conditions. These circuits consist of the main current path during ESD, and the choice of the protections affects the likelihood for soft failures to occur as well as hard failures. In addition, the amount of on-chip decap also plays a significant role. When the power

domain is regulated on chip, the design of the regulator needs to take into account its robustness against ESD.

Generally, the ESD current discharged in an IO exits the IC through the power nets and the ground nets. These currents then go through the power delivery network (PDN) of the system. The impedance of the system's PDN seen from the IC is not negligible, and there is a significant contribution from the package inductances. The "$L\frac{di}{dt}$" effect of these package inductances is a concern for on-chip power integrity, which may result in soft failures, and sometimes hard failures.

1.1 Overview

This dissertation first addresses the modeling of the contact discharge current during system-level ESD and then studies how this current disturbs the operation of an IC with the focus on the induced supply fluctuations. The contact discharge current is modeled with distributed elements to represent the coupling between the ground strap and its environment in Chapter 2. After the discharge current is modeled, Chapter 3 illustrates the case study of upsets in the various monitors on a 65-nm CMOS test chip with different board designs. The observations indicate that the upsets come from signal input corruption as well as supply fluctuations. Then Chapter 4 discusses how the power integrity is compromised by ESD for externally regulated supply domains with the "$L\frac{di}{dt}$" effect in particular, and Chapter 5 shows that the rail clamp in the ESD protection network can be one of the causes. The requirements for internally regulated supply domains to have robust power integrity against ESD are presented in Chapter 6. Chapter

7 shows the latch-up study of circuits using reverse body bias (RBB), where it is found that the supply fluctuation is one potential hazard leading to latch-up. In Chapter 8, a circuit model of air discharge is presented. Finally, Chapter 9 discusses future work and Chapter 10 concludes the dissertation.

1.2 Figures

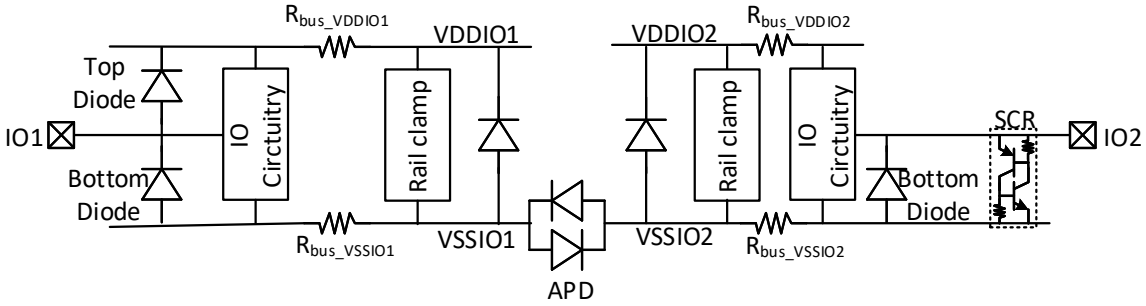


Figure 1.1: Typical ESD protection scheme. IO1 is protected by dual diodes. IO2 is protected by an SCR and a bottom diode. Both power domains are protected by rail clamps and reverse diodes. The two VSSIO nets are connected by APDs.

CHAPTER 2

MODELING OF SYSTEM-LEVEL ESD TEST CURRENT

To understand how soft and hard failures occur during system-level ESD, it is important to correctly model the ESD current. Since many soft failures are related to the rising and falling edges of the ESD current pulse, the model needs to generate the amplitude, the rise and fall times of the current that match the real case. The system-efficient ESD design (SEED) methodology, as described in [6], uses circuit-level simulation to design for robustness against hard failures caused by direct contact discharge. To run the simulations, there must be available circuit models for the ESD gun, the test bed, and the EUT. EUT modeling has been described in many publications, e.g. [15], [16], [17], [18]; similarly, circuit equivalent models of ESD guns can be found in the open literature, e.g. [19], [20], [21]. Full wave modeling and simulation have been used to extract test bed models [15], but this approach is computationally intensive. More typically, the models are measurement-based [22], [23], [24].

2.1 IEC 61000-4-2 test setup and calibration

According to IEC 61000-4-2, the system-level ESD test is performed on the test bed shown in Figure 2.1. The EUT, if not required to mount on ground, is placed on the 1.6 m

by 0.8 m horizontal coupling plane (HCP). This floating metal plane is connected to the ground plane through two 470 kΩ bleeding resistors. The discharging current is generated by the ESD gun, with its ground strap connected to the ground plane. It is essentially a one-pin discharge without a clearly defined current return path.

The ESD gun contains a 150-pF storage capacitor, a 330-Ω discharge resistor [25], and some pulse shaping elements. Lumped RLC models based on this RC circuit are widely used [26], [27], [28], [29]. The model shown in Figure 2.2 [21] is one of these RLC models that can be used to model the ESD gun discharging to a grounded 2 Ω target, which generates the current waveform shown in Figure 2.3 as required by the standard. R_{fast} and C_{fast} provide a first-order representation of the coupling between the gun and its environment, which in this case primarily consists of the calibration target's ground plane. These two elements would also capture the effect of (proprietary) components inside the gun added by the manufacturer to obtain an output waveform that conforms to the test standard. Representing the pulse-shaping circuitry and the coupling effects by a two-element RC model is likely an over-simplification, but is adequate for the case under consideration. The first peak shown in the figure comes from the pulse-shaping elements and the parasitics, including the capacitor formed between the gun and the EUT, that gets charged along with the major discharge unit. Fast Fourier transform (FFT) of this current in Figure 2.4 shows that most current components lie below 500 MHz.

The target consists of twenty-five 51 Ω resistors, connected in parallel; the target's ground-side consists of a large metal plane. An SMA connector is mounted on the target so that measurement apparatus can be connected in parallel with the load. The voltage

across the target is measured and the current is calculated based on the impedance of the target. All other discharge currents shown in this dissertation were measured at the gun tip with an F-65A current probe. The current probe has a band-pass characteristic. Its 3-dB roll-off frequency is below 100 kHz, and it has a uniform response up to 1 GHz. In this dissertation, the target is custom made. The target's S_{11} was measured so that any significant non-idealities could be accounted for in the simulation; the resultant data indicate that the target is more accurately represented as a 2.2 Ω resistor in series with an 8-nH inductor. The target begins to appear inductive above 44 MHz.

If the first peak of the ESD current waveform enters an IC without first being filtered, it is responsible for most of the soft failures. It may also cause hard failures resulting from the high electric field applied at the gate dielectric of the receiver. The peak current is not sensitive to the EUT characteristics; it is roughly equal to 3.75 A/kV. The rise time of the first peak depends on the system configuration, but it is usually on the scale of nanoseconds, or less. The large time-derivative of this current, di/dt, induces a strong magnetic field. This changing field induces voltages at neighboring nets and causes supply fluctuations, as will be shown in Chapter 3 and Chapter 4. The second peak of the waveform, if there is any, is mainly responsible for hard failures with its large energy injected into the system. This pulse may be longer than 100 ns, and excess carriers may accumulate in the substrate. These injected carriers may cause latch-up and data lost at high impedance nodes [30].

The current paths for the two peaks are not necessarily the same. The current of the second peak returns back to the gun through the ground strap, while the first peak is comprised primarily of displacement current flowing from the parasitic capacitances to

the EUT. Therefore, the current associated with the first peak does not necessarily flow through the ground strap [31].

The EUTs in this dissertation were placed on the HCP separated by an insulating layer. In one configuration, the EUT is not connected to earth ground (i.e., it is battery powered). This configuration is referred to as a mobile setup. In the other configuration, the EUT is connected to the earth ground directly or through another piece of equipment, referred to as a tethered setup. The second peak is much reduced in the mobile setup due to the absence of a low impedance path for current components at low frequencies.

2.2 Modeling approach

The modeling of the contact discharge current in system-level ESD needs the understanding of the test bed, which is the environment of the EUT. To obtain the most accurate solution, full-wave EM simulation is needed [15], [32], [27], but this requires long computation time. The current discharge waveform is a wide-band signal, and the measurement generally has “ripples” on top of a current pulse envelope. These ripples contain valuable information about the test bed. Substituting a VNA for the ESD gun allows one to characterize the impedance of the test bed over the frequency range of interest. The VNA measures the impedance at a constant input power at all selected frequencies, enhancing the accuracy of the measurements. Detailed information of the elements inside the gun is desired to obtain the gun model [23], but it is difficult to characterize the ESD gun using a network analyzer. The ESD gun contains a switch that closes only when a discharge is triggered. Therefore, the frequency-domain S-parameters of the gun must be measured when the switch is closed. If the switch is open, the S-

parameters of the gun cannot be measured without breaking the gun and performing measurements across the switch. Many works model the discharge setup with lumped RLC elements [19], [21], [33]. Due to the large size of the test bed, especially when the low-frequency current components are absent, the lumped RLC models cannot fully replicate the measured waveform. In particular, the ground strap in the setup should be treated as a transmission line [26].

To aid the development of a distributed model of the test bed, the time-domain measurements will be augmented by frequency-domain Z-parameter measurements (here, only one port, thus Z_{11}), obtained using a vector network analyzer (VNA) that can cover the frequency range from 10 MHz to 40 GHz. In essence, one wishes to know the load impedance seen by the ESD gun. To directly measure this quantity, the VNA is outfitted with a probe that accommodates an ESD gun tip. This special probe, referred to as a "mock gun tip," is designed to replicate the actual test setup as closely as possible [34], as shown in Figure 2.5. The mock gun tip consists of a removable ESD gun tip connected to the center conductor of an SMA connector; the shield of the SMA is directly attached to a cable whose length is comparable to that of the gun's ground strap. The far end of this cable is connected to the ground plane, as demanded by the test standard. This ensures that a similar loop area is created and presumably an equivalent inductance.

Z_{11} characterizes the device-under-test connected between the SMA connector's center conductor and its shield; the SMA connector is shown in Figure 2.5. The SMA connector and the coaxial cable which connects the mock gun tip to the VNA are "calibrated out" before the Z_{11} measurement, but the mock gun tip is not de-embedded. Therefore, the gun tip and the "mock ground strap" are part of the device-under-test. It

would not be possible to accurately de-embed the gun tip and ground strap. The EUT does not have a fixed size relative to those of the gun tip and ground strap; thus, their impact on the total impedance "seen" by the gun is variable. In summary, the device-under-test for the Z_{11} measurements includes the gun tip, the ground strap, and everything between the gun tip and the ground plane. The same device-under-test is referred to as the test bed.

The IEC 61000-4-2 test standard [11] specifies that a cable must be used to connect the floor ground plane to the building's power ground; for the Z-parameter measurement, this cable is removed to eliminate ground loops. This cable adds a highly inductive path back to the gun, which conducts much less current than other paths. Current waveforms obtained with and without this cable show little difference.

After the calibration procedure is complete, the various components of the test bed are inserted one at a time, and Z_{11} is measured at each step. The measurements are first performed with a bare test bed, and then with the EUT on the HCP. In this way, the test bed model is constructed in a systematic fashion. Each time a new component is added to the system, the previously extracted model may need to be slightly modified to account for new interactions between parts of the system due to radiative or capacitive coupling. For example, the HCP together with the ground plane below it acts as a low-Q resonator. The field generated by this structure will interact with other components of the test bed, such as the ground strap, affecting their circuit-level representations.

However, at the end of this exercise, the test bed model will be fixed and can be subsequently used without any changes for a variety of different EUTs. Since the objective of this dissertation is to model direct injection through the test bed, the test bed

model does not need to be accurate above a few hundred MHz because the test bed is in series combination with the gun, which filters out frequency components above the mid-100-MHz range. The complete SEED model will represent the system consisting of ESD gun, test bed and EUT.

2.3 Distributed element modeling of the test bed

2.3.1 ESD gun

The modeling process starts with the adoption of the ESD gun model shown in Figure 2.6 and the extraction of its parameters. The model is adapted from the one shown in Figure 2.2. C_{fast} and R_{fast} are used to fit the first peak of the discharge waveform for a 2 Ω target (Figure 2.7). Since C_{fast} and R_{fast} control the higher-frequency portion of the discharge, they should be extracted with a representation of the rest of the setup that is accurate in the same frequency range. Thus, in the simulation model, the target and the ground strap are both represented by their measured Z-parameters; since the gun's ground strap cannot be removed, it is actually the ground strap from the mock gun tip that is measured. In this measurement, the mock gun tip is removed from the setup. The shield of the coaxial cable remains connected to one end of the ground strap, and the center conductor of the coaxial cable that connects to the VNA is in contact with the other end of the ground strap. At low frequencies, the ground strap is equivalent to an inductor, and the target is a 2.2 Ω resistor; while at higher frequencies, these lumped models are not appropriate. Using the Z_{11} representations for ground strap and target noticeably affects

the simulated waveform for the first 10 ns of the discharge, which is the time range over which C_{fast} and R_{fast} are extracted.

Due to the frequency limitation of the VNA, Z-parameters cannot be obtained at frequencies less than 10 MHz. This affects the low-frequency accuracy of the Z-parameter-based ground strap model, which results in a worsened match between simulation and measurement at time points in the range of 20 – 60 ns; see Figure 2.7. To improve the accuracy of this simulation, one would need a model of the ground strap that is based on both the Z_{11} measurements and the lumped impedance obtained at lower frequencies using an LCR meter. However, it is not necessary to go through this exercise since the Z-parameter-based gun strap model is used only for the extraction of C_{fast} and R_{fast}, which control only the high-frequency components of the discharge. The ground strap Z_{11} data are not used in later modeling, since the gun strap is incorporated into the Z_{11} measurement of the whole test bed.

As an additional check on the validity of the model, the ESD gun was discharged into a 510 Ω load formed by ten parallel 5.1 kΩ resistors. The current is measured with a current probe. Using the gun model of Figure 2.6, the discharge waveform was simulated and the result is shown in Figure 2.8, along with the measured waveform. The overall fit to measurement is fairly good. The first peak of the simulated current is higher than the measured one, but the discrepancy is not necessarily due to any shortcoming of the model. The imaginary part of the measured impedance of the target changes its polarity at around 400 MHz, indicating a series resonance caused by the resistors' package capacitance and lead inductance, so it is almost a short termination at that frequency, which will compromise the accuracy of the S-parameter measurement. Since the S-

parameter data are used to represent the target in this simulation, the measurement error could result in simulation overestimating the first current peak, as this consists of frequency components close to 400 MHz.

2.3.2 Bare test bed

The input impedance of the bare test bed, which includes the gun tip, the HCP and the ground strap, is obtained by measuring Z_{11} between the points labeled N1 and GND in Figure 2.9. The mock gun tip probe is used for this measurement. N1 (node 1) is the point where the gun tip connects to the SMA cable, and GND is where the mock ground strap connects to the shield of the SMA cable; the SMA cable is connected to the VNA. The measurement results are plotted in Figure 2.10. A resonance is observed approximately every 70 MHz. The resonant behavior is attributed to the ground strap. A transmission line can capture this resonant behavior, because its impedance is a periodic function of frequency when there is an unmatched load. An empirical model of the test bed is formulated based on the Z-parameter data, and it is shown in Figure 2.11.

To gain insight into the mapping between the elements of the model and the physical test bed and, in particular, to determine the source of the resonances, additional experiments are performed. A longer ground strap cable is connected to the mock gun tip, and the test bed Z_{11} is measured two times: once, with the gun tip at the center of the HCP as before ("A" in Figure 2.12), and once with the gun tip touching the ground plane while the ground strap is pulled tight as indicated in the ESD test specification ("B" in Figure 2.12). Resonance now occurs roughly every 40 MHz, which indicates that the impedance of the test bed is strongly influenced by resonance in the ground strap cable. A

resonance occurs whenever the frequency is such that an integer multiple of half-wavelengths equals the cable length.

A comparison of the curves labeled “A” and “B” in Figure 2.12(b) reveals that the impedance at frequencies above 50 MHz is not sensitive to whether the gun tip is placed on the HCP (open at DC, like a capacitor) or placed on the floor plane (DC short). The HCP and the ground plane both act like the “shield” of the ground strap. At low frequencies, the impedance associated with the coupling from the HCP to its environment contributes significantly to the total impedance of the test bed. This effect is captured by the RLC elements in Figure 2.11. These elements also account for the non-uniformity of the transmission line formed by the ground strap and its environment, which is not captured by the transmission line element in the model.

The Z-parameter data of Figure 2.11 suggest a smaller value for L_{tip} than was extracted when the gun model of Figure 2.6 was fit to the waveform of Figure 2.7. The mock gun tip probe used for Z-parameter measurements includes the physical gun tip, so it is conjectured that part of the L_{tip} shown in Figure 2.6 is actually located inside the gun assembly.

The bare test bed model was derived using frequency-domain measurement data that were obtained without the actual gun body included in the setup. The size of the gun is not negligible, and therefore time-domain current waveforms of gun discharges to the HCP, as shown in Figure 2.13, are used to refine the model. This discharge does not involve any additional object that needs to be modeled. The combined model of the ESD gun and bare test bed is shown in Figure 2.14. The ESD gun model is connected to the bare test bed model at both node 1 (N1) and node 2 (N2). N2 represents the edge of the

HCP. This facilitates the representation of coupling between the ESD gun and the HCP. When the bare test bed and ESD gun models are integrated together, current through the gun's C_{fast} element is directed to N2. Note that while the coupling between the gun and the HCP is considered, coupling between the gun and the floor ground plane is not. Coupling between the gun and ground plane is assumed to be negligible because the gun is centered above the HCP and is small compared with the HCP. Therefore, the E-field lines from the gun will terminate on the HCP. A lumped LC circuit is added between N2 and ground in Figure 2.14 to account for current flow through the test bed back to the gun due to capacitive coupling between the gun and the HCP. The parameters of the lumped LC circuit are based on the geometry of the gun and its height above the HCP.

2.4 System-level ESD current into an EUT

Taken together, the ground plane of EUT and the HCP form a capacitor. The capacitance depends on the geometry of the EUT. Simulation and measurement results are compared for discharges to an EUT consisting of a 13.5-cm by 13.5-cm FR-4 circuit board first described in [35]. The discharge location is at a USB connector shield, which is connected to the ground plane of the EUT. The capacitance between EUT and HCP is estimated based on the area of the circuit board and its height above the HCP, assuming an infinitely large HCP. The effect of parallel-plate and the fringing capacitance are both included. By inserting this capacitor in the current return path, the model can reasonably well predict the current injected into the EUT from the gun, as shown in Figure 2.15. It is observed that the rise time and magnitude of the peak current are not sensitive to the vertical separation of the EUT from the HCP. Different from the current waveform

obtained from discharging into the 2-Ω calibration target, the second current peak is absent. This is expected because, in this mobile setup, the DC current path has a high impedance, consisting of the bleeding resistors. As a result, the second peak is only a small residual current, which decreases as the vertical separation of the EUT from the HCP increases.

When the EUT is placed very close to the HCP, such as a smartphone lying flat on the HCP, the capacitance between the EUT and the HCP is large due to the small spacing. The current waveform measured at the ESD gun tip approaches the one obtained when ESD current is discharged to the HCP directly, as shown in Figure 2.13.

A tethered EUT has a path for the current to return to the gun through the power cord of a DC supply as shown in Figure 2.16. The DC supply used here is HP E3631A. Z-parameter measurement data are used to find the input impedance of the tethered EUT; the results are shown in Figure 2.17. There are two sources for cable resonance, which are the ground strap and the power cord, but the ground strap has the stronger influence, since the wave on the cable of the supply needs to travel a longer distance before returning to the gun and therefore has higher loss. The power cord of the supply mainly contributes a low impedance path at low frequencies.

Due to the bandwidth limitations of the VNA, the precise inductance of the return path through the power supply cannot be extracted from the Z_{11} data; instead, the inductance is estimated based on the loop area formed by the power cord and then its value is refined to match the time-domain waveform. Note that the inductance along the return path through the EUT's power supply does not have a fixed value. A value of 5 μH is extracted when the power supply is directly grounded to the ground plane by connecting

the ground prong of the power cord of the supply to the ground plane with copper tape, and the power is off. A larger value, 8 µH, is extracted when the power supply is grounded at the wall outlet. The result is unsurprising as the loop size is larger in the second case. The simulated waveforms are shown in Figure 2.18. The first current peak is not sensitive to the placement of the tether. In contrast, making the loop area larger results in a lower amplitude of the second current peak with a longer trailing edge.

2.5 Figures

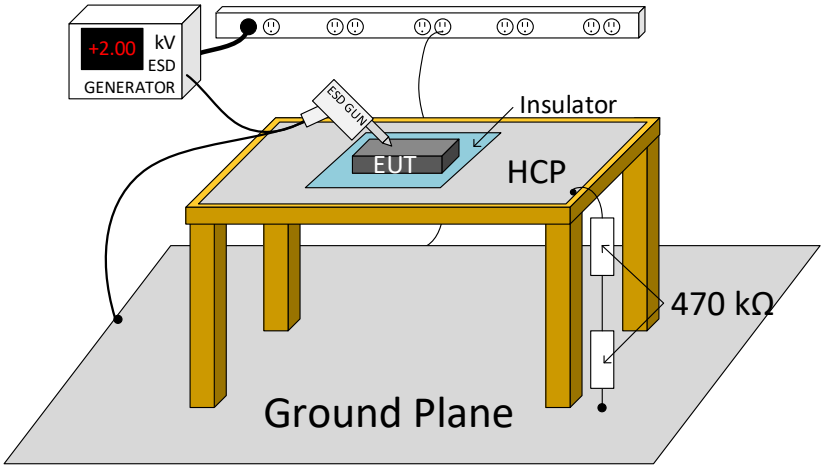


Figure 2.1: IEC 61000-4-2 test setup. The figure is taken from [36].

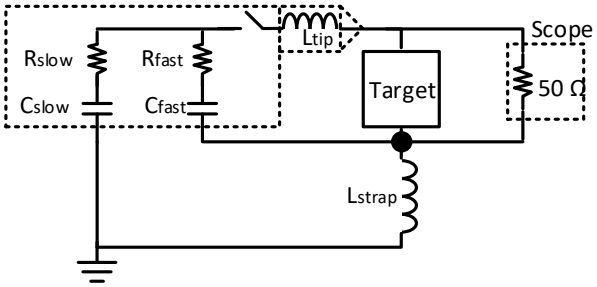


Figure 2.2: Lumped RLC model for IEC 61000-4-2 tester (ESD gun) discharging into a 2 Ω target. C_{slow} and C_{fast} are precharged to the ESD voltage level, typically on the order of kilovolts.

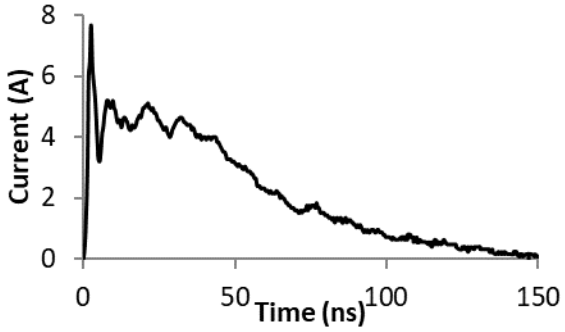


Figure 2.3: Measured current of IEC stress into a 2 Ω target.

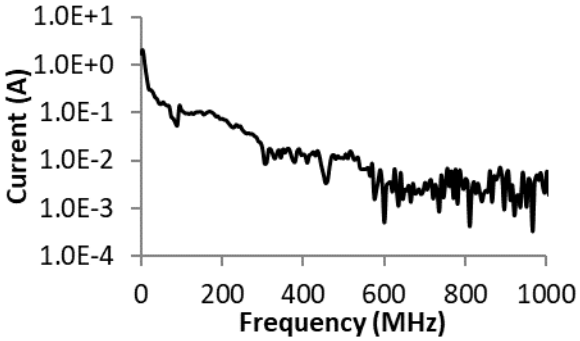


Figure 2.4: FFT of current of an IEC discharge into a 2 Ω target.

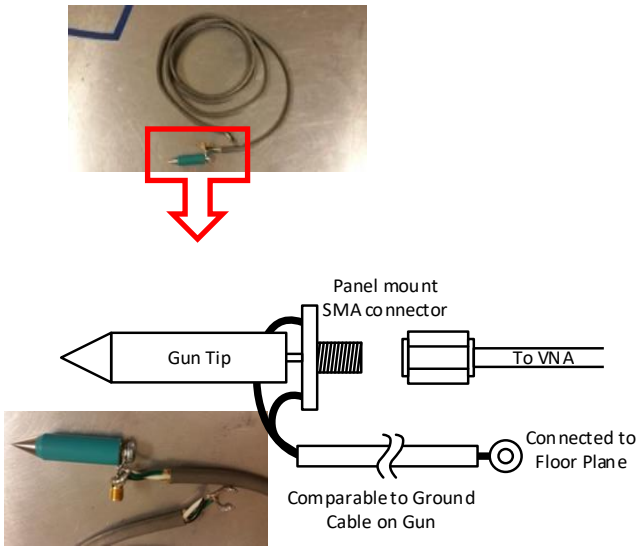


Figure 2.5: Mock gun tip used for Z-parameter characterization of the IEC test setup.

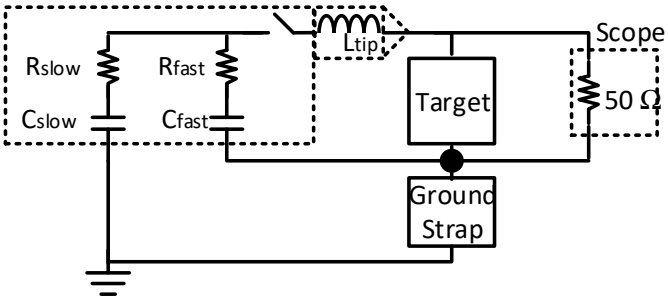


Figure 2.6: Gun model. R_{slow} = 330 Ω, C_{slow} = 150 pF, R_{fast} = 238 Ω, C_{fast} = 5 pF, L_{tip} = 140 nH. Ground strap is described by its measured Z_{11}.

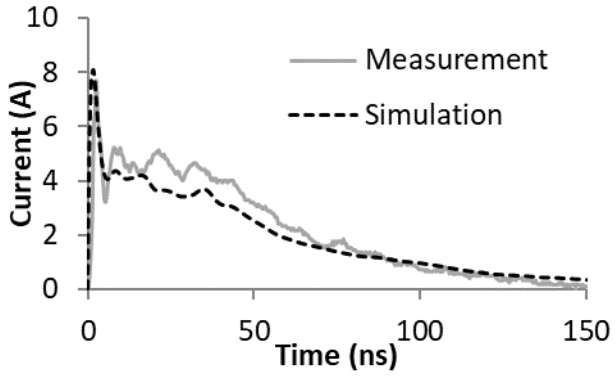


Figure 2.7: Discharge into a calibration target. Measured and simulated current waveforms. The model is shown in Figure 2.6.

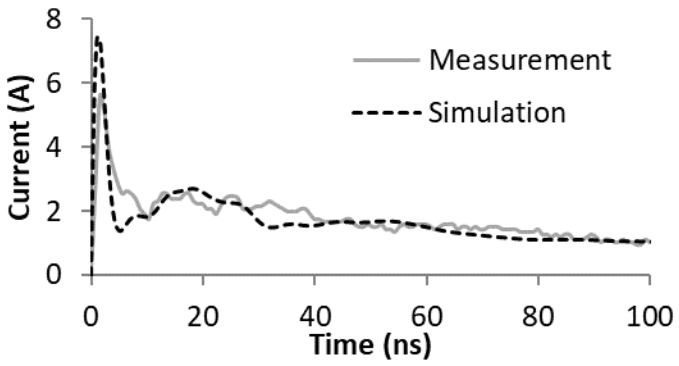


Figure 2.8: Discharge into a 510 Ω target. Measured and simulated current waveforms. The model is shown in Figure 2.6.

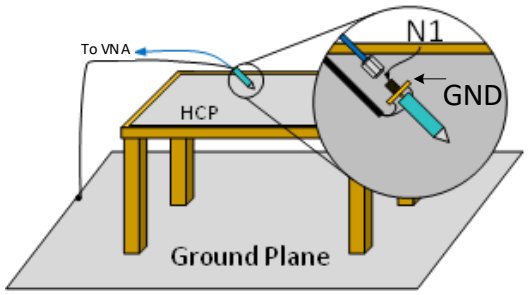


Figure 2.9: Measurement setup of the bare test bed. The VNA measures Z_{11} between N1 and GND.

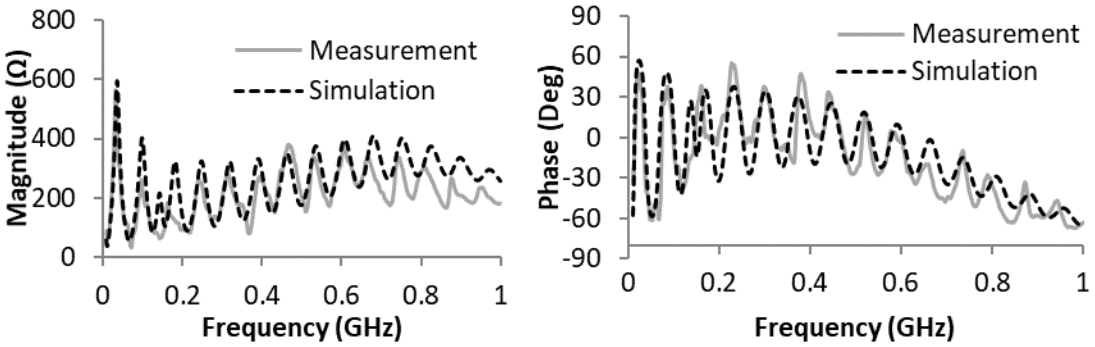


Figure 2.10: Measured and simulated Z_{11} of the bare test bed looking through the mock gun tip probe of the VNA.

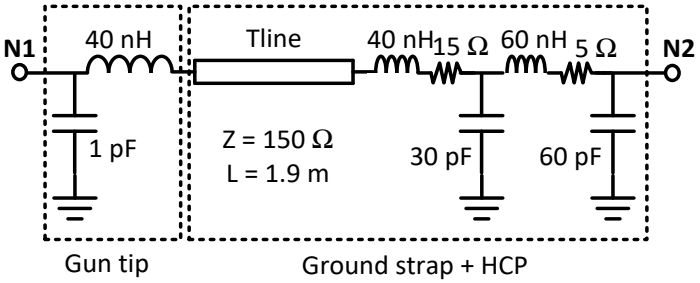
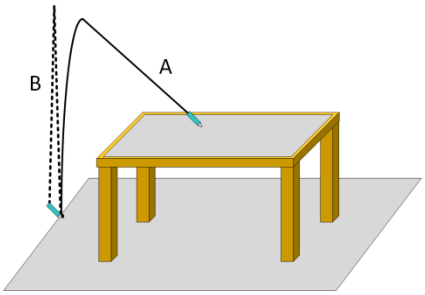
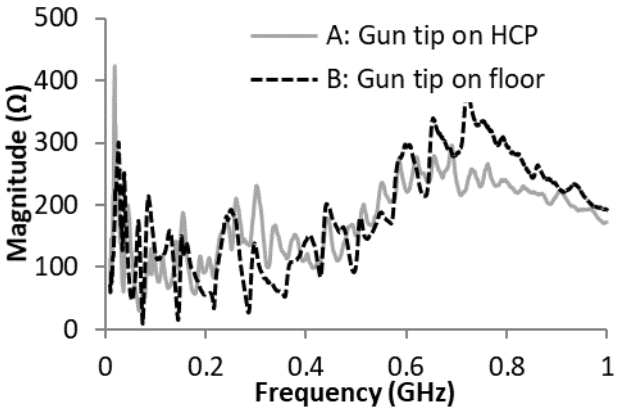


Figure 2.11: Model of the bare test bed with gun tip, HCP and ground strap.



(a)



(b)

Figure 2.12: (a) Test setups for measuring the impedance of the longer ground strap in various positions. (b) $|Z_{11}|$ as seen looking through the mock gun tip probe of the VNA. Ground strap length is longer than that for the dataset of Figure 2.9. Two different test setups are characterized.

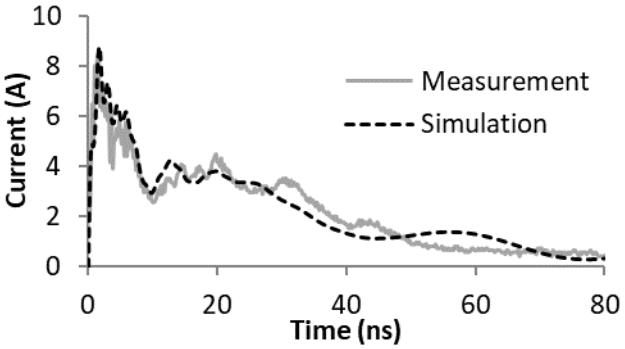


Figure 2.13: Current waveforms for an ESD gun discharge to the bare test bed.

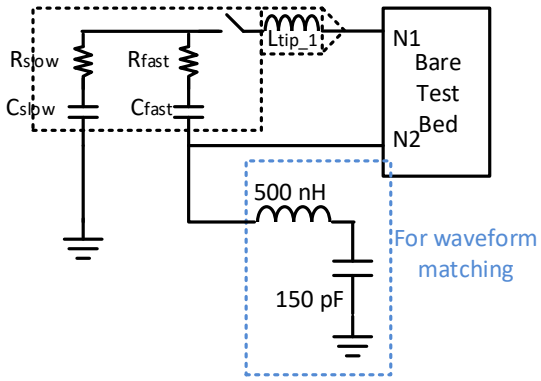


Figure 2.14: Model of gun and bare test bed.

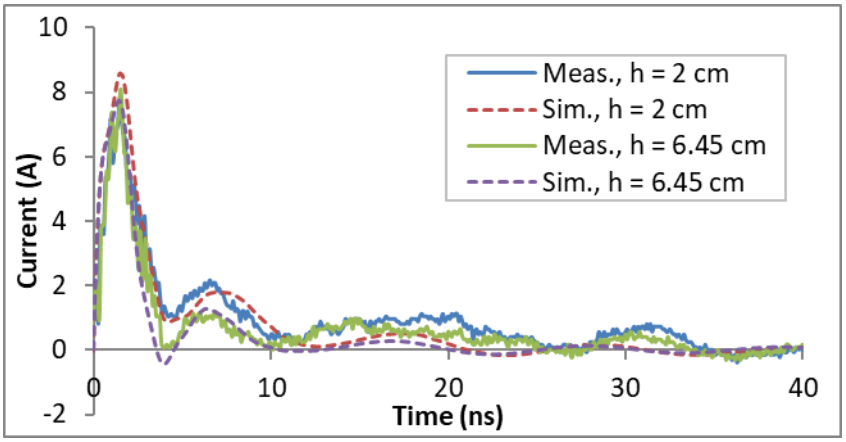


Figure 2.15: Measured and simulated ESD gun discharge current in mobile setup onto the ground plane of a 13.5-cm by 13.5-cm FR-4 circuit board at various heights above the HCP.

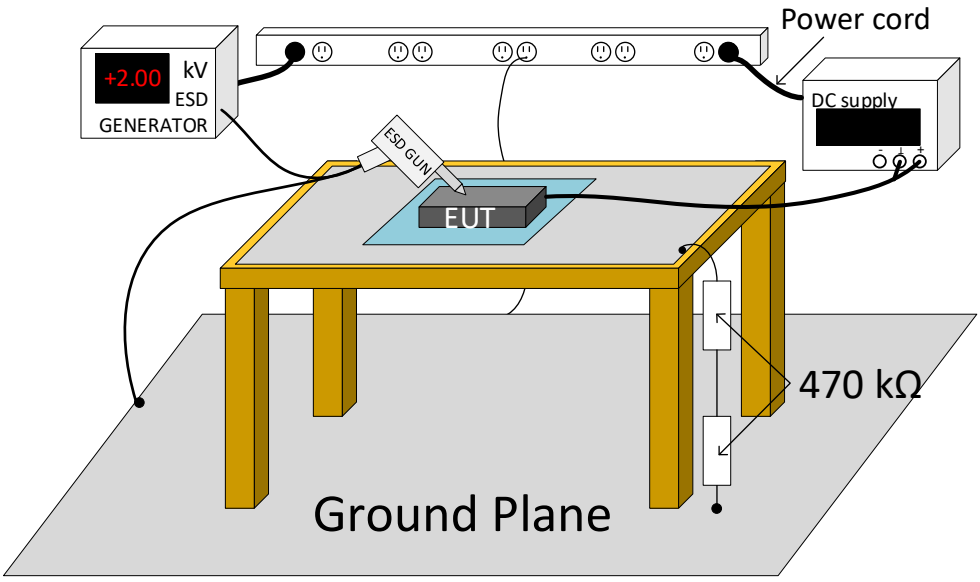
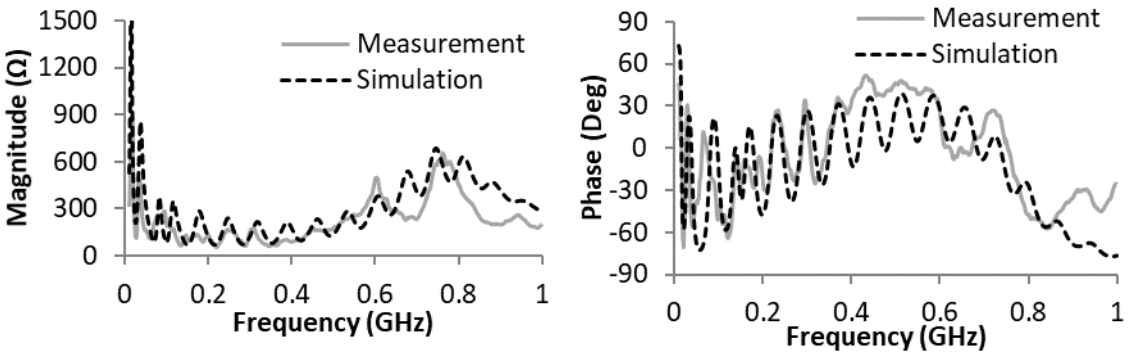


Figure 2.16: The tethered EUT under the system-level ESD test. The ground plane of the EUT is connected to the ground node of a DC supply. The power cord of the DC supply contains a ground wire. In the experiment, the supply is off and the ground wire is plugged into the outlet on the wall or in contact with the ground plane.



(a) (b)

Figure 2.17: Input impedance (a) magnitude and (b) phase seen between N1 and ground for the tethered EUT.

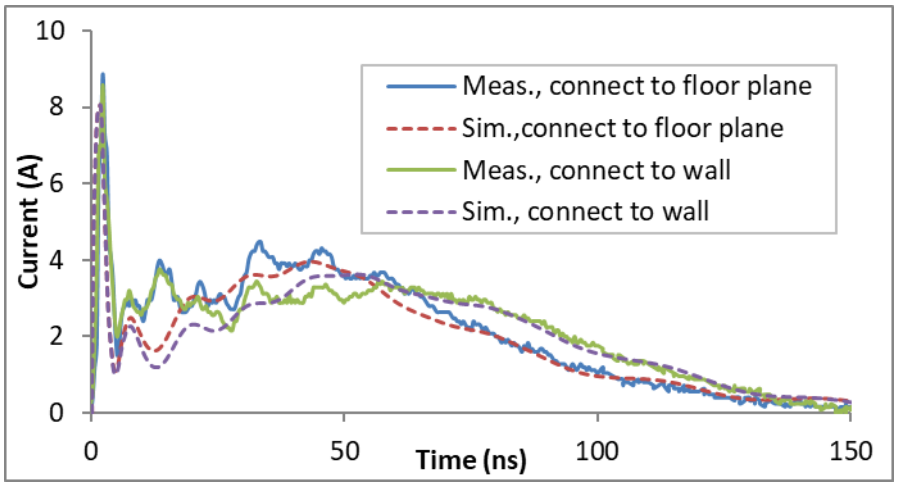


Figure 2.18: Measured and simulated ESD gun discharge current in tethered setup onto the ground plane of a 13.5-cm by 13.5-cm FR-4 circuit board at various tether locations.

CHAPTER 3

INTERFERENCE OF SYSTEM-LEVEL ESD WITH THE OPERATION OF AN IC

System-level ESD can interrupt the normal functionality of the system in many ways. The near-field coupling between the gun and the EUT generates noise at signal traces. The fast-changing current transients also create noise at signal inputs by magnetic coupling and direct injection. The large magnitude of the time derivative of the injected current into the chip presents a problem for packages with large inductances. These packages include most wire-bond ones as well as the flip-chip ones with long traces of package routing. The on-chip ESD protection directs the ESD current to the on-chip PDN, and the inductances of the package connecting the on-chip PDN to the system's PDN lead to a difference of power and ground potential between the chip and system. This means that inputs that are referenced to the system ground may not be interpreted correctly by the IC which has a different ground reference potential, even if the input signal does not have noise coupled onto it. These effects are described in [35] and [37].

Even if the printed circuit board (PCB) design provides good isolation between traces, eliminating magnetic and capacitive coupling between traces, the signal inputs are still subject to noise coupling at the package level, including the magnetic coupling from supply/ground bond wires since they are part of the main current return path.

3.1 Case study of a 65-nm CMOS test chip

A test chip was fabricated in 65-nm CMOS technology to investigate the effect of ESD on signal integrity. The power supply for the IO circuits, VDDIO, is 2.5 V, while the rest of the circuitry uses a 1.2 V supply, VDD. The two supplies share a common ground net, VSS. Most of the IOs for the experiments described in this section are located along one edge of the chip, as shown in Figure 3.1. There are two pairs of VDDIO-VSS pads at the two corners of the chip, and two more VSS pads are located five pads away from either of the VDDIO pads. Under the VDDIO pads are located rail clamps for the VDDIO domain. The VSS pad cells at the corners contain decaps for the VDDIO domain. The IO circuitry is described in Table 3.1. Many of the IOs contain a glitch detector (GD) to capture disturbances during ESD, specifically those in which the signal voltage crosses the switching threshold of the input circuitry. One of the IOs contains an out-of-range-error detector (ORED) [38] which can detect if the input goes above the on-chip VDDIO or below the on-chip VSS potentials. Potentially, the ORED output signal could be used to alert the system to the occurrence of ESD, thereby enabling it to take prompt corrective action. One of the IOs contains multiple low-pass filters; these act upon the input signal in parallel. Specifically, there are four analog RC filters with time constants of 3.2 ns, 10 ns, 32 ns, and 100 ns, as well as a digital filter driven by a 100 MHz clock that is generated on chip. The filters are in the VDD domain. The filters' outputs may be used to discern the time duration of ESD-induced glitches. For the input with the digital filter, timing between the glitch and the clock edge is important, and this effect would result in a higher rate of glitches to be observed than the input after the 100-ns analog filter.

Two PCBs were fabricated for this chip, as shown in Figure 3.2, to study the effect of board-level coupling on the likelihood of glitch occurrences during ESD. Both boards contain traces that connect the IO3, 4, 5, 7 and 8 pins to the test pads at the board edge. In the experiment, the ESD current is injected to one of the test pads. The number on the traces refer to the number of the IOs they are connected to; e.g., trace labeled “2” is connected to IO2. On Board 1, the traces are close to each other (8 mil spacing over a distance of 2 in); on Board 2, the traces are far apart and isolated from one another by a big metal shape connected to the ground plane so that the coupling effect between these traces are minimized. When an IO is configured as a victim subject to the noise from a neighbor being stressed, the IO is connected to a trace on the back side. All the back-side traces are connected to a single circuit that generates the input to the IOs. This circuit consists of a switch followed by a low-pass RC filter. The switch connects the input to the VDDIO plane or the ground plane on board. The back-side traces on Board 2 are connected to the chip at a closer location than those on Board 1. This helps to further filter the disturbance from the coupling of the ESD gun to the input traces.

3.2 Measurement results of data upsets on the 65-nm test chip

ESD gun discharges were applied at the test pads, using a mobile configuration. Table 3.2 shows the comparison of the minimum IEC levels needed to induce a glitch captured by the GDs on the two boards when discharging to the test pads connecting the IOs. When the test chip is mounted on Board 2, ESD currents to an IO induce fewer glitches at a neighboring IO than they do on Board 1, but the overall robustness, which is mostly

under 2 kV, still needs further improvement. The Board 2 design minimizes the noise contribution from board-level coupling, but the noise is still coupled through bond wires in the package. The voltage induced on bond wires by fast changing ESD current leads to a potential difference between ground reference on-board and on-chip, and signals referenced to board ground are not correctly interpreted by the chip. Furthermore, the results suggest that the package and chip-level effects produce noise that is of comparable magnitude to that generated on the circuit board. Coupling between bond wires, which is mostly inductive coupling, depends on the distance between the victim IO (i.e. the IO experiencing glitches) and the zapped IO (the IO receiving the ESD current). The general trend is that IOs progressively farther from the zapped IO are less likely to experience a glitch. IO8, the IO on the far right, with its bond wire orthogonal to those of the other IOs in VDDIO domain, is the most robust against glitches. The distance between the victim IO and the VDDIO-VSS pair is another significant factor, since the bond wires connected to the power and ground also belong to the major current path. For glitches that are caused by the difference between off-chip and on-chip supply and ground potentials, the impact should increase as the IOs get farthar away from the VDDIO-VSS pair, since the current directed to VDDIO or VSS by the ESD protection at the stressed IO generates a voltage drop along its path toward the VDDIO or VSS pin with the bus resistance of the path. In addition, on this test chip, the victim IOs and the stressed IOs are located within the same two VDDIO-VSS pairs except IO8. Out-of-range errors, as shown in Table 3.2, are caused by the same mechanism as glitches. These errors caught by the ORED also start to appear well below 2 kV.

Table 3.3 shows the minimum IEC level needed to trigger a glitch when the input is low-pass filtered before being received at the GD. For higher ESD levels, the results are shown in Table 3.4. It is observed that glitches occur for a range of ESD levels and the likelihood of detecting a glitch does not increase monotonically with the ESD level. It is also noted that the results provided by the GD that follows the 100-ns analog filter do not agree with those from the GD that follows the digital filter. Specifically, +0→1 glitches are reported by the GD that follows the digital filter at ESD levels above 3.5 kV but not by the GD that follows the 100-ns analog filter; furthermore, +1→0 glitches at 3 kV and 6 kV are only reported by the GD that follows the digital filter. In addition, it is expected that if a GD that follows an RC filter reports a glitch, all the other GDs that follow filters with smaller RC time constants will also report the glitch. However, +1→0 glitches reported by the GDs that follow the analog (RC) filters do not show this consistency. Positive ESD currents into the chip also induce many more upsets than do negative ESD currents, but noise induced by magnetic coupling between the traces and bond wires tend to cause glitches with comparable likelihood for both polarities of ESD currents. This implies that a mechanism other than magnetic coupling contributes to the occurrence of glitches.

It is suspected that the VDD supply on-chip collapses at ESD levels over 2 kV and that this is one of the sources of the anomalous results, specifically, the nonmonotonic relationship between ESD level and glitch detection, the inconsistent results between the GD which follows the 100-ns analog filter and the one that follows the digital filter and the dependence on the polarity of discharge. The input signal generated off-chip enters the chip through a Schmitt trigger and a level shifter in the VDDIO domain, and then

through buffers and a filter to the GD in the VDD domain. It is not clear which part of the circuitry is affected by the global on-chip supply noise. Based on the dependence of observed glitch on ESD current polarity, supply noise in the VDD domain is likely to cause loss of function of these GDs, which will be shown in Chapter 4.

Different from the results shown in Table 3.4, the results in Table 3.3 show a monotonic relationship between ESD level and detected glitches and the analog and digital filters appear to work equally well. Furthermore, the glitches have only a weak dependency on the polarity of the discharge. This observation suggests that the supply noise in the VDD domain is not strong enough to significantly disturb the function of the GDs below 2.5 kV, and that the GDs are accurately reporting on the occurrence of glitches. No glitches are reported for inputs that pass through RC filters with a time constant of 10 ns or longer which suggests that the noise duration is less than 10 ns.

Previous studies [35], [36] have shown that adding a transient voltage suppressor (TVS) to the signal line that may be subject to contact discharge can significantly reduce the impact of ESD on other inputs, since the TVS can sufficiently shunt the ESD current away from entering the IC. Similar experiments were performed on this system, where a TVS was added close to the test pad connected to IO4, and the vulnerability of the other IOs to the noise induced by contact discharge at this test pad is compared with the experiments when there is no TVS. The results are shown in Table 3.5.

The TVS used is rated for 15 kV contact IEC protection for 2.5 V IOs. The trigger voltage for this TVS is +3.1 V/-0.7V according to the data sheet, which is slightly lower than the on-chip protection in both positive and negative ESD. The TVS does increase the minimum IEC level to cause a glitch in almost all the cases, but the improvement has

polarity dependency, with limited effectiveness for -0→1 (negative ESD causing 0→1 data transition) glitches and +1→0 glitches (positive ESD causing 1→0 data transition). The reduced improvement compared with previous work indicates that for low voltage IOs with a reduced noise margin, the TVS has a limited effect on preventing soft input data errors during system-level ESD. It has been shown in [37] that -0→1 and +1→0 glitches are induced by the leading edge of the first current peak of the discharge. The turn-on speed of the TVS is finite, and the induced voltage at the package inductance of the TVS increases the total voltage across this component. Since the trigger voltages of the TVS and the ESD protections at the IOs are similar, the TVS has limited capability to instantly shunt the current away from the IO at the leading edge of the ESD current. Once the current enters the IO, the fast rate of the current change results in the glitches. After the leading edge, the TVS is on and most of the current is discharged through it. Therefore, the decreasing magnitude of the discharge current induces a lower voltage across the package inductances of the chip than the case without the TVS, and the chip becomes more robust to glitches.

3.3 Summary of the observations

The measurement results illustrate the difficulties to prevent soft failures on the 65-nm test chip. It is suggested that the glitches due to the magnetic coupling between traces and bond wires are widespread among the low-voltage IOs due to their reduced noise margin, and the disturbances caused by the coupling do not immediately vanish when the victim IO moves away from the stressed one. The coupling of the package inductances is strong enough to trigger glitches below 1 kV. The TVS at the stressed IO may not be as efficient

to protect the signal integrity of the victim IOs as the case with high-voltage IOs. The power integrity starts to be compromised below 4 kV with the low supply voltage on-chip.

3.4 Figures and tables

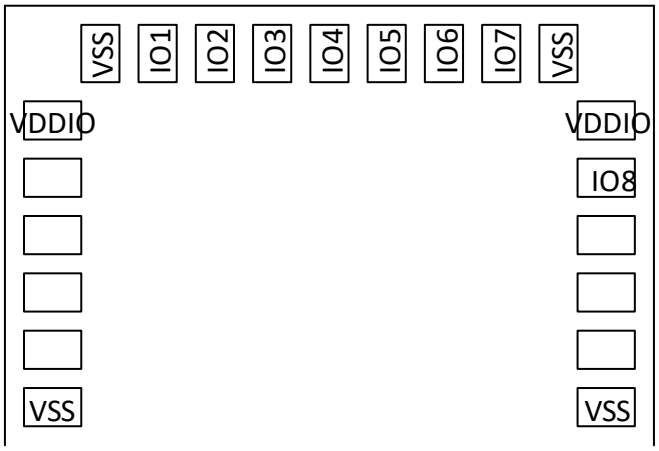
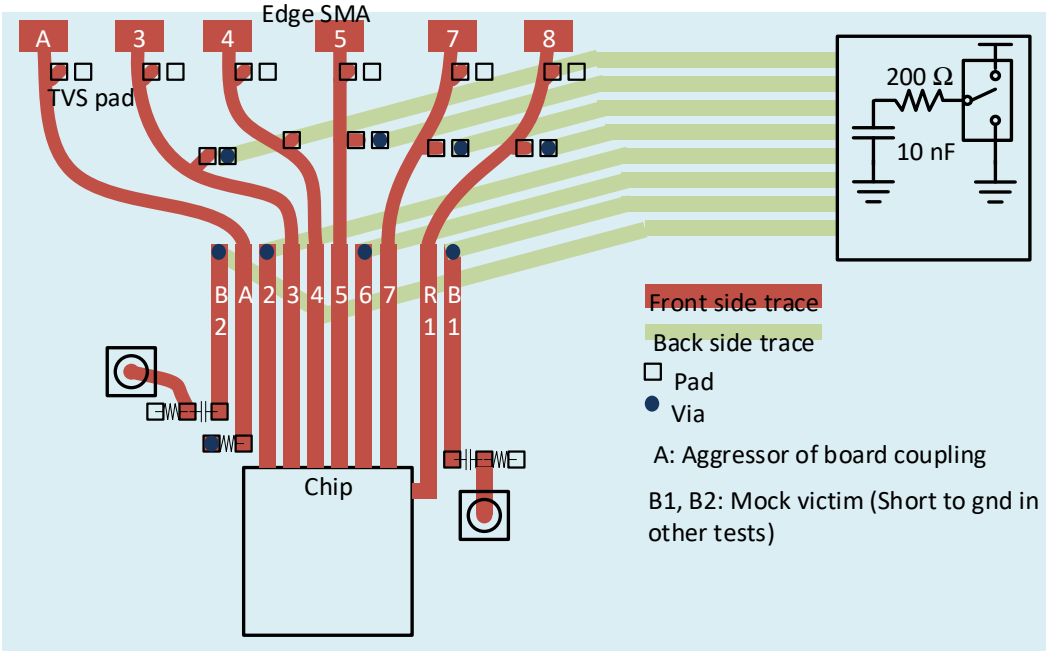


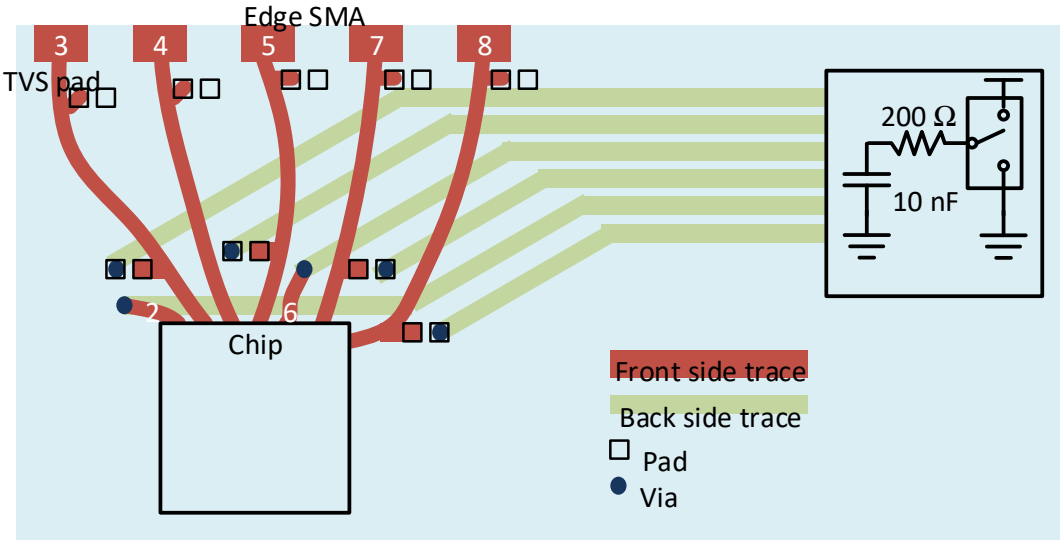
Figure 3.1: Pad assignment of the 65-nm test chip.

Table 3.1: Description of 2.5 V IOs on the 65-nm test chip. All receivers have a Schmitt trigger front-end except for the one at IO3.

	ESD protection level (HBM)	Circuitry
IO1	8 kV	Receiver
IO2	2 kV	Receiver with GD
IO3	8 kV	Receiver with ORED attached.
IO4	8 kV	Transmitter
IO5	8 kV	Receiver whose input is sent to multiple filters
IO6	2 kV	Receiver with GD
IO7	8 kV	Receiver with GD
IO8	8 kV	Receiver with GD



(a)



(b)

Figure 3.2: Two board designs with different trace layouts for the 65-nm test chip. The front side traces are always connected to the IOs. (a) Traces on the front side are closely coupled to each other; (b) traces on the front side are isolated from each other by shapes connected to the ground plane. A TVS may be placed on board across the TVS pads. An IO is configured as a victim when a 0-Ω resistor at the two pads close to each other connects the IO to the back side trace; the IO is configured is configured as a zapped IO when it is not connected to the back side trace.

Table 3.2: Minimum IEC level (kV) to trigger a glitch or out-of-range error with more than 50% possibility when discharging at test pads connected to IO3 and IO7 five times for the 65-nm test chip in the mobile setup. ORED_H: input voltage is higher than VDDIO voltage; ORED_L: input voltage is lower than VSS voltage.

Board 1	0→1				1→0			
Stressed IO	Positive		Negative		Positive		Negative	
	IO3	IO7	IO3	IO7	IO3	IO7	IO3	IO7
IO2	0.5	0.5	0.2	0.5	0.5	0.5	0.2	0.2
IO5	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
IO6	1	1	1	0.5	0.5	0.5	0.5	1
IO8	1	0.2	1	0.2	1	0.2	1.5	0.2
ORED_H	NA	0.5	NA	0.5	NA	0.2	NA	0.2
ORED_L	NA	0.2	NA	0.2	NA	0.5	NA	0.5

Board 2	0→1				1→0			
Stressed IO	Positive		Negative		Positive		Negative	
	IO3	IO7	IO3	IO7	IO3	IO7	IO3	IO7
IO2	0.5	1*	0.5	1.5	0.2	1	0.2	1
IO5	1	1	0.5	1	0.5	1	0.5	1
IO6	1	0.5	1	0.5	0.5	1	0.5	0.5
IO8	2	3	1.5	2	1.5	1.5	1.5	2.5
ORED_H	NA	0.5	NA	1	NA	0.2	NA	0.2
ORED_L	NA	0.2	NA	0.2	NA	1	NA	1

*Discharging into IO7 at +1.5 kV does not cause IO2 to upset with more than 50% possibility.

Table 3.3: Minimum IEC level (kV) to trigger a glitch in more than 50% of trials when the signal is filtered before reaching the GD circuit. Discharges were applied to test pads connected to IO3 of the 65-nm test chip on Board 2 in the mobile setup.

Board 2	0→1				1→0			
Stressed IO	Positive		Negative		Positive		Negative	
	IO3	IO7	IO3	IO7	IO3	IO7	IO3	IO7
0 ns	1	0.5	0.5	0.2	0.5	1	0.5	1
3.2 ns	1	1	1.5	2	2	>2.5	2.5	>2.5
10 ns	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5
32 ns	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5
100 ns	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5	>2.5
Digital	>2.5	>2.5	>2.5	>2.5	2.5	>2.5	>2.5	>2.5

Table 3.4: Same experiment as for Table 3.3 except that IEC levels are higher: ± 3 kV, ± 3.5 kV, ± 4 kV, and ± 6 kV. The ESD levels at which glitches are noted are listed in the table.

Board 2	0→1		1→0	
	Positive	Negative	Positive	Negative
3.2 ns	3, 3.5, 4, 6	3.5, 4, 6	3, 3.5, 4, 6	3.5, 6
10 ns	none	none	3, 3.5, 4, 6	none
32 ns	3.5, 4	none	3, 3.5, 4	none
100 ns	3	none	3.5, 4	none
Digital	3, 4, 6	none	3, 3.5, 4, 6	none

Table 3.5: Minimum IEC level (kV) to trigger a glitch or out-of-range error with more than 50% possibility when discharging to the test pad connected to IO4 with and without TVS protection on the 65-nm test chip in mobile setup. ORED_H: input voltage is higher than VDDIO voltage; ORED_L: input voltage is lower than VSS voltage.

Board 1	0→1				1→0			
	Positive		Negative		Positive		Negative	
	w/o TVS	w/ TVS	w/o TVS	w/ TVS	w/o TVS	w/ TVS	w/o TVS	w/ TVS
IO2	0.5	>2	0.2	1	0.5	1.5	0.2	>2
IO5	0.2	>2	0.2	0.5	0.2	0.2	0.2	1.5
IO6	0.5	>2	0.5	1	0.5	2	0.2	>2
IO7	0.5	>2	0.5	1.5	0.2	1	0.2	>2
IO8	0.5	>2	1	>2	0.5	2	0.5	>2
ORED_H	0.5	2	0.2	1	0.2	0.2	0.2	0.2
ORED_L	0.2	0.2	0.2	0.2	0.2	1	0.5	2

Board 2	0→1				1→0			
	Positive		Negative		Positive		Negative	
	w/o TVS	w/ TVS	w/o TVS	w/ TVS	w/o TVS	w/ TVS	w/o TVS	w/ TVS
IO2	1	>2	1	1.5	0.2	1.5	1	2
IO5	0.5	>2	0.5	1	0.2	1	1	>2
IO6	1	>2	1	1.5	0.5	1.5	1	>2
IO7	1	>2	1	>2	0.5	>2	1	>2
IO8	1	>2	1	>2	0.5	>2	1	>2
ORED_H	0.5	2	0.5	1.5	0.2	0.5	0.2	0.5
ORED_L	0.2	0.2	0.2	0.5	0.5	2	0.5	>2

CHAPTER 4

POWER INTEGRITY SIMULATION AND MEASUREMENT

Previous experiment observations (see Table 3.4) have suggested that large amplitude noise may be induced on the on-chip PDN during ESD. This presents a global threat to the proper functioning of the IC rather than having the threat confined to the IOs subject to the ESD current injection or their neighbors. For cases where the large-amplitude ESD current enters the IC with a non-ideal system PDN, this is very likely to occur. If it is desired to detect soft errors and correct them on the hardware or software level, it is important to understand how the on-chip supply is affected in order to design robust circuitry to work in the presence of the supply disturbance or to have detection circuitry to identify such disturbances.

ESD currents easily get shunted to all power and ground nets on-chip since all these nets are connected through ESD protection circuits [39]. Figure 4.1 shows the current path through two on-chip power domains when a negative ESD occurs at an IO in the VDDIO domain. Another supply domain, VDD, is connected to the VDDIO domain through APDs linking VSS to VSSIO. In Figure 4.1, VSS and VSSIO are both connected to the system ground.

Due to the inductances of the package, when ESD current through an IO is directed to the on-chip power or ground net, the voltage on that net is decoupled from the

corresponding power or ground net on-board. A portion of the noise induced on one rail (power or ground) is converted to common-mode noise on the other rail by the on-chip decap; like the first rail, the second rail is isolated from the dc planes on the board by the package inductance. In summary, both the on-chip power and ground nets are affected, independent of which net the ESD protection at the IO directs the ESD current to. The on-chip decap may not be large enough to maintain the normal supply voltage on-chip; the decap may even discharge during ESD, which is referred to as supply collapse [39], [40]. This phenomenon is of particular concern for wire-bond packages, for which the package inductance is usually several nanohenries. System-level ESD currents which easily rise to several amps within 1 or 2 ns will result in several volts across the bond wires. This high amplitude ground bounce can forward bias one of the two diodes in the APD, and then the APD injects a large amount of current from one on-chip ground net to the other, affecting another power domain. The magnetic coupling between bond wires also causes excessive current in and out of the power and ground nets and generates supply fluctuations.

With fast rise and fall times, system-level ESD usually results in noise voltage transients with bipolarity. Therefore, a situation in which the supply voltage drops below its nominal value (under-voltage) and one in which supply voltage rises above (over-voltage) are both expected to occur. The under-voltage transients probably have a larger impact than the over-voltage ones.

The influence of system-level ESD currents on power integrity can be predicted with circuit simulation. With the accurate representation of on-chip supply voltage fluctuation transients, the performance of circuits can be understood and their outputs can be

correlated to the actual fluctuation in experiments. This is especially important for the detectors that are to identify the ESD transients.

The circuit simulation requires the accurate input of the ESD current. The model shown in Chapter 2 gives an estimation of the system-level ESD current into the IO. The next task is to describe the ESD current division between the multiple paths through the on-chip PDN and the off-chip PDN. The model of the off-chip PDN needs to at least include the package and off-chip decaps, both accompanied by inductances. There have been many studies on the modeling of the PDN to characterize supply fluctuations caused by simultaneous switching noise and electromagnetic emission [41], [42], [43]. The off-chip PDN design to minimize the self- and transfer-impedance has been shown to improve performance in system-level ESD as well [44]. The model of the on-chip PDN needs to at least include the bus resistance of the power and ground nets, the on-chip decaps, the rail clamps, the reverse diodes and the APDs. Component models used in the simulation should represent any nonlinearities. On-chip decaps consisting of MOSFETs are modeled as nonlinear elements in this dissertation. Some off-chip decaps and inductances in the PDN also have nonlinearities due to an excess of the voltage across them or self-heating, but these effects are not covered in the dissertation.

4.1 Supply fluctuations of a generic circuit during ESD

4.1.1 Supply fluctuations in a single power domain

Supply fluctuations are mainly caused by a large inductance (several nanohenries) in the PDN. When the ESD current injected to an IO is directed to the PDN by the ESD protection at the IO, the rising and falling edges of this current induce voltages at the inductances of the PDN. However, it is not necessary to eliminate the inductances in the PDN, nor is it sufficient for the PDN inductances to decrease in order to eliminate supply fluctuations. As a simplified situation, consider the case of a chip that has only one power domain VDDIO. There will be no fluctuation of the on-chip supply voltage if condition (4.1) is satisfied, since the off-chip supply voltage is usually well-maintained by the off-chip decap.

$$L_{VDDIO}\frac{di_{VDDIO}(t)}{dt} \approx L_{VSSIO}\frac{di_{VSSIO}(t)}{dt} \tag{4.1}$$

where L_{VDDIO} is the equivalent inductance of the package connected to the VDDIO net, L_{VSSIO} is the equivalent inductance of the package connected to the VSSIO net, and i_{VDDIO} and i_{VSSIO} are the currents through the VDDIO and VSSIO nets out of the chip respectively. Since the magnitude of the ESD current can be much larger than the normal current consumption of the chip,

$$i_{VDDIO}(t) + i_{VSSIO}(t) = i_{ESD}(t) \tag{4.2}$$

where $i_{ESD}(t)$ is the total ESD current injected to the IO. These two conditions suggest that the on-chip decap and the rail clamp, which are the main current paths between the

VDDIO and VSSIO nets during ESD, should help to distribute the ESD current between the two nets to reach similar voltages across L_{VDDIO} and L_{VSSIO}. On the other hand, if the on-chip decap and rail clamp are fixed, reducing L_{VDDIO} and L_{VSSIO} will not necessarily result in improved power-integrity during ESD, if the currents through L_{VDDIO} and L_{VSSIO} are unbalanced (unless, of course, the inductances can be made very small).

The amount of on-chip decap plays a significant role for the on-chip power integrity during ESD. Figure 4.2 illustrates a case when there is an ESD current i'_{esd} directed to v_{ss}, probably from a bottom diode at an IO or the APD. The disturbance induced on $(v_{dd} - v_{ss})$ is assumed to be negative so that the rail clamp remains off. Based on the schematic shown in Figure 4.2, the ESD current will induce an amount of supply fluctuation given by

$$\frac{v_{dd} - v_{ss}}{i'_{esd}} = \frac{sL_{VSS}}{1 + \frac{Z_{off-chip}}{Z_{on-chip}}} \tag{4.3}$$

where

$$Z_{off-chip} = \frac{1}{sC_{off-chip}} + s(L_{VDD} + L_{VSS}) + R_{off-chip} \tag{4.4}$$

$$Z_{on-chip} = R_{load} || \frac{1}{sC_{on-chip}} \tag{4.5}$$

The amount of supply fluctuation needs to be small, suggesting that the magnitude of $Z_{off-chip}/Z_{on-chip}$ be large, or that sL_{VSS} be small. L_{VSS} is the package inductance and it cannot be made negligibly small in some designs. Therefore, it is necessary to control the ratio between $Z_{off-chip}$ and $Z_{on-chip}$. $Z_{off-chip}$ is usually very small given the amount of off-chip decap. It is desired to have the magnitude of $Z_{on-chip}$ be comparable to the

magnitude of $Z_{off-chip}$ at frequencies of interest during system-level ESD. For a direct contact discharge, the edge of the first ESD current spike contains components at several hundred megahertz. In most designs, $\left|\frac{1}{sC_{off-chip}}\right|$ is negligibly small in this frequency range. R_{load} varies from design to design, but it is usually in the range of several hundred ohms to several hundred kiloohms, which is large. If $\left|\frac{1}{sC_{on-chip}}\right|$ is not sufficiently small, Condition (4.3) indicates that differential mode noise will appear on the supply. Physically, this occurs because there is more current through L_{VSS} than L_{VDD} and, consequently, different voltages are induced across the two inductors.

The rail clamp also affects the on-chip power integrity. For example, when a positive ESD current is injected to an IO with dual-diode protection, the current is directed to the on-chip power net from where it has multiple return paths to the system ground. The current may return to ground through the package inductances connected to the power net and the off-chip decap, or it may flow through the on-chip decap and the rail-clamps to the package inductances connected the ground net. When the on-chip supply voltage rises beyond the turn-on voltage of the rail clamp, the rail clamp turns on and directs a larger portion of the current to the ground net. The rail clamp will be kept on until the supply overvoltage diminishes. Without a rail clamp or a large on-chip decap, a larger fraction of the current exits the chip through the supply bond wires, and when the ESD current starts to decrease, the supply under-voltage transient is exacerbated by the unbalanced current distribution. Therefore, an efficient rail clamp can help reduce under-voltage transients that immediately follow an over-voltage one. This phenomenon happens for the first current peak entering the IC during the IEC test.

The minimum on-chip supply voltage during the fluctuation may not monotonically increase with the ESD level, due the nonlinear behavior of the rail clamp. In power-on ESD, the I-V curve of the rail clamp is close to a piecewise linear function, with decreasing equivalent resistances at higher currents as shown in Figure 4.3. For the ESD current directed from an IO to the power net, an increasing fraction of this current goes through the rail clamp rather than the supply bond wires as the ESD level is increased, and therefore more of the current exits the chip through ground bond wires. This may decrease the amplitude of the under-voltage transient.

The rail clamp also turns on during negative ESD at an IO. The bottom diode of the IO directs the current to VSSIO, and the current leaving the chip through the VSSIO pin induces a ground bounce, which causes an over-voltage transient of the supply voltage at the leading edge of the current and turns on the rail clamp. As the ESD level increases, the rail clamp takes an increasing fraction of the ESD current, which increases the current through the bond wires connected to VDDIO bus. As a result, there is a more balanced split of the ESD current through the supply and ground bond wires at higher ESD levels. If the trailing edge of the negative ESD current immediately follows the leading edge, the decrease of the ESD current induces voltages on the supply and ground bond wires that are of closer magnitudes at higher ESD levels. As a result, the amplitude of the under-voltage transient is decreased.

4.1.2 Interaction of multiple power domains

The supply domains that are connected to the IO (stressed) domain through APDs also experience ESD-induced noise; whether the supply voltage fluctuation begins with an

under-voltage transient or an over-voltage one depends on the voltage on the ground bond wires.

The circuit shown in Figure 4.4 is simulated to study the effect on the supply voltage of an ESD current that is directed to the power or ground net by the protection circuitry at an IO. The simulation includes the on-chip decap, the off-chip decap, the package inductances and the supply clamp, which is a parallel combination of the rail clamp and reverse diode. The I-V curve of the supply clamp is shown in Figure 4.5. Positive ESD current is assumed to be directed to the power net through the ESD top diode at the IO, and negative ESD current is directed to the ground net through the ESD bottom diode. The waveform of the ESD current is sketched in Figure 4.6, which represents the first peak of the current compliant to the IEC 61000-4-2 test standard. In the simulation, values of C_1, R_1, and I_{ESD} are varied to study the influence of the on-chip decap, the off-chip decap and the on-resistance of the rail clamp on the amplitude of the supply fluctuation. The results are shown from Figure 4.7 to Figure 4.10. The amplitude of on-chip VSS potential is also shown as a metric of noise injection to other power domains.

Figure 4.7 indicates that the maximum and minimum supply voltage during system-level ESD has a strong dependence on the amount of the on-chip decap if it is below 1 nF. If the on-chip decap is small, the on-chip supply voltage drops to a value that is too low to maintain the function of the IC. Figure 4.8 and Figure 4.9 shows that, especially at large amplitudes of ESD currents, an efficient rail clamp with a small on-resistance can increase the minimum on-chip supply voltage and helps with power integrity. Figure 4.10 confirms that the minimum supply voltage is not monotonically decreasing with the increasing ESD current, as has been discussed previously. The amplitude of voltage

fluctuation on VSS is sensitive to the on-resistance of the rail clamp and increases with the magnitude of the ESD current.

Figure 4.11 shows a circuit to be simulated to study the supply fluctuation of a domain when the ESD current is discharged to an IO in another domain on the same IC. In this case, current is injected to an IO in the VDDIO domain and the amplitudes of supply fluctuation of the VDD domain are shown with various amounts of the on-chip and off-chip decap and package inductance. VSS and VSSIO are connected by APDs. Figure 4.12 illustrates that several nanofarads of on-chip decap is necessary to maintain power integrity, which is similar to the result in Figure 4.7. With 300-pF on-chip decap and 1-nH bond wire inductance, the amplitude of the over-voltage and under-voltage transients of the supply voltage is not sensitive to the amount of the off-chip decap, unless the off-chip decap is very small, as shown in Figure 4.13. In Figure 4.14, it is shown that a large package inductance connected to VDD may improve the minimum supply voltage on the VDD domain due to the ESD current injection. This concurs with the observation from Condition (4.3) that a larger impedance of the off-chip path formed by bond wire inductances and off-chip decap helps with power integrity during ESD.

The rail clamp has a nonlinear behavior and it only turns on beyond a certain voltage. As a result, the amplitude of supply fluctuations depends on the polarity of the ESD current. The amplitude of under-voltage transient may be larger in the positive ESD than the negative one when there are multiple power domains whose ground nets are connected by APDs and the rail clamps are better at clamping the on-chip supply voltage than the on-chip decap. As an example, an IC is assumed to have one VDDIO domain and one VDD domain as shown in Figure 4.1.

When a positive ESD current is injected into an IO in the VDDIO domain protected by the dual diodes, the current is directed to VDDIO and then part of the current is directed to VSSIO by the rail clamp. The current exiting the VSSIO pin induces a voltage on the package inductance. At the leading edge of the ESD current, VSSIO is at a higher potential than the board ground and the APD connecting VSSIO and VSS turns on. The current injected from VSSIO to VSS induces another voltage on the package inductance and then VSS is also at a higher potential than the board ground. As a result, the VDD domain undergoes an under-voltage transient. At the trailing edge of the ESD current, VSS has a lower potential than the board ground and there is an over-voltage transient in the VDD domain. When a negative ESD current is injected into the same IO, the potential of VSS is first higher and then lower than that of the board ground, and there is an over-voltage transient followed by an under-voltage one in the VDD domain.

If the rail clamp in the VDD domain turns on before the under-voltage transient occurs, which is the usual case for a negative ESD, this will reduce the deviation from the normal supply potential when the ESD current starts to decrease. In other words, the ESD current is distributed with a better balance among the package inductances, such that the current through L_{VDD} is larger than the case when the rail clamp is off. When the negative ESD current diminishes, there is a higher voltage induced on L_{VDD} to cancel the voltage induced on L_{VSS}, which gives smaller amplitudes of under-voltage transients in the negative ESD than in a positive one.

The noise induced on the VDD supply does not change significantly if the IOs in the VDDIO domain are protected by local clamps rather than dual-diodes. This finding is

expected since the disturbance is caused by the current injected from VSSIO to VSS, which is similar in both cases.

The preceding discussion focused on the propagation of noise from the VDDIO domain (zap domain) to the internal VDD domain. Conversely, the noise in the VDDIO domain is affected by the ESD response of the VDD domain. In particular, if the rail clamp of the VDD domain turns on, it can affect the amplitude of the noise on the VDDIO supply. In the VDDIO domain, the turning-on of the rail clamp in the VDD domain at the trailing edge of the positive ESD current alters the rate of current change through L_{VSSIO}. At this trailing edge, voltages are induced on package inductances so that on-chip VDDIO and VSSIO potentials are pulled below the corresponding potentials on-board. There is then an over-voltage transient in the VDD domain, and the rail clamp in this domain turns on. The additional current from L_{VDD} through the VDD rail clamp reduces the magnitude of the induced voltage on L_{VSSIO}. This results in a larger amplitude of under-voltage transient in the VDDIO domain during the positive ESD than a negative one, where the under-voltage transient occurs at the same time for the VDDIO and VDD domain. The amplitude of supply fluctuation in the zapped domain is thus larger with the smaller equivalent resistance of the rail clamp in a domain that is not zapped, as shown in Figure 4.15.

For IOs protected by local clamps in the VDDIO domain, positive discharges also cause a larger amplitude of under-voltage transient in the VDDIO domain than negative ones. However, this polarity dependence is not caused by the ESD response of the VDD domain. When the IO is protected by a local clamp, the under-voltage transient appears at the leading edge of a positive ESD current without the rail clamp turned on, while this

transient appears at the trailing edge of negative ESD current when the rail clamp is on. It has been shown that the amplitude of the under-voltage transient is smaller if the rail clamp turns on before this transient, and therefore there is the polarity dependence for IOs protected by local clamps.

4.2 Measured and simulated supply fluctuations on a 130-nm test chip

Figure 4.16 shows the simulated supply fluctuation in response to a 2-kV ESD gun discharge on a 130-nm CMOS test chip in a wire-bond package. There are two power domains on the chip, the 3.3 V VDDIO domain and the 1.5 VDD domain. The two ground nets, VSSIO and VSS are connected by APDs. The ESD current is discharged to an IO in the VDDIO domain in the tethered setup. For the IO protected by dual diodes, the zapped domain (VDDIO) will have similar supply fluctuation waveforms during a positive discharge and a negative one, where there is first an overshoot in supply voltage and then an undershoot. In positive discharges, the overshoot is caused by a major portion of the ESD current being directed to the power net. For the IO protected by SCR in positive ESD, only the supply noise in the zapped domain is different, which begins with an undershoot, since the current is directed to VSSIO.

On this test chip there are supply noise monitors that can detect and measure nanosecond-scale transient supply disturbances and record the maximum and minimum supply voltage, as illustrated in Figure 4.17 and Table 4.1. The monitors are assigned to the VDDIO and VDD domains. The details of the supply voltage monitor circuits are

given in [45]. The monitor circuits' outputs are read out after the system-level ESD event, shown in Table 4.2. Under-voltage and over-voltage transients occur regardless of IO ESD protection, power domain under stress, and the polarity of ESD current, although the amplitudes are different. However, positive ESD current induces larger amplitudes of the under-voltage and over-voltage transients, as explained in Section 4.1.2.

According to the monitor outputs, minimum supply voltage of both domains is smaller for positive discharges into a dual-diode protected IO in VDDIO domain than negative discharges.

With the simulation setup shown in Figure 4.18, a reasonably good match between the simulation and measurement can be achieved, as shown from Figure 4.19 to Figure 4.21 for the three zapped IOs shown in Table 4.2 with different ESD protections at the IOs in two power domains. The discrepancies are attributed to imperfect representations of the ESD tester, PCB and IC package. These three sources, especially the PCB and package, introduce coupling between traces and between bond wires that are connected to the circuit, and this is not accurately captured by the simulation. The magnetic coupling between input or output traces and bond wires induces current of the opposite direction at neighboring IOs of the zapped IO, since they are connected to these traces and bond wires. These IOs may provide additional low-impedance current return paths for the ESD current. The magnetic coupling between bond wire connected to the zapped IO and that connected to the power or ground pin alters the impedance of the current return path through the PDN. These coupling mechanisms change the distribution of ESD current directed to the VDDIO, VSSIO, VDD and VSS nets on-chip. The simulated waveforms

are very sensitive to the rate of the ESD current change, which strongly depends on the characteristics of the traces and bond wires.

4.3 Measured and simulated supply fluctuation transients on the 65-nm test chip

The amplitudes of supply fluctuation at different locations on-chip vary due to the bus resistances of power and ground nets. When an ESD current exits the chip through power and ground pins, it results in voltage drops on the buses. Within the IO supply domain, the supply voltage has its largest amplitude fluctuation at the location where the ESD current is injected. ESD current is injected to other domains through APDs, and the largest amplitude of supply fluctuation for these domains occurs at the location of the APDs. A shared VSS between multiple domains may reduce the amplitude of supply fluctuation of the domain of the zapped IO by reducing the impedance of its ground net. However, ESD-induced supply noise also travels to other power domains more easily through a shared VSS than separate VSSIO and VSS with APDs.

Figure 4.22 shows the location dependence of supply fluctuation in system-level ESD on the 65-nm test chip. The current is injected to IO7 of VDDIO domain, and the pad assignment is shown in Figure 3.1. For on-chip supply voltages of VDDIO domain at different IOs, it is observed that the magnitude of the over-voltage transient decreases as the location moves away from IO7. However, the magnitude of this over-voltage transient does not vary significantly between different locations on-chip and therefore the disturbance on the supply voltage must be considered to be a global issue for the chip. For on-chip supply voltages of the VDD domain, the amplitude of the under-voltage

transient is largest at the right VDDIO pad in a positive ESD event, where a lot of current is directed to VSS through the rail clamp here. In a negative ESD event, the amplitude of under-voltage transient of the VDD domain is largest at the location closest to IO7 due to the shared VSS bus.

A circuit's robustness against supply fluctuations varies from design to design. On the other hand, if a circuit is known to malfunction under ESD-induced supply fluctuation, this circuit can be used as a supply noise detector or monitor. Figure 4.23 shows two circuits on the 65-nm test chip in the VDD domain that were disturbed under ESD gun discharges to IOs in the VDDIO domain with the mobile setup. One is a cross-coupled inverter with additional unbalanced capacitive loads. The other is a D-latch which resets to logic low. Figure 4.24 shows the actual implementation of the D-latch. Both circuits are sensitive to an event where the supply collapses and then recovers.

The cross-coupled inverter is initially reset to $OUT = 0$. As shown in Figure 4.25, ESD may cause the net supply voltage ($VDD - VSS$) to decrease briefly, which causes a partial discharge of the two capacitors in the circuit through the transistors. If the supply voltage falls below a certain level, the output of the cross-coupled inverter is indeterminate; once the supply starts to recover, the displacement current through the capacitors will cause the stored bit to be flipped relative to its original value and thus $OUT = 1$. The likelihood for these upsets to occur mainly depends on the speed of the positive voltage transient at the on-chip supply, where a faster recovery induces larger displacement current to trigger the upset, as shown in Figure 4.26.

The D-latch is initially reset to $OUT = 0$, and experiences a similar upset mechanism. It has a feedback inverter in the circuit and whether an upset occurs depends on the

relative drive strength to the capacitive loads seen by the forward stage and the feedback stage. The parasitic capacitance connected to node Q is dominated by the gate capacitances in the inverter whose output is node Qb. The parasitic capacitances connected to Qb is dominated by the gate capacitances of $M5$ and $M7$. When $(VDD - VSS)$ rises back to its normal value, the gate capacitances of the PMOS devices are pulling the node voltages to VDD, and those of the NMOS ones are pulling the voltages to VSS. The gate capacitance of $M7$ is connected to VDD through two PMOS devices, which degrades its efficiency to couple the voltage at node Q to VDD. Thus the circuit tends to reset to logic high if there is a fast power up. On this chip, supply voltage reversal can occur, as predicted in Figure 4.22. As shown in Figure 4.27, the D-latch is more robust against upset than are the cross-coupled inverters, i.e., upset is predicted to occur only occurs if there is a sizable supply reversal in which VSS is more than one diode drop above VDD. However, the D-latch appears to be less sensitive to power supply recovery speed than is the cross-coupled inverter.

RST is shared by both circuits, and it is an external signal that is filtered on-chip by a 100-ns RC filter. The filter drives a buffer consisting of two inverters. When $\Delta V'$ is very large and tr is small, the output of the buffer can be coupled high and the upset is erased. Figure 4.28 illustrates this effect in the D-latch, and a similar observation is made in the simulation of the cross-coupled inverter. This effect may or may not appear in the real chip, as $\Delta V'$ is determined by the performance of the rail clamp. An efficient rail clamp turns on quickly to prevent a high over-voltage transient when the supply recovers, which is the case for this test chip.

When a strongly reversed supply voltage appears on an IC, all the substrate diodes and well diodes turn on, and the IC is in danger of latch-up with the minority carrier injection. The diffusion capacitances of these diodes are dependent on the diode current, and may slow down the recovery speed of on-chip supply when they are discharged.

Simulation has shown that, for the upsets in these monitors to occur, it is necessary that a strong supply collapse occurs. The likelihood of the occurrence of upsets depends on the discharging of parasitic capacitors as well the capacitive coupling to a fluctuating supply. The coupling effect for the monitors on this test chip is significant enough to cause a rise time dependence, but a severe supply collapse discharging the parasitic capacitors is still necessary to trigger the upsets..

Table 4.3 shows the measurements results during ESD gun discharges in a mobile setup. The cross-coupled inverter upsets when ESD level reaches ±2 kV, while the D-latch upsets only when ESD level is at or higher than +4 kV. The measurement suggest that the negative discharges induce smaller amplitude of supply noise, since this chip has two externally regulated power domains similar to the 130-nm test chip. The simulated values of the minimum ESD level needed to trigger the noise monitor are also shown in Table 4.3. The simulation results show reasonable agreement with the measurements. The simulation setup is similar to the one shown in Figure 4.18 and the simulation netlist includes the ESD tester, ESD protection devices at the IO pin, the package bond wire inductances for the IO and all power and ground pins, the rail clamps for all the power domains, the on-chip and off-chip decaps, and the power and ground buses.

On the test chip, there is a third type of monitor, a SR-latch. The circuit contains a NAND gate as the feed-forward stage and an identical NAND gate as the feed-back

stage. The input is connected to a tie-high cell, as shown in Figure 4.29. Figure 4.30 shows the simulation results of the circuit's response to the disturbance shown in Figure 4.25, indicating that this circuit needs an even greater supply reversal to upset than do the other monitor circuits. There is less dependence on the speed of power recovery compared with the cross-coupled inverter and the D-latch, and the upset is mainly controlled by the discharging time of the capacitors.

On the same test chip, there are also GDs attached to internally generated signals from tie-low or tie-high cells along a signal line. These GDs contain two SR-latches, as shown in Figure 4.31. Upsets occur for these circuits (see Figure 4.32 and Figure 4.33), and they are also triggered by the discharging of parasitic capacitors and the coupling of these capacitors to the fluctuating supply. The ESD threshold for upset is slightly lower when the input is connected to a tie-high cell than a tie-low cell. In the case where the input is from a tie-high cell, it is the SR-latch at the top that upsets. This latch is slightly more sensitive than the standalone one, which results from its input, IN, driving a NAND gate and an inverter with a stronger capacitive coupling effect to VSS, instead of driving a single NAND gate. The simulation results are in agreement with measurement results obtained for system-level ESD test of the mobile setup. In measurement, glitches start to appear at +4 kV and are reported for tie-high lines more often than for tie-low lines.

4.4 Figures and tables

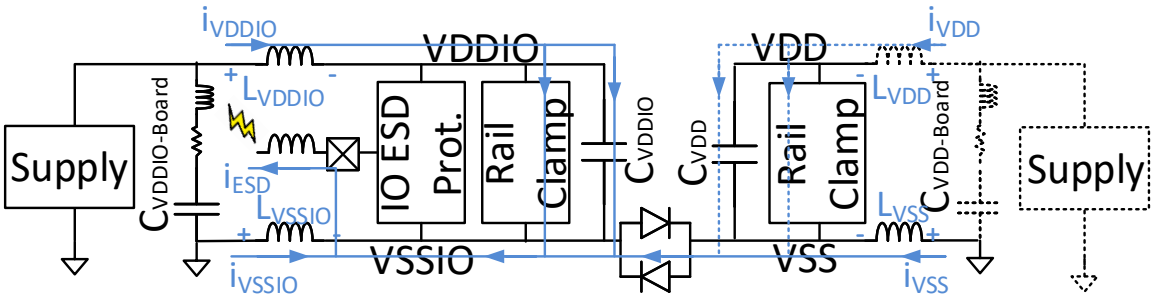


Figure 4.1: Interaction across multiple chip power domains in ESD. A negative ESD current is discharged to an IO of VDDIO domain, and the current (shown in blue) is drawn from all power and ground nets to this IO. VDD domain may or may not require the off-chip supply.

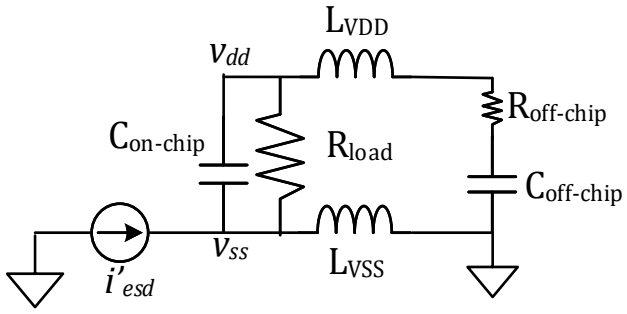


Figure 4.2: Simplified circuit representation to study the effect of ESD current injected to the on-chip ground net on the supply voltage of the VDD domain. The on-chip decap ($C_{on-chip}$), off-chip decap ($C_{off-chip}$), and package inductances (L_{VDD} and L_{VSS}) are involved. R_{load} represents the power-consuming circuits in the VDD domain. $R_{off-chip}$ represents the equivalent series resistance of $C_{off-chip}$.

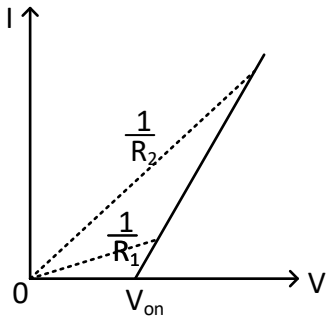
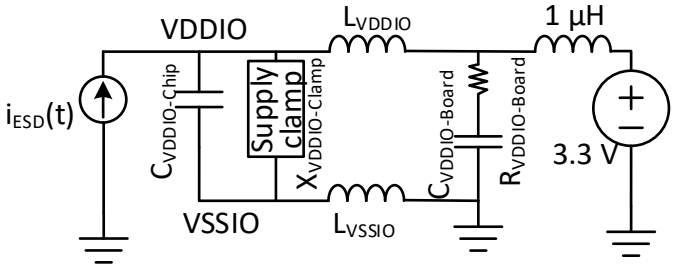
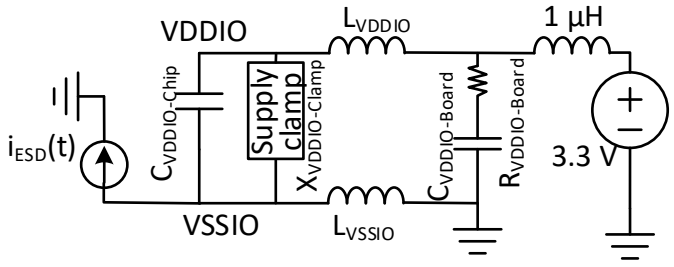


Figure 4.3: I-V curve of a typical rail clamp. The equivalent resistance of the circuit is decreasing when the current increases, i.e., $R_2 < R_1$.



(a)



(b)

Figure 4.4: A generic circuit to study supply fluctuations during system-level ESD. The on-chip supply voltage is normally at 3.3 V. The ESD current, $i_{ESD}(t)$, is injected to (a) the power net (VDDIO) from an ESD top diode at an IO or (b) the ground net (VSSIO) from an ESD bottom diode at the IO. L_{VDDIO} and L_{VSSIO} are package inductances. $C_{VDDIO-Chip}$ is the on-chip decap. $C_{VDDIO-Board}$ is the off-chip decap, and $R_{VDDIO-Board}$ is its equivalent series resistance. Unless otherwise specified, $C_{VDDIO-Chip}$ = 300 pF, L_{VDDIO} = 1 nH, L_{VSSIO} = 1 nH, $C_{VDDIO-Board}$ = 100 nF and $R_{VDDIO-Board}$ = 20 mΩ. The supply clamp model is shown in Figure 4.5.

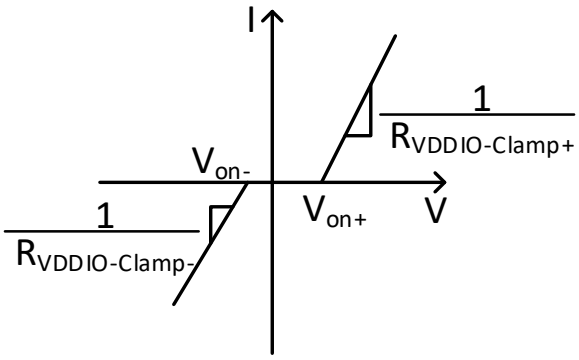


Figure 4.5: I-V model of the supply clamp shown in Figure 4.4. When voltage across the clamp is above V_{on+}, the rail clamp turns on. When voltage across the clamp is below V_{on-}, the reverse diode is forward biased. Unless otherwise specified, V_{on+} = 4 V, $R_{VDDIO-Clamp+}$ = 0.2 Ω, V_{on-} = -1.05 V, $R_{VDDIO-Clamp-}$ = 0.25 Ω.

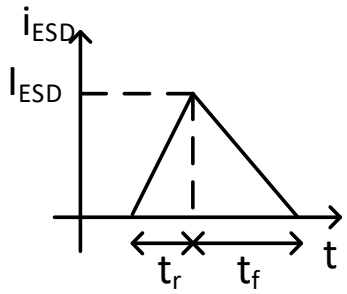
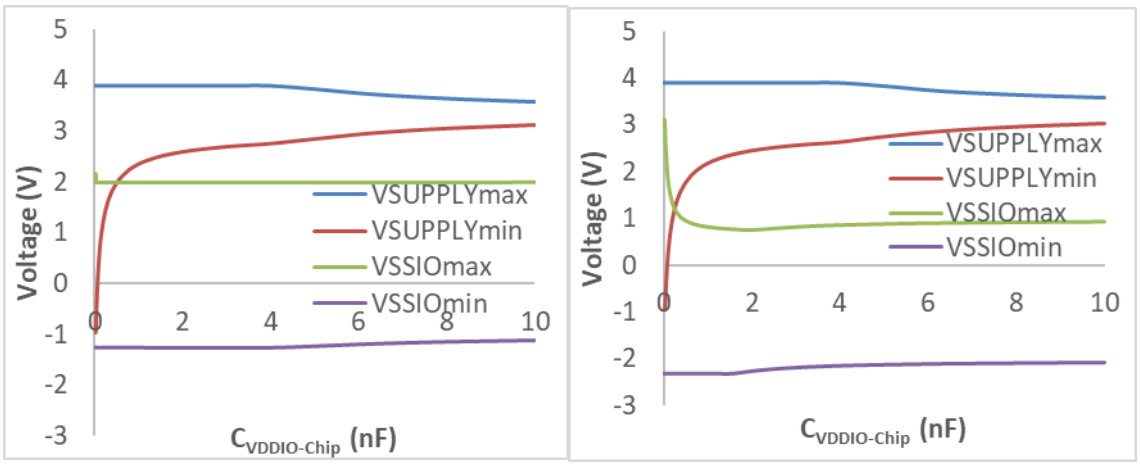
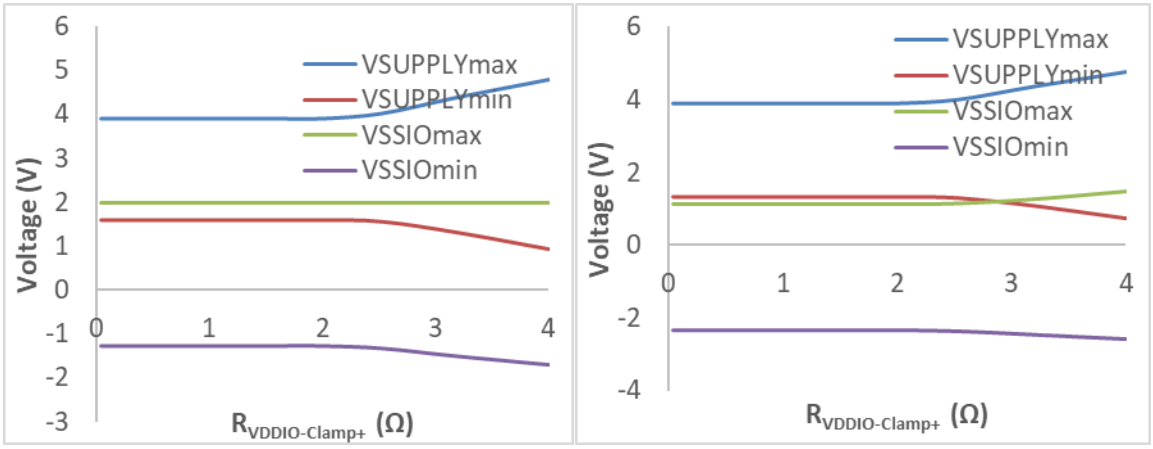


Figure 4.6: Waveform of $i_{ESD}(t)$ in Figure 4.4. Unless otherwise specified, t_r = 1 ns, t_f = 2 ns, I_{ESD} = 4 A.



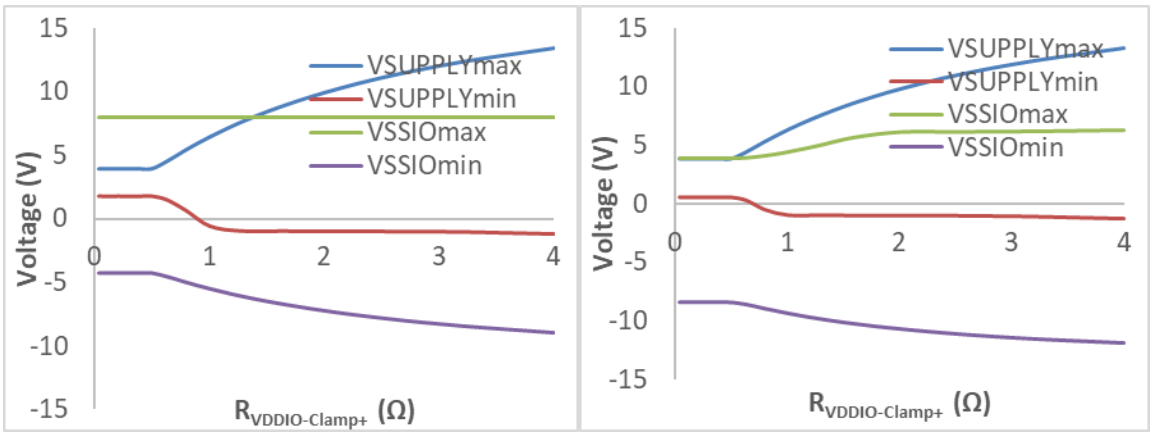
(a) (b)

Figure 4.7: Maximum and minimum voltages of the on-chip supply and VSSIO of the circuit shown in Figure 4.4 with respect to the amount of on-chip decap, $C_{VDDIO-Chip}$, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSS. $VSUPPLY = VDDIO - VSSIO$.



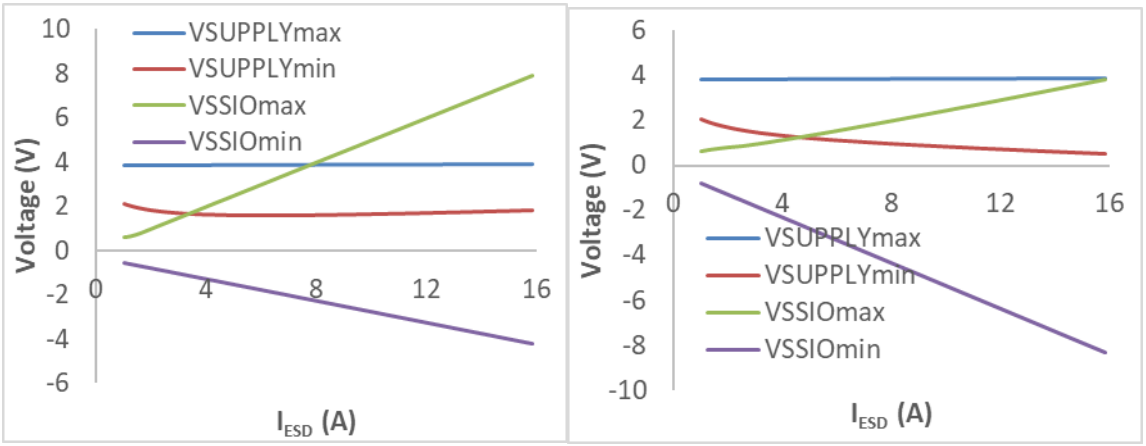
(a) (b)

Figure 4.8: Maximum and minimum voltages of the on-chip supply and VSSIO of the circuit shown in Figure 4.4 with respect to the on-resistance of the rail clamp, $R_{VDDIO-Clamp+}$, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSS. $VSUPPLY = VDDIO - VSSIO$. When there is no rail clamp, i.e., $R_1 \rightarrow \infty$, the minimum supply voltage becomes -1 V, clamped by the reversed diode. The I-V model parameters of the reverse diode, i.e., V_{on-} and $R_{VDDIO-Clamp-}$, are not varied in the simulation.



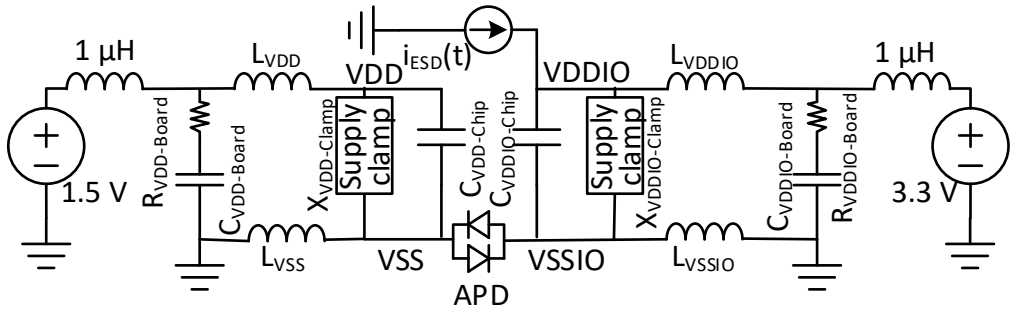
(a) (b)

Figure 4.9: Maximum and minimum voltages of the on-chip supply and VSSIO of the circuit shown in Figure 4.4 with respect to the on-resistance of the rail clamp, $R_{VDDIO-Clamp+}$, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSS. $VSUPPLY = VDDIO - VSSIO$. The peak ESD current is 16 A. The I-V model parameters of the reverse diode, i.e., V_{on-} and $R_{VDDIO-Clamp-}$, are not varied in the simulation.

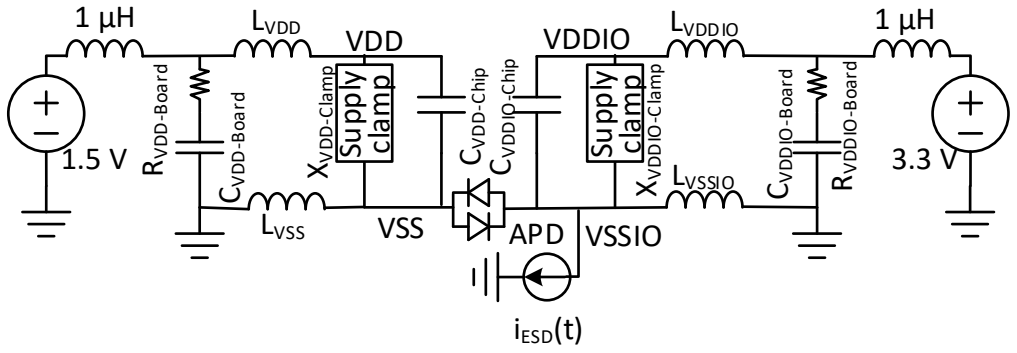


(a) (b)

Figure 4.10: Maximum and minimum voltages of the on-chip supply and VSSIO of the circuit shown in Figure 4.4 with respect to the peak ESD current, I_{ESD}, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSS. $VSUPPLY = VDDIO - VSSIO$.

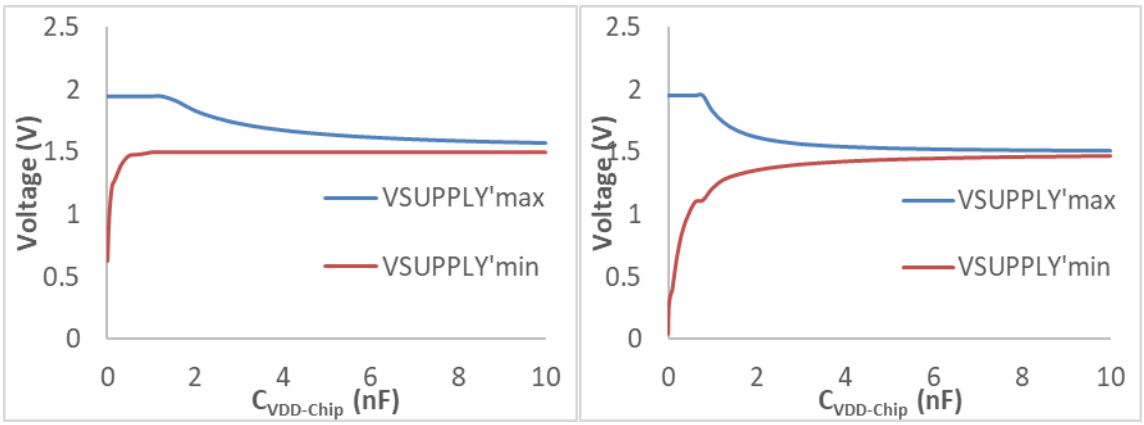


(a)



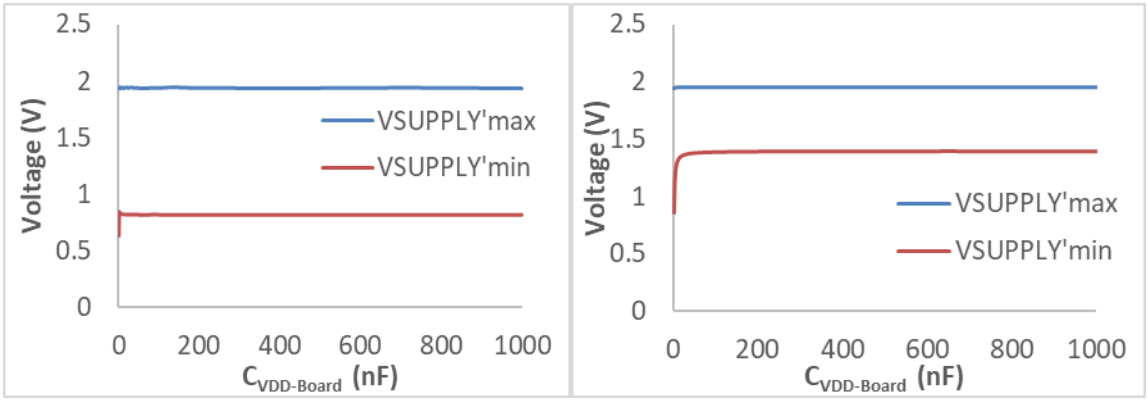
(b)

Figure 4.11: A generic circuit based on the one shown in Figure 4.4 to study supply fluctuations when ESD-induced noise travels from one power domain to another during system-level ESD. The on-chip supply voltage is normally at 3.3 V for the VDDIO domain and 1.5 V for the VDD domain. VSS and VSSIO are connected by APDs. The APDs have a turn-on voltage of 1 V and an on-resistance of 0.15 Ω. The ESD current, $i_{ESD}(t)$, is injected to (a) the power net (VDDIO) from an ESD top diode at an IO in VDDIO domain or (b) the ground net (VSSIO) from an ESD bottom diode at the IO. The waveform of $i_{ESD}(t)$ is shown in Figure 4.6. L_{VDDIO}, L_{VSSIO}, $C_{VDDIO-Chip}$, $X_{VDDIO-Clamp}$, $C_{VDDIO-Board}$ and $R_{VDDIO-Board}$ are the same as shown in Figure 4.4. L_{VDD} and L_{VSS} are package inductances. $C_{VDD-Chip}$ is the on-chip decap for VDD domain. $X_{VDD-Clamp}$ is the parallel combination of rail clamp and reverse diode in VDD domain. Its I-V model is similar to that for $X_{VDDIO-Clamp}$, except that the trigger voltage of the rail clamp, V_{on+}, is 2 V and the on-resistance of the rail clamp, $R_{VDD-Clamp+}$, is 0.2 Ω. The parameters in the I-V model are not changed in the simulation unless specified. $C_{VDD-Board}$ is the off-chip decap for VDD domain, and $R_{VDD-Board}$ is its equivalent series resistance. Unless otherwise specified, $C_{VDD-Chip}$ = 300 pF, L_{VDD} = 1 nH, L_{VSS} = 1 nH, $C_{VDD-Board}$ = 100 nF and $R_{VDD-Board}$ = 20 mΩ.



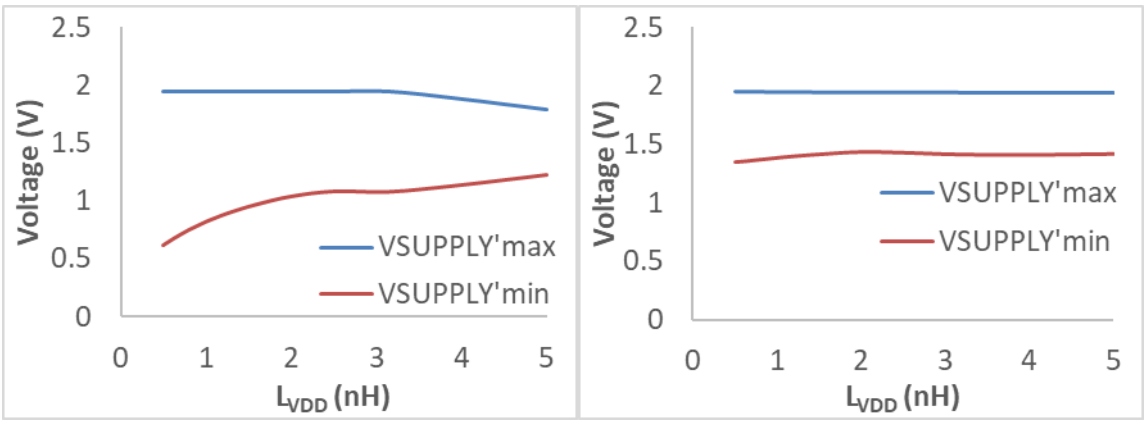
(a) (b)

Figure 4.12: Maximum and minimum voltages of the on-chip supply of the VDD domain shown in Figure 4.11 with respect to the amount of on-chip decap in the VDD domain, $C_{VDD-Chip}$, during system-level ESD for (a) a positive ESD current directed to VDDIO; (b) a negative ESD current directed to VSSIO. $VSUPPLY' = VDD - VSS$.



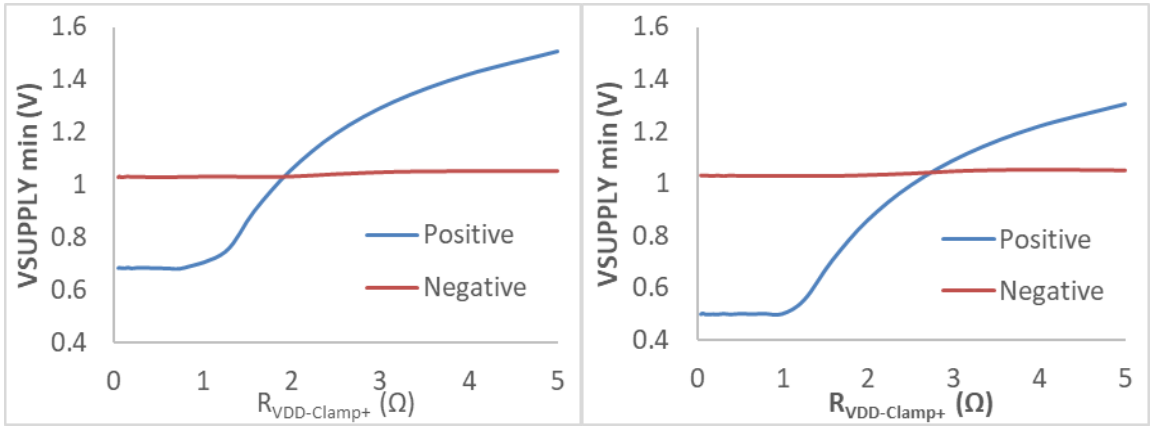
(a) (b)

Figure 4.13: Maximum and minimum voltages of the on-chip supply of the VDD domain shown in Figure 4.11 with respect to the amount of off-chip decap for the VDD domain, $C_{VDD-Board}$, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSSIO. $VSUPPLY' = VDD - VSS$.



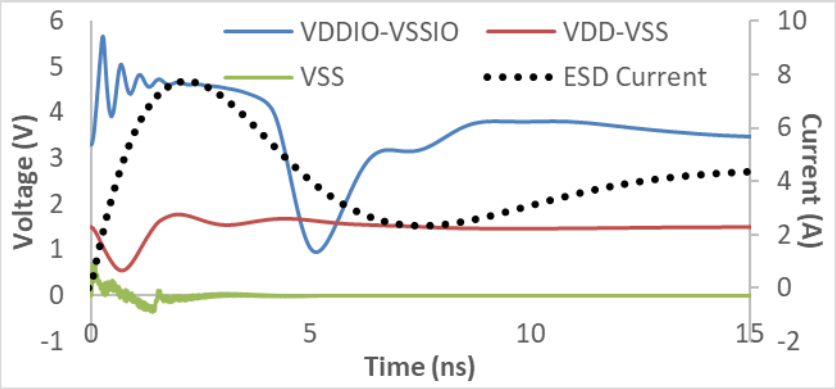
(a) (b)

Figure 4.14: Maximum and minimum voltages of the on-chip supply of the VDD domain shown in Figure 4.11 with respect to the inductance of the bond wire connected to VDD, L_{VDD}, during system-level ESD for (a) positive ESD current directed to VDDIO; (b) negative ESD current directed to VSSIO. $VSUPPLY' = VDD - VSS$.

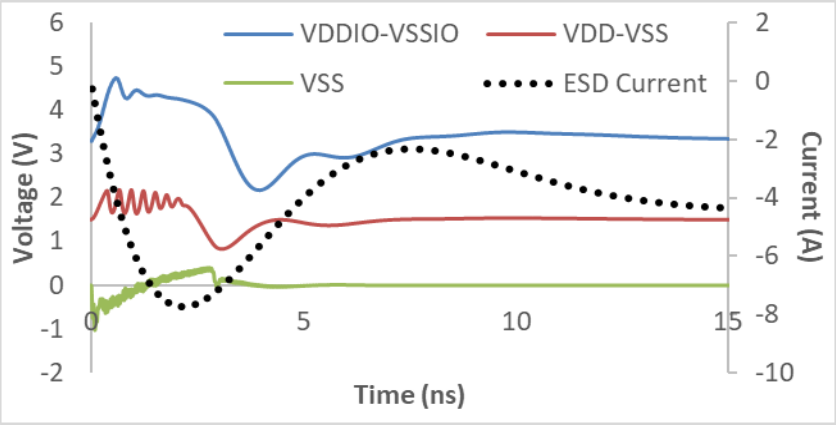


(a) (b)

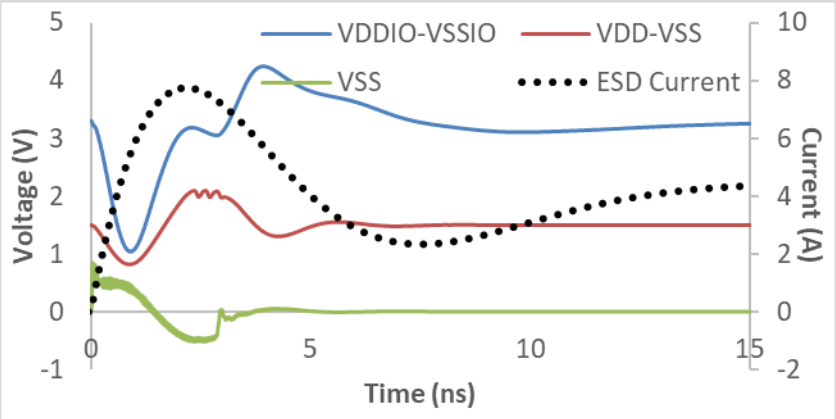
Figure 4.15: Minimum voltages of on-chip supply of the VDDIO domain shown in Figure 4.11 with respect to the on-resistance of the rail clamp in the VDD domain, $R_{VDD-Clamp+}$, during system-level ESD with peak current, I_{ESD} = 8 A for (a) $R_{VDD-Clamp+}$ = 0.2 Ω; (b) $R_{VDD-Clamp+}$ = 1 Ω, where $R_{VDD-Clamp+}$ is the on-resistance of the rail clamp in the VDDIO domain. $VSUPPLY = VDDIO - VSSIO$. The I-V model parameters of the reverse diode in the VDD domain, i.e., V_{on-} and $R_{VDD-Clamp-}$, are not varied in the simulation.



(a)



(b)



(c)

Figure 4.16: Simulated on-chip supply voltage of the 130-nm test chip during a 2-kV ESD gun discharge into an IO in the VDDIO domain. Simulated voltage on VSS with respect to board ground is also shown. (a) Positive discharge into a dual-diode protected IO. (b) Negative discharge into the dual-diode protected IO. (c) Positive discharge into IO with a local clamp protection: DTSCR and reverse diode.

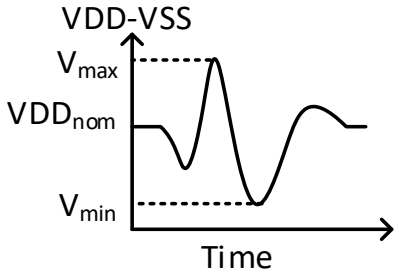


Figure 4.17: Supply voltage monitor circuits to record V_{max} and V_{min}.

Table 4.1: The supply voltage monitor output levels are calibrated using VFTLP measurements (pulse width 4 ns, rise time 200 ps). The nominal supply voltage for the VDD domain is 1.5 V, and the nominal supply voltage for the VDDIO domain is 3.3 V.

(a) Monitors in the VDD domain.

	VDD	
	Under-voltage monitor	Over-voltage monitor
Level 0	$V_{min} > 1.15$ V	$V_{max} < 2.1$ V
Level 1	0.54 V $< V_{min} \leq 1.15$ V	2.1 V $\leq V_{max} < 2.29$ V
Level 2	0.13 V $< V_{min} \leq 0.54$ V	$V_{max} \geq 2.29$ V
Level 3	$V_{min} \leq 0.13$ V	Not applicable

(b) Monitors in the VDDIO domain.

	VDDIO	
	Under-voltage monitor	Over-voltage monitor
Level 0	$V_{min} > 1.94$ V	$V_{max} < 3.88$ V
Level 1	1.36 V $< V_{min} \leq 1.94$ V	3.88 V $\leq V_{max} < 4.66$ V
Level 2	0.36 V $< V_{min} \leq 1.36$ V	$V_{max} \geq 4.66$ V
Level 3	$V_{min} \leq 0.36$ V	Not applicable

Table 4.2: Outputs of the supply voltage monitors in VDDIO and VDD domains after discharges compliant to IEC 61000-4-2 at various IOs in the VDDIO domain. The results are shown for tethered discharges. ZAPIO2 is a dual-diode protected IO in the VDDIO domain. ZAPIO_SCR1 is an IO in the VDDIO domain protected by an SCR and bottom diode. LV_ZAPIO1 is a dual-diode protected IO in the VDD domain.

IEC level (kV)	VDDIO: Under-voltage			VDDIO: Over-voltage		
	ZAPIO2	ZAPIO_SCR1	LV_ZAPIO1	ZAPIO2	ZAPIO_SCR1	LV_ZAPIO1
-5	0	NA	NA	1	NA	NA
-4	0	NA	NA	1	NA	NA
-3	0	NA	NA	1	NA	NA
-2	0	0	0	1	1	1
-1.5	0	0	0	1	1	1
-1	0	0	0	1	1	1
-0.5	0	0	0	1	1	0
0	0	0	0	0	0	0
0.5	0	0	0	1	1	0
1	0	0	0	1	1	0
1.5	1	0	0	2	1	1
2	1	1	0	2	1	1
3	3	NA	0	2	NA	1
4	3	NA	NA	2	NA	NA
5	3	NA	NA	2	NA	NA

IEC level (kV)	VDD: Under-voltage			VDD: Over-voltage		
	ZAPIO2	ZAPIO_SCR1	LV_ZAPIO1	ZAPIO2	ZAPIO_SCR1	LV_ZAPIO1
-5	1	NA	NA	2	NA	NA
-4	1	NA	NA	2	NA	NA
-3	1	NA	NA	2	NA	NA
-2	1	1	1	1	1	1
-1.5	0	1	1	1	1	1
-1	1	1	1	1	1	1
-0.5	0	0	0	0	0	0
0	0	0	0	0	0	0
0.5	1	0	1	0	0	2
1	1	1	1	1	0	2
1.5	2	1	1	1	1	2
2	3	2	1	1	1	2
3	3	NA	2	2	NA	2
4	3	NA	NA	2	NA	NA
5	3	NA	NA	2	NA	NA

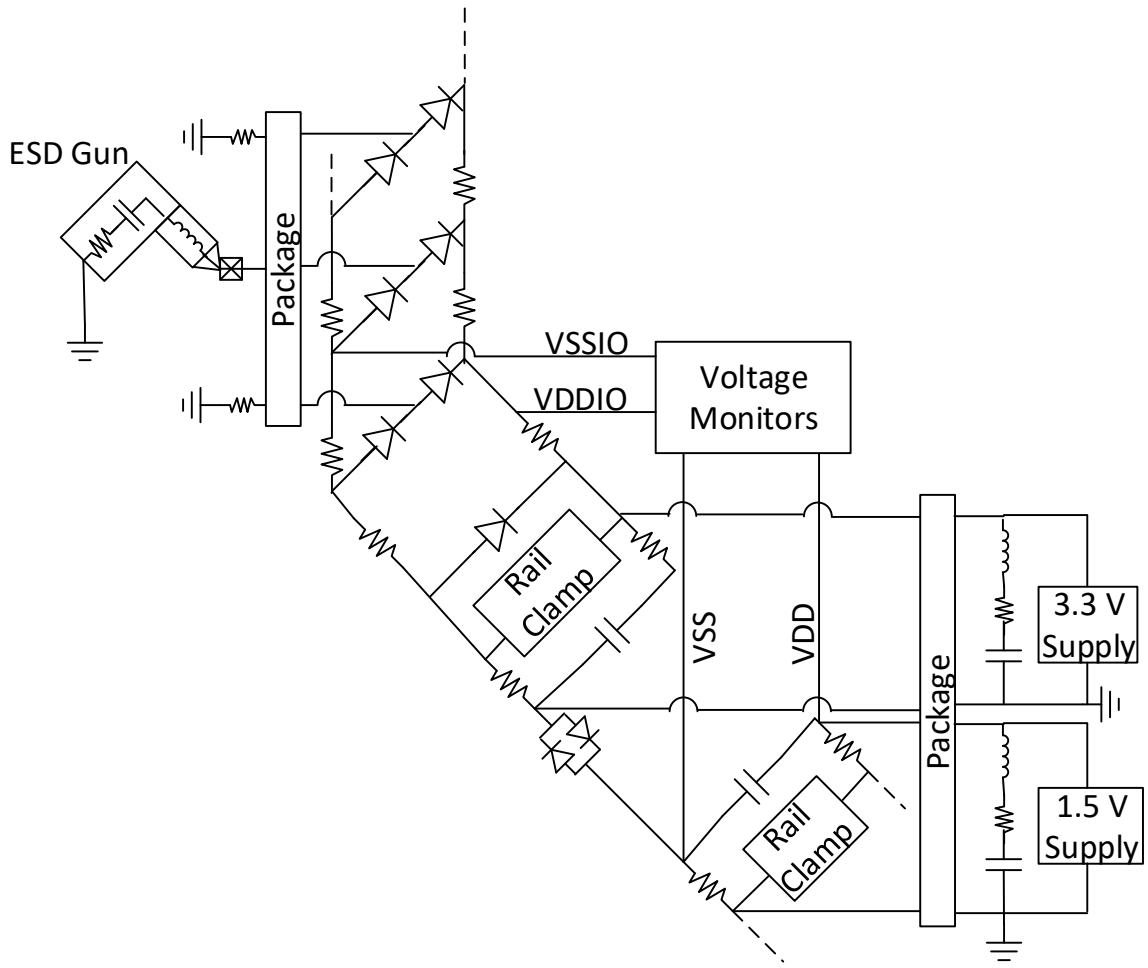
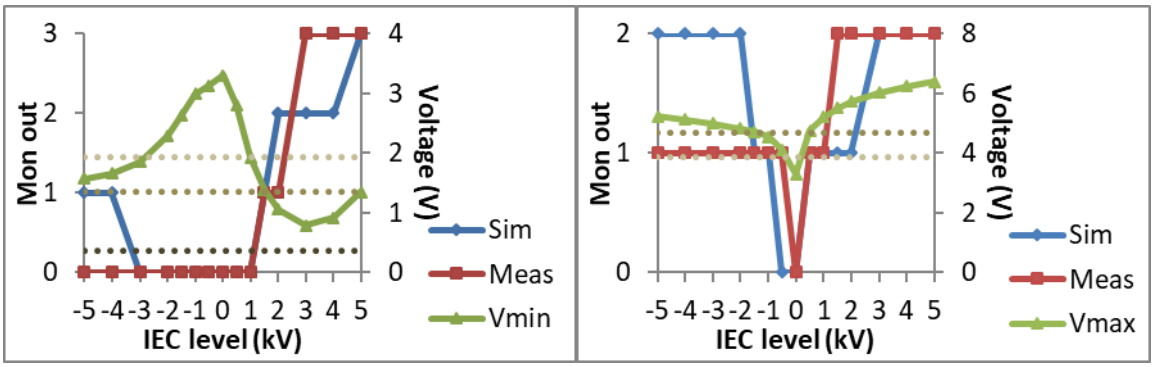


Figure 4.18: Conceptual simulation setup to study the response of the voltage monitors on the 130-nm test chip during system-level ESD.



(a) (b)

(c) (d)

Figure 4.19: Simulated and measured outputs of (a) under-voltage monitors in the VDDIO domain; (b) over-voltage monitors in the VDDIO domain; (c) under-voltage monitors in the VDD domain; (d) over-voltage monitors in the VDD domain when ZAPIO2, a dual-diode protected IO in the VDDIO domain is stressed. The simulated minimum or maximum supply voltages on chip are also shown. Dashed lines are measured thresholds of the voltage monitors in VFTLP experiments with 200 ps rise time and 4 ns pulse width.

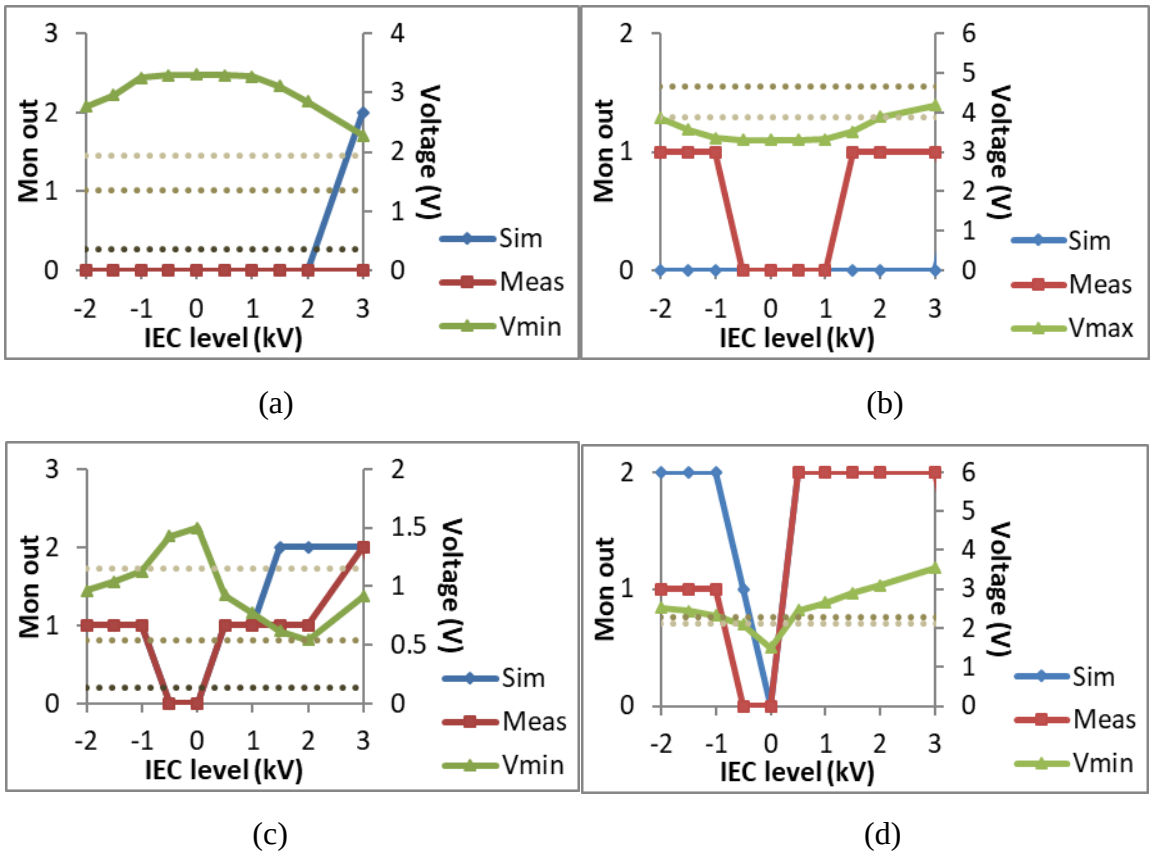


Figure 4.20: Simulated and measured outputs of (a) under-voltage monitors in the VDDIO domain; (b) over-voltage monitors in the VDDIO domain; (c) under-voltage monitors in the VDD domain; (d) over-voltage monitors in the VDD domain when ZAPIO_SCR1, an IO in the VDDIO domain protected by a local clamp (an SCR in parallel with a reverse diode) is stressed. The simulated minimum or maximum supply voltages on chip are also shown. Dashed lines are measured thresholds of the voltage monitors in VFTLP experiments with 200 ps rise time and 4 ns pulse width.

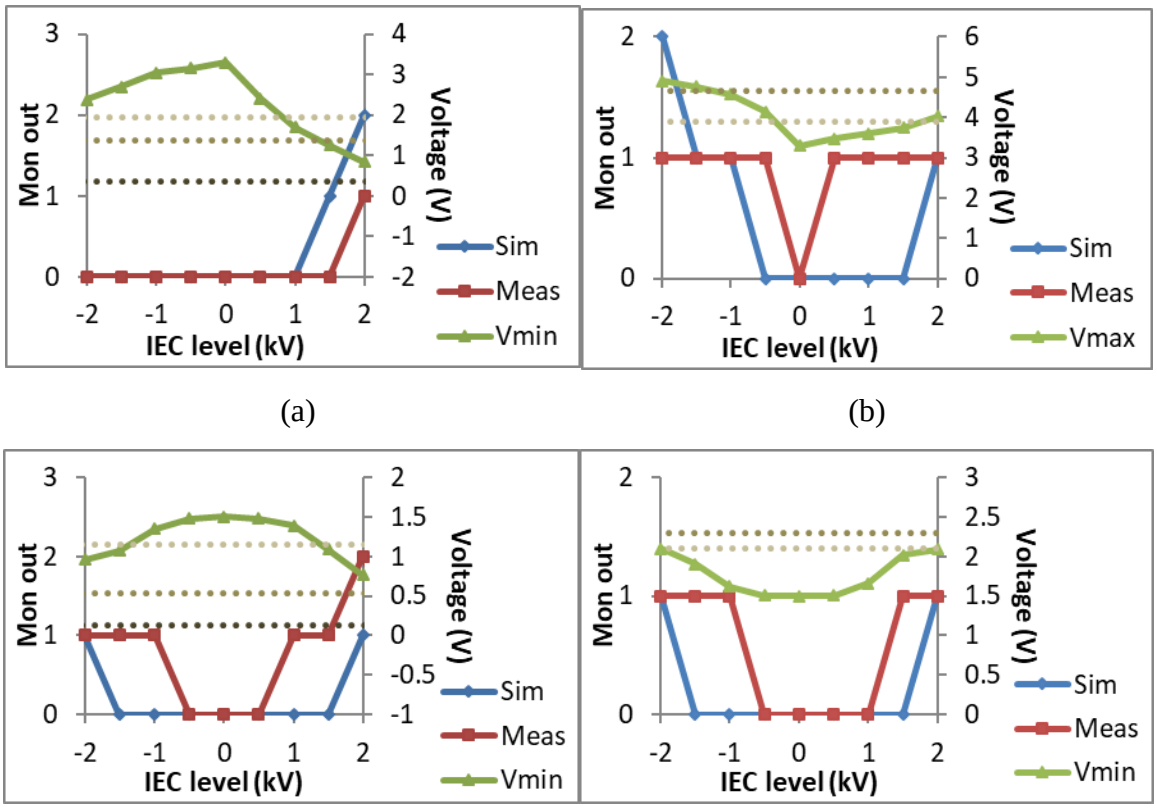
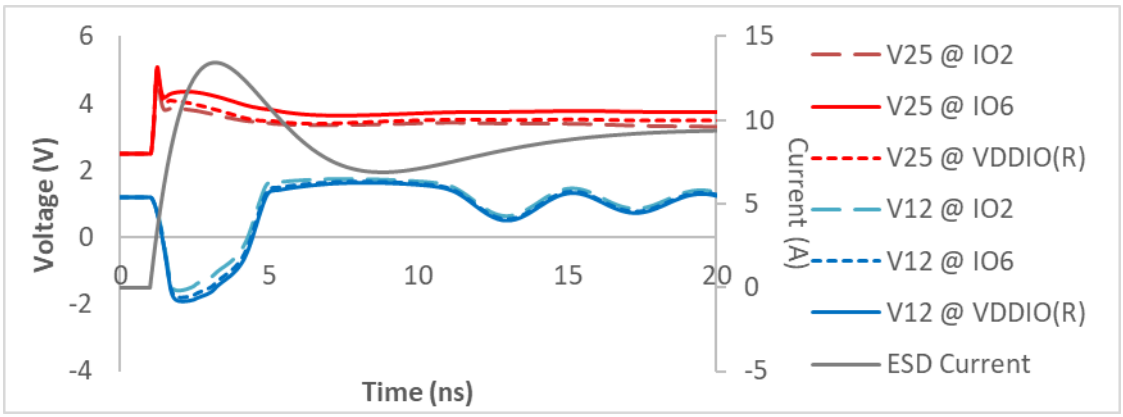
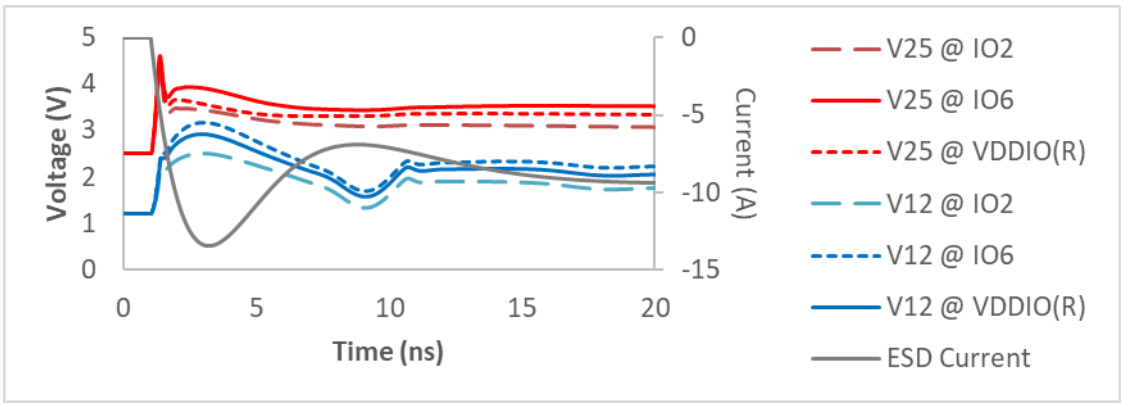


Figure 4.21: Simulated and measured outputs of (a) under-voltage monitors in the VDDIO domain; (b) over-voltage monitors in the VDDIO domain; (c) under-voltage monitors in the VDD domain; (d) over-voltage monitors in the VDD domain when LV_ZAPIO1, a dual-diode protected IO in the VDD domain is stressed. The simulated minimum or maximum supply voltages on chip are also shown. Dashed lines are measured thresholds of the voltage monitors in VFTLP experiments with 200 ps rise time and 4 ns pulse width.

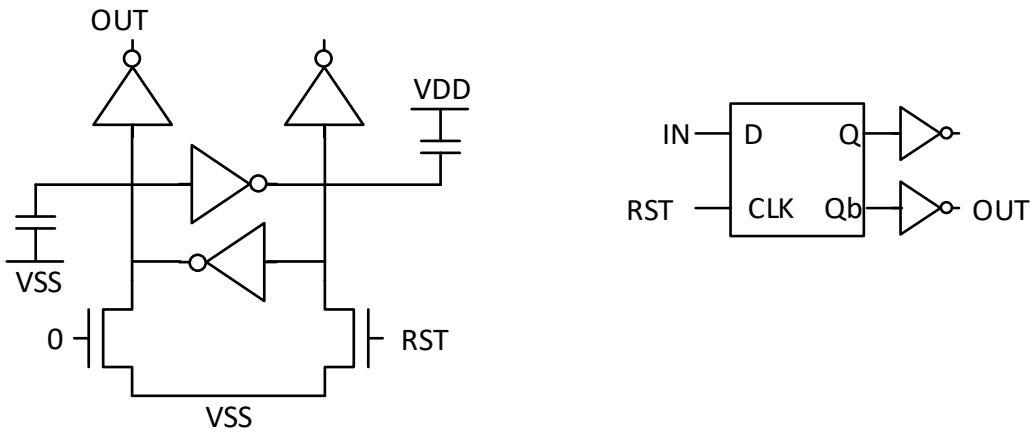


(a)



(b)

Figure 4.22: Simulated on-chip supply voltages of the 65-nm test chip during (a) +4 kV and (b) -4 kV ESD gun discharges in the tethered setup. $V25 = VDDIO - VSS, V12 = VDD - VSS$. The ESD current is injected to IO7. This IO is powered by VDDIO and is protected by dual diodes.



(a) (b)

Figure 4.23: Monitor circuits on the 65-nm test chip. (a) Cross-coupled inverter with unbalanced capacitive load; (b) D-latch that resets to logic low. The reset signal (RST) is generated off-chip and goes through an on-chip 100-ns RC filter before it arrives at the monitors.

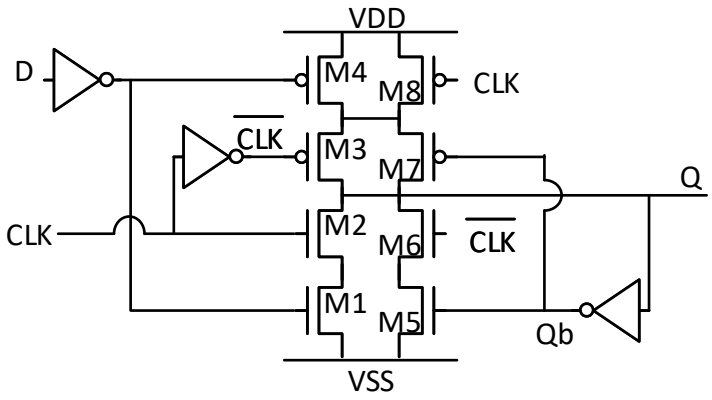


Figure 4.24: Circuit schematic for the D-latch in Figure 4.23. All PMOS devices have W =720 nm and L = 60 nm; all NMOS devices have $W = 360$ nm and $L = 60$ nm.

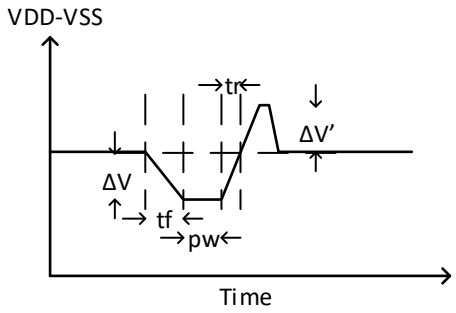


Figure 4.25: Waveform of the on-chip supply used to study upsets in the voltage monitors on the 65-nm test chip.

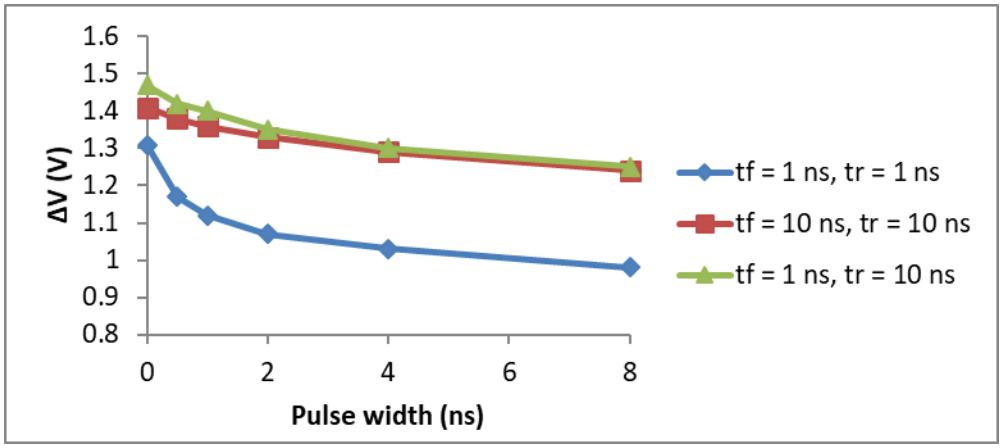


Figure 4.26: Minimum supply fluctuation ΔV needed to cause an upset in the cross-coupled inverter. The waveform of the supply disturbance is shown in Figure 4.25.

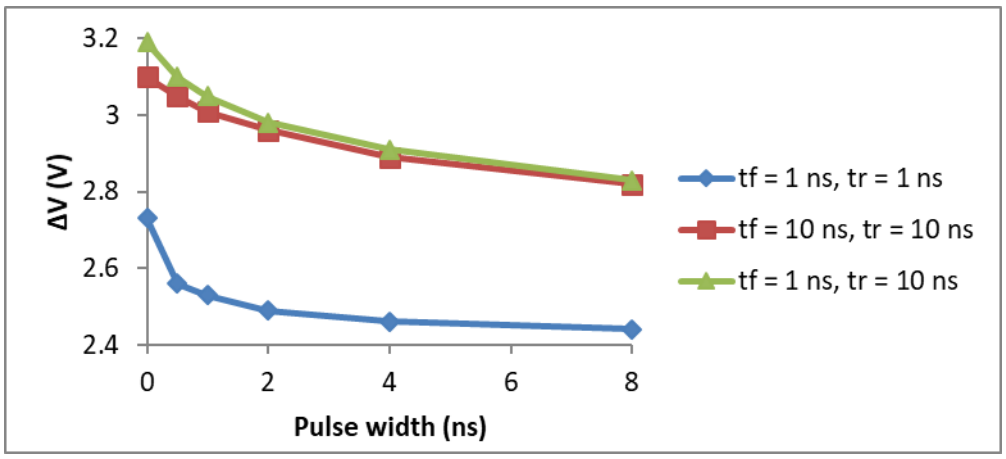


Figure 4.27: Minimum supply fluctuation ΔV needed to cause an upset in the D-latch. The waveform of the supply disturbance is shown in Figure 4.25.

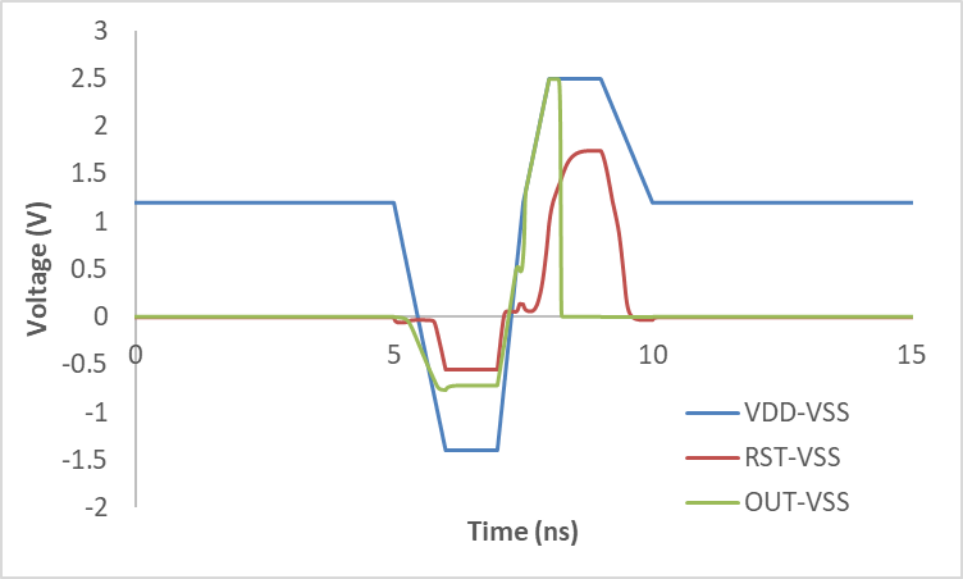


Figure 4.28: Simulation of a D-latch upset erased by an upset on RST, when there is a large amplitude of over-voltage transient in the VDD domain. The potential of the on-chip power net, VDD, drops temporarily below VSS, causing a discharge in the parasitic capacitances in the load. The output will then be capacitively coupled high during the recovery. With the overshoot of on-chip supply, RST can also be coupled high, erasing the upset at OUT.

Table 4.3: IEC levels to cause upsets in the monitor circuits on the 65-nm test chip.

	Positive		Negative	
	Measurement	Simulation	Measurement	Simulation
Cross-coupled inverter	≥ 2 kV	≥ 1 kV	≥ 2 kV	≥ 1 kV
D-latch	≥4 kV	≥ 3 kV	≥ 8 kV	≥ 8 kV

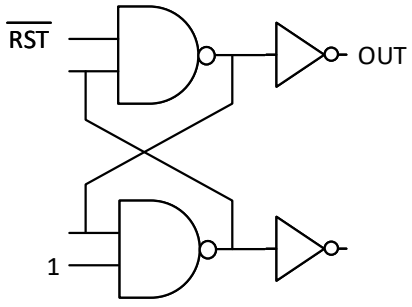


Figure 4.29: Schematic of the SR-latch on the 65-nm test chip.

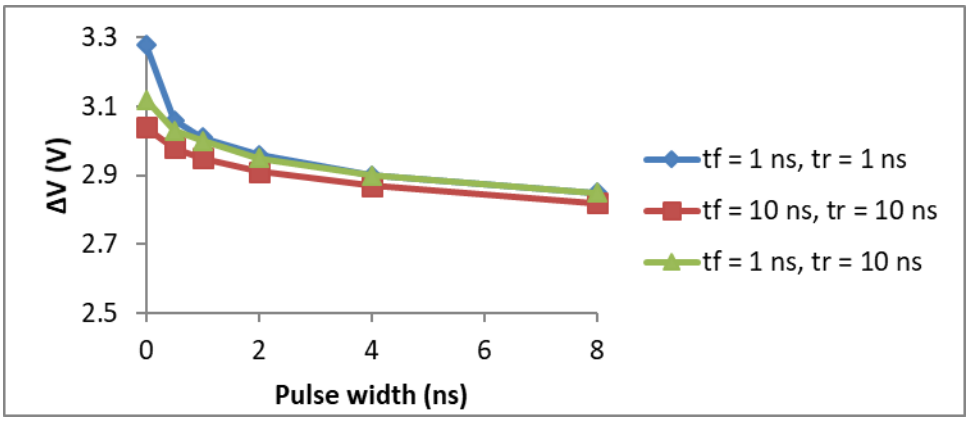


Figure 4.30: Minimum supply fluctuation ΔV according to the waveform shown in Figure 4.25 needed to cause an upset in the SR-latch.

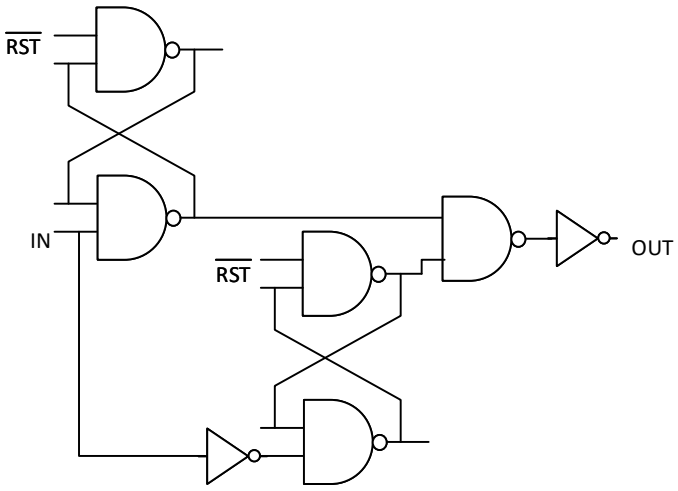


Figure 4.31: Schematic of the glitch detector on the 65-nm test chip.

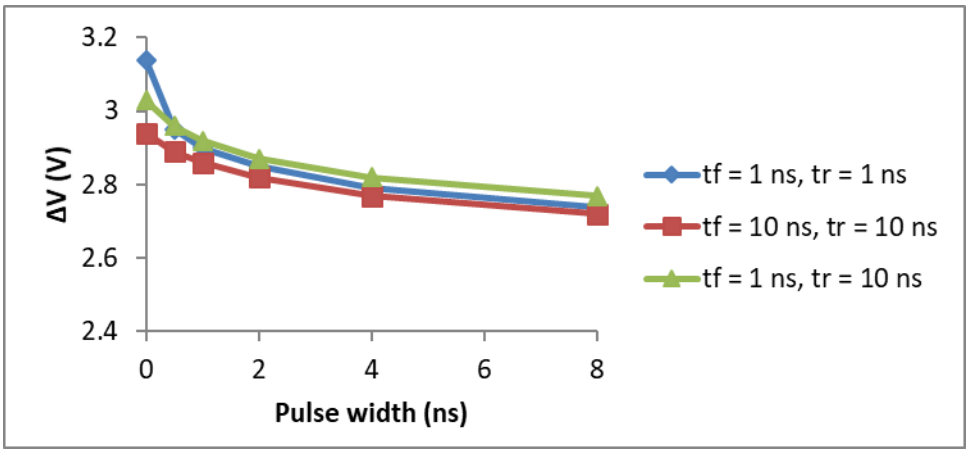


Figure 4.32: Minimum supply fluctuation ΔV according to the waveform shown in Figure 4.25 needed to cause an upset in the GD when the input is normally at logic high.

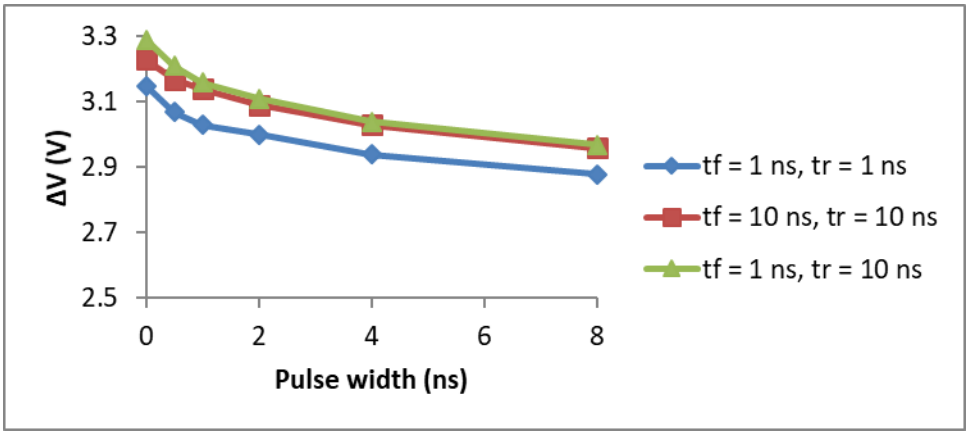


Figure 4.33: Minimum supply fluctuation ΔV according to the waveform shown in Figure 4.25 needed to cause an upset in the GD when the input is normally at logic low.

CHAPTER 5

SUPPLY INSTABILITY CAUSED BY THE RAIL CLAMP

5.1 Rail clamp stability analysis

There is an additional concern for power integrity during system-level ESD related to the rail clamp stability. A typical rail clamp design is shown in Figure 5.1 [46]. This design works well during power-off ESD, but not during the power-on case. During the normal operation of the IC, the BigFET in the rail clamp is off, and there is only leakage current. In response to an over-voltage transient, the RC timer turns on the BigFET through inverter stages and the BigFET shunts the ESD current to its ground rail. This circuit works as an amplifier with unity feedback, as shown in Figure 5.2, where the input is VDD that connects to the trigger circuit and the output is VDD that connects to the BigFET. The loop is closed with unity-gain feedback since VDD is a common node for the BigFET and the trigger circuit.

Oscillation will occur if the phase margin associated with the feedback loop becomes negative. The phase of the loop gain is determined by the trigger circuit poles. The poles are not fixed; they move to higher frequencies when the on-resistance of the transistors in the trigger circuit becomes smaller, which occurs as the ESD current rises. This suggests that rail clamp instability, which will cause ringing of the on-chip supply, may be more

likely to occur in response to a relatively low-amplitude static discharge than to a high-amplitude one. Ringing on the supply line will deteriorate the chip power integrity, potentially corrupting the data in the system.

In theory, an active clamp with a limited gain [47] and high bandwidth will be most stable [39]. It is important to note that the trigger circuit for a conventional active clamp [46] is comprised of CMOS inverters and, when the clamp triggers under power-on conditions, each inverter is biased in its high gain state. Designs with reduced gain have been proposed for system-level ESD protection [47], [48].

The location of the pole at the drain of the BigFET depends on self-impedance of the PDN. If the amount of decap is very large, due to a large on-chip decap or a combination of on- and off- chip decap with a small package inductance, the BigFET will not turn on thanks to the regulation provided by decap. Otherwise, the pole at the drain of the BigFET affects stability of supply during ESD, depending on the rail clamp as well as the amount of decap that is placed on the IC.

Two rail-clamp designs [40] were implemented as standalone test structures on the 65-nm test chip. The schematics are shown in Figure 5.3. The rail clamp with a three-stage trigger circuit shown on the left is inherently more likely to be unstable, regardless of the amount of decap between VDD and VSS. The rail clamp with a two-stage trigger circuit has two instantiations on the test chip: one with 20-pF decap and one without. For this rail clamp, the dominant pole is at the output of the second stage in the trigger circuit. The output pole at the drain of the BigFET affects the stability if it lies close to the poles of the trigger circuit, a situation that occurs when the amount of the decoupling capacitance is not negligible. For the circuit shown in Figure 5.3 with the 20-pF decap,

the output pole actually lies between the two poles of the trigger circuit. Thus it is expected that the two-stage rail clamp without the decoupling capacitor will be more stable.

Small-signal analysis of the three rail clamp test circuits is conducted by means of AC circuit simulation and the results, shown in Figure 5.4, are consistent with the preceding analysis. The only rail clamp that has a positive phase margin is the one that has a two-stage trigger circuit and no decoupling capacitance. The other two rail clamps have negative phase margins and may be susceptible to sustained ringing of the supply voltage during ESD.

Figure 5.5 shows the resonant frequency of the two-stage rail clamp with decap obtained in AC simulation. AC simulation suggests that the two-stage rail clamp has positive phase margin for ESD currents higher than 1.6 A, so the data-plot only covers lower current levels. The stability of the rail-clamp is improved at higher ESD currents.

The results of AC analysis may not be definitive since the on-chip waveforms during ESD cannot be considered to be "small-signal." Therefore, transient simulation was also performed; the ESD stimulus is assumed to be a square current pulse with 1 ns rise time. The results are shown in Figure 5.6 and are qualitatively consistent with the AC analysis. High amplitude ringing is predicted for the three-stage rail clamp, and the significant excursions below the nominal supply voltage of 2.5 V threaten the data integrity of any low noise-margin circuits connected to this supply. The two-stage rail clamp with the 20-pF decap shows a much reduced amplitude of oscillation during ESD since it is only marginally unstable; without the capacitor, the circuit is stable and there is no sustained ringing.

The test conditions used for the transient simulation were reproduced in the laboratory using the set-up shown in Figure 5.7. The measurement results are shown in Figure 5.8. The three-stage rail clamp cannot stabilize the supply voltage against the ESD disturbance. The two-stage rail clamp with the decoupling capacitor performs better, but the decoupling capacitor degrades its stability, as predicted. The measurement results shown in the figure are qualitatively very similar to the simulated ones. Quantitative differences between measurement and simulation are attributed to two factors: (1) an imperfect representation of the bias-tee and the DC supply; (2) BigFET breakdown was not included in the simulation model although in reality it limits the maximum voltage excursion on VDD.

A one-stage rail clamp is the most straightforward way to avoid the stability issue by having the least number of poles. The trade-off is that the capacitor in the RC timer needs to be made larger to drive the trigger circuit. The last stage in the trigger circuit is sized to quickly turn on the BigFET and avoid an excessive amount of supply voltage transient overshoot. The size of the BigFET is determined based on the target of the ESD passing level, which determines the amount of the ESD current the BigFET should be able to handle before its drain-to-source voltage, i.e., the on-chip supply voltage, rises beyond the transistor's safe operating area (SOA). The parasitic capacitances in the trigger stage, which increase with the size of the transistors, form a capacitive divider with the RC timer as shown in Figure 5.9 and will affect the turn on voltage in ESD.

5.2 Figures

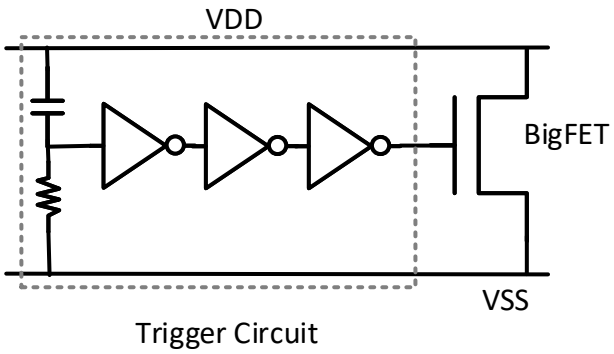


Figure 5.1: A typical rail-clamp design.

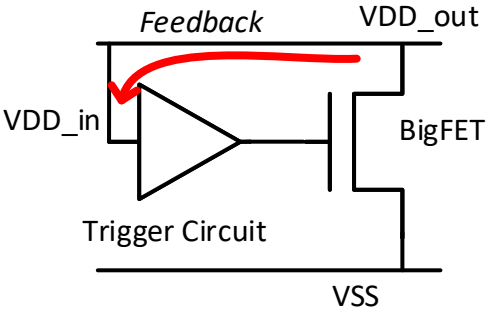


Figure 5.2: Feedback loop in rail clamp.

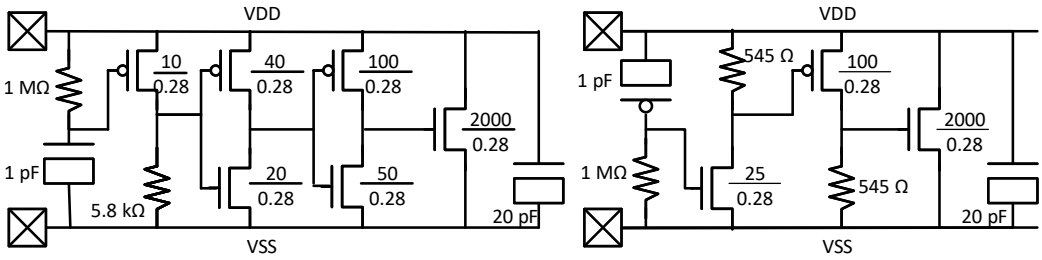


Figure 5.3: Rail clamp test structures used on the 65-nm test chip. The one on the left contains a three-stage trigger circuit, and the one on the right contains a two-stage trigger circuit. There is a third structure of the same rail clamp shown on the right, without the 20-pF decap.

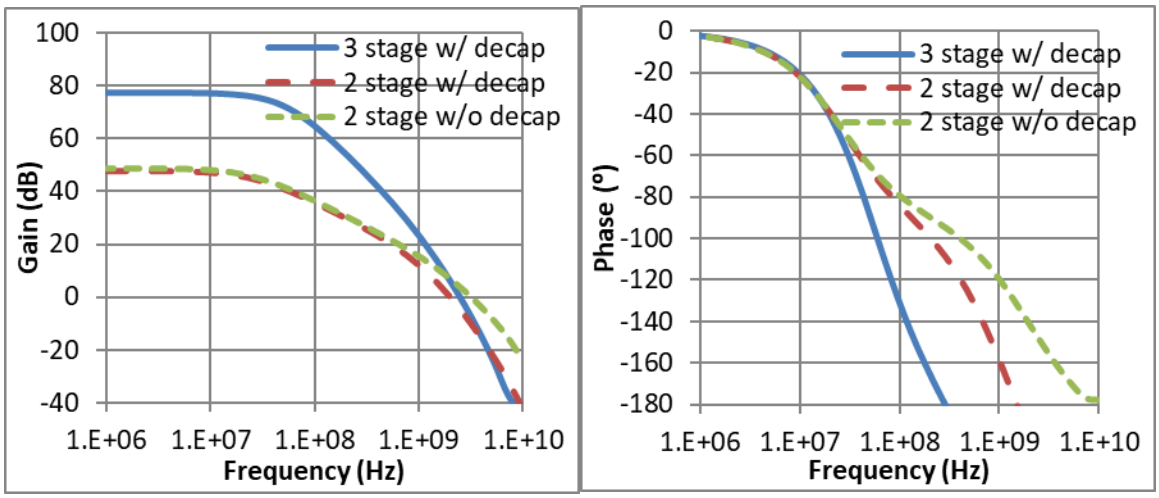


Figure 5.4: AC response of the three rail clamps on the 65-nm test chip.

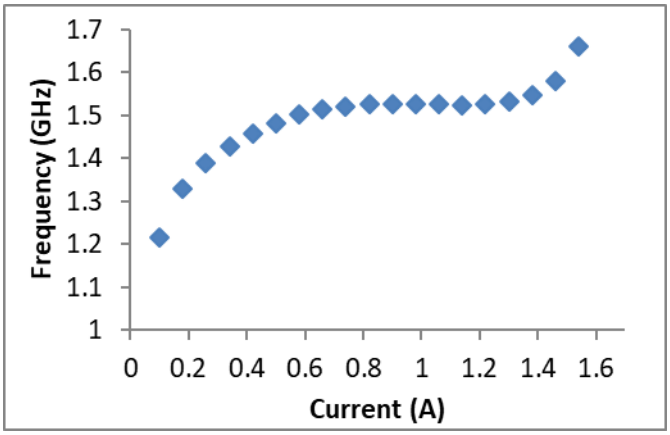


Figure 5.5: Simulated oscillation frequency for the two-stage rail clamp with the decap in AC analysis.

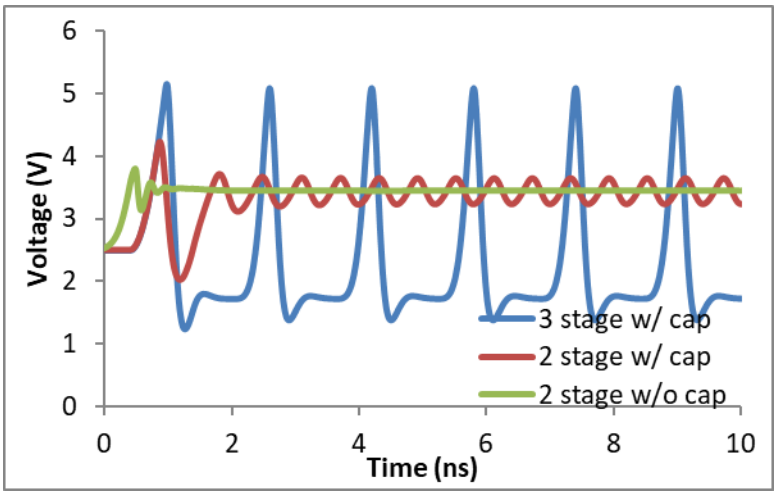


Figure 5.6: Simulated voltage across each of the three rail clamps in power-on condition during a 10-ns ESD current pulse. The amplitude of the pulse is 0.6 A, and the rise time is 1 ns. The schematics of the rail clamps are as shown in Figure 5.3.

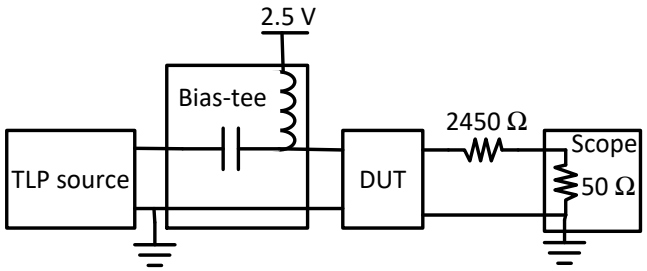


Figure 5.7: Experiment setup for TLP measurement on the rail clamps.

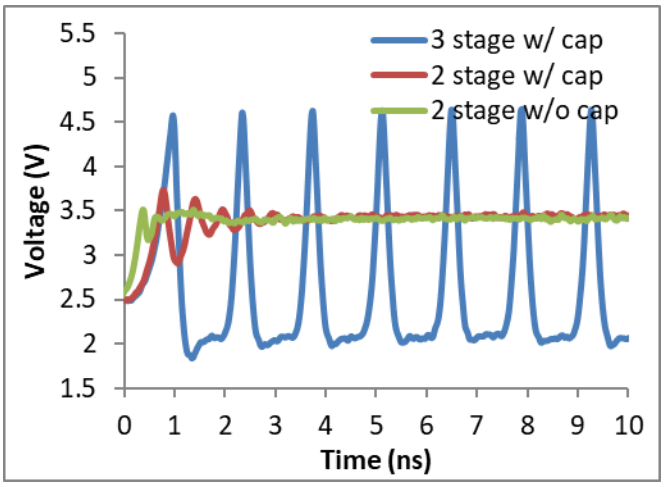


Figure 5.8: Measured $(VDD - VSS)$ of the three rail clamps in response to TLP at 0.6 A with 1 ns rise time and 10 ns pulse width on top of the 2.5-V DC bias.

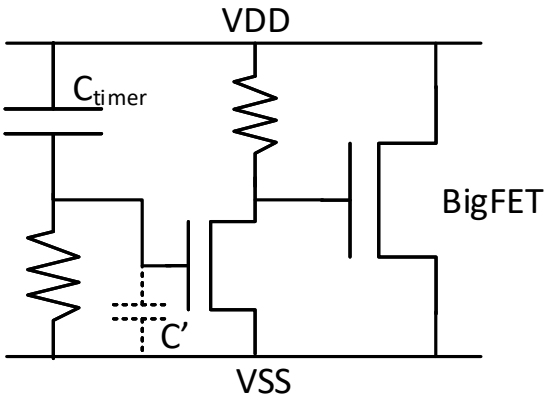


Figure 5.9: Schematic of a rail clamp with a one-stage trigger circuit. The capacitive voltage division between C_{timer} and C' in the trigger circuit may affect the turn on voltage of the rail clamp in ESD.

CHAPTER 6

POWER INTEGRITY OF INTERNALLY GENERATED SUPPLIES DURING ESD

The on-chip supply voltage can be generated externally or internally. Externally generated supplies rely on off-chip voltage regulators to provide supply currents to the IC directly. Voltage regulators are usually necessary to convert the output of a power source, such as a battery or the AC line, to a stabilized DC voltage required by the IC. Internally generated supplies have a voltage regulator on-chip to complete the conversion. Internally generated supplies are widely used to generate a low supply voltage (VDD) for the core circuitry from the higher supply voltage used in the IO domain (VDDIO). Relative to off-chip voltage regulators, on-chip LDO regulators provide a higher level of integration and improve noise immunity and power efficiency. However, it remains a question whether an internally generated power supply is also able to isolate the core supply from the ESD-induced fluctuations on the IO supply, and whether the on-chip LDO will continue to operate properly during a power-on ESD event. It has been shown in the previous chapters that on-chip supplies powered by off-chip regulators are subject to large amplitude voltage fluctuations induced by ESD currents. Prior works showed that an internally generated supply can be disturbed by the excessive substrate current resulting from a static discharge [49], [50].

In this chapter, it will be shown that an internally generated supply may be able to maintain its power integrity during ESD, depending on the impedance of the current path through the off-chip decap. The regulator needs to compensate the noise induced by this current path [51].

In addition, the configuration of on-chip ground nets affects the characteristics of the supply noise induced on the internally regulated domain. On-chip ground nets are usually connected by APDs. The APDs are used for a balance between reliability and noise isolation. During ESD, the APDs limit the potential difference across different domains to protect circuits that are connected to more than one supply. In normal operation, the APDs are off to isolate noise. The on-chip regulator may draw the power from one supply referenced to one ground net and provide the power to the internally regulated domain connected to a different ground net. In such cases, the potential difference between the two ground nets becomes a source to inject supply noise in the internally regulated domain if the amount of on-chip decap in this domain is insufficient. However, the required amount of on-chip decap to mitigate the supply noise caused by this mechanism is for most designs comparable to that needed to minimize supply voltage fluctuations due to a change in load currents.

When the on-chip regulator is an LDO with a PMOS pass transistor, there can be a discharge of the internally regulated domain through the parasitic diode. The discharge occurs when the supply from which the regulator sources its power collapses. A well bias voltage control circuit for this PMOS device can mitigate the problem.

Figure 6.1 shows a typical LDO used for on-chip voltage regulation [52]. In the figure, the LDO draws power from VDDIO. Alternatively, the LDO can draw power from a

Vbias pin, and the Vbias pin is connected to on-board VDDIO. If powered from a dedicated Vbias pin, the regulator is not subject to the SSN from the IO circuitry in the VDDIO domain. However, the supply voltage of the regulator, i.e., Vbias with respect to the on-chip ground, is still subject to noise during ESD. It is affected in a similar manner as is VDD discussed in Section 4.1.2. In addition, any ESD-induced noise on the board-level supply will appear on Vbias.

A well-designed LDO will have a large power-supply rejection ratio (PSRR); this will prevent ESD-induced supply fluctuations on VDDIO from propagating to VDD. The supply fluctuation can be considered as a noise source to the LDO. The stability is a major concern when designing an LDO. A stable design is achieved by ensuring that the circuit's dominant pole lies at a significantly lower frequency than do the others. Decoupling capacitance C_{DD} is placed on VDD to minimize voltage fluctuations when the load changes, e.g., when the current being drawn from VDD changes due to logic activity. An LDO cannot instantly respond to a rapid change of load, due to its limited bandwidth. If the required decoupling capacitance is large, it is reasonable to place the dominant pole at the LDO output.

6.1 Experimental observation of ESD-induced noise on two internally regulated supply domains

Figure 6.2 shows two regulator designs. Design A was used on the 65-nm test chip. This regulator uses an NMOS pass transistor and can provide up to 5 mA of supply current. The dominant pole of this design was placed at the gate of the NMOS pass transistor by adding C_0. The decap at the output of the regulator is 1 pF.

For simplicity, the 1.2 V reference for the comparator was generated externally, but it passes through an on-chip low-pass filter that removes noise. The chip contains a single VSS bus that is common to the IO and core supply domains.

On the test chip, there are circuits as shown in Figure 4.23 in both the externally generated VDD (VDD_{ext}) domain and the internally generated one (VDD_{int}). ESD-induced upsets were observed for the VDD_{ext} domain (see Table 4.3), but none were observed for the VDD_{int} domain, up to ±6 kV.

Design B was used on the 130-nm CMOS test chip. This LDO can provide up to 18 mA of supply current. This regulator achieves stability if the decoupling capacitance at its output node, C_{chip}, is at least 60 pF, assuming that the load current is below 60 μA. The load current moves the location of the pole at the output of the regulator and affects its stability. However, to support larger load currents and to minimize the voltage fluctuations associated with load changes, a larger decoupling capacitance is needed. An additional 10-nF off-chip decap is place on-board, along with the 16-pF on-chip decap. The off-chip decaps are surface-mount devices, and they are placed close to the chip. Placing part of the VDD_{int} decap on the board requires that there is a pin connected to VDD_{int}, and therefore a rail clamp is placed on VDD_{int}. In contrast, the VDD_{int} supply on the previous (65-nm) test chip, which was isolated from the outside world, did not have a rail clamp.

For simplicity, the 1.5 V reference for the regulator was generated externally (VDD_{ext}). The reference voltage VDD_{ext} is unfiltered and will become noisy during system-level ESD but, since the bandwidth of the regulator is 120 kHz, the noise at the

reference will have minimal effect on VDD_{int}. The test chip contains two separate ground nets; VSSIO and VSS are connected through APDs.

The test chip with Design B contains power supply under-voltage and over-voltage monitor circuits, previously shown in Section 4.2, in its VDD_{ext} and VDD_{int} supply domains. ESD gun discharges were made to an IO pin and the measurement results are shown in Table 6.1. Evidently, the VDD_{int} domain is subject to an even larger amplitude of supply fluctuations than the VDD_{ext} domain. This finding is in marked contrast to that for Design A. Design B had not been expected to have worse ESD robustness than Design A. It had been expected to have somewhat better noise isolation between its power supply domains than did Design A, because it uses separate VSSIO and VSS buses.

6.2 Simulation and analysis

In this section, the contribution of various noise sources is analyzed in simulation. It is assumed for now that there is a shared VSS net on-chip. There are three possible sources of the ESD-induced noise on VDD_{int}: differential noise on VDDIO, differential noise on VDD_{ext}, and noise on VSS. To separate the contribution of each, the simulation setup of Figure 6.3 is used to inject noise from just one of the sources at a time. The voltage waveform used for each noise source is obtained from the ESD simulation results at -2 kV. These results are similar to those shown in Figure 4.16(b), where the ESD current injected to a bottom diode of the ESD protection at an IO induces noise on the supply and ground nets on-chip.

Figure 6.4 and Figure 6.5 show the effect of each noise source on the power integrity of VDD_{int}. For Design A, none of the sources generate a strong disturbance on VDD_{int}. For Design B, VSS noise generates supply noise, i.e., fluctuations of $(VDD_{int} - VSS)$. The simulation results indicate that Designs A and B are most different in their response to noise on VSS. Furthermore, VSS noise is the major source of the VDD_{int} supply voltage disturbance in Design B. Design B is sensitive to VSS noise in a similar manner as the externally generated VDD that has been discussed in Chapter 4.

Figure 6.6(a) shows the schematic used to explain the results of those simulations. ESD induces voltage fluctuations on both the VDDIO and VSS nets. The voltage fluctuations may be separated into the common-mode noise on VDDIO and VSS, $v_c(t)$, and the differential-mode noise, $v_d(t)$. The total effect is approximated by the linear superposition of the individual contributions from the two sources of noise. Figure 6.6(b) is used to analyze the effect of $v_d(t)$; it suggests that if the regulator has a large power supply rejection ratio, PSRR, the effect of the differential-mode noise will be small. However, in the actual circuit of Design B, the amplifier of Figure 6.2(b) is connected to VSSIO. This detail does not change the conclusion regarding the effect of $v_d(t)$, in part because the noise waveforms on the VSSIO and VSS nets are very similar. The PSRR of Design B is 40 dB at 10 MHz, which is sufficiently large such that the differential-mode noise between VDDIO and VSSIO (or, equivalently, between VDDIO and VSS) is rejected.

The circuit used to analyze the effect of the common-mode noise between VDDIO and VSS is shown in Figure 6.6(c) and this can be transformed to the equivalent schematic shown in Figure 6.6(d). The common-mode noise $v_c(t)$ in Figure 6.6(a) and (c) is the

ESD-current-induced voltage difference between the on-chip VSS net and the board ground net. It is given by

$$v_c(t) = L_{VSS}\frac{di_{LVSS}}{dt} \tag{6.1}$$

where i_{LVSS} is the ESD current exiting the chip through the bond-wires connected to VSS.

The magnitude of this noise increases with increasing L_{VSS} and $\frac{di_{LVSS}}{dt}$. Therefore, having a smaller package inductance connected to VSS or a smaller ESD current directed to VSS will improve the power integrity of the VDD_{int} domain. This is consistent with the previous analysis of power integrity in a supply domain without an integrated voltage regulator.

Figure 6.7(a) includes more details of the LDO circuit shown in Figure 6.6(d). C_1 represents the sum of the decap in the VDD_{int} domain and the parasitic capacitance of the pass transistor, M_p, connected to $ivdd$. M_p is driven by an amplifier with a transfer function $A(s)$; this amplifier is comprised of an error amplifier and the buffer stage that drives the PMOS pass transistor. The loop in the LDO is closed by a feedback stage with a transfer function $f(s)$. In this analysis, it is assumed that the reference voltage, REF, is quiet with respect to VSS, which is the ground in Figure 6.7. A quiet reference can be provided by a reference voltage generator, such as a bandgap reference, if low-pass filtering is applied at the output of the reference. The product $A(s)f(s)$ is approximated as

$$A(s)f(s) \approx \frac{A_{DC}f_{DC}}{1 + s/p_1} \tag{6.2}$$

where p_1 is the dominant pole in this product and the term $A_{DC}f_{DC}$ is large.

Condition (6.2) is used to formulate LDO design guidelines such that the supply voltage fluctuation during ESD will be limited. The impedance looking into the output of the LDO, Z_1, is given by

$$Z_1 = \frac{1 + s/p_1}{A_{DC}f_{DC}g_{mp}} = sL_1 + R_1 \tag{6.3}$$

where

$$L_1 = \frac{1}{A_{DC}f_{DC}g_{mp}p_1} \tag{6.4}$$

$$R_1 = \frac{1}{A_{DC}f_{DC}g_{mp}} \tag{6.5}$$

and g_{mp} is the transconductance of the PMOS pass transistor. Condition (6.3) indicates that the LDO may be modeled by an inductor in series with a resistor, as shown in Figure 6.7(b).

To minimize the voltage fluctuations on vdd_{int} with respect to ground (vss), the voltage gain from v_c to vdd_{int} must be small.

$$\left|\frac{vdd_{int}(s)}{-v_c(s)}\right| = \left|\frac{Z_{on-chip}}{Z_{off-chip} + Z_{on-chip}}\right| \ll 1 \tag{6.6}$$

where

$$Z_{on-chip} = \frac{sL_1 + R_1}{s^2L_1C_1 + sC_1R_1 + 1} \tag{6.7}$$

$$Z_{off-chip} = R_0 + sL_0 + \frac{1}{sC_0} \tag{6.8}$$

A sufficient condition to satisfy Condition (6.6) is given in Condition (6.9) and an alternative sufficient condition is given in Condition (6.10).

$$C_1\left(4\pi^2 f^2 L_0 + \frac{1}{C_0}\right) \gg 1 \tag{6.9}$$

where f is in the range of several hundred MHz. Alternatively,

$$\begin{cases} L_1 \ll L_0 \\ R_1 \ll R_0 \end{cases} \Rightarrow \begin{cases} A_{DC} f_{DC} g_{mp} p_1 L_0 \gg 1 \\ A_{DC} f_{DC} g_{mp} R_0 \gg 1 \end{cases} \tag{6.10}$$

In essence, Conditions (6.9) and (6.10) indicate that the impedance of the on-chip path from $ivdd$ to vss must be much smaller than that of the off-chip path. Condition (6.10) suggests that the gain and bandwidth of the LDO be made large, since the gain is in proportion to $A_{DC} f_{DC} g_{mp}$, and the bandwidth may increase with increasing p_1. The test chip with Design B had poor power integrity during ESD because $C_{on-chip}$ does not satisfy Condition (6.9) and the LDO does not have a sufficiently high gain and bandwidth to compensate; additionally, the VDD_{int} bus routing in Design B uses a more resistive metal layer than does VDD_{ext}, which tends to make VDD_{int} relatively noisier.

6.3 Comparison of shared and separate on-chip ground nets

Separating on-chip ground nets provides noise isolation between supply domains. However, the noise isolation is incomplete, since APDs must be placed between the ground nets to provide component-level ESD protection. The separate ground nets connected by APDs should reduce the amplitude of noise voltages when the noise on VSSIO propagates to all the supply domains, although they cannot completely isolate the noise. In Section 6.2, the analysis assumes a shared ground net, while this section investigates the effect of separate ground nets with APDs in simulation.

Figure 6.8(a) shows the setup to simulate the supply noise in the VDD_{int} domain regulated by Design B in Section 6.1 when a noise voltage is excited on VSSIO. The noise voltage is obtained from a discharge at -2 kV to an IO protected by dual diodes. Figure 6.8(b) shows that the VDD_{int} domain is quiet even though the VSSIO voltage is noisy with respect to the board ground. It is not necessary to have a large amount of the VDD_{int} decap (i.e., less than 100 pF) to maintain a quiet supply voltage. In the same figure, it is also shown that when the dominant pole of the design is moved from the output (VDD_{int}) to the gate of the PMOS pass transistor, the VDD_{int} domain is still reasonably quiet.

Figure 6.9(a) shows the setup to simulate the supply noise in the VDD_{int} domain regulated by Design A in Section 6.1 when the noise voltage obtained from a discharge at -2 kV is excited on VSSIO. Figure 6.9(b) shows that the VDD_{int} domain is vulnerable to the VSSIO noise in this case. This is caused by the insufficient 1-pF decap in the VDD_{int} domain, and it is not relevant to the fact that this design uses an NMOS pass transistor or that the dominant pole is at the gate of the NMOS. Another design with an NMOS pass transistor and the dominant pole at the gate of the NMOS implemented within the 130-nm technology can generate a quiet VDD_{int} domain with 300-pF decap, as shown in Figure 6.10. This design has the similar problem as the one on the 65-nm test chip if the VDD_{int} decap is reduced to 1 pF.

The simulations above indicate that the potential difference between the VSSIO net and the VSS net is generally not a problem for the internally regulated domains when there is enough on-chip decap and no off-chip decap.

With separate ground nets, the amplitude of noise voltage on the VSS net can be reduced, which benefits designs requiring off-chip decap. Figure 6.11 shows the simulation setup to compare of the amount of supply noise in the VDD_{int} domains with different amounts of decap and ground net configurations. These domains are regulated by Design B of Section 6.1. Figure 6.12 and Figure 6.13 show the simulation results when an ESD current at 2 kV is discharged to an IO in the VDDIO domain. It is observed that the amplitude of the coupled VSS noise is reduced by 1 V, which is the turn-on voltage of the APDs during ESD. The mitigated VSS noise decreases the amount of supply noise in the VDD_{int} domain, since the supply noise is mainly caused by the different ground reference potentials between the circuitry on-chip and the decap off-chip. As shown in Figure 6.14, when all the VDD_{int} decap is on chip, the VDD_{int} domain remains quiet regardless whether the ground nets of the VDDIO domain and the VDD_{int} domain are separate or shared. Figure 6.15 confirms that a regulator with its dominant pole at the gate of the pass transistor can maintain a quiet VDD_{int} supply if it has on-chip decap only, regardless of the on-chip ground net configuration.

Figure 6.16 illustrates the simulation result of Design A in Section 6.1. Although the regulator uses on-chip decap only for the VDD_{int} domain, it is observed that a larger amplitude of supply noise is induced when the ground nets are separate. This is caused by the same mechanism by which a noisy VSSIO voltage induces supply noise to the VDD_{int} domain when the amount of the VDD_{int} decap is too small.

The previous analysis assumes that the amplitudes of noise in the VDDIO domain and on VSSIO are independent of whether the ground nets are separate or shared. However, the APDs restrict the ESD current to VSSIO and the connected package inductances. As

a result, the amplitude of the supply noise in the VDDIO domain increases, and this noise may couple to the regulators and affect the supply voltage of the VDD_{int} domain. As shown in Figure 6.17, this effect is more significant when the ESD current is directed to VSSIO by the protection circuit.

6.4 Noise at the VDDIO domain

Although integrated voltage regulators have a large PSRR, this small-signal characteristic does not always hold true when the amplitude of the noise on VDDIO with respect to VSSIO is large enough to cause a supply collapse in the VDDIO domain. Supply collapses in the VDDIO domains were not observed in the experimental results discussed in Section 6.1, but they will occur at higher IEC levels or in packages with larger inductances. Secondary discharges in IEC tests may also cause supply collapses [53], [54]. Secondary discharges occur after the ESD gun discharges to a floating metal object and the tethered EUT containing the IC is nearby. The electric field between the charged object and the EUT increases until a spark forms in between. In a contact IEC discharge, the 330 Ω resistor in the gun limits the current of the second current peak when the 150 pF capacitor discharges. In this secondary discharge, the current is limited only by the spark resistance. The resistance quickly decreases to tens of ohms within 1 ns after the spark forms, and the current amplitude is therefore large. In particular, when the IOs in the VDDIO domain are protected by local clamps, positive discharges may lead to large amplitudes of under-voltages in the VDDIO domain. There may be a supply collapse in the VDDIO domain, and during the collapse, the VDD_{int} supply is at a higher potential than the VDDIO potential. In these cases, it is possible that the VDD_{int} supply

discharges to the VDDIO one through the pass transistor in the regulator. As a result, a significant drop on the VDD_{int} supply voltage appears.

In order to compare the response of different regulators to a supply collapse in the VDDIO domain, four regulators in the 130-nm technology were designed and simulated. These regulators have different types of pass transistors, pole locations and amount of VDD_{int} decap. Design 1, with the topology shown in Figure 6.18(a), uses the PMOS as the pass transistor that supplies the current to VDD_{int}, and the dominant pole is at the output (VDD_{int}) of the regulator. Design 2, with the topology shown in Figure 6.18(b), uses the NMOS as the pass transistor, and the dominant pole is at the gate of this NMOS. Design 3 moves the pole of Design 1 to the gate of the PMOS. Design 4 is the same as Design 2 except that the amount of output capacitance is reduced.

The properties of the four designs are shown in Table 6.2. The first two designs have a similar open-loop DC gain (50-60 dB) and closed-loop bandwidth (800 kHz – 4 MHz) when the load current is small (several hundred μA). The amounts of decap in the VDD_{int} domain are also similar. Design 3 has a much smaller amount of VDD_{int} decap and a larger bandwidth, and Design 4 has similar characteristics to Design 2 although the amount of VDD_{int} decap is much smaller. All of these regulators can support more than 10 mA of maximal DC current with less than 3% gain error.

The four regulators are simulated for the case where there is a supply collapse in the VDDIO domain for one nanosecond. The potentials at the gate of the pass PMOS or NMOS transistors, and the supply voltage of the VDD_{int} domain, i.e., $(VDD_{int} - VSS)$, are shown in Figure 6.19. It can be observed that there is a significant under-voltage event in all the VDD_{int} domains except for the one regulated by Design 2. The VDD_{int}

domain regulated by Design 1 has a smaller amplitude of under-voltage than those regulated by Designs 3 and 4.

The under-voltage event in the VDD_{int} domain results from the discharging of the VDD_{int} decap through the pass transistor to the VDDIO net, the voltage of which approaches zero. When a PMOS pass transistor is used, most of the stored charge on the VDD_{int} decap is discharged through its forward biased body diode. The potential on the VDD_{int} net cannot be well-maintained unless the amount of VDD_{int} decap is huge (e.g., >10 nF for Design 1). The transient potential at the gate of the PMOS has little effect on the discharge.

When, instead, an NMOS pass transistor is used, VDD_{int} discharges more slowly during the VDDIO collapse, assuming the body of the NMOS is tied to the on-chip ground net. Note, however, that the NMOS is in its on-state during this time, due to the limited capability of its gate potential to respond to the collapse. In the normal operation, the NMOS is on to source current to the load circuitry in the VDD_{int} domain. The amplifier in the regulator is not fast or reliable enough to immediately turn it off during the VDDIO collapse. While the NMOS remains its on-state, its MOS current starts to discharge the decap. Therefore, if the output decap is too small, such as the one in Design 4, the VDD_{int} voltage cannot be well-maintained.

On the 65-nm test chip, large amplitudes of supply fluctuations in the VDD_{int} domain were not observed from the outputs of the monitors. The simulation on this test chip indicates that a VDDIO collapse is unlikely. The VDD_{ext} rail clamps are quite resistive when they turn on, which prevents the VDDIO collapse (see Section 4.1.2). The effective on-resistance of these rail clamps are larger than those on the 130-nm test chip due to a

different size of the BigFET in a different technology and the more resistive metal buses. Therefore, the simulation results presented here are consistent with the measurement results shown in Section 6.1.

If the NMOS is placed in a triple well and its body is shorted to its source, VDD_{int}, there is a diode junction between the isolated P-well and the N-well isolation. The N-well isolation is tied to a voltage that is higher than VDD_{int}. The VDD_{int} domain may discharge through this diode junction during a voltage collapse at the N-well bias. Therefore, placing the NMOS in a triple well does not always prevent the discharge of VDD_{int} due to the collapse of another on-chip supply

The comparison of the four designs confirms that the VDD_{int} voltage may decrease during a supply collapse in the VDDIO domain and that the magnitude of the disturbance is not related to the location of the dominant pole in the regulator but is strongly influenced by the type of the pass transistor. The PMOS pass transistor inherently poses a greater challenge than the NMOS one because of the forward-biased body diode during the collapse. However, PMOS pass transistors are predominantly used in regulator designs because of their low drop-out voltage. Therefore, for these regulators, it is necessary to hold the N-well bias voltage above the VDD_{int} voltage to maintain power integrity during power-on ESD. A well-bias control circuit that always connects the N-well bias voltage to the higher of VDDIO voltage and VDD_{int} voltage is needed to prevent the discharge through the diode path. There is also a requirement on the minimum decap in the VDD_{int} domain to prevent excessive discharging due to the transistor current when the VDDIO voltage collapses. If the amount of decap is limited, it is desired to turn-off the pass transistor during ESD.

6.5 Figures and tables

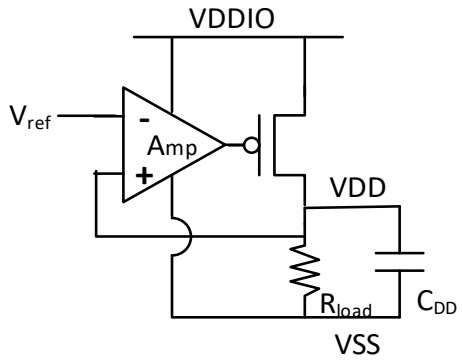
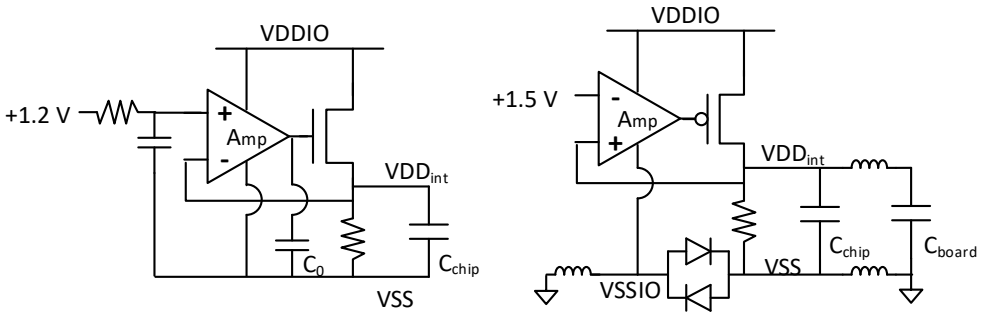


Figure 6.1: On-chip voltage regulator. R_{DD} represents the load of the VDD domain. C_{DD} can be placed on-chip or off-chip.

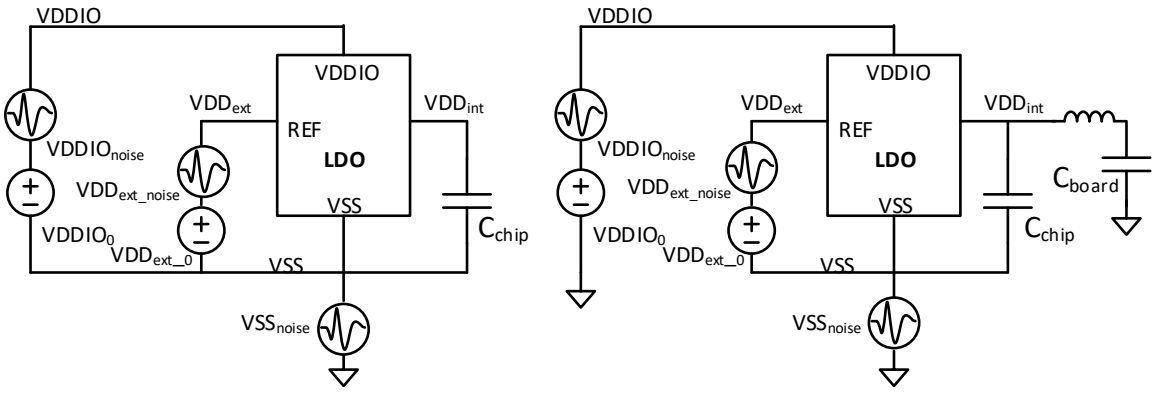


(a) (b)

Figure 6.2: Two voltage regulators used for comparison during system-level ESD. Design A (a) was fabricated on the 65-nm test chip. Design B (b) was fabricated on the 130-nm test chip. It requires additional off-chip decap, C_{board}.

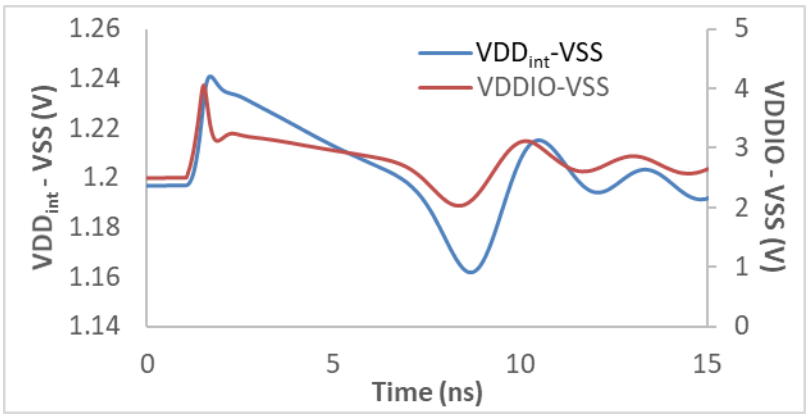
Table 6.1: Supply voltage monitors outputs after discharges compliant to IEC 61000-4-2 at two IOs in the VDDIO domain of the 130-nm test chip. The results are combined of mobile and tethered discharges. UV: under-voltage; OV: over-voltage.

	Dual-diode protected IO				SCR and reverse diode protected IO			
V_{IEC} (kV)	VDD_{ext} UV	VDD_{int} UV	VDD_{ext} OV	VDD_{int} OV	VDD_{ext} UV	VDD_{int} UV	VDD_{ext} OV	VDD_{int} OV
-5	2	3	2	2	2	3	2	2
-4	1	3	2	2	2	3	2	2
-3	1	3	1	2	1	3	2	2
-2	1	2	1	2	1	3	1	2
-1.5	1	1	1	1	1	2	1	1
-1	1	1	1	1	1	2	1	1
-0.5	0	1	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0
0.5	0	1	0	1	0	1	0	1
1	1	1	1	1	0	1	0	1
1.5	1	3	1	2	1	2	1	1
2	1	3	1	2	2	3	1	2
3	2	3	1	2	3	3	1	2
4	3	3	2	2	3	3	2	2
5	3	3	2	2	3	3	2	2

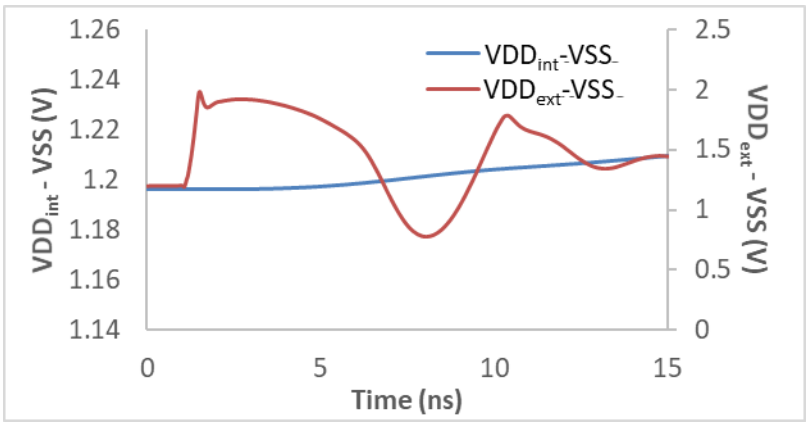


(a) (b)

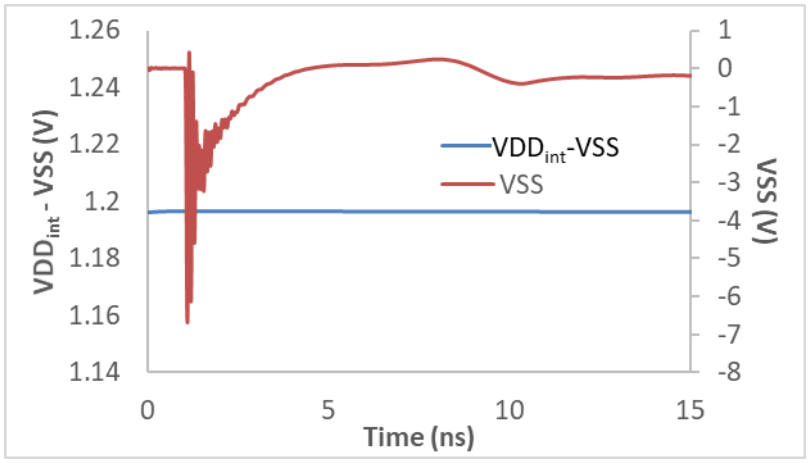
Figure 6.3: Supply noise simulation setup for (a) Design A and (b) Design B shown in Figure 6.2. Only one noise source is active in a single simulation. The simulation assumes a shared VSS net on-chip for all the power-domains.



(a)

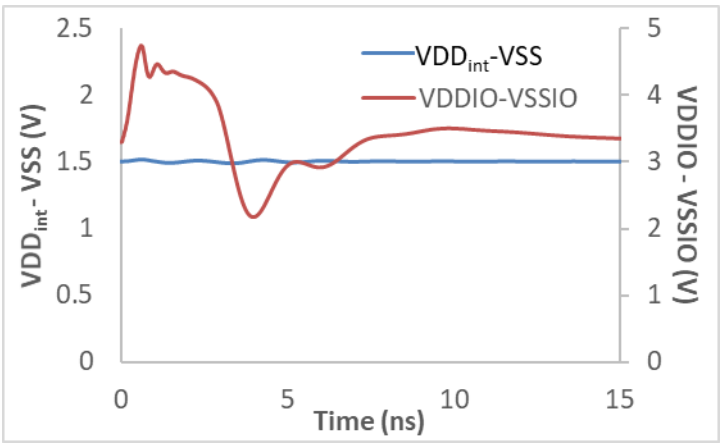


(b)

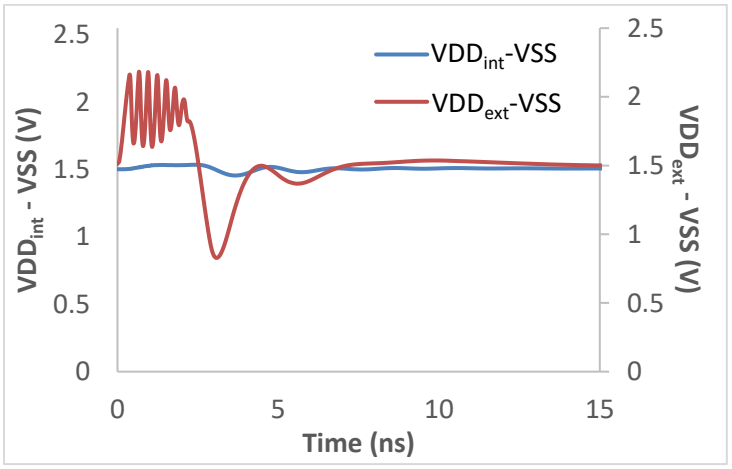


(c)

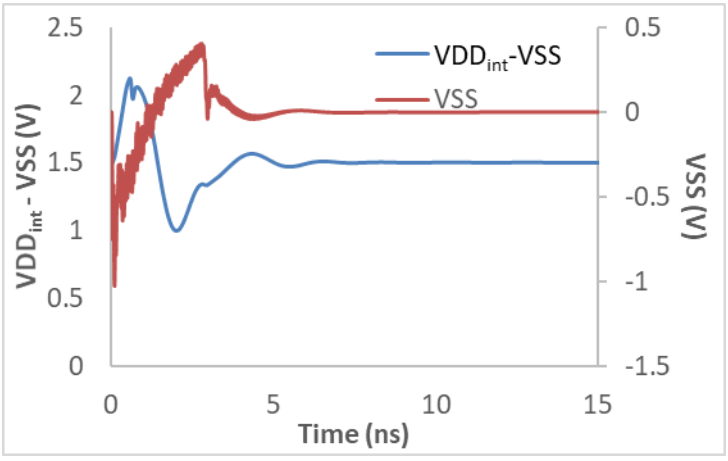
Figure 6.4: Design A. Simulated response of VDD_{int} to various noise sources. (a) Noise on $(VDDIO - VSS)$. (b) Noise on $(VDD_{ext} - VSS)$. (c) Noise on VSS.



(a)



(b)



(c)

Figure 6.5: Design B. Simulated response of VDD$_{int}$ to various noise sources. (a) Noise on $(VDDIO - VSS)$. (b) Noise on $(VDD_{ext} - VSS)$. (c) Noise on VSS.

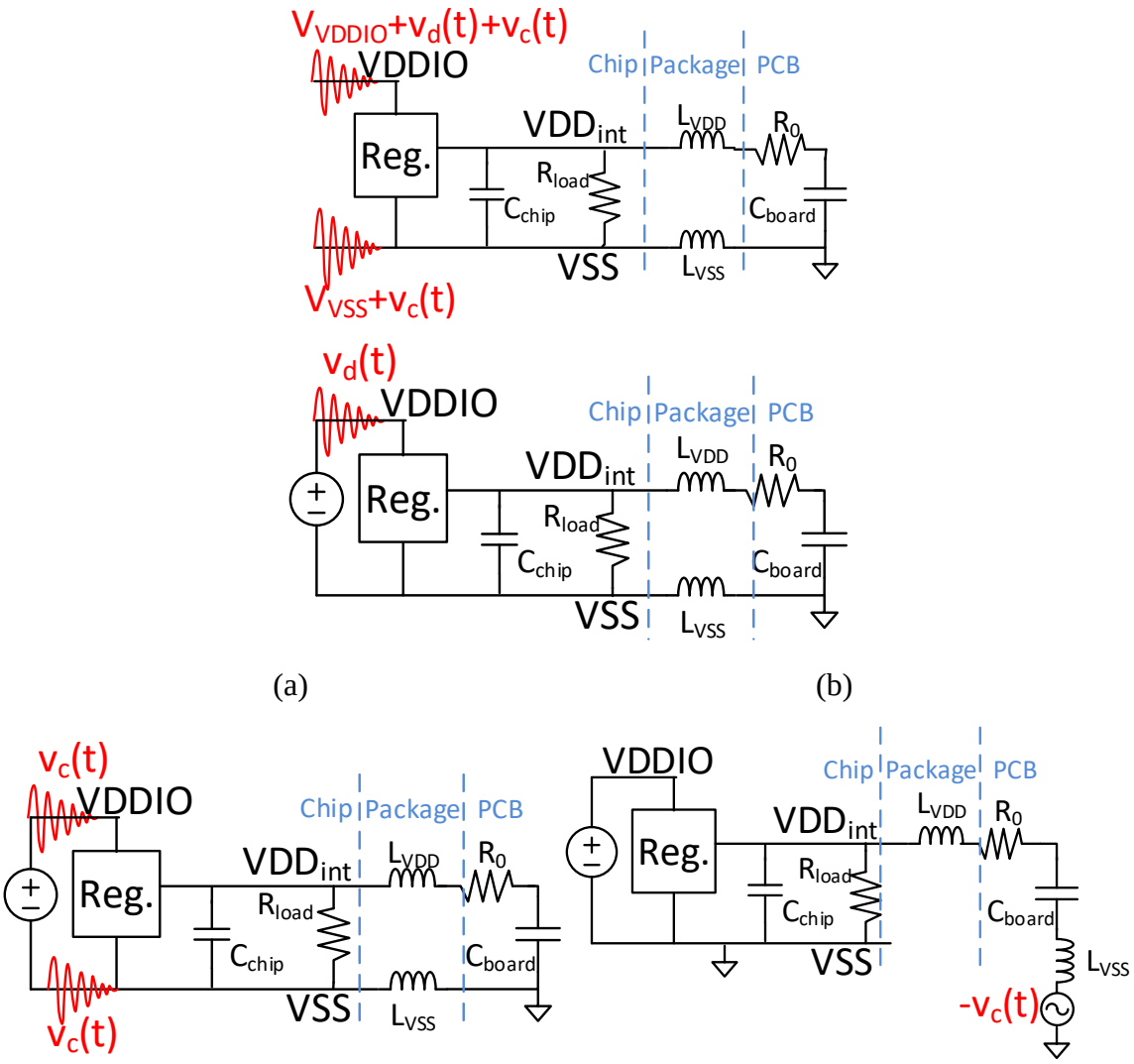
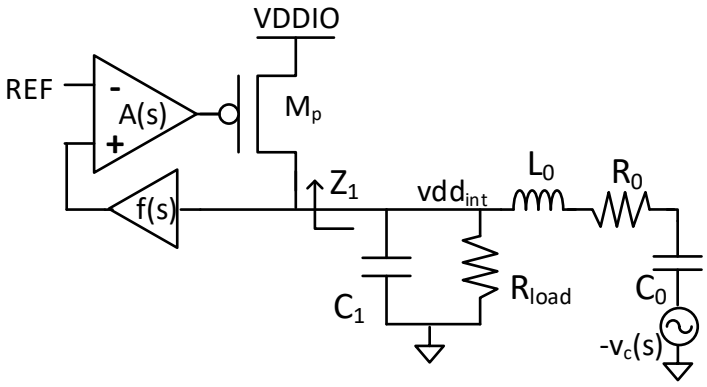
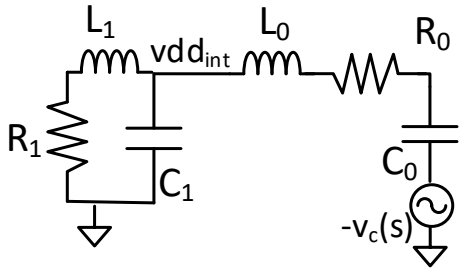


Figure 6.6: (a) The ESD current induces noise voltages on both VDDIO and VSS. $v_d(t)$ is the differential noise voltage between VDDIO and VSS. $v_c(t)$ is the common noise voltage between VDDIO and VSS. For linear circuits, the total effect is a superposition of the effect of $v_d(t)$ and $v_c(t)$ separately, as shown in (b) and (c). The circuit shown in (d) is equivalent to the one in (c) for studying the noise on $(VDD_{int} - VSS)$.

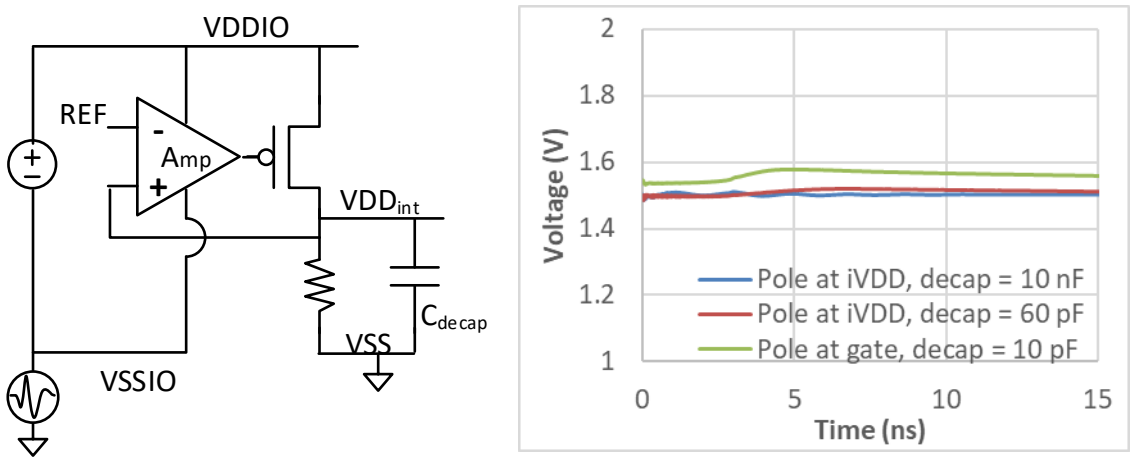


(a)



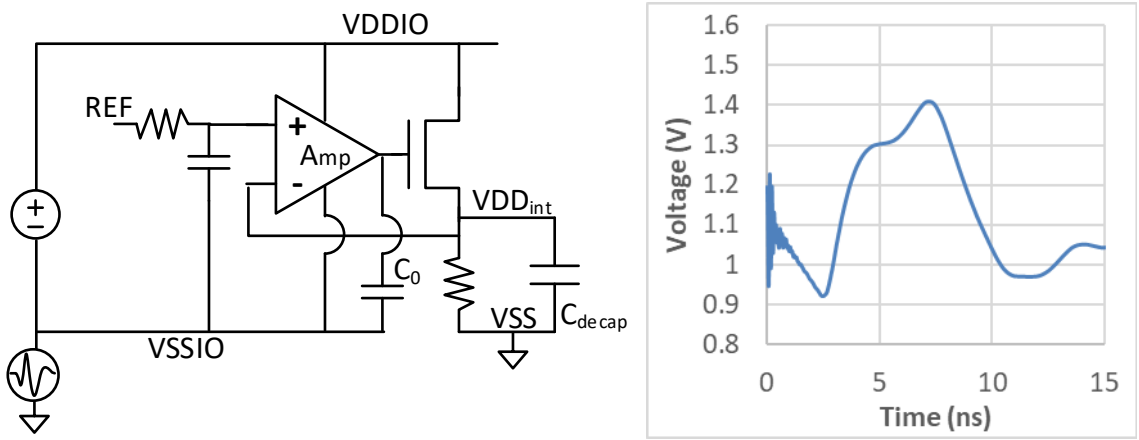
(b)

Figure 6.7: (a) Internally generated power supply subjected to ESD-induced noise $v_c(s)$, including a representation of a generic LDO. L_0 is the sum of the package inductance connected to vdd_{int} and the ESL of the off-chip decap C_0. R_0 is the ESR of the off-chip decap. R_{load} represents the power-consuming circuits in the VDD_{int} domain. (b) Equivalent circuit of the one shown in (a). Since R_{load} is large (several hundred ohms with several mA of operating current), it is neglected in the analysis.



(a) (b)

Figure 6.8: (a) Simulation setup where noise on VSSIO injects supply noise to the VDD_{int} domain with a regulator using a PMOS pass transistor. The design with 10 nF of decap is identical to Design B shown in Section 6.1. (b) The simulated $(VDD_{int} - VSS)$ is generally quiet regardless of the amount of VDD_{int} decap and the pole location of the regulator.



(a) (b)

Figure 6.9: (a) Simulation setup where noise on VSSIO injects supply noise to the VDD_{int} domain with a regulator using an NMOS pass transistor. The design is identical to Design A shown in Section 6.1. (b) The simulated $(VDD_{int} - VSS)$ is significantly affected by the VSSIO noise.

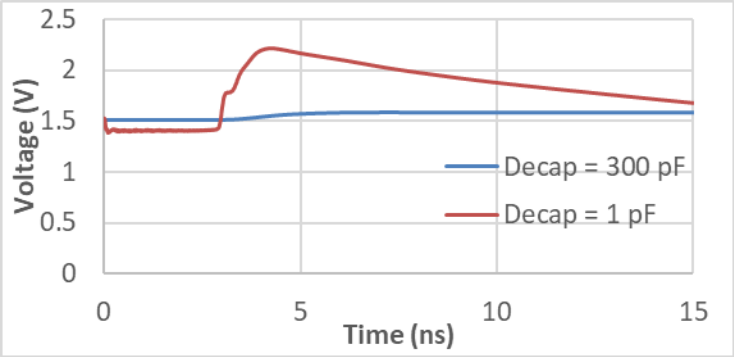


Figure 6.10: Simulated $(iVDD - VSS)$ with a regulator using an NMOS pass transistor in the 130-nm technology. The regulator has its dominant pole at the gate of the NMOS pass transistor.

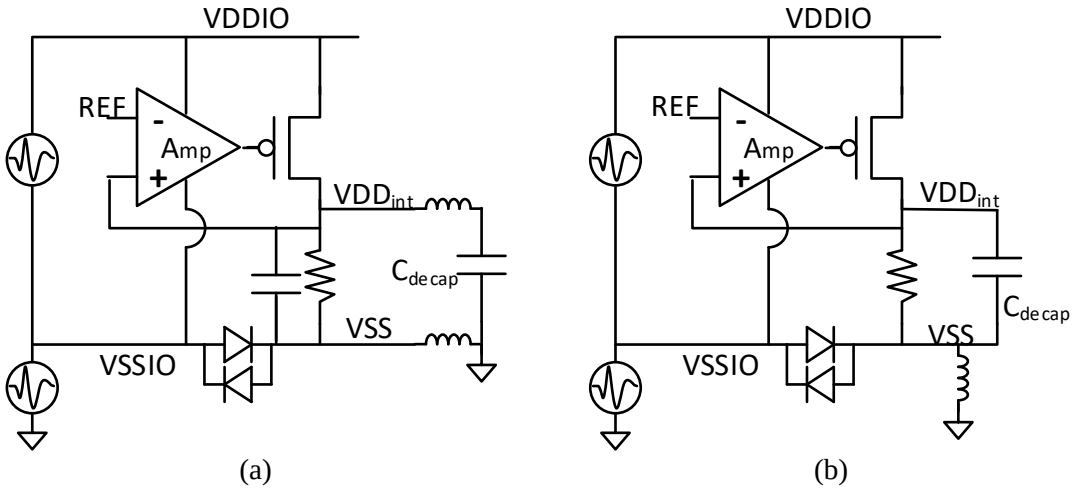
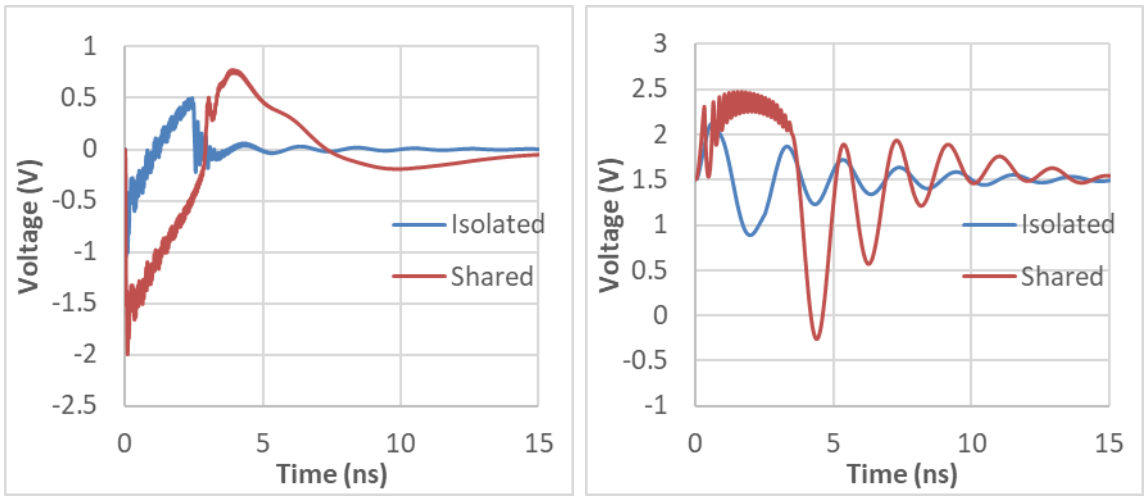
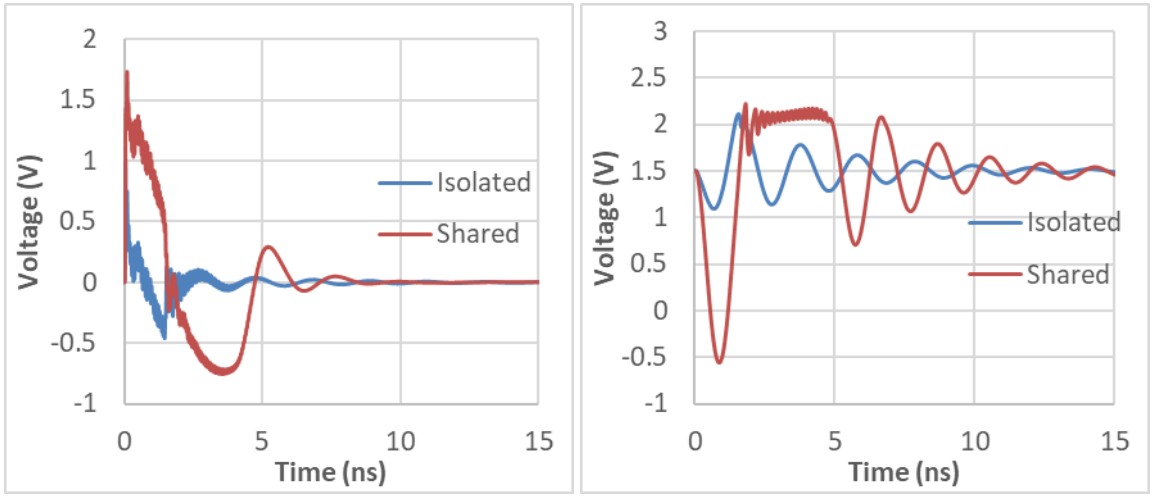


Figure 6.11: Simulation setup where noise in the VDDIO domain injects supply noise to the VDD_{int} domain through a regulator using a PMOS pass transistor (a) with off-chip decap and (b) without off-chip decap.



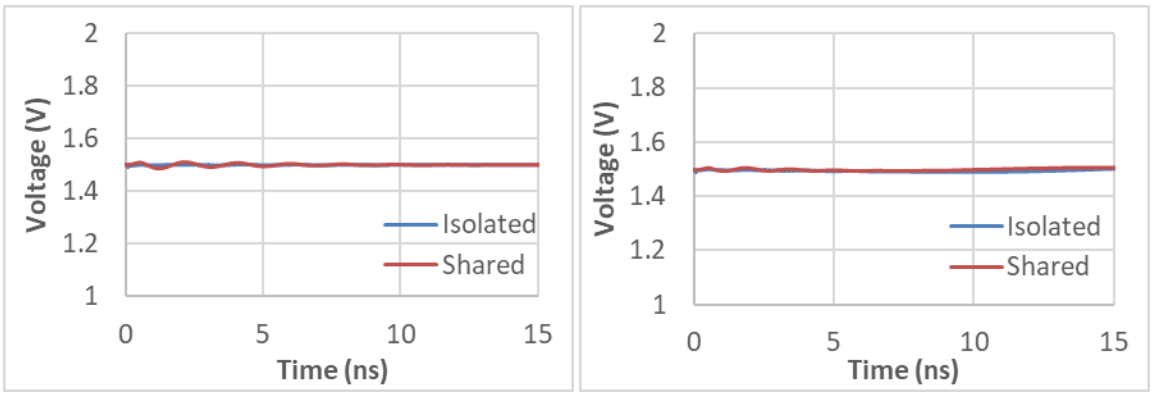
(a) (b)

Figure 6.12: Simulated (a) VSS voltage with respect to the board ground and (b) $(VDD_{int} - VSS)$ voltage when there is noise in the VDDIO domain. The on-chip ground nets are either separated by APDs or shared. The regulator uses a PMOS pass transistor with 10 nF off-chip decap and it is identical to Design B shown in Section 6.1. The noise source voltages are obtained from the simulation of a discharge at -2 kV to an IO protected by dual diodes in the VDDIO domain.



(a) (b)

Figure 6.13: Simulated (a) VSS voltage with respect to reference ground and (b) $(VDD_{int} - VSS)$ voltage when there is noise in the VDDIO domain. The on-chip ground nets are either separated by APDs or shared. The regulator uses a PMOS pass transistor with 10 nF off-chip decap and it is identical to Design B shown in Section 6.1. The noise source voltages are obtained from the simulation of a discharge at +2 kV to an IO protected by dual diodes in the VDDIO domain.



(a) (b)

Figure 6.14: Simulated ($(VDD_{int} - VSS)$ voltage when there is noise in the VDDIO domain. The on-chip ground nets are either separated by APDs or shared. The regulator is identical to the one shown in Figure 6.13 except that it has (a) 10 nF or (b) 60 pF on-chip decap and no off-chip decap. The noise source voltages are obtained from the simulation of a discharge at -2 kV to an IO protected by dual diodes in the VDDIO domain.

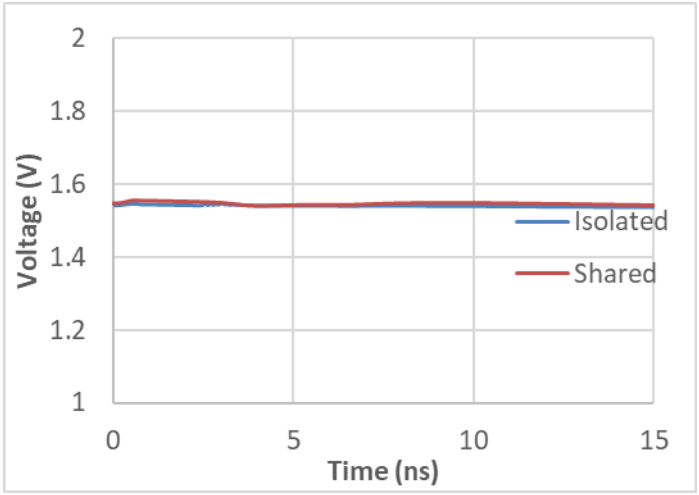


Figure 6.15: Simulated ($(VDD_{int} - VSS)$ voltage when there is noise in the VDDIO domain. The on-chip ground nets are either separated by APDs or shared. The regulator has its dominant pole at the gate of the PMOS pass transistor and the VDD_{int} decap is 10 pF. The noise source voltages are obtained from the simulation of a discharge at -2 kV to an IO protected by dual diodes in the VDDIO domain.

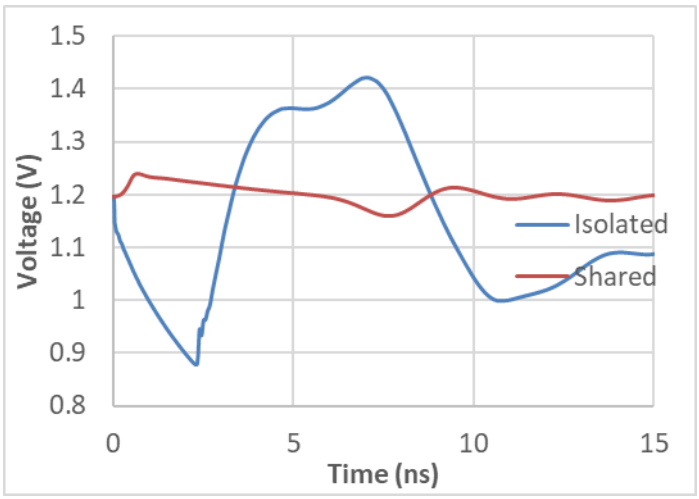


Figure 6.16: Simulated ($VDD_{int} - VSS$) voltage when there is noise in the VDDIO domain. The on-chip ground nets are either separated by APDs or shared. The regulator is identical to Design A shown in Section 6.1 in the 65-nm technology. The noise source voltages are obtained from the simulation of a discharge at -2 kV to an IO protected by dual diodes in the VDDIO domain.

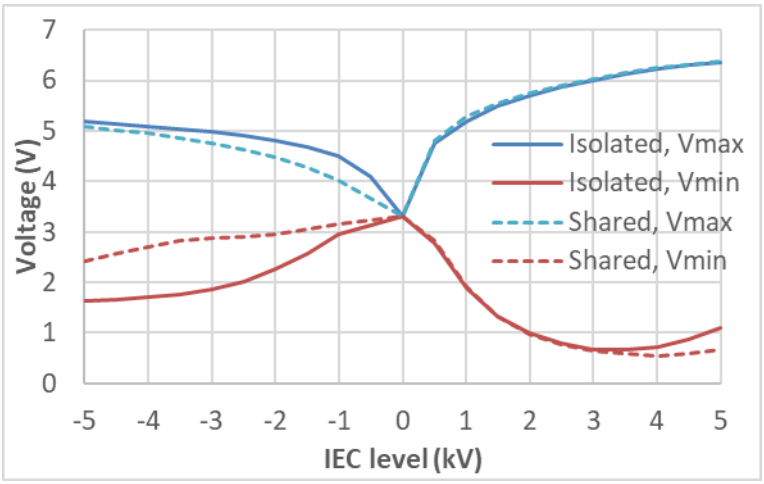


Figure 6.17: Simulated maximum and minimum ($VDDIO - VSSIO$) of the 130-nm test chip with shared or separate VSS on-chip during ESD discharges to an IO protected by dual diodes.

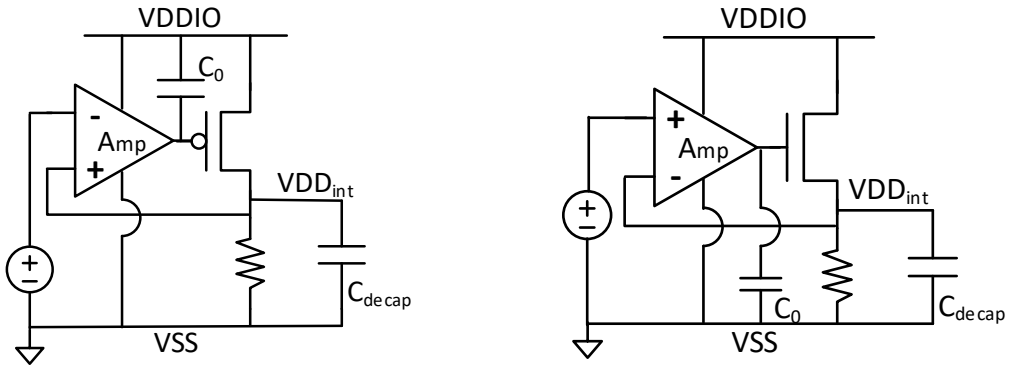


Figure 6.18: Regulators with (a) a PMOS pass transistor and (b) an NMOS pass transistor respond differently to the transient noise of a large amplitude between VDDIO and VSS.

Table 6.2: Properties of the four regulator designs.

Design #	Pass transistor	Dominant pole location	VDD_{int} decap	Max DC current
1	PMOS	Output	300 pF	>10 mA
2	NMOS	Gate	300 pF	>10 mA
3	PMOS	Gate	1 pF	>10 mA
4	NMOS	Gate	1 pF	>10 mA

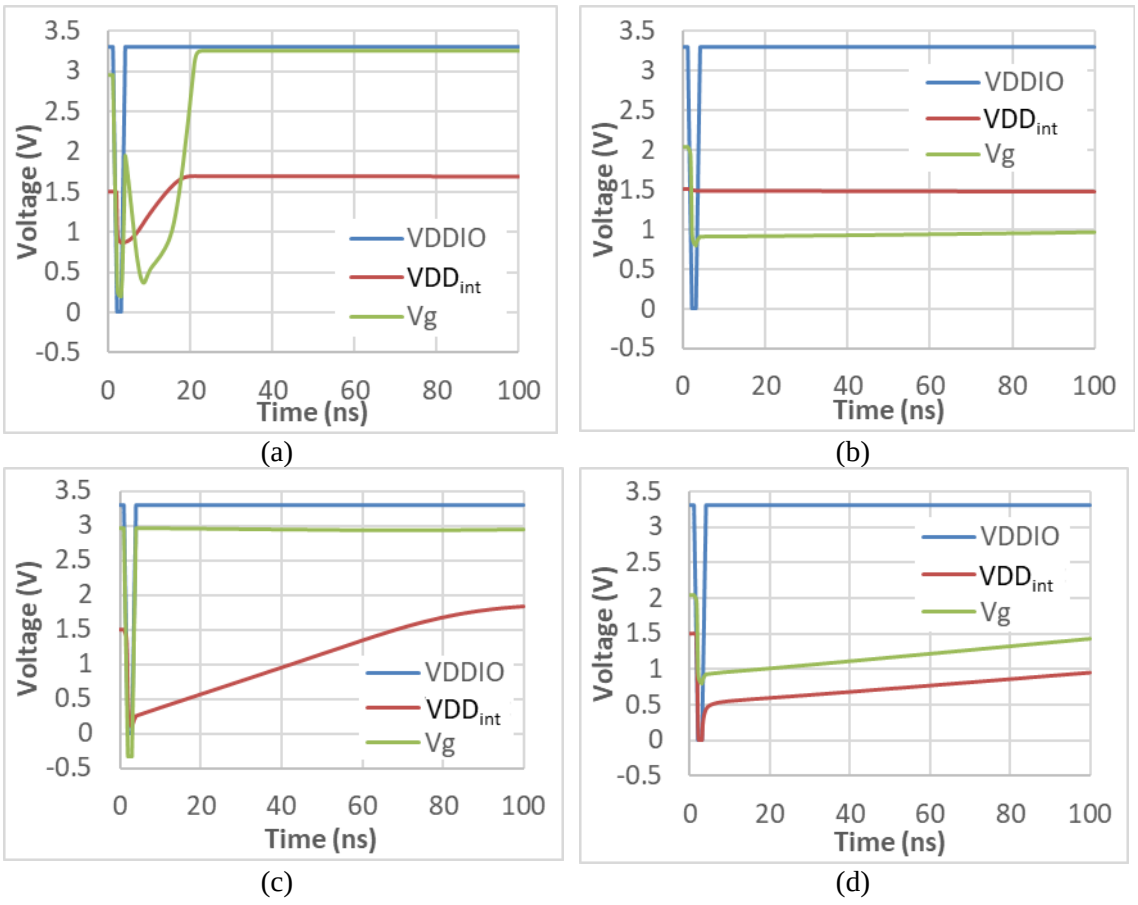


Figure 6.19: (a-d) Simulated supply voltages of the VDD_{int} domain and the gate potentials of the pass transistors in Designs 1-4 during an under-voltage event in the VDDIO domain where its supply voltage drops to 0. V_g is the gate voltage of the pass transistor with respect to VSS.

CHAPTER 7

LATCH-UP CAUSED BY SUPPLY FLUCTUATION

It has been shown in previous chapters that the on-chip supply is significantly disturbed during system-level ESD. A supply reversal can occur and easily cause many circuits to upset. These upsets are very likely to cause soft failures during an IEC test. It may also trigger latch-up, the inadvertent triggering of a parasitic PNPN inherent to CMOS logic circuits. Latch-up may cause hard failures due to the excessive current through the circuits.

7.1 Reverse body bias (RBB)

RBB is a scheme to reduce off-state leakage current in CMOS logic circuits; the NMOS devices have a P-well potential that lies below the ground reference potential (VSS) and/or the PMOS devices have an N-well potential that lies above the supply voltage (VDD). RBB requires additional drivers to generate the well-bias potentials. Because the well-ties are not connected directly to the low-resistance ground or power net, the resistance in parallel with the various well-diffusion PN junctions may be large, which tends to increase the latch-up hazard by increasing base resistances of the parasitic PNP and NPN relative to those in the circuits without RBB.

Figure 7.1 illustrates the parasitic PNPN associated with the CMOS logic. If the base-emitter junction of the PNP or NPN becomes forward-biased, positive feedback ensues and the PNPN may transition from its blocking state to its low-impedance on-state. The supply and ground potentials are disturbed during ESD, as shown in Chapter 4; this may cause one or both PN junctions to become forward-biased. Additionally, ESD at an IO pad produces large substrate currents. If the N-well of the PNPN is able to collect the excess minority carriers from the substrate, this may provide the base current needed to turn on the PNP; if the P-well of the PNPN is able to collect the excess majority carriers from the substrate, this may provide the base current needed to turn on the NPN [55].

On the 130-nm CMOS test chip, RBB was implemented in several separate power domains. Charge pump circuits generate the well biases; a mux allows the user to select between zero and non-zero body bias. The well bias scheme is pictured in Figure 7.2. The supply voltage VDD_{int} is generated by an on-chip LDO. The test chip contains five separate VDD_{int} supplies (VDD_{int1} through VDD_{int5}); each uses an identical LDO design. VDD_{int} is set to 1.5 V. The test chip also contains pins for an externally generated 1.5 V supply, denoted VDD_{ext}.

The body-bias generator circuits are shown in Figure 7.3. When RBB is not activated, both clk_1 and clk_2 are at logic low; when RBB is activated, the clocks toggle as shown in the timing diagram of Figure 7.4. When RBB is activated, $V_{nwell} = 2.5$ V and $V_{pwell} = -1$ V.

In this dissertation, RBB is applied to both PMOS *and* NMOS devices; this requires that an isolated P-well structure be used. The process technology utilized in this dissertation provides a true triple well T3, as illustrated in Figure 7.5. During ESD, holes

or electrons can be injected into the chip substrate, depending on the polarity of the ESD current and the type of IO protection circuit. The N-well and P-well of Figure 7.5 are isolated from substrate currents.

Intentional PNPN devices were placed in supply domains VDD_{int1} through VDD_{int5} and in the VDD_{ext} domain. The PNPN layout is shown in Figure 7.6. Table 7.1 provides details of the well biasing schemes and latch-up test circuits for each of the supply domains. In some cases, the wells are biased at VDD_{ext} and VSS through muxes with variable size (i.e., pass transistors of varying width); this was intended to show whether the resistance from the bias generator to the NPN/PNP base region is an important factor in latch-up sensitivity. The minimum-sized mux has a PMOS pass transistor with an equivalent resistance of 430 Ω and an NMOS pass transistor with an equivalent resistance of 140 Ω.

An IEC 61000-4-2 ESD gun was discharged into a variety of IO pins on the test chip; if the quiescent current has increased following the test, it is likely that latch-up has occurred. For ESD discharges up to ±5 kV, no increase in the dc operating current was observed when the test was performed at room temperature. Next, the chip temperature was increased by aiming a hot-air gun at the socket holding the test chip. Since the plastic socket covers the entire IC and the chip is encapsulated in a plastic package, the on-die temperature cannot be directly measured. Measurement with a thermocouple indicated that the top of the socket was at approximately 100 ^{0}C and the side of the socket was at approximately 70 ^{0}C. Latch-up could be observed when the hot-air gun was used; all subsequent data were obtained at the elevated temperature.

The symptom of latch-up was a 20 mA increase in the DC operating current. When the current increase occurred, the active VDD_{int} supply was measured to be at around 1.2 V instead of the normal 1.5 V; VDD_{int} is measured at an (ESD-protected) pin connected to this bus. Based on the characteristics of the on-chip LDO, such a voltage droop is expected to occur when the current drawn by VDD_{int} is larger than can be sourced by the LDO. The DC operating current returns to normal when this VDD_{int} domain is powered-off. All these observations indicate that latch-up has occurred in VDD_{int}. Latch-up was not observed in the VDD_{ext} domain.

Table 7.2 lists the ESD levels needed to trigger latch-up. These are the worst-case results, found for the case of a negative ESD into an IO pin that is next to a VDD_{int} pin (and this particular VDD_{int} is active during the ESD test). In fact, when the IO pin being discharged to is farther away from the VDD_{int} pin, latch-up did not occur. In these experiments, latch-up was not significantly affected by the mux size, mux location, or whether the system is tethered or mobile. As expected, increasing the well-tie density, which reduces the base resistance, prevents latch-up from occurring. Applying a reverse bias to the P-well improves robustness against latch-up; this is not unexpected since it makes the parasitic NPN in the PNPN structure (see Figure 7.1) harder to turn on. However, applying a reverse bias to the N-well did not have a significant effect.

Whether the system is tethered or mobile has no discernible effect on the ESD level needed to trigger latch-up; this observation allows us to rule out substrate carrier injection as the cause of latch-up [55], because a far larger amount of substrate carriers is injected in the tethered case. Nor did the mux size play a major role, whereas increasing the well tie density did impact the latch-up immunity. This suggests that the mux does not

significantly contribute to the base resistance of the test structures; this finding is unexpected and requires further investigation. The data show that circuits in the internally generated power domains on this chip are susceptible to latch-up whereas those in the externally generated power domain are not.

Circuit simulation was used to examine the noise induced on the supply and well bias buses during ESD. As shown in Figure 7.7, simulation of an ESD discharge to an IO pin of the test chip reveals that both VDD_{ext} and VDD_{int} are significantly disturbed. The supply noise is caused by the "$L\frac{di}{dt}$" effect as described in Chapter 4. In the case that $EN\_BBG = 0$, the well bias voltage is VDD_{ext}. If VDD_{ext} is lower than VDD_{int} when both quantities are positive, the parasitic PNP of the PNPN connected to VDD_{int} can turn on and trigger latch-up. Simulation indicates that VDD_{int} exceeds VDD_{ext} by a significantly larger amount for negative discharges, explaining why latch-up was observed only for negative ESD.

For this test chip, it is claimed that the noise on the supply voltage triggers latch-up and that the substrate current does not. This assertion is confirmed by TLP measurements; the square pulses have a slower rise-time (10 ns) than the IEC pulses but a longer duration, so more substrate carriers are injected. No latch-up was observed at elevated temperatures for 50 ns long pulses up to ±9 A, 100 ns long pulses up to ±5.5 A, and 200 ns long pulses up to ±4 A.

It was shown in [56] that PNPN structures with the layout shown in Figure 7.6(b) have a higher holding voltage than those with the layout of Figure 7.6(a) and thus are less likely to latch-up, which is consistent with the observation that VDD_{int5} never latched up. However, it must also be noted that VDD_{int5} is the only domain listed in Table 7.1 that

does not have an IO pin where ESD current can be injected directly adjacent to its VDD_{int} pin. In the cases of VDD_{int1} through VDD_{int4}, the bond wires for the "zap pin" and the VDD_{int} pin are parallel to one another. Instead, for VDD_{int5}, the zap IO pin and the VDD_{int} pin are on either side of a corner and are thus perpendicular to each other. The larger inductive coupling between parallel bond wires induces more current into the power domain at the leading edge of the negative ESD current pulse. This additional current leads to a larger difference between the supply and N-well bias potentials, as shown in Figure 7.8, between 3 ns and 5 ns.

According to Table 7.2, the minimum IEC levels to trigger a latch-up in VDD_{int4} are not sensitive to whether the RBB on the N-well bias voltage, V_{nwell}, is activated or not. The circuit is more robust with the activation of RBB on the P-well bias voltage. This suggests that there is differential-mode noise between VDD_{int} and the N-well bias voltage, V_{nwell}. This result may be understood as follows. The charge pump cannot quickly respond to the nanosecond-scale supply voltage fluctuations so the generated N-well bias remains relatively quiet, however the voltage difference between the noisy VDD_{int} and quiet V_{nwell} can be large enough to trigger latch-up. For this test chip, the voltage margin between V_{nwell} and VDD_{int} is reduced during latch-up testing, because the elevated ambient temperature leads to an increased leakage current. Since the charge pump circuit can provide only a limited amount of bias current, at the elevated temperature, the charge pump circuit generates a somewhat reduced output voltage. The simulation result shown in Figure 7.9 confirms that negative discharge to an IO pin causes the quantity $(VDD_{int} - V_{nwell})$ to briefly become positive, potentially triggering latch-up.

7.2 High-voltage tolerant IO

The 130-nm test chip includes a high-voltage tolerant IO test circuit, as shown in Figure 7.10. This circuit is designed to tolerate 3.3 V at the IO pin when it is configured as an input, despite being powered by a 1.5 V supply, VDD. To prevent current injection to the n-wells when the IO is at a higher potential than VDD, the wells of the PMOS transistors are left floating. These n-wells are then always charged to the higher potential between VDD and the IO. With a floating n-well, the circuit may also be more vulnerable to carrier injection to the N-wells, leading to latch-up. The circuit is protected by an SCR for positive ESD, since a diode connecting IO and VDD can turn on during normal operation.

The circuit was stressed up to ±5 kV in the tethered setup under both room and elevated temperature conditions. It was also subjected to TLP pulses up to ±6 A with 100 ns pulse width and ±4 A with 300 ns pulse width; those measurements were performed in the elevated temperature condition. No latch-up was observed in any of these experiments. One of the possible causes is that the holding voltage of the circuit may be higher than the supply voltage at 1.5 V. The IO can be tested at a higher supply voltage to study whether latch up occurs.

7.3 Figures and tables

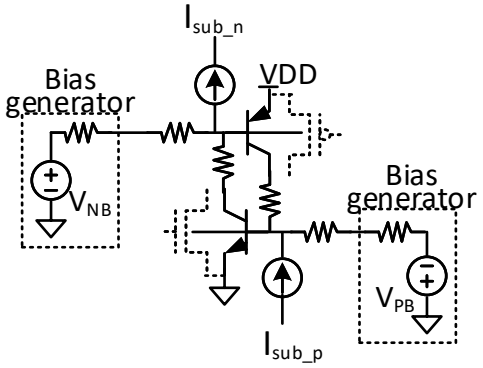


Figure 7.1: RBB scheme and the parasitic PNPN structure. Under normal operating conditions, $V_{NB} \geq$ VDD and $V_{PB} \leq$ VSS. ESD-induced transient supply noise may cause VDD > V_{NB} or VSS < V_{PB}, potentially turning on the PNPN structure. Depending on the process technology, the N-well and P-well in which the MOS transistors are placed may be able to collect minority carrier substrate current (I_{sub_n}) or majority carrier substrate current (I_{sub_p}); the resulting base current may also trigger the PNPN structure.

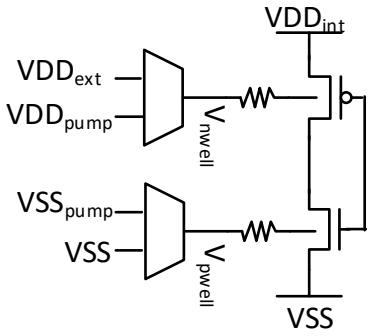


Figure 7.2: Well bias scheme on the test chip.

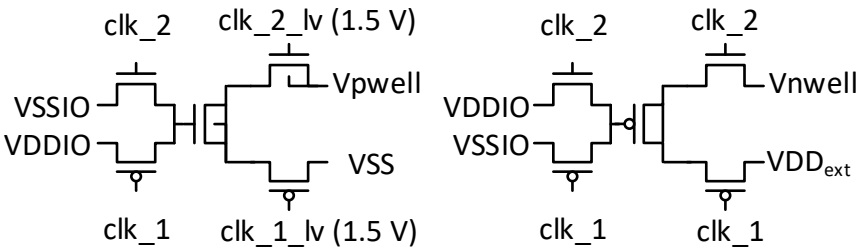


Figure 7.3: Drivers that generate the p-well and n-well bias voltages. *clk*_1_*lv* is a shifted down version (1.5 V) of *clk*_1 with no phase change.

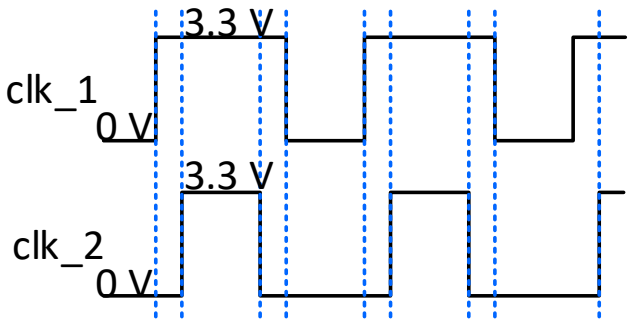


Figure 7.4: Timing diagrams of *clk*_1 and *clk*_2 shown in Figure 7.3. The signals are at 200 MHz.

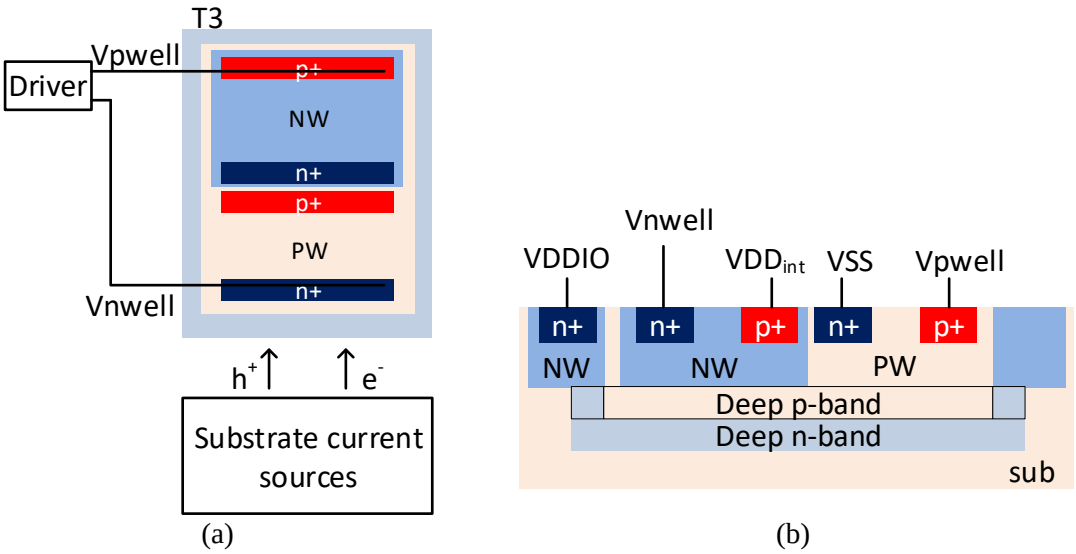
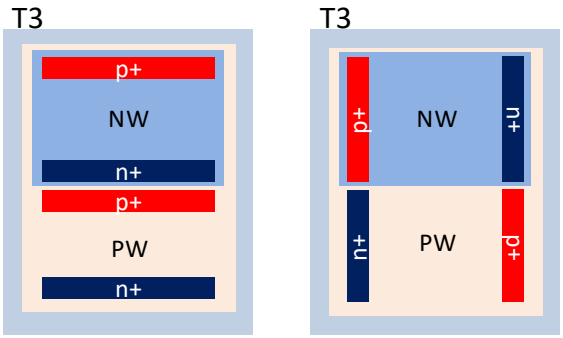


Figure 7.5: (a) Top-view of the RBB test structure layout. (b) Cross section of the test structure in the triple well T3.



(a) (b)

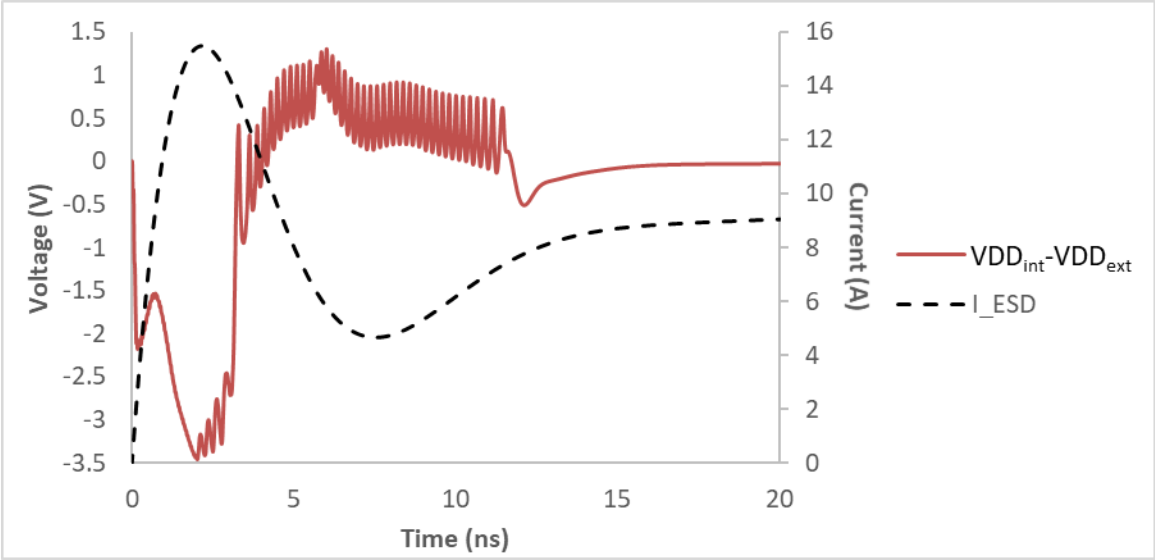
Figure 7.6: Two layout of PNPN structures used in the latch-up test with RBB.

Table 7.1: RBB test structure variations. For structures with an adjustable mux size, the use can select from mux sizes of 1x, 2x, 4x, and 8x. Two PNPN layouts are included; type 1 is shown in Figure 7.6(a), and type 2 is shown in Figure 7.6(b).

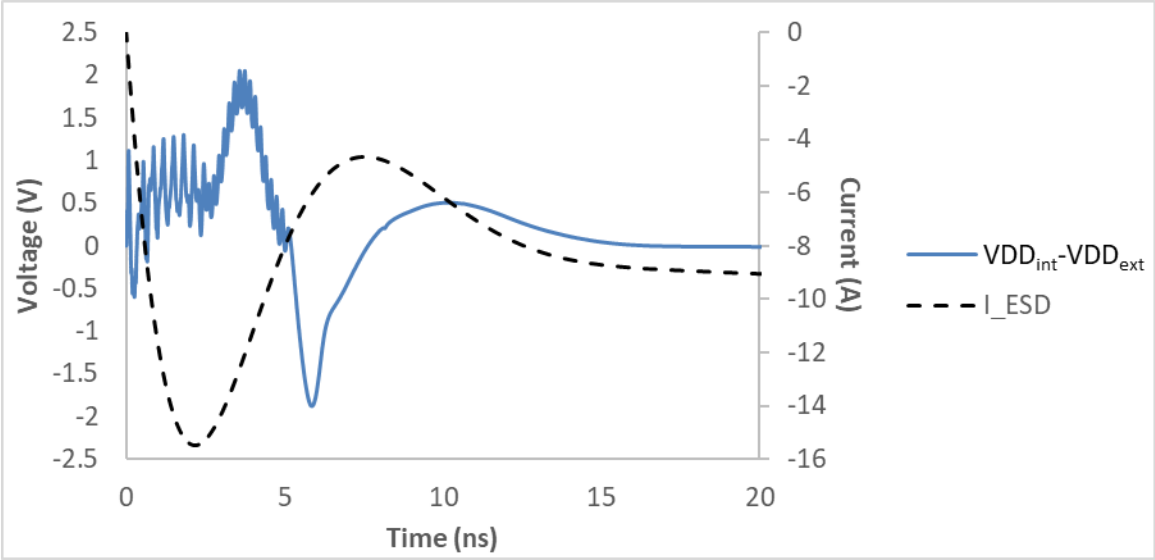
Domain	Bias generator	Mux size	# of muxes	Well tie density	Layout type
VDD_{ext}	None	Adjustable	1	1x	1
VDD_{int1}	None	Adjustable	1	1x	1
VDD_{int2}	None	4x	1	2x	1
VDD_{int3}	None	2x	2	1x	1
VDD_{int4}	PW & NW	4x	1	1x	1
VDD_{int5}	PW & NW	4x	1	1x	2

Table 7.2: Minimum IEC levels (kV) to trigger a latch-up in the specified domain at a lifted temperature. ESD testing is done in steps of 1 kV. Results are shown for negative ESD discharges. None of the positive discharges up to 5 kV caused latch-up.

Domain		Tethered	Mobile
VDD_{ext} (Mux sizes of 1x, 2x, 4x, 8x)		>5	>5
VDD_{int1} (Mux sizes of 1x, 2x, 4x, 8x)		4	4
VDD_{int2}		>5	>5
VDD_{int3}		4	4
VDD_{int4}	No RBB & RBB on NW	4	4
	RBB on PW & RBB on both PW and NW	>5	>5
VDD_{int5}		>5	>5



(a)



(b)

Figure 7.7: Simulated voltage difference between VDD_{int} and VDD_{ext} during (a) +4 kV (b) -4 kV system-level discharges. The circuit board is tethered and k = 0.4, where k is the coupling factor between bond wires connected to the zapped IO and VDD_{int}. If $(VDD_{int} - VDD_{ext})$ is a positive number that exceeds the on-voltage of a PN junction, the PNP in the parasitic PNPN structure (see Figure 7.1) enters its active region and may trigger latch-up. In these simulations, signal EN_BBG is set low (see Figure 7.2); this is the "no RBB" case.

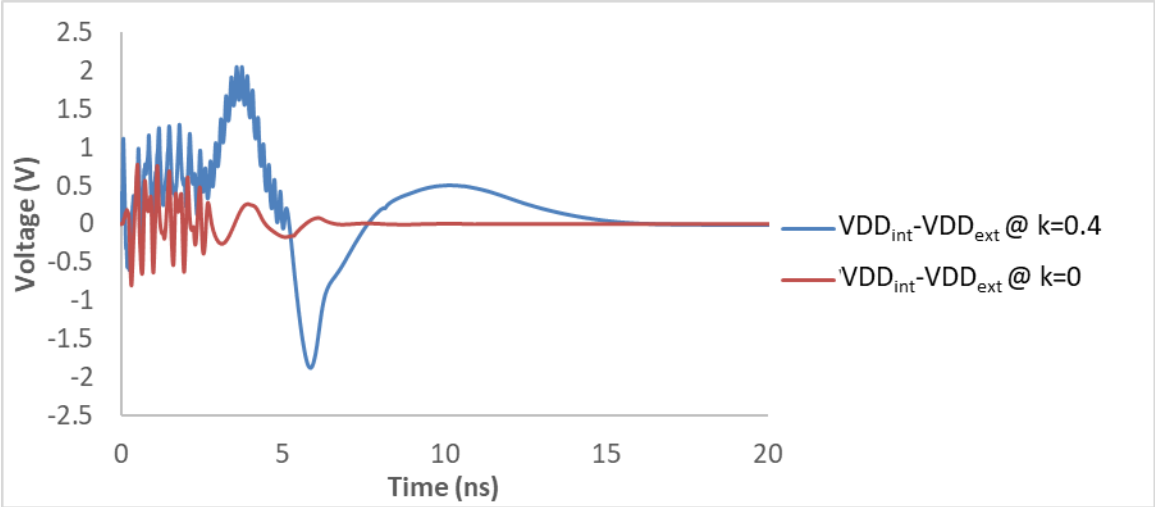


Figure 7.8: Simulated voltage difference between VDD_{int} and VDD_{ext} during a system-level ESD discharge at -4 kV. The coupling factor between bond wires, *k*, is varied in the simulations; *k* is the coupling factor between the bond wires connected to the zapped IO and VDD_{int}.

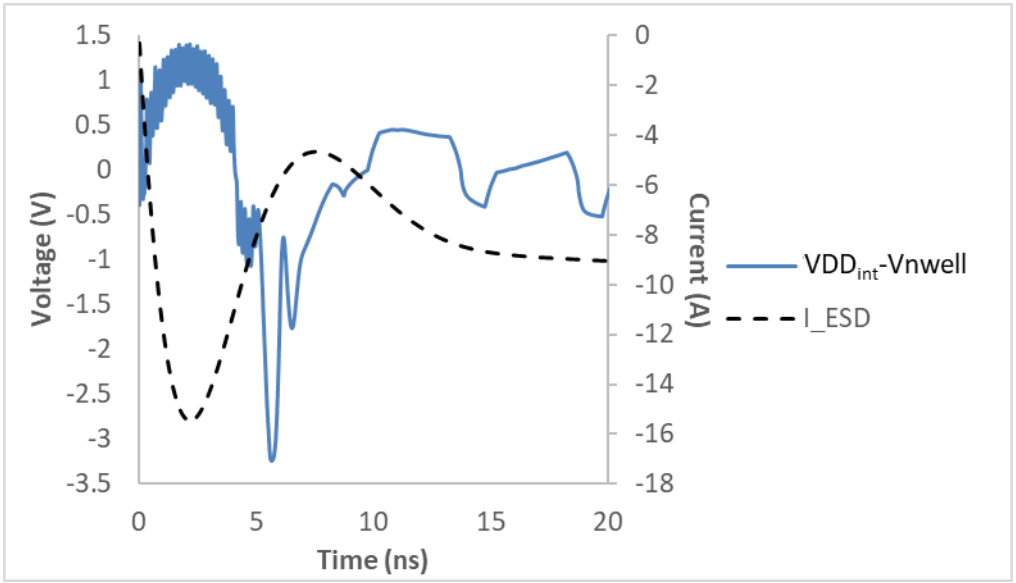


Figure 7.9: Simulated voltage difference between VDD_{int} and the pumped-up V_{nwell} during a system-level ESD discharge at -4 kV to an IO pin. The circuit board is tethered and k = 0.4, where k is the coupling factor between bond wires connected to the zapped IO and VDD_{int}. In simulation, there is a 15 µA leakage current from the N-well. A positive difference between VDD_{int} and Vnwell may turn on the PNP in the parasitic PNPN structure and trigger latchup.

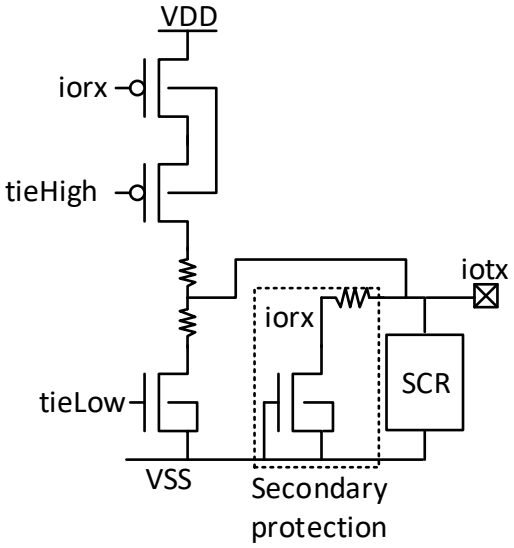


Figure 7.10: Schematic of high-voltage tolerant IO for system-level ESD testing.

CHAPTER 8
MODELING OF AIR DISCHARGE CURRENT

This chapter briefly presents a model for understanding the primary parameters describing an air discharge current pulse. The parameters studied are the peak discharge current and the rise time of this peak.

Air discharges were performed on a simple EUT. The EUT is a 11.8 cm by 5.5 cm sheet of copper laminate positioned 1.5 cm above the HCP with non-conductive plastic stand-offs. The discharges were delivered to the EUT in a mobile setup using the automated tester described in [57]. These discharges are also simulated according to the schematic shown in Figure 8.1. In the mobile setup, the current mainly consists of the discharge of the parasitic capacitance between the gun and its environment. Therefore, the schematic only includes one RC discharge branch. The simulation requires the knowledge of the spark resistance, the model of which is shown below [58].

$$R(t) = \frac{d}{\sqrt{2a \int_0^t i(\zeta)^2 d\zeta}} \tag{8.1}$$

where d is the length of the spark, and i is the discharge current through the spark. a is an empirical parameter in the range between 0.5 m^2/V^2 and 1 m^2/V^2, and in the simulation it is set to 1 m^2/V^2. The simulation assumes that once the spark forms, the discharge will not stop until the potentials across C_{fast} and C_{EUT} are equal.

The spark resistance increases with the spark length, and a larger spark resistance decreases the peak discharge current and increases the rise time of the current pulse. In the measurement, it is observed that the peak current and rise time have a wide variation when the precharge voltage is held constant. This implies that the spark length has a wide variation in the performed air discharges. The varied spark resistance from one discharge to another results in the variation of the peak current and rise time of the current at a fixed precharge level. However, there remains a certain relationship between the two parameters. Figure 8.2 shows the peak current per kilovolt of the precharge voltage with respect to the rise time in the simulation of air discharge at 15 kV. In the simulation, the spark length is varied between 1 mm and 10 mm. The log plot of the two parameters indicates that the simulated results approximately fall on a straight line. Figure 8.3 shows the simulation results where the precharge level is a function of the spark length. This simulation assumes that there is one unique value of the spark length given the precharge level, i.e., there is no variation of the spark length when the precharge level is held constant. The precharge level is derived from the breakdown field between two parallel plates shown below [59].

$$V = Bpd(C + \ln(pd)) \tag{8.2}$$

where B and C are parameters dependent on the composition of the gas, p is the gas pressure, and d is the distance between the plates. For air, B = 365 V/(cm·Torr), and C =1.18. In this dissertation, p is one atmosphere (760 Torr). The log plot of the normalized peak current with respect to the rise time still indicates that the simulated results approximately fall on a straight line. The data obtained from the two simulations can be fit to straight lines that only have a slightly different slope and offset. This implies

that in this setup, all the measurements of the normalized peak current and the rise time, if plotted on the log scale, would fall close to one straight line. The expectation is borne out by the measurement of 3610 discharges [60], and the simulated curves also agree with the measurement results shown in [61].

It should be noted that, when the spark length has a wider range of variation, this relationship may no longer hold true. The slope and offset of the line also tends to change with different EUTs or different setups. C_{EUT} is dependent on the size of the EUT as well as its vertical separation from the HCP. The change in the equivalent capacitance or resistance in the discharge alters the relationship between the peak current and rise time.

8.1 Figures

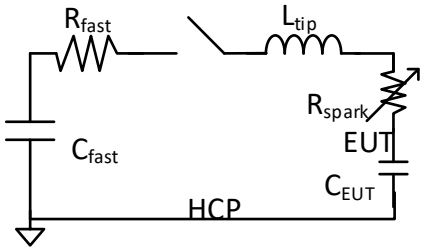


Figure 8.1: Schematic of the circuit to represent an air discharge in the simulation. C_{fast} is precharged to the ESD voltage level. C_{fast} = 12 pF, R_{fast} = 238 Ω, and L_{tip} = 140 nH. For the EUT studied in this chapter, C_{EUT} = 6.3 pF.

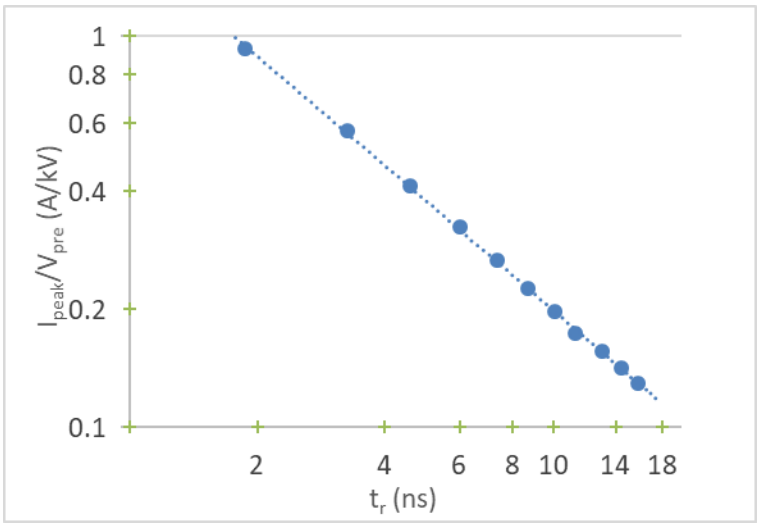


Figure 8.2: Simulated I_{peak} and t_r at 15 kV when the spark length is varied between 1 mm and 10 mm. The simulated points fall very close to the curve $\frac{I_{peak}}{V_{pre}}(A/kV) = 1.688\ t_r(ns)^{-0.9305}$.

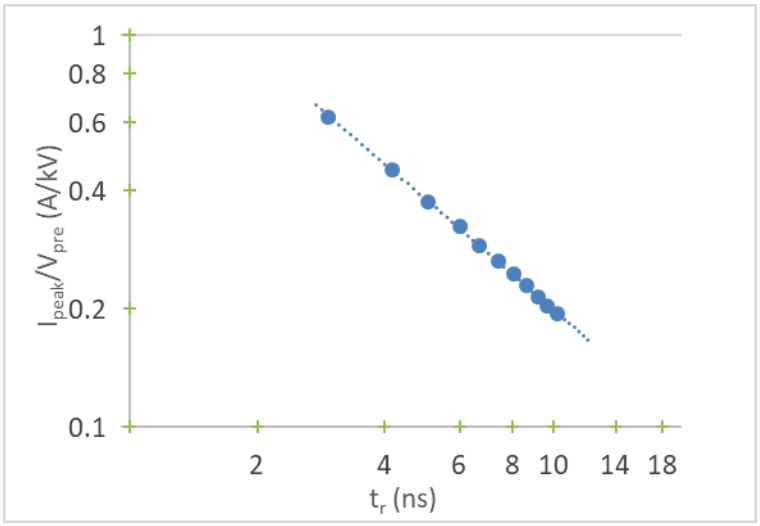


Figure 8.3: Simulated I_{peak} and t_r when the spark length is varied between 1 mm and 10 mm. The precharge level is calculated based on Condition (8.2) given the spark length. The simulated points fall very close to the curve $\frac{I_{peak}}{V_{pre}}(A/kV) = 1.704\ t_r(ns)^{-0.9333}$.

CHAPTER 9

SUGGESTIONS FOR FUTURE WORK

Future exploration of the work shown in this dissertation includes parametric modeling of the ESD current, robust regulator designs against ESD, faster rail clamps against SSN, and improved well bias generators.

This dissertation has used distributed elements to model the contact discharge current for both mobile and tethered configurations, and the simulation and measurement agrees reasonably well with each other. However, it has been observed that the system-level ESD current waveform between 5-10 ns after the first peak is highly dependent on the tether's distance to the other metal parts in the test setup. This dependence creates a significant variation in the corresponding voltage waveform. In order for a simulator to accurately capture the variation when the tether changes its location, further parametric modeling methodology needs to be developed for contact discharge current to an EUT tethered in different ways. Once the injected ESD current and the induced voltages are well-predicted by simulation, proper ESD protections can be developed for the worse case in the design phase. The criteria of the worse case vary, and one tether setup that results in maximum injected energy does not necessarily gives the largest induced voltage.

It remains a question whether it is possible to implement an on-chip voltage regulator that has enough gain and bandwidth to counteract the disturbance caused by the induced voltages on package inductances. Since it is not plausible to completely remove the supply noise induced by ESD for the circuits requesting absolutely quiet supplies, it is worthwhile to show the maximum capability of the on-chip voltage regulators to improve power integrity. In addition, it is proposed to use a shared VSS bus on-chip with the off-chip decap of the internally regulated domain disconnected to the board ground. This proposal needs to be evaluated of its effectiveness to mitigate supply noise during ESD.

Rail clamp may find another application during power-on to mitigate overshoots of the supply voltage due to SSN. Apart from the stability concerns addressed in this dissertation, the rail clamp needs an even faster trigger circuit to accommodate the switching frequency. The trigger circuit can be made faster by reducing the delay to turn on the BigFET or by decreasing the turn-on voltage during power-on.

This dissertation has not shown that the RBB scheme presents a latch-up hazard if the well bias potentials are implemented with reference to its own power or ground potential. When the substrate current increases in a design with a large and dense core circuit, the RBB scheme becomes more vulnerable to latch-up than the experiments shown in this dissertation. In that case, it is worthwhile to investigate the optimal design of the well bias generators to provide the largest possible current with the smallest area without a latch-up hazard during ESD. Latch-up remains a potential hazard for high-voltage tolerant IOs connected to a higher supply voltage than the one used in this dissertation.

CHAPTER 10

CONCLUSION

System-level ESD affects the operation of an IC in many aspects. If the fast-changing current peak in the IEC 61000-4-2 test is injected directly to the IC, it causes most of the problems by corrupting data inputs and threatening on-chip power integrity.

Modeling the discharge current of system-level ESD requires the understanding of the coupling mechanisms in the test bed since the current return path is not clearly defined. The coupling of the gun strap and the EUT's tether to the environment, especially the HCP, needs models with distributed elements and is subject to changes in the setup. A frequency domain measurement of a mock gun tip is very useful to the modeling process.

The data inputs are corrupted by the fast-changing current peak due to the magnetic coupling on the board and in the package. Isolating sensitive traces to those that are subject to ESD is helpful but not sufficient when coupling in the package is significant. TVS can be useful if it responds fast enough to the leading edge of the current peak and shunts most of the ESD current away from the chip.

ICs in wire-bond packages in particular are vulnerable to the fast changing current peak and experience severe supply fluctuations if the amount of on-chip decap is insufficient with respect to required ESD protection level. Supply fluctuations occur in all power domains on-chip regardless of how the stressed IOs are protected and the polarity

of the ESD current. An insufficient amount of on-chip decap leads to similar supply fluctuations for externally and internally generated supplies, if the internally generated one needs a large off-chip decap. An efficient rail clamp mitigates the supply fluctuations in some cases, but may cause higher amplitudes of supply fluctuations in other domains. The rail clamp must be stable when triggered during power-on ESD. These supply fluctuations may lead to global data upsets and latch-up issues. In addition, it is suggested to use separate ground nets on-chip to limit the amplitude of noise coupled from the stressed IO domains to the other domains. A well-bias control circuit is necessary for LDO regulators with PMOS pass transistors to prevent the supply fluctuation of the internally generated domains due to the voltage collapse in the IO domain.

ESD may induce latch-up in circuits using RBB when the well bias circuit is not robust against the supply noise. The well-bias circuit needs to be designed referencing the supply voltage that the circuit with RBB is using so that the differential mode noise between the well-bias voltage and the supply voltage is minimized.

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